



# Finite State Machine

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## I. ABSTRACT

This paper explains a Finite State Machine by deconstructing the decade counter and here we verified the both incrementing decoder from 0 to 9 and decrementing decoder from 9 to 0 using arduino uno.

## II. COMPONENTS

The required components list is given in Table: I., seven segment display is shown in Fig.1, and 7474 D-Flip Flop pin diagram is shown in Fig-2.

Components	Value	Quantity
IC	7474	2
seven segment display		1
Arduino	UNO	1
Jumper Wires		50
Breadboard		1

TABLE I

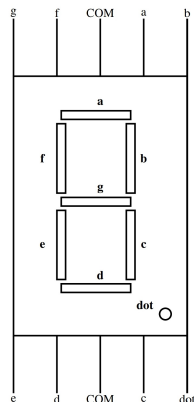


Fig. 1.

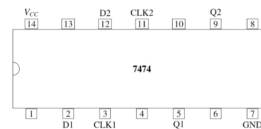


Fig. 2.

## III. PROCEDURE

- 1) Make the connections of arduino, and two 7474 ICs according to Fig-4.

	INPUT					OUTPUT					CLOCK		5V	
	W	X	Y	Z		A	B	C	D		CLK1	CLK2	D13	
Arduino	D6	D7	D8	D9		D2	D3	D4	D5		CLK1	CLK2	1	4
7474	5	9				2	12				1	4	10	13
7474			5	9		2	12				1	4	10	13
7447						7	1	2	6					16

Fig. 3.

- 2) Block diagram of fsm for decade counter

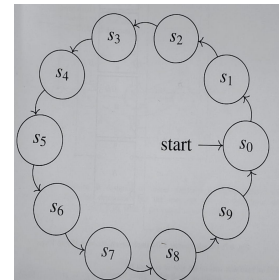


Fig. 4.

- 3) Block diagram of Decade Counter.
- 4) Block diagram of Decade Counter FSM implementation using D-Flip Flops.
- 5) Truth Table for incrementing from 0 to 9 in seven segment display

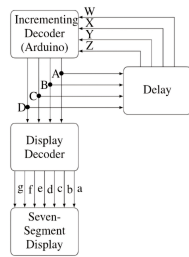


Fig. 5.

Z	Y	X	W	D	C	B	A
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	1	1	1
1	0	0	1	1	0	0	0

TABLE III

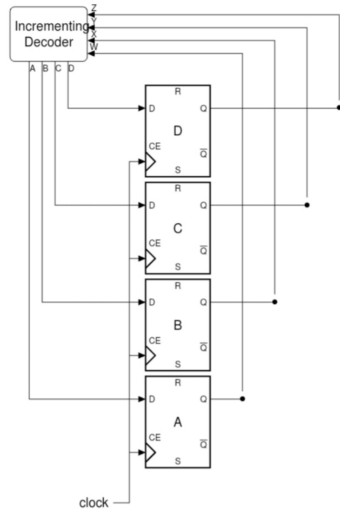


Fig. 6.

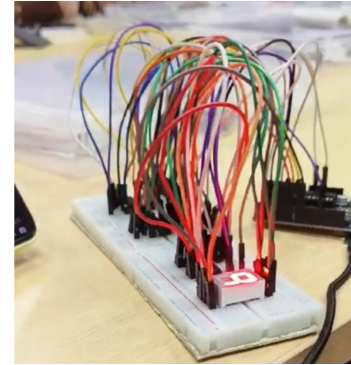


Fig. 7.

## V. CONCLUSION

Hence implementation of 7474 IC Decade Counter on Seven segment display using arduino UNO is done.

- 6) Truth Table for decrementing from 9 to 0 in seven segment display
- 7) Execute the arduino code without any errors.
- 8) After upload the code into hardware setup using arduino IDE platform with hex file.

## IV. RESULTS

- 1) Download the code given in the link below and execute them to see the output as shown in Fig.6,7.
- 2) <https://github.com/patnamkeerthi4545/Fwc/blob/main/Fsm/main.cpp>

Z	Y	X	W	D	C	B	A
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

TABLE II