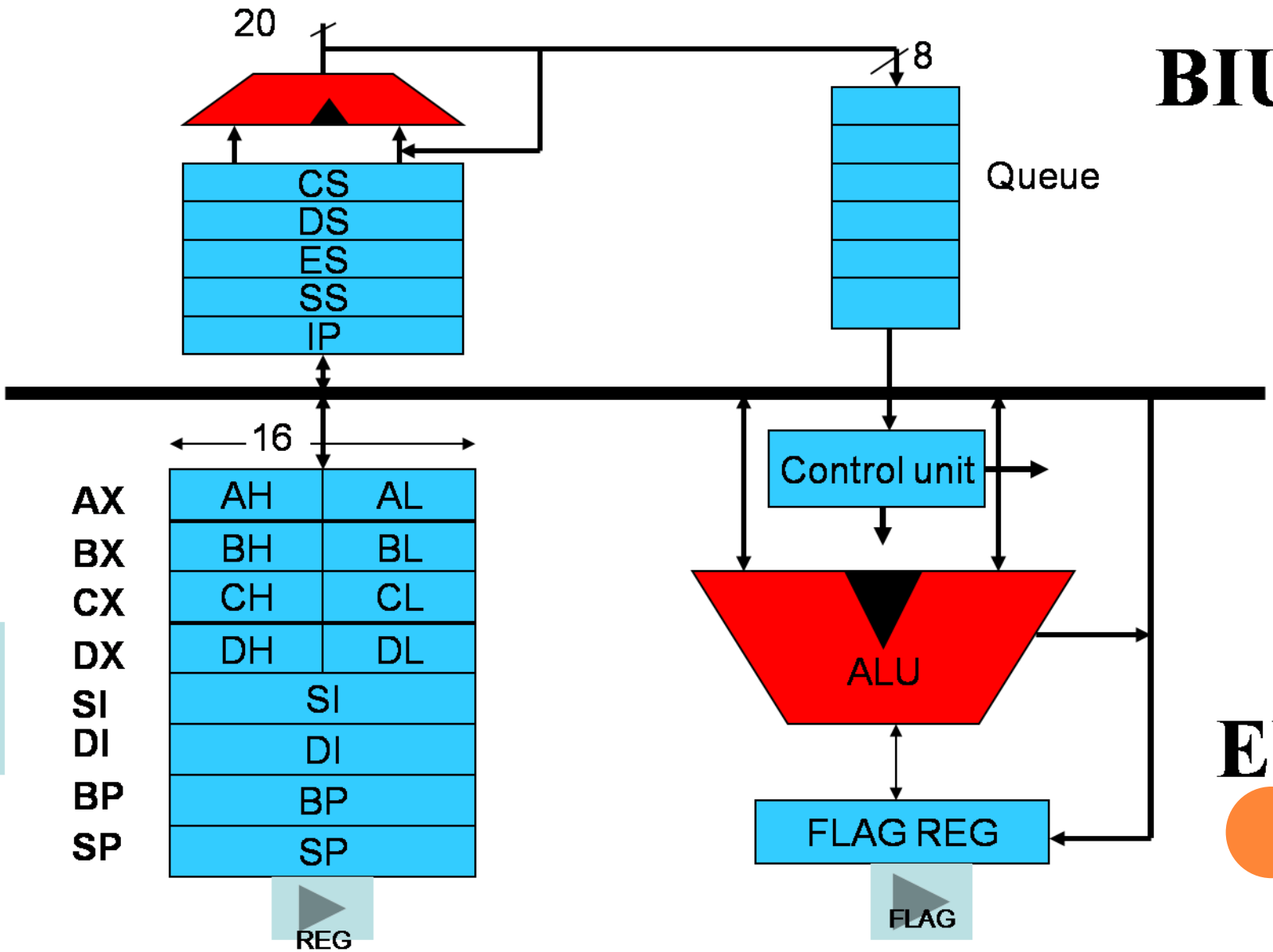
ARCHITECTURE OF 8086 MICRO PROCESSOR

P.RAJESH M.Tech.,
ASST PROFESSOR
DEPT OF ECE
CRIT COLLEGE OF ENGG

8086 Architecture



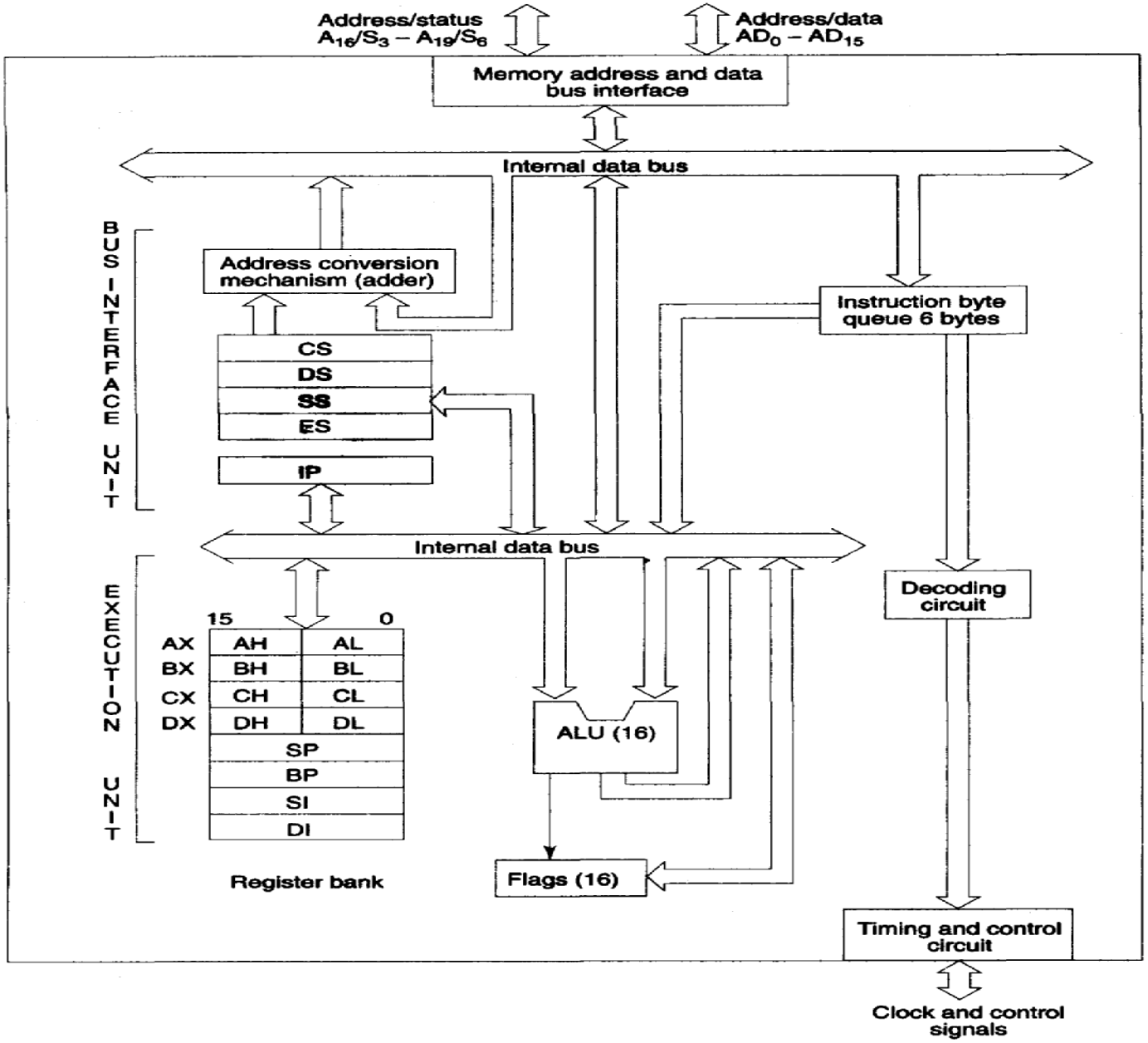


Fig. 1.5 *8086 Architecture*

- 8086 microprocessor has two units;

A) Bus Interface Unit (**BIU**) and

B) Execution Unit (**EU**).

- They are dependent and get worked by each other.

- The 8086 supports 16-bit ALU(Arithematic logical unit)
- A set of 16-bit segmented registers and Registers
- A rich instruction set.
- Has powerful interrupt architecture.
- Feted instruction queue for overlapped fetching and execution
- The 8086 mp's a 16-bit internal and external data bus with 20 address lines it can access.

Bus Interface Unit :

- As the EU has no connection with the system Busses, this job is done by BIU.
- BIU and EU are connected with an internal bus.
- BIU connects EU with the memory or I/O circuits.
- It is responsible for transmitting data, addresses and control signal on the busses.

- BIU contains the circuit for physical address calculations (ADDER)
- pre decoding instructions byte queue
- Segment registers
- Instruction pointers

Function of BIU

- The BIU handles all interfaces with external bus and generates external memory and I/O address.
- BIU reads the data from memory and ports and write data in to memory and ports .
- fetches instructions codes from the memory and keeps them in to 6-byte instruction queue.
- In case of jump and call instruction the BIU dumps the queue and then starts reloading it from new address.

ADDER

- The 8086 mp's address a segmented memory .
- The complete Physical Address (PA) which is 20 bits long is generated using segment and Offset register.

- For generating PA from contents of two register segment & Offset , the content of segment register which is called segment address is shifted left bit wise 4-times

- The content of Offset address is also called Offset address

- Offset address is added to 4-bit shifted segment address to produce Physical address(PA)
- Example:-
- If segment address is 1005H
- Offset address is 5555H
- PA= ?
- Calculated as
- Segment address-→ 1005H = 0001 0000 0000 0101
- shifted 4-bit position →
  - 0001 0000 0000 0101 0000

OA → 5555H = 0101 0101 0101 0101

  - PA= (4-bit shifted SA)+ OA
  - PA= 155A5 H

- The segment register indicates the base address of particular segment .
- The offset register indicates the distance of required memory location in segment from base of address.
- the segment address by segment value 1005H can have Offset from 000H to FFFFH with in it .ie 64Kbyte location may be accommodated in segment.
- since offset is a 16-bit number each segment can have a maximum 64Kb locations .

Instruction Queue

- BIU contains an instruction queue.
- When the EU executes instructions, the BIU gets up to 6 bytes of the next instruction and stores them in the instruction queue and this process is called instruction pre fetch.
- This is a process to speed up the processor.
- A subtle advantage of instruction queue is that, as next several instructions are usually in the queue.
- This means that slow-memory parts can be used without affecting overall system performance.

- Queue is 6-bytes long FIRST-IN-FIRST OUT structure.
- The instruction from the queue are taken for decoding sequentially.
- Once a byte is decoded , the queue is rearranged by pushing it out and the queue status is checked for possibility of next op-code fetch cycle.

Execution Unit (EU) :

- Execution unit receives program instruction codes and data from the BIU, executes them and stores.

- the results in the general registers. It can also store the data in a memory location or send them to an I/O device by passing the data back to the BIU.
- This unit, EU, has no connection with the system Buses. It receives and outputs all its data through BIU.

ALU (Arithmetic and Logic Unit) :

- The EU unit contains a circuit board called the Arithmetic and Logic Unit.

- The ALU can perform arithmetic, such as, +,-,×,/ and logic such as OR, AND, NOT operations.

Registers

- A register is like a memory location where the exception is that these are denoted by name rather than numbers.
- It has 4 data registers, AX, BX, CX, DX .
- 2 pointer registers SP, BP and
- 2 index registers SI, DI and
- 1 temporary register and
- 1 status register FLAGS .

- AX, BX, CX and DX registers has 2 8-bit registers to access the high and low byte data registers.

- The high byte of AX is called AH and the low byte is AL. Similarly, the high and low bytes of BX, CX, DX are BH and BL, CH and Cl, DH and DL respectively.

- All the data, pointer, index and status registers are of 16 bits.

- Else these, the temporary register holds the operands for the ALU and the individual bits of the FLAGS register reflect the result of a computation.

- BIU has 4 segment busses, CS, DS, SS, ES. These all 4 segment registers holds the addresses of instructions and data in memory.
- These values are used by the processor to access memory locations.
- It also contain 1 pointer register IP. IP contains the address of the next instruction to executed by the EU.

Flags

- 8086 has a 16-bit flags register. Nine of these condition code flags are active, and indicate the current state of the processor: Carry flag (CF), Parity flag (PF), Auxiliary carry flag (AF), Zero flag (ZF), Sign flag (SF), Trap flag (TF), Interrupt flag (IF), Direction flag (DF), and Overflow flag (OF).