

DIGITAL INTEGRATED CIRCUITS ANALYSIS

ELECTRONICS & COMMUNICATION ENGINEERING

unit-2

HAND NOTES

BY:

P.RAJESH M.TECH.,

ASSISTANT PROFESSOR

EMAIL: rajesh.crit@gmail.com

ph: 9989786119

9985786099

CRIT COLLEGE OF ENGG & TECHNOLOGY

ANANTAPURAMU

Unit - 2

(1)

Bipolar logic and interfacing:-

Bipolar logic families use semi-conductor diodes and bipolar junction transistors as the basic building blocks of logic circuits. The simplest bipolar logic family consists of resistors and diodes.

1) Diode logic :- (D) (d) Diode resistor logic:-
Constructs boolean logic gates from diodes acting as electrically operated switches.

While diode logic has the advantage of simplicity, the lack of an amplifying stage in each gate limits its application and not all the logical functions can be implemented in diode logic alone only the non-inverting logical AND and OR functions can be realized by gates.

a) AND-Gate:-

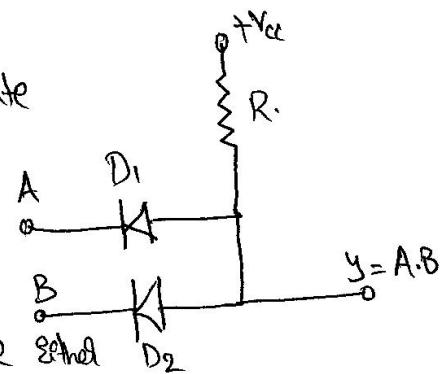
In logic building of 2¹p AND gate using diode logic. The 9¹p are labelled A and B while the dp Y.

Let us assume Supply voltage V_{cc} of 5V.

Also we assume that 9¹p voltages are either 0(V) or +5V (High).

Case 1:- A is low and B is low:- When both 9¹p voltages are low the cathode of each diode is grounded. Therefore positive supply forward-biases both diodes in parallel. Because of this the dp voltage is ideally zero.

Case 2:- A is low and B is high:- When A is low upper diode is forward biased (on) and it pulls the dp down to low voltage 0(V). With the B 9¹p high the lower diode gets reverse bias (off)



Case 3:- A is high and B is low :- Because of the symmetry the circuit operation is similar to Case 2. But in this case upper diode is reverse biased (off), lower diode is forward biased (on), and Y is low.

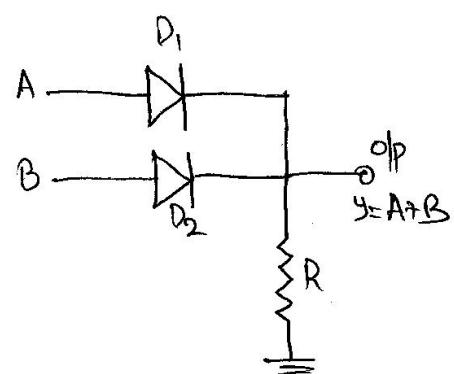
Case 4:- A is high and B is high :- When both op's are +5V both diodes are reverse biased and there is no current through diodes and Resistor R. This pulls up the op Y to supply voltage therefore Y is high.

A	B	D ₁	D ₂	op
0	0	F	F	0
0	1	F	R	0
1	0	R	F	0
1	1	R	R	1

(0 (low) \rightarrow forward)
1 (High) \rightarrow Reverse)

2) OR-Gate :-

The op's voltages sources are connected to A and B. Diode anodes and diode cathode are joined to op, which is connected through the pull down resistor 'R' to the ground.

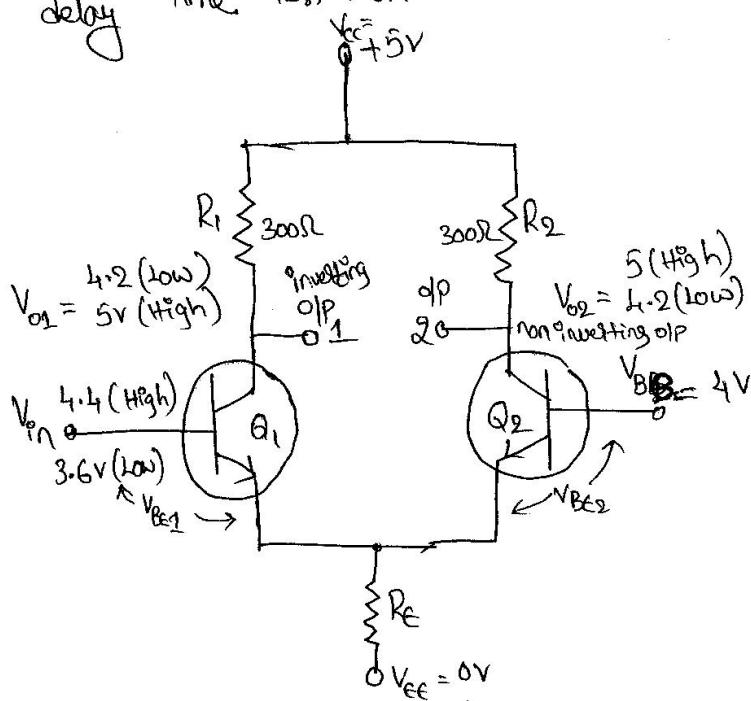


A	B	D ₁	D ₂	op
0	0	F	F	0
0	1	F	R	1
1	0	R	F	1
1	1	R	R	1

(3)

① Emitter Coupled Logic :- Look family:-

ECL gate is fastest gate of all logic families and is employed in applications where very high speed is essential. Among the ECL families, look series is fastest one with a propagation delay time less than 1ns.



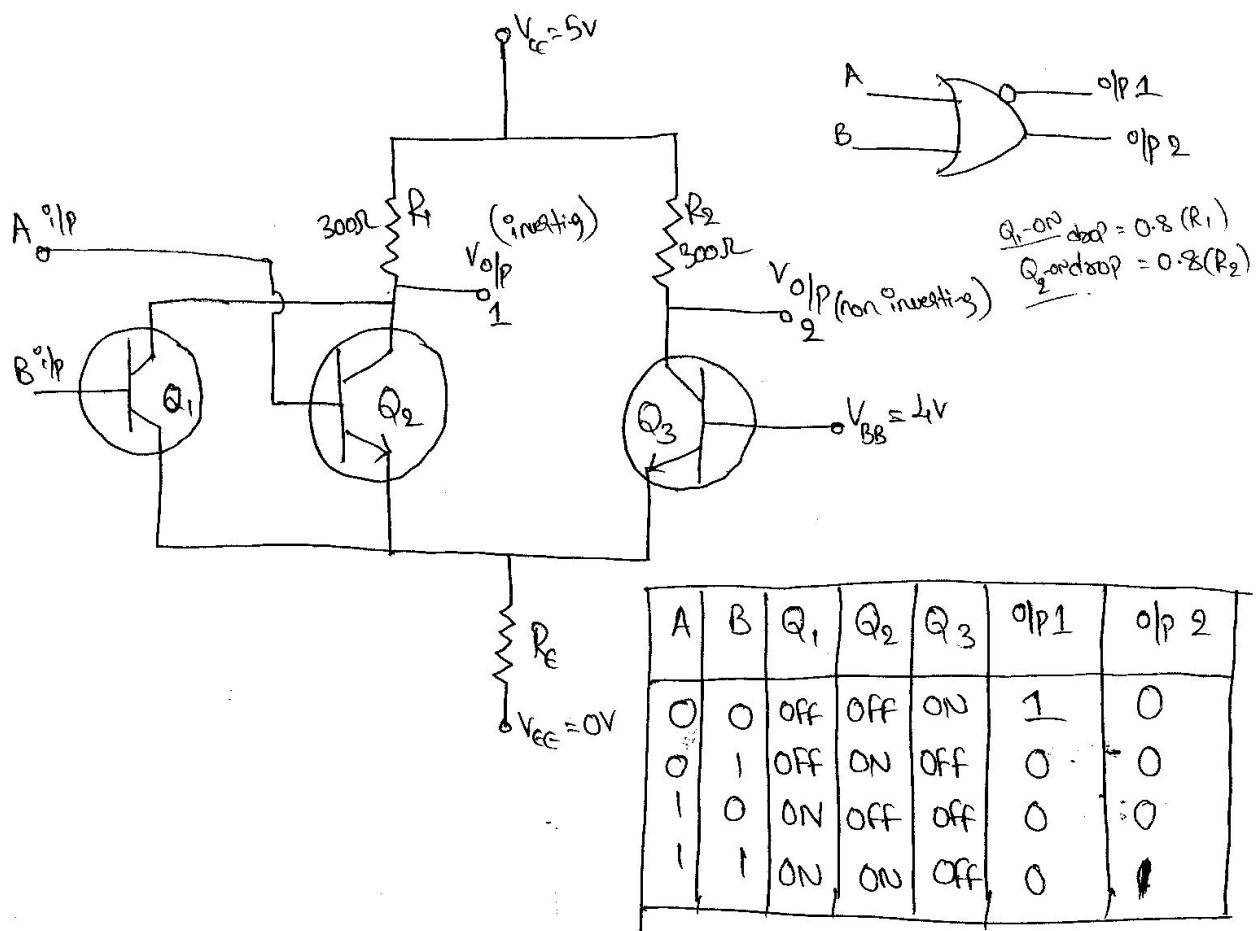
- * The ECL inverter/Buffer circuit has both inverting and non inverting o/p's.
- * It consists of two transistors connected in differential amplifier single ended input mode with a common emitter resistor.
- * Power supply voltages are $V_{cc} = 5V$; $V_{BB} = 4V$; $V_{EE} = 0V$.
- * When $V_{in} = 3.6V$ (Low), transistor Q_1 is off state and its collector potential is nearly equals to $+V_{cc}$, where Q_2 is ON through R_1 and drop across $R_2 = 0.8V$. $V_{O1} = 5V$ (High)

(4) When V_{in} is High (4.4V) transistor Q_1 is ON, but not saturated and transistor Q_2 is OFF. Thus V_{o2} is pulled to 5V (High) through R_2 and drop across R_1 is 0.8V so we get $V_{o1} = 4.2V$ (Low)

$$V_{o2} = 4.2 \text{ (Low)}$$

\circ/p voltage	\circ/p	Q_1	Q_2	\circ/p 1 inverter	\circ/p 2 buffer
3.6V	Low	OFF	ON	High (5V)	Low (4.2V)
4.4V	High	ON	OFF	Low (4.2V)	High (5V)

(2) Emitter Coupled logic NOR OR gate :-



24/7/13

Two input 10K ECL NOR/OR circuit

(5)

The figure shows the 10K ECL 2*I*/P OR/NOR gate

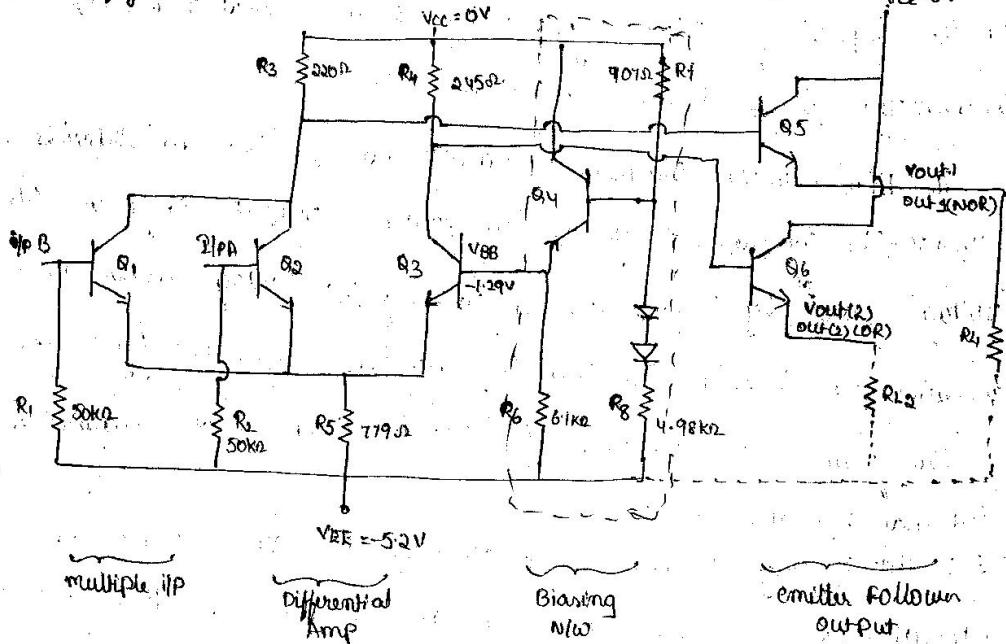


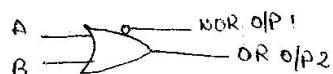
Fig: Two i/p 10K ECL NOR/OR gate circuit

Inputs		Transistors				Outputs		
A	B	Q ₁	Q ₂	Q ₃	Q ₅	Q ₆	Output 1 NOR O/P	Output 2 OR O/P
0	0	OFF	OFF	ON	ON	OFF	High	Low
0	1	OFF	ON	OFF	OFF	ON	Low	High
1	0	ON	OFF	OFF	OFF	ON	Low	High
1	1	ON	ON	OFF	OFF	ON	Low	High

Function Table

Inputs		NOR O/P	OR O/P
A	B	1	0
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Truth Table



Logic Symbol

c) circuit has two additional components i) Bias network and ii) complementary emitter follower pair. The pull down resistors are provided at the inputs of OR/NOR gate. They ensure that if the input is unconnected it is treated as low.

The bias network component values are selected to provide $V_{BB} = -1.29V$. The complementary emitter follower output shift the O/P down by 0.6V matching I_P and O/P voltage levels and increases the current sourcing capacitor. As shown in figure the emitter follower circuit used in ECL 10k circuit does not require an external pull down resistor.

ECL 10k family operates with $V_{CC} = 0V$ and $V_{EE} = -0.5V$ and no external power supply is needed as the internal bias network provides V_{BB} .

ECL 10k circuit operated by negative logic

The DC noise margin for ECL 10k family are 0.155V in low state and 0.12V in high state.

The propagation delay of 10k ECL family is 2nsec and consumes power around 26mW

Working:

When A = B = Low

If the two inputs are low then the transistors Q₁, Q₂, Q₆ are in OFF state and Q₃, Q₅ are in ON state

∴ output of NOR = High

output of OR = Low

When A = B = High

If the inputs are high then the transistors Q₃, Q₅ are in OFF state

then Q₁, Q₂, Q₆ are in ON state

∴ output of NOR = Low

output of OR = High



Input
A B
0 0
0 1
1 0
1 1

Input
A B
0 0
0 1
1 0
1 1

Input
A B
0 0
0 1
1 0
1 1

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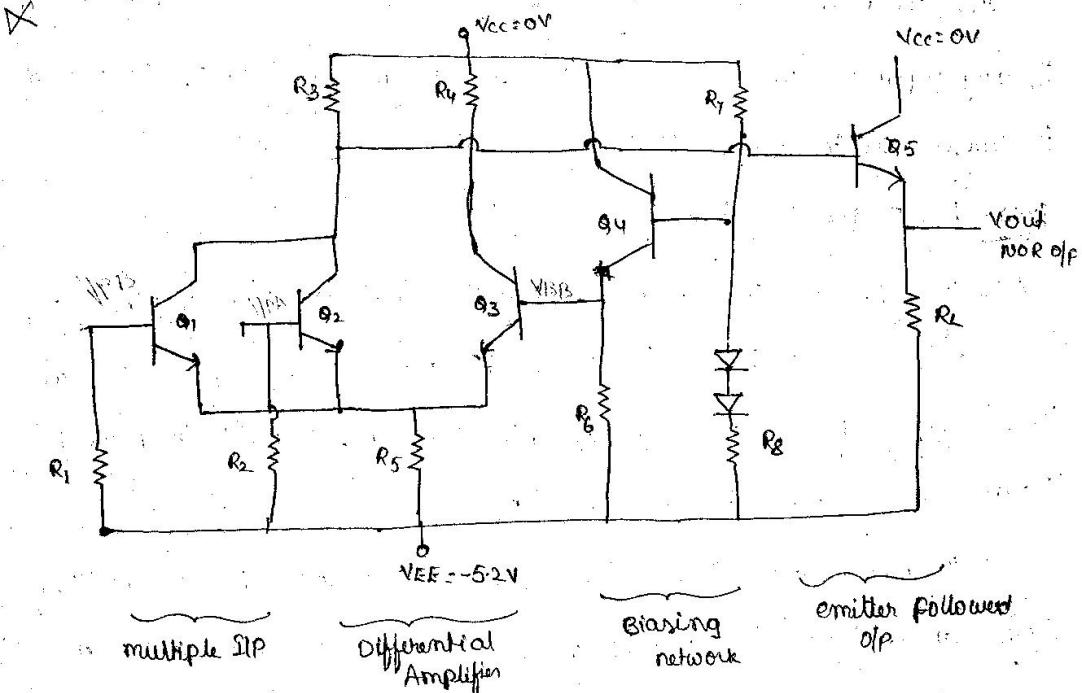
55V in low

and consumes

B_2, B_6 are in

are in OFF state

2iIP 10K ECL NOR gate:



2iIP 10K ECL NOR gate

Inputs	Transistors	Output (NOR)
A B	$Q_1 \quad Q_2 \quad Q_3 \quad Q_5$	
0 0	OFF OFF ON ON	High
0 1	OFF ON OFF OFF	Low
1 0	ON OFF OFF OFF	Low
1 1	ON ON OFF OFF	Low

Inputs	NOR o/p
A B	
0 0	1
0 1	0
1 0	0
1 1	0

The figure shows the 10K ECL two i/p NOR gate. The circuit has two additional components \Rightarrow Bias network and \Rightarrow Emitter follower output stage.

The pull down resistors are provided at the i/p's A & B or of the ECL NOR gate. If the i/p's are not connected it is treated as low.

25/7/13 When inputs A = B = low

then the transistors Q₁, and Q₂ are off and the output is high.

If any input is high then the corresponding transistor is ON and it causes Q₃ to turn OFF, where the output is low.

ECL 10K circuit operated by negative logic i.e. V_{cc} = 0V and V_{EE} = -5.2V. As the internal bias network provides V_{BB}. No external power supply is required. In the bias network, network component values are selected to provide V_{BB} = -1.29V.

complementary emitter follower output shift the output voltage levels down by 0.6V matching i/p and o/p voltage levels and increase the current sourcing capability.

The DC noise margin for ECL 10K family is 0.155V in low state and 0.105V in the High state.

The Propagation delay of ECL 10K family is 2nSec.

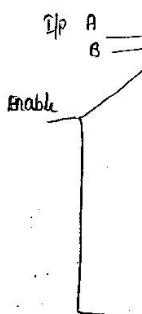
The power consumption of ECL 10K family is 26mWatts.

29/7/13 TTL Three State NAND gate

Design a tri state NAND gate and explain the operation with the help of function Table.

A TTL tri state TTL NAND gate is as shown in fig. This circuit is called Tri state TTL because it allows 3 possible output states.

- 1) High impedance state
- 2) Low state
- 3) High state



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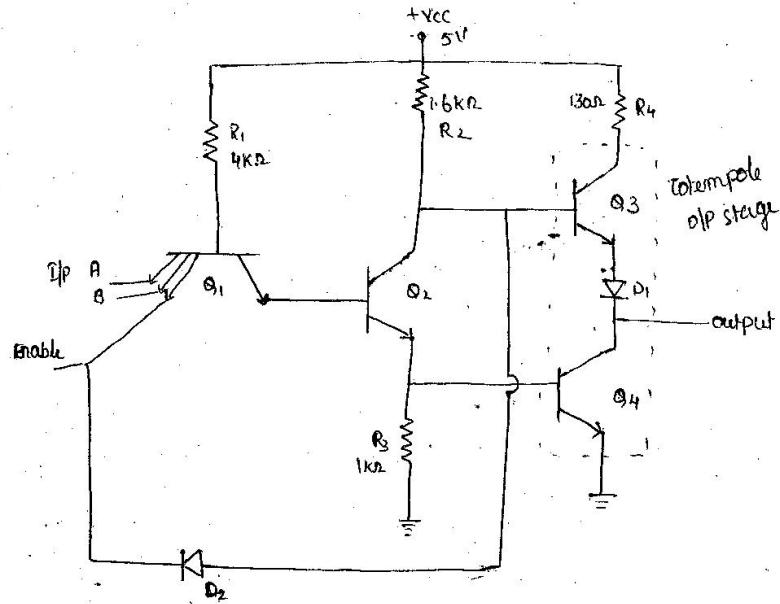
0.155 V in

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TRI STATE TTL NAND Gate

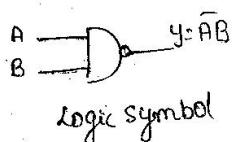
The O/P stage is connected in totem pole arrangement. The transistor Q_3 , Q_4 and diode D_1 form the totem pole stage. The transistor Q_3 , Diode D_1 , and transistor Q_4 are stacked on top of each other (1 NPN is in series with another NPN)

The advantage of totem pole stage is to increase the speed of operation and increase the current capability.

The above circuit is a simplified circuit for Tri-State NAND gate. It has 3 inputs A, B and EN. A and B are normal logic i/P's, whereas EN is Enable i/P. The transistor Q_1 is a multi-emitter transistor type.

Enable	Inputs	Transistors	Output
EN	A B	Q_1 Q_2 Q_3 Q_4	Hi-Z \leftarrow High impedance
L	X X	ON OFF OFF OFF	1 \leftarrow High state
H	0 0	ON OFF ON OFF	1 \leftarrow Low state
H	0 1	ON OFF ON OFF	1 \leftarrow Low state
H	1 0	ON OFF ON OFF	1 \leftarrow Low state
H	1 1	OFF ON OFF ON	0 \leftarrow Low state

Function Table:



Inputs		Output
A	B	$Y = \bar{A}B$
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

10

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working:

i) Enable = Low:

when enable I/P is low regardless of the state of logic input A and B, the Base emitter junction of Q_1 is forward biased. As a result it turns ON. This shunts the current through R_1 away from Transistor Q_2 OFF. i.e. there is no positive voltage at Base of Q_2 . As Q_2 is OFF there is no sufficient drive for Q_4 to conduct and hence Q_4 turns OFF. The low at Enable I/P also FB the diode D_2 which shunt current away from base of Q_3 , making it OFF.

ii) when enable input is low the O/P transistors Q_3 and Q_4 are OFF and o/p is High impedance stage. As a result is o/p is open. (iii) floating. it is neither low nor High

$\therefore \text{o/p} = \text{High impedance} \rightarrow \text{①}$

10/9/13

iii) Enable: High ; $A=B=0$; $A=0, B=1$; and $A=1, B=0$

when enable is high, the circuit works as a normal NAND gate.

when both the inputs are A and B are low or any one of its input is low then the base emitter junction of the transistor Q_1 is forward biased and so Q_1 is 'ON'.

As there is no sufficient voltage on the base of Q_2 if gate off. The collector potential of Q_2 is HIGH and emitter potential is zero.

3) Enable
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TTL Fam

iii) List of

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Also when $EN = \text{High}$, the diode D_2 gets reverse biased and acts as an open circuit so there is no voltage on the base of Q_3 from V_{CC} through R_2 . So Q_3 is ON. At the same time Q_4 is OFF.

In short Q_1 is ON, Q_2 is OFF, Q_3 is ON, Q_4 is OFF.

$\therefore [O/P = \text{High}] \rightarrow ②$

3) Enable: HIGH; A = B = High.

When both the inputs are High and $EN = \text{High}$ the base emitter junction of Q_1 becomes reverse biased and so Q_1 is OFF.

There is sufficient voltage from V_{CC} through R_1 on the base of Q_2 . As a result Q_2 is ON.

The collector potential of Q_2 is low as a result Q_3 gets OFF. At the same time Q_4 is ON due to emitter current of Q_3 .

In short $Q_1 = \text{OFF}$, $Q_2 = \text{ON}$, $Q_3 = \text{OFF}$, $Q_4 = \text{ON}$

$\therefore [O/P = \text{Low}] \rightarrow ③$

From the above it shows the Tri State TTL has the possible off state.

Tri state circuit is used in the data multiplexing when a single bus is shared among different data sources.

TTL Families:

- ✓ 8) List out TTL families and compare them with reference to Propagation delay, Power consumption, speed power product and low level input current.

List of TTL families.

TTL Families

early TTL Families

74 Series
TTL
(High speed
TTL)

74L
(Low
Power
TTL)

74S
(Schottky
TTL)

74LS
(Low
Power
Schottky
TTL)

Schottky TTL Families

74AS
(Advanced
Schottky
TTL)

74ALS
(Advanced
Low Power
Schottky TTL)

74P
(Fast TTL)

Q_3 if gates
Potential is

Comparison of TTL Families

S.No	Parameters	T4	T4S	T4 LS	T4 AS	T4ALS	T4F	
1.	Propagation delay (ns)	9 ns Slowest	3 ns	9 ns Slowest	1.7 ns Fastest	4 ns	3 ns	* For TTL i) Low \rightarrow C
2.	Power consumption (mW)	10 mW	20 mW Highest	2 mW	8 mW	1.2 mW Lowest	6 mW	V _{OH} min: 9V For TTL families
3.	Speed power Product (PJ)	90 PJ Highest	60 PJ	19 PJ	13.6 PJ	4.8 PJ Least	18 PJ	V _{TH} min: 9V as High
4.	Low level input current (mA)	-	-2 mA	-0.4 mA	-0.5 mA	-0.8 mA	-0.6 mA	V _{OL} max: 9V a low V _I
5.	max. clock rate (MHz)	35	125	45	200	70	100	i) DC noise margin it is a case output by an input
6.	Fan out	10	20	20	40	20	33	High state it is 0 by V _{NH} V _A
7.	Voltage Parameter							For low state
	V _{OH} min	2.4V	2.7V	2.7V	2.5V	2.5V	2.5V	V _{NL} = V _{IL} max
	V _{OL} max	0.4V	0.4V	0.5V	0.5V	0.4V	0.3V	ii) Low state when
	V _{TH} min	2V	2V	2V	2V	2V	2V	Since it file
	V _{IL} max	0.8	0.8	0.8	0.8	0.8	0.8	P _L max = 0.4

Explain following terms with reference to TTL gate

i) Logic levels ii) Voltage levels for logic 1 and logic 0

iii) DC noise margin.

iv) Low state unit load

v) High state fan out

vi) Logic levels : $V_{CC} = 5V$

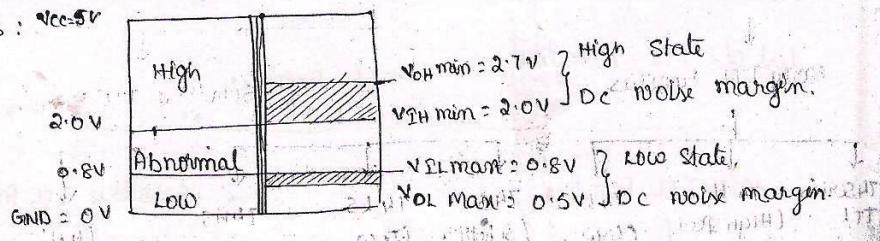


Fig Logic levels and noise margins for TTL logic families

(T4LS, T4S, T4ALS, T4AS, T4F)

iii) Low State

when

Since it file

P_L max = 0.4

iv) High State

the gate can
specifications

for TTL

AS	T4ALS	74F
7ns	4ns	3ns
start		
7W	1.0mW	6mW
lowest		
6PJ	4.8PJ	18PJ
worst		
mA	-0.2mA	-0.6mA
70	100	
20	33	
9.5V	2.5V	
0.4V	0.3V	
0.1V	2V	
0.8	0.8	

* For TTL families to the logic levels are:

i) Low \rightarrow 0V to 0.8V

ii) HIGH \rightarrow 2V to 5V

$V_{OH\ min}$: It is the minimum output voltage produced in HIGH for TTL families. $V_{OH\ min} = 2.7V$

$V_{IH\ min}$: It is the minimum i/p voltage guaranteed to be recognized as High. $V_{IH\ min} = 2V$ for TTL families

$V_{IL\ max}$: It is the max o/p voltage guaranteed to be recognized as Low. $V_{OL\ max} = 0.8V$ for TTL logic

$V_{OL\ max}$: It is max o/p voltage in the low state. $V_{OL\ max} = 0.5V$ for most TTL logic families

ii) DC noise Margin:

If it is a measure of how much noise it takes to corrupt a worst case output voltage into a value that may not be recognized properly by an input

High State DC Noise Margin:

It is the difference between $V_{OH\ min}$ and $V_{IH\ min}$. It is denoted by V_{NH}

$$V_{NH} = V_{OH\ min} - V_{IH\ min} = 2.7 - 2.0 = 0.7V$$

$$\boxed{V_{NH} = 0.7V}$$

For low state dc noise margin:-

$$V_{NL} = V_{IL\ max} - V_{OL\ max} = 0.8 - 0.3 = 0.5V \quad \boxed{V_{NL} = 0.5V}$$

iii) Low State Unit Load:

When TTL op-amp is in low state, current flows out of TTL i/p since it flows out of TTL i/p its values is -ve, typically

$I_{IL\ max} = -0.4mA$ for LSTTL. This is referred as "Low State Unit Load"

iv) High State Fan-out: Fan-out is defined as number of inputs that the gate can drive without exceeding its worst case loading specifications.

For TTL logic families, $I_{OL\ max} = 8mA$ $I_{OH\ max} = 400mA$

$$I_{IL\ max} = 0.4mA$$

$$I_{IH\ max} = 20mA$$

$$\text{Low State Fanout} = \frac{I_{OL\ max}}{I_{IL\ min}} = \frac{8\text{mA}}{0.4\text{mA}} = 20$$

$$\text{High State Fanout} = \frac{I_{OH\ max}}{I_{IH\ min}} = \frac{400\text{nA}}{20\text{nA}} = 20$$

$$\boxed{\text{High State Fanout} = 20}$$

$I_{OL\ max}$: The max. current on o/p can sink in low state while maintaining an o/p voltage no more than $V_{OH\ min}$. Since current flows into the o/p, $I_{OL\ max}$ has +ve value, 0.8mA for most LS-TTL outputs.

$I_{OH\ max}$: The max. current on o/p can source in High State, while maintaining an o/p voltage no less than $V_{OH\ min}$. Since current flows out of o/p, $I_{OH\ max}$ has -ve value, -400nA for most LS-TTL outputs.

Comparison of CMOS, TTL, ECL

- 1) Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, Propagation delay and Fanout.

SNo	Parameters	CMOS	TTL	ECL
1)	Device used	N channel MOSFET & P channel MOSFET	BJT	BJT
2)	Logic level	Low level \rightarrow 0 to 1.5V High level \rightarrow 3.5 to 5V	Low level \rightarrow 0 to 0.8V High level \rightarrow 2 to 5V	Low \rightarrow -1.850 to -1.630V High \rightarrow -0.98 to 0.81V
	$V_{IH\ min}$	3.5V	2V	-1.2V
	$V_{IL\ max}$	1.5V	0.8V	-1.4V
	$V_{OH\ min}$	4.95V	2.7V	-0.9V
	$V_{OL\ max}$	0.005V	0.4V	-1.7V
3)	DC noise margin	0.4V	0.3V	0.1V

High
margin
low
margin

4) NOIS

5) PROP
delay

6) FAN-

7) SWITC

8) POWER
PER %

9) SPEED
PRICE

10) POWER
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11) POWER

12) APPLI

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High level noise margin	$V_{NH} = 1.45V$	$V_{NH} = 0.4V$	$V_{NH} = 0.3V$
Low level noise margin	$V_{NL} = 1.45V$	$V_{NL} = 0.4V$	$V_{NL} = 0.3V$
4) Noise immunity	Better than TTL less than CMOS		more vulnerable to noise
5) Propagation delay	20ns	10ns.	500ps, 0.5ns.
6) Fan-out	50	10	25
7) Switching Speed	less than TTL	faster than CMOS	Fastest
8) Power dissipation Per gate	0.1mW	10mW	2.5mW
9) Speed power Product	0.7PJ	100PJ	0.5PJ
10) Power Supply Voltage	3 to 15V	Fixed 5V	-4.5 to -5.2
11) Power dissipation	increase with frequency	increase with frequency	constant with frequency
12) Applications	Portable instruments where battery supply is used	Laboratory instruments	High speed instruments

Explain Sinking and Sourcing current of TTL O/p which of the parameters decide fan-out and how.

Sinking current: When the current flows into a TTL output in the low state, the O/p is said to be "Sinking current". If the current flows from power supply through load and through TTL O/p to ground known as sinking current of TTL output.

Sourcing current: When current flows out of a TTL O/p in High state the output is said to be "sourcing current".

If current flows from power supply out of device O/p and through the load to ground, it is known as "sourcing current".

ECL

BJT

Low \rightarrow -1.85V to -1.6302

High \rightarrow -0.98 to 0.81V

-1.2V

-1.4V

-0.9V

-1.7V

Parameters which decides the fan-out:

Both sinking current and sourcing current are used to decide the fanout depending on low and high states.

Low State $I_{OL\ max}$:

The max. current an O/P can sink in low state, maintaining the o/p voltage less than $V_{OL\ min}$.

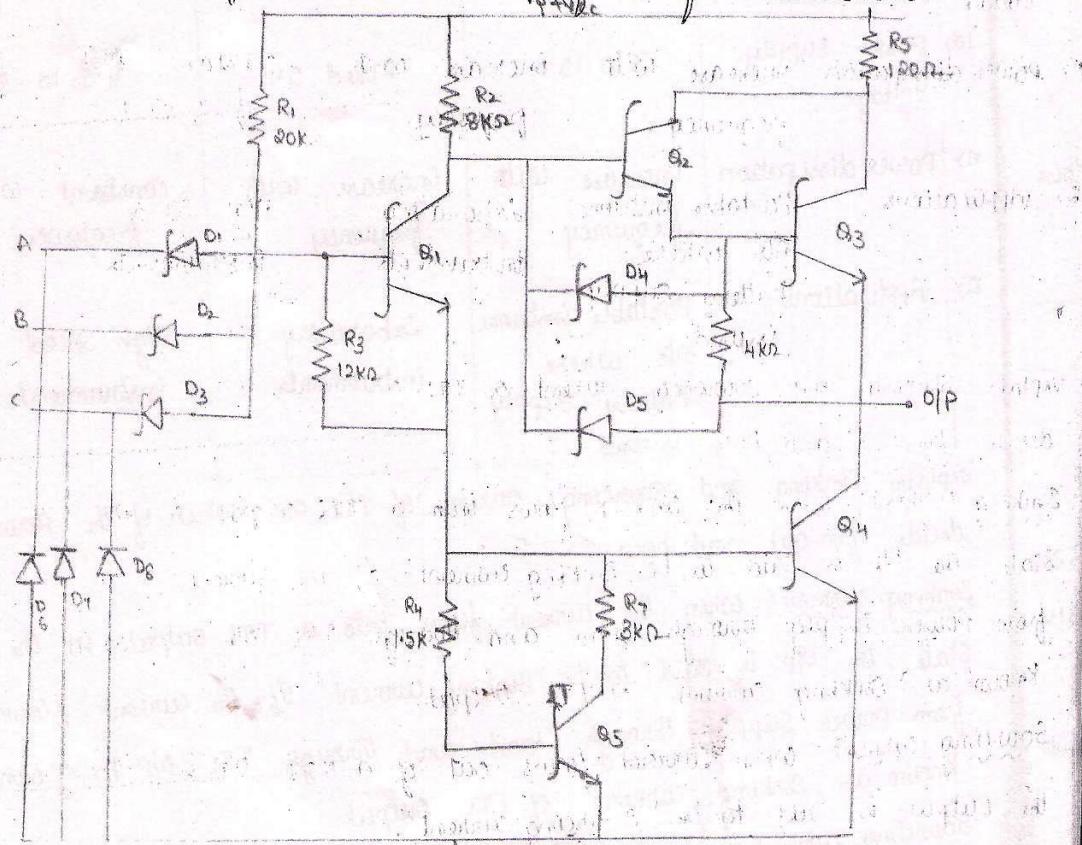
$$\therefore V_{OL\ max} = 8\text{mA} \text{ for most LS-TTL output}$$

High State $I_{OH\ max}$:

The max. current an output can source in high state, maintaining the output greater than $V_{OH\ min}$.

$$I_{OH\ max} = -100\mu\text{A}$$

1) Design three i/p NAND gate using diode logic and transistor inverter. Analyze circuit with help of transfer characteristics.



diode AND gate and i/p protection

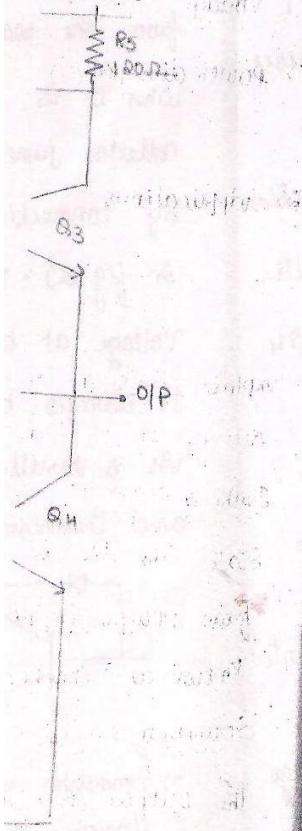
Phase Shifter

O/P Stage

3*i/p* LS-TTL NAND gate

used to decide
what state was
maintaining
high state, maintain-

and transistor
characteristics.

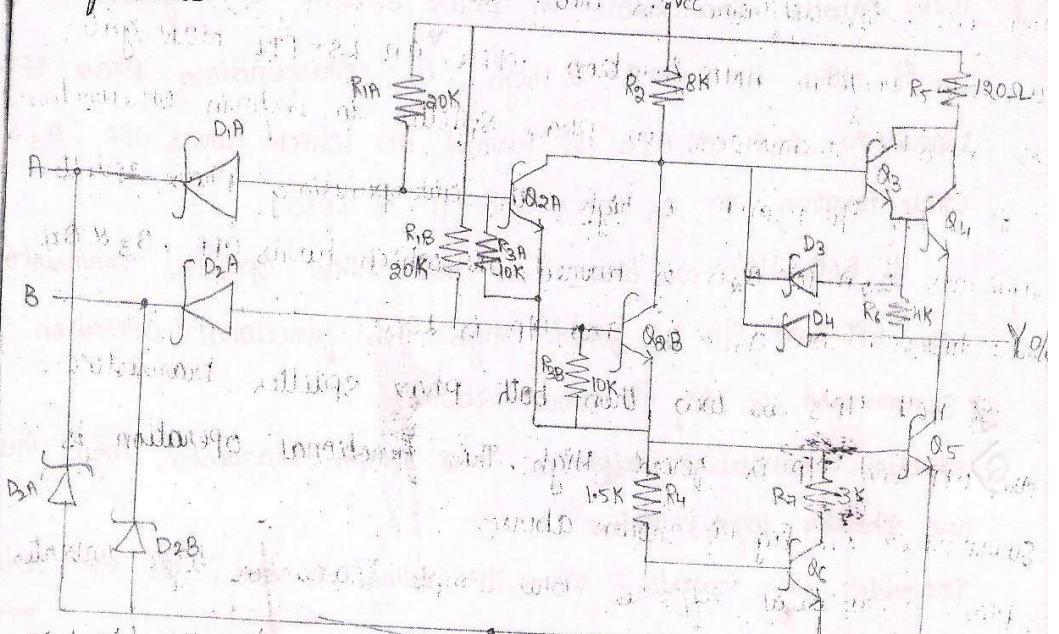


The Figure Shows the circuit diagram for 3-I/P LS-TTL NAND (74LS00). we know that NAND function can be obtained by inverting the O/P of AND function. The circuit uses same logic to implement NAND function. The circuit is basically divided into 3 function parts i) Diode AND gate and input protection ii) Phase Shifter iii) O/P stage

The diodes D_1, D_2, D_3 with resistor R_1 forms 3-I/P NAND gate. Diodes D_6, D_7, D_8 at I/P are used as protective diodes. These diodes protect the circuit from large negative transients. If an I/P attempts to go more than about 1 volt -ve, the protective diode conducts and clamps I/P voltage to its conducting voltage.

The Q_2 transistor acts as a inverter. The transistor Q_2 with surrounding resistors form a phase splitter that controls the O/P stage.

- ✓ Draw the circuit for a I/P LS-TTL NOR gate and explain its operation. give the function table, truth table and logic sym for same



Diode I/P's & O/P operation

function & phase shifter

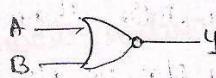
& I/P LS-TTL NOR gate

The above figure shows 2-IIP LS TTL NOR gate

Punchin Table

Inputs		Transistors (turn on output)					
A	B	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆
0	0	OFF	OFF	ON	OFF	OFF	OFF
0	1	OFF	ON	OFF	OFF	ON	ON
1	0	ON	OFF	ON	OFF	ON	ON
1	1	ON	ON	OFF	OFF	ON	ON

Logic symbol & Truth Table



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The figure shows circuit diagram for an LS TTL 2-IIP NOR gate.

The circuit is basically divided into 3 parts.

i) input circuit ii) phase splitter iii) output stage.

The circuit is almost identical to those of an LS TTL NAND gate. The difference is that an LS-TTL-NAND gate uses diodes to perform AND function, while an LS-TTL NOR gate uses parallel transistors in phase splitter to perform OR function.

If either IIP A or B is high, the corresponding phase splitter transistor Q₁ or Q₂ is turned ON which turns OFF Q₃ & Q₄ while turning on Q₅ & Q₆ and O/P is LOW.

If both IIP's are low then both phase splitter transistor are off and O/P is forced HIGH. This functional operation is

summarized in fig @ shown above.

Q) explain behavioural difference b/w simple transistor logic inverter and Schottky logic inverter.

Transistor logic inverter: when IIP voltage is low, the O/P voltage

is high from one transistor

Schottky

and will

transistor

causes a

change

is switcher

carriers

delays (

only

from one

when it

collectes

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in fig @

Voltage (

It clamp

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and that

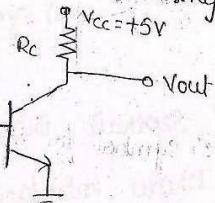
water

as

transist

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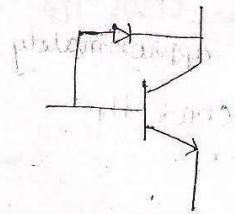
is high, and vice versa. Therefore we can make a logic inverter from an n-p-n transistor in the CE configuration. The operation transistor inverter for both i/p's using switching analogy.



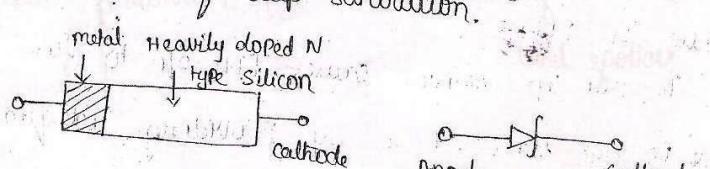
✓ Schottky Transistor:

With standard TTL, high speed TTL, and low power TTL transistors are ON, they are driven into hard saturation. This causes a surplus of carriers to be stored in base. This excess charge carriers in base region must be removed before transistor is switched from ON to OFF. The time required to remove these carriers called "storage time" is responsible for high propagation delays or low switching times.

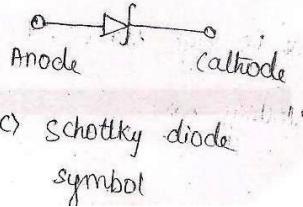
The only way to counter this problem is to prevent the transistor from going into deep saturation when it is turned ON i.e. to restrict the F.B. of its base to collector junction to few tenths of volt. This can be accomplished by connecting diode across base to collector junction as shown in fig (a). The diode does not allow to increase the forward bias voltage at base to collector junction above its cut-in voltage. It clamps base to collector voltage upto its small cut-in voltage. As a result the junction cannot be heavily forward biased and transistor is kept out of deep saturation.



a) Transistor with clamping diode



b) Schottky diode conduction



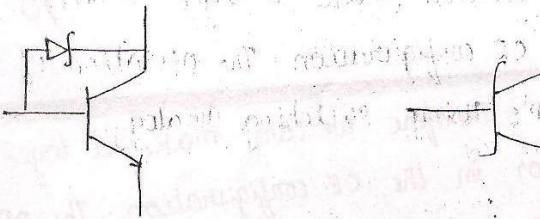
c) Schottky diode symbol

Transistor operation is similar to logic inverter.

Storage logic inverter

the off voltage

TTL Drv
when
becomes
operated
arrange



d) Schottky clamped
transistor.

e) symbol for Schottky clamped transistor

Q) What is necessity of separate interfacing circuit to connect CMOS gate to TTL gate? Draw interface circuit and explain operation.

When two circuits have different electrical characteristics direct connection cannot be made. In such cases driver and load circuit are connected through interface circuits. Its function is to take the driver o/p signal and condition it so that it is compatible with requirements of load.

The driver o/p must satisfy voltage and current requirements of load circuit.

The driver and load circuit may require different power supply. In such cases o/p of both circuit must swing b/w its specific voltage ranges.

* $V_{OH} \text{ min}$ for TTL $\ll V_{IH} \text{ (min)}$ for

CMOS for this situation TTL o/p must

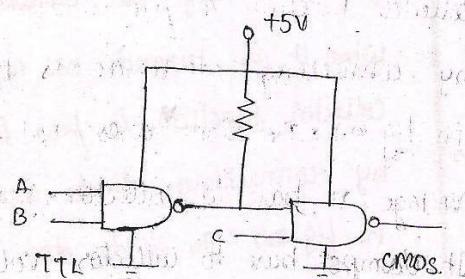
raise to an acceptable level for

CMOS. This is done by connecting

Pull-up resistor at o/p of TTL as

Show in Figure

The pull-up resistor causes TTL o/p to rise to approximately 5V in high state, thereby providing adequate CMOS input voltage level.



i) when T
collector is
operating

Fig
2) The second
as the
a low ve
CMOS.

• 14 bits digit in
16 bits no more
above of maximum

imped transistor.

connect cmos

plum operation.

characteristics direct

voltage and load

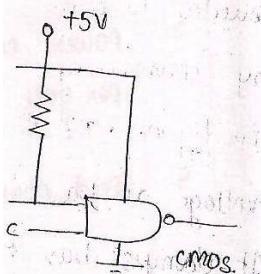
• Its function

in it so that

current requirements

1 different power

swing b/w its



g CMOS using
Pull up resistor

• approximately
CMOS i/p

TTL Driving in High voltage CMOS
when o/p CMOS circuit is operated with $V_{DD} > 5V$, the situation becomes more difficult. o/p's of many TTL devices cannot be operated at more than 5V. In such cases some alternative arrangement are made two of TTL's are discussed below

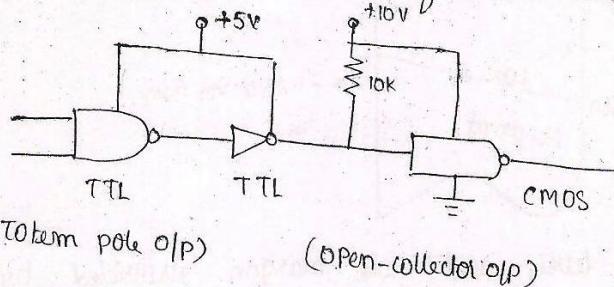


Fig open collector buffer used as interface circuit

• when TTL o/p cannot be pulled up to V_{DD} one can use open collector buffer as an interface b/w totem pole TTL o/p and CMOS operating at $V_{DD} > 5V$ as shown in fig.

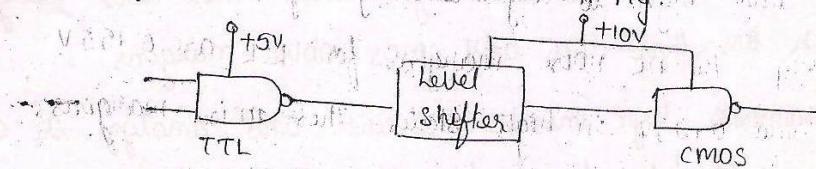
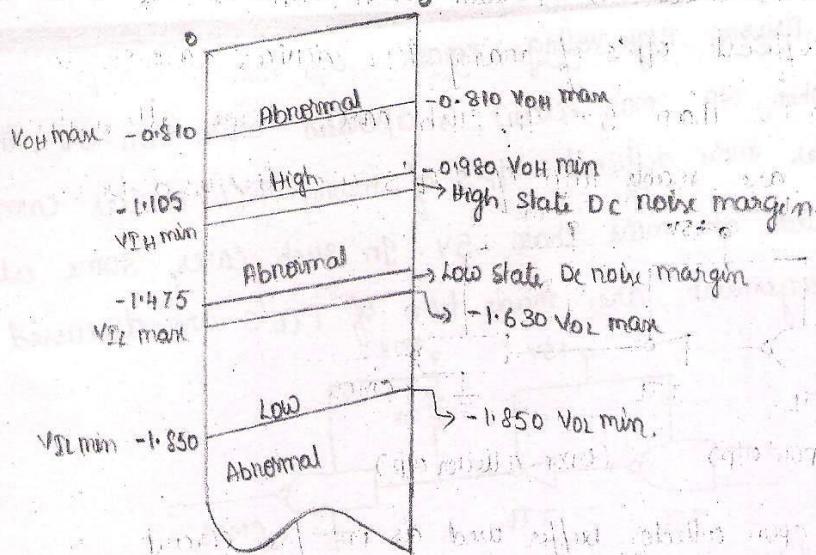


Fig Level Shifter used as interface circuit

• The second alternative is to use level translator circuit such as the _____. This is a CMOS chip that is designed to take a low voltage i/p and translate it to high voltage o/p for CMOS.

Mention the DC noise margin levels of ECL 10K Family



The Voltage levels and noise margin provided by 10K ECL family is shown in fig even though power supply is ECL -ve assigns the names Low and High to algebraically higher and lower voltages respectively. The DC noise margins for ECL are 0.155V in low state and 0.125V in high states. These noise margins are much less than TTL and CMOS noise margins.

Draw transistor logic inverter circuit and analyze the circuit behaviour with help of transfer characteristics.

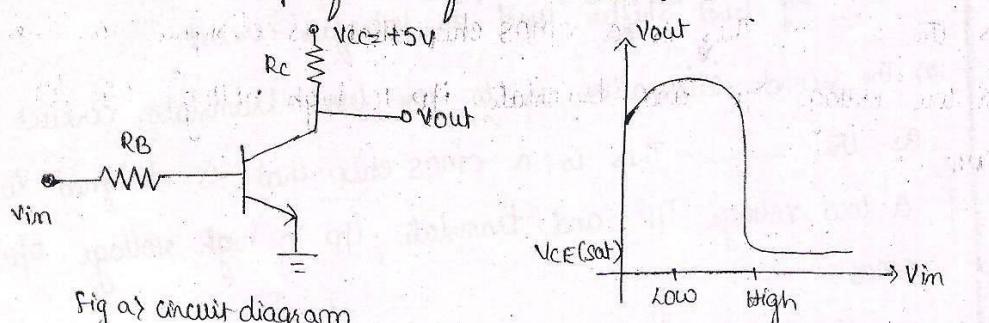
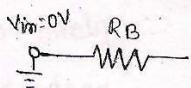
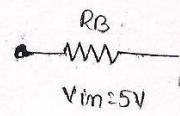


Fig a) circuit diagram

Transistor inverter

when i/p voltage is low the o/p voltage is high and vice versa
∴ we can make logic inverter from an NPN transistor in CE configuration as shown in figure

The below inputs (HIC)

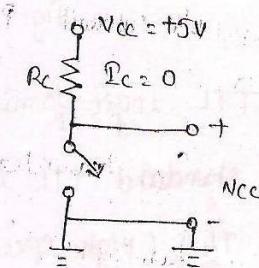
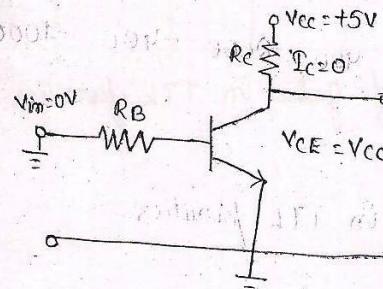
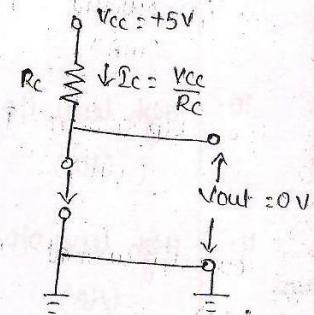
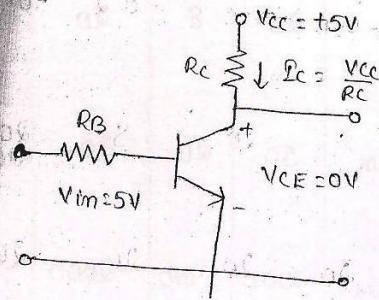


Transistor

List out differ
Discuss electrica

SNO	Description
1.	Maximum f delay (ns)
2.	Power conv. per gate (r)
3.	Speed power
4.	Low level P/P
5.	Low level O/P
6.	High level i/p

The below figure shows operation of transistor inverter from inputs (High and low) using switching analogy.



Transistor cut off.

Switch off state

- ✓ List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74LS00.

SNO	Description	Symbol	74S	74LS	Family	74AS	74ALS	74F
1.	Maximum Propagation delay (ns)		3	9	1.7	4	3	
2.	Power consumption per gate (mw)		19	2	8	1.2	1	
3.	Speed power Product (Ps)		57	18	13.6	4.8	1.2	
4.	Low level P/P voltage (V)	$V_{IL\max}$	0.8	0.8	0.8	0.8	0.8	0.8
5.	Low level O/P voltage (V)	$V_{OL\max}$	0.5	0.5	0.5	0.5	0.5	0.5
6.	High level O/P voltage (V)	$V_{IH\min}$	2.0	2.0	2.0	2.0	2.0	2.0

		V_{OH} min	2.7	2.7	2.7	2.7	2.7	2.7	t_{PLH}	t_{PHL}	t_{PCL}
7.	High level O/P voltage (V)										Switching
8.	Low level I/P current (mA)	I_{IL} max	-2.0	-0.4	-0.5	-0.2	-0.6				Parameter
9.	Low level O/P current (mA)	I_{OL} max	20	8	20	8	20				t_{PLH}
10.	High level I/P current (mA)	I_{IH} max	50	20	20	20	20				t_{PHL}
11.	High level O/P current (mA)	I_{OH} max	-1000	-400	-2000	-400	-1000				electrical

fig: characteristics of gates in TTL families.

TTL Logic families:

- 1) standard TTL logic
- 2) 74H (high speed TTL logic)
- 3) 74L (low power TTL logic)
- 4) 74S (Schottky TTL logic)
- 5) 74LS (low power Schottky TTL logic)
- 6) 74AS (Advanced Schottky TTL logic)
- 7) 74ALS (Advanced low power Schottky)
- 8) 74FS (Fast Schottky TTL logic)

Data sheet for 74LS00:

Recommended operating conditions

Parameters	Description	SN54LS00			SN74LS00			unit
		min	nom	max	min	nom	max	
V_{DD}	Supply voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
V_{IH}	High level I/P voltage	2.0	-	-	2.0	-	-	V
V_{IL}	Low level I/P voltage	-	-	0.7	-	0.8	-	V
I_{OH}	High level O/P current	-	-	-0.4	-	-0.4	-	mA

2.7	2.7	I_{OL}	low level O/P current			4		8	mA
-0.2	-0.6	T_A	operating free air temp	-55		125	0	70	°C

Switching characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$

Parameter	From (O/p)	To (O/p)	Test conditions	min	Type	max	unit
t_{PLH}	A or B	X	$R_L = 2k\Omega$	9		15	ns
t_{PHL}			$C_L = 15pF$	10		15	ns

-400 -1000

electrical characteristics over recommended free-air temperature range

Parameter	Test conditions	SN54LS00			SN74LS00			unit
		min	Type(Q)	max	min	Type(Q)	max	
V_{IK}	$V_{CC} = \text{min}$; $I_N = 18mA$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{min}$; $V_{IL} = \text{max}$ $I_{OH} = 0.4mA$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{min}$; $V_{IH} = 2.0V$ $I_{OL} = 4mA$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{min}$; $V_{IH} = 2.0V$ $I_{OL} = 8mA$				0.35	0.5		V
I_L	$V_{CC} = \text{max}$; $V_I = 7.0$			0.1			2.0	mA
I_{IH}	$V_{CC} = \text{max}$; $V_I = 0.7V$			2.0			-0.4	mA
I_{IL}	$V_{CC} = \text{max}$; $V_I = 0.4V$			-0.4			-1.00	mA
$I_{OS(3)}$	$V_{CC} = \text{max}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{max}$; $V_I = 0V$		0.8	1.6		0.8	1.6	mA
I_{CCL}	$V_{CC} = \text{max}$; $V_I = 4.5V$		2.4	4.4		2.4	4.4	mA

unit :-

max

5.25 V

V

0.18 V

-0.4 mA

(26)

1) In VHDL 'v' stands for very high speed IC (VHSC)

2) In CMOS logic 1 represents (b)

- a) 0 to 1.5V
- b) 3.5 to 5V
- c) 1.5 to 5
- d) 0 to 0.8

3) In CMOS logic 0 represents 0 to 1.5V

4) Low power consumption for the logic family (b)

- a) ECL
- b) CMOS
- c) TTL
- d) RTL

5) TTL output stage is called (a)

- a) Totem pole
- b) Push Back
- c) Pull back
- d) Pulled out

6) First logic family came into picture is (a)

- a) TTL
- b) CMOS
- c) NMOS
- d) PMOS

7) When V_{DD} of 5V is applied to the CMOS circuit PMOS is OFF and NMOS is ON

- a) All OFF
- b) OFF ON
- c) ON ON
- d) OFF OFF

8) When V_{DD} of 0V is applied to the CMOS circuit PMOS is ON and NMOS is OFF

9) From the following symbol compulsorily to complete \oplus syntax (a)
Statement (b)

- a) :
- b) ;
- c) =
- d) and (&)

10) ECL belongs to the family (b)

- a) Bipolar Saturated
- b) Bipolar non saturated
- c) Unipolar Saturated
- d) Unipolar non saturated

11) Which one of the family belongs to unipolar logic family (a)

- a) CMOS
- b) TTL
- c) CML
- d) HTL

12) Which one of the family belongs to bipolar logic family (TTL)

13) In ECL propagation delay is (a)

- a) short time
- b) long
- c) constant
- d) zero

14) PORT is used in following syntax (a)

- a) entity
- b) architecture
- c) concurrent statement
- d) sequential

15) IEEE STD.

- a) memm

16) CMOS - HI

- a) 74 AC

17) Basically

- a) multi

18) Power a

- a) PJ

19) Port ma

- a) lab

- b) labs

- c) to ce

- d) PDI

20) Componen

- a) Stru

21) High sta

- a) (74 LS

- a) 0 to

22) Fastest

- a) TTL

23) In Has I

- a) P-N J

24) In CMOS

- a) low to

- a) full HI

25) In CMOS {

- 15) IEEE.STD LOGIC-1164.ALL represents the standard logic (b)
- memory
 - package
 - procedure
 - function
- 16) CMOS High speed represents (b)
- 74ACT30
 - 74HC30
 - 74AC30
 - 74DC30
- 17) Basically the single stage CE transistor acts as a logic circuit (c)
- multiplexer
 - decoder
 - inverter
 - differentiator
- 18) Power consumption for gate units used in 74F family (c)
- pJ
 - nsec
 - mWatts
 - Volts
- 19) Port map symbol (a)
- Table : component-name Portmap (Signal1, Signal2 ... Signaln)
 - Table : Portmap (componentname (Signal1, " "))
 - to component name - table Portmap (Portmap Signal1, Signal2 ...)
 - Portmap (Signal1, Signal2 ... : table component name)
- 20) Component declaration used in the following model (a)
- structural
 - constant
 - behavioural
 - dataflow
- 21) High state DC Margin for Popular TTL Families (d)
- 74LS
 - 74S
 - 74ALS
 - 74F
- 0 to 0.5V
 - 0.5 to 0.8V
 - 0.8 to 2V
 - 2 to 2.7V
- 22) Fastest logic family from the following (b) ECL-PinT
- TTL
 - Schottky TTL
 - RTL
 - DTL
- 23) In this the following diode there is no depletion region is (d)
- p-n Junction
 - Zener
 - Si Tunnel diode
 - Schottky diode
- 24) In CMOS output takes change from (b)
- low to high state
 - fall time
 - rise time
 - propagation delay time
 - constant time
- 25) In CMOS output takes change from high to low state (a)

(28)

Questions

19) Design CMOS 4 input OR and invert gate. Draw the logic diagram and explain with function table.

20) Design CMOS AND or invert gate and draw logic diagram and explain its working.

21) Explain the following terms with reference to CMOS logic
 a) logic levels b) DC noise margin c) Power supply range d)
 propagation delay.

22) Design CMOS Transistor circuit for two input AND gate. Explain the circuit with the help of function table.

23) Design a CMOS Transistor circuit that has the functional behaviour

$$F(Z) = \overline{a(b+c)}$$

unit-II

24) Design a Transistor circuit of two input ECL NOR gate explain working with help of function table

25) What is the necessity of separate interfacing circuit to connect CMOS gate to TTL

26) Draw interface circuit and explain it

27) Design a TTL 3 state NAND gate and explain operation with the help of function table

28) Define sinking and sourcing currents

Compare CMOS, TTL, ECL with reference to logic levels, Propagation

margin.
 29) Draw the circuit diagram of two input LS-TTL NOR gate and explain its functional behaviour

unit-II

30) Explain the dataflow design elements of VHDL with syntax.
 Write any VHDL program using concurrent signal assignment statements in dataflow model

31) Design the logic circuit and write structural VHDL program for the following function $F(A) = \sum_{B,C,D} (0, 2, 5, 7, 8, 10, 13, 15) + d(11)$

32) Design a

and with

43) write

53) write

63) write

$$F(S) =$$

$$P(C_0)$$

73) Design
Program

F

83) write
style

3) Design a logic circuit to detect the prime numbers of 4 input
and write VHDL program in dataflow model.

4) write structural model VHDL program for full adder.

5) write VHDL program for all logic gates.

6) write behavioural style VHDL program for following function

$$F(S) = A + B + C,$$

$$P(C_0) = AB + AC_1 + BC_1$$

7) Design the logic circuit and write a structural style VHDL
Program for following function.

$$F(A) = \prod_{i=1}^7 p_{2^i} (1, 3, 4, 5, 6, 7, 9, 12, 13, 14)$$

8) write a VHDL program for 4x1 Multiplexer in dataflow
style.

explain

at CMOS

with the

delay, Fanout
and explain

in
gument

am for the

ii)