

## Unit-8

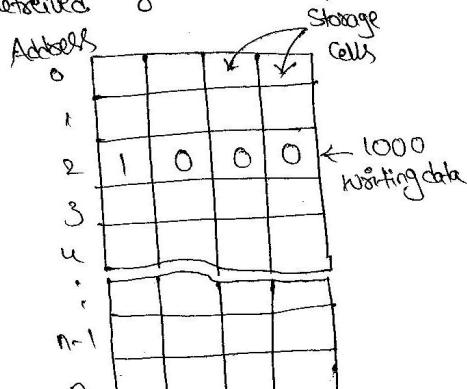
### Memoses:-

Register is a type of storage devices which are used to store large amount of digital data.

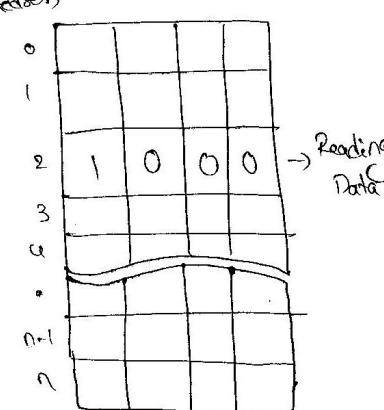
Memories are made up of registers. Each register in the memory is one storage location. Each location is identified by an address. Each location can accommodate one (or) more bits.

Generally the total no. of bits that a memory can store is its capacity. Most of the times the capacity is specified in terms of bytes (group of eight bits).

Each register consists of storage elements (flip-flops, flip-flops in semiconductor memory and magnetic domain in magnetic storage), each of which stores one bit of data. A storage element is called a cell. The data stored in memory by a process called "writing" and are retrieved from memory by a process called "reading".



Write operation

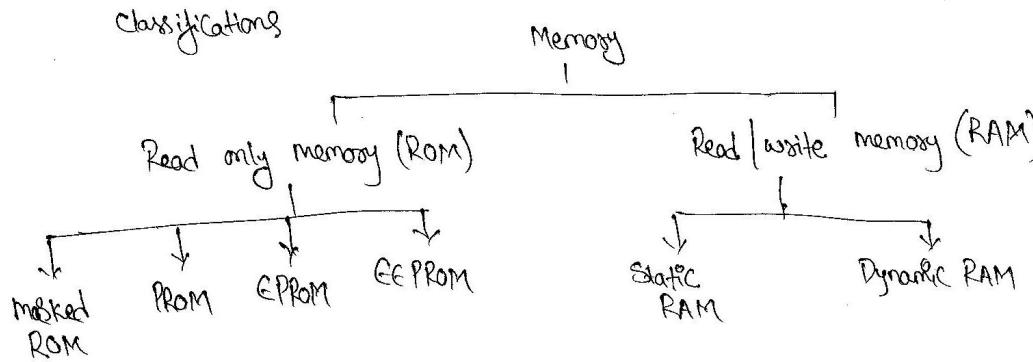


Read operation

A memory unit stores binary information in groups of bits (3)  
called word.  
The word in memory is an entity of bits that move in & out  
of storage as unit.

The word having group of 8-bit is called "byte".  
The word having group of 16-bit contains 2-bytes ; 32-bit word contains 4-bytes.

### \* Semiconductor memories:-



### \* Read only Memory :- (ROM)

We can't write data in this memory. It is non volatile memory  
i.e. it can hold data even if power is turned off. Generally ROM  
is used to store the binary codes for the sequences of  
instructions you want the computer to carry out and data such as  
look up tables.

4-types of ROM's are

- 1) Masked ROM ; 2) PROM (Programmable Read only memory)
- 3) EEPROM (Erasable Programmable Read only memory).
- 4) EEPROM (Electrically Erasable Programmable Read only memory).

(3)

▷ Read Only Memory :-

This type of Memory is used to hold data that are either Permanent (i) will not change. Data can only be read from ROM and is non-volatile mask programmable.

For ROM the data that are stored have to be built in during manufacturing process.

For other ROM (Programmable) data can be entered electrically. The process is known as Programming (i) burning the ROM.

(A) Maskable ROM (i) Mask Programmable ROM :-

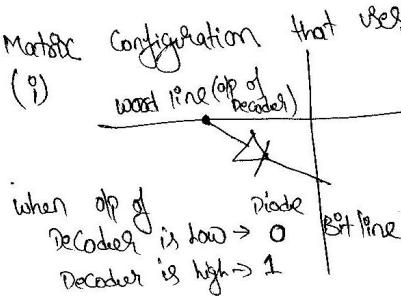
This type of memory can be programmed by the IC Manufacturers. A user who purchases a mask PROM supplies the manufacturer with the data to be stored in the ROM i.e. Program.

The Mask PROM are constructed in Matrix Configuration that uses

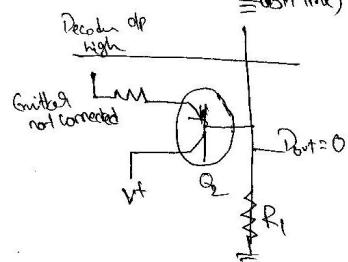
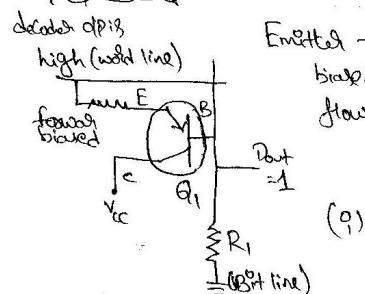
(i) Diodes

(ii) Bipolar junction transistors (BJT)

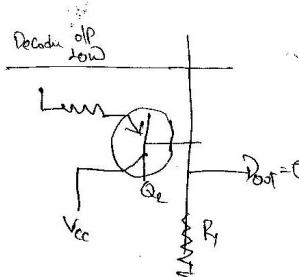
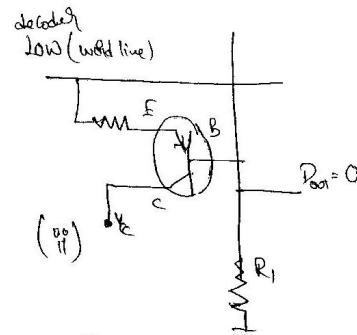
(iii) MOSFET



(ii) Bipolar Junction Transistor (BJT)



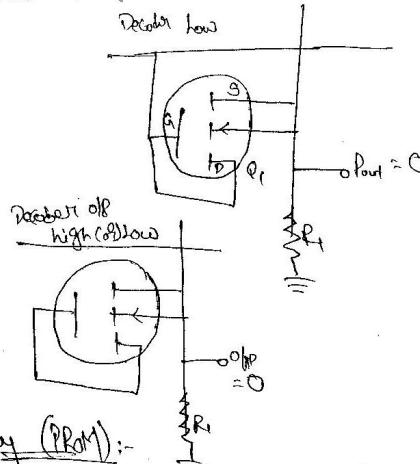
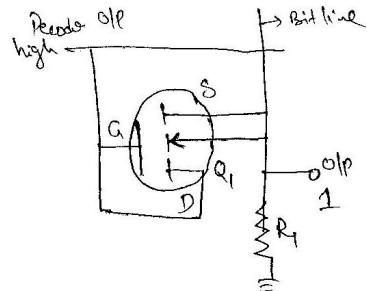
Emitter - Base junction forward biased which allows current to flow through Resistor  $R_1$



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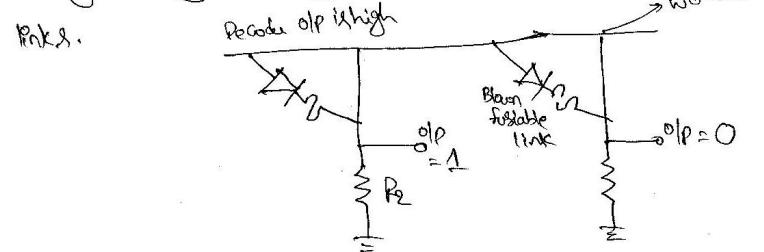
(iii) Mask ROM's:- MOSFET's are used to connect the interlocking conductors.

The gate and drain of  $Q_1$  are connected to horizontal  $\phi$  line, and the substrate and source terminals are connected to vertical line. When decoder  $\phi$  line is selected by high  $\phi$ , the FET resistance is near zero ohms, which allows corresponding lines to intersect. Thus current flows throughout resistor  $\phi$ .



(B) Programmable Read only memory (PROM):-

This IC is unprogrammed contains either 0's or 1's. Initially every memory bit consist of diode in series with fusible links.



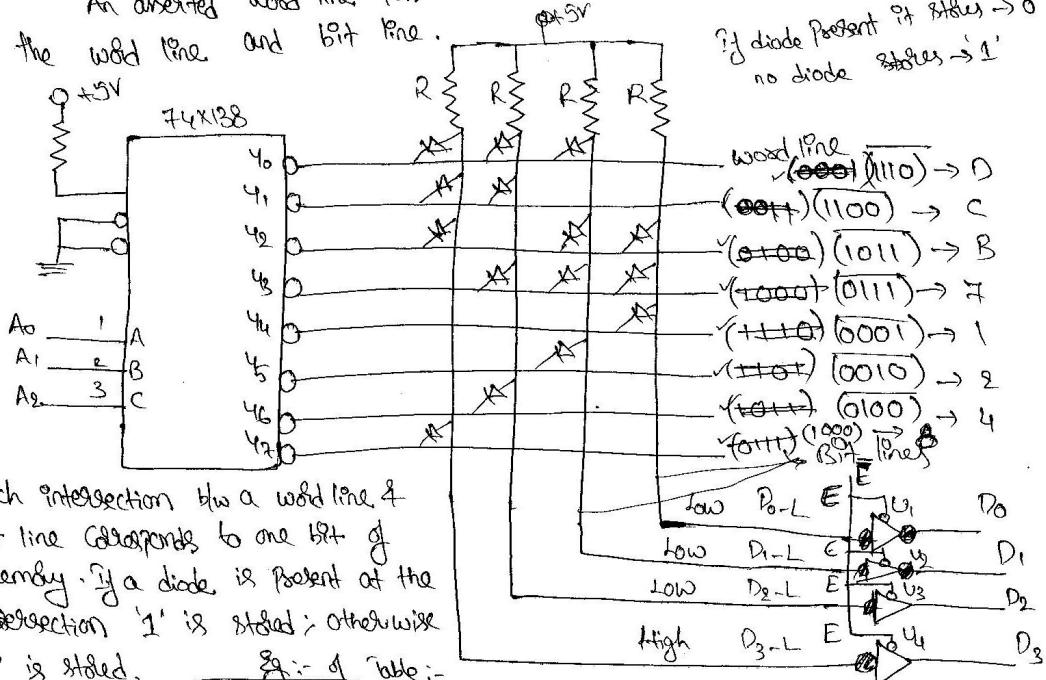
(3)

### \* Internal Structure of ROM:-

The mechanism used by ROM's to store information varies with different ROM techniques. In most ROM's the presence (H) absence (L) of diode (D) transistor distinguishes b/w 0 & 1.

The 8x4 ROM having decoder and a handful of diodes. The address pin select one of the decoded o/p to be asserted. Each decoder o/p is connected to one of the word line, because it selects one row (H) word of table stored in ROM. A word line, because it selects one row (H) word of table stored in ROM. Each vertical line is called a bit line because it corresponds to one o/p bit in the ROM.

An asserted word line pulls a bit line low if diode is connected b/w the word line and bit line.



Each intersection b/w a word line & bit line corresponds to one bit of memory. If a diode is present at the intersection '1' is stored; otherwise '0' is stored.  
Eg:- of table:-

Table:-

Address in Binary	Binary data	Data in Hex
000	1011	B
001	0100	4
010	0001	1
011	1111	F
100	0111	7
101	1110	F
110	1101	D
111	1100	C

o/p of data line is available only when o/p enable signal is low

## 1) Programmable Read only memory :-

A typical PROM comes with all bits reading as '1'. Burning a fuse during Programming causes its bits to read as '0'. The memory can be programmed just once after manufacturing by "blowing" the fuses, which is a irreversible process. Programming is done by applying high voltages pulses which are not encountered during normal operation.

Advantages:-

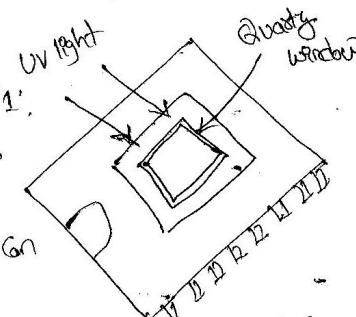
- (i) Reliability
- (ii) Stores data permanently
- (iii) Moderate price
- (iv) Built using IC, rather than discrete components
- (v) fast ~~step~~ reading is b/w 35ns & 60ns.

## 2) Erasable Programmable Read only Memory (EPROM) :-

This stores 1 & 0's as a packet of charge in a buried layer of IC chip. EPROM can be programmed by use with a special EPROM programmer. To Erase the stored data in the EPROMS by exposing chip to ultra violet light through its quartz window for 15 to 30 minutes. This chip can be reprogrammed.  
useful for:- Product development, experimental projects, and College laboratories.

### EPROM Programming:-

When erased each cell in the EPROM contains '1'. Data is introduced by selectively programming 0's in to the desired bit locations. Although only 0's will be programmed both 1's and 0's will be presented in the data.



During Programming address and data are applied to address and data pins of the EPROM. When the address and data are stable, program pulse is applied to the program pin of the EPROM. The program pulse duration is some ms and its amplitude depends on EPROM IC. It is typically 12.5V

to 25V. In EPROM it is possible to program any location at any time - either individually, sequentially, (8) or random. ⑤

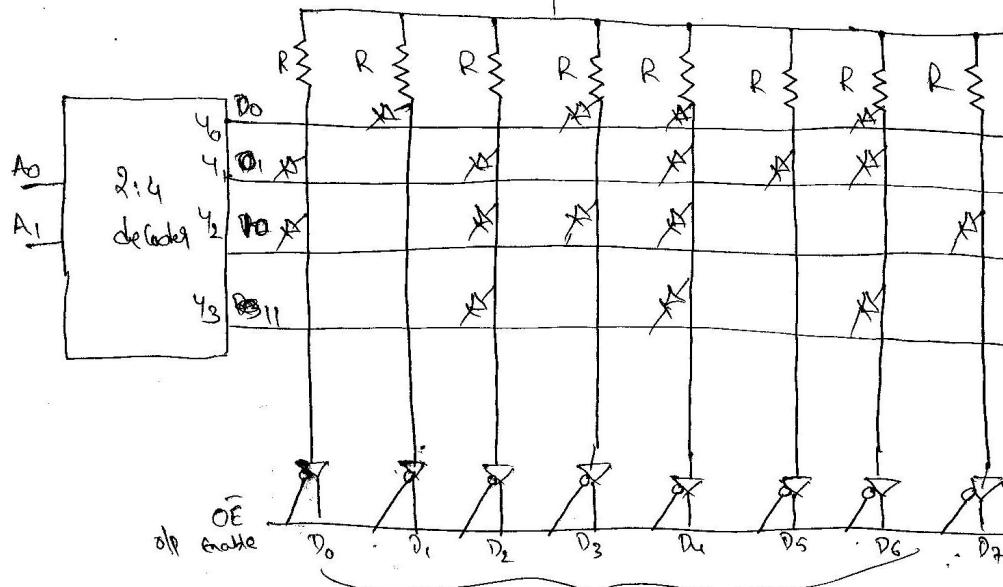
### 3) EE PROM :- (Electrically Erasable Programmable Read only Memory) :-

Electrically Erasable Programmable ROM also use MOS circuitry very similar to that of EEPROM. Data is stored as charge (8) no charge on isolated layer (8) on insulated layer ~~or~~ floating gate in the device. The insulating layer made very thin ( $< 200\text{A}$ ). Therefore a voltage as low as 20 to 25V can be used to move charges across the thin ~~isolated~~ ~~bottom~~ ~~bottom~~ in either direction for Programming (8) Erasing.

### \* Commercial ROM types :-

Type	Technology	Read Cycle	Write Cycle	Comments
MASK ROMS	NMOS, CMOS	10-200 ns	4 weeks	write once, High density, Low Power.
	Bipolar	$< 100\text{ns}$	"	write once; High power; Low density
PROM	Bipolar	$< 100\text{ns}$	<del>10-50 ns</del> 10-50 μs/byte	write once, High Power, <del>Low density</del>
EPROM	NMOS, CMOS	25-200 ns	10-50 μs/byte (erase time 15-20ms)	Re-writable, Low Power, High Erase time
EPPROM	NMOS	50-200 nsec	10-50 μs/byte Erase time 100ms	Re-writable, Low erase time

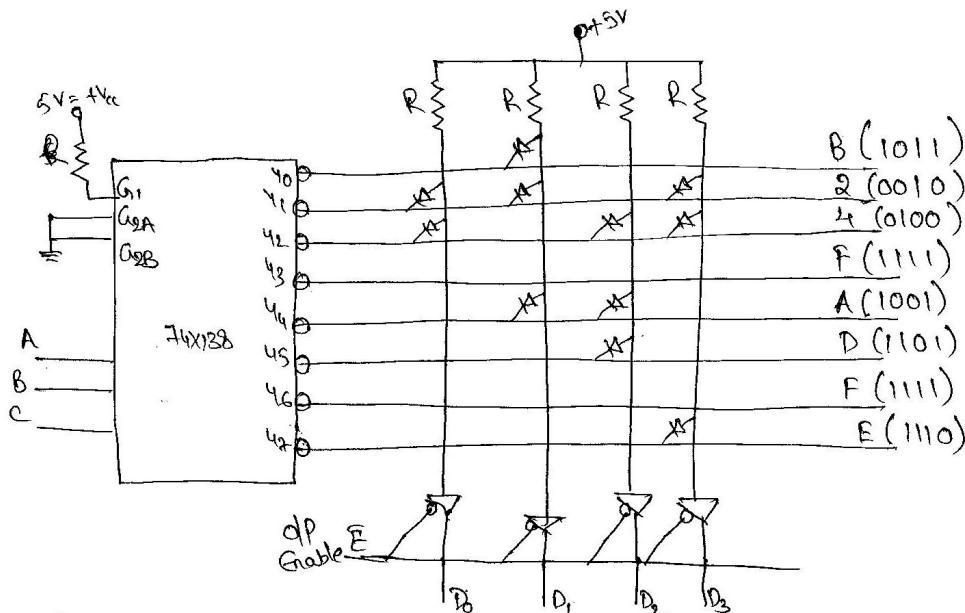
\* Design 4-byte Rom using 2:4 decoder - (8) 4x8 diode Ram using ⑥  
5V



Address in binary	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	Data ° in Hex
00	1	0	1	0	0	1	0	1	A5
01	0	1	0	1	0	0	0	1	51
10	0	1	0	0	0	1	1	0	46
11	1	1	0	1	0	1	0	1	D5

A<sub>0</sub> and A<sub>1</sub> are two address lines and these address lines are decoded by 2:4 decoder and they are used to select one of four rows.

Design 8x4 diode ROM using 74x138 for following data starting from ⑦ the first location B, 2<sub>4</sub>, F, A, D, F, E.



Address:-  
Binary

A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
0	0	0	1	0	1	1
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	1	1	1
1	0	0	1	0	0	1
1	0	1	1	1	0	1
1	1	0	1	1	1	1
1	1	1	1	1	1	0

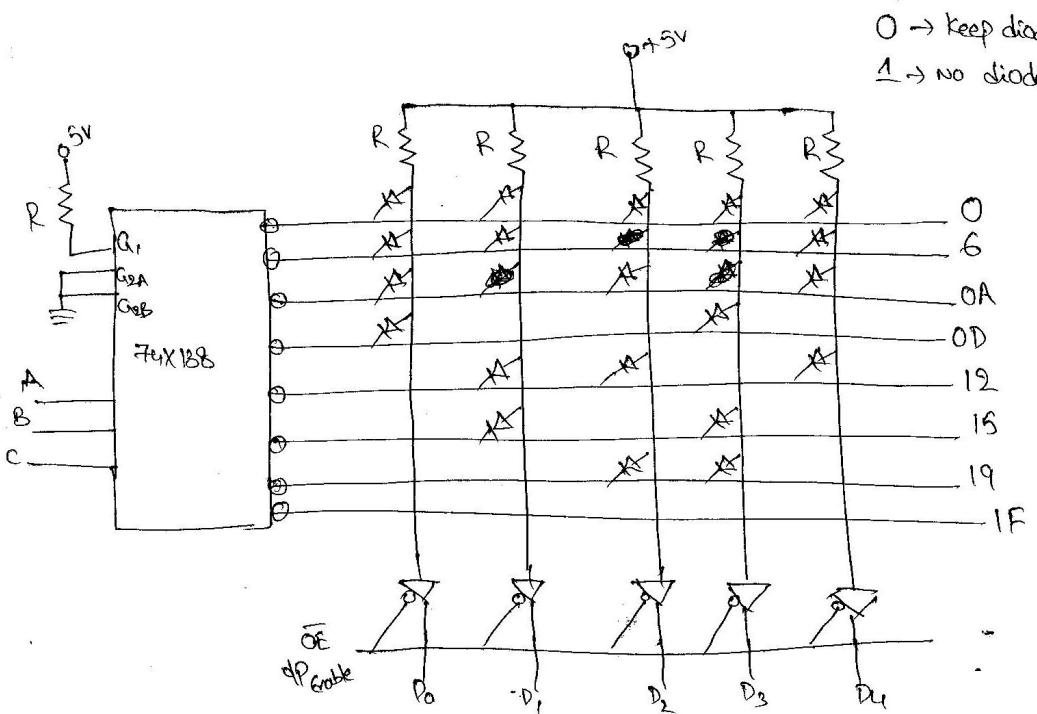
Hexa  
Decimal dP

B  
2  
4  
F  
A  
D  
F  
E

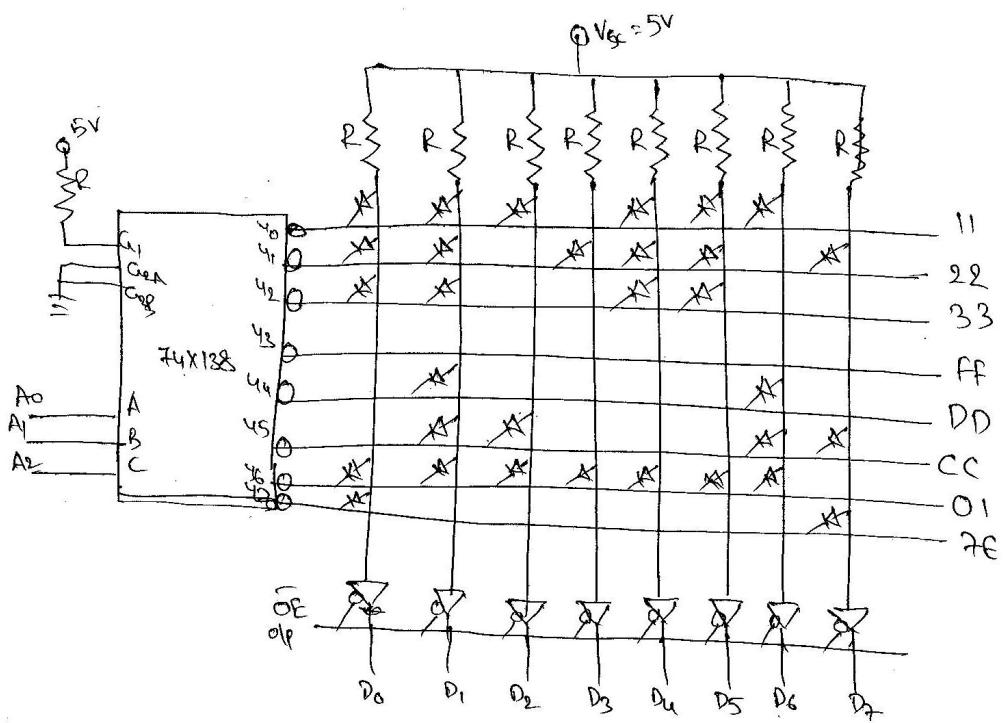
From given question first analyze the dP in the Hexa to binary and assign the logic circuit connection using diodes.

P) Design a diode ROM for full adder circuit using 74x138 ~~sing~~ ②  
3:8 decoder?

Address Binary			Binary data						Hex decimal			
A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A	B	C	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	Sum	Carry
0	0	0				0	0	0	0	0	0	
0	0	1				0	0	1	1	0	6	
0	1	0				0	1	0	1	0	A	
0	1	1				0	1	1	0	1	D	
1	0	0				1	0	0	1	0	12	
1	0	1				1	0	1	0	1	15	
1	1	0				1	1	0	0	1	19	
1	1	1				1	1	1	1	1	1F	







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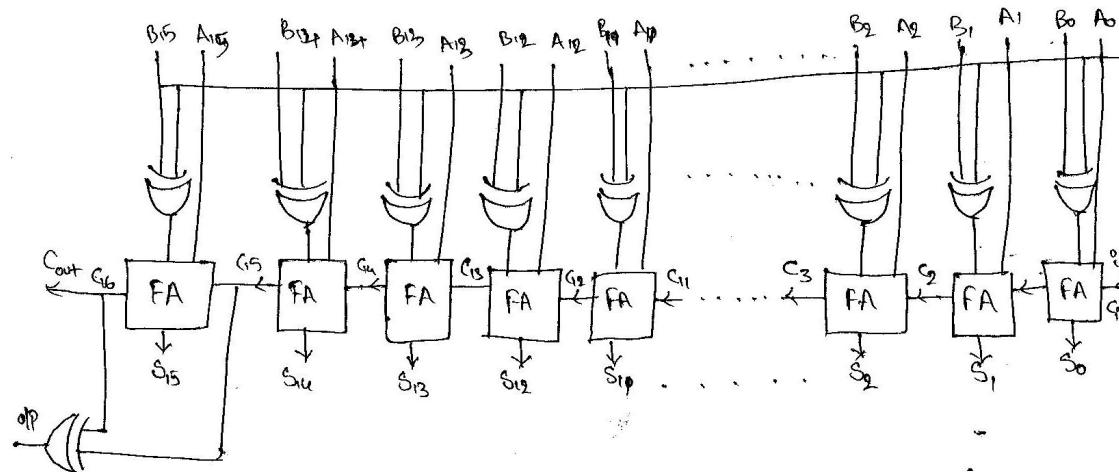
\* How Many ROM bits are required to built a 1-bit adder/subtractor bit with mode control, 2's Complement overflow dp, Garry °IP and Garry °OP. Show the block schematic with all °IP's and dp's.

Sol:- The total no. of °IP & dp required to built a 16-bit adder/subtractor with Garry °IP, mode Control, 2's Complement overflow and Garry °OP are calculated as below.

$$\begin{array}{l}
 \text{Total } °\text{IP} = 5/\text{P} \cdot A_0 \text{ to } A_5 = 16 \\
 \quad | \\
 \quad | \quad 5/\text{P} \quad B_0 \text{ to } B_5 = 16 \\
 \quad | \quad 5/\text{P} \quad \text{Garry} = 01 \\
 \quad | \quad \text{mod Control } 5/\text{P} = 01 \\
 \hline
 \text{Total } \text{dp} = 34
 \end{array}$$

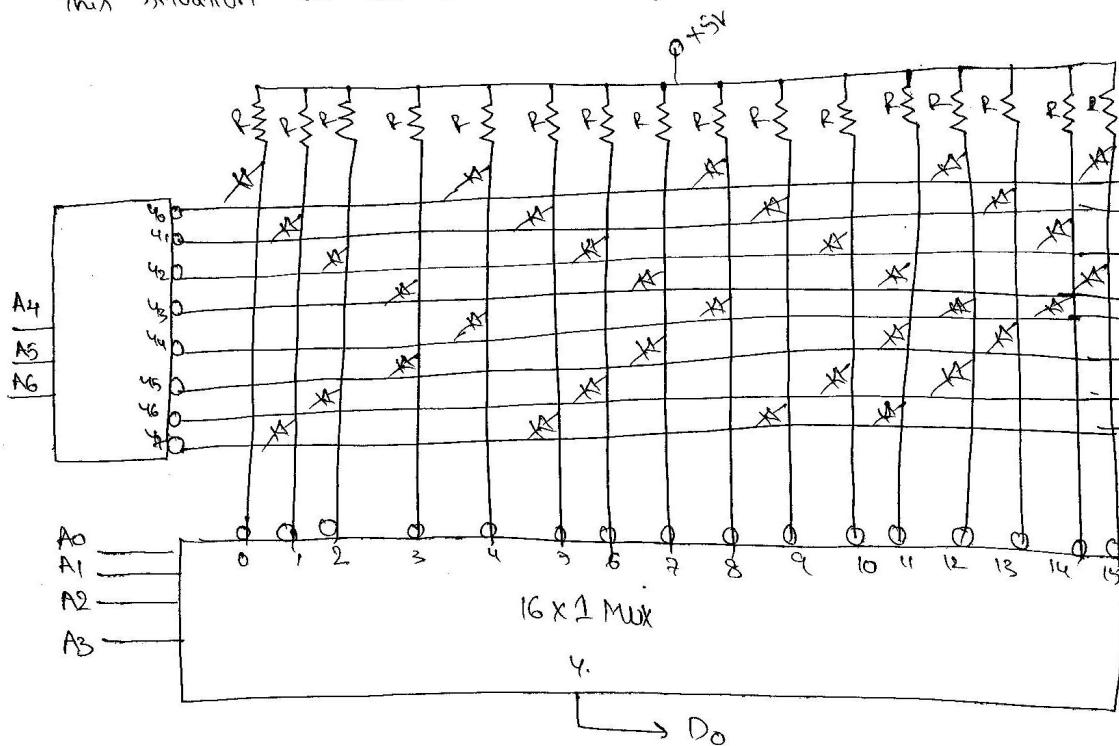
$$\begin{array}{l}
 \text{dp Bits } S_0 \text{ to } S_5 = 16 \\
 \quad | \\
 \quad | \quad \text{2's complement overflow} = 01 \\
 \quad | \quad \text{dp Garry Out} = 01 \\
 \hline
 \text{Total } \text{dp} = 18
 \end{array}$$

∴ The no. of bits required to built a 16-bit adder/subtractor with mode Control and Garry °IP is  $2^{34} \times 18 = 3.09 \times 10^9$ .  
 $\therefore 3.09 \times 10^9$  bits are required to built a 16-bit adder/subtractor.



Q) Explain the necessity of 2-D decoding mechanism in memory cell in ROM and explain the operation.

The 2-D mechanism is used to reduce the decoder size for example to construct a  $128 \times 1$  ROM we require large size of decoder. To avoid this situation we can use 2-D decoding.

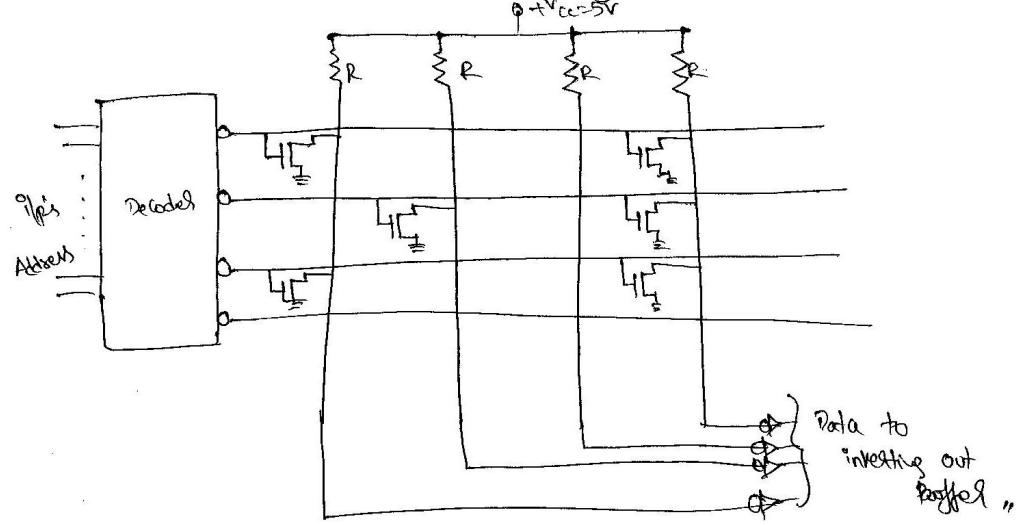


Internal structure of  $128 \times 1$  Rom using 2-D decoded.

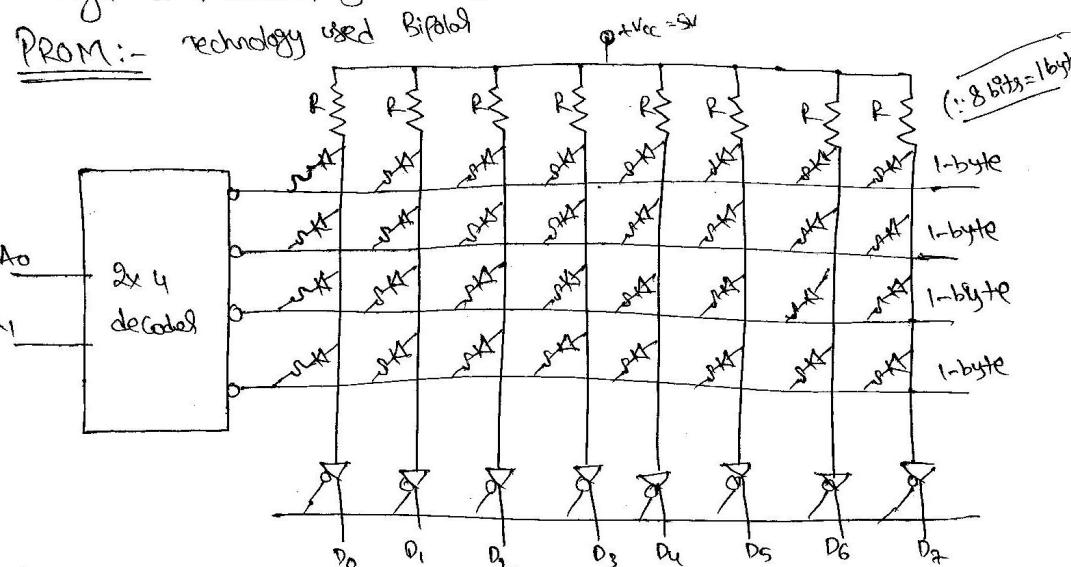
The basic idea in 2-D decoding is to arrange ROM cells in an array. The 3-highest order address bits A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub> are used to select a row. Each row stores 16-bits starting at address A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, 0, 0, 0, 0. When an address is applied to the ROM all 16-bits in the selected row are readout in parallel and the bit lines. A 16-to-1 mux selects the desired data bits based on the lower order address bits.

MOS transistors as storage element in ROM.

(13)



\* Design 2-4 decoder for 4-byte PROM (Programmable Read only memory).



A 4-byte PROM as shown in figure, It has diodes in every bit position. Each diode as a foldable link. The user can program PROM with special PROM programmer. The programmer selectively burns the fuses according to bit pattern to be stored. The PROMs are one time programmable once programmed the information stored is permanent.

## EEPROM & EA PROM :-

(14)

EEPROM Stands for Electrically Erasable PROM.

EA PROM " " " Alternate "

Technology used is N-mos. EEPROM & EA PROM both are same but it EEPROM can erase selected data by using electrical signals.

The Erase timing quite small 10msec as compared to EPROM.

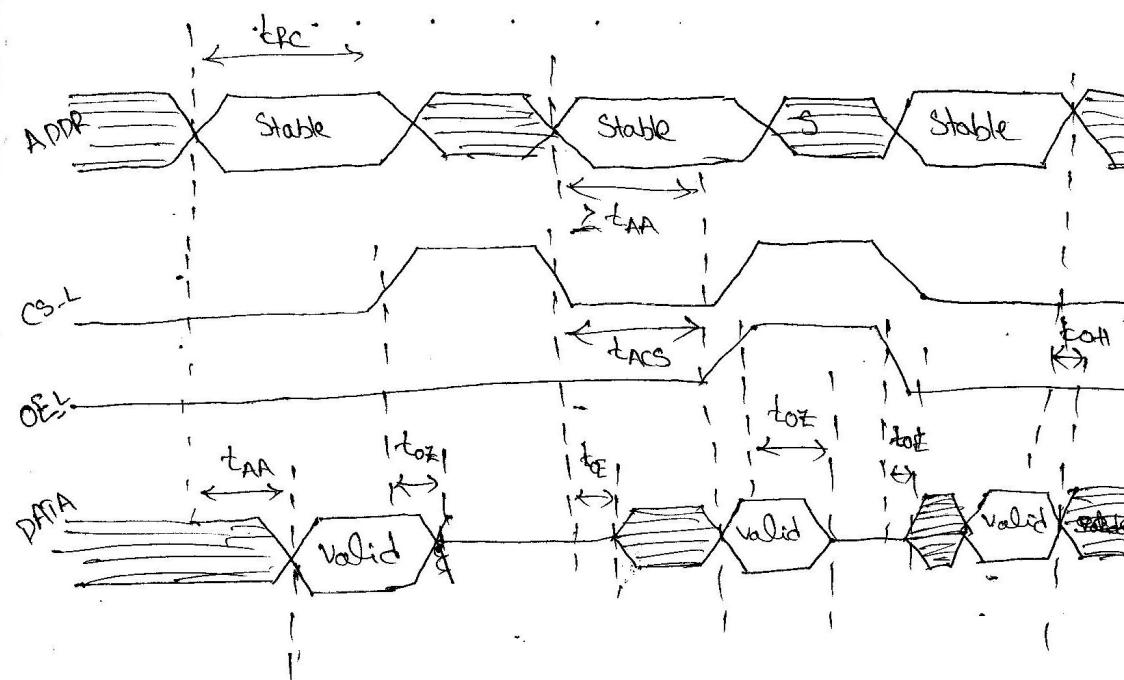
EEPROM are expensive. These memories are called flash memories because an entire block can be erased in flash time.

## \* ROM timing:-

Discuss in detail ROM access mechanism with the help of timing waveform

discuss in detail ROM access mechanism with the help of timing waveform

(Q) give a brief description of ROM timing parameters.



$t_{AA}$  :- (Address Access time)

Stands for Access time from address.  $t_{AA}$  of a ROM is the propagation delay from stable address  $\oplus$  to valid data  $\oplus$ .

$t_{RC}$  :- (Read Cycle time) :-

It is minimum time for which an address must be held stable on the address bus.

$t_{AC}$  :- (Access time from chip select) :-

It is the propagation delay from point where the chip select  $C_s$  is becoming low to the point where the data is becoming valid.

$t_{OE}$  :- (Op of enable line) :-

It is propagation delay from the point where  $C_s$  and  $OE$  goes low to the point where the high impedance state ends.

$t_{OZ}$  :- (Op disabled time) :-

It is the propagation delay from point where  $C_s$  ( $OE$ )  $OE$  becomes high to the point where there is a occurrence of high impedance state.

$t_{OH}$  :- (Op hold time) :- It is the time upto which, the  $\oplus$  data remains valid even after address changes ( $C_s$   $OE$  ( $C_s$  goes high)).

## \* RANDOM ACCESS MEMORY (RAM) (or) Read/ Write Memory (RWM)

Large Scale random access memory (RAM), also known as Read/ write memory is used to temporary storage of data and Program instruction in microprocessor based systems.

In term Random means the contents of any memory location can be accessed randomly.

A major drawback of RAM's is that they are volatile and lose all stored data if power is switched off.

The RAM device include internal address decoders and op buffers. Also op amplifiers are used to sense low voltage levels of data stored at each memory location so that information can be increased to a certain readable level at the op of IC.

(1) Static RAM (SRAM)      (2) Dynamic RAM (DRAM).

\* In static RAM (S-RAM), once a word is written at a location it remains stored as long as power is applied to the chip, unless the same location is written again.

\* In Dynamic RAM (D-RAM) the data stored at each location must be refreshed periodically by ~~refreshing~~ reading it and then writing it back again, or else it disappears.

→ Most RAM's lose their memory when power is removed; they are a form of volatile memory.

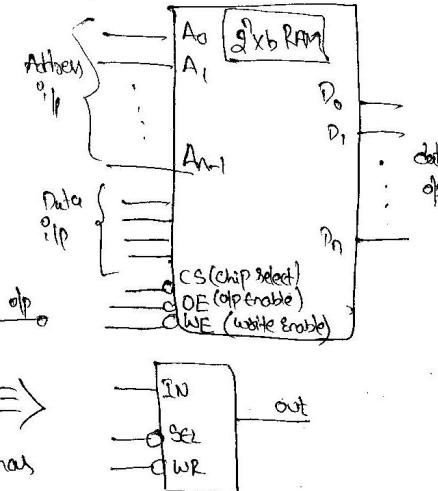
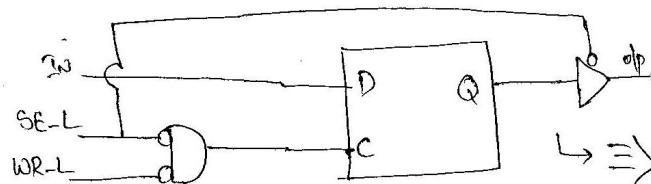
→ RAM's retain their memory even when power is removed they are called non-volatile memory.

▷ Static RAM :-

Like a ROM, a RAM has address and control pins & data pins, but it also has data pins. The address & data pins can range  $2^k \times b$ -bits static RAM. The control pins are compatible to those RAM with the addition of write-enable (WE) pin. When WE is asserted, the data pins are written into the selected memory location.

Internal Structure of Static RAM :-

Functional behavior is shown below

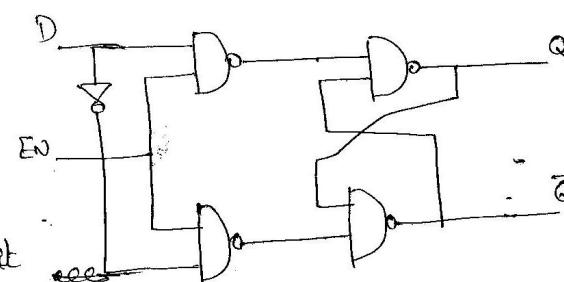


Each bit of memory in a static RAM has functional behavior circuit. The storage device in each cell is D-latch. When a cell's SEL-L pin is asserted, the stored data is placed on the cell's o/p, which is connected to a bit line. When both SEL-L and WR-L are asserted, the latch is open and new data bit is stored.

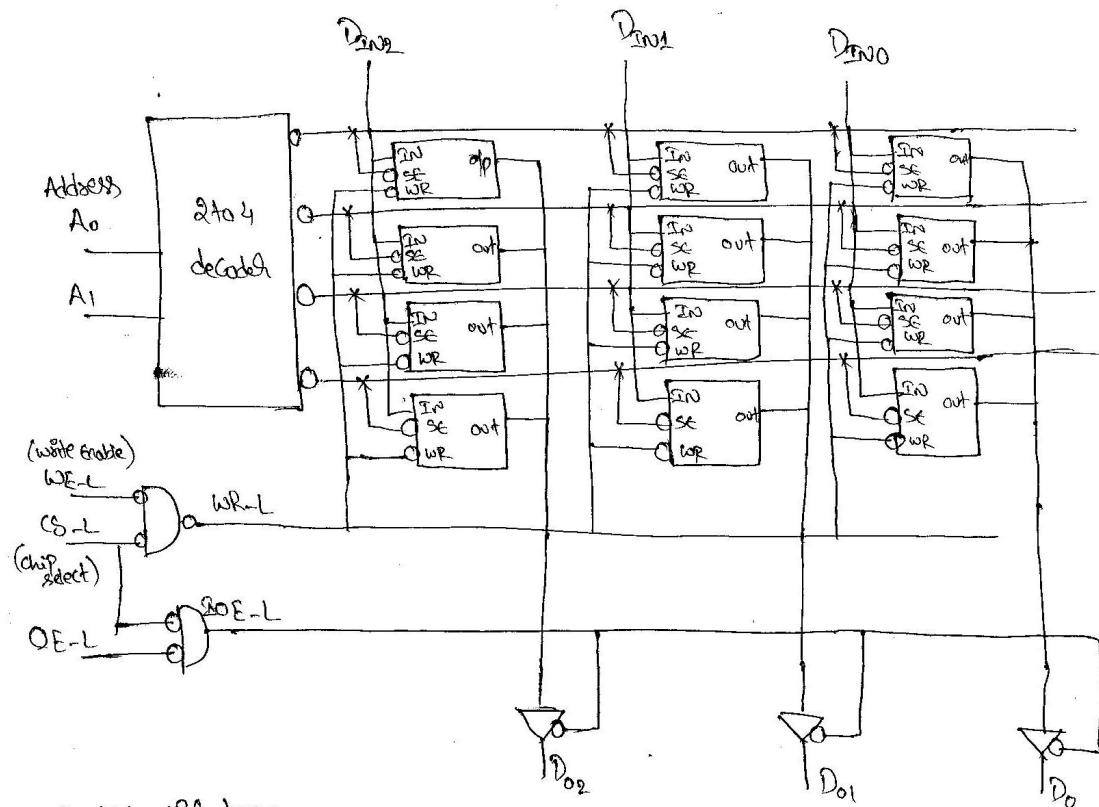
D-latch :-

Truth table

EN	D	Q	$\bar{Q}$	mode of operation
0	0	Q	$\bar{Q}$	Hold
0	1	0	1	Hold
1	0	Q	$\bar{Q}$	Reset
1	1	1	0	Set



## Internal structure of $4 \times 3$ Static RAM:-



### SRAM operation:-

- 1) During Read operation, the Q<sub>p</sub> data is a combinational function of the address, Q<sub>p</sub> as in a ROM. The Read operation is performed when chip select (CS) and Q<sub>p</sub> enable (OE) are asserted. The buffers at the bottom are activated when both (CS) and (OE) are asserted and the data stored in storage cells (D-flip flop) is delivered to the Q<sub>p</sub>.
- 2) During write operation, the Q<sub>p</sub> data is stored in latches the write operation is performed, when CS and WE are asserted by addressing the CS & WE the buffers are opened and the D-flip flop in the storage cells is activated. So the Q<sub>p</sub> data will be stored in the storage cells. Hence, the basic operation SRAM is Read and write the operation performed in (S-RAM).