

DIGITAL INTEGRATED CIRCUITS ANALYSIS

ELECTRONICS & COMMUNICATION ENGINEERING

HAND NOTES

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ANANTAPURAMU

Digital IC Applications:-

(1)

Unit - I

CMOS LOGIC:-

* Introduction to logic families:-

Collection of different IC chip that have similar op & o/p and internal circuit characteristics perform different logic functions.

- 1) Bipolar logic family
- 2) uni-Polar logic family.

1) Bipolar logic family:-

" " " are either Saturated (1) non Saturated Bipolar logic families.

These logic families differ in the major components that they use in their circuitry. Bipolar use 'Diode', whereas TTL & ECL use bipolar transistors as major circuit elements.

e.g:- RIL (Resistor Transistor logic)
 DCIL (Direct Control Transistor logic)
 IIL (Integrated Transistor logic)
 DIL (Diode " ")
 HIL (High threshold logic)
 TIL (Transistor - Transistor " ")

} Saturated Bipolar logic families:-
 ckt driven in to saturation is called saturated logic.

2) Non-Saturated Bipolar logic families:-

ckt which avoids saturation of their transistor are Non Saturated logic.

e.g:- Schottky TTL

ECL (Emitter Coupled logic).

(2)

3) Unipolar logic families :-

Metal Oxide Semiconductor are unipolar device where MOSFET transistors are principle component. because of the use of different principle component their electrical behaviors are different. //

*> CMOS logic levels :-

CMOS \rightarrow (Complementary Metal Oxide Semiconductor)

Basic building of CMOS is "MOS transistors".

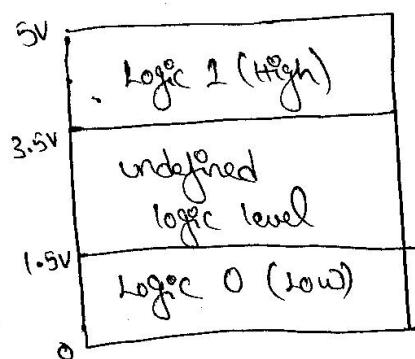
Logic levels :- CMOS logic levels operate from 5V Power Supply where

Range (0-1.5V) as a [logic '0'] ~~or~~ (L) [Low-level]

Range from (1.5V - 3.5V) is considered as [undefined logic level]

Range from (3.5V - 5V) is " " [logic '1'] & [High level].

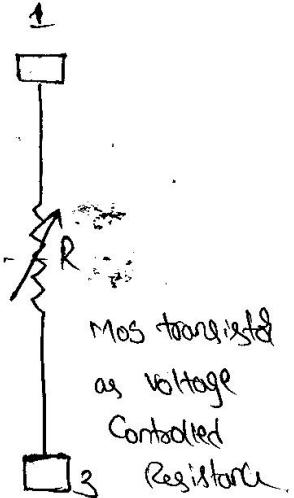
Range from (3.5V - 5V) is " "



*> MOS Transistor :-

" " is 3-terminal device acts like a "Voltage Controlled Resistance"

*) When an V_{GP} applied to one terminal 2
Controls the resistance b/w the two terminals..



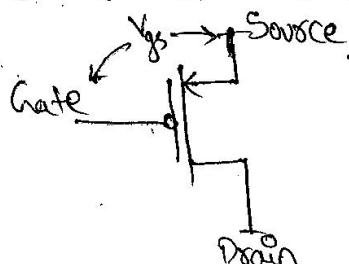
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There are 2-types of MOS transistors :-

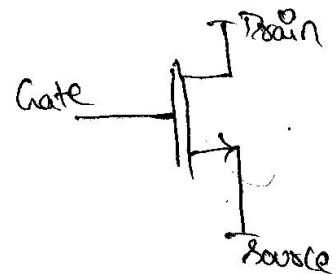
a) N-channel MOS (NMOS)

b) P-channel MOS (PMOS)

Where the MOS transistor has 3-terminals Gate, Source, Drain.



P-MOS transistor



N-mos transistor

$\rightarrow V_{gs}$ is normally zero (0) v.e

\rightarrow If $V_{gs} = 0$; then R_{ds} is very high.

\rightarrow If V_{gs} = enough v.e then R_{ds} is very low.

$\rightarrow V_{gs}$ is normally zero (0) v.e

\rightarrow If V_{gs} is '0' then R_{ds} is very high

\rightarrow If V_{gs} = enough v.e then R_{ds} is very low

\hookrightarrow The gate of MOS transistor is separated by Drain and Source by an insulating material with a very high resistance.

\hookrightarrow The voltage applied to gate terminal creates electric field

that enhances (or) retards the flow of current b/w Source and Drain. due to this field effect the MOS transistor is also known as MOSFET (metal oxide semiconductor field effect transistor).

MOSFET (metal oxide semiconductor field effect transistor) Regardless of gate voltage almost no current flows from gate to Source (or) from gate to drain. The resistance b/w gate and other terminals of device is extremely high. In order of few megohms.

The small amount of current that flow across this resistance is very small, typically less than one microampere and is called leakage current:

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*> Basic CMOS Inverted Circuit :-

Consists of 2-MOSFET's in series
whole P-channel device has its source
Connected to $+V_{DD}$ (a Positive Voltage) and
N-channel device connected to ground.

both Gates of two devices are connected
together to common V_{in} ; Drains connected to o/p's

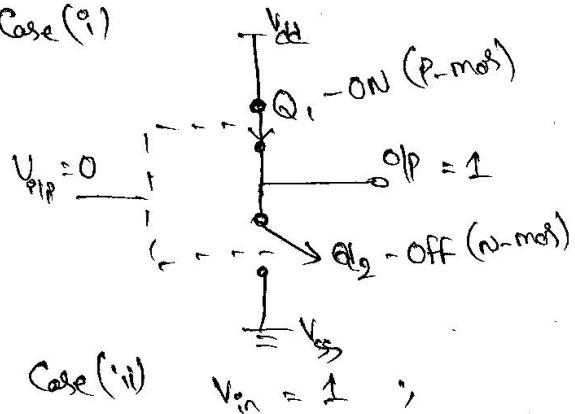
When V_{in} is High, the gate of Q_1 (P-channel)

is at 0V relative to source of Q_1 , i.e. $V_{gss1} = 0V$
Thus Q_1 is OFF; on other hand Q_2 - o/p is at $+V_{DD}$, i.e. $V_{gss2} = +V_{DD}$

$V_o = \text{logic 1 (d) High}$

Circuit Operation:-

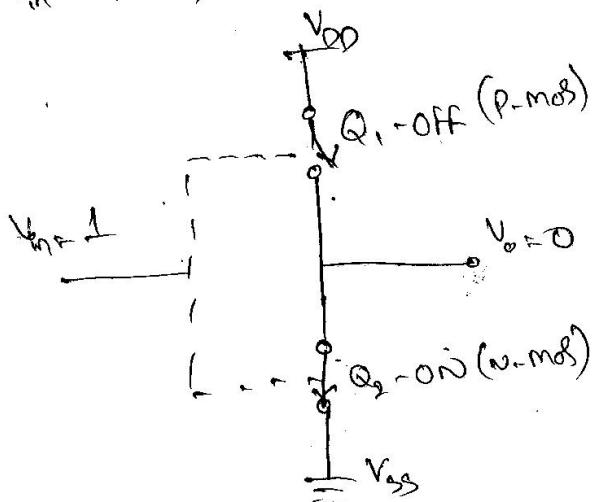
Case (i)



Case (ii)

$V_{in} = 1$;

V_{in}	P-mos	N-mos	O/P
0	ON	OFF	1
1	OFF	ON	0



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*> Transfer characteristics of CMOS Inverter :-

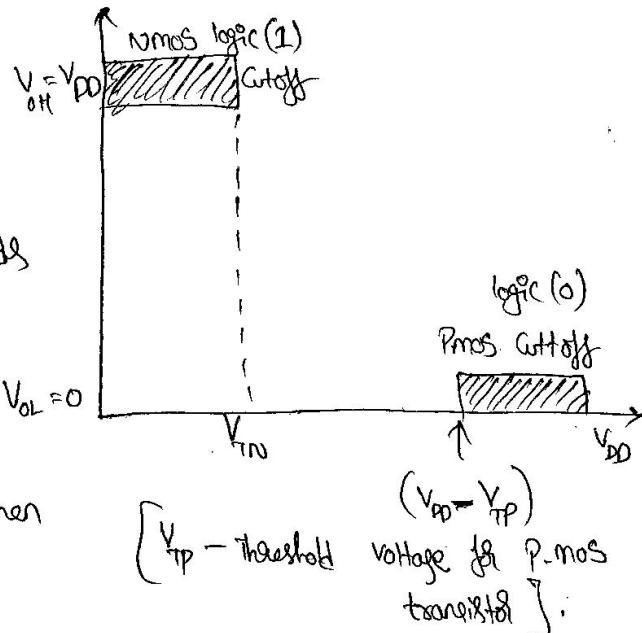
This shows Voltage transfer characteristics for CMOS inverter.

- *) The more positive op voltage corresponds to a logic '1' is $V_{DD} = V_{OH}$

- *) The more negative op voltage corresponds to a logic '0' is $V_{OL} = 0$

- *) When op is logic (0) state then $V_{OL} = 0$
P-mos transistor is cut off \Rightarrow

- *) When op is in logic (1) state then
N-mos transistor is cut off \Rightarrow



*> Noise Margin :-

This shows voltage transfer function of CMOS inverter

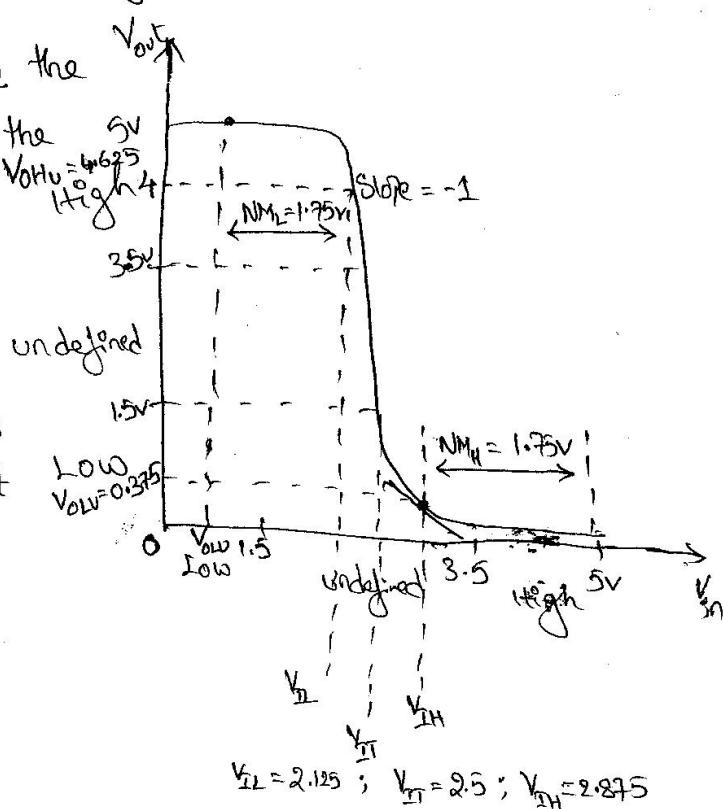
The parameter V_{IH} & V_{IL} determine the

noise margin and are defined as the

$$\text{Point } \frac{dV_o}{dV_i} = -1$$

for $V_i \leq V_{IL}$ and $V_i \geq V_{IH}$

the gain is less than unity and
the op changes slowly with input
voltage.



(6)

*> Electrical Behaviours of CMOS Circuits:-

Includes study of steady state electrical behaviours,
and dynamic electrical behaviours of CMOS circuits.

(A) CMOS Steady State Electrical Behaviours:-

(i) Logical Levels:-

normally CMOS circuits used in digital of two logic levels
logic (0) and logic (1).

This CMOS device manufacturer specifies 4 voltage parameters.

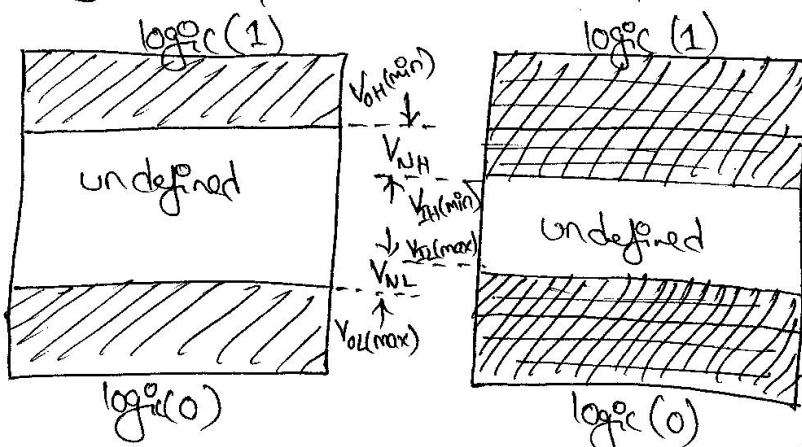
* $V_{IH(\min)}$ → High Level I_p Voltage :-
Minimum voltage required for logic (1) at
I_p. Any voltage below required level will not accept as a high
logic circuit.

* $V_{IL(\max)}$ → Low Level I_p Voltage :-
Maximum voltage level required for logic (0)
at I_p. Any voltage above required level will not accept
as a low by logic circuit.

* $V_{OH(\min)}$ → High level o_p voltage :-
Minimum voltage level at a logic circuit
o_p in logic (1) state under defined load conditions.

* $V_{OL(\max)}$ → Low Level o_p Voltage :-
Maximum voltage level at logic circuit
o_p in logic (0) state under defined load conditions.

(7)

(ii) Noise Margin :- o/p

(iii) Dc-Noise Margin :- Measured how much noise it makes to affect (F) damage a worst case o/p voltage into a value that may not be recognized properly by an o/p.

Given as

$$V_{NH} = \text{lowest Possible High o/p } (V_{OH(min)}) - \text{minimum voltage required for High o/p } (V_{IH(min)})$$

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

Similarly

V_{NL} = voltage diff b/w largest possible low o/p ($V_{OL(max)}$) and the maximum voltage $V_{IL(max)}$ required for low o/p.

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

(iv) Power Supply rails :- The Power supply voltage V_{DD} & ground are called Power Supply rails.

The CMOS logic levels are always function of Power supply rails.

$$V_{OH(min)} = V_{DD} - 0.1V ; V_{IH(min)} = 70\% \text{ of } V_{DD}$$

$$V_{IL(max)} = 30\% \text{ of } V_{DD} ; V_{OL(max)} = \text{Ground} + 0.1V$$

(V) Resistive Loads :-

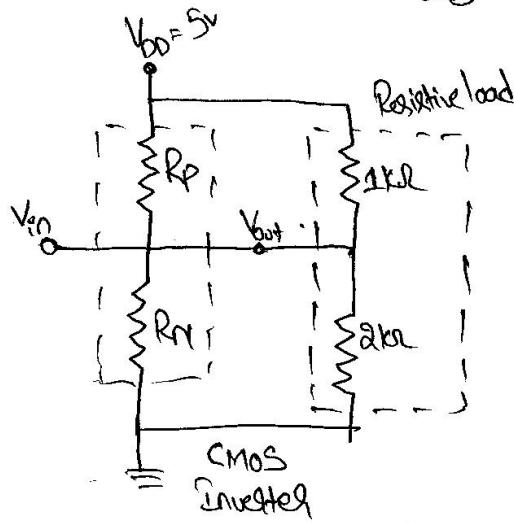
(8)

If impedance of CMOS gate is very high and therefore they consume very little current from circuit that drives them.

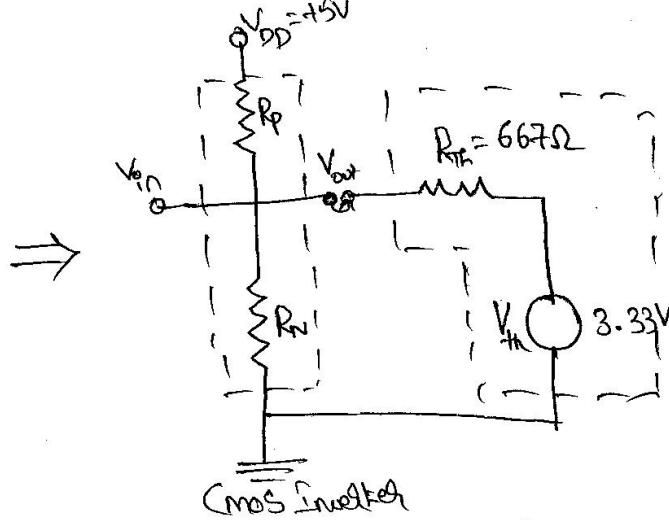
There are other devices such as discrete resistor, TTL gate, LED, relay which require non-trivial amounts of current to operate. These such device is connected to a CMOS op-amp we say Resistive load (or) DC load.

When op-amp of CMOS circuit is connected to a resistive load, the op-amp is not ideal.

The op voltage may be higher than 0.1V in low state and lower 4.4V in the High state.



R_P & R_N → Resistance of P-channel & N-channel.



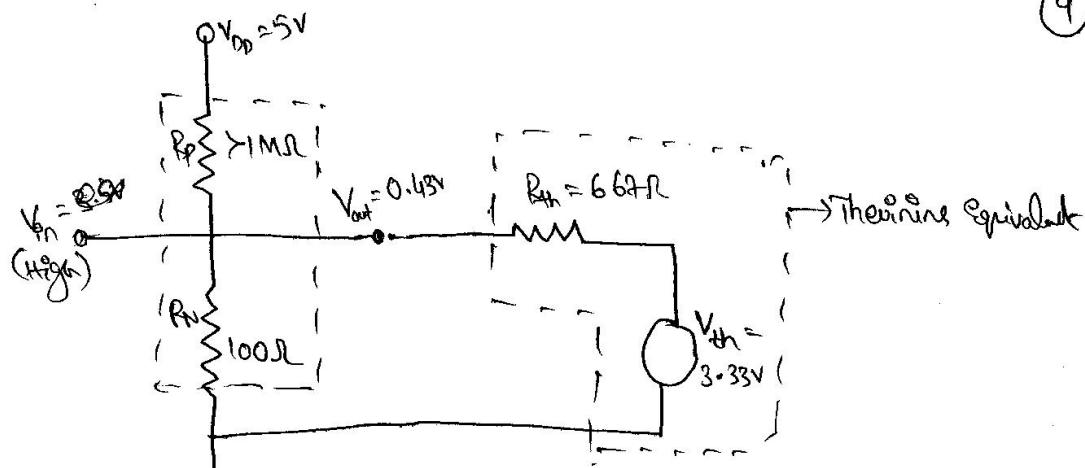
Thevenin's equivalent circuit

In normal operation depending upon op voltage (High or Low) one resistance is high ($> 1M\Omega$) and other is low (nearly 100Ω).

A resistive model for CMOS low op with resistive load

Therefore, Equivalent Circuit - is.

(9)

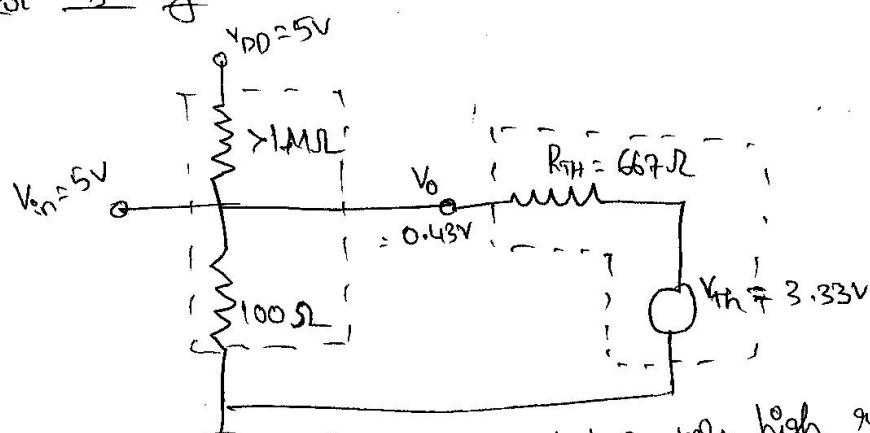


Q9- From Voltage divider rule

$$V_{th} = \frac{2k}{2k+1k} \times 5V = 3.33V$$

$$R_{th} = 1k \parallel 2k = 667\Omega$$

Case(i) Input is High:-



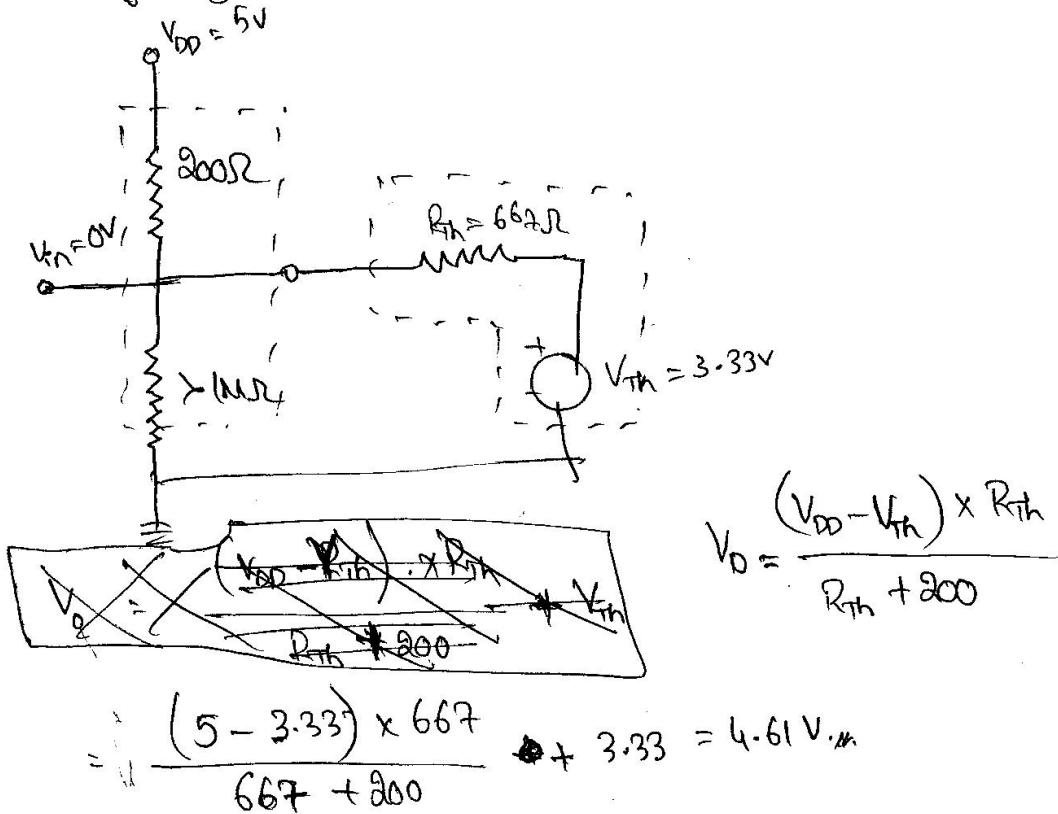
When q_{lp} is High P-channel is off and has very high resistance on the other hand n-channel is ON and has " low resistance say (100Ω) . The actual ON resistance depends on the CMOS family and other characteristics.

$$V_o = \frac{V_{th} \times 100}{(100 + 667)} = \frac{3.33V \times 100}{(100 + 667)} = 0.43V$$

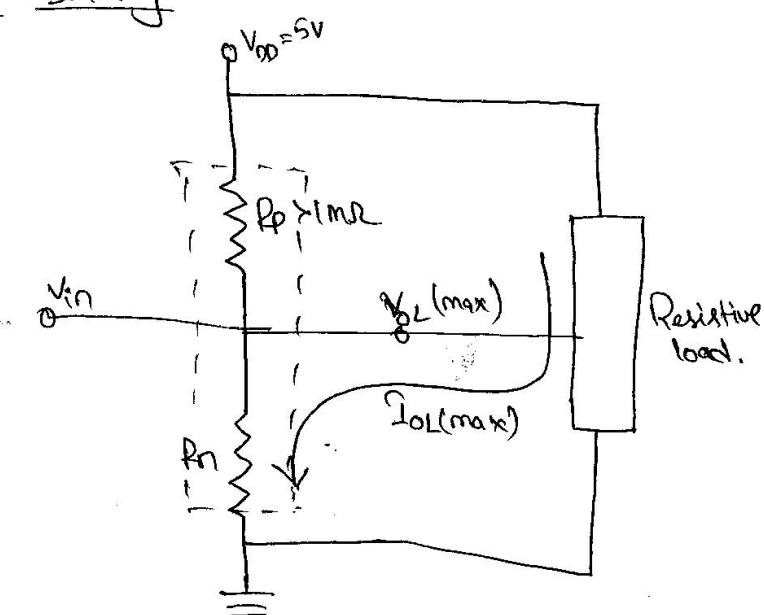
(Contd ii) Input is low:-

(10)

When V_{in} is low P-channel is ON and has low resistance say 200Ω . On the other hand N-channel is off and has high resistance.



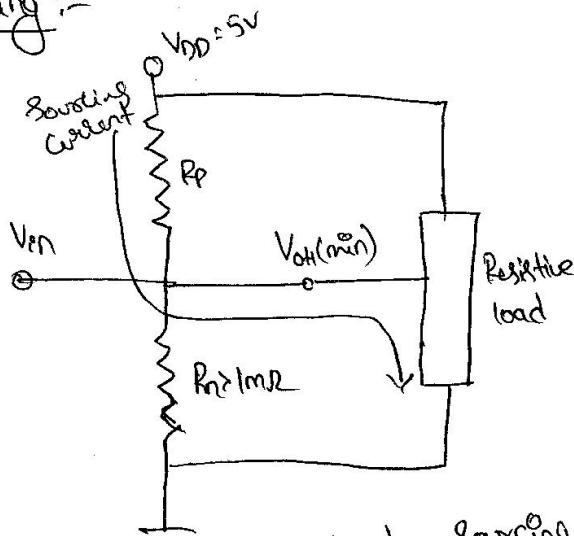
* Current sinking:-



(11)

A device Op is said to be sink current when Current flows from Power supply through the load and through the device Op to ground.

* Current Sourcing:



The Op is said to be current sourcing when Current flows from the Power Supply, out of the device Op and through the load to ground.

Note:- IC manufacturers specify a maximum load for Op in each state (for High or Low) and guarantee a worst case Op voltage for that load. The load specifies 2-tuples

$I_{OL(max)}$:- The maximum current that the Op can sink in the low state while still maintaining an Op voltage not greater than $V_{OL(max)}$

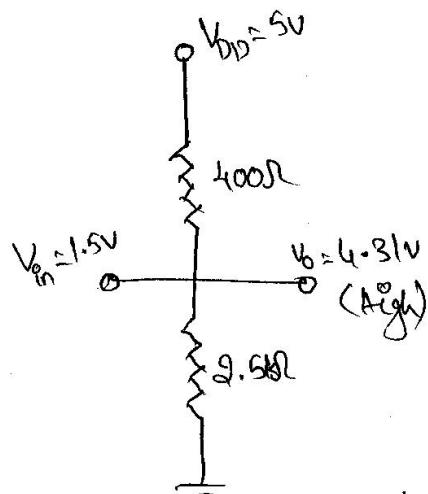
$I_{OH(max)}$:- The maximum current that the Op can source in the high state while still maintaining an Op voltage not less than $V_{OH(min)}$

* Circuit behaviour with Non ideal op's :-

(b)

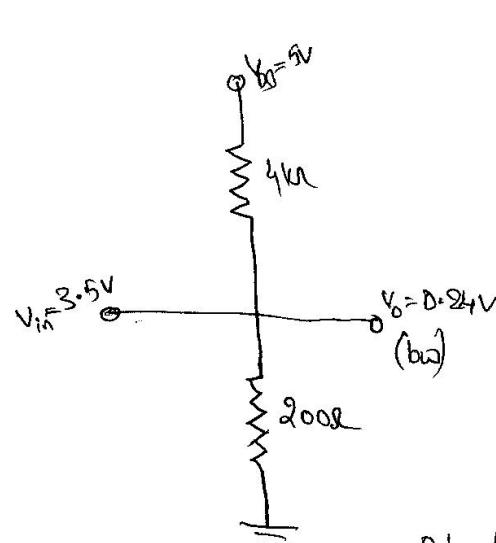
CMOS inverter may be ideal in all cases because it does not depend on op voltage but also on characteristics of load

The op's are not equal to Power Supply rails i.e. transistor may not be full ON (or) full off



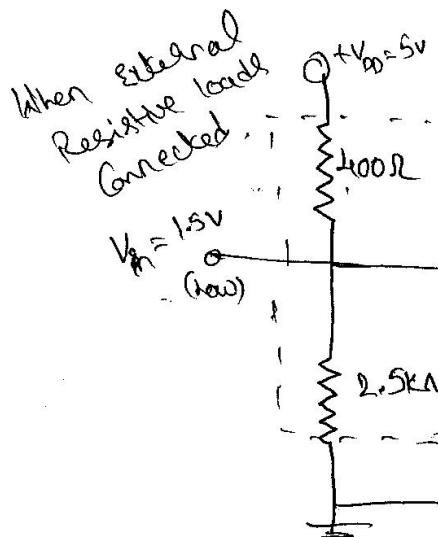
CMOS with non-ideal op

$$V_{out} = 5 \times \frac{2.5k\Omega}{2.5k\Omega + 400} = 4.31V$$

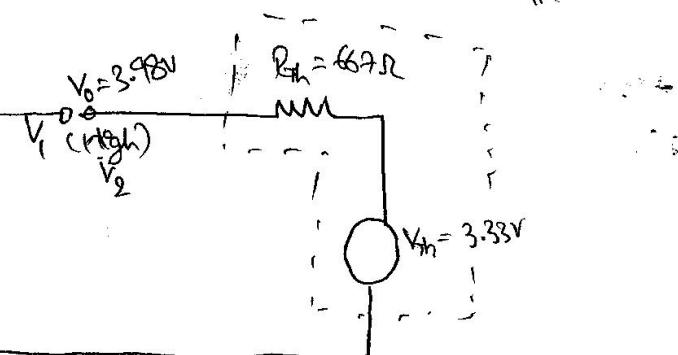


CMOS inverter with non-ideal op

$$V_{out} = 5 \times \frac{200}{200 + 4k\Omega} = 0.24V$$



CMOS inverter with load & non ideal op
V_in = 1.5V

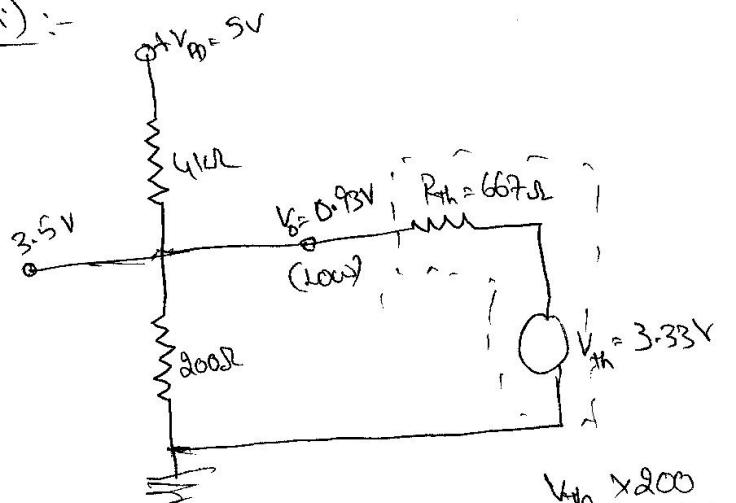


$$V_o = V_1 + V_2 = \frac{5 \times (2.5k\Omega \parallel 667)}{600 + (2.5k\Omega \parallel 667)} + \frac{3.33V (400 \parallel 2.5k)}{667 + (400 + 2.5k)}$$

$$= 2.8414V + 1.135V$$

$$= 3.98V$$

Case(ii) :-



$$V_o = \frac{V_{in} \times 200}{(200 + 667)} =$$

* CMOS Dynamic Electrical Behaviour:-

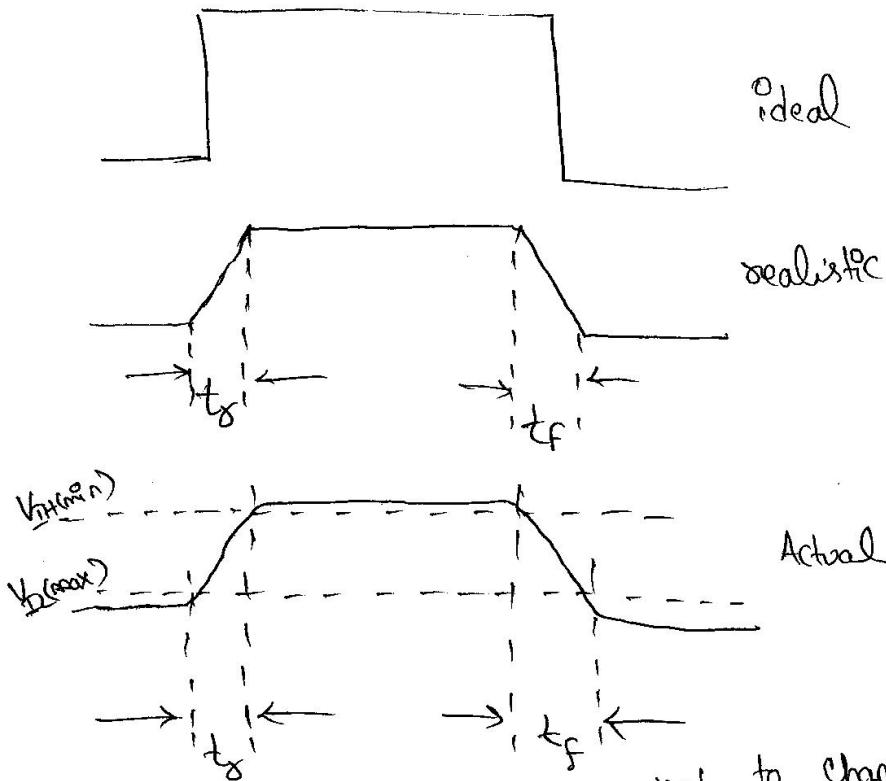
Depends on transition time & Propagation delay.
where the speed and power consumption of CMOS are mostly depended on dynamic characteristics of the device and its load.

(i) Transition time:-

The amount of time required that op of a logic circuit takes to change from one state to another is called transition time.

In practice the op cannot change instantaneously, because they need time to charge the stray capacitance of the wires and other components that they drive.

The stray capacitance is also called a capacitive load (or) AC load



Rise time (t_r) :- The time required to change from low to high.

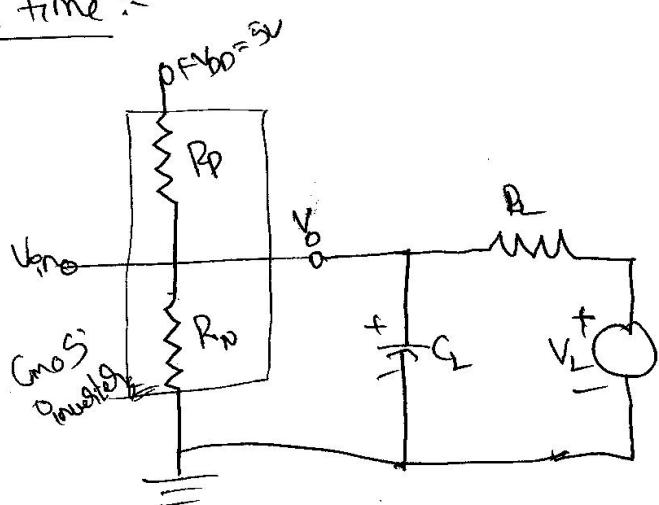
Fall time (t_f) :- The time required to change from high to low.

If we consider undefined region b/w low and high, the initial part of transition is not included in rise (or) fall times.

The Rise and fall time of CMOS depends mainly on

two factors, the ON transistor resistance and load capacitance.

Analysis of fall time :-



(15)

Equivalent load circuit consists of 3-components R_L , V_L & C_L

~~represents DC load~~

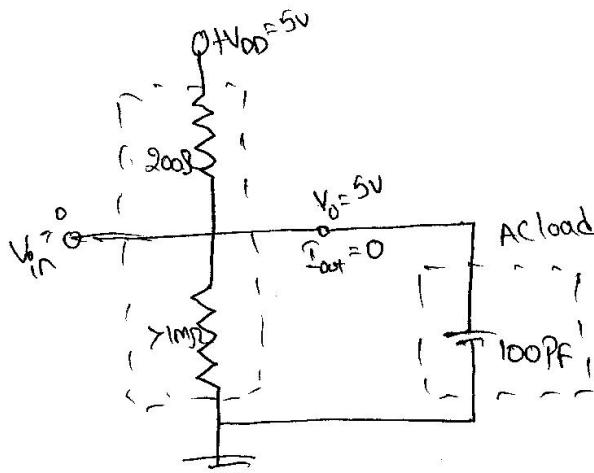
The R_L & V_L represents the DC load, which determine voltage and current that are present when the op-amp has settled in to static High (or) Low.

The C_L represents AC load, it determines the voltage and currents that are present while the op-amp is changing and how long it takes to change from one state to another.

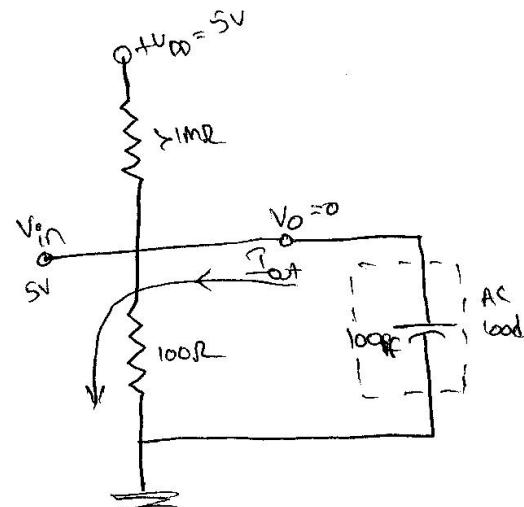
When CMOS drives only CMOS op-amps, the DC load is negligible.

Let us assume $R_L = \infty$, $V_L = 0$, $C_L = 100\text{ pF}$; $R_P = 200\Omega$;

$$R_n = 100\Omega$$



(a) High State



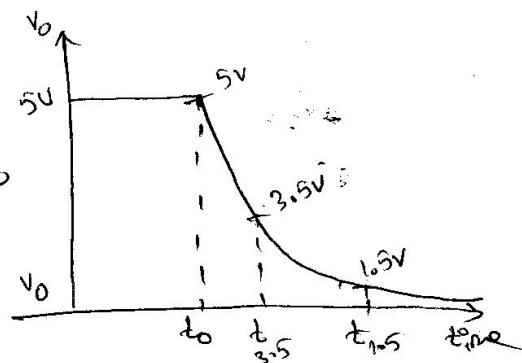
(b) Low State

Analysis of fall time:-

At time $t=0$; $V_{out} = 5V$ & $t=\infty$; $V_{out} = 0$

In this capacitor discharged and the value V_{out} is governed by exponential law

$$V_{out} = V_{DD} \cdot e^{-t/(R_n C_L)}$$



$$V_o = 5 \times e^{-t/(100 \times 100 \times 10^{-12})}$$

$$V_o = 5 \times e^{-t/(10 \times 10^9)}$$

The Product $R_L C_L$ is time constant. Here for High to Low transition time constant is 10×10^9 .

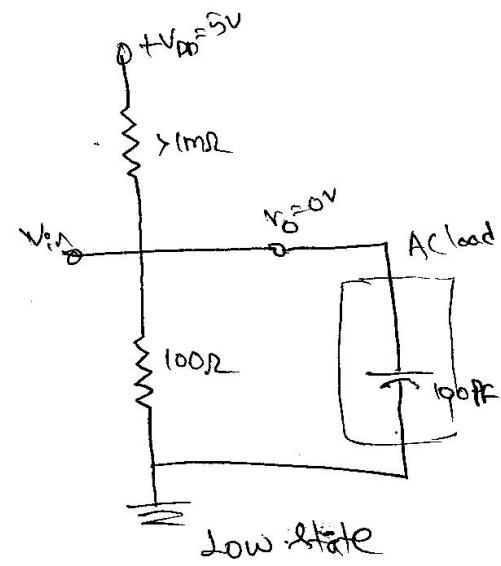
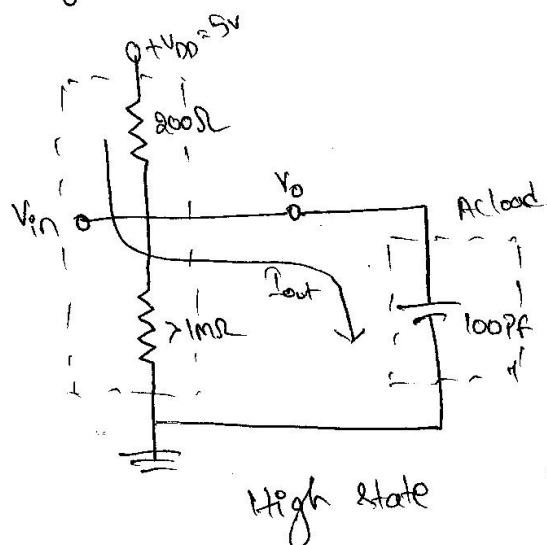
$$\text{for } t_{3.5} = -R_L C_L \ln \left[\frac{V_{out}}{V_{DD}} \right]$$

$$t_{3.5} = -10 \times 10^9 \ln \left[\frac{3.5}{5} \right] = 3.57 \text{ ns}$$

$$\begin{aligned} \text{for } t_{1.5} &= -R_L C_L \ln \left[\frac{V_{out}}{V_{DD}} \right] \\ &= -10 \times 10^9 \ln \left[\frac{1.5}{5} \right] = 12.04 \text{ ns} \end{aligned}$$

$$\therefore \text{fall time} = t_{1.5} - t_{3.5} = 12.04 \text{ ns} - 3.57 \text{ ns} \\ = 8.47 \text{ ns.}$$

Analysis of Rise Time :-



$V_o = V_{DD} \times \left(1 - e^{-t/(R_C C_L)}\right)$
 $= 5 \times \left(1 - e^{-t/(200 \times 100 \times 10^{-12})}\right) V$
 $= 5 \times \left(1 - e^{-t/(20 \times 10^{-9})}\right) V$

The RC time constant in this case is 20×10^{-9}

for $V_o = 3.5$ & $V_o = 1.5 V$

$$\begin{aligned}
 t_{3.5} &= -R_C \ln \left[\frac{V_{DD} - V_o}{V_{DD}} \right] \\
 &= -20 \times 10^{-9} \times \ln \left[\frac{5 - 3.5}{5} \right] \\
 &= 24.08 \text{ ns}
 \end{aligned}$$

$$\begin{aligned}
 t_{1.5} &= -R_C \ln \left[\frac{V_{DD} - V_{out}}{V_{DD}} \right] \\
 &= -20 \times 10^{-9} \times \ln \left[\frac{5 - 1.5}{5} \right] \\
 &= 7.13 \text{ ns}
 \end{aligned}$$

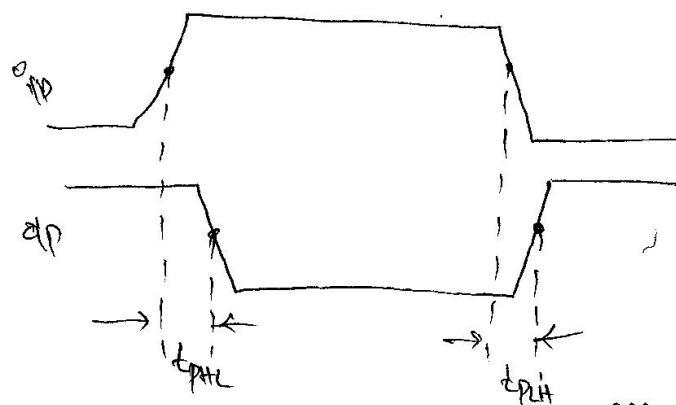
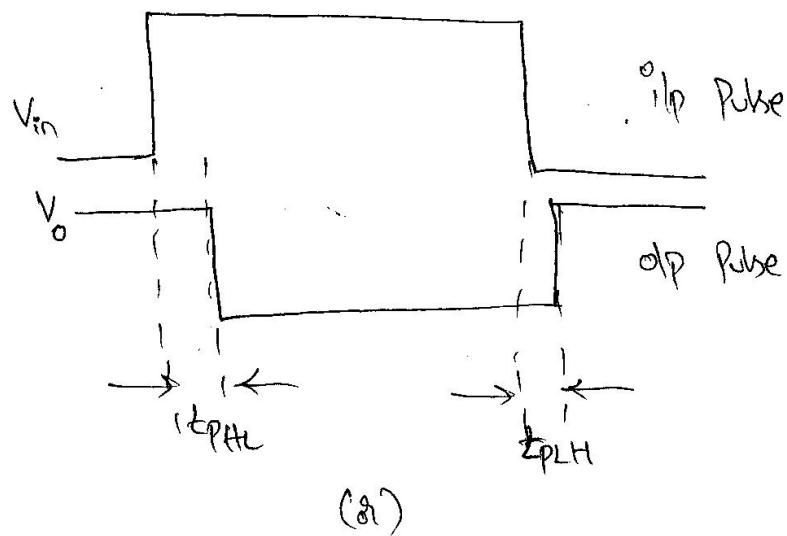
∴ Rise time $t_r = t_{3.5} - t_{1.5}$
 $\approx 24.08 \text{ ns} - 7.13 \text{ ns} = 16.9 \text{ ns}$

b) Propagation delay:-

Depends on amount of time that it takes for a change in QP signal to produce OLP signal.

The Propagation delay of a gate is basically the time interval b/w the application of an QP Pulse and occurrence of the resulting OLP Pulse.

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Propagation delay is measured in mid point of transition.

t_{PDL} :- time b/w an op change and corresponding op change when op is changing from High to Low.

t_{PLH} :- time b/w an op change and corresponding op change when the op is changing from Low to High.

Factors causing Propagation delay:-

- a) Op Capacitance and op load
- b) Transition state charge of mos
- c) Semiconductor material used in manufacturing
- d) Multistage device such as non-inverting gates.

c) Power Consumption :- (Static Power dissipation):-

The Power Consumption of a stable CMOS circuit whose op is not changing is known as static Power dissipation.

(i)

Defined as the amount of Power Consumed by CMOS Circuits when it is in Stable state.

(ii) Dynamic Power dissipation:

The amount of Power Consumed by CMOS circuit when it is in transition state.

Expression for dynamic Power dissipation:

Total Power dynamic dissipation is

$$P_D = P_f + P_L \rightarrow ①$$

$$P_f = C_{PD} \times V_{CC}^2 \times f \rightarrow ②$$

where $P_f \rightarrow$ internal Power dissipation of CMOS due to op.

$V_{CC} \rightarrow$ Power supply

$f \rightarrow$ Transistor frequency of op signal

$P_L \rightarrow$ Power dissipation by Capacitive load

$C_L \rightarrow$ Load Capacitance

$$\therefore P_L = C_L \times \left(\frac{V_{CC}^2}{2} \right) 2f = C_L V_{CC}^2 f \rightarrow ③$$

Now $\therefore ①$

$$P_D = C_{PD} V_{CC}^2 f + C_L V_{CC}^2 f$$

$$P_D = V_{CC}^2 f (C_{PD} + C_L)$$

$$P_D = V_{CC}^2 f \times C \quad (\text{where } C_{PD} + C_L = C).$$

* (MOS Logic families:-)

(20)

The Commercially available CMOS families.

- a) 4000 Series (mos)
- b) 74 Series HC (High speed (mos))
- c) 74 " HCT (High speed CMOS, TTL compatible)
- d) VHC (Very High Speed (mos))
- e) VHCT (" " " , TTL compatible)
- f) FCT (Fast CMOS, TTL compatible)
- f) FCT-T (" " " with V_{OH}) "

a) 4000 Series CMOS :- first commercially available CMOS family was 4000 series although 4000 series family offered a benefit of low power consumption, they were fairly slow and not easy for interface with most popular families of TTL.

b) HC and HCT families :-

The Prefix 74 is simply a number that was used by early TTL family. The first two 74 series CMOS families are HC and HCT [High speed CMOS & High speed CMOS, TTL compatible]. These families have higher speed and better sinking and sourcing capability than 4000 series.

This family having Power supply voltage same as TTL, +5V.

The Power supply voltage range from HC family is 2V to 6V.

This higher power supply voltage used for higher speed and lower voltage used for lower power dissipation. *

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⇒ VHC and VHCT families:-

In 1980 & 1990's two more CMOS families were introduced. These families are twice fast as HC/HCT families and they maintain backward compatibility with their predecessors.

⇒ FCT and FCT-I families:-

In 1990 another family called FCT was introduced. The main advantage of this family is to meet (f) exceed the speed and the op done compatibility with TI. The FCT family has drawback of producing full 5V CMOS V_{DD} creating enormous power dissipation and noise as its op voltage swing from 0-5V.

In FCT-I family was quickly introduced to reduce the drawback of FCT family. By the high level of op is reduced, thereby reducing both power consumption and switching noise while maintaining high speed operating.

* CMOS Three State Buffer (T₃S State Buffer):-

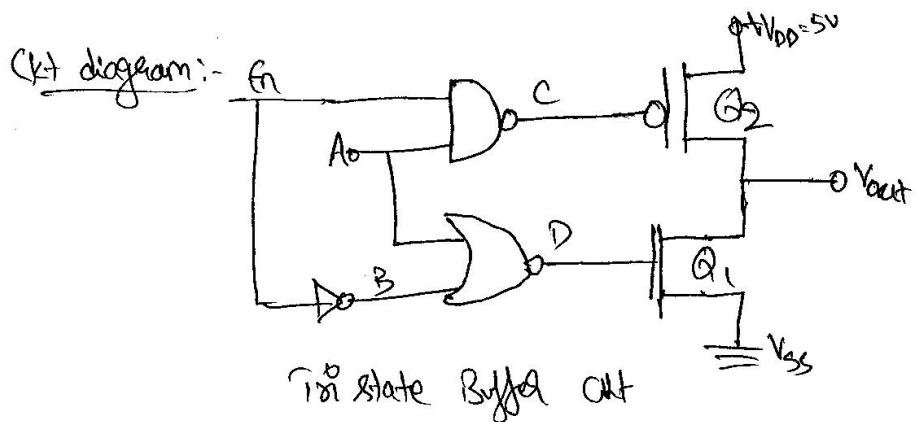
An op with 3-Possible states is called 3-state op. T₃S state Buffer is similar to ordinary buffer except that it has an extra op called Enable op.

Symbol:-



CMOS T₃S State Symbol

Ckt diagram:-



functional table:-

G1	A	B	C	D	Q1	Q2	dP
0	0	1	1	0	OFF	OFF	Hi-Z
0	1	1	1	0	OFF	OFF	Hi-Z
1	0	0	1	1	ON	OFF	Low
1	1	0	0	0	OFF	ON	High

(31)