Code: 9D06101

M.TECH - I Semester Regular and Supplementary Examinations, April/May 2012

DIGITAL SYSTEM DESIGN

(Common to DSCE and DECS)

Time: 3 hours Max Marks: 60

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) How does the ASM chart differ from a software flow chart?

(b) Draw an ASM chart of JK flip flop. Realize it using SR flip flop and required gates.

2 (a) Describe important features of FPGA.

(b) Draw the general structure of a CPLD and explain how a logic function can be realized on CPLD with simple example.

3 (a) Write short notes on intermittent faults.

(b) Explain how Kohavi algorithm is useful in deflection of faults in digital circuits.

4 (a) Describe the algorithmic steps involved in D-algorithm.

(b) Write short notes on random testing.

5 (a) Distinguish between mealy and Moore machines.

(b) Classify the fault detection experiments for the sequential circuit

6 (a) Explain the various types of cross point fault that occur in PLAs.

(b) Explain PLA folding.

7 (a) Plot the following PLA on the map. Identify the undetectable faults. Derive a minimal test set for all detectable faults.

X_1	X_2	X_3	X_4	Z_1	Z_2
1	2	0	1	1	0
2	0	1	1	1	0
1	1	0	2	1	1
0	1	1	0	0	1

(b) Discuss different fault models.

8 Write short note on any Two:

(a) Flow model.

(b) Minimal closed covers.

(c) Cycles and hazards.

*****

Code: 9D06101

M.Tech - I Semester Supplementary Examinations, November 2012

DIGITAL SYSTEM DESIGN

(Common to DSCE, DECS and ECE)

Time: 3 hours

Max Marks: 60

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Develop an ASM chart of D flip flop and realize it using only NAND gates.

(b) Discuss about reduction of state tables.

2 (a) Design a four-way traffic light controller that will keep traffic moving efficiently along two busy streets that intersect. Implement the controller using PALs.

(b) Write an example explain how a logic function can be realized on FFGAs.

3 (a) Write short notes on bridging faults.

(b) Discuss the features of path sensitization technique.

4 (a) Describe the algorithmic steps involved in PODEM.

(b) Write short notes on testing for bridging faults.

5 (a) Give the steps involved in design of fault detection.

(b) Convert the following mealy machine into a corresponding Moore machine.

PS		
A	B,O	G,O
B	E,O	D,O
C	D,I	A,O
D	C,I	E,O
E	B,O	D,O

6 (a) Describe the advantages of PLA minimization and folding.

(b) Describe the types of cross point fault that occur in PLAs.

7 (a) Explain how test generation can be achieved in testing a PLA.

(b) Apply PLA minimization procedure and obtain the minimized expression to be implemented on PLA. F = 2021 + 0022 + 1200

8 Write short note on:

(a) Minimal closed covers.

(b) Races and hazards.

*****

M. Tech I Semester Regular Examinations, April/May 2013

DIGITAL SYSTEM DESIGN

(Common to DSCE, DECS, ECE and MNE)

Time: 3 hours Max. Marks: 60

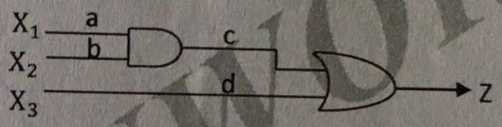
Answer any FIVE questions.
All questions carry equal marks.

*****

1 (a) With an example, explain the use of ASM charts in the design of digital circuits.
(b) What is HDL? What are the major differences between VHDL and verilog HDL?

2 (a) Tabulate the truth table and implement the following using ROM with capacity 4×2 ROM.
$F_1 (A, B) = \sum (1, 2, 3)$
$F_2 (A, B) = \sum (0, 2)$
(b) Describe some important features of an FPGA and CPLD.

3 (a) Explain how a fault in a circuit is diagnosed and also describe the testing process.
(b) Draw the table giving the set of all possible single struck faults and the faulty and fault free responses and also construct the fault cover table for the circuit shown in below.



4 (a) With an example, discuss in detail about determination of stuck-at-faults using D-algorithm.
(b) With an example, explain the transition count testing method and also mention a few advantages of this method.

5 (a) Classify the fault detection experiments for the sequential circuits.
(b) What is the difference between 'Melay' and 'Moore' models of sequential machines? Explain using structural diagrams.

6 (a) Briefly describe about PLA folding.
(b) Minimize the following function implemented on PLA using IISC algorithm.

7 (a) Discuss different fault models.
(b) Explain how test generation can be achieved in testing a PLA.

8 (a) Discuss about races, cycles and hazards in connection with asynchronous sequential machine design.
(b) Write short notes on flaw table.

*****

Code: 9D06101a

M.Tech - I Semester Regular Examinations, April/May 2013

DIGITAL SYSTEMS DESIGN

(Common to VLSIES, ESVLSI and VLSIESD)

Time: 3 hours

Max Marks: 60

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Develop an ASM chart of D flip flop and realize it using only NAND gates.

(b) Discuss in detail about hardware description language and control sequence method.

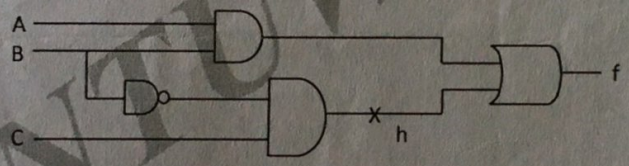
2 (a) Describe some important features of an FPGA and CPLD.

(b) Design a four way traffic light controller that will keep traffic moving efficiently along two busy streets that intersect. Implement the controller using PALs.

3 (a) What is the significance of Kohavi algorithm? Explain how it detects multiple faults in a two level networks with a simple example.

(b) Discuss the different types of faults in digital circuits.

4 (a) Apply D-algorithm to detect 'h' SAO fault in the given circuit and derive the test vector.



(b) Write with an example the transition count testing method.

5 (a) Distinguish between Mealy and Moore machines. Explain using structural analysis.

(b) The response of the machine shown in table below to an unknown input sequence is give to the experimenter. Explain a procedure that the experimenter may use in order to identify the initial state. What are the minimum-length sequences that will make such an identification possible?

PS	NS	
	x = 0	x = 1
A	A, 0	B, 0
B	C, 0	D, 0
C	D, 1	C, 1
D	B, 1	A, 1

Contd. in Page 2

Code: 9D06101a

6 (a) Apply PLA maximization procedure and obtain the minimized expression to be implemented on PLA. F = 2021 + 0022 + 1200.

(b) Design a 3-bit BCD to grey code converter and realize the circuit using PLA and then show that how folding will reduce the number of cross points given on the PLA.

7 (a) Plot the following PLA on the map. Identify the undetectable faults. Determine a minimal test set for an detectable faults.

x_1	x_2	x_3	x_4	z_1	z_2
0	2	2	1	1	0
2	1	1	2	1	1
0	1	2	1	0	1

(b) Discuss the BIST scheme for PLD and CPLDs.

8 Write a short note on:

(a) Races, cycles and hazards.

(b) State reduction with example.

(c) Flow table with example.

*****