

ELECTRONIC CIRCUITS AND APPLICATIONS

SUMMARY

Unit – 1

Amplifiers:

- Amplifiers can be classified based on configuration, operating point, number of stages, type of output, frequency range, band width and devices used(BJT or FET)
- CE stage has large current gain, voltage gain and power gain. Output voltage has 180° phase shift with respect to input it has moderate input impedance
- CC stage has high current gain, unity voltage gain, good power gain = current gain. It has no phase shift of output with respect to input. It features high input impedance and low output impedance
- CB stage has current gain < 1 , high voltage gain and power gain. There is no phase shift in current or an voltage. It has large output and low input impedance
- For low frequency BJT can be represented by H parameters for AC. It can also be represented in “re” model.
- The parameters are specified at a particular operating point and they change with operating point.
- FET amplifier also can be represented in CS, CD, CG, in a similar way to BJT.
- For simplified case CE can be represented by h_{ie} at input and a current source of $h_{fe} \cdot i_b$ at output in h model.
- In re model it can be simplified as βr_e at input and βi_b at output
- A common collector stage can be simplified to βh_{ie} at input.
- A CB stage can be simplified to h_{ie} at input and current source $h_{fb} \cdot i_e$ at output. However h_{fb} is approximately = 1
- A CS amplifier is simplified to open circuit at input and a current source of $g_m V_{gs}$ at output

STABILIZING

- Q operating point is determined by drawing load line and finding intersection point with specified base current.
- Operating point moves up with increase of I_b and moves down with decrease of I_b
- The location of Q and signal amplitude are confined to active region
- When BJT is cutoff $V_c = V_{cc}$ and when in saturation $I_c = V_{cc} / R_L$ (approx.)

COUPLING AND BYPASS CAPACITORS

- Coupling capacitors together with R_L and R_i determine low frequency cutoff. Shunt capacitors and input capacitance together with R_L and R_i determine HF cutoff f_2 .

HYBRID π MODEL

- At high frequencies BJT can be better represented by π model. The resistors are r_{bb}^1 , r_{b^1e} , r_{μ} , r_{ce} and at output a current source $= g_m v_{b^1e}$ is used. b^1 is an imaginary internal base in addition to physical terminal.
- Important parameters are $g_m = I_c / V_t$; $r_{b^1} = h_{fe} / g_m$;
- $r_{bb}^1 = h_{ie} - r_{b^1e}$; $r_{b^1c} = r_{b^1e} / h_{re}$; $g_{ce} = 1 / r_{ce} = h_{oe} - (1 + h_{fe}) g_{b^1e}$
- Current gain $A_i = -h_{fe} / (1 + j(f/f_{\beta}))$
- $f_{\beta} = 1 / 2\pi r_{b^1e} (c_{b^1e} + c_{b^1c}) \approx 1 / 2\pi r_{b^1e} c_{b^1e}$
- $f_{\beta} = \beta$ cutoff frequency
- Similarly f_{α} can be defined as $f_{\alpha} = \frac{h_{fe} \cdot f_{\beta} (c_{b^1e} + c_{b^1c})}{c_{b^1e}} \approx h_{fe} \cdot f_{\beta} \approx F_t$
- f_{β} = frequency at which current gain falls by $1/\sqrt{2}$ (h_{fe})
- α cutoff frequency is the frequency at which α falls to 0.707
- F_t is gain bandwidth product where current gain = 1.
- $f_t = h_{fe} \cdot f_{\alpha} = \frac{g_m}{2\pi(c_{b^1e} + c_{b^1c})} = \frac{g_m}{2\pi c_{b^1e}}$

HYBRID CONDUCTANCES

- $g_m = \partial I_c / \partial v_{be} = I_c / V_t$
- $g_{b^1e} = 1 / r_{b^1e}$ = input conductance
- $g_{b^1c} = 1 / r_{b^1c}$ = feed back conductance
- $g_{ce} = 1 / r_{ce}$ = output conductance
- above in terms of others are
- 1) $g_m = |i_c| / v_t$ 2) $g_{b^1e} = 1 / r_{b^1e} = g_m / h_{fe}$ 3) $r_{bb}^1 = h_{ie} - r_{b^1e}$
 - 4) $r_{b^1c} = r_{b^1e} / h_{re}$ or $g_{b^1c} = h_{re} / r_{b^1e}$
 - 5) $g_{ce} = 1 / r_{ce} = h_{ie} - (1 + h_{fe}) g_{b^1c}$

HYBRID CAPACTANCES

- 1) Transition capacitance c_{b^1c} due to reverse biased cb junction
- 2) diffusion capacitance c_e of be junction.
- 3) $C_e \propto I_e$; $C_e = g_m \cdot W^2 / 2D_e$

VARIATION OF HYBRID PARAMETER

- hybrid parameters are considered linear up to $f_t/3$
- g_m is independent of V_{ce} but varies directly with $|i_c|$ and inversely with T .
- r_{bb}^1 decreases with I_c and increases with temperature
- r_{b^1e} decreases with I_c and increases with temperature
- $C_e \propto I_c$ and decreases with V_{ce}
- h_{fe} decreases on either side of a particular value of I_C
- h_{ie} decreases with i_c .

UNIT – II

MULTISTAGE AMPLIFIER

- In order to achieve high voltage and power gain, drive low impedance output & take input from high / low impedance sources, to achieve high gain and band width there is a need to employ more than One amplifiers in cascade.
- Three coupling scheme are employed. They are direct coupled DC, RC coupled and transformer coupled between Two stages of amplifiers.
- Only DC amplifier gives bandwidth down from DC.
- DC output DC voltage effects input of next stage.
- DC biasing can be independently designed and used in RC coupled amplifier and inter stage coupling is done by suitable value of coupling capacitors. This capacitors determines low frequency cut off.
- At mid band couple capacitors, emitter / source by-pass capacitors offer low / short resistance in the circuit.
- Transformer coupling isolate DC and can be employed to match input impedance to required output impedance between stages. Transformer coupling like RC determines low frequency cutoffs. It also suffer from result frequency of primary and secondary windings.
- Effective load on multistage amplifier is determined by capital R_{L1} and R_{i2} still parallel.
- Overall voltage gains $V_0 / V^i = A_{v0} \cdot A^{v1} \dots \dots \dots A_{vn}$. and phase shift $\theta_n = \theta_1 + \theta_2 \dots \dots \dots \theta_n$
- Overall current gain $A_{in} = A_{i1} \cdot A_{i2} \dots \dots \dots A_{in}$
- $A_{ik} = -h_{fek} / (1 + h_{oe} \cdot R_{in})$
- $R_{in} = h_{ie} + h_{re} A_{in} R_{in}$
- For estimating input impedance multistage amplifier start from last stage to determines A_{in} , R_{in} , & proceed back to first stage progressively
- .
- Output impedance of first stage $R_{O1} = 1/y_{01}$; $y_{01} = h_{oe} - \frac{h_{re} \cdot h_{fe}}{h_{ie} + R_s}$

$$\blacksquare \quad R_{O1} = \frac{R_{O1} R_{C1}}{R_{O1} + R_{C1}}$$

R_{O1} forms source impedance to calculate Y_{02} for second stage.

REVIEW OF BJT AMPLIFIERS

- | | |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CE | $A_i = h_{fe} / (1 + h_{re} \cdot Z_i)$; $A_v = A_i \cdot Z_L / Z_i$; $Z_i = h_{ie} - h_{fe} \cdot h_{re} / (Y_L + h_{oe})$
$Y_0 = h_{oe} - h_{fe} h_{re} / (h_{ie} + R_s)$
Approximately $A_i = h_{fe}$; $A_v = h_{fe} R_L / R_i$; $R_i = h_{ie}$ |
| CB | $A_i = h_{fb} / (1 + h_{ob} R_L)$; $Z_i = h_{ib} + h_{rb} A_i Z_L$
$A_b = A_i \cdot R_L / R_i$; $R_o = 1/Y_0$; $Y_0 = h_{ob} - h_{fb} h_{rb} / (h_{ib} + R_s)$
Approximately $A_i = h_{fb} = \alpha$; $A_v = h_{fb} R_L / r_e$; $R_v = \infty$ |
| CC | $A_i = 1 + h_{fe}$; $Z_i = (1 + h_{fe}) R_L$; $A_v = 1 - h_{ie} / R_i$
$Z_0 = (h_{ie} + R_s) / (1 + h_{fe})$
Approximately $A_i = (h_{fe} + 1)$; $Z_i = h_{fe} R_e$; $Z_0 = r_e$ |

REVIEW OF FET

CS	$Z_i = R_g$; $A_v = -g_m R_L$; $Z_o = R_L$ Approximately $Z_i = \infty$; $Z_o = \infty$; $A_v = -g_m R_L$; $\mu = g_m r_p$
CG	$A_v = (g_m r_d + 1) R_d / (r_d + R_d)$
CD	$A_v = g_m R_s / (1 + g_m R_s)$

DISTORTIONS

- Non linear distortion is caused by non linearity of collector / drain currents and voltages
- Frequency distortion is caused by variation of gain with respect to frequency. These are determined by passive capacitors in coupling input output.
- Phase distortion is counter part of frequency distortion. Phase shift varies with frequency. Caused by coupling capacitors and capacitors at input and output.

FREQUENCY OF AMPLIFIERS

- Frequency and phase shift response is plotted by BODE plots.
- $A = A_0 / (1 + j f/f_p)$; $f_0 = 1 / (2\pi R_1 C_1)$, $\theta = \tan^{-1} (f/f_p)$
- Slope of gain is 20 db/decade or 6db/octave. Octave means frequency ratio of $1/2$ or 2. For multistage amplifier $A = A_0 / (1 + jf/f_{p1})(1 + jf/f_{p2}) \dots (1 + jf/f_{pn})$
- $f_{p1} \dots \dots \dots f_{pn}$ are called poles of response
- If poles are at least 4 times apart from each other, lowest of these called dominant pole and overall cutoff frequency is determined by dominant pole.

STEP RESPONSE

- If hf response can be very efficiently be determined by response to step input.
- t_r = rise time is time taken for 10 to 90% of steady state. $T_r = .35/BW$
- Tilt gives indication of low frequency cutoff.
- % tilt $P = t_1 / (R_1 C_1) \times 100\%$.
- Overall f_H is given by $\frac{1}{\sqrt{1 + (f_{H*} / f_{H1})^2}} \times \dots \times \frac{1}{\sqrt{1 + (f_{H*} / f_{Hn})^2}} = 1/\sqrt{2}$
- For 'n' amplifiers of same f_H $f_{H*} / (f_H) = \sqrt{(2^{1/n} - 1)}$
- For $f_L^* / (f_L) = 1 / \sqrt{(2^{1/n} - 1)}$
- Empirically $1/f_H = 1.1 \sqrt{(1/f_1^2 + 1/f_2^2 \dots + 1/f_n^2)}$
- $t_r = 1.1 \sqrt{(t_{r1}^2 + t_{r2}^2 + \dots + t_{rn}^2)}$

MILLER EFFECT

- The feedback capacitance between output and input can be represented either at input or at output by using millers theorem.
- At input $C = (1+A)C_c$, at output $C_c A / (1-A)$
- This method is very effective and useful in simplifying amplifier analyzed by hybrid π circuit.

OTHER MULTISTAGE AMPLIFIERS

- Transformer coupled amplifier isolates to stages of amplifiers. Tran ratio of primary to secondary is determined to match impedances
- Inductance determines low cutoff frequency of the amplifier.
- While determine turns ratio winding resistance forms part of impedances being matched.
- An impedance R_l is reflected to primary as $(n_1/n_2)^2 R_l$
- Low cutoff frequency f is determined by $2 \pi f L = R_0$
- Cascade amplifier consists of CE feeding to CB. This amplifier completely isolates impedances $A_v = g_{m1} R_c$ where R_c is collector resistance of CB
- Darlington pair is used to give high input impedance $R_i = \beta_1 h_{ie2}$ current gain $= \beta_1 \beta_2$
- In CB-CC amplifier CC is used to offer low output impedance to the load and high input impedance to the previous stage.
- Differential amplifier is a multistage amplifier to give two signals 180° in out of stage.

UNIT – III

POWER AMPLIFIER

- Amplifier which drive loads like loudspeaker outputs of Radio and Television etc., require large current and voltages. They dissipate heat in operate at high current/voltage.
- Devices used for power amplifier features high current, power rating and are relatively big inside suitable for mounting heat sinks or mounted on chassis.
- Power amplifiers are classified based on conduction angle of current through the device. BJT / FET. They are class A, B and C.
- Class A amplifier operate in linear regions of device and current close to device for full period 0-360° of signal.
- Class B amplifier operate exactly half period of signals or 0-180°. They are essentially biased to cutoff initially. Only signals drive to conduction of exactly ½ cycle or period.
- Class C amplifier operates for small period of input cycle i.e. is less than 180°. These devices are operated beyond cutoff and essentially used as tuned amplifier over a small band of frequency.

CLASS A AMPLIFIER

- Class A operation requires operating point in linear region and its location control maximum undistorted output signal. In a BJT class A amplifier, Q point can be controlled by increasing / reductions of base current. The operation is limited to region between saturation region and cutoff. This region is considered linear. $V_{ce(sat)} < 1$ volt, $V_{ce\ cutoff} \sim V_{cc}$. $I_{C\ sat} = (V_{cc} - V_{ce(sat)}) / R_L$ else. Strait line joining V_{cc} / R_L and V_{cc} is called load line. Q goes up on load line with increase of I_B which increases I_C . Q point goes down with decrease of I_B . The voltage V_c is – 180° out of phase with input while I_C is in phase with I_B .
- If Q point is exactly at $V_{ce\ sat} + (V_{cc} - V_{ce\ sat}) / 2$ or approximately $V_{cc} / 2$ the amplifier gives maximum voltage and current signal. Otherwise output gets truncated clipped to V_{cc} or $V_{ce\ sat}$.
- Product of V_{ce} & I_c is power dissipated in collector and $I_{rms}^2 R_L = P_O$ or $P_{ac} =$ output power. Input DC power $P_i = V_{cc} I_{CQ}$

- Amplifier is operated such that instantaneous power dissipated is within specified limit of device. This limit is hyperbolic on V_c , I_c curve. Maximum dissipation occurs under no signal condition.
- The ratio of P_{ac} / P_{dc} expressed in percentage is called collector efficiency of amplifier.
- The maximum efficiency possible in class A amplifier is 25% for resistive load. Operating point shall be located at $V_{ceq} = V_{cc}/2$, $I_{cq} = I_{cmax}/2$.

TRANSFORMER COUPLED CLASS A

- In case of class A amplifier employing transformer, operating point is determined first by DC resistance of primary windings and I_B supplied from base circuit. From this point AC load line can be drawn $R_{l(ac)} = (n_1/n_2)^2 \cdot R_l$
- For maximum efficiency to shall be located at $I_{cq} = V_{cc}/R_{l(ac)}$. $V_{ac\ p-p} = 2V_{cc}$. $I_{ac\ max\ (p-p)} = V_{cc}/R_{l(ac)}$.
- Maximum efficiency possible in transformer coupled class A is 50%.

HARMONIC DISTORTION

- Power amplifier are operated over large signal in device in linear and non-linear regions. Hence signals are distorted in varying proportions. Collector current can be expressed by $i_c = I_c + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t$.
- The coefficients B_0, B_1 and B_2 can be expressed in terms of $i_{c\ max}$.
- $B_0 = B_2 = (I_{cmax} - I_{cmin} - 2I_{cq}) / 4$, $B_1 = (I_{c(max)} - I_{c(min)}) / 2$
- Harmonic distortion is expressed as ratio of these coefficients wrt B_1
- Second harmonic distortion $D_2 = \text{modules } B_2/B_1 \times 100\%$.
- Harmonic distortion = $\text{modules } B_n/B_1 \times 100\%$.
- Total harmonic distortion $D = \sqrt{D_2^2 + D_3^2 + \dots + D_n^2}$

CLASS A PUSH PULL AMPLIFIER

- Class A push pull amplifier employs 2 class A stages of mirror reflection of each other.
- Class A push pull amplifier is free from even harmonic distortion and delivers large hours.

CLASS B PUSH PULL AMPLIFIER

- Class B is always realized using in push pull transformer coupled are complimentary stage configuration.
- Class B requires 0 and 180° out of phase signals requiring a center tapped driver transformer are phase splitter circuit driving through capacitors.
- Class B suffers from crossover distortion which is due to non conduction of device for small period of input.
- Crossover distortion can be avoided by biasing devices to near conduction.
- Class B push pull amplifier features efficiency = 87.5%.

COMPLIMENTARY SYMMETRY AMPLIFIER

- A pair of NPN & PNP transistor matched to each other in respect of V_{be} , β and V_{cc} and I_{max} rating are employed in this amplifier.
- This amplifier is initially biased at cutoff and can be DC coupled at input and coupled to load directly. This amplifier is essentially an emitter follower with mirror reflector stage and therefore can drive loads directly.
- For complimentary amplifier input DC is 0 an output DC also is 0 voltage. It employs + V_{cc} and - V_{cc} .
- Efficiency of this amplifier is 87.5% max.
- This amplifier suffer from crossover distortion which can be prevented by biasing arrangement near conduction by use of (1) 2 forward biased diodes (2) use of $\frac{1}{2}$ Amp (3) V_{be} multiplier circuit
- By using capacitors at output input it is possible to realize complimentary stage with single supply.

CLASS C TUNED AMPLIFIER

- Class C amplifier employed a tuned circuit and is biased beyond cutoff.
- Different biasing arrangements are possible for class C operation.
- The efficiency = 90-99% and class C employed in HF outputs of Radio & TV.

SWITCHING POWER AMPLIFIER

- Switching power amplifier employs N and P channels MOSFETS with center tapped driver input.
- Output is a tuned LC circuit with series load R_L .
- This circuit offers high efficiency but operates only at one frequency.

UNIT V

REGULATED POWER SUPPLIES.

VOLTAGE MULTIPLIERS.

- From an AC supply it is possible to generate high dc voltage in integral multiples of peak ac voltage.
- A half wave doubler consists of a half wave rectifier with capacitor filter followed by a clamper. Doubler gives dc voltage = $2 V_p$.
- By joining half wave rectifiers + and - ve outputs we can get Full wave doubler.
- It is possible to derive ' nV_p ' dc voltage using ' n ' diodes in chain.
- Irrespective of High voltage generated each capacitor is charged to ' $2V_p$.' And hence each diode used shall have $piv = 2 V_p$.
- HV generated has lot of applications in nuclear physics, TV and instruments.

VOLTAGE REGULATORS

- Due to variation of input ac mains voltage dc voltages generated using rectifiers is subject to fluctuations even if load is constant. The internal resistance of rectifier diodes changes with load.
- A regulated voltage supply gives constant dc voltage against large changes in ac voltage and load. They also reduce ripple drastically.
- Line regulation = $\{ \Delta V_o / \Delta V_i \} \times 100 \%$
- Load regulation = $\{ [V_o(nl) - V_o(fl)] / V_o(nl) \} \times 100 \%$
- Output resistance $R_o = \Delta V_o / \Delta I_o$.
- A dc voltage produced is also subject to change with temperature.
- $S_T = \Delta V_o / \Delta T$
- The overall change in output
- $\Delta V_o = (\partial V_o / \partial V_i) \Delta V_i + (\partial V_o / \partial I_o) \Delta I_o + (\partial V_o / \partial T) \Delta T$.

TYPES OF VOLTAGE REGULATORS.

- Basically there are 2 types of regulators. (1) zener (2) feedback type
- Feedback type regulators are 3 types.
- series (2) shunt (3) switching.

ZENER REGULATOR

- A fixed regulated voltage = V_z can be generated to overcome line and load fluctuations.
- A zener is always operated in reverse bias. Always a minimum current $I_z(\min)$ is assured in zener supply for proper operation. A zener current $I_z(\max)$ is also observed such that under no load and when .
- V_i is highest, current through zener is kept $< I_z(\max)$.
- If not specified $I_z(\max) = P_z / V_z$. And $I_z(\min) = I_z(\max) / 10$.
- A zener regulated power supply is simplest regulator which uses a series resistor R_s in series with zener connected across unregulated voltage V_i . Load is connected in parallel with zener.
- Current through zener is maximum when input voltage V_i is high and load minimum .

- Current through is minimum when input is min $V_i(\text{min})$ and load current at maximum.
- R_s can be determined by
- $R_s = \{ (V_{i\text{min}} - V_z) / (I_{z\text{min}} + I_{l\text{Max}}) \}$
- $= (V_{i\text{max}} - V_z) / (I_{z\text{max}} + I_{l\text{Min}})$.
- any ripple at Dc Current can be determined by $\Delta v_o = \Delta V_i \cdot R_z / (R_s + R_z)$.
- When Load current is maximum together with V_i permitted minimum can be determined by $V_z = V_i \text{ min} \cdot R_l / (R_l + R_s)$. And $R_l = V_z / I_{l\text{ max}}$.

FEED BACK REGULATORS.

- Block diagram of feed back regulator consists of 4 basic blocks viz control element, sampling ckt, reference voltage, comparator/error amplifier.
- Output voltage is sampled , compared against reference at error amplifier which drives control element to change output.
- Based on functional features of control element , feed back regulators are further classified to series, ,shunt and switching regulators.
- In series regulator $V_o = V_i - I_o \cdot R_s$. Series element acts as variable resistance to drop voltage under varying V_i and I_o .
- In shunt regulator $V_o = V_i - R_s(I_o + I_{sh})$. Shunt regulator acts as a variable shunt resistor to drain away current to maintain specified output V_o .
- In switching regulator $V_o = V_i \cdot T_{on} / (T_{on} + T_{off})$. Switching element acts as toggle switch to connect V_i to output into LC filter for variable period so as to charge capacitor to V_o under varying V_i and I_o . To keep V_o constant.

SERIES REGULATORS.

- Series regulator in simplest form has a series pass transistor that is driven by an error amplifier where sample of output $V_o \cdot R_2 / (R_1 + R_2)$ is compared against reference voltage usually a zener V_z .Series pass transistor actually an emitter follower connected on error amplifier.
- $V_z + V_{be} = V_o \cdot R_2 / (R_1 + R_2)$ determines V_o .
- It is customary to maintain $I_z \text{ min}$ in zener. $R_2 < (V_i + V_o) / I_{b\text{ max}}$.
- $I_{b\text{ max}} = I_o / \beta_1$.
- This type of regulator gives $V_o > V_z$.
- To assure same load regulation even at $V_i \text{ min}$, a pre regulator is employed in place of R_3 (resistor between V_i and base of series pass transistor) to provide constant current ' I_{b1} ' required for max load current.
- Even OP Amps can be used as error amplifiers.
- It is desirable to supply I_s through V_o instead of V_i to obtain small ripple.
- Current rating can be increased by use of boost up transistor as Darlington pair.
- Short circuit protection can be achieved by including a current sense resistor in output and connecting a transistor between base and output .This transistor is turned on by drop in current sense resistor to cut off series pas transistor.
- Fold back operation is one which limits current in load less than maximum in case of short circuit. This can be achieved by pre biasing base of sc protection control transistor connected BE junction of series pass transistor.
- $R_{of} = \Delta V_o / \Delta I_o = (V_t / I_o) \cdot (V_o \cdot V_r) \cdot (1 / A_{ol})$.
- $\Delta V_o / V_o = (\Delta I_o / I_o) \cdot (V_t / V_r) \cdot (1 / A_{ol})$.

SHUNT REGULATOR

- Shunt regulator acts as a current draining circuit connected in shunt with RL.
- When $I_o = 0$, all the current $(V_i - V_o)/R_s$ flows through shunt transistor and dissipation is maximum.
- Maximum load current the supply can give is $(V_i - V_o)/R_s$.
- Simplest form of shunt regulator employs a zener connected between base and V_o . This zener can be biased to $I_{z \min}$ by connecting a resistor R_z between base and ground. $R_z = V_{be}/I_{z \min}$. $V_{be} = 0.7\text{V}$.
- Shunt regulator is preferred for small currents.

IC REGULATORS.

- 78xx, series ICs are 3 terminal fixed voltage regulators over a range of output voltages 6, 9, 12, 15, 18, ..24
- for +ve or 79XX series are -ve voltage. These are available in TO 220, TO 202 and TO3.
- These regulators require min differential voltage 2V in excess of V_o .
- Current boosting can be achieved by connecting a transistor externally between V_i and V_o .

ADJUSTABLE REGULATOR

- LM 317, LM337 are adjustable voltage regulators in 3 pin package available in TO 202, 220 and also in TO2, TO3.
- LM 317 gives 1.25 V between V_o and center pin and a resistance of 240 ohms is recommended at these pins.. By connecting variable resistance ground and center pin variable voltage $V_o = V_{ref}(1 + R_2/R_1)$ can be achieved.

LM 723.

- LM 723 is a multi pin adjustable voltage regulator.
- It is available in 10 pin metal package and 14 pin DIL package.
- 723 is versatile IC and can be used for + and - ve regulators with all improvements like SC, current boost, fold back etc..
- 723 contains a reference amplifier that gives 7V ref voltage, error amplifier with INV, NIV inputs. Error amplifier is connected to 2 transistors to be used for current boost, short circuit and fold back protection.
- When $V_o < 7\text{V}$ output V_r is attenuated and when $V_o > 7\text{V}$ V_r is connected directly to INV input.
- For short circuit protection R_s is connected between CS and CL. Terminals.

SWITCHING REGULATORS

- There are 3 types of switching regulators. Buck, Boost, Invert types. Buck is step down and Boost is step up.
- Block diagram of switching regulator consists of a switch controlled by a sample of output. Switch connects V_i to a LC filter whose output is sampled for control of switch.
- For step down regulator the switch is in series with the filter and for step up it is in shunt to output after an inductor.
- Switching regulators give regulated output less than greater than or inverted to input and achieve efficiencies close to 100 %.

IC SWITCHING REGULATOR

- 78 S40 is a an example of IC switching regulator.
- This IC consists of a reference 1.25v, an oscillator, gate generator, error amplifier and a switch (Flip flop).
- This IC gives step up, down or inverting voltage. Accepts $V_i = 2$ to 40v and gives V_o between 1.5- 40v @ I_{pk} 1,5 Amp.

UNIT – IV

TUNED AMPLIFIER

- Communication circuit very widely use tuned amplifier they are used in MW & SW radio frequency 550 KHz – 16 MHz, 54 – 88 MHz, FM 88 – 108 MHz, cell phones 470 - 990 MHz
- Band width is 3 dB frequency interval of pass band and –30 dB frequency interval is called Skirt.
- Tune amplifiers are also classified as A, B, C similar to power amplifiers based on conduction angle of devices.
- Tune amplifiers are series and parallel tuned type.

SERIES RESONANT CIRCUIT

- Series resonant features minimum impedance (R_S) at resonant.
- $f_r = 1/2\pi\sqrt{LC}$; $q = \omega L/R_S$ at resonance $\omega L = 1/\omega C$, $BW = f_r/Q$
- It behaves as purely resistance at resonance, capacitive below and inductive above resonance

PARALEL RESONANT CIRCUITS

- Parallel resonance features maximum impedance at resonance $= L/R_S C$
- At resonance $f_r = 1/2\pi\sqrt{1/(LC - R_S^2/L^2)}$; if $R_S = 0$, $f_r = 1/2\pi\sqrt{LC}$
- At resonance it exhibits pure resistance $R = 1/R_S C$. This resistance can also be expressed as parallel resistance $R_p = Q_0 \omega_0 L$, $Z_0 = R = 1/LR_S = \omega_0 LQ$ or $Q/\omega_0 C$ or $R_S Q^2$
- Below f_r parallel circuit exhibits inductive and above capacitive impedance

ANALYSIS OF TUNED CIRCUIT IN AMPLIFIERS

- At resonance since parallel circuit is a resistance R_t gain of BJT CE circuit with tune circuit is $-g_m R_t$. Where $R_t = r_d \parallel R \parallel R_i$
- Gain in any frequency away from f_0 $A_r = A_0 / (1 + 2j\delta Q)$ $\delta = \omega - \omega_0 / \omega_0$
 $Q_e = R_t / \omega L$ or $\omega_0 C R_t$, $Z = R_t / (1 + 2j\delta Q_e)$
- $BW = 2\delta\omega_0 = \omega_0 / Q = 1/R_t C$
- $GBW = g_m / C$

INTERSTAGE COUPLING METHODS

- Output of one tuned amplifier stage can be coupled to next stage by (a) inductive/magnetic coupling so as to match impedances (b) tapped inductor forming part of tuned circuit with capacitors (c) coupling through capacitors without any tapings. No effort made to match impedances (d) magnetically coupled secondary tuned circuit with controlled coupling.

DOUBLE TUNED AMPLIFIER

- A tuned circuit at output of amplifier is coupled to next stage by another tuned circuit at input of succeeding stage with controlled coupling makes a double tuned amplifier.
- When coupling coefficient $K_c = 1/\sqrt{(Q_{01} Q_{02})}$ is called critical coupling and response looks like a single tuned circuit.
- Inductance of primary shall be $L_p = M$ where $M = b M_c$. B = coupling coefficient M_c = mutual inductance at critical coupling.
- When loosely coupled the amplifier gives lower BW.

- When over coupled bandwidth BW increases with a dip at center in W shape.
- $3\text{dB BW} = \omega_0/Q \sqrt{(b^2-1) \pm 2b}$
- Double tuned amplifier gives nearly 3 times BW of single stage.

SYNCHRONOUS TUNING

- Tuned amplifier tuned to a frequency f_0 and having same bandwidth can be cascaded. Such tuning is called synchronous tuning.
- Synchronous tuning features increased gain but reduced VW with respect to single tuned amplifier stage. As amplifiers are tuned to same frequency and have same BW.
- Overall gain of 'n' similar stages with synchronous tuning gives

$$\left| \frac{A}{A_0} \right|^n = 1/\{ \sqrt{1+(2\delta Q)^2} \}^n$$

- $3\text{dB BW of 'n' such stages} = \text{BW} \sqrt{2^{1/n}-1} = f_0/Qe \sqrt{2^{1/n}-1}$

STAGER TUNING

- Stager tuning is employed to achieve large bandwidth in cascading without aiming increase of gain.
- Generally odd numbers of stages are employed. One at the center of required band and two either side at equidistant in frequency intervals in pairs. All amplifiers so stager tuned have same BW but different tuned frequency as required.

IC TUNED AMPLIFIER

- In IC tuned amplifier circuit has provision to connect tuned circuit from outside at input or output.
- A diode is employed to enable tuned circuit.
- One such IC is MC 1550 which is connected in cascode amplifier.

INSTABILITY & STABILISATION METHODS

- Feed back capacitances between input and output tuned circuits together with amplifier gain gives rise to undesired oscillation below tuned frequency. This is called instability.
- In simple case instability can be prevented by (a) connecting a series LC circuit between collector & BJT to prevent oscillation. (b) Power supply is connected at tap of an inductor and a capacitor is connected between base and other end of coil. Adjusting C to prevent oscillation.
- More sophisticated methods are by (a) Hazel tine (b) Rice (c) Common feedback. These are improved schemes based on simple methods narrated.
- Hazel tine method uses splitting of inductor of second tuned circuit to in equal parts L_{2a} , L_{2b} , connect supply from junction of these inductors. And C_n between input and output of inductance of L_{2a} . At balance $C_n = C_f.(L_{2b}/L_{2a})$
- Rise scheme is similar to hazel tine scheme, which employs splitting of inductance at input tuned circuit to equal parts. $C_n = C_f$
- Common circuit neutralization scheme handles feedback effects at microwave frequencies. Consists of capacitance C_n from ground lead.

CLASS 'C' TUNED AMPLIFIERS

- Current in class C tuned amplifier flows for $< 180^\circ$, few degrees around 90° . Hence amplifier is biased far below cutoff.
- This amplifier features tuned circuit purely as a resistive load for tuned frequency.
- And efficiency of nearly 90-99% can be achieved.