

## The typical Embedded System:-

### Introduction :-

- Learn building blocks of typical E.S
- Learn about General Purpose Processor (GPP), ~~ASIP's~~ (Application specific)
- Learn about Microprocessors; MC ; DSP ;  
Integrated Instruction Set Processors ; microprocessors ; MC ; DSP ;  
RISC & CISC Processors ; Harvard & Von-Neuman Processor &  
Load Store operation & instruction Pipelining.
- Learn about PLD's ; CPLDs ; FPGAs , etc..
- Learn about Memories → masked Rom ; PROM ; OTP ; EEPROM ;  
EEPROM ; FLASH memory
- Learn about serial Access memory (SAM) ; Static Random Access memory  
(SRAM) ;
- Learn about non-volatile SRAM (NVRAM).

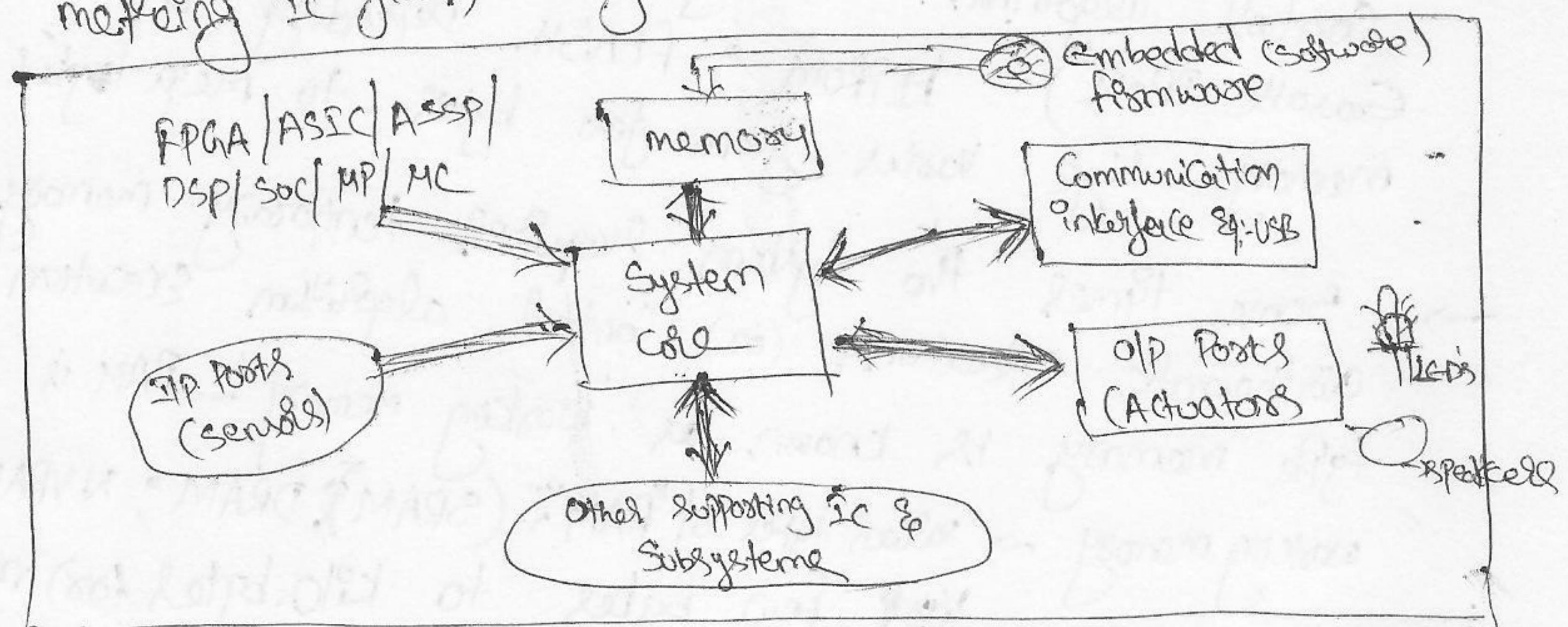
(DRAM), & non-volatile memory

2)

A typical E.S consists of single chip Controller which acts

like master brain of system.

- The Controller can be MP (8086, 80486, 80386) (or) MC (Atmel AT89C51)
- (or) a field Programmable Gate Array (FPGA) devices (xilinx spartan)
- (or) digital signal Processors (e.g. Blackfin ® Processor from
- (or) digital signal Processors (e.g. Blackfin ® Processor from
- Analog devices) (or) Application Specific IC (ASIC) / Application
- Specific Standard Product (ASSP) (e.g. ADC7760 single phase Energy
- metering IC from) Analog devices for energy metering applications.



→ Embedded hardware / software designed to regulate Physical variable  
(or) manipulate the state of some devices by sending some control signals to the Actuators / device connected to I/O Port of System, in response to I/O signals provided by End user of Sensors.

Hence an E.S can be viewed as Reactive system.

→ Some E.S do not require any manual intervention for their operation. They automatically sense the variations in the I/O Parameters in accordance with the changes in real world to which are interacting through the Sensors connected through I/O. The sensor information is passed to the Processor after signal conditioning and digitisation. Upon receiving the sensor data the Processor (or) brain of E.S performs some predefined operations with help of firmware.

→ The memory of system is responsible for holding the Control algorithm and other important configurations details.

→ For most of Embedded systems, the memory for storing the algorithm (or) Configuration data is of fixed type, which is kind of Read only memory (ROM) and it is not available for end user for modifications which means memory is not protected from unwanted user interaction. by implementing some kind of memory protection.

→ The most common type of memories used in E.S are for Control algorithms storage are OTP, ROM, UVEPROM (Ultra-violet Erasable PROM), EEPROM, FLASH. Depending on Control application memory size varies from few bytes to mega bytes.

→ Some times the system requires temporary memory for performing arithmetic operations (or) Control algorithm execution and this type memory is known as "working memory". RAM is known as working memory → various types of "RAM's" (SRAM, DRAM, NVRAM) ...  
Working memory → varies from few bytes to kilo.bytes (or) mega bytes.

### 3) Case of Embedded Systems:-

The Case of Embedded falls under.

- 1) General purpose & Domain specific Processors

→ microprocessor  
→ microcontroller  
→ Digital Signal Processor

- 2) Application Specific Integrated Circuits (ASIC's)

- 3) Programmable Logic Devices (PLD's)

- 4) Commercial off the shelf Components (COTS)

### 1) General Purpose & Domain specific Processors:-

- (a) Microprocessor:- is a silicon chip representing a CPU to which is ~~capable~~ of performing arithmetic and logical ~~operations~~ operation according to predefined set of instructions.

In general CPU ~~contain~~ Arithmetic logic unit (ALU), Control Unit, working with registers.

1st microprocessor by Intel 4004 in 1971 Nov (4-Bit)

which is featured 1k data memory ; a 12-bit Program Counter and 4k Program memory ; sixteen 4-bit GPR and 46-instructions, with clock speed of 740 KHz, designed for (Calculator).

In 1972 ; 16-more instructions were added to 4004 MP 8-bit instruction set & Program Space is upgraded to 8k also interrupt capabilities were added and renamed to 4040.

In 1972 (8-bit) Intel 8008 similar to 4040 MP only difference is Program Counter of 16-bit wide followed with terminal Counted.

In 1974 April (8-bit) Intel 8080 with 16-bit Address Lines and Program Counter, and seven 8-bit Reg. (A-E ; H:L ; BC , DE and HL Pairs formed the 16-bit Reg of Processor).

- (e) Immediately after Intel 8080 Motorola entered with Motorola 6800 with different Architecture & instruction set compared to 8086 MP.
- (f) In 1976 Intel came up with advancement in 8080 MP to 8085(8 bit) newly added instructions set & interrupt pins & serial I/O. CLK generator & bus controller circuits built in Power supply +5V.
- (g) In July 1976 Zilog entered in MP with Z80 Processor.
- (h) Technical advances in the field of Semiconductors industry brought a new dimension to the microprocessor market and twentieth century witnessed as fast growth technology. 16, 32 & 64-bit microprocessor came into existence. Initial 2MHz clock is old today. Presently with clock speed up to 2.4 GHz are available.

### (ii) General Purpose Processors (GPP) vs Application Specific Instruction Set Processor

- GPP Processor designed for general computing tasks.
- The Processor running inside your laptop (or) desktop (Pentium 4 / AMD Athlon) these are produced in large volumes & targeting the general market due to high volume production the per unit cost for chip is low compared to ASIC (or) other specific IC's.
- Application Specific Instruction Set Processors (ASIPs) with architecture and instruction set optimised to specific domain / application require like networking processing, Automotive, telecom, media applications, digital signal processing control applications, etc.,
- Eg.: - for (ASIPs) are microcontrollers like (Automotive, AVR, USB AUR, from Atmel) System-on-chips, DSP etc.,

## Micro Controller:-

Micro Controller is an highly IC that contains a CPU, Scratchpad RAM, Special & General Purpose Registers arrays, on-chip ROM for FLASH memory for Program Storage, timed & interrupt Control units and dedicated I/O Ports.

1) 1<sup>st</sup> MC is by Texas Instruments "TMS 1000" in 1974.

→ It followed Intels 4004 / 4040 Processors design and added some amount of RAM, Program storage memory (ROM) and I/O support on single chip.

2) In 1977 Intel entered the micro controller market with a family of controllers which comes under MCS-48 family.

→ The Processors under MCS-48 family were 8038 HL, 8039 HL,

8040 AHL, 8048 HE, 8049 HT, and 8050 AH.

→ Intel first MC 8048 is recognised and prominent and used in original member in MCS-48™ family. Which was used in IBM-PC keyboard.

→ The inspiration behind 8048 was Ford's F8 MP's.

→ The design of 8048 adopted by Harvard Architecture. Where Programming & data memory shared the same address bus.

→ Intel came out with 8-bit MC domain - (8051) which is most popular and powerful 8-bit MC. It was developed in 1980's and put under MCS-51 family.

CPU	RAM	ROM
I/O Port	Timer	Serial Com Port

- 8-bit MC are commonly used in embedded systems where the processing power is not a big constraint
- High performing speed micro controllers families like ARM11 etc are also available in the market, which provides solution to applications requiring hardware acceleration & high processing capability.

- The instruction set architecture of MC can be either RISC (os) CISC micro controllers, are designed for either general purpose application requirement. (os) domain specific requirement.
- The Intel 8051 is typical example for (General Purpose MC)
- AVR micro controller family from Atmel Corporation is typical example for ASIP specifically designed for automotive domain

(iv)	Difference b/w Microprocessor & micro Controller:- Microprocessor	Micro Controller.
<ul style="list-style-type: none"> <li>1) Multitasking in nature (or perform multiple task at a time). e.g. MP3C, writing text, game,</li> <li>2) RAM, ROM, I/O, and timers can be added externally</li> <li>3) Designed can be decide the no. of memory (os) I/O port needs</li> <li>4) External support of external memory and I/O ports makes a microprocessor based system hard and costlier</li> <li>5) External device require more space and Power consumption is more</li> </ul>	<ul style="list-style-type: none"> <li>1) Single task oriented e.g. washing machine</li> <li>2) RAM, ROM, I/O Ports, timers cannot be added externally together on chip</li> <li>3) fixed no. of memory (os) I/O makes a micro controller ideal for limited but specific task.</li> <li>4) micro controller are light weight and cheaper than a microprocessor.</li> <li>5) A mc based system consume less Power and takes less space.</li> </ul>	

## Digital Signal Processors :-

- DSPs are powerful special purpose 8/16/32-bit MP designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communication applications.
- DSP are 2 to 3 times faster than C.P.S
- DSP implements algorithm in hardware which speeds up the execution where Central Processor implements the algorithm in firmware and speed execution depends on clock.

### → RISC vs CISC :-

RISC → Reduced Instruction Set Computing  
 CISC → Complex      "      "      "

- RISC Processors/Controllers posses lesser no. of instructions typically in a range of 30 to 40
- CISC → in this instruction set is complex and instructions are high in number from a programmer point of view RISC Processors are comfortable since user need to learn few instructions.

e.g.: for RISC is Atmel AVR microcontroller.

<u>RISC</u>	<u>CISC</u>
<ol style="list-style-type: none"> <li>1) Lesser no. of instructions</li> <li>2) Complex design of compiler</li> <li>3) Few Addressing modes, fix instruction formats</li> <li>4) Instruction length varies</li> <li>5) Low clock cycle per second</li> <li>6) Emphasis is on software</li> <li>7) Each instruction is to be executed by hardware</li> </ol>	<ol style="list-style-type: none"> <li>1) Greater no. of instructions</li> <li>2) Simpler design of compiler, considering larger set of instructions</li> <li>3) Many addressing modes causing complex instruction formats</li> <li>4) Instruction length is variable</li> <li>5) High clock cycle per second</li> <li>6) Emphasis is on hardware</li> <li>7) Control units implement large instruction set using micro program unit.</li> </ol>

5)

## Harvard 'Vs' Von - Neumann Processor/Controller :-

Mono Processors/Controllers based on Von-Neumann architecture. Shares a single common bus for fetching both instructions and data. Program instructions and data are stored in common main memory.

→ Von Neuman architecture based Processors/Controllers first fetch an instruction and then fetch data to support the instruction from Code memory. It needs two separate fetches slow down the controller operation.

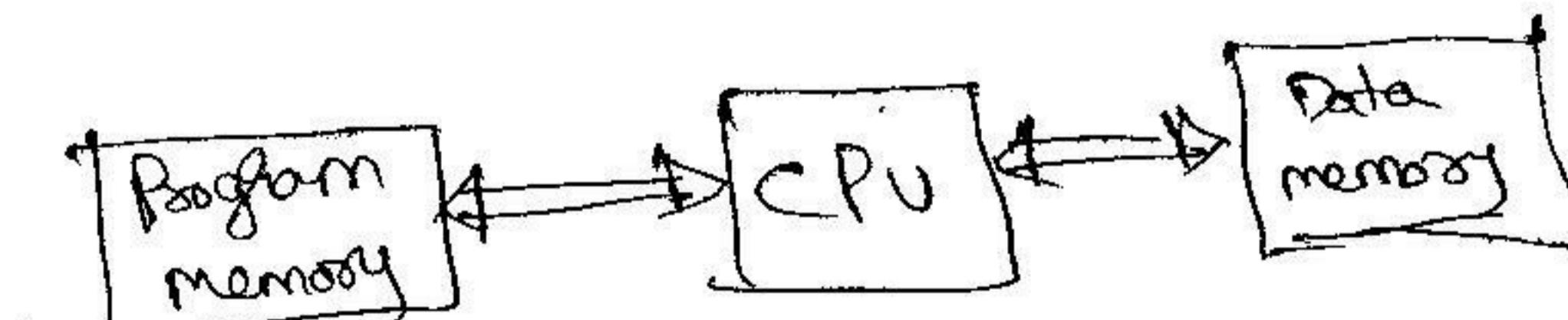
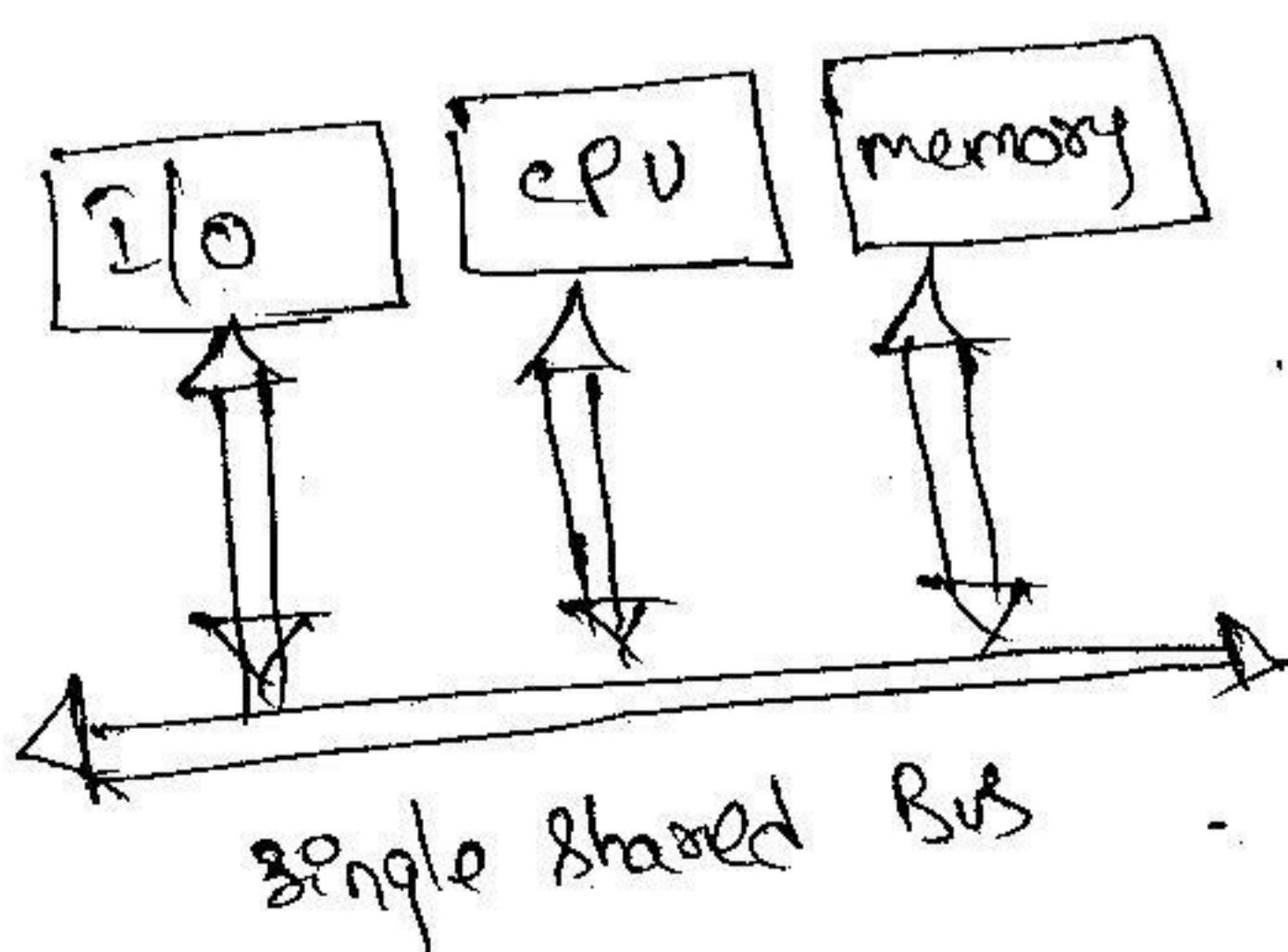
→ MP & MC based on Harvard architecture will have separate data bus and instruction bus.

It allows data transfer and Program fetching to occur simultaneously on both buses, with Harvard architecture.

→ The data memory can read & write while Program memory is being accessed.

→ These separated data memory and Code memory buses allow one instruction to execute while the next instruction is fetched (pre-fetching).

→ The pre-fetching theoretically allows faster execution than Von-Neuman architecture. Since some additional hardware logic is required for generation of control signals.



## Big-Endian Vs Little-Endian :- (Processor/Controller)

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Endianness specifies the order on which the data is stored in memory by processor operation in a multi byte system (Processor whose word size is greater than one byte)

∴ If word length is 2-bytes then data stored in 2 ways

- ① Higher order data byte @ higher memory & lower order data byte @ location just below the higher memory.
- ② Lower order data byte @ higher memory & higher order data byte @ location just below the higher memory.

Little-Endian :- (lower order byte of data stored in memory at lowest address) and (higher order byte at higher address)

e.g. 4-byte long integer Byte 3, 2, 1, 0.

Base address + 0

Base address + 1

" " + 2

" " + 3

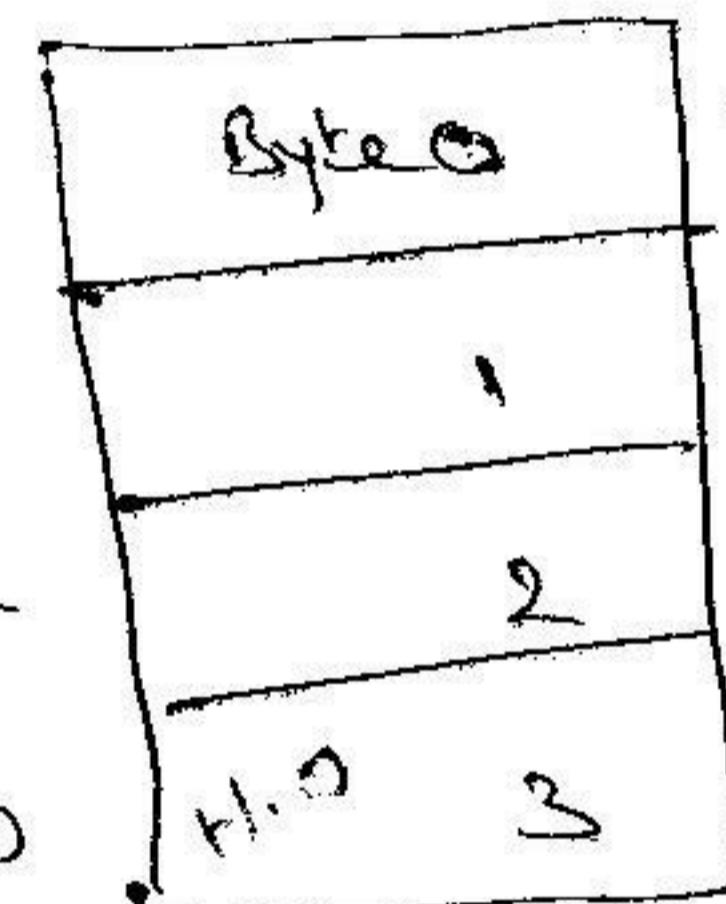
" "

Byte 0

Byte 1

Byte 2

Byte 3



0x20000 (Base Address)

0x20001 (BA+1)

0x20002 (BA+2)

0x20003 (BA+3)

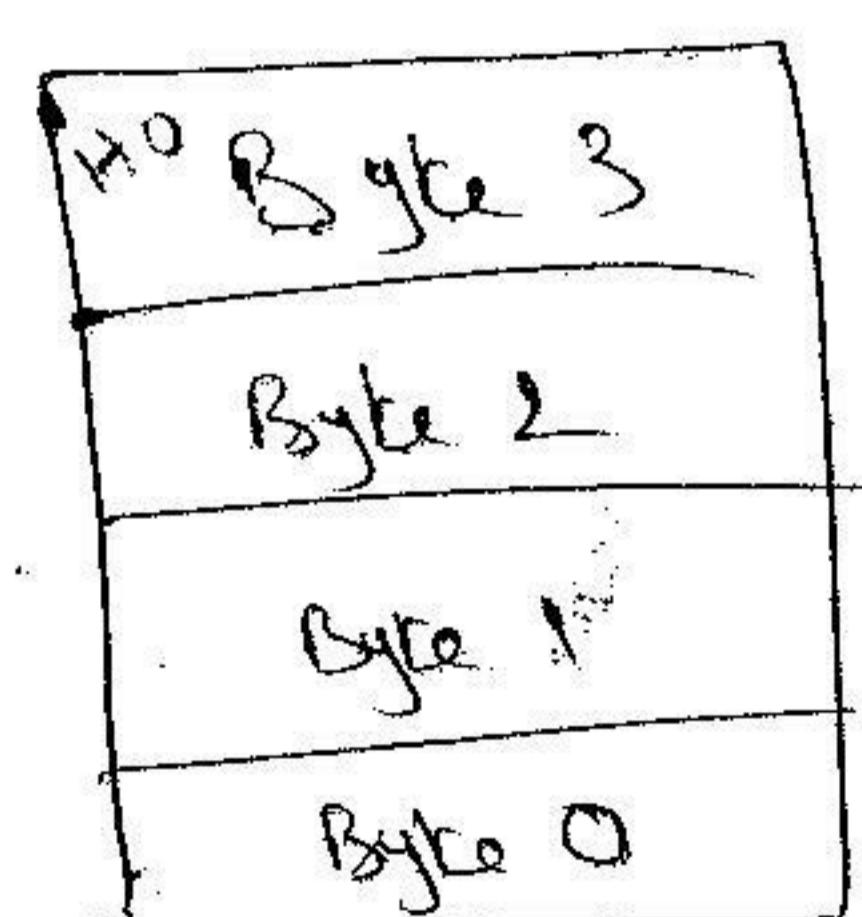
Big-Endian :- mean higher order byte of data stored memory at the lowest address and lower order byte at highest address.

BA + 0

BA + 1

BA + 2

BA + 3



0x20000 (BA)

0x20001 (BA+1)

0x20002 (BA+2)

0x20003 (BA+3)

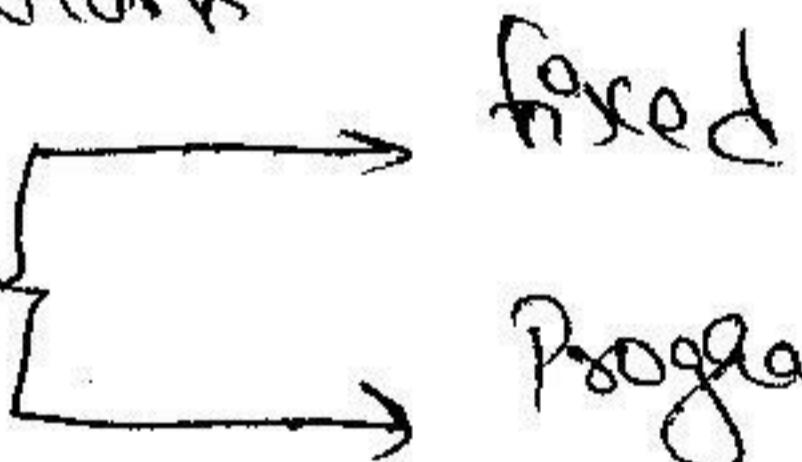
## 7) Application Specific Integrated Circuits (ASIC)

II - 10

- ASIC is a microchip
- designed to perform specific (or) unique applications
- As single chip ASIC consumes very small area in total system and their by help in design smaller system with high capabilities / functionalities.
- ASIC can be fabricated for special applications (or) can be custom fabricated by using components from a re-usable building blocks.
- The ADC 7160 Energy meter ASIC developed by Analog devices for Energy metering application is typical example for Application specific standard product (ASSP).

8)

Programmable Logic Device :- is a combination of logic device & memory device.

- Logic device provides specific functions, including (EPROM; EEPROM; flash).
- Logic device provides:
  - (a) device to device interfacing
  - (b) data communication
  - (c) signal processing
  - (d) data display
  - (e) timing & control operations
- Logic device classified into 

fixed Logic device :- circuit are fixed which performs one function (or) set of functions - once.

Programmable LD :- gives customers a wide range of logic capacity, features, speed and voltage characteristics and these devices can be reconfigured to perform any no. of functions at a time.

- PLD designers use inexpensive software tools to quickly develop, simulate, and test their designs.
- PLD can be quickly programmed into a device and immediately tested in a live circuit.

- Another key benefit of using PLDs is that during design the design phase customers can change circuitry as often as they want until the design is fixed.
  - i.e. PLD are based on re-writable memory technology to change the design, device is simply reprogrammed.
- (i) CPLD's and FPGAs:-
- Two types of PLD
- Field Programmable Gate Arrays (FPGA's)
- Complex Programmable Logic devices (CPLD's)

(a)

- FPGAs offer highest amount of logic density.
- Largest FPGAs now shipping part of xilinx virtex line devices.
- Provides (8-million system gates)
- FPGAs used in data processing and storage, instrumentation, tele-comm

EDSP

- (b) CPLD's:- offer much smaller amount logics up to 10,000 gates
- CPLD's offers very predictable timing characteristics and ideal for critical control applications.
  - CPLD's such as xilinx coolrunner series also require extreme low amounts of power and very inexpensive, making them ideal for cost sensitive, battery operated, portable applications such as mobile phones and digital handheld assistants.

- (ii) Advantages of PLD :- offers more advantages over fixed logical devices.
- PLD offers customers much more flexibility during the design cycle as design iteration are simply a matter of changing programming file, and results can be seen immediately after changing & working parts.
  - A new Programming file to PLD, via Internet, creating new hardware logic in the system.

PLD - supplier : Xilinx are fabless Companies.

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→ Xilinx at source. Job to partners like Toshiba & UMC. → making

∴ Xilinx focus to new architecture ; software tools ; intellectual property cores  
Advanced PLDs help in :- faster performance ; integration of more features ;  
reduced power consumption and lower cost.

✓ (Field Programmable Gate Arrays)

(iii) FPGAs :- Popular for Prototyping ASIC design. where designer can test

the design by downloading the design file in FPGA device.

→ field programmable means the device is programmed by the customer

not by manufacturer.

→ FPGAs are usually programmed after being soldered down to circuit board

in manner ~~taller~~ to CPLDs.

→ FPGAs are more suitable for large state machines (i.e MP).

q) Commercial off the Shelf Components :- (CoSIS) :-

i) CoSIS products are designed in such a way to provide easy integration and interoperability with existing system components.

ii) CoSIS components itself may be developed around a general purpose (or) domain

specific processor (or) an ASIC (or) programmable logic device.

e.g. hardware units are controlled by remote includes RF circuitry.

e.g. high frequency microwave electronics (2-2000 GHz) ; high BW

high performance ; high speed digital converters , devices and components for operation of

Analog to digital conversion , electro optic IR imaging arrays UV/IR detectors.

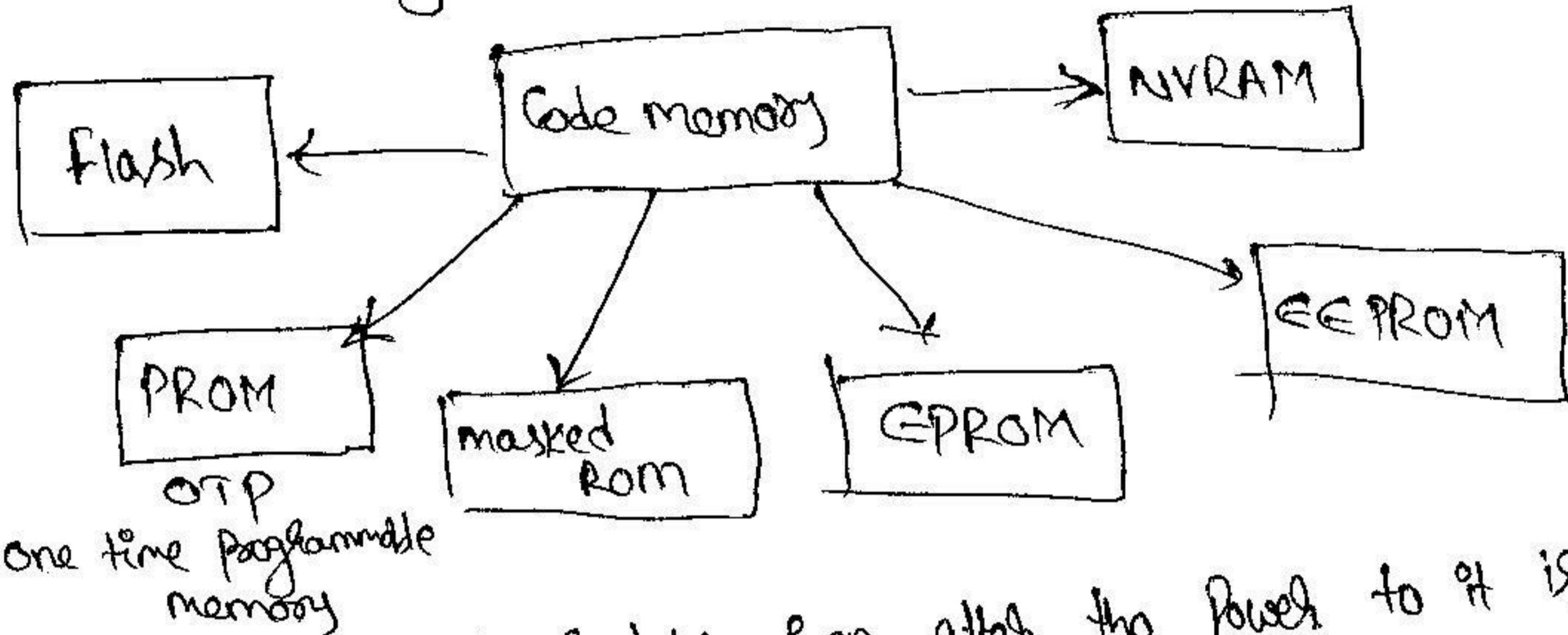
very high temperatures , plugin module available from various manufacturers

like 'Wiznet' , 'freescale' , 'Dynamax' etc., are good CoSIS products.

## Program Storage Memory (ROM) :-

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Program " (or) Code storage memory of ES stores program instructions



The Code memory retains its contents even after the power to it is turned off. It is generally known as Non-volatile storage memory.

is one-time Programmable device.

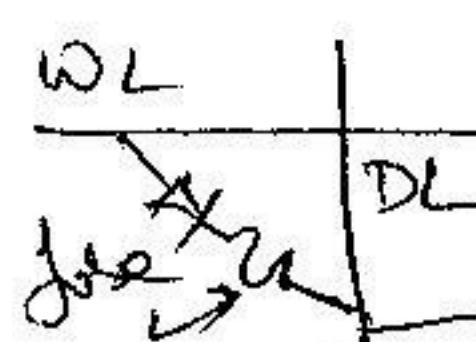
### (i) Masked ROM (M-ROM) :-

- which makes use of hardwired technology for storing data.
- Device is factory programmed by masking and metallisation process at the time of production itself due to data provided by end user.
- Advantage is low cost high volume production.
- Mechanisms for Masking Process:-

@ Creation of Enhancement (or) depletion mode transistors through channel implant.

- ⑥ By creating a memory cell either using a standard transistor or high threshold transistors.
- In high threshold mode the supply voltage required to turn on the transistor is above the normal ROM IC operating voltage.
- Masked ROM is good candidate for storing ES firmware for low cost. Once the design is proven and firmware requirements are tested and frozen, the binary data.
- MROM is permanent in bit storage, if it is not possible to alter the bit information.

## (ii) Programmable Read only Memory (PROM) :- (OTP)



III -

- i) One Time Programmable memory (OTP) (or) PROM is not Pre Programmed by manufacturer.

- ii) This memory has nichrome (or) Polysilicon wires arranged in a matrix. These wires are functionally viewed as fuses.

- iii) Fuses which are not blown/burned represents a logic '1', whereas blown/burned represents a logic '0'. The default state is logic '1'.

## (iii) Erasable Programmable Read only memory (EPROM) :-

- i) OTP are not useful and worth for development purpose.

- ii) EPROM gives the flexibility to de-program the same chip.

- iii) EPROM stores a bit by charging the floating gate of an FET.

- iv) which requires high voltage to charge the floating gate.

- v) If window is exposed to ultra violet rays for a fixed duration the entire memory will be erased.

- vi) Even EPROM chip is flexible in term of de-programmability it needs to be taken out of circuit board and put in UV erase device for 20 to 30 minutes. (so it is time consuming process).

## (iv) Electrically Erasable Programmable Read only Memory (EEPROM) :-

- i) Information can be altered by electrical signals at register/Byte level.

- ii) They can be erased and reprogrammed in circuit.

- iii) Chip includes a erase mode. In this mode, they can be erased in few milliseconds.

- FLASH:- (i) Latest ROM used mostly on C.S. (ii) Flash memory is a variation of EEPROM technology. It combine re-programmability of EEPROM and high capacity of ROMS.

- (iii) Flash memory is organised as sectors (blocks) (or) pages.

- (iv) Flash memory stores information in array of floating gates MOSFET transistors.

- (v) Erasing memory done at sector level (or) page level without affecting sector pages.

(vi) Each sector page should be erased before de-Programming. II - 15

(vii) Typically erasable capacity of flash is 1000 cycles.

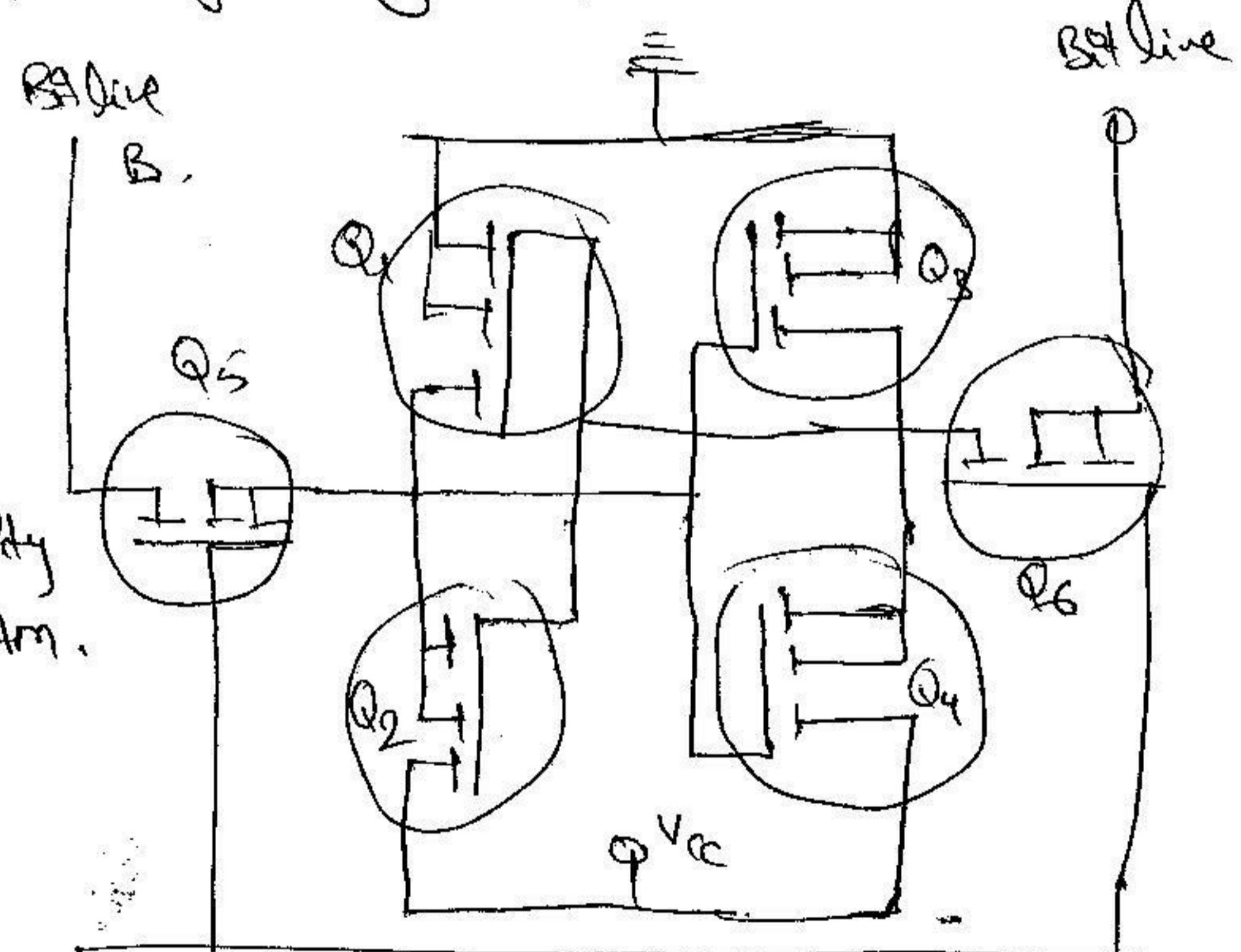
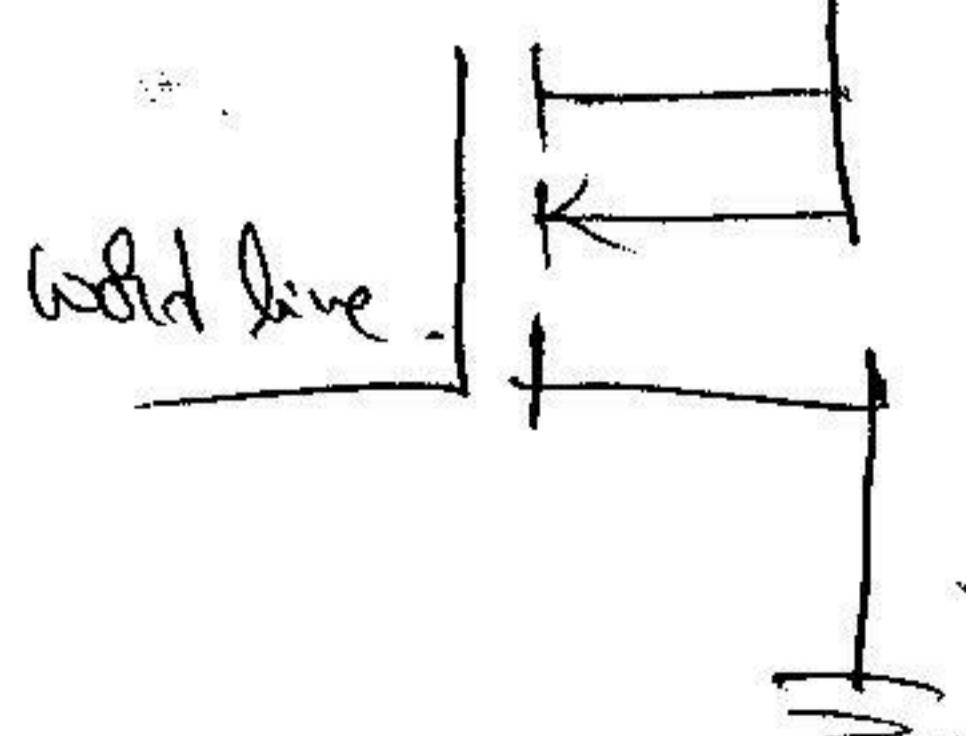
(viii) W27CS12 from WINBOND is an example 64KB FLASH memory.

- (vi) NVRAM :- (Non-volatile RAM). It is an RAM with battery backup.  
(i) Contains static RAM based memory and minute battery for holding supply to memory in absence of external power supply.  
(ii) memory and battery are packed together in single package.  
(iii) life span of NVRAM is around 10 years.  
Ex:- DS1642 from maxim/dallas 32KB NVRAM.

ii) (i) Read - Write Memory / Random Access memory (RAM) :-  
(i) RAM is data memory (or) working memory of controller/processor.  
(ii) RAM is volatile, meaning when power is turned off, all contents destroys.

(ii) Static RAM :- (SRAM) stores data in form of voltage. made up of flip-flops.

Dynamic RAM :- (DRAM)  
stores data in the form of charge.  
→ made of mos transistor gates.  
→ Advantage of DRAM has high density and low cost compared to SRAM.



Memory According to type of Interface:-

The interface of memory with Processor/Controller can be various type may be Parallel interface.

Data lines / Address lines used to interface.

## 12) Sensors and Actuators :-

1) Sensor :- is transduced device (mechanical or electrical) Converts Energy from one form to another for measurement or control purpose.

2) Actuators :- is a form of transducer (mechanical or electrical) Converts Signals to corresponding physical action (motion).

3) I/O Subsystems :-

4) LED :- indicates device on ; Battery low ; charging ; Alarms ... etc.,

5) 7-Segment LED display :-

6) Stepper Motor

7) Relay

8) Keyboard

9) Piezo Burger

10) Push button switch

11) Programmable peripheral interface (PPI)

12) LED (Light Emitting Diode) :- is an P-N junction diode Contains

Anode and Cathode.

→ functioning of LED Anode to be connected to the terminal Power Supply voltage and Cathode to 've' terminal Power supply voltage.

→ Current flowing through LED must be limited to a value below the maximum current that can conduct.

→ A resistor is used in series with PowerSupply and LED limits current flow.

→ LED can be interfaced to Processor/controller in 2-ways.

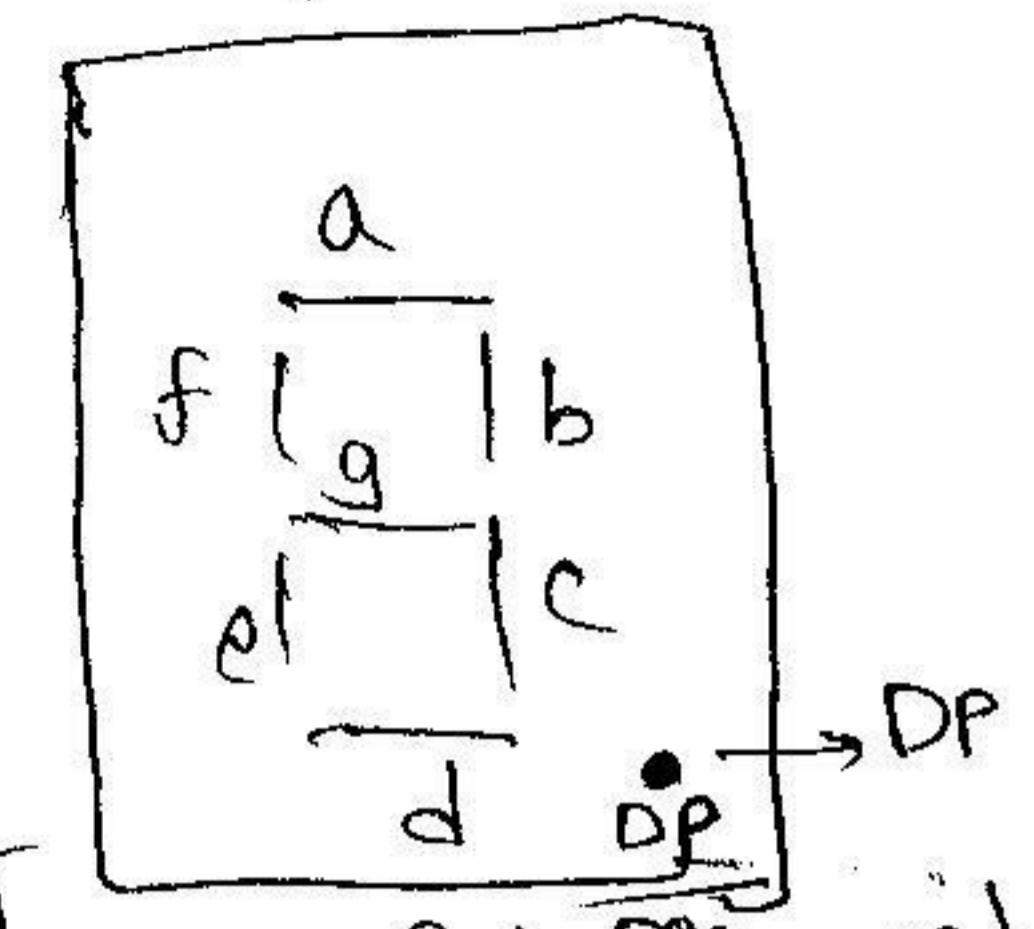
1-way :- Anode is directly connected to Port Pin and Port pin drives LED. in this method Port Pin sources current to LED. when Port Pin is (log1) High.

2<sup>nd</sup> way:- The Cathode of the LED is connected to Port pin of Processor controlled and anode to supply voltage through Current limiting resistor. The LED turned on when Port pin is at logic low (0). (Sinks current)

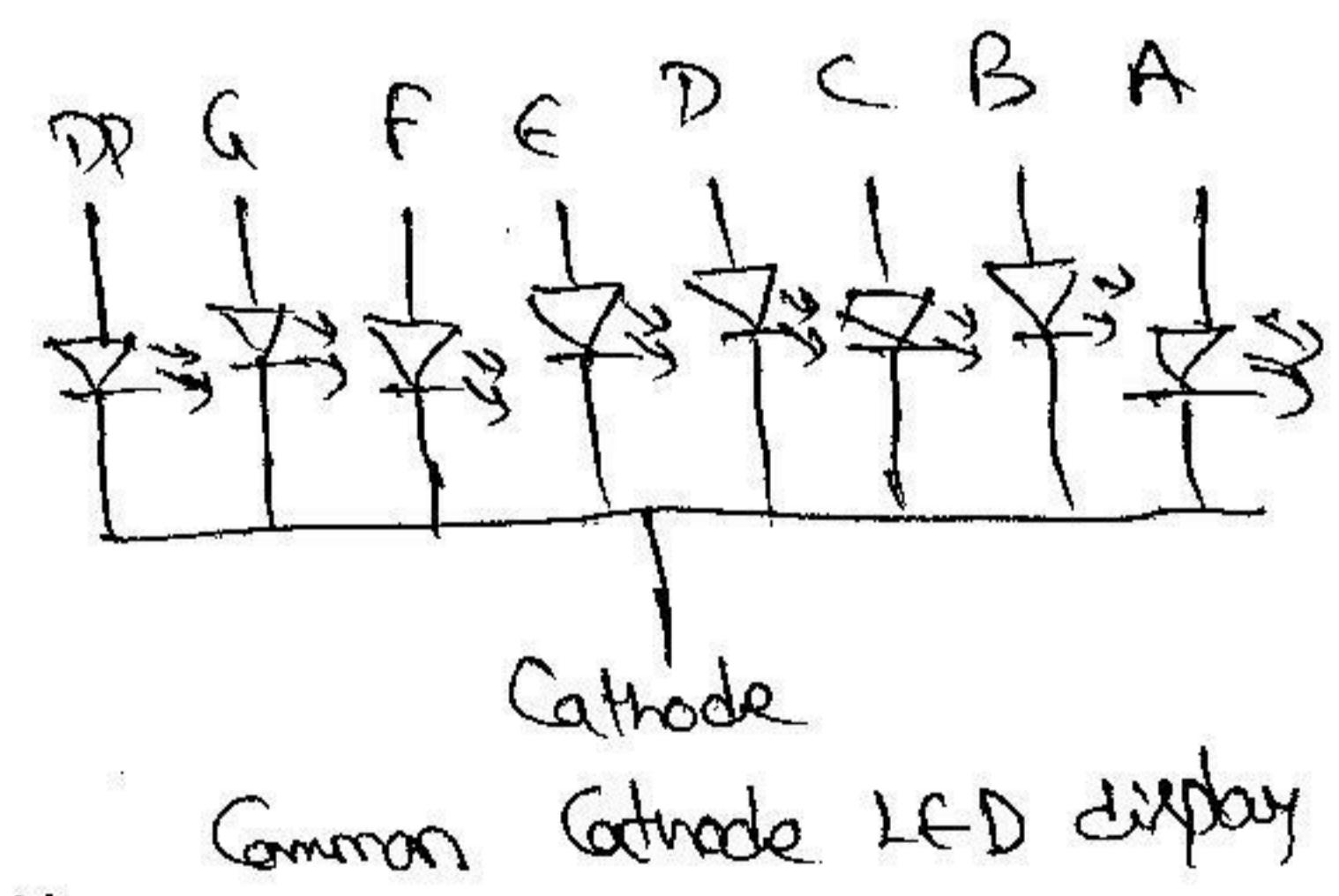
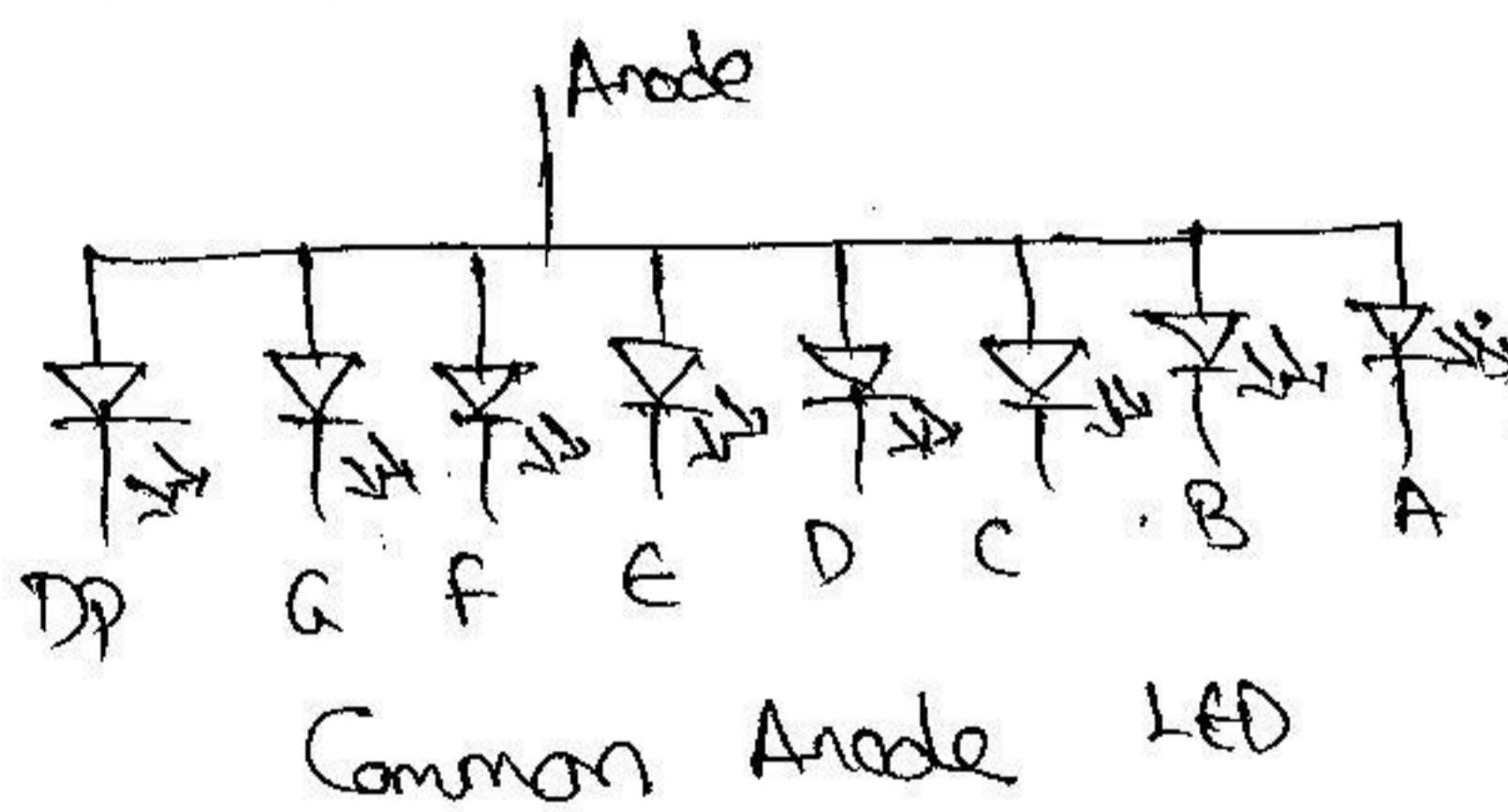
→ If LED directly connected to Port pin depending on max current that a Port pin can source, brightness of LED may not be required level.

3) Seven segment display:- (7-Segment)  
used to identify (0-9) & (A-F)

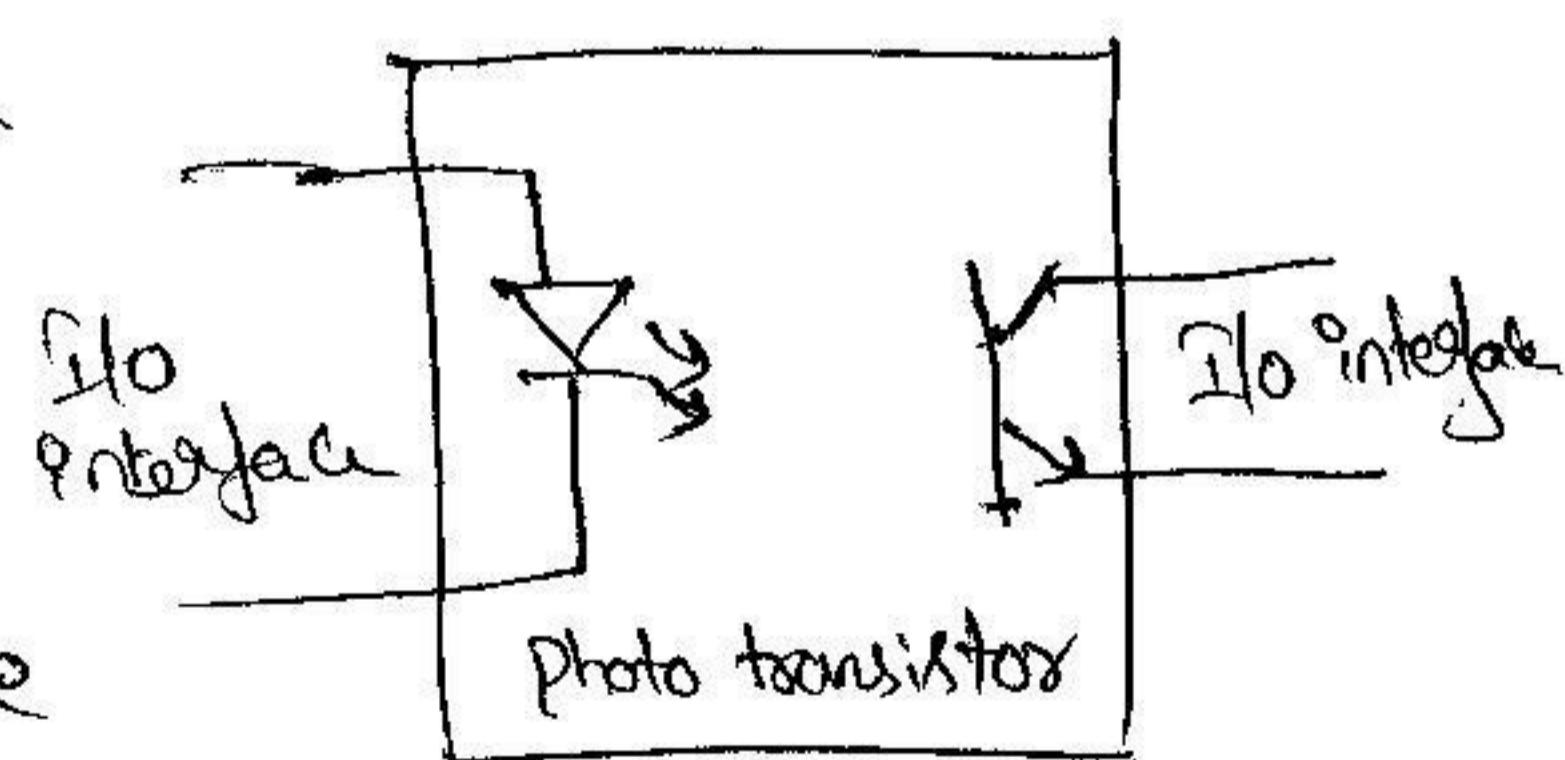
Based on Configuration of 7-segment LED unit, LED segment anode (or) Cathode is connected to Port of Processor (controlled in order 'A' segment to least significant Port Pin and DP segment to most significant Pin)



- The current flow through each of LED segment should be limited to maximum value supported by LED display unit.
- Typical value current falls within range of 20mA
- Current through each segment can be limited by connecting a current limiting resistor to anode (or) Cathode of each segment



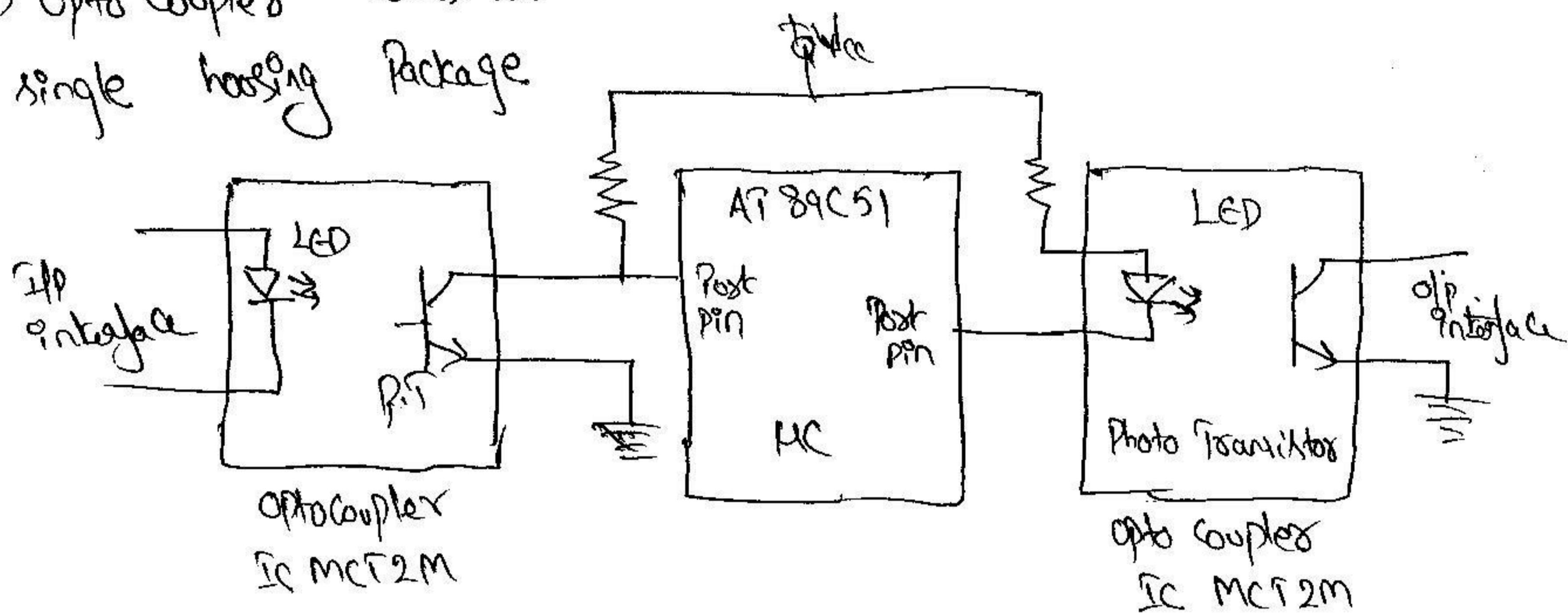
→ The anode of common Anode LED display is connected to 5V Power Supply voltage through current limiting resistor and Cathode of each LED is connected to Port pin to set at logic '0'. Cathode of LED segment is connected should be



6) Opto Coupler:- is solid state device to isolate

two Part of Circuit

→ Opto Coupler Combines an LED and a photo transistor in a single housing package



→ Optocoupler used for suppressing interface in data communication circuit isolation, high voltage separation, simultaneous separation, and signal intensification.

7) Stepper Motor:- is electro mechanical device. generate discrete (motion) displacement in response to dc signal.

→ The dc motor produces continuous rotation on applying dc-voltage

→ The dc motor produces discrete rotation in response to whole Stepper motor produces discrete rotation in response to

dc voltage applied to it.

→ Stepper motor are widely used in industrial embedded applications,

consumed electronics products and robotics control system.

→ The paper feed mechanism of a printer/fax makes use of

stepper motors for its functioning.

Based on coil winding arrangements a two phase stepper motor classified into.

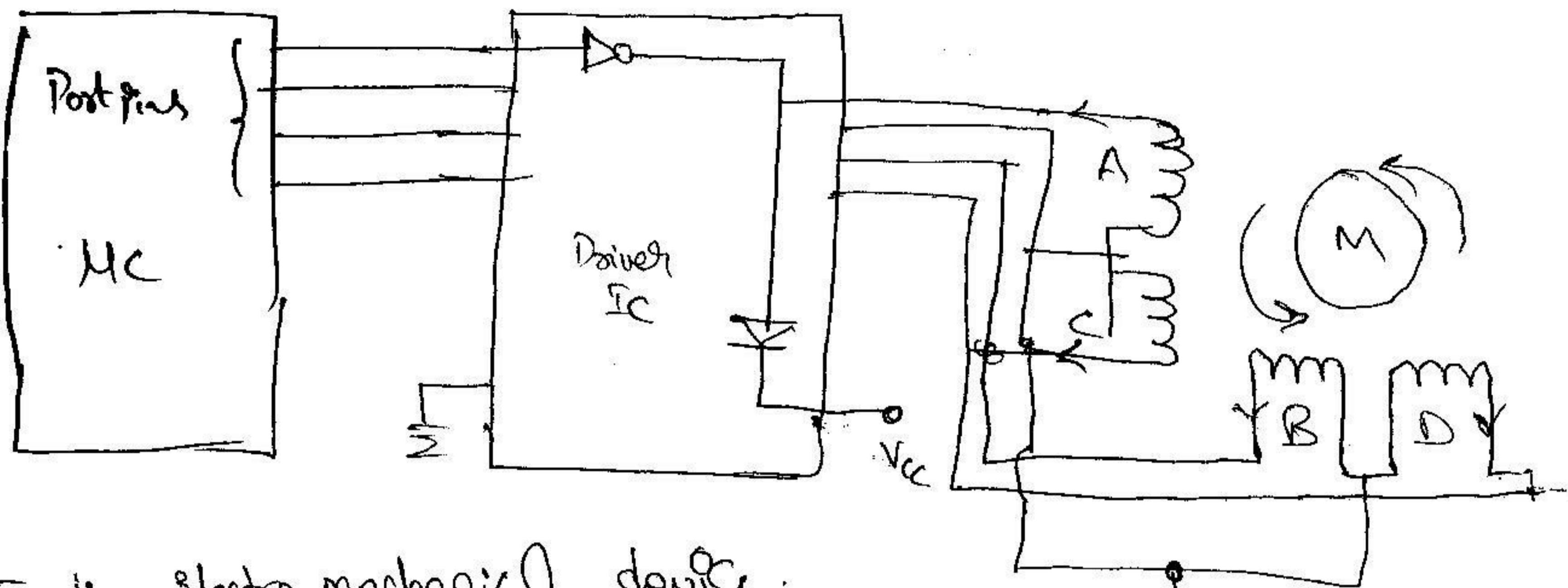
1) Unipolar

2) Bipolar.

1) Unipolar :- Contains two windings per phase. The direction of rotation (clockwise or anti-clockwise) of a stepper motor is controlled by changing the direction of current flow.

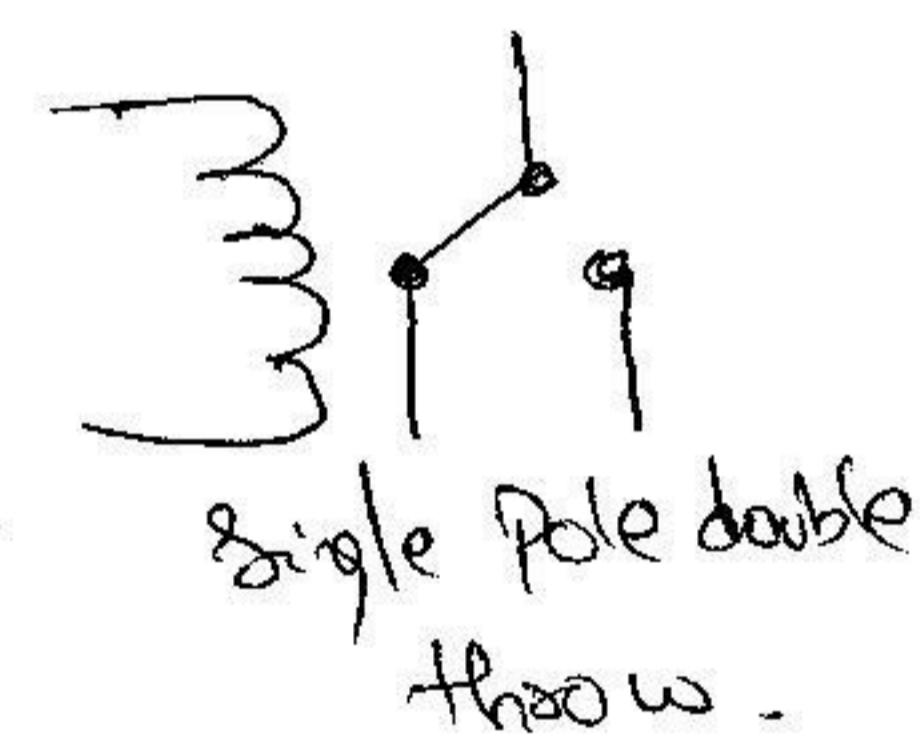
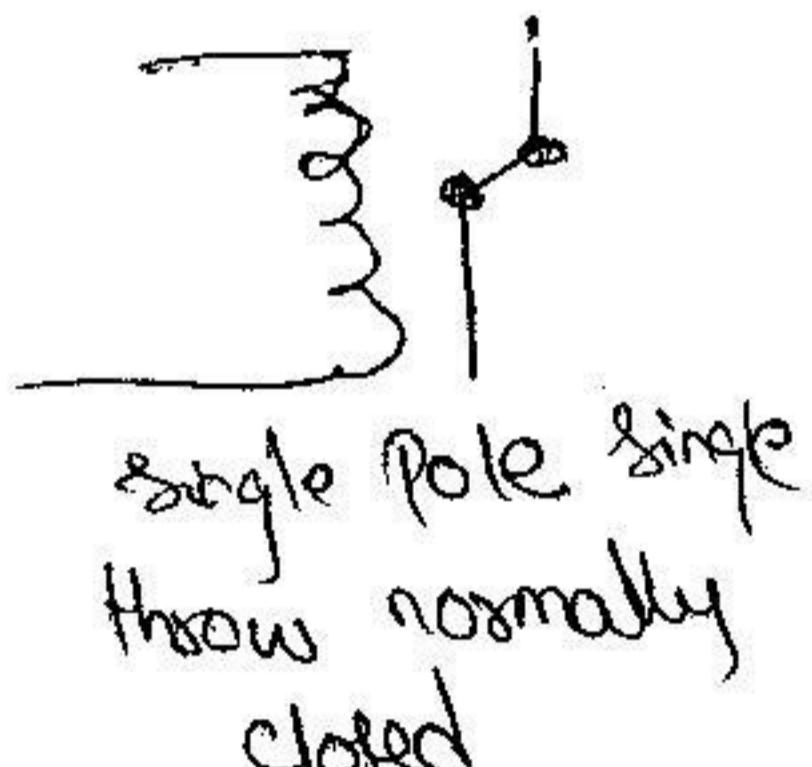
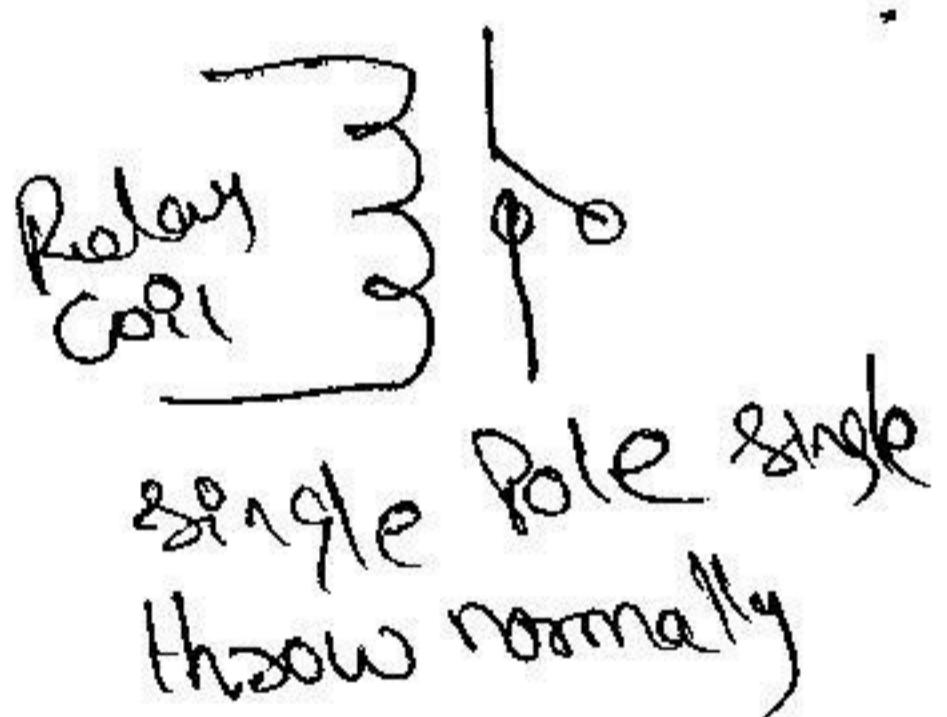
Solids: Stepper motor contains single winding per phase. For reversing the motor's rotation the current flow through the winding is reversed dynamically.

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Relay :- is electro mechanical device.

- 2) Relay unit acts as dynamic path selector for signals.
- 3) Relay unit contains a relay coil made up of insulated wire on metal core and metal armature with one or more contacts.
- 4) Relay works on electromagnetic principle.
- 5) When a voltage applied to relay coil, current flows through coil which in turn generates magnetic field.
- 6) The magnetic field attracts the armature coil and moves contact point where power signal flow path.



Piezo Buzzers :- is Piezo electric device for generating audio indications

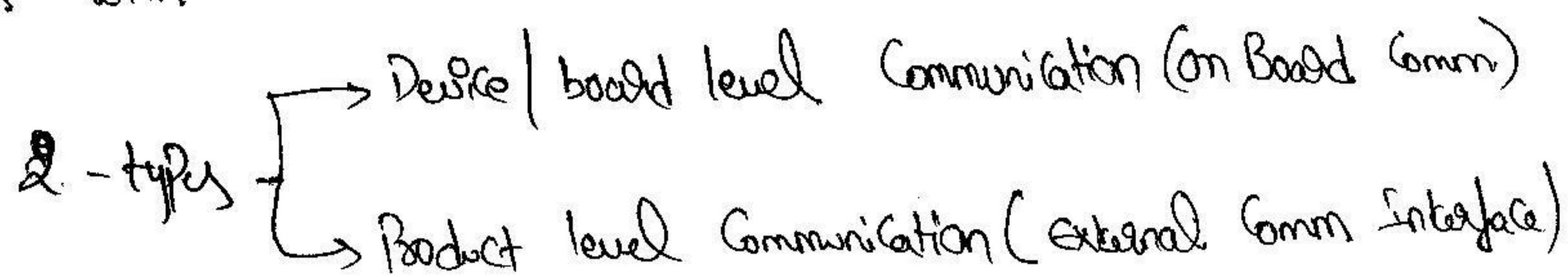
in embedded application.

- A Piezo electric buzzer contains Piezo electric diaphragm which produces audible sound in response to voltage applied to it.
- It is available in 2 types:
  - Self driving
  - External driving

- i) Self driving circuit contains all necessary components generate sound at prefigured tone. It will generate tone on applying the voltage.
- ii) External driving supports generation of different tones. Tone can be varied by applying a variable pulse train to Piezo electric buzzer.

## Communication Interface:-

Essential for communicating with various subsystems of embedded systems with external world.



→ Embedded Product is combination of different (devices/chips) arranged on PCB (Printed Circuit Board).

→ The communication channel which interconnects the various components with Embedded Product is referred as device board level communication.

→ Interface (on-Board Comm interface).  
e.g.: Serial interfaces like I<sub>2</sub>C ; SPI ; UART ; 1-Wire etc., and Parallel Bus interfaces.

→ Some E.S are self contained (Control unit) and don't require any interaction with other subsystem (or) External world.

and data transfer with other subsystem (or) External device (or) master.

→ The Product level communication interface (or) External Comm interface :-

It's possible for data transfer b/w E.S & other External device (or) master.

→ External interface may be either a wired (or) wireless media and can be serial (or) parallel interface.

e.g.: Infrared (IR) ; Bluetooth (BT) ; wireless LAN (WiFi) ; Radio freq. wave (RF)

GPRS ; ... etc., → wireless eg

wired eg:- RS232 ; RS422 ; RS485 ; USB ; Ethernet IEEE 1394 port ; Parallel port ; CF-II interface ; SDIO ; PCMCIA ;

### (i) On-Board Communication Interface:-

a) Intel integrated circuit (I<sub>2</sub>C) (or) I<sub>2</sub>C :-

b) Serial Peripheral Interface (SPI) Bus

c) Universal Asynchronous Rx/Tx :-(UART)

d) 1-Wire interface

e) Parallel interface .

intel integrated circuit ( $I^2C$ ) or I<sub>2</sub>C :-

is a synchronous bidirectional half duplex (1-directional communication)

intention → to provide connection b/w microprocessor/controlled and peripheral chips in IV sets

→ serial clock (SCL)

Controlled 2-bit lines → serial data (SDA)

SCL → responsible for generating synchronization & clock.

SDA → " " transmitting serial data across devices.

→ I<sub>2</sub>C bus is shared bus system to which many number of I<sub>2</sub>C devices

can be connected

→ I<sub>2</sub>C bus can act either Master | Slave device.

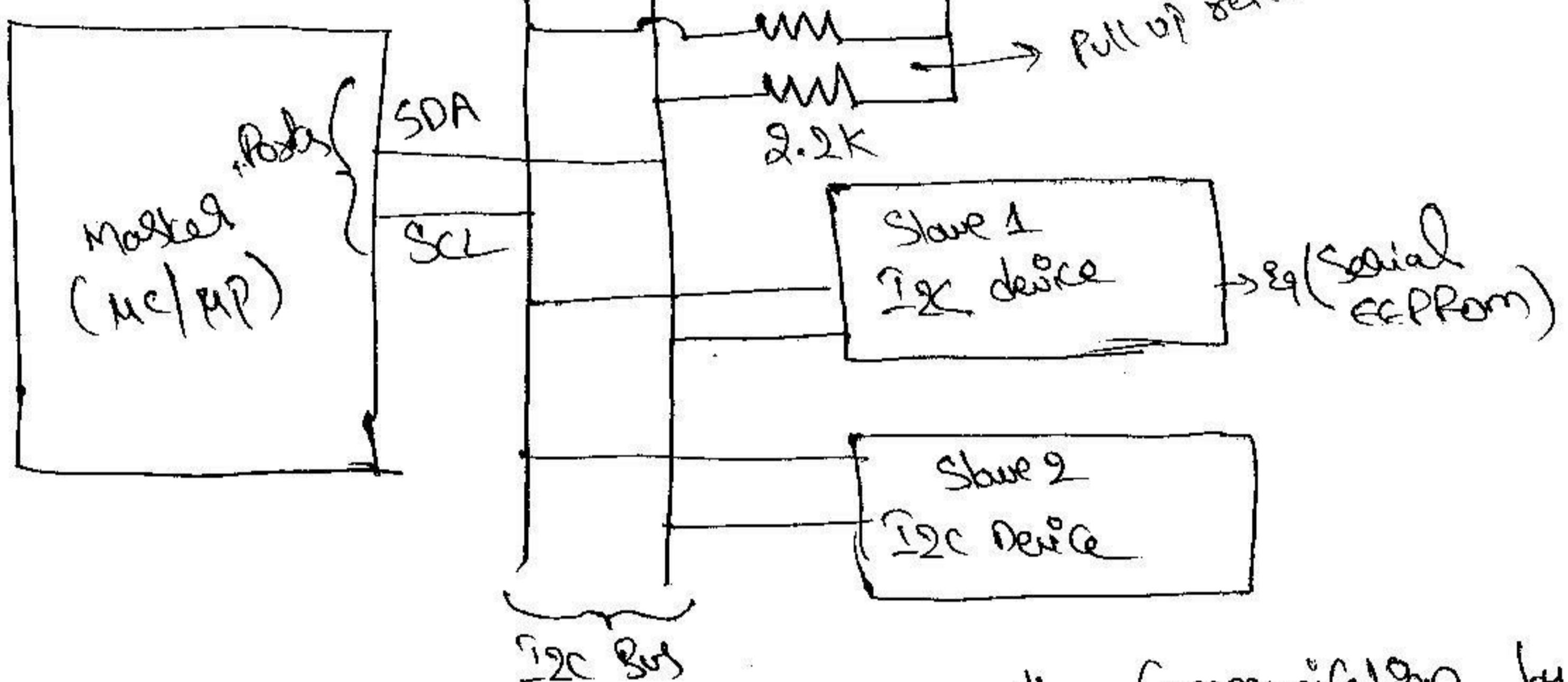
Controlling Communication

by sending data transfer

SCL SDA

$5V \rightarrow TTL$  family  
 $3.3V \rightarrow CMOS$  family

Pull up resistors



→ Master device is responsible for controlling the communication by initiating / terminating data transfer, sending data and generating necessary synchronization clock pulses.

→ Slave wait for the commands from master and respond upon receiving the command.

→ The I<sub>2</sub>C bus interface built around open drain buffer and an open drain

(or) collector transistors. When bus is in idle state the open drain / collector transistors will be in floating state and op of (SDA & SCL) switch to high impedance state.

for proper operation of bus both the bus lines should be pulled up to supply voltage (5V for TTL family & 3.3V for CMOS family) using pullup resistors. (II - 22)

→ value of pull up resistor is 2.2kΩ

### operations:-

- 1) Master device pulls clock line (SCL) of bus to High. → (Start Condition)
- 2) If dataline (SDA) is Low when (SCL) ↑
- 3) M.D sends 7bit (00) 10bit wide of slave device to which it works to communicate over SDA line  
    { if Bit value = 1 → Read  
    " " = 0 → write
- 4) For Read / write operation
- 5) MD waits for Acknowledgment (Ack) from slave device whose address sent on bus along Read / write operation command.
- 6) Slave device connected to bus compare the address received.
- 7) Up on Receiving of (Ack) MD sends 8-bit data to slave device over SDA line. (if Reg is write operation).  
    (if Reg is Read " ) then send master device over SDA line
- 8) → I<sup>2</sup>C bus supports 3-different data rates.  
    ① Standard mode (Data rate upto 100 kbit/sec)  
    ② Fast mode (" " " 400 kbit/sec)  
    ③ High speed " (" " " 3.4 Mbit/sec)
- 1<sup>st</sup> generation of I<sup>2</sup>C device designed to support data rate only up to 100 kbps.
- New generation operates at data rate upto 3.4 Mbps. //

(ii - 23)

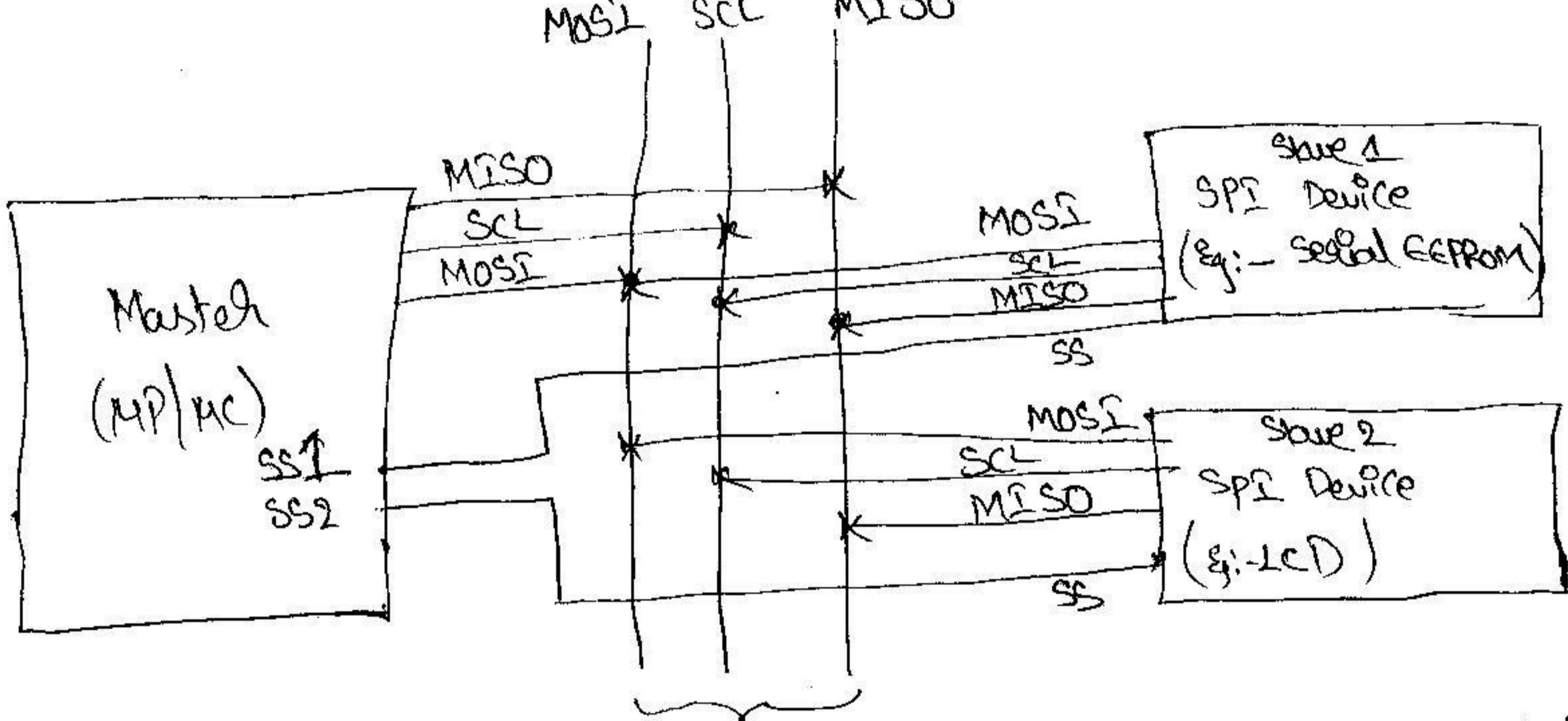
## Serial Peripheral Interface (SPI) :-

- It is synchronous bidirectional full duplex four wire serial interface bus.
- It was introduced by Motorola.
- It is a single master multi-slave system.
- It requires 4 signals for communication.
- (i) Master out slave in (MOSI) :- Signal line carrying the data from master to slave device .. also known as Slave Input / Slave Data In (SDI) (SI)

(ii) Master in slave out (MISO) :- Signal line carrying the data from slave to master device. It is also known as Slave Out (SO / SDO).

(iii) Serial clock (SCLK) :- Signal line carrying clock signal.

(iv) Slave Select (SS) :- " " for slave device select. It is an active low signal.



### Operation:-

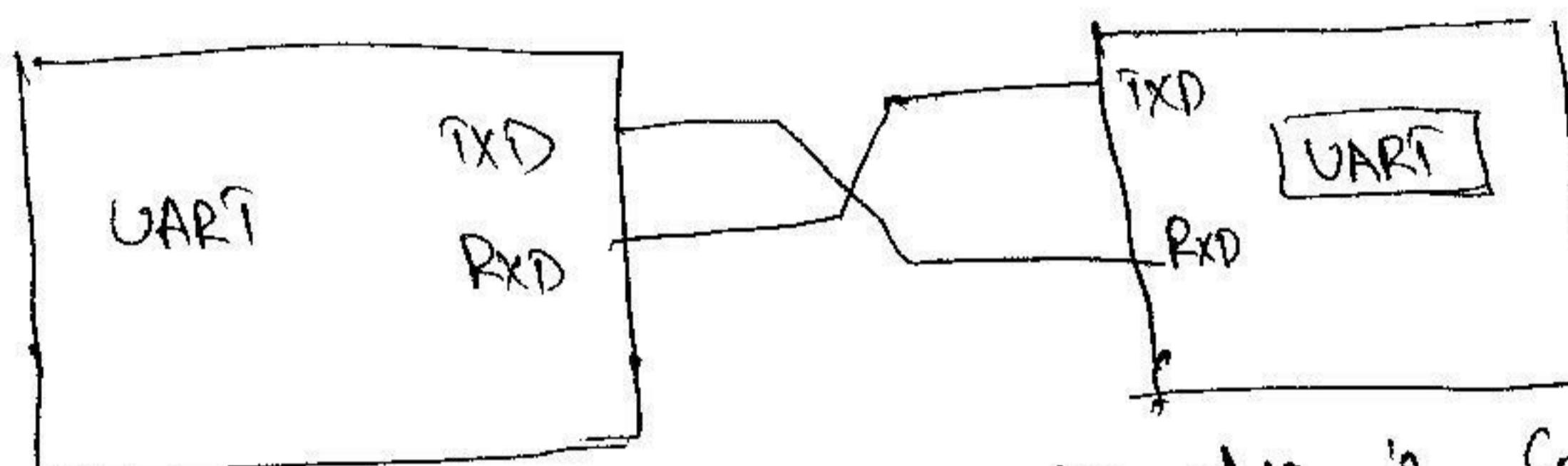
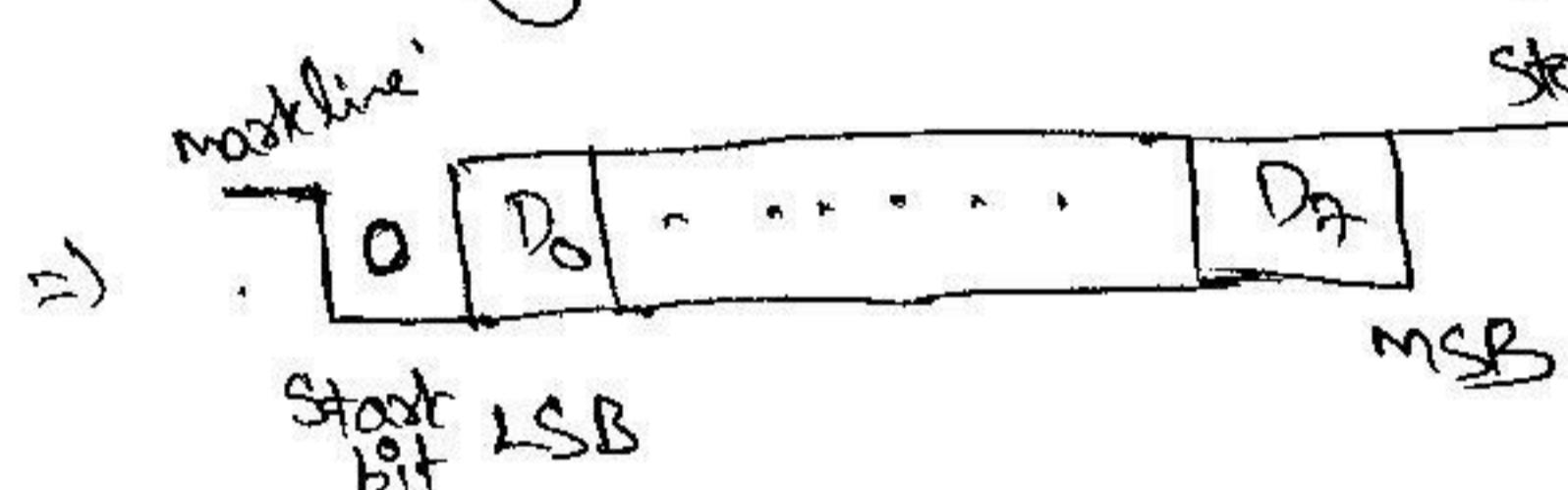
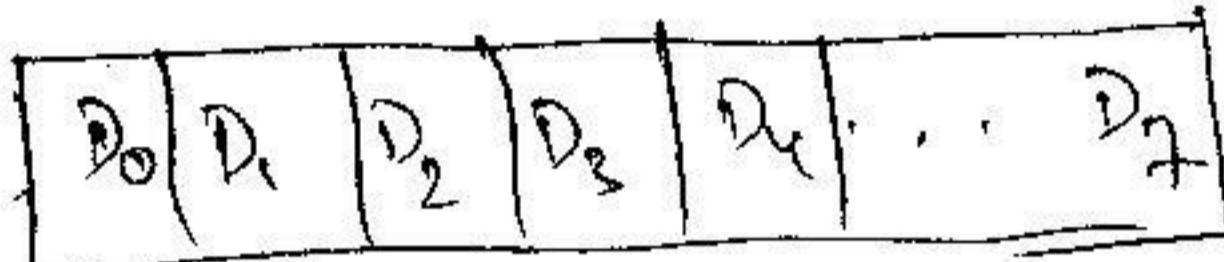
- ① Master device (MD) responsible for generating clock signal, which selects required slave device by asserting the corresponding slave devices slave selected signal low. The data out line (MISO) of all the slave devices when not selected floats at high impedance state.
- ② Serial data tx through SPI bus is fully configurable, SPI contains a certain set of Registers for holding Configuration.
- ③ SPI works on principle of shift Register.

## Universal Asynchronous Receiver Transmitter :- (UART)

(II - 24)

- Data Tx is asynchronous form of serial data tx.
- which doesn't require clock signal to synchronize (Tx & Rx) ends.
- The serial communication settings (Baudrate, no. of bits per byte, Parity, no. of start bits and stop bit and flow control). for both transmitter and receiver should be set as identical.
- The start & stop bits in communication is indicated through inserting special bits in data stream.
- while sending bytes of data start bit is added first (0) and stop bit is added at end indicates (1).

Bit value - 1 is for odd no. of 1's for parity bit  
 " " - 0 " " " Even no. of 1's for " " " 1  
 Stop bit

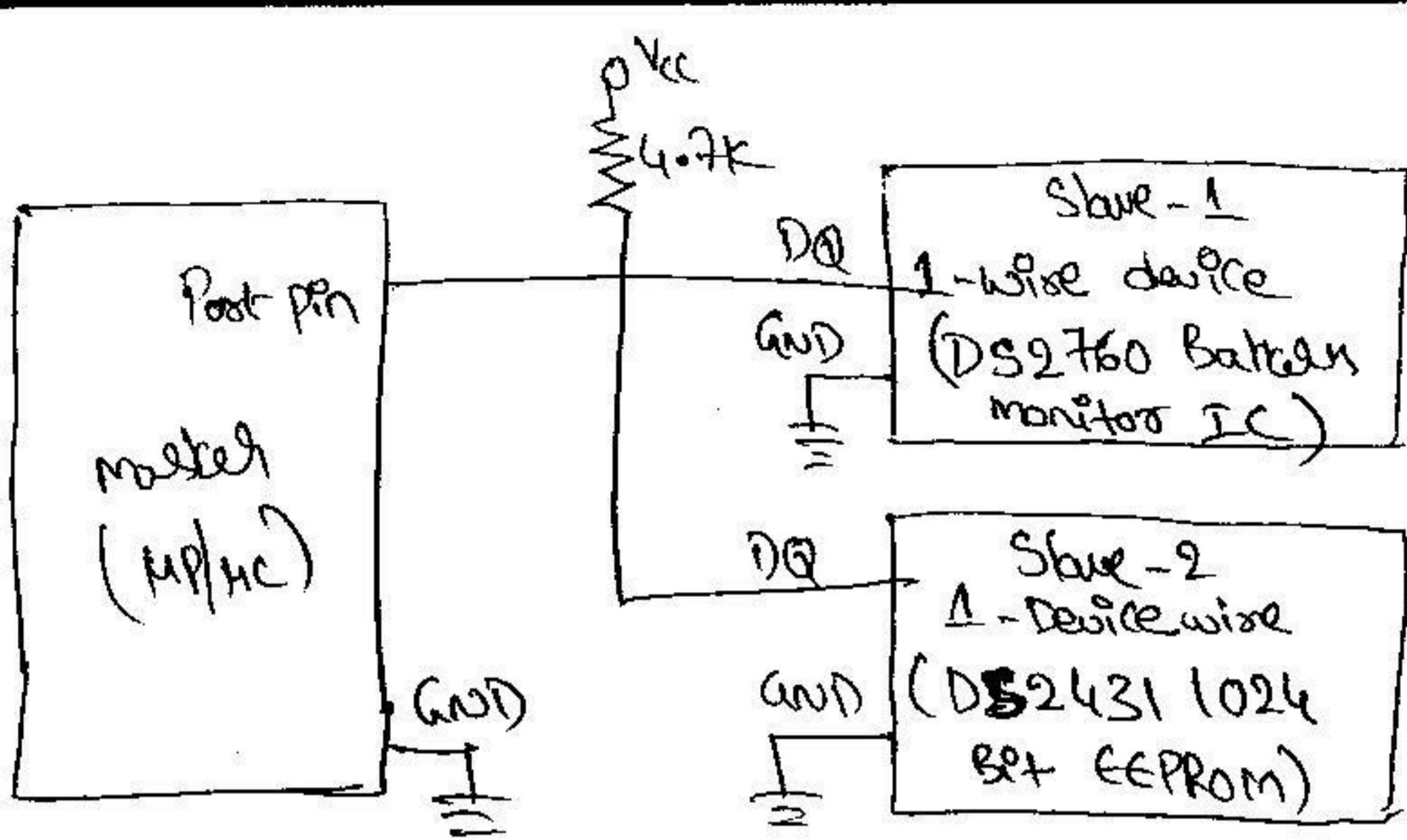


TxD - Transmitter line  
 RxD - Received "

- National Semiconductor 8250 UART chip is considered as standard setting.
- National Semiconductor 8250 UART chip is considered as standard setting.
- nowadays MP/Uc built up with integrated (UART).

### 1-wire Interface:-

- It is asynchronous half duplex communication protocol developed by Maxim Dallas semiconductors, also known as Dallas 1-wire protocol.
- It makes use of only single signal line (wire) called DQ for communication.
- Its key feature is allows power to be sent along signal wire as well.
- The I2C slave device incorporate internal capacitors (typically around 300pf) to power the device from single line.
- The 1-wire interface supports a single master and one (or) more slave devices on the bus.



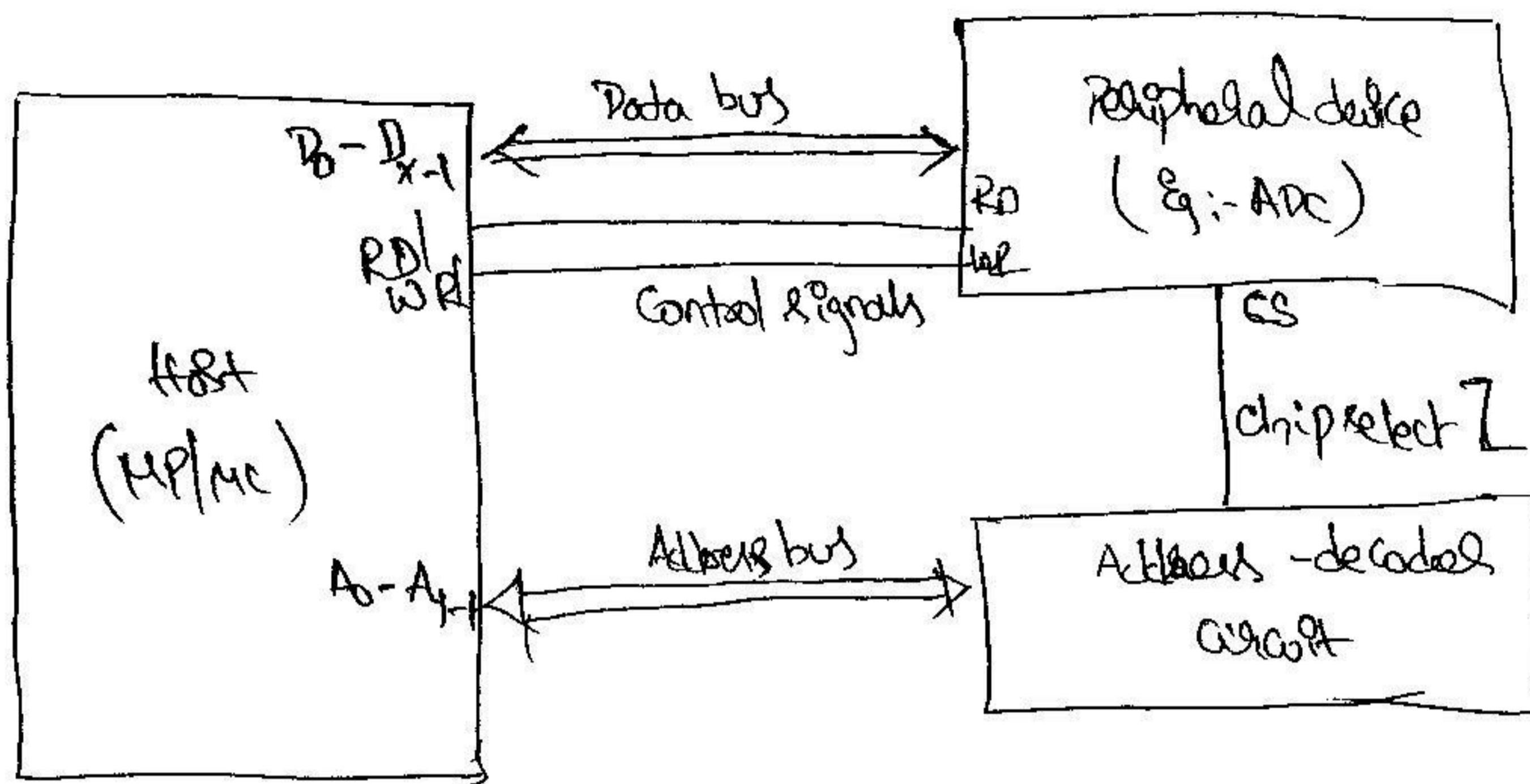
- Every 1-wire device contains a globally unique (64-bit) identification no.
- This identification no.: used for addressing individual devices present on the bus in case there are multiple slave devices connected to 1-wire bus.
- Identified has 3-parts.
  - (a) 8-bit family code
  - (b) 48-bit serial no.
  - (c) 8-bit CRC computed from first 56 bits.

### Operation:-

- The MD sends a Request 'Reset' Pulse on the 1-wire bus.
  - The slave devices present on the bus respond with a presence pulse.
  - The MD sends ROM Command (not Address Command followed by 64-bit address)
  - The MD sends a command to initiate a command which addresses slave devices. It also initiates a command to r/w internal memory (or) to read/write function command.
  - The MD sends a Read/write function command to r/w internal memory (or) register of slave address.
- Register of slave address.
- Communication over a 1-wire bus is divided into time slots (60ms)
- The communication over a 1-wire bus occupies 8-time slots
- The Reset Pulse occupies 8-time slots by master device as well as slave device by rolling 1-wire bus 'Low'.
- For starting master device as well as slave device on bus and ready for communication it should be at least 8-time slots (480 μsec).
- If slave device present on bus and ready for communication it should respond to master with a presence pulse with (60μs) of release.
- Reset Pulse by master.
- Slave device responds with presence pulse by rolling 1-wire bus Low for minimum 1 time slot (60 μsec)
- For writing (bit value - 1) the bus master pulls for (1-15 μsec) and release the bus for reset of time slots.
- A (bit value - 0) written on bus by master pulling the bus for minimum of 1-time slot (60 μsec) and max of 2-time slots (120 μsec).
- Read bit for slave device is low at (1-15 μsec)
- " (bit value - 0) device for reset time slot / / "

## Parallel interface :-

→ On-board Parallel Interface normally used for Comm - with Parallel devices which are memory mapped. (To the host of system.



width of data bus may be 4-bit ; 8-bit ; 16-bit ; 32-bit. .... etc

## (ii) External Communication Interface:- (Product level)

- a) RS 232C / RS 435 → Recommended Standard 232. Revision C
- b) USB - universal serial Bus
- c) IEEE 1394 (firewire)
- d) infrared
- e) Bluetooth.
- f) wifi
- g) zigbee
- h) General Radio Packet service (GPRS),