CHIRANJEEVI REDDY INSTITUTE OF ENGINEERING & TECHNOLOGY

(Approved by AICTE,New Delhi & Affiliated to JNTU,ANANTAPUR)
Susheela Nagar, Bellary Road, ANANTAPUR.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING.

PULSE AND DIGITAL CIRCUITS LAB
(9A04506)

(III B.Tech I Semester)

LAB-MANUAL

Head of the Department

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M-Tech.,
Assistant professor in ECE.

JAWAHARLAL NEHRU
TECHNOLOGICAL UNIVERSITY ANANTAPUR
Electronics and Communication Engineering
(9A04506) PULSE & DIGITAL CIRCUITS LAB
(Common to ECE, E Con E, EIE)
B.Tech III-I Sem. (E.C.E.)

Minimum Twelve experiments to be conducted:

1. Linear wave shaping.
2. Non Linear wave shaping – Clippers.
3. Non Linear wave shaping – Clampers.
4. Transistor as a switch.
5. Study of Logic Gates & Some applications.
6. Study of Flip-Flops & some applications.
7. Sampling Gates.
8. Astable Multivibrator.
9. Monostable Multivibrator.
10. Bistable Multivibrator.
11. Schmitt Trigger.
12. UJT Relaxation Oscillator.
13. Bootstrap sweep circuit.
14. Constant Current Sweep Generator using BJT.

Equipment required for Laboratories:

1. RPS - 0 – 30 V
2. CRO - 0 – 20 M Hz.
3. Function Generators - 0 – 1 M Hz
4. Components
5. Multi Meters

PULSE AND DIGITAL CIRCUITS LAB

LIST OF EXPERIMENTS

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1. LINEAR WAVESHAPING

A.INTEGRATOR

AIM: To observe the response of RC Low pass circuit for a square wave input for different time constants

i) RC>>T ii) RC = T iii) RC<<T and to determine rise time for RC<<T

APPARATUS:

1. Function Generator
2. CRO
3. Decade Resistance Box
4. Capacitor - 0.1 μ F
5. Breadboard
6. Connecting wires

CIRCUIT DIAGRAM:

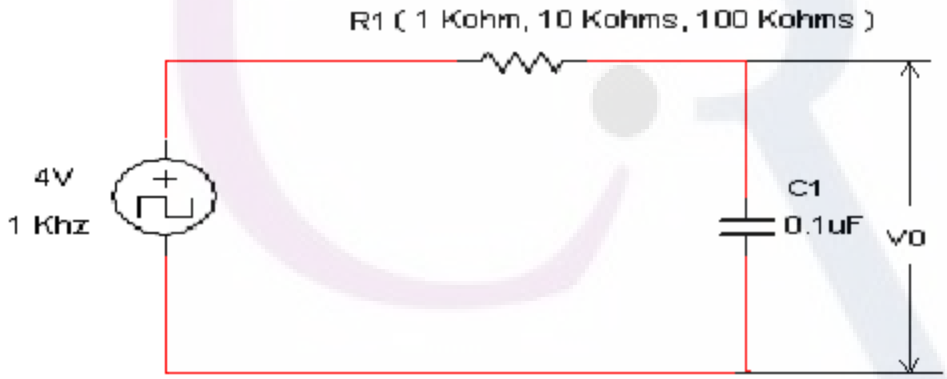
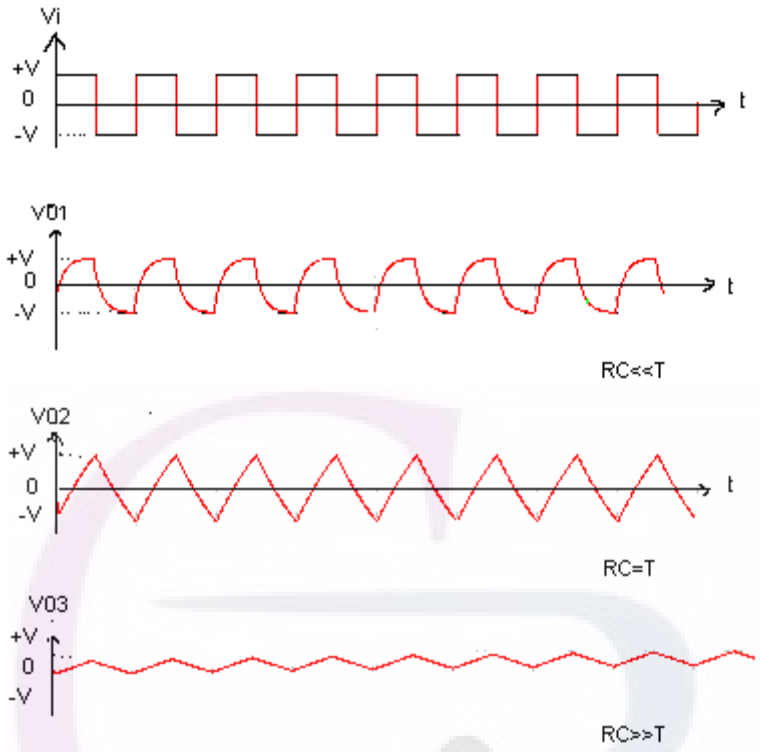


Figure 1: RC Low pass circuit

MODEL WAVE FORMS:



OBSERVATIONS:

V_i(volt)	R	C	RC	T	V_o(volt)

DESIGN:

1. Choose T = 1msec.
2. Select C = 0.01μF.
3. For RC = T; select R.
4. For RC >> T; select R.
5. For RC << T; select R.

THEORY:

LINEAR WAVE SHAPING

The process where by the form of a non-sinusoidal signal is altered by transmission through a linear network is called "LINEAR WAVE SHAPING".

A) RC Low Pass Circuit:

The resistor in series arm and capacitor in the shunt arm, The resulting circuit is called Low pass circuit. The circuit passes low frequencies readily but attenuates high frequencies because the reactance of the capacitor decreases with increasing frequency. At very high frequencies the capacitor acts as a virtual short circuit and the output falls to zero. This circuit also works as integrating circuit. A circuit in which the output voltage is proportional to the integral of the input voltage is known as integrating circuit. The condition for integrating circuit is RC value must be much greater than the time period of the input wave (RC>>T)

Let ***Vi*** = alternating input voltage.

i = resulting current

then the output voltage is proportional to the integral of the input voltage.

$$Vo = \frac{1}{RC}\int_0^t vi \; dt$$

PROCEDURE:

1. Connect the circuit as shown in the figure1.
2. Connect the function generator at the input terminals and CRO at the output terminals of the circuit.
3. Apply a square wave signal of frequency 1 KHz at the input. (T = 1 msec.)
4. Observe the output waveform of the circuit for different time constants.
5. Calculate the rise time for low pass filter and compare with the theoretical values.
6. For low pass filter select rise time (t_r) = 2.2 RC (theoretical). The rise time is defined as the time taken by the output voltage to rise from 0.1 to 0.9 of its final value.

PRECAUTIONS:

1. Connections should be tight.
2. Take care when biasing the supply.

RESULT:

VIVA QUESTIONS:

1. What is high pass circuit under what condition it acts as a differentiator?
2. What is low pass circuit under what condition it acts as a integrator?
3. Show theoretically how you get a triangular wave when a square wave is given to an integrator?
4. What happens when a sine wave is applied to a differentiator or integrator circuit?
5. What are different applications of a differentiator?
6. What are different applications of a integrator?
7. What is the ideal value of phase shift offered by an RC circuit?

1 (B) .DIFFERENTIATOR

AIM: To observe the response of RC High pass circuit for a square input for different time constants i) RC>>T ii) RC = T iii) RC<<T and to determine percentage tilt for RC = T

APPARATUS:

1. Function generator
2. CRO
3. Resistors 1k, 10k, 100k
4. Capacitor 0.1 μ F
5. Bread board
6. Connecting wires

CIRCUIT DIAGRAM:

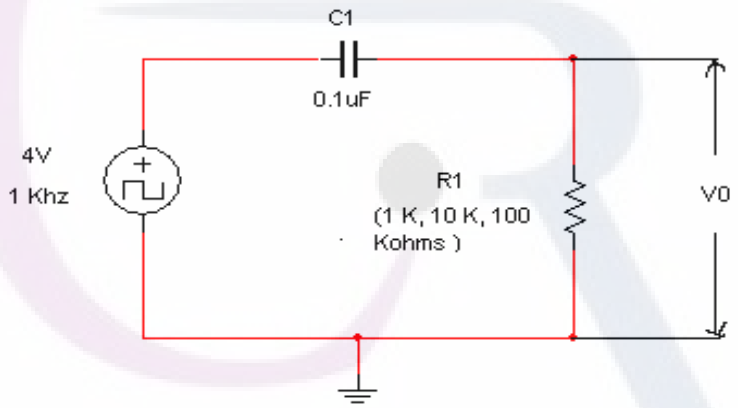
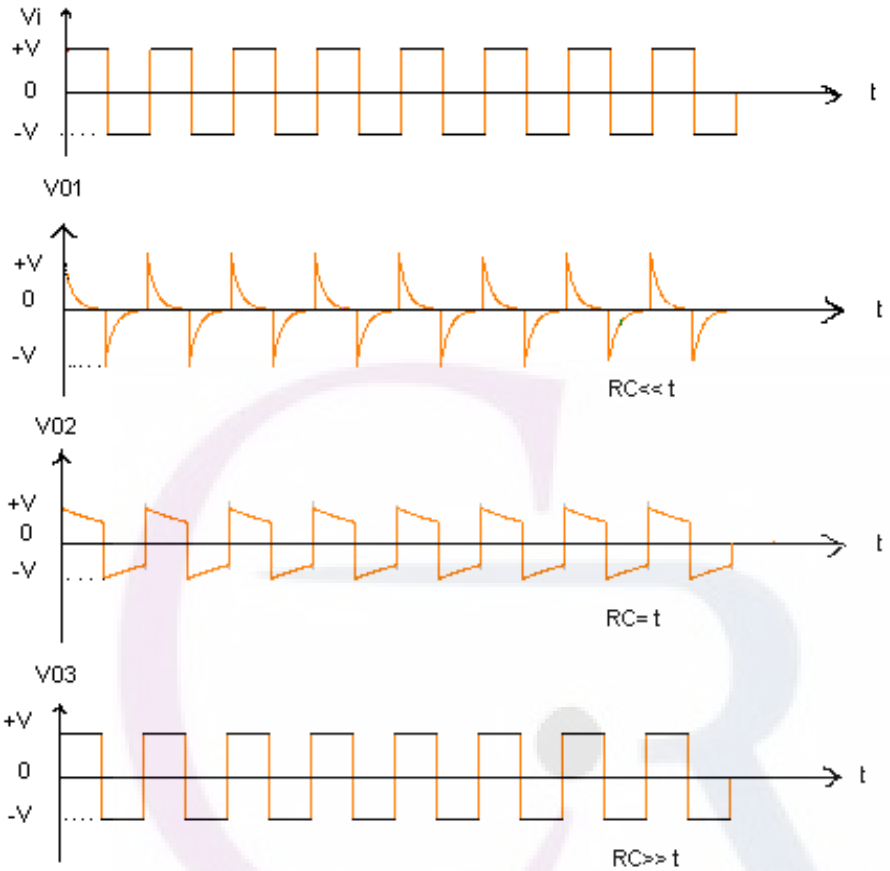


Figure 2: RC High pass circuit

MODEL WAVE FORMS:



OBSERVATIONS:

V_i(volt)	R	C	RC	V_0(volt)

DESIGN:

1. Choose T = 1msec.
2. Select C = 0.01μF.
3. For RC = T; select R.
4. For RC >> T; select R.
5. For RC << T; select R.

THEORY:

B) RC High Pass Circuit.

The Capacitor in series arm and resistor in the shunt arm, the resulting circuit is called High pass circuit The higher frequency components in the input signal appears at the output with less attenuation than the lower frequency components because the reactance of the capacitor decreases with increase in frequency. This circuit works as a differential circuit. A circuit in which the output voltage is proportional to the derivative of the input voltage is known as differential circuit. The condition for differential circuit is RC value must be much smaller then the time period of the input wave *(RC<<T)*.

Let ***Vi*** = alternating input voltage.

i = resulting current

then the output voltage is proportional to the differentiation of the input voltage.

$$V_o = RC\frac{d}{dt}v_i$$

PROCEDURE:

1. Connect the circuit as shown in the figure2.
2. Connect the function generator at the input terminals and CRO at the output terminals of the circuit.
3. Apply a square wave signal of frequency 1 KHz at the input. (T = 1 msec.)
4. Observe the output waveform of the circuit for different time constants.
5. Calculate the %tilt for high pass filter and compare with the theoretical values.
6. % tilt = *(T/2RC) * 100* (theoretical)
   % tilt = *[(V1 – V1^1) / (V / 2)] *100* (practical)

PRECAUTIONS:

1. Connections should be tight.
2. Take care when biasing the supply**.**

RESULT:

VIVA QUESTIONS:

1. What is high pass circuit under what condition it acts as a differentiator?
2. What is low pass circuit under what condition it acts as a integrator?
3. Show theoretically how you get a triangular wave when a square wave is given to a integrator?
4. What happens when a sine wave is applied to a differentiator or integrator circuit?
5. What are different applications of a differentiator?
6. What are different applications of a integrator?
7. What is the ideal value of phase shift offered by an RC circuit?

2 . NON-LINEAR WAVE SHAPING - CLIPPERS

AIM: To study the clipping circuits for different reference voltages and to verify the responses.

APPARATUS:

1. Diodes 1N4001 – 2 NOS
2. Resistor 1K Ω
3. Regulated power supply
4. CRO
5. Function Generator
6. Bread Board
7. Connecting wires

CIRCUIT DIAGRAMS:

1. **Shunt diode positive clipper**

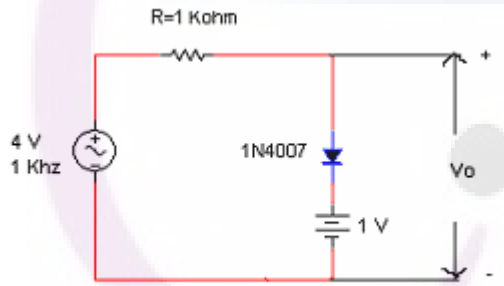
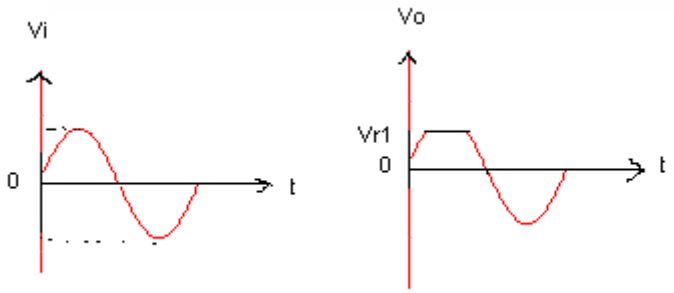


Figure :1

i) Input signal **ii) Output signal**



2. Shunt diode negative clipper

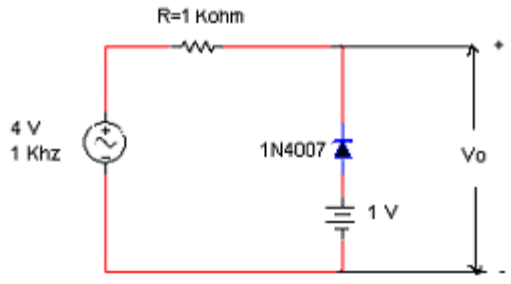
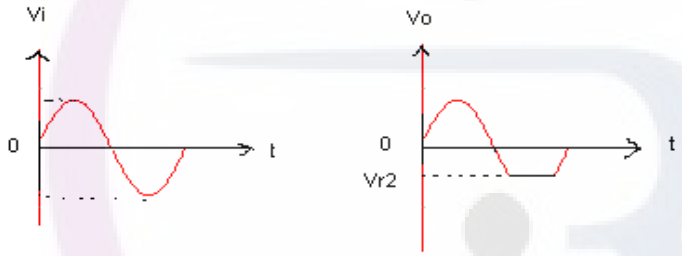


Figure : 2

i) Input signal **ii) Output signal**



3. Series diode positive clipper

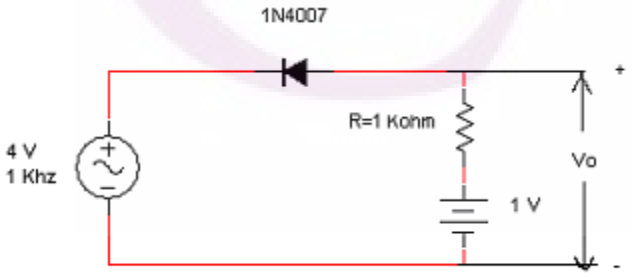
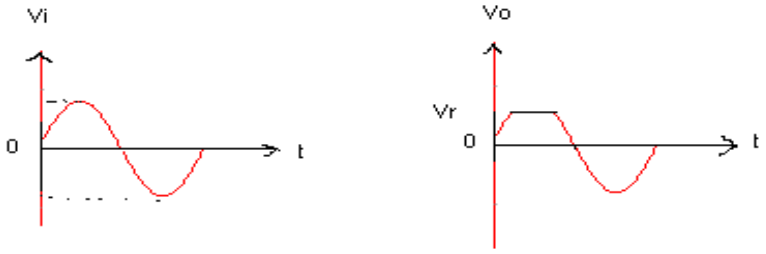


Figure :3

i)Input signal **ii) Output signal**



4. Series diode negative clipper

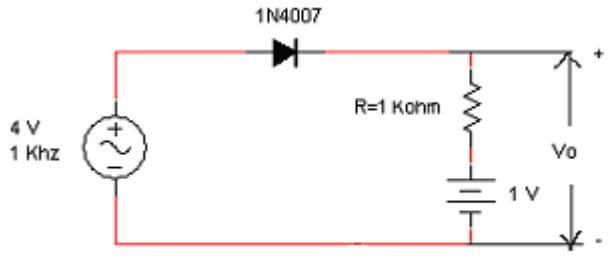
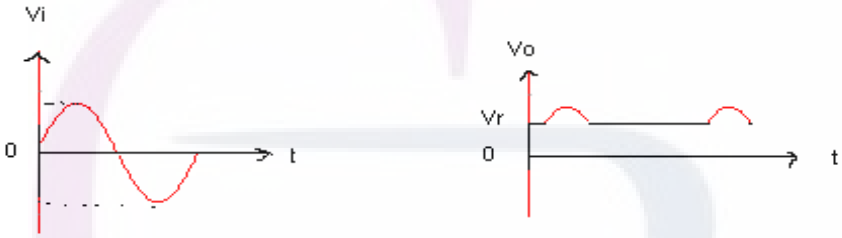


Figure :4

i) Input signal **ii) Output signal**



5. Two level clipper

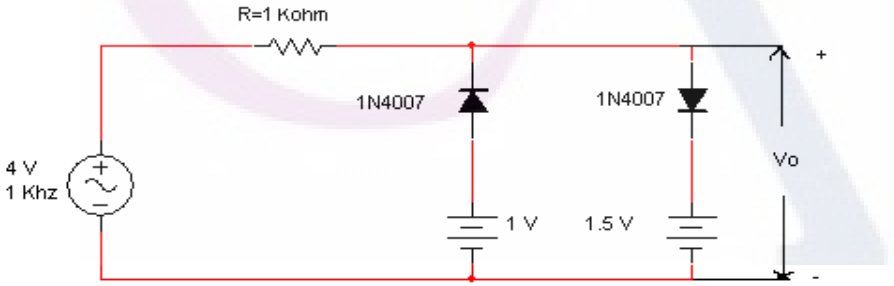
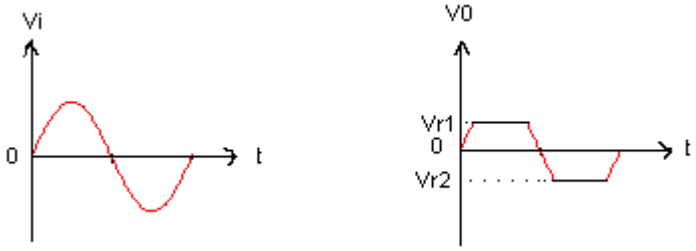


Figure:5

i)Input signal **ii) Output signal**



THEORY:

When sinusoidal or non-sinusoidal waveforms are applied to non linear networks consisting one nonlinear device such as diode or transistor the resultant output waveform may be different from the i/p waveform. Hence the nonlinear circuit said to shape the i/p voltage waveform. This is called non linear wave shaping.

The clipping circuit may be defined as a circuit that limits the amplitude of a voltage by removing the signal above or below the reference voltage. Either +ive side or –ive side or both sides of the waveform may be clipped. Clipping circuits are also known as voltage or current limiters.

The diode clipper circuits are classified according to the placement of the diode in the circuit as a series diode clipper or shunt diode clipper.

SHUNT DIODE CLIPPERS:

i) WITH POSITIVE BIAS CLIPPERS:

Assuming the diode used is an ideal the shunt diode clipper with +ve bias is shown in the figure. The diode is forward biased only when Vi > Vr as the cathode is at the potential of Vr. To make the diode forward bias the potential at the cathode must be greater than Vr.

During the +ve half cycle Vi>Vr the diode acts as a short circuit and o/p voltage is equals to the reference voltage Vr. When Vi <Vr the diode is reverse bias and the total i/p voltage Vi appears across the open circuit o/p terminals as shown in the figure.

ii) WITH NEGATIVE BIAS CLIPPERS:

Assuming the diode used is an ideal in the shunt clippers with –ve bias is shown in the figure. The diode is forward bias during –ve half cycle when Vi<Vr during this period diode acts as a short circuit and the o/p voltage equals to the reference voltage Vr.

During complete +ve half cycle as well as during –ve half cycle when Vi > Vr the diode is reverse biased and it acts as a open circuit. Therefore Vi appears across open circuit terminals of the o/p circuit.

SERIES DIODE CLIPPERS:

Assuming the diode used is an ideal the series diode clippers with +ve bias as shown in the figure, The diode conducts during –ve half cycle as well as during +ve half cycle when Vi<Vr as the anode of the diode is at the potential Vr. During this conduction the current flows through the resistor when an o/p voltage appears across the open circuited o/p terminals which is equal to Vi . During +ve half cycle when Vi >Vr

the diode is reverse biased no current flows through the resistor and the o/p voltage equal to the reference voltage Vr.

Assuming the diode used is an ideal one the series diode clipper with +ve bias is shown in the figure. The diode conducts only when Vi >Vr as the cathode is at the potential of Vr. To make diode forward bias anode potential must be greater than Vr. During +ve half cycle when Vi > Vr the diode is forward bias and the current flows through the diode as well as resistor. An o/p voltage appears across the open circuit output terminals which are equal to Vi. During –ve half cycle as well as during +ve half cycle when Vi<Vr the diode is reverse bias and no current flows through the diode , hence through the resistor . Thus o/p voltage equals to the reference voltage Vr.

UNBIASED SHUNT CLIPPERS:

During the +ve half cycle the diode is forward biased and diode acts as a short circuit for the i/p signal. Therefore o/p voltage is zero. During –ve half cycle the diode is reverse biased and the diode acts as an open circuit. Thus Vi=Vr . During –ve half cycle the diode is forward bias and acts as a short circuit for the i/p signal. Therefore o/p is equal to zero. During +ve half cycle the diode is reverse biased and the diode acts as an open circuit thus the o/p voltage = i/p voltage.

DOUBLE DIODE CLIPPERS:

This type of clippers is to clip at two independent levels. When both diodes are not conducting o/p follows the i/p.

Diode D1 conducts during +ve half cycle when Vi>Vr1. Where as Diode D2 conducts during the –ve half cycle when Vi> Vr2. Thus during the period Vi<Vr1 and Vi>Vr2 both diodes are reverse biased and the o/p voltage follows the i/p as shown in the figure.

PROCEDURE:

1. Connect the circuit as shown in the figure 1.
2. Connect the function generator at the input terminals and CRO at the output terminals of the circuit.
3. Apply a sine wave signal of frequency 1KHz, Amplitude greater than the reference voltage at the Input and observe the output waveforms of the circuits.
4. Repeat the procedure for remaining figures.

PRECAUTIONS:

1. Connections should be tight.
2. Take care when applying proper supply.

RESULT:

VIVA QUESTIONS:

1. Define clipping?
2. Define clamping?
3. Define peak inverse voltage of diode?
4. What are the other names for the clamper?
5. What are the applications of clampers?
6. Explain the clipping process?

3. NON-LINEAR WAVESHAPING - CLAMPERS

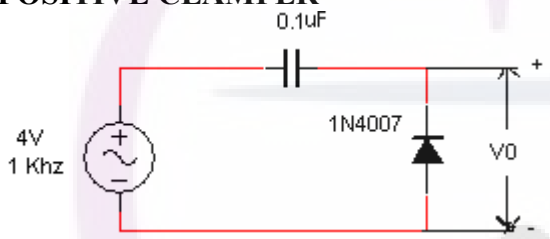
AIM: To study the clamping circuits for different reference voltages and to verify the responses.

APPARATUS:

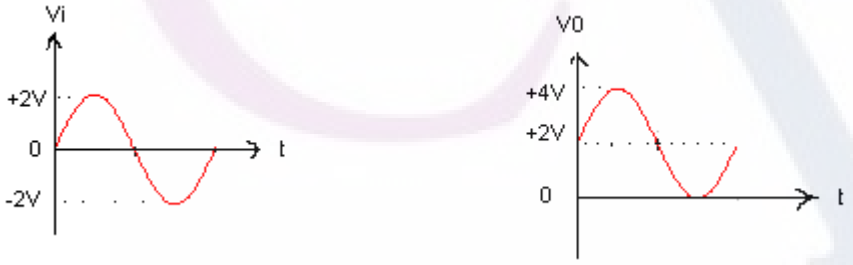
1. Diode – 1N4001 – 1 No
2. Capacitor 0.1 μF
3. Resistor - 1K Ω
4. Function Generator
5. RPS
6. CRO

CIRCUIT DIAGRAMS:

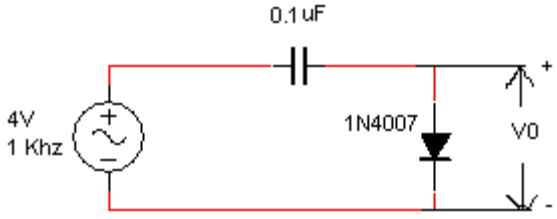
1. POSITIVE CLAMPER



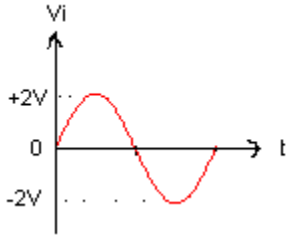
1. Input signal **2.Output signal**

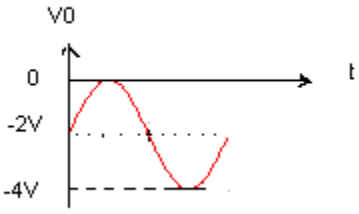


2. NEGATIVE CLAMPER



1. Input signal **2.Output signal**





THEORY:

Clamping circuits are circuits, which are used to clamp or fix the extremity of a periodic wave form to some constant reference level. Clamping circuits may be one way clamps or two way clamps.

The clamping circuits only changes the dc level of the input signal .It does not affect its shape. Clamping circuits may be positive voltage clamping circuits or negative voltage clamping circuits. In positive clamping, the negative extremity of the wave form is at the reference level and the entire wave form appears above the reference level. i.e. the output wave form is positively clamped with reference to the reference level. In negative clamping the positive extremity of the wave form is fixed at the reference level and the entire wave form appears below the reference voltage. i.e. the output wave form is negatively clamped with reference to the reference level.

The capacitors are essential in the clamping circuits. The difference between the clipping and clamping circuits is that while the clipper clips off an unwanted portion of the input wave form, the clipper simply clamps the maximum positive or negative peak of the wave form to a desired level.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. I/P signal is applied to the circuit with the amplitude of 4v p-p and 1 KHz frequency.
3. The AC / DC push button switch of CRO is to be kept in DC mode.
4. Note down the o/p amplitude for each and every circuit.
5. The O/P waveforms are to be drawn on the graph sheet.

RESULT:

VIVA QUESTIONS:

1. Define clipping?
2. Define clamping?
3. Define peak inverse voltage of diode?
4. Draw the o/p waveforms for

    i) Series diode +ve clipper
    ii) Series diode -ve clipper
    iii) Shunt diode +ve clipper
    iv) Shunt diode -ve clipper
    v) Two level clipper
5. Draw the o/p wave forms for
    1. +ve clamper
    2. –ve clamper
6. What are the other names for the clamper?
7. What are the applications of clampers?
8. Explain the clipping process?

4.TRANSISTOR AS A SWITCH

AIM: To design and observe the performance of a transistor as a switch

APPARATUS:

1. Breadboard Trainer
2. Transistor (BC107)
3. Resistors
4. Function generator
5. Regulated power supply (0-30V)
6. CRO
7. Light Emitting Diode (LED)
8. Connecting wires.

CIRCUIT DIAGRAMS:

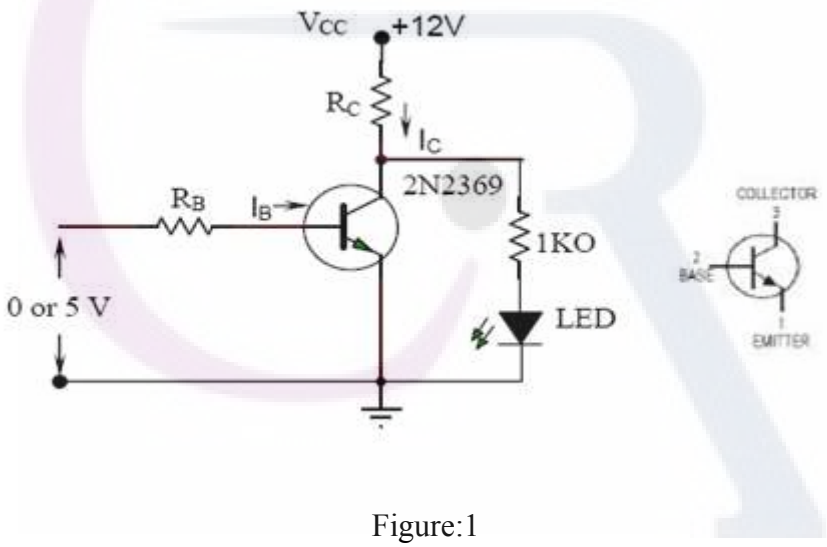
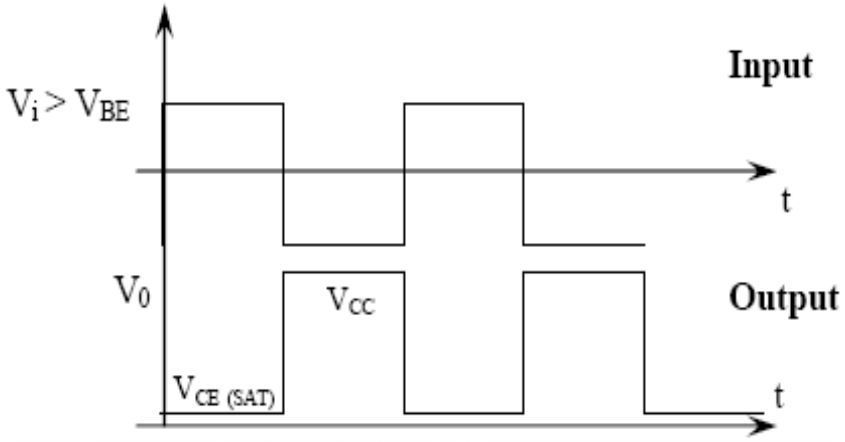


Figure:1

MODEL WAVE FORMS:



OBSERVATIONS:

	V_{BE}	V_{CE}	V_{CB}
When transistor is ON			
When transistor is OFF			

DESIGN :

Ic max = 5mA, V_{BE} = 0.7V, $V_{CE\ (sat)}$ = 0.2V, Vcc = 12V.

Rc min= V_{CC} / Ic max=?

$I_{CS} = (V_{CC} - V_{CE\ (sat)}) / Rc$=?

$I_B = I_{CS}/ h_{fe}=(V_i-V_{BE})/R_{B=}$?

$R_B = (V_i - V_{BE}) / I_{B=?}$

THEORY:

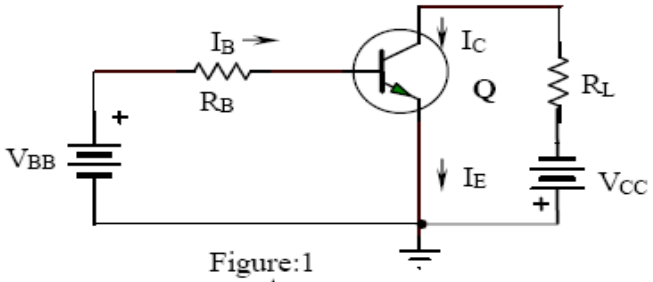


Figure:1

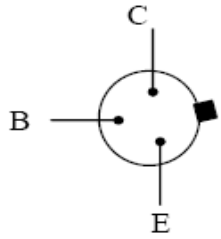


Figure:2

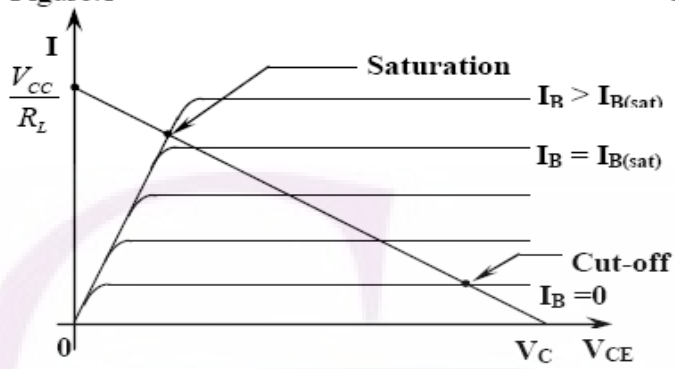


Figure:3

Fig.1. Transistor as a switch. Fig.2 Pin configuration of transistor 2N2369.
Fig.3 Output characteristics with load line(d.c)

The transistor *Q* can be used as a switch to connect and disconnect the load *RL* from the source *VCC*. When a transistor is saturated, it is like a closed switch from the collector to the emitter. When a transistor is cut-off, it is like an open switch

$$I_C = (V_{CC}-V_{CE})/R_L$$

Cut-off and Saturation: The point at which the load line intersects the *IB = 0* curve is known as cut-off. At this point, base current is zero and collector current is negligible small i.e. only leakage current *ICEO* exists. At cut-off, the emitter diode comes out of forward bias and normal transistor action is lost.

$$VCE(sat) = VCC$$

The intersection of the load line and the *IB = IB(sat)* is called saturation. At this point base current is *IB(sat)* and the collector current is maximum. At saturation, the collector diode comes out of reverse bias, and normal transistor action is again lost.

$$Ice(sat)=Vcc/R_L$$

In figure:3 *IB(sat)* represents the amount of base current that just produces saturation. If base current is less than *IB(sat)*, the transistor operates in the active region somewhere

between saturation and cut-off. If base current is greater than *IB(sat),* the collector current approximately equals V_{CC}/R_C. The transistor appears like a closed switch

$$V_{BB}=V_{BE}+I_BR_B$$

If base current (*IB*) is zero, the transistor operates at the lower end of the load line and the transistor appears like an open switch.

PROCEDURE :

1. Connect the circuit as shown in the figure 1.
2. Connect 12V power supply to *VCC* and 0V to the input terminals.
3. Measure the voltage (1) across collector – to – emitter terminals, (2) across collector – to – base terminals and (3) Base – to – emitter terminals.
4. Connect 5V to the input terminals.
5. Measure the voltage (1) across collector – to – emitter terminals, (2) across collector – to – base terminals and (3) Base – to – emitter terminals.
6. Observe that the LED glows when the input terminals are supplied with 0 volts. The LED will NOT glow when the input voltage is 5V.
7. Remove the load (1kΩand LED) and DC power supply (connected between RB and Gnd.). Now connect a function generator to the input terminals.
8. Apply Square wave of 1 KHz, V (p-p) is 10V
9. Observe the waveforms at the input terminals and across collector and ground.
10. Plot the waveform on a graph sheet. Note the inversion of the signal from input to output.

RESULT:

VIVA QUESTIONS:

1. What are the different switching times of a transistor?
2. Define ON time of a transistor?
3. Define OFF time of a transistor?
4. Explain how transistor acts as a switch?
5. Define delay time (td), raise time (tr), saturation time (ts) and fall time (tf) of a transistor?

5. STUDY OF LOGIC GATES & SOME APPLICATIONS

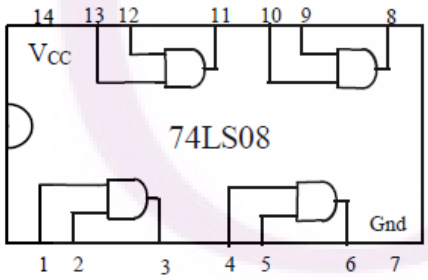
STUDY OF LOGIC GATES

AIM: To verify the truth tables of AND, OR, NOT, NAND, NOR, and EX-OR gates.

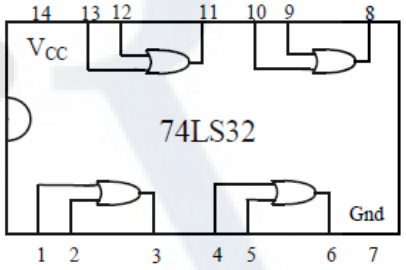
APPARATUS:

1. Bread board IC trainer
2. IC74LS08 (AND)
3. IC74LS32 (OR)
4. IC 74LS04 (NOT)
5. IC74LS00 (NAND)
6. IC74LS02 (NOR)
7. IC74LS86 (EX-OR)
8. Patch cards

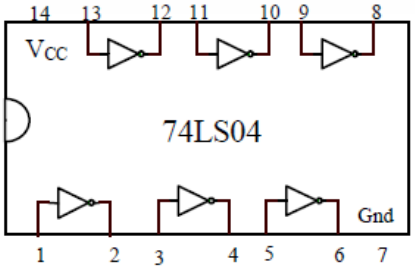
CIRCUIT DIAGRAM



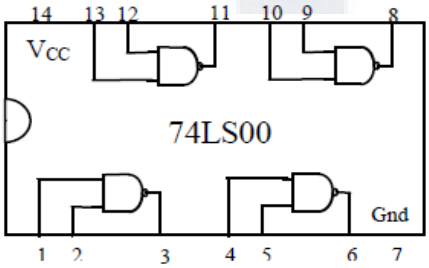
AND GATE IC



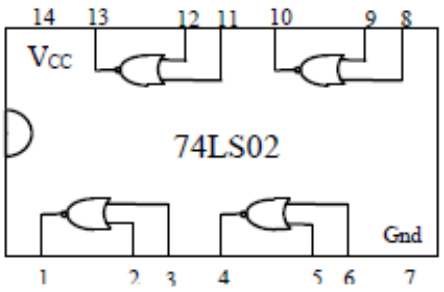
OR GATE IC



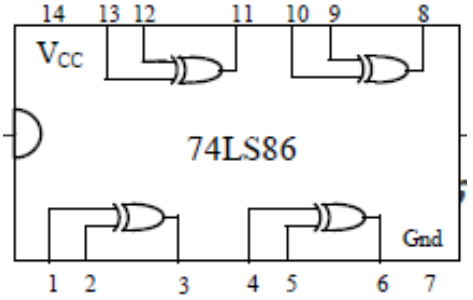
NOT GATE IC



NAND GATE IC



NOR GATE IC



EX-OR GATE IC

OBSERVATIONS:

AND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

OR Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

NAND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

NOR Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

NOT Gate

A	Y
0	
1	

EX-OR Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

THEORY:

In digital electronic circuits two discrete levels are recognized as two logic levels logic '1' and logic '0'. These are also known as high and low logic levels depending up on the actual voltages. There are two logic circuits

1. Positive logic – in which higher voltage level corresponds to 1 (high) and the lower level corresponds to 0(low)
2. Negative logic - in which the lower voltage level corresponds to logic 1 and the higher voltage level corresponds to logic 0.

In digital circuits there are only 4 basic operations which are required to be performed. These are AND, OR, NOT, and EX-OR. There are two types of digital circuits.

1. Combinational circuits
2. Sequential circuits.

COMBINATIONAL CIRCUITS:

In combinational circuits the o/p at any 4 instances of time depend completely on the i/p's present at the instance of time. In such circuits only AND, OR, NOT operations are required.

SEQUENTIAL CIRCUITS:

In sequential circuits the o/p at any instant of time depend up on the past o/p's as well as the present i/p's at that instant of time. Here in addition to AND, OR, NOT operations, Flip-Flops are also defined which can be used to realizes AND, OR, NOT, operations.

The function, logic diagram and truth table for each of the gates are given. These tables illustrates AND, OR, NAND, and NOR gates with two i/p's only. But the number of i/p's can be more than also.

These functions can be realized by using discrete devices such as Diodes, BJT and FET's. However since the gates are available in the form of ICs.

BASIC OPERATIONS:

AND GATE:

IC4LS08 is quad 2-i/p AND gate: It requires 5v between VCC and ground terminals. The o/p of AND gate is HIGH when both the two i/p's of AND gate are HIGH. Otherwise the o/p always LOW.

IC74LS32 is quad 2-i/p OR gate: It requires 5v between VCC and ground terminals. The o/p of OR gate is LOW when both the i/p's are LOW. Other wise the o/p always remains at "HIGH".

IC4LS04 is hex NOT gate: It requires 5v between VCC and GND terminals. The o/p of NOT gate is always the complement of i/p.

IC74LS00 is quad 2-i/p NAND gate: It requires 5v between VCC and ground terminals. It is the series connection of AND and NOT gates. The o/p of NAND gate is LOW when both the i/p's of NAND gates are HIGH. Otherwise the o/p is HIGH.
IC74LS02 is quad 2-i/p NOR gate: It requires 5v between VCC and ground terminals. It is the series connection of OR and NOT
Gates. The o/p of NOR gate is HIGH only when both the i/p's of the NOR gate are at LOW. Other wise the o/p remains at LOW.

IC74LS86 is quad 2-i/p EX-OR gate: It requires 5v between VCC and ground terminals. The o/p of EX-OR gate is HIGH when two different i/p's are applied . Otherwise the o/p is LOW.

PROCEDURE:

1. +5V DC is applied at VCC (pin no:14) of each IC w.r.t. ground(pin no:7).
2. I/p's are applied (at pin no's 1 &2) and o/p is taken from (pin no:3).
3. I/p's are applied from toggle switches and o/p is observed at o/p indicators.

PRECAUTIONS:

1. Avoid loose connections on Breadboard.
2. Take care while making connections with NOT and NOR gates.

RESULT:

5(b) APPLICATIONS

HALF ADDER, FULL ADDER AND HALF SUBTRACTOR

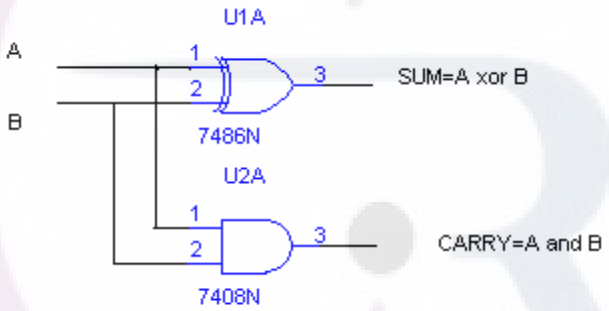
AIM: To construct and verify the truth tables of half adder half Sub tractor and full adder.

APPRATUS:

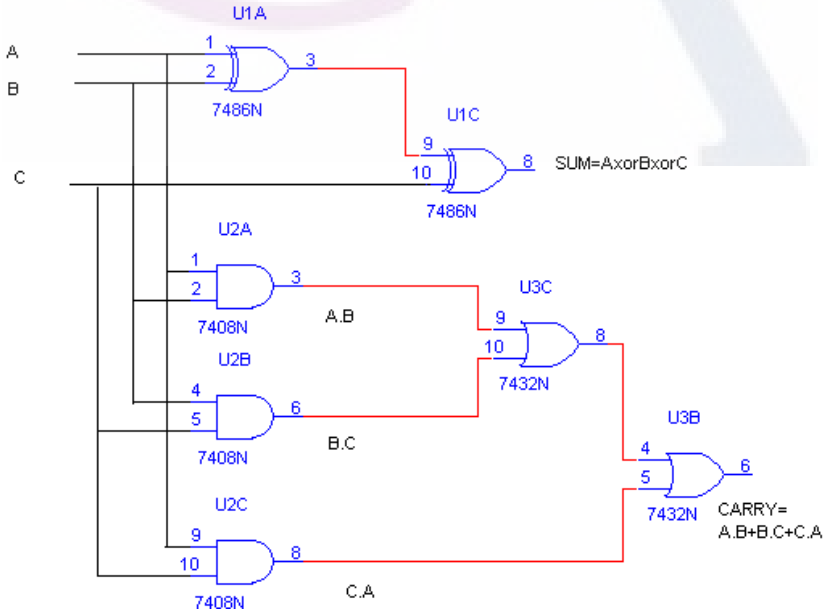
i. IC 7432-- OR gate
ii. IC 7408--AND gate
iii. IC 7404—NOT gate
iv. IC 7486—EX-OR gate
v. Bread board IC trainer
vi. Patch cards

CIRCUIT DIAGRAMS:

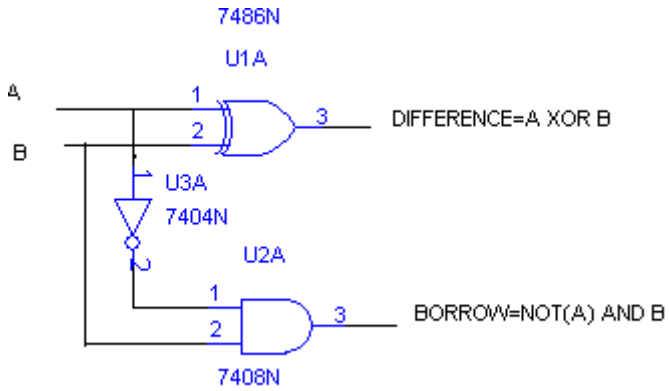
Half adder:



Full adder:



Half Subtractor:



THEORY:

Digital computers today perform a number of tasks out of which arithmetic operations like addition and subtraction are basic operations. The simple addition consists of 4 elementary operations produces a sum and carry. A combinational circuit that performs the addition of two bits is called half adder

$SUM=A \oplus B$

$CARRY=AB$

And which performs the addition of 3 bits is a full adder. A Full adder can be design by using two half adders.

$SUM=A \oplus B \oplus C$

$CARRY=AB+BC+CA$

A Half sub tractor circuit is combinational circuit that subtracts two bits and produces their difference.

$DIFFERENCE = A \oplus B$

$BORROW= \overline{A}\, B$

PROCEDURE:

Half adder:

1. All the connections are made as per the circuit diagram.
2. Inputs are applied from logic inputs and outputs are observed at the output indicators.
3. The truth table of half adder is verified.

Half Subtractor:

1. All the connections are made as per the circuit diagram.
2. Inputs are applied from logic inputs and outputs are observed at the output indicator.
3. The truth table of half sub tractor is verified.

Full Adder:

1. All the connections are made as per the circuit diagram
2. Inputs are applied from logic inputs and outputs are observed at the output indicator
3. The truth table of full adder is verified.

TRUTH TABLES:

Half Adder:

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Subtractor:

INPUTS		OUTPUTS	
A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Adder:

INPUTS			OUTPUTS	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

PRECAUTIONS:

1. Connections should be correct.
2. Pin numbers should be identified properly.

RESULT:

.

VIVA QUESTIONS:

1. What is meant by half adder?
2. What is meant by full adder?
3. What is meant by half subtractor?
4. What is meant by 1's complement?
5. What is meant by 2's complement?
6. Why do you prefer 2's complement in computers?
7. What is Boolean expression for full adder sum and carry?
8. What is the advantage of look ahead carry adder?
9. Design full adder by using half adders?
10. What is the disadvantage of look ahead carry adder?

6. STUDY OF FLIP FLOPS & SOME APPLICATIONS

STUDY OF FLIP FLOPS USING ICS

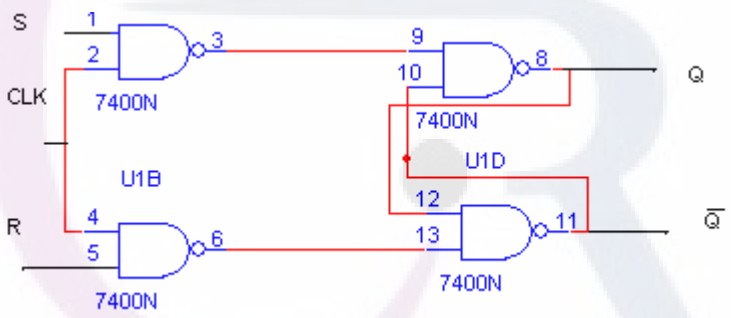
AIM: To construct and verify the truth tables of SR flip flop, JK flip flop, D and T flip - flop.

APPRATUS:

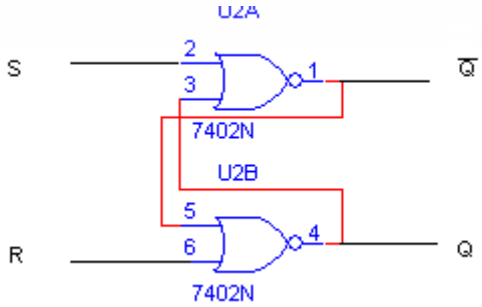
i. IC 7473 JK flip flop
ii. IC 7400NAND gate
iii. IC 7404 NOT gate
iv. Patch cards
v. Connecting wires
vi. IC bread board trainer

CIRCUIT DIAGRAMS:

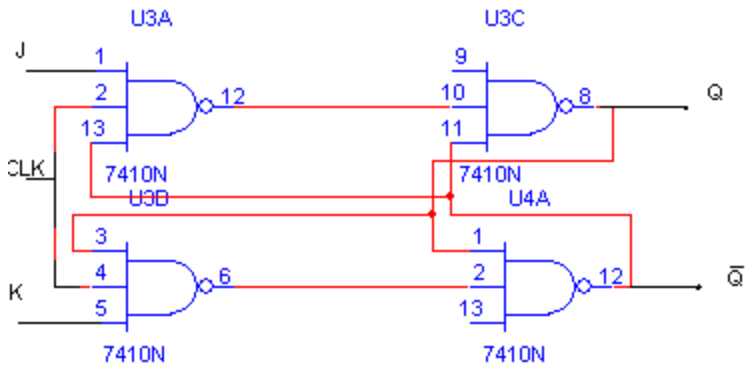
i) S-R FLIP-FLOP using NAND gate



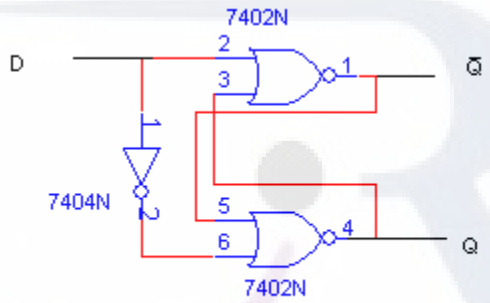
ii) S-R FLIP-FLOP using NAND gate



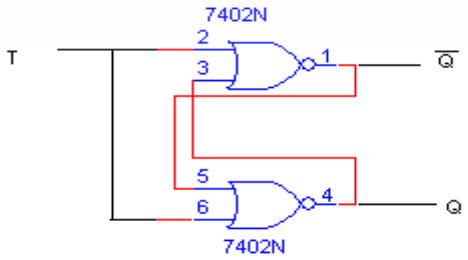
iii) J-K FLIP- FLOP



iv) D FLIP- FLOP



v) T FLIP- FLOP



TRUTH TABLES:

S-R FLIP-FLOP:

Inputs		Outputs
S	**R**	Q_{n+1}
0	**0**	Q_n
0	**1**	**0**
1	**0**	**1**
1	**1**	**Indetermine**

J-K FLIP-FLOP:

Inputs		Outputs
J	**K**	Q_{n+1}
0	**0**	Q_n
0	**1**	**0**
1	**0**	**1**
1	**1**	**NC(Q_n)**

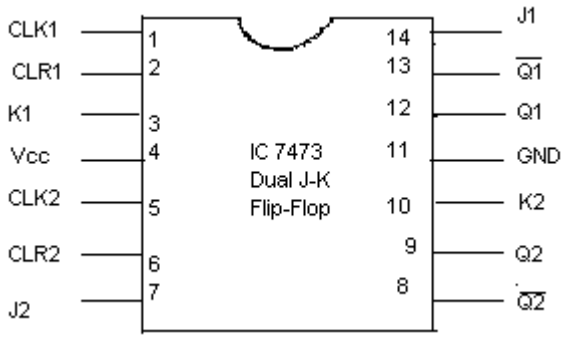
D- FLIP-FLOP:

D	Q_{n+1}	NOT(Q_{n+1})
0	**0**	**1**
1	**1**	**0**

T- FLIP-FLOP:

T	Q_{n+1}	NOT(Q_{n+1})
0	Q_n	**0**
1	$\overline{Q_n}$	**1**

PIN DIAGRAM:



THEORY:

A flip-flop can be constructed from two NAND gates or two NOR does gates.the cross coupled connection from the output of one gate to the input of the other gate constitute a feedback path. Each flip flop has two out put Q and Q ─and two inputs Set and Reset .This types of flip flop is sometimes called direct coupled flip flop or SR latch

A JK Flip flop is a refinement of the RS flip-flop in that the intermediate state of the RS type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip flop. The inputs J and K for set and the input marked k is for reset. When both inputs J and K are equal to 1, the flip-flop switches to its complement state, i.e. if Q=1, it switches to Q=0, and vice versa. A KJ flip-flop constructed with two cross neither coupled NOR gates and two AND gates.

The T- flip-flop is a single input version of the JK flip-flop. The T flip-flop is obtained from the JK Flip-flop when inputs are tied together. The designation T comes from the ability of the ability of the flip-flop to “toggle” or complement, its state.

The D flip flop has two inputs D and CP. The D input goes directly to the S input and its complement is applied to the R input. If D is 1, the output goes to 1, placing the circuit in the Set state. If D is 0, the output Q goes to 0 and the circuit switches to the clear state.

PROCEDURE:

1. The input S, R is given to NAND gates and clock pulse is applied between the other two terminals and NAND gates.
2. The input of the one NAND gate is connected to the other gate and vice versa to form SR latch.
3. The output of the NAND gate whose input is S, is connected to the input of the other NAND gate.
4. The output of the NAND gate whose input is R, is connected to the input of the other NAND gate whose output is 'Q^1'.

J K flip-flop:

1. Connections are made as per the circuit diagram.
2. The inputs J_1 and K_1 are given to the pin numbers 14 and 3 of IC 7473.
3. Clock pulse CP1 is applied at the pin 1.
4. V_{cc} and ground connections are given to the pin 4 and 11.
5. The outputs Q_1 and Q_1 bar are connected to pin 12 and 13.

D flip-flop

1. Connections are made per the circuit diagram.
2. A NOT gate is connected between the inputs J and K.
3. From JK flip flop we can obtain the D flip flop.

T flip-flop

1. Connections are made as per the circuit diagram.
2. From J K flip flop, we can obtain the T flip-flop by shorting the two inputs J and K.

RESULT:

.

6 (b) APPLICATIONS OF FLIP- FLOPS

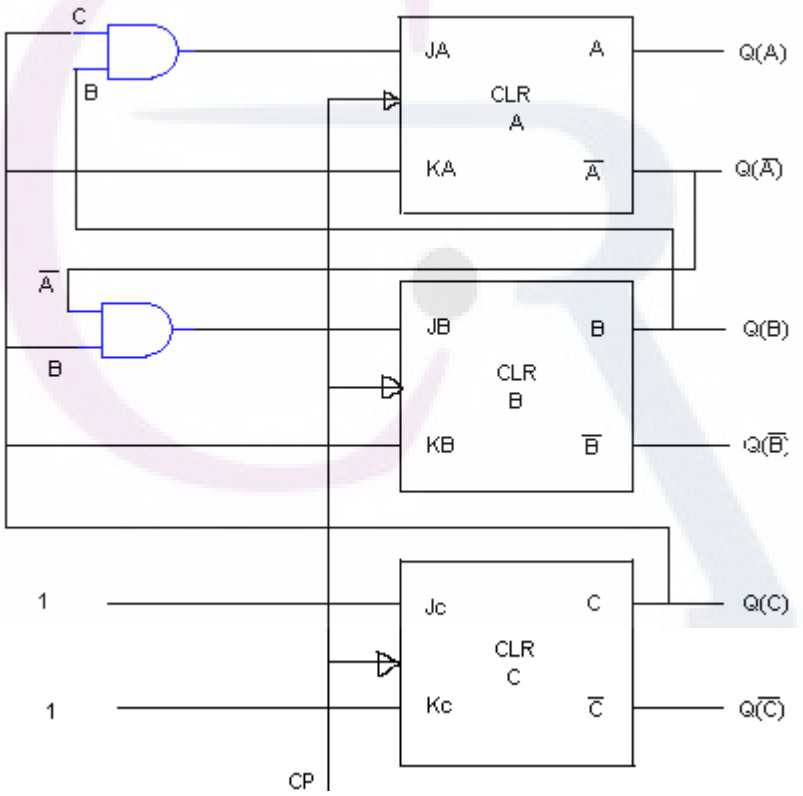
AIM:

1. Verification of truth tables for J-K flip-flop, D-flip-flop and T-flip-flop.
2. Design of Modulo-6 synchronous counter and realization using J-K flip-flop.

APPARATUS:

1. J-K flip-flop(IC 7473)
2. AND gate(IC 7408)
3. Patch cards
4. Bread board trainer
5. Connecting wires

LOGIC DIAGRAM:



THEORY:

Flip flops: A flip flop can maintain a binary state indefinitely until directed by an input signal to switch the state. The major differences among various types of flip-flops are in the no of inputs they possess and the manner in which the inputs effect the binary states. It has two states i) Actual state (set) ii) Complement state (Reset). In J-K flip-flop J is set and K is reset.

Counters: A sequential circuit that goes through a prescribed sequence of states up on the application of the input pulses is called a counter.

Application of counters are, they are used for counting the no of occurrences of an event and are useful for generating timing sequences to control operations in a digital system. An n-bit binary counter consists of n flip-flops and can count in binary from 0 to 2^n -1.

Modulus of a counter is designed as the number of states through which the counter can progress. A single flip-flop is a mod-2 counter, since a, flip-flop can progress through 2 states. But as we needmod-6 counter, 3 flip-flops are needed and logic diagram is drawn.

PROCEDURE:

1. Truth table for J-K flip-flop is determined and is verified on bread board trainer using flip-flop.
2. Outputs of mod-6 counter are determined.
3. Logic diagram is drawn.
4. Outputs are determined by applying clock pulse.

PRECAUTIONS:

1. Connections should be made carefully.
2. IC's and flip-flops should be handled carefully.

RESULT:

VIVA QUESTIONS:

1. What does meant by memory?
2. Define sequential circuits?
3. Define combinational circuits?
4. What is the difference between RS and JK flip flops

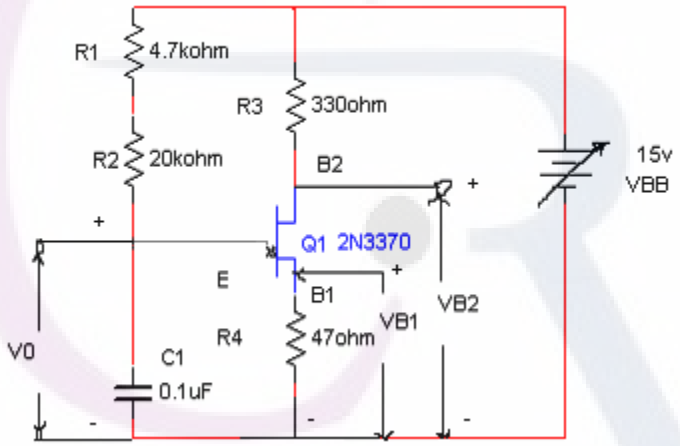
7. UJT RELAXATION OSCILLATOR

AIM: To construct and study the operation of UJT as Relaxation Oscillator.

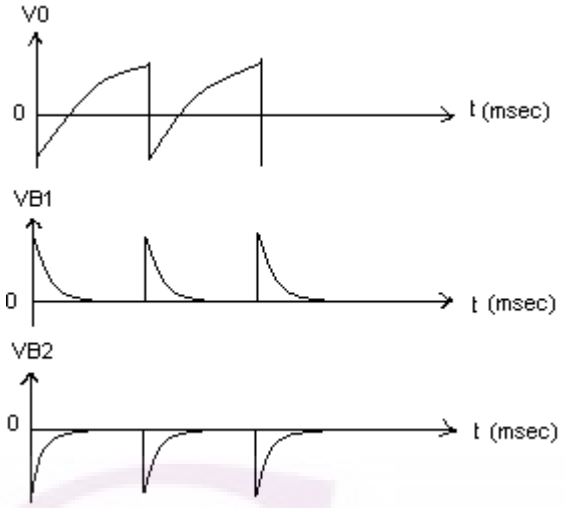
APPARATUS:

1. Bread board trainer
2. UJT 2N 2646
3. Resistors-(4.7k Ω ,47Ω,330Ω)
4. DRB
5. Capacitors-(0.1µf)
6. CRO
7. Regulated power supply(0-30V)
8. Connecting wires

CIRCUIT DIAGRAM:



MODEL WAVE FORMS:



THEORY:

The Unijunction transistor is a efficient switch, its switching time is in range of nano seconds. As UJT is exhibits Negative resistance characteristics it can be used as a relaxation Oscillator. Relaxation circuits are circuits in which the timing interval is established through the gradual charging of a capacitor, the timing interval being terminated by the sudden discharge of a capacitor. The multivibrator, the sweep generator, the blocking oscillator all these circuits have in common a timing interval and a relaxation interval and each exists in an astable or monostable form the mechanism of synchronization and frequency division is the same for all these devices.

In the pulse synchronization of a sweep generator using UJT, in the absence of an external synchronous signal, the capacitor stops charging when the capacitor voltage reaches peak or break down voltage V_p of the negative resistance device. There after, the capacitor discharges abruptly through the negative resistance device UJT. When the capacitor voltage falls to the valley voltage, the UJT goes off and the capacitor begins to recharge. A negative pulse is applied at the base B_2 of the UJT will lower V_p.

THEORITICAL CALCULATIONS:

$$T = R_T C_T \ln(1/(1-n))$$
$$n = (V_P - V_D)/V_{BB}$$

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. The Output V_o is noted, time period is also noted.
3. The theoretical time period should be calculated.
4. $T=R_TC_T \ln(1/1-n)$
5. The Output at base 1 and base 2 should note.
6. Graph should be plotted and waveforms are drawn for V_0, V_{B1},V_{B2}.

PRECAUTIONS:

1. Connections should be tight.
2. UJT terminals are identified properly.
3. Readings can not be exceeding the limits.

RESULT:

.

VIVA QUESTIONS:

1. Draw the circuit symbol of double sided diode?
2. Define intrinsic-standoff ratio?
3. Define peak voltage?
4. Define valley voltage?
5. Mention the names for negative resistances devices?

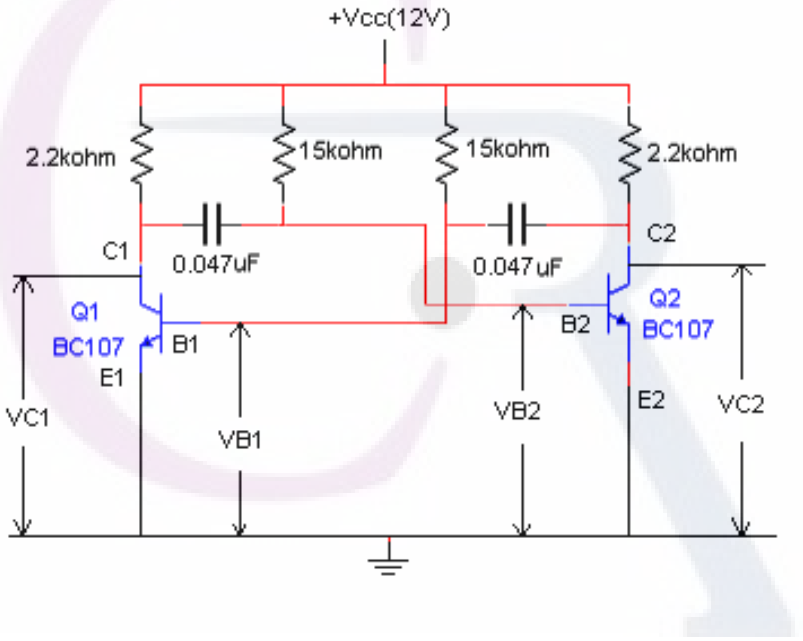
8. ASTABLE MULTIVIBRATOR

AIM: To understand the response at base and collector points of the Astable multivibrator.

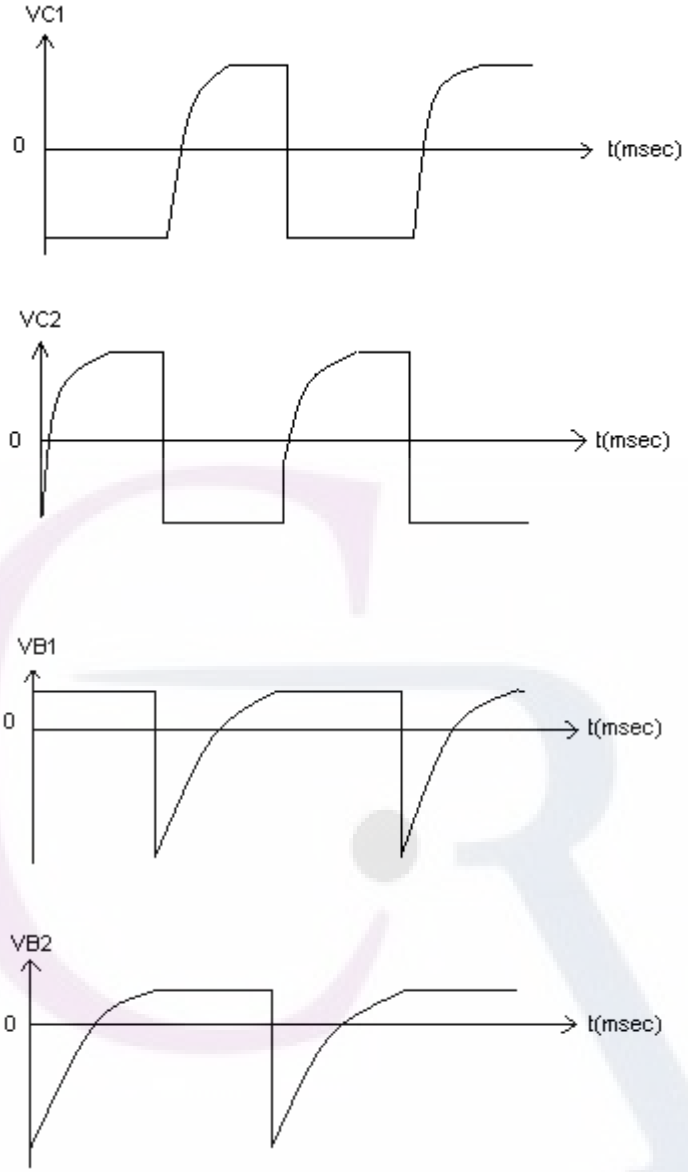
APPARATUS:

1. Function generator.
2. Resistors (2.2 kΩ, 15 kΩ) (2 no's.)
3. Capacitors (0.047 μF) (2no's.)
4. CRO
5. RPS (0-30 V)
6. Bread board
7. Connecting wires

CIRCUIT DIAGRAM:



MODEL WAVEFORMS:



THEORY:

Multivibrators are electronics circuits are used to generate waveform of type non-sinusoidal. A multivibrator have two states if these states are semi stable states it is called an astable multivibrator.

Astable multivabrator is called free running multivibrator. This vibrator changes its state from one to another on its own without any application of external trigger .The duration
Of each of the two semi stable state is dependent upon two RC times constants within the multivibrator circuit

Depending upon the β value we con conform which transistor is in ON position. Higher value of β first switched ON, here consider T2 enter into saturation and T1 is in cut-off when T2 is conducting, C2 changes to Vcc as T1 is off C2 cannot force its voltage on to the base of the T2. Base of T2 gets sufficient bias voltage to operate in saturation through Rb2. Therefore, T2 continues to conduct even though C2 is charged to Vcc. but when T2 is conducting +ve plate of the C1 is grounded though short circuited T2 . C1 is already charged to VCC thus –ve plate is connected to base of T1, which reverse biases NPN transistor and therefore T1 remains in cut-off.

Now capacitor starts charging through Rb1 and short circuited T2 from –VCC to +VCC. When charged voltage on C1 becomes 0v, the base T1 starts getting +ve potential from C1 and it enters into saturation. When T1 is short circuited as it is ON, +ve plate of the C2 is effectively grounded and its –ve plate is connected to the base of T2. Therefore T2 comes out of saturation and it becomes OFF. When T2 is OFF, C1 which is at this time charged to +ve VCC is not connected to the base of T1 and required base drive for T1 be in saturation is obtained from Rb1. Capacitor C2 which starts charging from –VCC to +VCC through Rb2 and short circuited T1. When charge on C2 becomes 0v, T2 starts conducting and therefore –ve plate of C1 is connected to the base of T1, so T1 comes out of saturation.

$$T1 = 0.69Rb1*C1$$
$$T2 = 0.69Rb2*C2$$

When Rb1 =Rb2 and C1=C2 (for square wave)

$$T = T1 + T2.$$

PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. Different voltages are measured at base and collector points of two transistors w.r.t ground as VC1, VC2, VB1 and VB2.
3. All the waveforms are plotted on the graph sheet, the amplitudes and time periods are noted down.
4. Theoretical values of amplitudes and time periods are compared with practical values.

PRECAUTIONS:

1. Connections should be tight.
2. Should take care when applying proper supply.

RESULT:

VIVA QUESTIONS:

1. Define stable state of a transistor?
2. Define semi-stable state of transistor?
3. What are the other names of Astable Multivibrator?
4. Explain the operation of a Astable Multivibrator?
5. How many stable states and semi-stable states present in the Astable Multivibrator?
6. Draw the waveforms of VC1 and VC2 of a Astable Multivibrator?
7. What is the formula for the theoretical value of T in Astable Multivibrator?

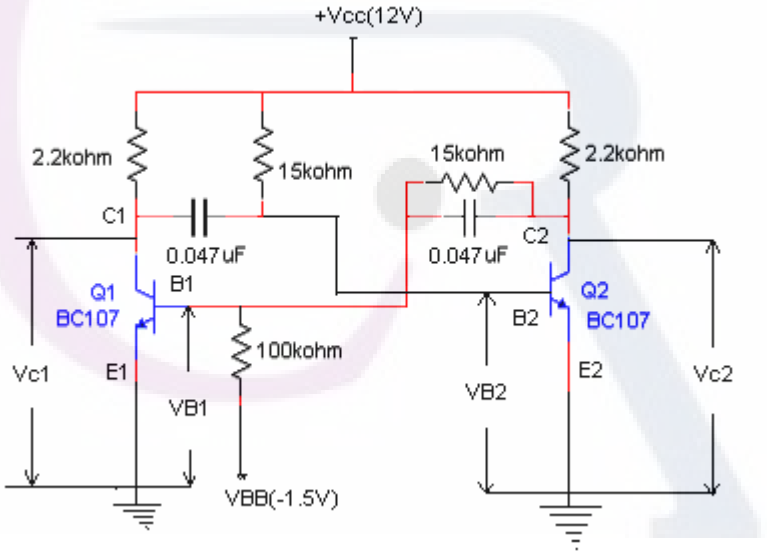
9. MONOSTABLE MULTIVIBRATOR

AIM: To construct and study the operation of monostable multivibrator using transistors and to observe the response at base and collector points of the transistors.

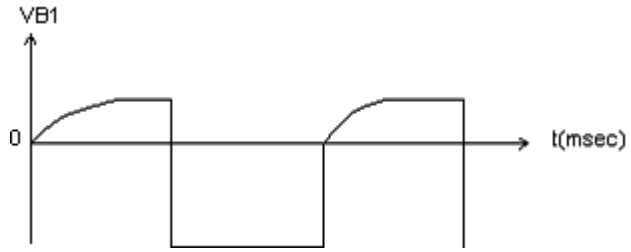
APPARATUS:

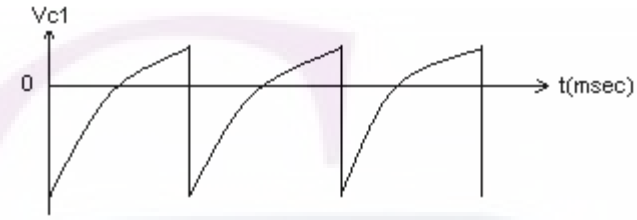
1. Transistors – BC107 (2 no's)
2. Breadboard trainers
3. Resistors 1kΩ , 10kΩ , 100kΩ
4. Capacitors 0.047μF (2 no's)
5. CRO
6. Connecting wires
7. R.P.S

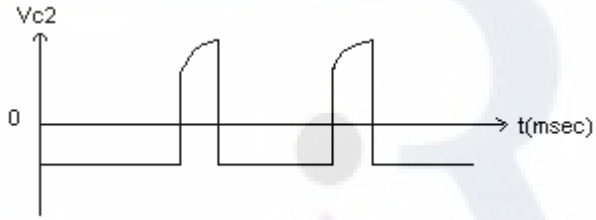
CIRCUIT DIAGRAM:

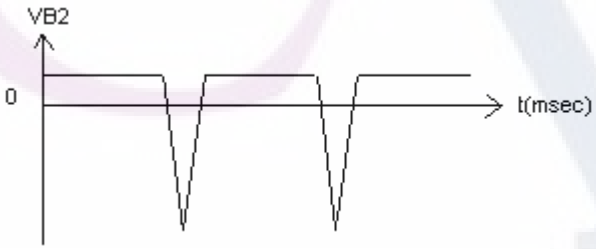


MODEL WAVEFORMS:









THEORY:

In the monostable multivibrator one state is stable and the other is semi or quasi stable state. So it is called Monostable multivibrator. It requires an external force to change from stable state to semi stable state. Where as on its own after a small duration it changes its state from semi stable state to stable state. This duration of staying in semi stable state completely depends upon timing elements resistor and capacitor with in the circuit.

When no trigger pulse is applied to the base of T2 transistor T1 is OFF and transistor T2 is ON. During this stable state of this circuit capacitor C charges through resistor R to VCC. This charging will not affect the base drive of T2 as T1 is opened and the charged voltage as T1 is open and the charged voltage V_{cc} is not w.r.t ground. Due to T2 is conducting, the collector voltage T2 is very small , which is applied through potential R1&Rb1 can not drive T1into saturation, Thus T1 remains in cut-off during stable state.

When a negative triggering pulse is applied to the base of ON transistor T2, which decreases base drive and T2 becomes OFF. Due to this collector voltage of T2 rises to VCC in turn this increases base drive of T1. Now T1 becomes ON. Due to T1 becomes short circuit, the +ve plate of charged capacitor C is effectively connected to the ground. The –ve plate is connected to the base of T2. Charged capacitor C provided the –ve voltage to the base of T2. To turn on T2 it requires a +ve drive as it is an NPN transistor.

The capacitor C starts charging from –VCC to +VCC through resistor R. When the charging on capacitor reaches '0' volts base of T2 starts getting +ve base drive and it turns ON the T2. Depending upon RC constant, circuit returns to its stable state. When T2 is ON, the collector voltage of it falls to $V_{ce(sat)}$ and there by T1becomes OFF. This stable state exists as long as again external triggering voltage is applied to the base of T2.

THEORITICAL CALCULATIONS:

$$\mathbf{T_1 = 0.69R_1C_1}$$
$$\mathbf{T_2 = 0.69R_2C_2}$$

Where $\mathbf{R_1 = R_2}$
$\mathbf{C_1 = C_2}$
$\mathbf{T = T_1 + T_2}$
$\mathbf{F = 1/T}$

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. The voltages are measured at collector and base terminals w.r.t ground by giving the VBB of –1.5v through the 100k Ω resistor and the wave forms are drawn as VC1, VC2, VB1, VB2.
3. The amplitudes and time periods of all the waveforms are noted down.

RESULT:

.

VIVA QUESTIONS:

1. What are the other names of Monostable Multivibrator?
2. How many stable and semi stable states present in the Monostable Multivibrator?
3. Explain the operation of Monostable Multivibrator?
4. What is the theoretical value of T ?
5. What is the name of base capacitor and what is the purpose of base capacitor?

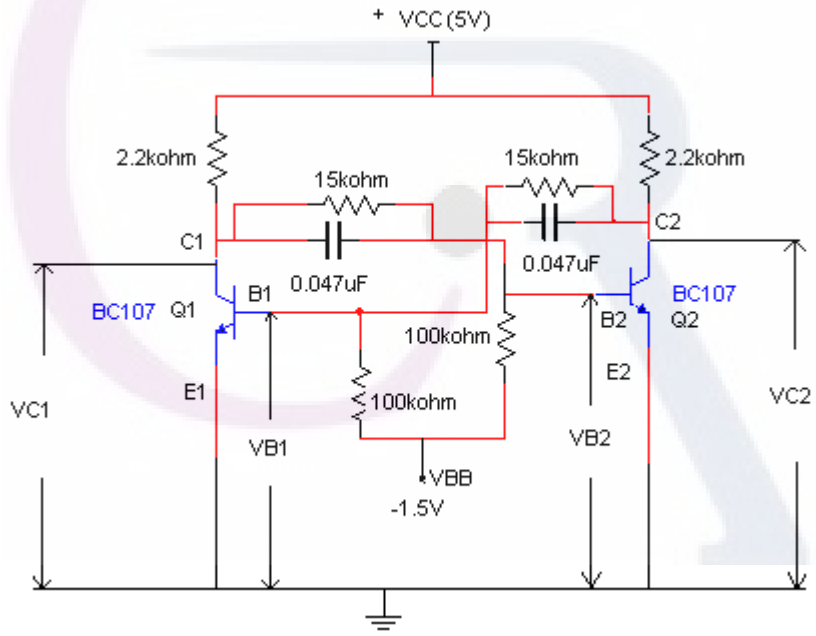
10. BISTABLE MULTIVIBRATOR

AIM: To understand the working of Bistable Multivibrator using transistors.

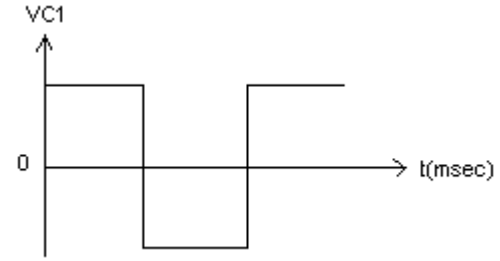
APPARATUS:

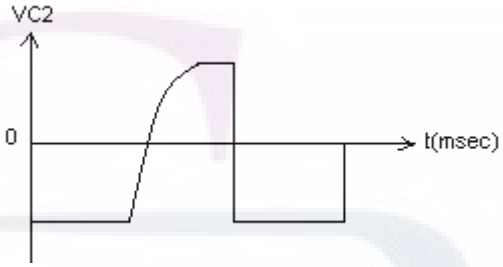
1. Transistors - BC107 (2 no's)
2. Breadboard trainer
3. Resistors (2.2 kΩ ,15 kΩ ,100 kΩ)
4. CRO
5. Capacitors - 0.047μF (2 no's)
6. Connecting wires
7. R.P.S

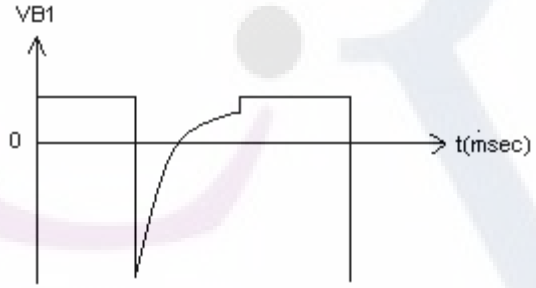
CIRCUIT DIAGRAM:

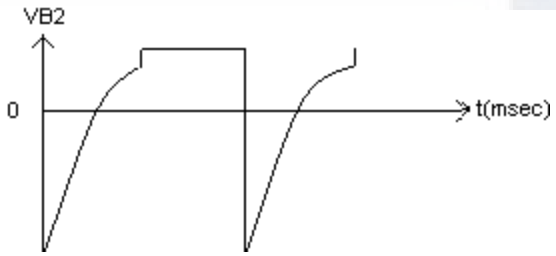


MODEL WAVEFORMS:









THEORY:

If the circuit stays at one state may be at high state or at low state until unless a disturbance comes extremely to change the state from high to low or from low to high, then we can say the state of the circuit is stable. The multivibrator in which the two states are stable is called the Bistable Multivibrator. This Multivibrator needs an external voltage to change from unstable state to another stable state.

Assume that when the circuit is switched ON the transistor T1 is switched OFF and Transistor T2 is ON in the absence of triggering pulse. When T2 is ON the collector voltage at point A is VCE (sat). The small voltage is not sufficient to drive T1 to saturation. Therefore it remains OFF. Due to T1 OFF its collector voltage at point B is coupled to VCC. This high voltage through R1 and C1 parallel combination is applied to base of T2, which is sufficient to drive T2 into saturation. For saturation emitter base junction and collector base junction must be forward biased. Here base is P-type gets greater potential than collector it is driven into saturation. This state of operation remains stable until an external pulse is applied to the base of transistor T2, so that its base drive is reduced to a voltage for it which it comes out of saturation becomes OFF, raising its collector voltage to VCC from VCE sat.

This high voltage connected to the base of T1 makes it ON from OFF and thus collector voltage VCC fall to VCE sat. This small voltage applied to base of T2 is not sufficient to drive T2, I.e., T2 will OFF and T1 will ON. This stable condition exists as long as another triggering pulse is applied. Here capacitors C1 and C2 are called speed up capacitors, which turns transistors ON and OFF quickly by supplying sufficient charge flow to the base of the transistor. The circuit consisting RB1, RB2 and -VBB is used to empty the charge flow quickly when transistor is made OFF from conduction.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Without keeping the base resistances and with base resistances measure the voltages at base and collector points of the two transistors T1 and T2 as VC1, VB1 and VC2, VB2 respectively.
3. By applying the triggering voltage of –1.5V at the base terminals measure the time period and amplitude of the waveform.
4. All the graphs are drawn on the graph sheet.

RESULT:

VIVA QUESTIONS:

1. What are the other names of Bistable Multivibrator?
2. How many stable and semi stable states present in the Bistable Multivibrator?
3. Explain the operation of Bistable Multivibrator?
4. What is the theoretical value of T?
5. What is the name of base capacitor and what is the purpose of base capacitor?

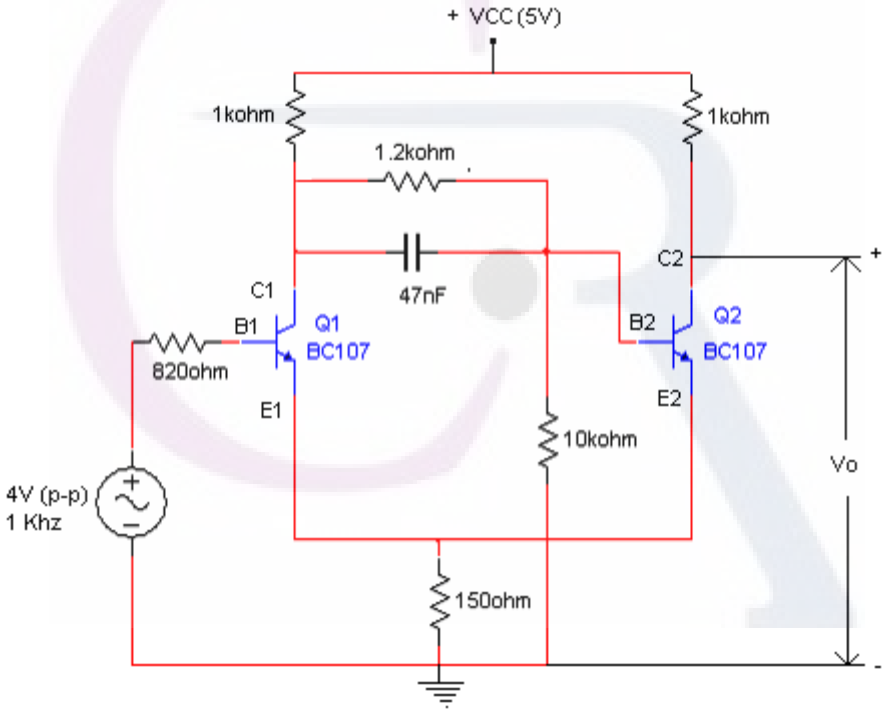
11. SCHMITT TRIGGER

AIM: To construct and study the operation of Schmitt trigger using transistors.

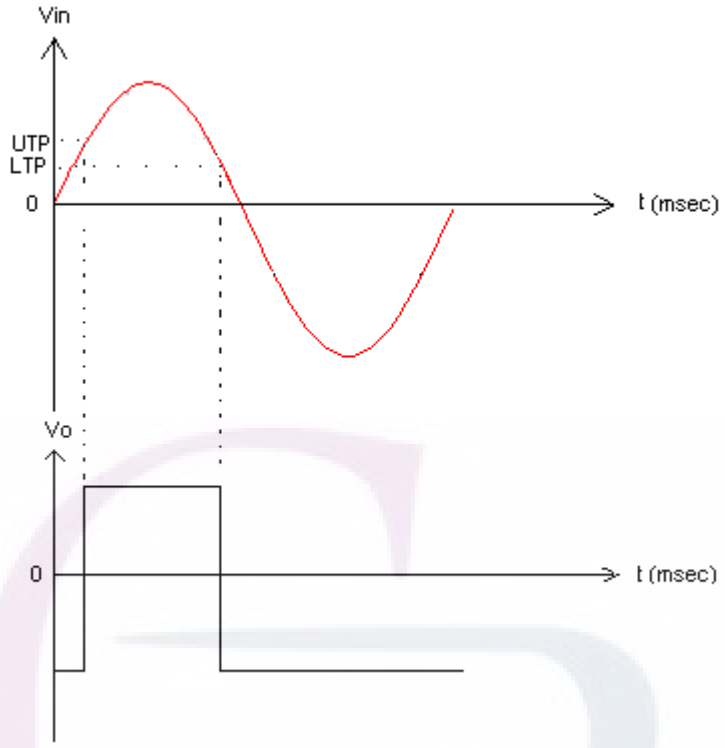
APPARATUS:

1. Breadboard trainer
2. Function generator
3. Transistors BC107 - (2 no's)
4. Resistors (820Ω, 1.2kΩ , 1kΩ (2no's), 10kΩ, 150Ω)
5. Capacitors (0.047 μF)
6. Function generator
7. CRO
8. R.P.S

CIRCUIT DIAGRAM:



MODEL WAVE FORMS:



THEORY:

Schmitt trigger is an electronic circuit which is a special form of bistable multivibrator in which one stable state to the other is changed by changing the amplitude of i/p applied voltage.

When the circuit is switched on without any i/p voltage T1 will be in cut off and T2 will be in saturation. As there is no base drive to T1 it will be off. Collector voltage of T1 will be coupled to VCC through RC1. The voltage is connected through the potential divider to the base of T2 which is sufficient to drive T2 in to saturation. Now saturation current starts flowing through the RC2, T2 and RE.

Therefore a voltage is developed across which is o/p voltage. This emitter resistance Re also connected to the emitter of T1. To drive T1, to saturation from cut-off, it required i/p voltage of voltage across Re plus VBE of T1. As the i/p voltage reaches the voltage T1 starts conducting there by its collector voltage falls and base drive to the transistor T2 is stop. Due to this the collector voltage of T2 raises to VCC which is the o/p voltage.

Voltage across Re now is due to current flow through T1. Suppose RC1 > RC2 voltage across Re due to current flow through T1 is smaller than voltage across Re due to current flow through T2. To stop conduction in T1 i/p voltage has to be reduced to lower value than to make it to conduct. Thus by increasing & decreasing the i/p amplitude one

stable state is changed to another. The greater amplitude for which T1 becomes ON from OFF is called Upper Trigger Point (UTP) , the lower amplitude for which T1 becomes OFF from ON is called Lower Trigger Point (LTP).

THEORITICAL CALCULATIONS:

$$UTP = (V_{CC}.R_E/(R_{C2}+R_E))+V_{BE1}$$

$$LTP = V_{CE\,(sat)} + V_{BE}$$

$$HYSTERISIS = UTP - LTP$$

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Fixed the i/p voltage 4v p-p at 1 KHz frequency.
3. The o/p voltage was taken at the collector point of transistor T2. w.r.t the ground applying the bias voltage 5V.
4. The magnitudes of UTP and LTP are noted. By observing waveform on CRO.

PRECAUTIONS:

1. Connections should be tight.
2. Should take care when biasing proper supply.

RESULT:

VIVA QUESTIONS:

1. Define upper trigger potential?
2. Define lower trigger potential?
3. Define hysterisis?
4. What are the other names of Schmitt trigger?
5. For any type of i/p what is the o/p of a Schmitt trigger?
6. Explain the operation of a Schmitt trigger?
7. What is the theoretical value of UTP?
8. What is the theoretical value of LTP?

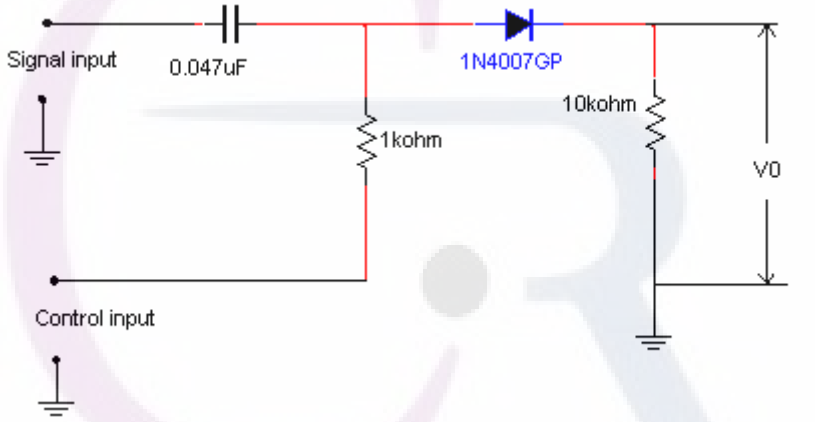
12. SAMPLING GATES

AIM: To construct and verify the response of sampling gate by using diode.

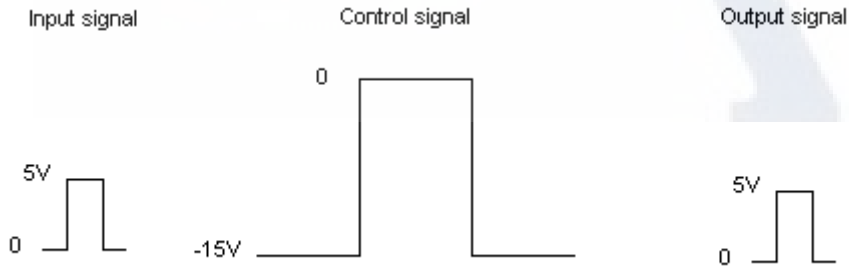
APPARATUS:

1. Function generator
2. CRO
3. Connecting wires
4. Resistors(1 KΩ, 10 KΩ)
5. Capacitor (0.047μF)
6. Diode 1N4007

CIRCUIT DIAGRAM:



MODEL WAVEFORMS:



THEORY:

An ideal sampling gate is a transmission circuit that produces an output signal identical to the input signal during a selected time interval. The output of the sampling gate is zero outside this selected time interval. The sampling gate is open during the sampling interval and it is closed at all other times. The time interval for transmission is monitored by a control input signal, which is usually rectangular in shape. In practice, the idealized transmission gate is not realized. As long as the output is produced at the correct time the performance of the practical sampling gates available is treated to be quite satisfactory.

PROCEDURE:

1. Connect the circuit as per circuit diagram
2. Applying both inputs (signal input and control input) simultaneously to the circuit.
3. Repeat the second step by varying input signal and putting the control signal fixed.
4. Note down the output waveforms for various range of input signals

PRECAUTIONS:

1. Connections should be tight.
2. Take care when applying the control signal.

RESULT:

VIVA QUESTIONS:

1. What is sampling gate?
2. Define control signal?
3. What is the other name for the control signal?
4. What is the difference between logic gates and sampling gates?
5. What is the necessity of the sampling gate?