# CHIRANJEEVI REDDY INSTITUTE OF ENGINEERING & TECHNOLOGY

**(Approved by AICTE,New Delhi & Affiliated to JNTU,ANANTAPUR)**
**Susheela Nagar, Bellary Road, ANANTAPUR.**

## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING.

## ANALOG & DIGITAL COMMUNICATIONS LAB (9A04607)

## (III B.Tech II Semester)

## LAB-MANUAL

**Head of the Department**

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**M-Tech.,**
**Assistant professor in ECE.**

**JAWAHARLAL NEHRU**
**TECHNOLOGICAL UNIVERSITY ANANTAPUR**
**Electronics and Communication Engineering**
**(9A04607) ANALOG & DIGITAL COMMUNICATIONS LAB**
**B.Tech III-II Sem. (E.C.E.) T P C**
**0 3 2**

**Minimum Twelve Experiments to be conducted: (Six from each part A & B)**

**Part A (Analog Communication Lab):**

1 Amplitude modulation and demodulation.
2 Frequency modulation and demodulation.
3 Characteristics of Mixer.
4 Pre-emphasis & de-emphasis.
5 Pulse Amplitude Modulation and demodulation.
6 Pulse Width Modulation and demodulation.
7 Pulse Position Modulation and demodulation.
8 Radio Receiver measurements – Sensitivity, Selectivity, & Fidelity.

**Part B (Digital Communication Lab):**

1 Sampling Theorem – verification.
2 Time division multiplexing.
3 Pulse Code Modulation.
4 Delta modulation.
5 Frequency shift keying - Modulation and Demodulation.
6 Phase shift keying - Modulation and Demodulation.
7 Differential phase shift keying - Modulation and Demodulation.
8 QPSK - Modulation and Demodulation.

**Equipment required for Laboratories:**

1 RPS - 0 – 30 V
2 CRO - 0 – 20 M Hz.
3 Function Generators - 0 – 1 M Hz
4 RF Generators - 0 – 1000 M Hz. /0 – 100 M Hz.
5 Multimeters
6 Lab Experimental kits for Communication
7 Components
8 Radio Receiver/TV Receiver Demo kits or Trainees

# DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
# ANALOG & DIGITAL COMMUNICATIONS LABORATORY
# LIST OF EXPERIMENTS

**Part A (Analog Communication Lab):**

1. Amplitude Modulation and Demodulation.
2. Frequency Modulation and Demodulation.
3. Characteristics of Mixer.
4. Pre-Emphasis & De-Emphasis.
5. Pulse Amplitude Modulation and Demodulation.
6. Pulse Width Modulation and Demodulation.
7. Pulse Position Modulation and demodulation.
8. Radio Receiver measurements – Sensitivity, Selectivity, & Fidelity.

**Part B (Digital Communication Lab):**

1. Sampling Theorem – verification.
2. Time division multiplexing.
3. Pulse Code Modulation.
4. Delta modulation.
5. Frequency shift keying - Modulation and Demodulation.
6. Phase shift keying - Modulation and Demodulation.
7. Differential phase shift keying - Modulation and Demodulation.
8. QPSK - Modulation and Demodulation.

## ADDITIONAL EXPERIMENTS

1. Synchronous Detector.
2. Differential Phase shift Keying.

## ADVANCED EXPERIMENTS

1. Implementing Convolutional Encoder/Decoder using MATLAB.
2. Implementing Viterbi Algorithm using MATLAB.

| EXP.NO | DATE | Experiment Name | Page No | Remarks |
|---|---|---|---|---|
| 1 | | | | |
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# 1. Amplitude Modulation & Demodulation

**Aim:** 1. To generate amplitude modulated wave and determine the percentage modulation.

2. To Demodulate the modulated wave using envelope detector.

**Apparatus Required:**

1. Amplitude Modulation and Demodulation Trainer
2. Function Generator
3. Oscilloscope
4. Connecting Wires

**Circuit Diagram For modulation:**

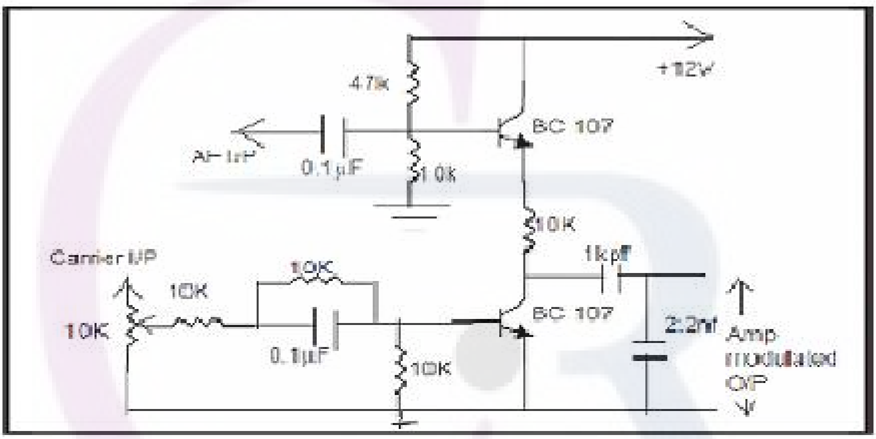


**Fig 1: CIRCUIT FOR AMPLITUDE MODULATION**

**Circuit Diagram For Demodulation:**

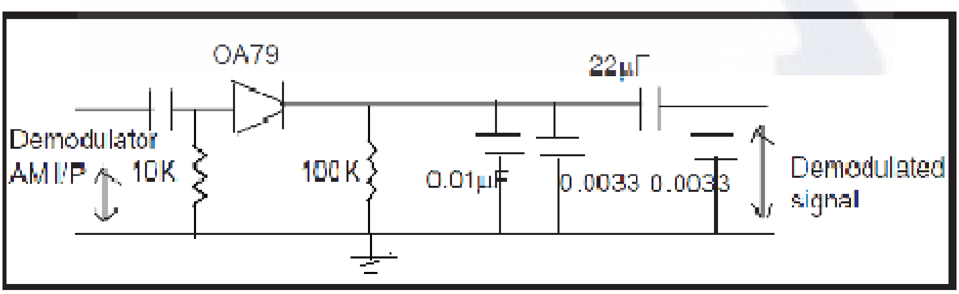


**Fig 2: CIRCUIT FOR AM DEMODULATOR**

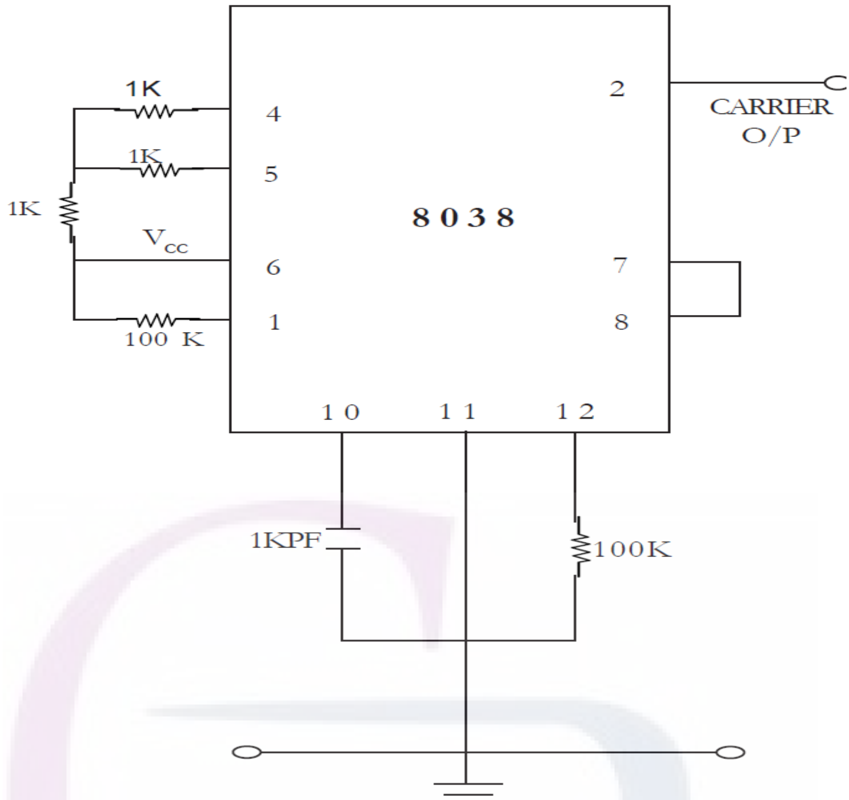


**Fig 3: Carrier Generator**

**Theory:**

Modulation is defined as the process by which some characteristics of a carrier signal is varied in accordance with a modulating signal. The base band signal is referred to as the modulating signal and the output of the modulation process is called as the modulation signal.

Amplitude modulation is defined as the process in which is the amplitude of the carrier wave is varied about a means values linearly with the base band signal. The envelope of the modulating wave has the same shape as the base band signal provided the following two requirements are satisfied

(1). the carrier frequency fc must be much greater then the highest frequency components fm of the message signal m (t)

i.e. fc >> fm

(2) The modulation index must be less than unity. if the modulation index is greater than unity, the carrier wave becomes over modulated

**Procedure:**

1 Switch on the trainer and check the O/P of carrier generator on oscilloscope.

2. Connect 1KHz with 2 Volts A.F signal at AF I/P to the modulator circuit.

3. Connect the carrier signal at carrier I/P of modulator circuit.

4. Observe the modulator output signal at AM O/P Spring by making necessary changes in A.F. signal.

5. Vary the modulating frequency and amplitude and observe the effects on the modulated waveform.

6. The depth of modulation can be varied using the variable knob (potentiometer) provided at A.F. input.

7. The percentage of modulation or modulation factor can be calculated using the following formulas.

$$\% \text{ of Modulation} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \times 100$$

$$\text{or Modulation factor} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

8. Find the value of R from $f_m=1/(2*Pi*R*C)$ , C=0.1µF

9. Connect the circuit diagram as shown in Fig.2.

10. Feed the AM wave to the demodulator circuit and observe the output

11. Note down frequency and amplitude of the demodulated output waveform.

12. Draw the demodulated wave form., m=1

**Tabular Column:**

| S. No | Modulator O/P | | | | | Demodulator O/P | |
|---|---|---|---|---|---|---|---|
| | $F_m$ (Hz) | $V_m$ (V) | $V_{max}$ (V) | $V_{min}$ (V) | m | Fo (Hz) | V0 (V) |
| | | | | | | | |
| | | | | | | | |
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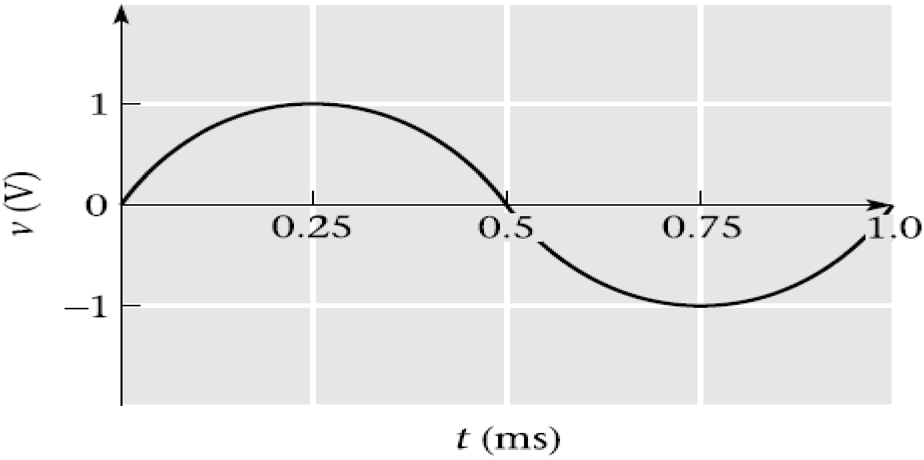
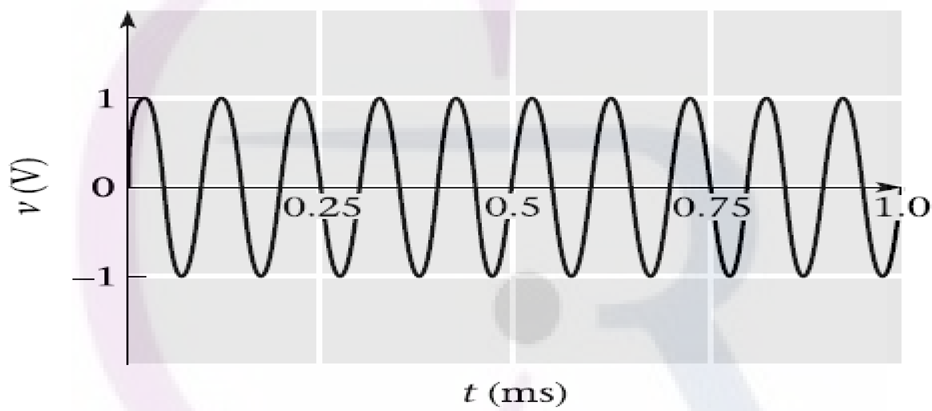
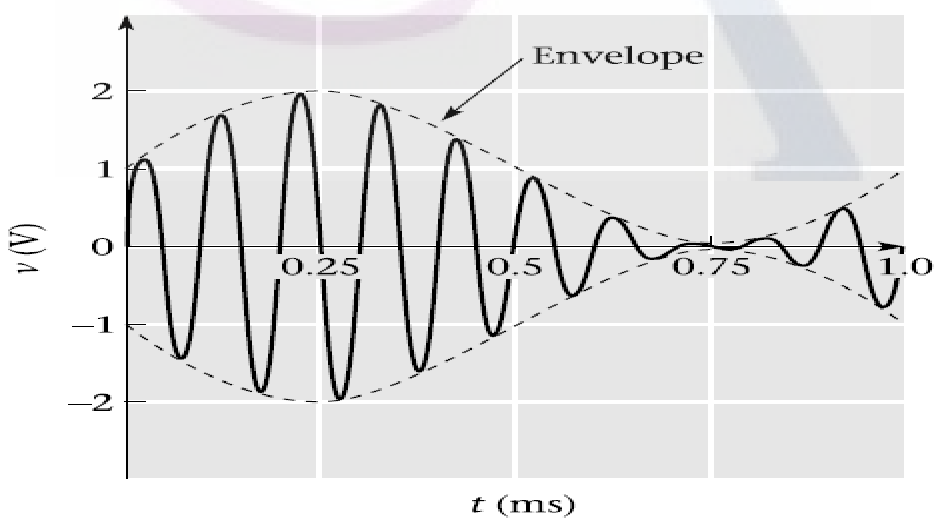



(a) $e_m$

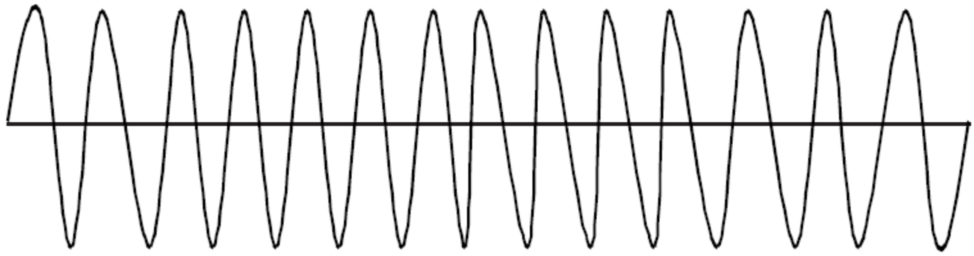



(b) $e_c$

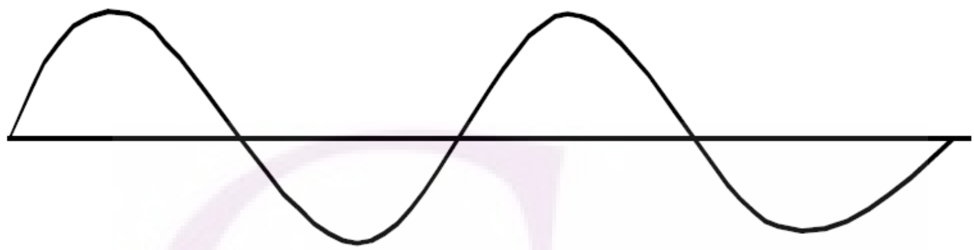



(c) 100% Amplitude modulation

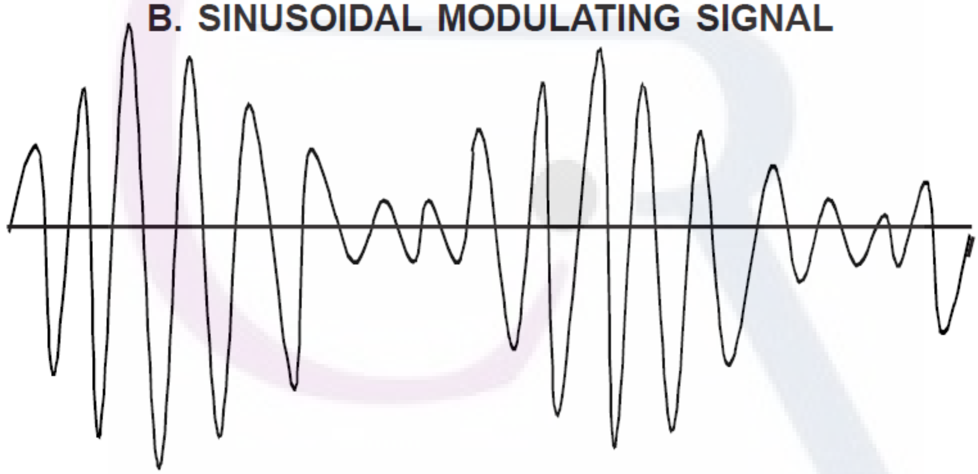
**EXPECTED WAVEFORMS**



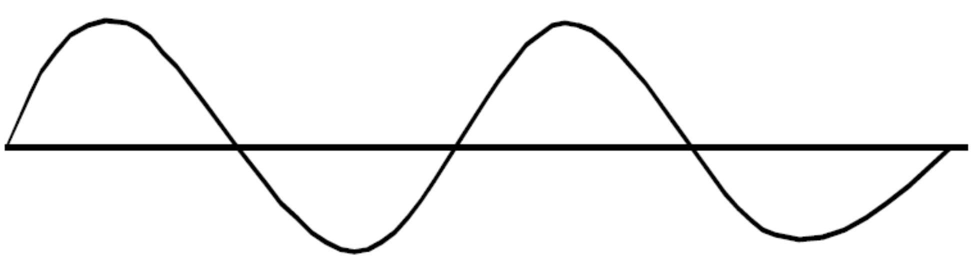
A. CARRIER WAVE



B. SINUSOIDAL MODULATING SIGNAL



C. MODULATED SIGNAL



D. DEMODULATED SIGNAL

**PRECAUTIONS:**

1. Connect the circuit as shown in the circuit diagram.
2. Apply the required voltages wherever needed.
3. Do not apply stress on the components.

## Result:

# 2. Frequency Modulation & Demodulation

**Aim:** 1. To generate frequency modulated signal and determine the modulation index and bandwidth for various values of amplitude and frequency of modulating signal.

2. To demodulate a Frequency Modulated signal using FM detector.

**Apparatus required:**

1. Amplitude Modulation and Demodulation Trainer
2. Function Generator
3. Oscilloscope
4. Connecting Wires

**Theory:**

The process, in which the frequency of the carrier is varied in accordance with the instantaneous amplitude of the modulating signal, is called “Frequency Modulation”. The FM signal is expressed as

Where $A_c$ is amplitude of the carrier signal, $f_c$ is the carrier frequency β is the modulation index of the FM wave

**Circuit Diagram:**

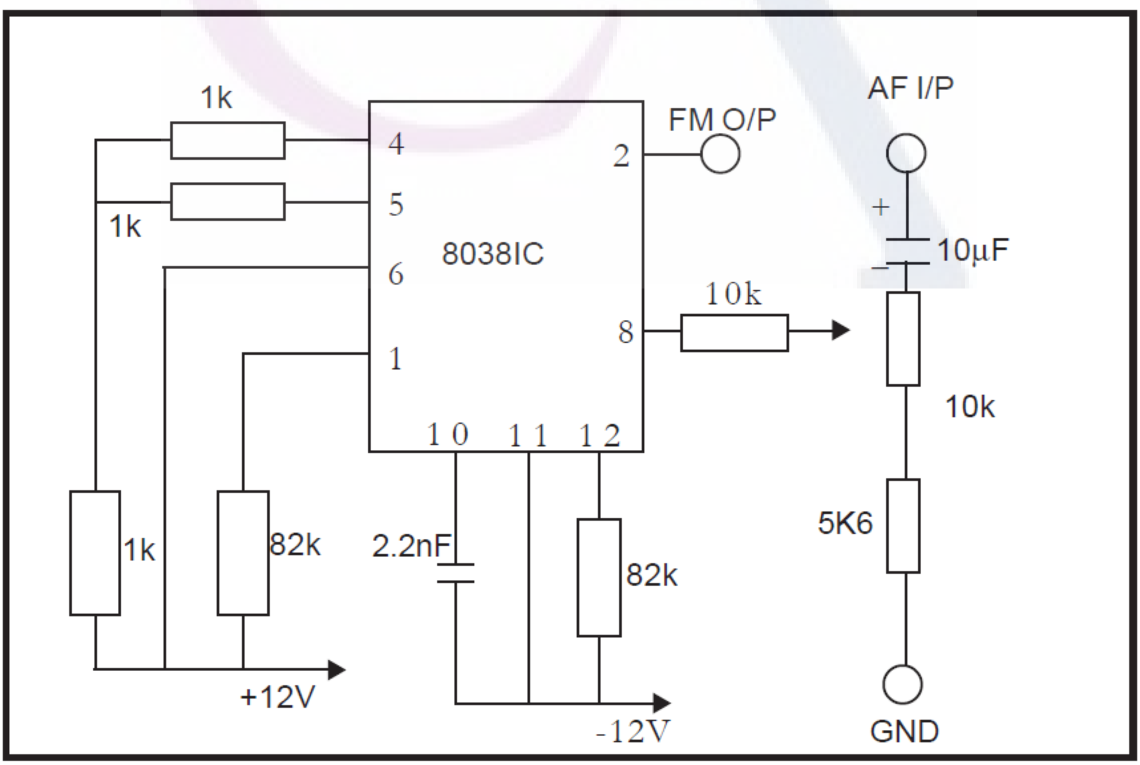


**Fig 1: Circuit Diagram for Frequency Modulator**

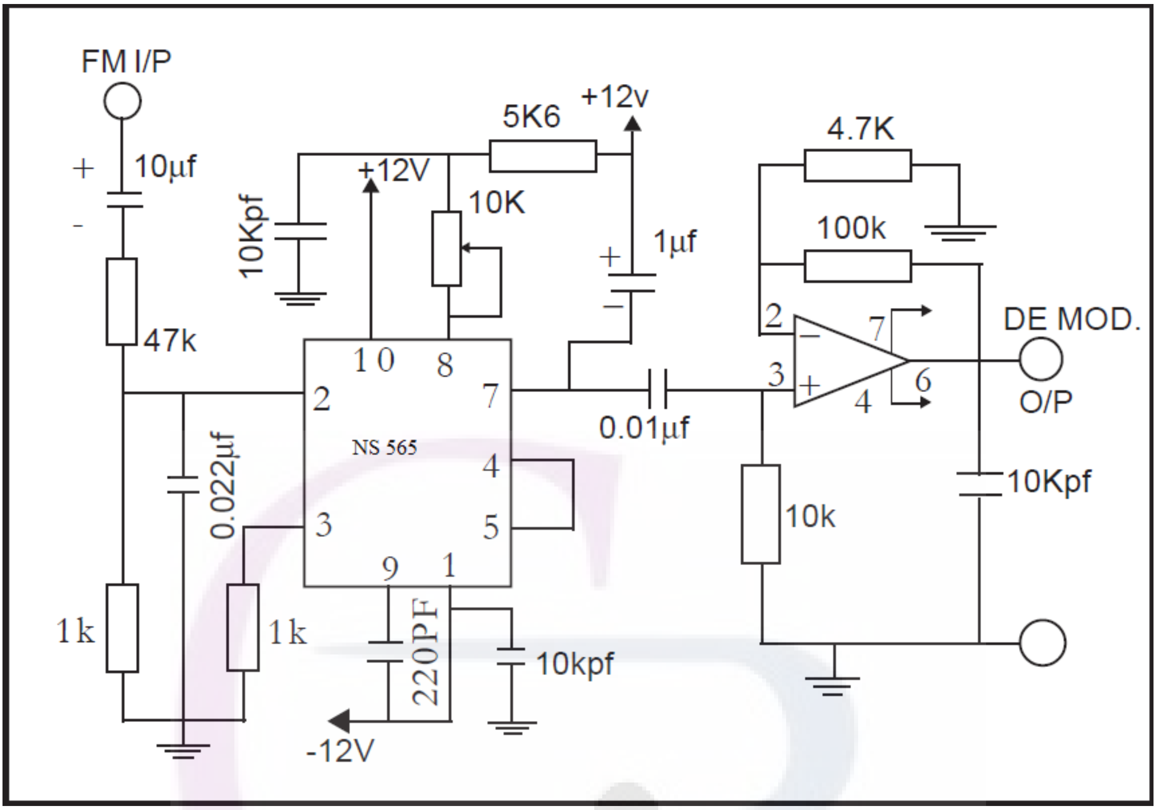



**Fig 2 : Circuit for Frequncy Demodulator**

**PROCEDURE:**

1. Switch on the FM experimental board.
2. Connect Oscilloscope to the FM O/P and observe that carrier frequency at that point without any A.F. input.
3. Connect around 7KHz sine wave (A.F. signal) to the input of the frequency modulator (At AF input).
4. Now observe the frequency modulation output on the 1st channel of on CRO and adjust the amplitude of the AF signal to get clear frequency modulated wave form.
5. Vary the modulating frequency (A.F Signal) and amplitude and observe the effects on the modulated waveform.
6. Connect the FM o/p to the FM i/p of De-modulator.
7. Vary the potentiometer provided in the demodulator section.
8. Observe the output at demodulation o/p on second channel of CRO.
9. Draw the demodulated wave form

**Tabular Column:**

**$V_c$=  , $F_c$=  ,$V_m$=**

| Sl No | $F_m$ (KHz) | $T_{max}$(µsec) | $T_{min}$(µsec) | $F_{max}$ (KHZ) | $F_{min}$ (KHZ) | Δ F (KHZ) | β | B.W (KHZ) | Demod Vo (V) |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |
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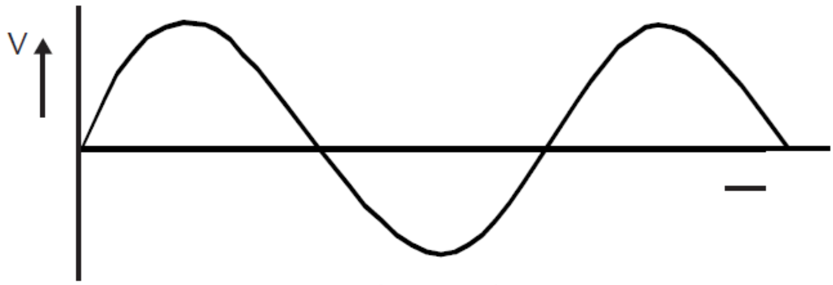
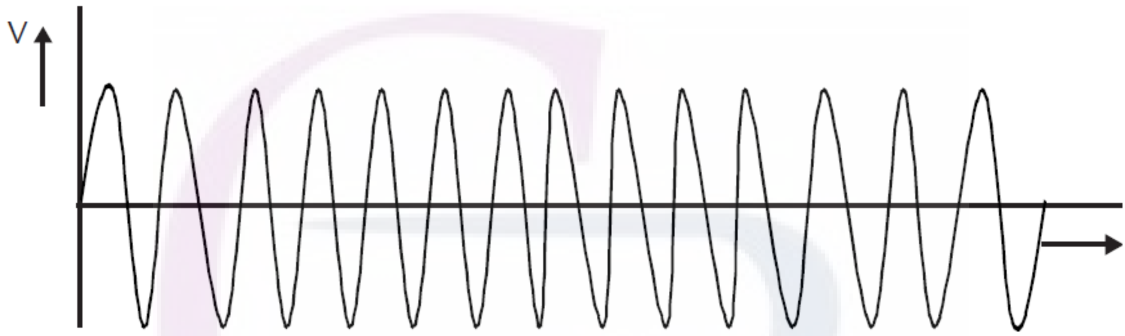
**PRECAUTIONS:**
1. Connect the circuit properly.
2. Apply the required voltages wherever needed.
3. Do not apply stress on the components.

## Result:

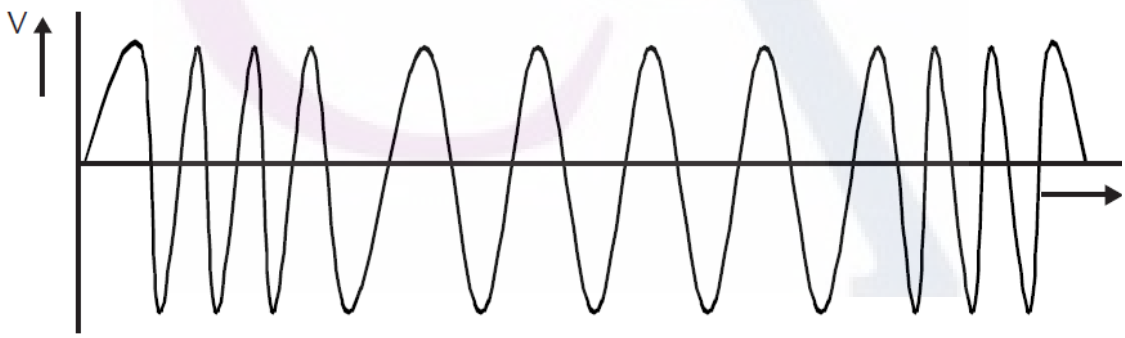
**Expected Waveforms :**



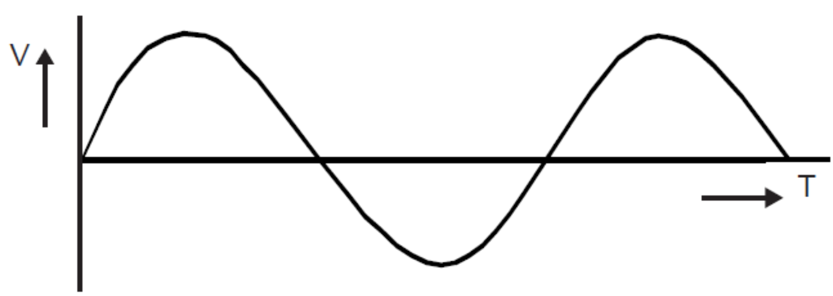

Input Modulation Signal




Carrier Wave




Frequency Modulated Signal




Demodulated signal

## 3. Characteristics of Mixer

**Aim:** To observe the characteristics of a Frequency Mixer and to measure its conversion gain..

**Apparatus Required:**

1. Frequency mixer trainer kit.
2. Function generator - (2)
3. C R O
4. B N C Probes

**Theory:**

The mixer is a nonlinear device having two sets of input terminals and one set of output terminals. Mixer will have several frequencies present in its output, including the difference between the two input frequencies and other harmonic components

**Circuit Diagram:**

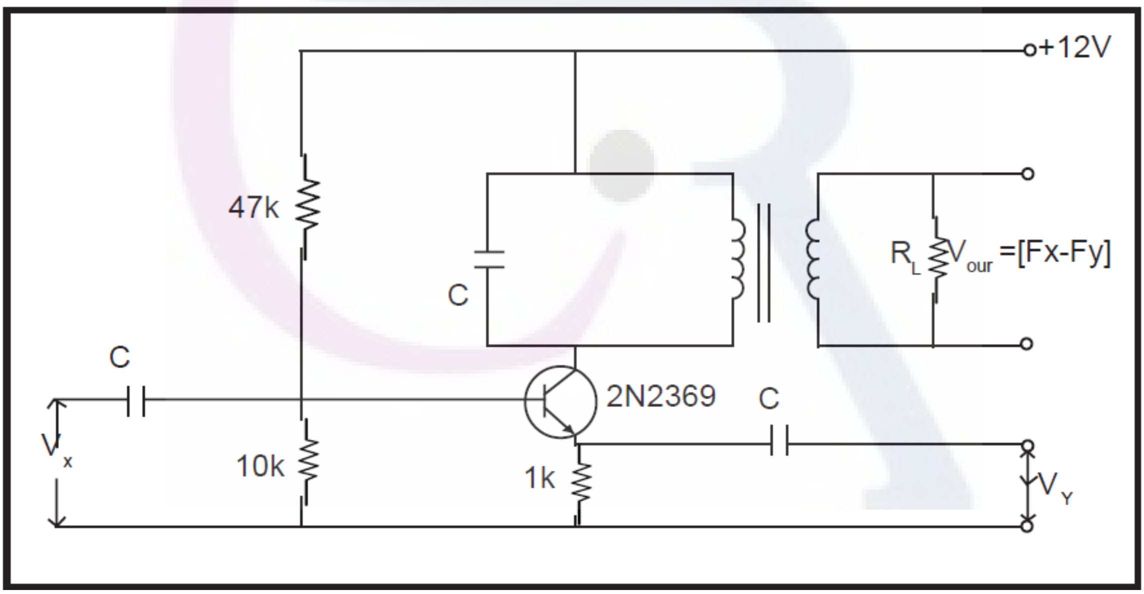



**Fig 1: Mixer Circuit Diagram**

**PROCEDURE :**

1. Connect the circuit as shown in the circuit diagram.
2. Apply 99 kHz signal to the base of the transistor and 100 kHz, signal to the emitter of the transistor.
3. Observe a sinusoidal signal with 1kHz frequency across output terminals.

4. Vary Base signal frequency and note down O/P amplitude. The output reaches to a maximum value at a particular frequency. Calculate conversion gain.

Conversion gain = (O/P Voltage)/ (Base signal voltage)

5. Plot conversion gain vs base signal frequency,

**Sample readings:**

| S.No | $F_x$ (KHz) | $F_y$ (KHz) | $V_x$ (V) | $V_y$ (V) | $F_o$ (KHz) | Output voltage(V) | Gain(dB) |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

**PRECAUTIONS:**

1. Connect the circuit properly.
2. Apply the required voltages wherever needed.
3. Do not apply stress on the components.

## Result:

## 4. Pre-Emphasis & De-Emphasis

**Aim:**

I) To observe the effects of pre-emphasis on given input signal.
ii) To observe the effects of De-emphasis on given input signal.

**Apparatus Required:**

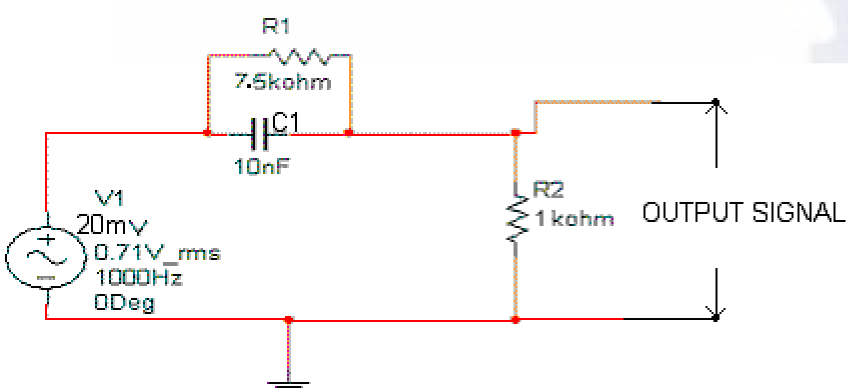
1. Resistors (10 K-2, 47K, 75K,1K)
2. Capacitors (22µF, 0.1µ-2,)
3. Transistor BC107
4 Function generators
5. CRO
6. Connecting Wires
7.RPS (15V)
8. Connecting wires.

**Theory:**

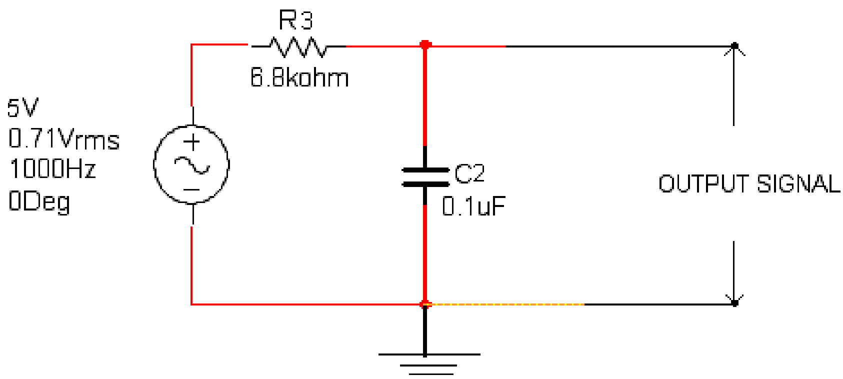
The noise has a effect on the higher modulating frequencies than on the lower ones. Thus, if the higher frequencies were artificially boosted at the transmitter and correspondingly cut at the receiver, an improvement in noise immunity could be expected, thereby increasing the SNR ratio. This boosting of the higher modulating frequencies at the transmitter is known as pre-emphasis and the compensation at the receiver is called de-emphasis

**Circuit Diagrams:**

**Pre-Emphasis:**



**De-Emphasis:**




**Procedure:**

1. Connect the circuit as per circuit diagram as shown in Fig.1.
2. Apply the sinusoidal signal of amplitude 20mV as input signal to pre emphasis circuit.
3. Then by increasing the input signal frequency from 500Hz to 20KHz, observe the output voltage
(vo) and calculate gain (20 log (vo/vi).
4. Plot the graph between gain Vs frequency.
5. Repeat above steps 2 to 4 for de-emphasis circuit (shown in Fig.2). by applying the sinusoidal signal of 5V as input signal.

**Sample readings:**

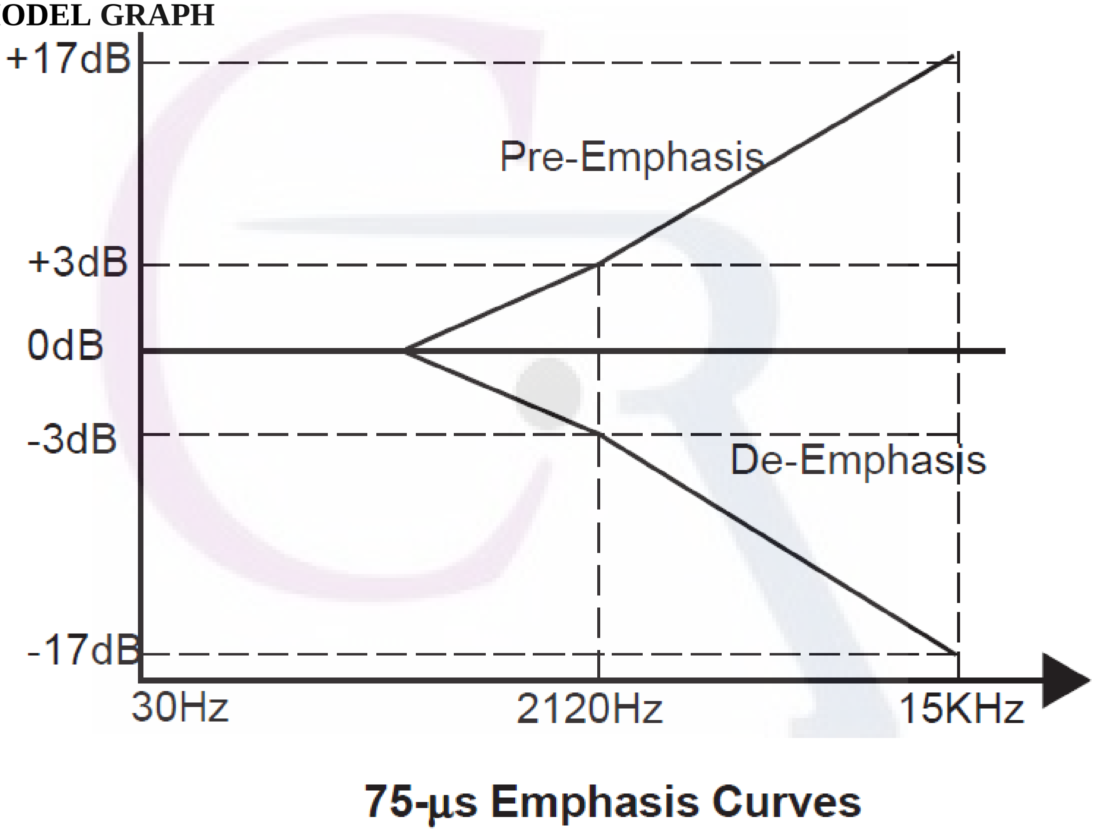
Table1: Pre-emphasis   Vi  =  20mV

| S.No | Frequency (KHz) | Output voltage (V) | Gain (dB) |
|---|---|---|---|
| 1. | | | |
| 2. | | | |
| 3. | | | |
| 4. | | | |
| 5. | | | |

Table2: de-emphasis Vi = 5V

| S.No | Frequency (KHz) | Output voltage (V) | Gain (dB) |
|---|---|---|---|
| 1. | | | |
| 2. | | | |
| 3. | | | |
| 4. | | | |
| 5. | | | |
| 6. | | | |

**MODEL GRAPH**




1

**Result:**

## 5. Pulse Amplitude and Modulation

**Aim:** To generate the Pulse Amplitude modulated signal and demodulated signals.

**Apparatus required:**

1.Pulse amplitude modulation trainer.

2. Signal generator

3. CRO

4. BNC probes, connecting wires.

**Theory:**

PAM is the simplest form of the data modulation. The amplitude of uniformly spaced pulses is varied in proportion to the corresponding sample values of a continuous message m(t).

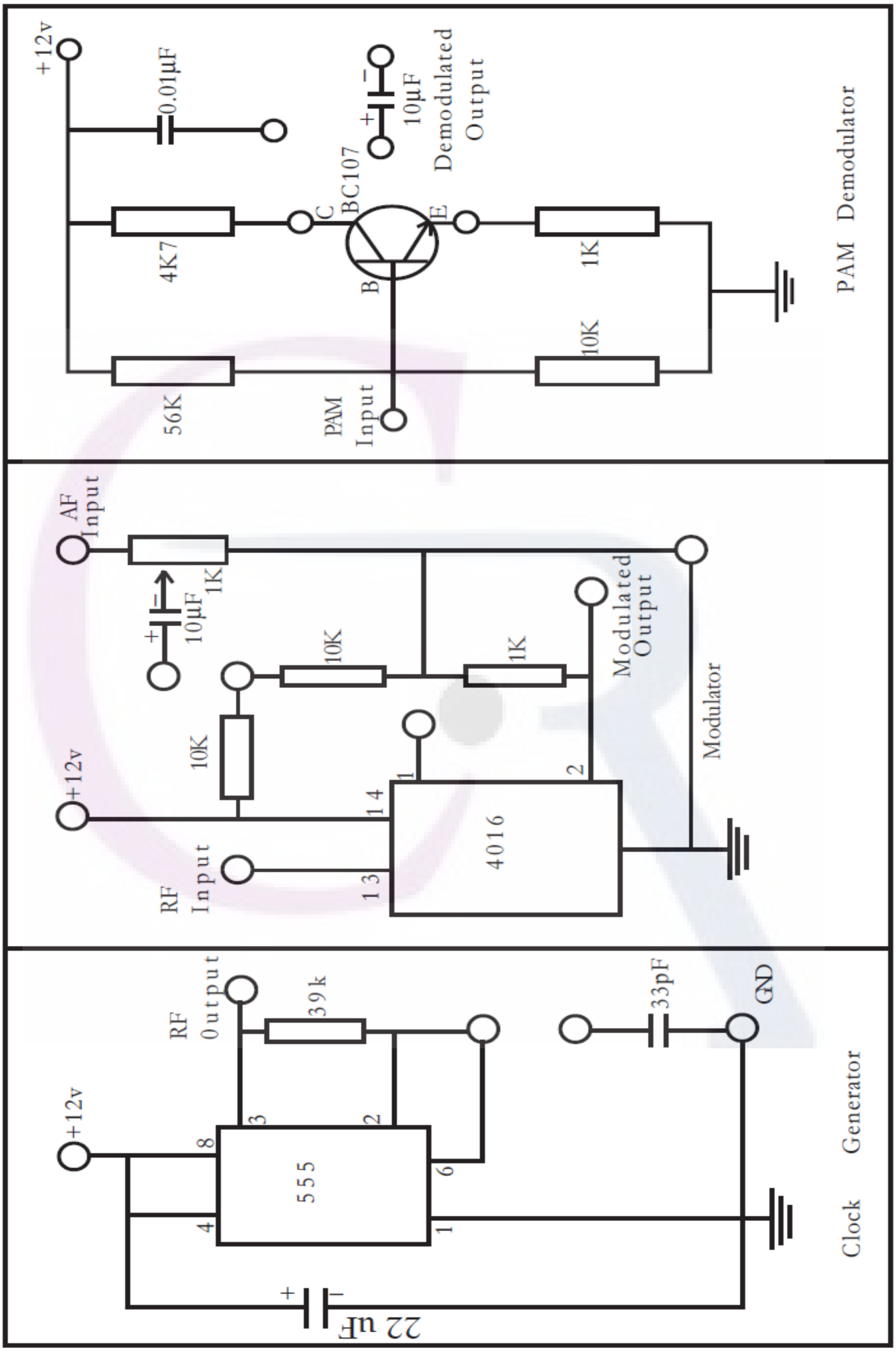
A PAM waveform consists of a sequence of list-topped pulses. The amplitude of each pulse corresponds to the value of the message signal x(t) at the leading edge of the pulse.

The pulse amplitude modulation is the process in which the amplitude of regularity spaced rectangular pulses vary with the instantaneous sample values of a continuous message signal in a one-one fashion.

PAM is of two types :

1. Double polarity PAM – This is the PAM wave which consists of both positive and negative pulses.
2. Single polarity PAM – This consists of PAM wave of only either negative or positive pulses. In this the fixed dc level added to the signal to ensure single polarity signal.

**Circuit Diagram:**




CONNECTION CIRCUIT DIAGRAM OF PAM

**Procedure:**

1 . Switch on pulse Amplitude modulation and demodulation trainer.

2 . In clock generator section connect pin 6 of 555IC to the 33pfcapacitor terminal.

3 . Check the clock generator (RF)output signal.

4 . Connect RF output of clock generator to the RF input of modulator section.

5 . Connect a 1KHz; 2vp-p of sine wave from function generator to the AF input of modulator section.

6 . Short the 10F terminal and 10k terminal of modulator.

7 . Connect 10k terminal to pin 1 of IC 4016.

8 . Connect the CRO to modulated output of modulator section.

9 . Adjust the 1k potentiometer to vary the amplitude of the modulated signal.

10. Adjust the AF signal frequency from 1KHZ-10KHZ to get stable output waveform. While increases the AF signal frequency decreases the output signal pulses.

11 During demodulation, connect the modulated output to the PAM input of Demodulator section.

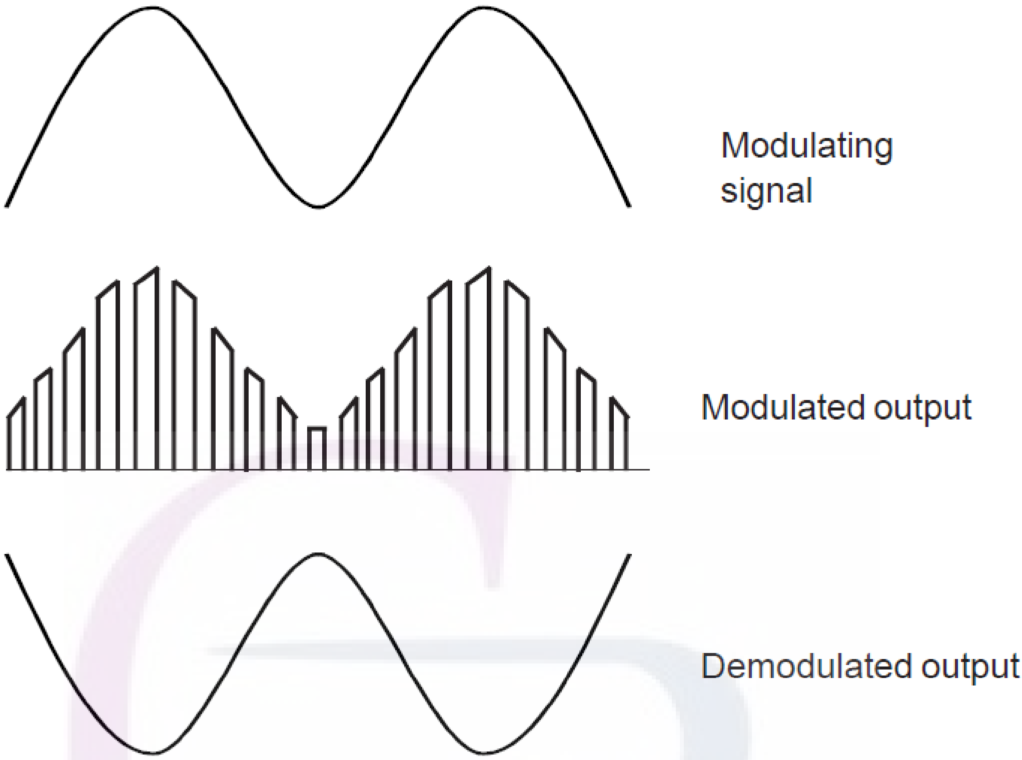
12 . Connect channel 1 of CRO to modulating signal and channel-2 to demodulated output. Observe the two waveforms that they are 1800out of phase, since the transistor detector operates in CE configuration.

**Sample Readings:**

RF frequency = RF Voltage =

| S. No | AF input voltage $V_{p\text{-}p}$ (volts) | RF Voltage $V_{p\text{-}p}$ (volts) | PAM output voltage | |
|---|---|---|---|---|
| | | | $V_{max}$ (volts) | $V_{min}$ (volts) |
| | | | | |
| | | | | |
| | | | | |

**Expected Waveforms:**




**Result:**

# 6. PULSE WIDTH MODULATION AND DEMODULATION

**Aim:** To generate the pulse width modulated and demodulated signals

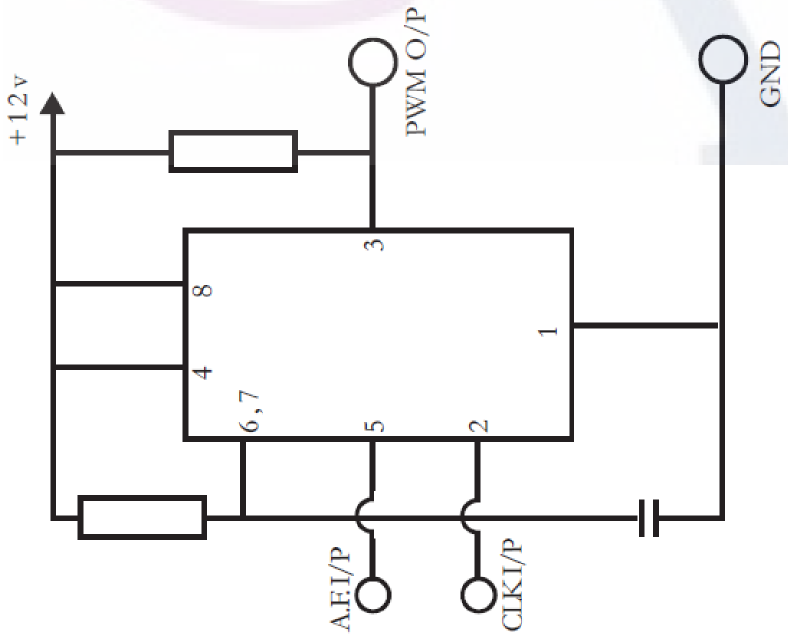
**Apparatus required:**

1. Pulse width modulation and Demodulation Trainer.
2. CRO
3. BNC probes and Connecting Wires

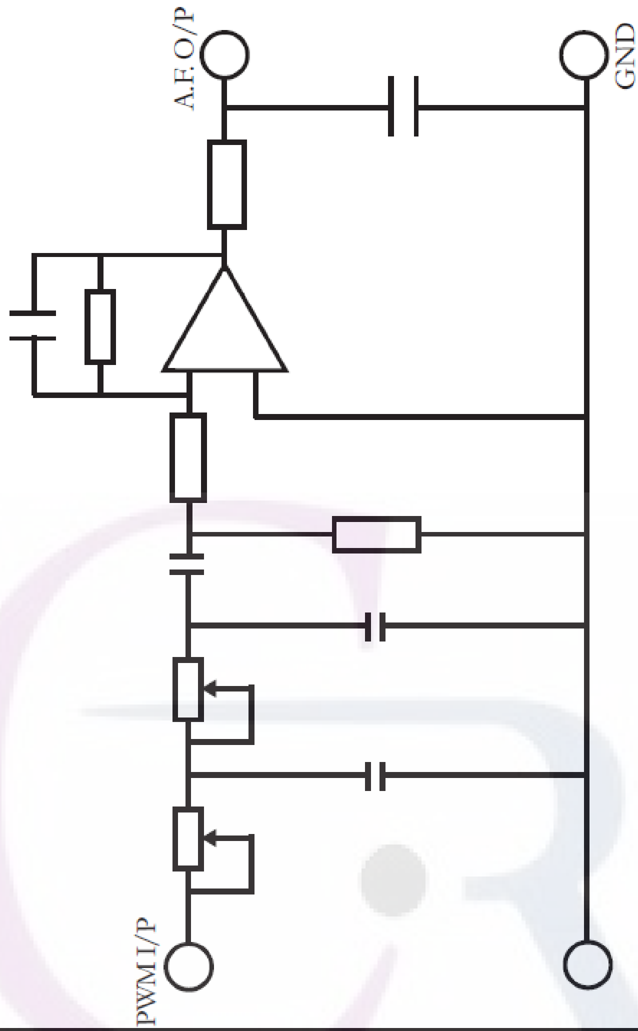
**Theory:**

In PWM, the samples of the message signal are used to vary the duration of the individual pulses. Width may be varied by varying the time of occurrence of leading edge, the trailing edge or both the edges of the pulse in accordance with modulating wave. It is also called Pulse Duration Modulation.

**PWM Modulation**




**PWM Demodulation**



**Procedure:**

1 . Switch on pulse width modulation and Demodulation trainer .

2 . Connect the Clk O/P to the clk I/P terminal of PWM modulation.

3 . Connect the AF O/P to AF I/P terminal of PWM modulation.

4 . Observe the PWM O/P at pin 3 of 555 IC on CRO.

5. By varying frequency and amplitude of the modulating signal, observe the corresponding change in the width of the output pulses.

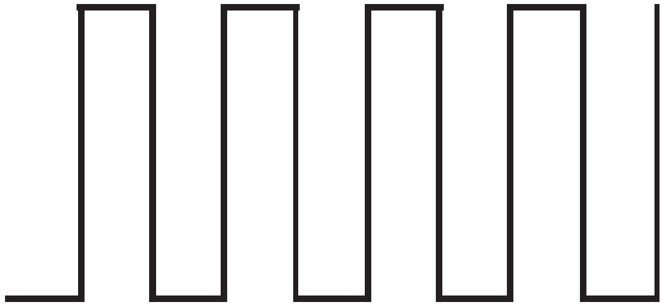
6 . During demodulation, connect the PWM O/P of PWM modulation to the PWM I/P of PWM demodulation.

7 . Observe the demodulated output at AF O/P of PWM demodulation on CRO.

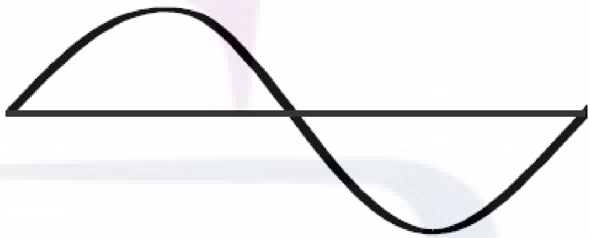
**Observations:**

| S.No | Control Voltage(V) | o/p pulse width (msec) |
|---|---|---|
| | | |
| | | |
| | | |
| | | |
| | | |

**Expected Wave forms:**

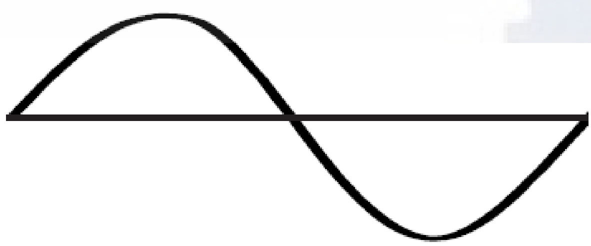


Clock Pulse



A.F.Signal

PWM O/P



Demodulated Signal

**Result:**

# 7. Pulse Position Modulation & Demodulation

**Aim:** To generate pulse position modulation and demodulation signals and to study the effect of amplitude of the modulating signal on output.

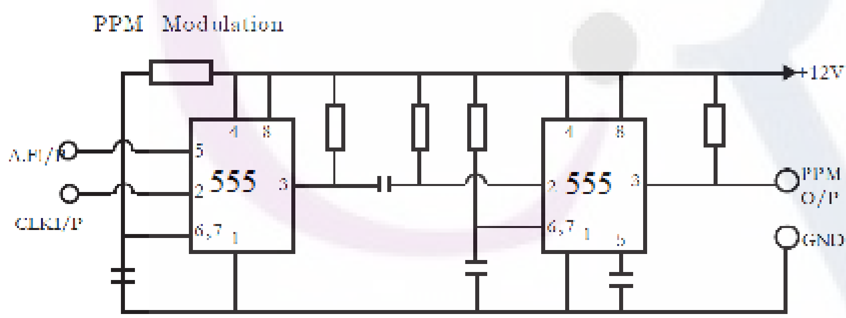
**Apparatus required:**

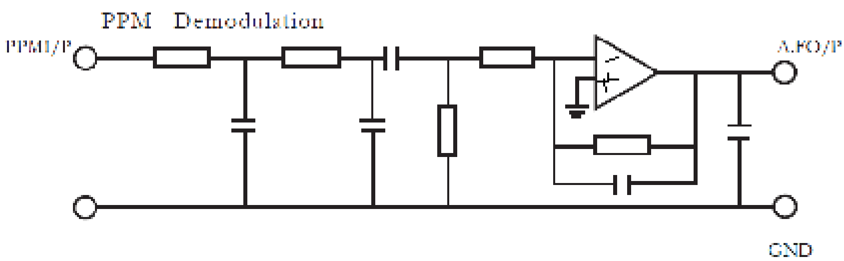
1. Pulse position modulation and demodulation trainer.
2. CRO
3. BNC probes and Connecting Wires

**Theory:**

In Pulse Position Modulation, both the pulse amplitude and pulse duration are held constant but the position of the pulse is varied in proportional to the sampled values of the message signal. Pulse time modulation is a class of signaling technique that encodes the sample values of an analog signal on to the time axis of a digital signal and it is analogous to angle modulation techniques. The two main types PTM are PWM and PPM. In PPM the analog sample value determines the position of a narrow pulse relative to the clocking time. In PPM rise time of pulse decides the channel bandwidth. It has low noise interference.

**Circuit Diagram:**



**Procedure:**

1. Switch on  PPM modulator and demodulator trainer.

2 . Connect the Clk O/P to the Pin 2 of 555 IC.

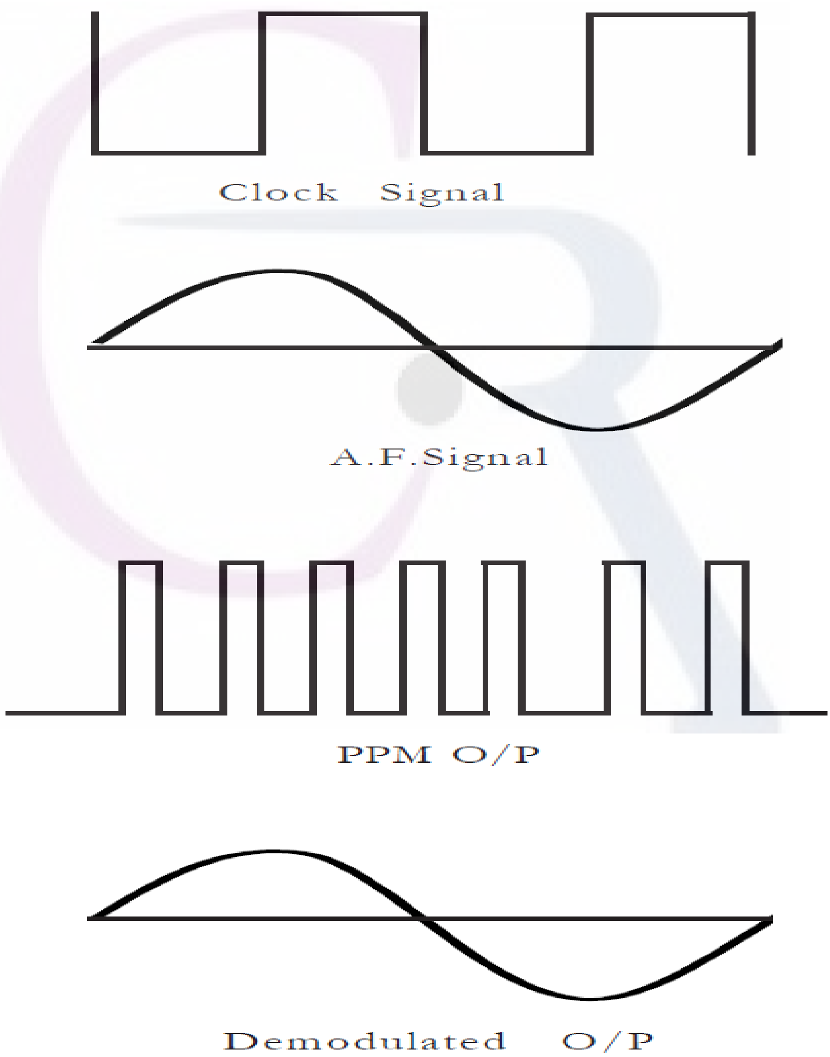
3 . Connect the AF O/P to the pin 5 of 555 IC.

4 . Observe the PPM O/P at pin 3 of second IC 555 on CRO.

5 . Connect the PPM O/P to the PPM I/P of PPM demodulation.

6. Observe the demodulated O/P on CRO**.**

**Expected Waveforms:**



**Observations:**

| Modulating Signal Amplitude (Vp-p) | Time Period (ms) | | Total Time Period(ms) |
|---|---|---|---|
| | Pulse Width ON (ms) | Pulse Width OFF (ms) | |
| | | | |
| | | | |
| | | | |

## Result:

## 8. Sampling Theorem – Verification

**Aim:** To study and verify the sampling theorem and reconstruction of sampled wave form.

**Apparatus Required:**

1. PHYSITECH's Sampling Theorem Trainer Kit
2. Function Generator
3. CRO
4. Connecting wires.
5. BNC Probes.

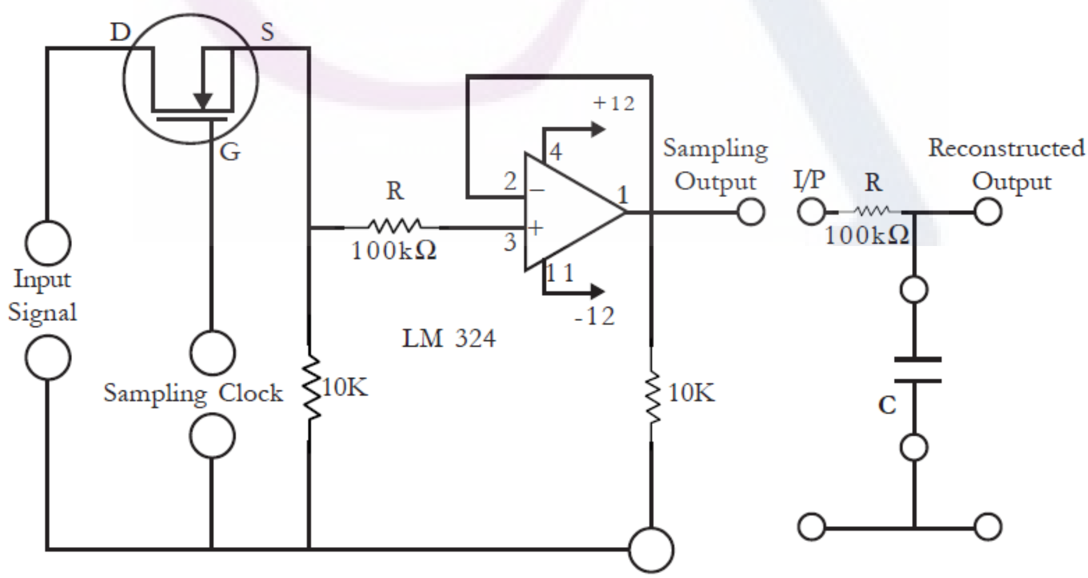
**Theory:**

The analog signal can be converted into a discrete time signal by a process called sampling. The sampling theorem for a band limited signal of a finite energy can be stated as

"A band limited signal of finite energy which has no frequency component higher than W Hz is completely described by specifying the values of the signal at instants of time separated by 1/2W seconds".

It can be recovered from the knowledge of the samples taken at the rate of 2W per second.

**Circuit Diagram:**




Circuit Diagram for Verfication of Sampling Theorem

**Procedure:**

1 . Connections are made as per the Circuit diagram.

2 . Apply the input signal with a frequency of 500Hz (VP-P) using a function generator.

3 . Sampling clock frequency which is variable of 3KHz to 50KHz should be connected across the terminals which is indicated.

4 . Now observe the sampling output of the circuit at the o/p.

5 . By using the capacitors provided on the trainer, reconstruct the signal and verify it with the given input.

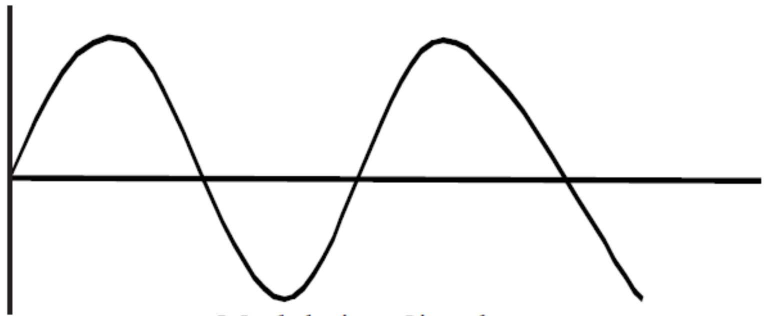
6 . Reconstructed signal voltage will be depends on capacitor value.

7 . Vary the sampling frequency and study the change in reconstructed signal.

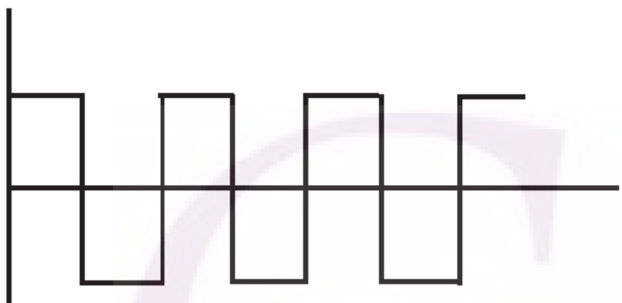
8 . If the sampling clock frequency is below 20KHz you will observe the distorted demodulated output.

**Observations:**

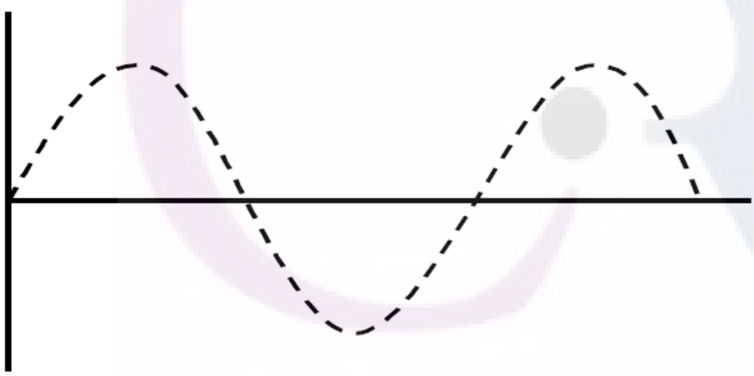
| S. No | Cases | Message signal frequency ($f_m$ KHz) | Smpling frequency ($f_s$ KHz) | Inference |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |



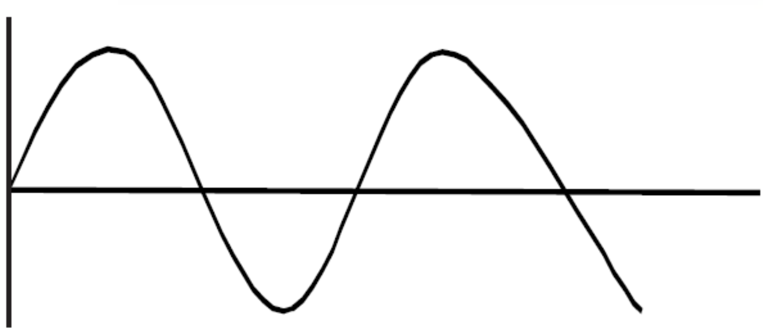
Modulating Signal



Sampling Clock



Sampling Output



Demodulating Signal

**Result:**

# 9 DELTA MODULATION & DEMODULATION

**Aim:** To study the Delta modulation process by comparing the present signal with the previous signal of the given modulating signal.

**APPARATUS:**

1. Delta Modulation trainer
2. CRO
3. Connecting wires.

**Theory:**

DM uses a single bit PCM code to achieve to achieve digital transmission of analog signal. With conventional PCM each code is binary representation of both sign and magnitude of a particular sample. With DM, rather than transmitting a coded representation of a sample a single bit is transmitted, which indicates whether the sample is smaller or larger than the previous sample. The algorithm for a delta modulation system is a simple one. If the current sample is smaller than the previous sample then logic 0 is transmitted or logic 1 is transmitted if the current sample is larger than the previous sample. The input analog is sampled and converted to a PAM signal followed by comparing it with the output of the DAC. The output of the DAC is equal to the regenerated magnitude of the previous sample which was stored in the up/down counter as a binary number. The up/down counter is incremented or decremented whether the previous sample is larger or smaller than the current sample. The up/down counter is clocked at a rate equal to the sample rate. So, the up/down counter is updated after each comparison.

**Procedure:**

1. Switch on the experimental board
2. Connect the clock signal of Bit clock generator to the bit clock input of Delta modulator circuit.
3. Connect modulating signal of the modulating signal generator to the modulating signal input of the Delta modulator.
4. Observe the modulating signal on Channel 1 of CRO
5. Observe the Delta modulator output on channel 2 of CRO
6. Connect the DM o/p of modulator to the DM I/P of Demodulator circuit.

7. Connect the clock signal to the Bit clock I/P of Demodulator circuit.
8. Observe the demodulated o/p on channel 2 of CRO.
9. Connect the demodulated o/p to the filter input of demodulator circuit.
10. Observe the demodulated o/p with filter on CRO.

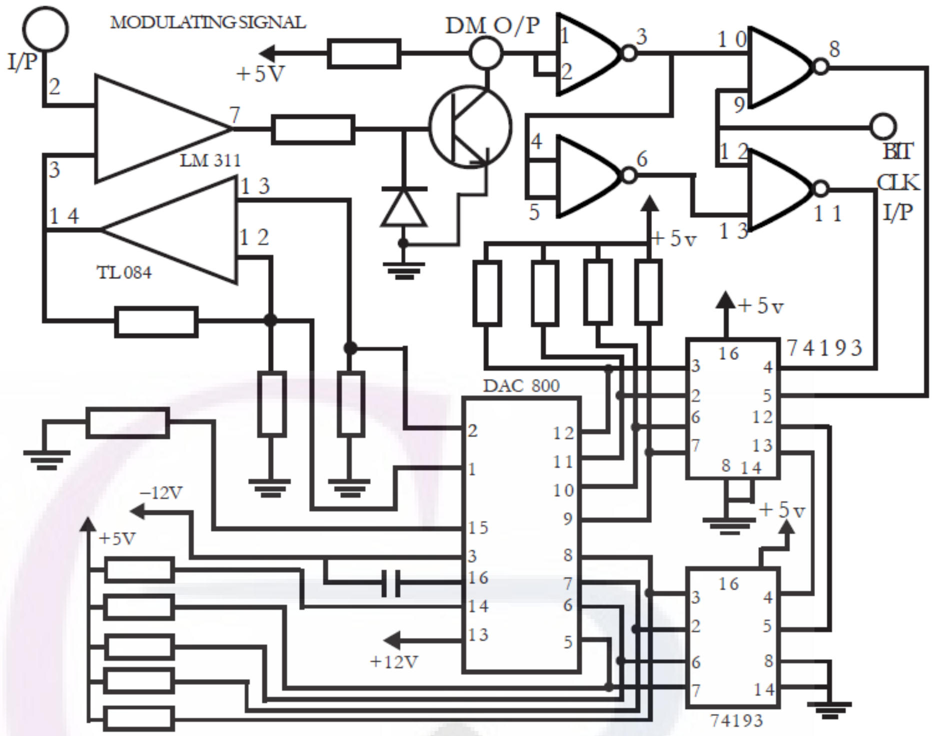
**Observations:**

| S. No | Waves | Amplitude(volts $v_{p-p}$) | Frequency ( Hz) |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

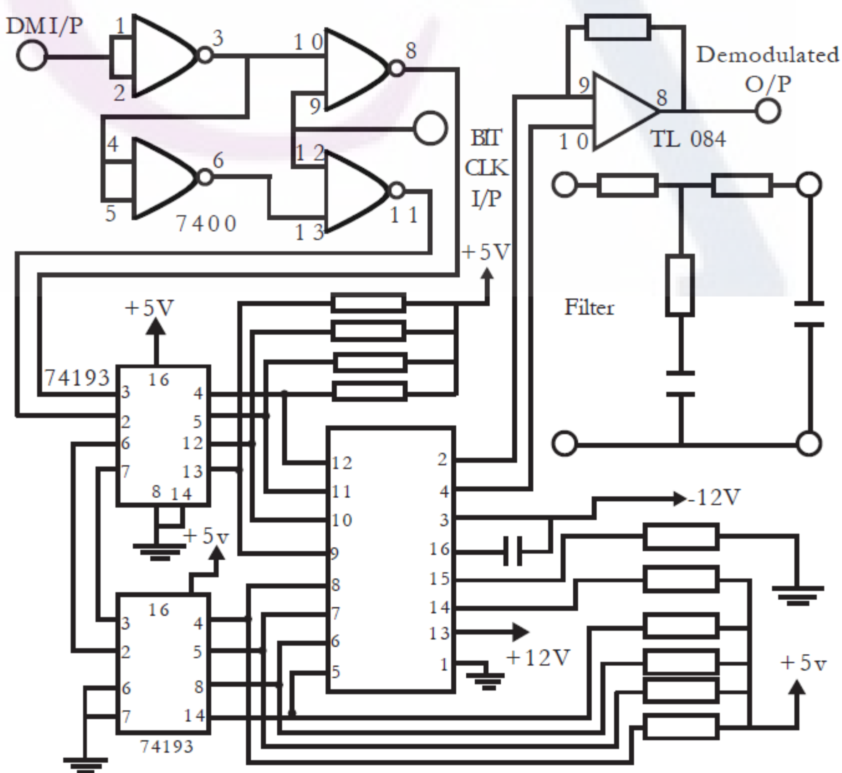
# Delta Modulation & Demodulation

**Circuit Diagram :**

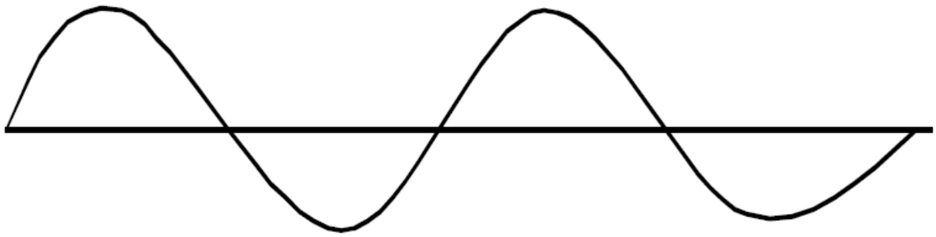
## Modulator



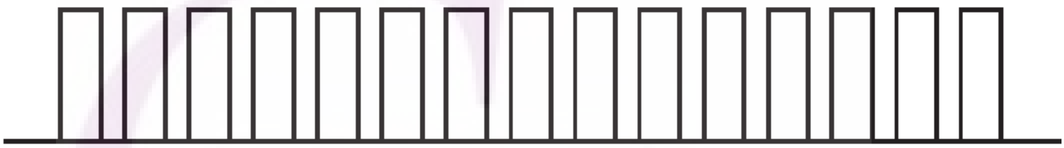

## Demodulator



## Expected Waveforms:

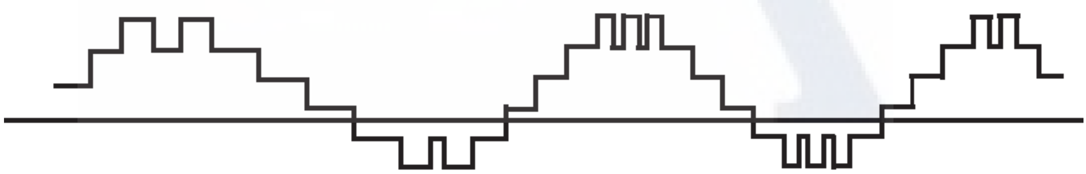


Modulating Signal I/P

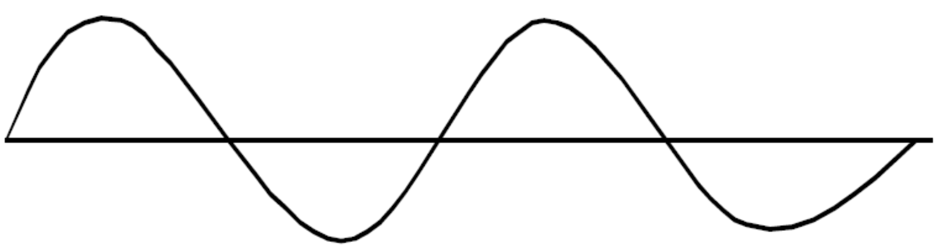


Clock I/P

Delta Modulator O/P



D/A Output



Filtered Output

**Result:**

# 10. FREQUENCY SHIFT KEYING

**Aim**: To study frequency shift key (FSK) Modulator and Demodulator

**Apparatus :**

1 . FSK Modulator-FSK Demodulator.

2 . Function Generator.

3. CRO.

4 . BNC Probes.

**Theory:**

In this method, the binary signal u (t) is used to generate a waveform.

$$V_{FSK}(t) = A \cos(W_o \pm U)\, t$$

The pulse sign is applied when v (t) = +V and minus sign is applied when V (t) =- V. Thus the frequency of transmitted signal is high for 1 and low for a 0. A straight forward way to detect an FSK signal is to use a suitable filter of sharp cut-off.

**PROCEDURE :**

1 . Connect the output of the carrier o/p provided on kit to the input of carrier i/p1 terminal.

2 .Also connect one of the data output to the data input terminal provided on kit.

3. connect sin wave of certain frequency to the carrier i/p2 terminal.

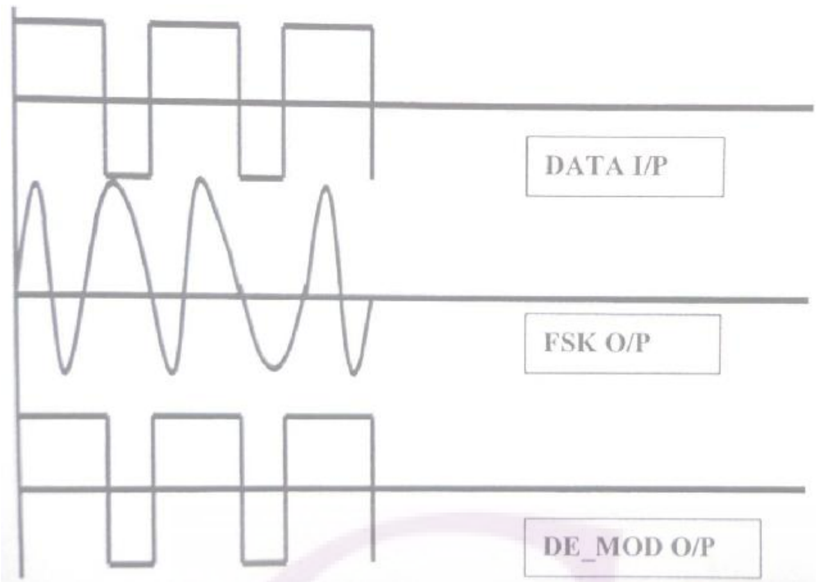
4. switch ON function generator and FSK modulation and demodulation Kit.

5. Observe the FSK o/p by connecting it to CRO. Thus FSK modulation can be achieved.

6.For FSK demodulation, connect FSK o/p terminal to the FSK i/p terminal of demodulator.

7.Observe the demodulated wave at demodulated o/p terminal by connecting it to CRO.

**Model Waveforms:**



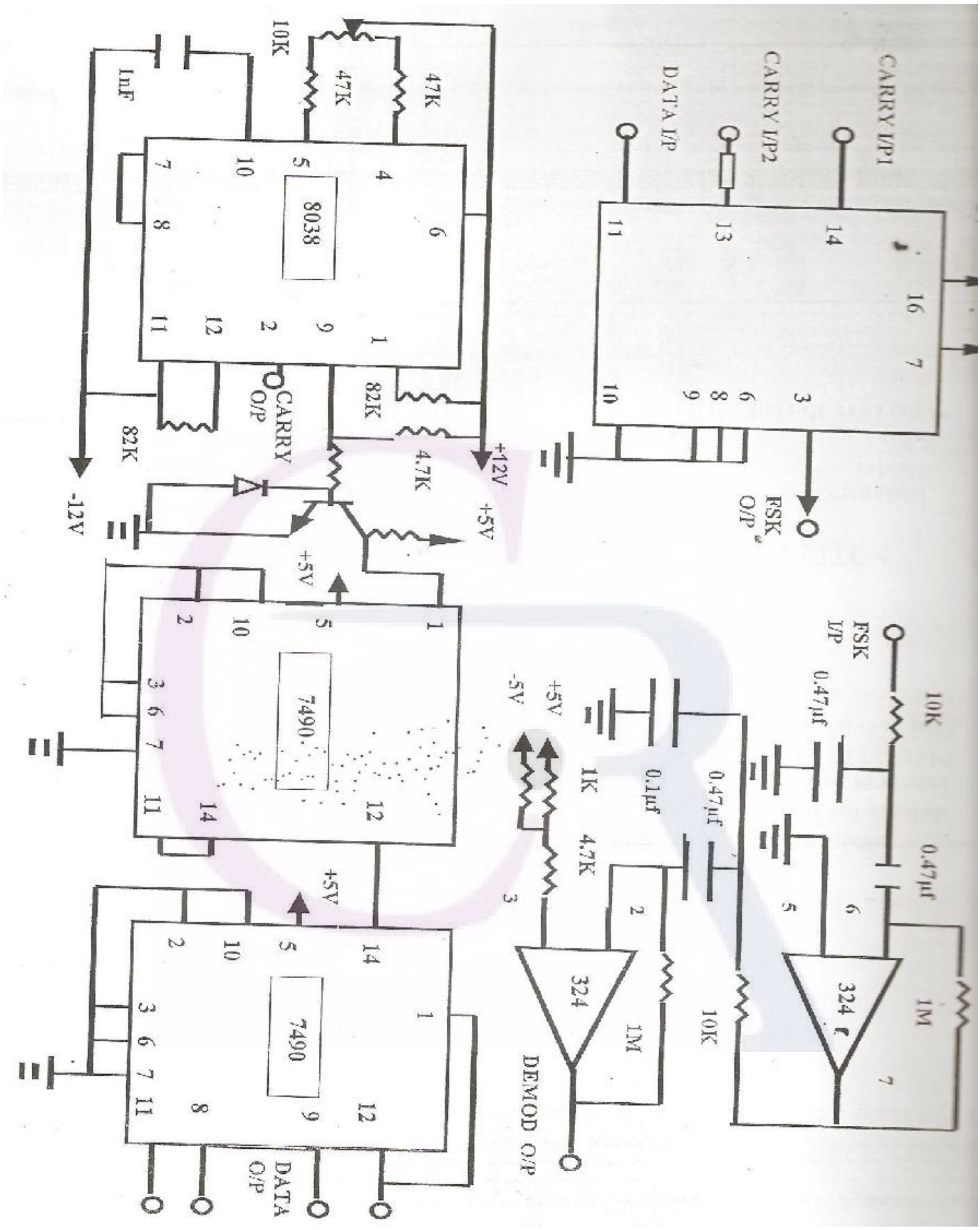

**Observations:**

**Data input:**

| Waves | Amplitude V(volts) | Duration of Bits (micro seconds) | |
|---|---|---|---|
| | | Bit 1 | Bit0 |
| Data input-1 | | | |
| Data input-2 | | | |
| Data input-3 | | | |
| Data input-4 | | | |

**Carrier input:**

| Waves | Amplitude($V_{p-p}$) (volts) | Frequency(KHz) |
|---|---|---|
| Carrier input-1 | | |
| Carrier input-2 | | |



CARRY I/P1
CARRY I/P2
DATA I/P
FSK O/P
8038
CARRY O/P
+12V
-12V
+5V
7490
FSK I/P
324
DEMOD O/P
DATA O/P


**Result:**

# 11. PSK MODULATION& DEMODULATION

**AIM:**

To study the various steps involved in generating the phase shift keyed signal at the modulator end and recovering the binary signal from the received PSK signal.

**Apparatus:**

1. PSK Modulation & Demodulation
2. CRO
3. Connecting Wires

**Theory:**

If the carrier phase is shifted between two values then the method is called Phase Shift keying (PSK). In PSK the amplitude of the carrier remains constant.

To generate a binary PSK signal, we have to represent the input binary sequence in polar form with symbols 1 and 0 represented by constant amplitude levels of $+\sqrt{E}$ b and $-\sqrt{E}$ b, respectively. This signal transmission encoding is performed by a polar non return – to – zero (NRZ) level encoder. The resulting binary wave and a sinusoidal carrier φ (t), whose frequency fc = (nc / Tb) for some fixed integer nc, are applied to a product modulator as shown fig.1. The carrier and the pulses used to generate the binary wave are usually extracted from a common master clock. The desired PSK wave is obtained at the modulator output. To detect the original binary sequence of 1s and 0s, we apply the noisy PSK signal x (t) (at the channel output) to a correlator, which is also supplied with a locally generated coherent reference signal φ1 (t) as shown fig.2. The correlator output, X1 is compared with a threshold of zero volts. If X1 <0, it decides in favour of symbol 0. If X1 is exactly zero, the receiver makes a random guess in favour of 0 or 1.

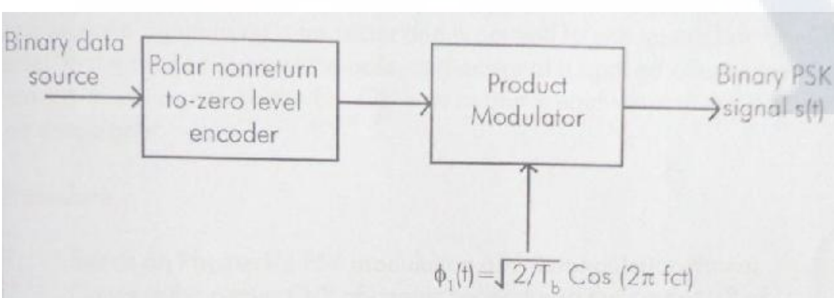



Fig1.Block diagram for BPSK transmitter

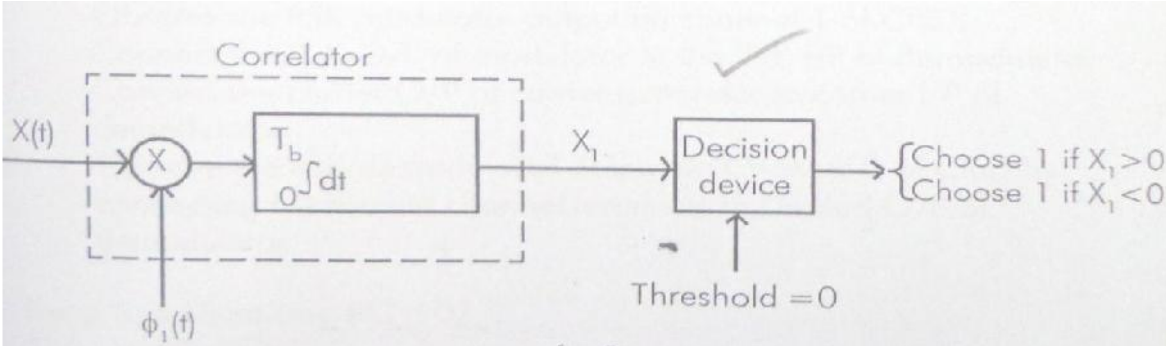



Fig2. Block diagram of BPSK receiver

In PSK modulation and demodulation, the IC 8038 is a basic wave form generator which generates sine, Triangle and square waveforms. The sine wave generated by this 8038 IC is used as carrier signal to the system. The square wave generated by IC 8038 is at ± 12 volts level. So this is converted into a ± 5 volts signal with the help of a transistor and diode. This square wave is used as a clock input to a decade counter (IC 7490) which generates the modulating data outputs. IC CD4051 is an analog multiplex inputs of the IC. Modulating data input is applied to its control input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered to the output. The 1800 phase shift of the carrier signal is created by an operational amplifier using 324 IC.

During the demodulation, the PSK signal is converted into a +5 volts square wave signal using a transistor and is applied to one input of an EX – OR gate. To the second input of the gate, carrier signal is applied after conversion into a +5 volts signal. So the EX – OR gate output is equivalent to the modulating data signal.

**Procedure:**

1. Switch on PSK modulation and demodulation trainer.
2. Connect the carrier O/P of carrier generator to the carrier I/P of modulator.
3. Connect the data O/P of Data generator to the Data I/P of Modulator.
4. Connect CH1 OF CRO to Data generator o/p and CH2 to the PSK O/P of modulator.
5. Compare these two signals.
6. Connect the PSK O/P of modulator to the PSK I/P of demodulator.
7. Connect the carrier O/P of carrier generator to carrier I/P of demodulator.
8. Connect CH1 OF CRO to Data generator o/p and CH2 to the demodulator o/p.
9. Compare these two signals.

**Observations:**

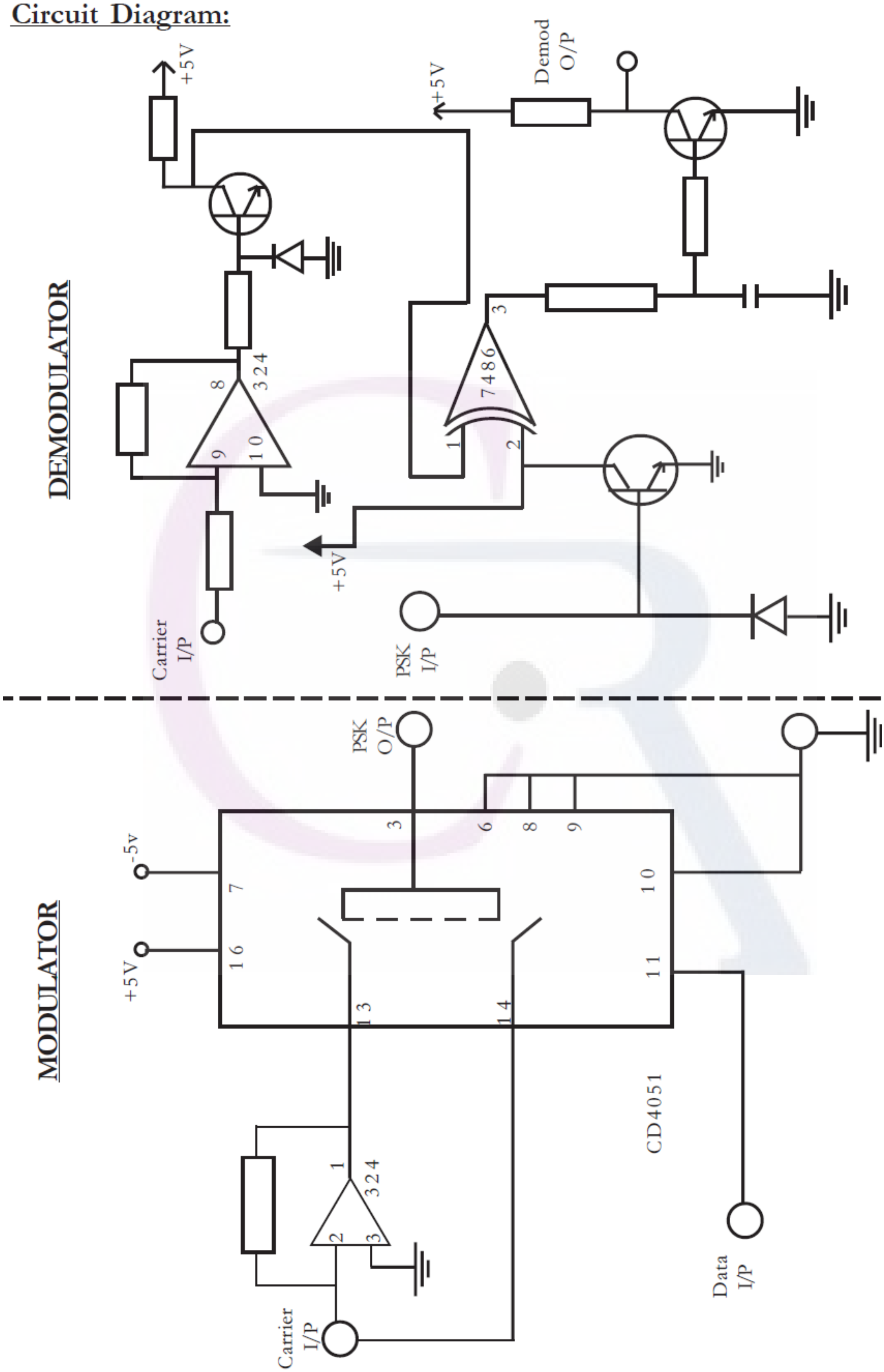
Carrier voltage = 5.68 volts; Carrier frequency = 5.681 K Hz

| Waves | Voltage(volts) | Bit duration(micro seconds) | |
|---|---|---|---|
| | | Bit 1 | Bit 0 |
| Data input-1 | | | |
| Data input-2 | | | |
| Data input-3 | | | |
| Data input-4 | | | |

Bit clock voltage = ; clock on time period =

PSK Modulation & Demodulation

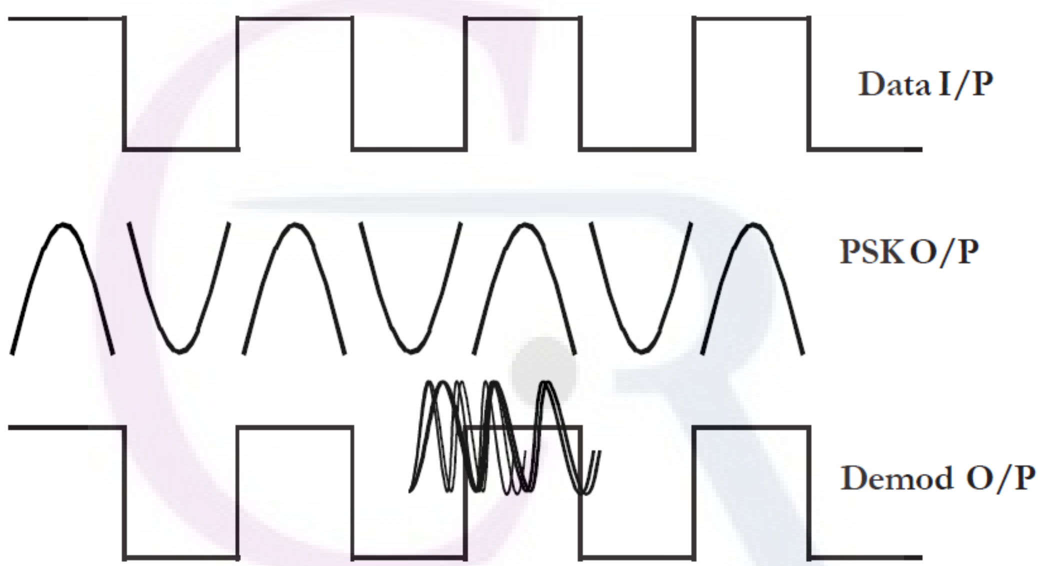
**Circuit Diagram:**



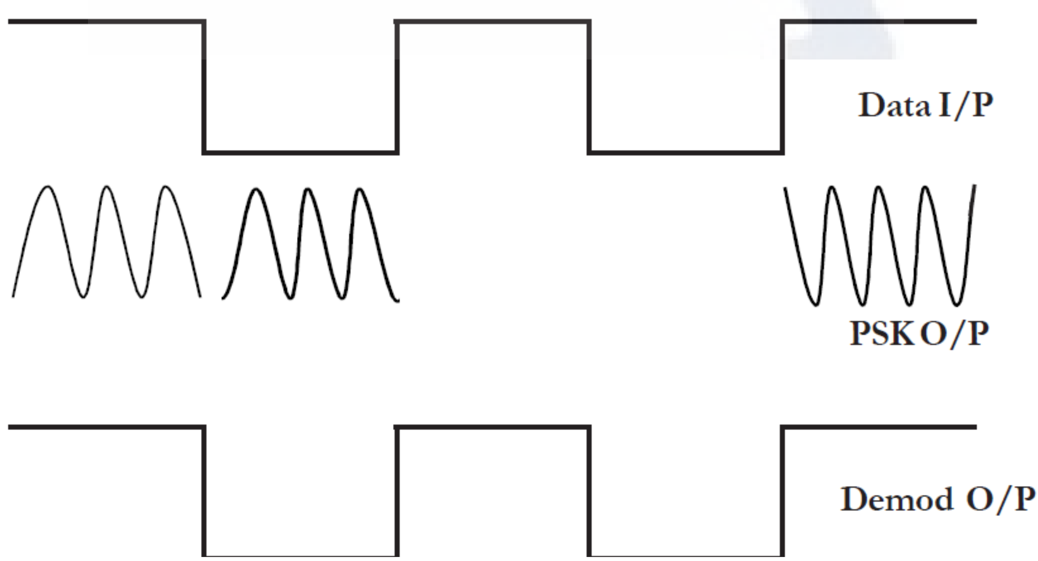
# PSK Expected wave forms

Carrier I/P

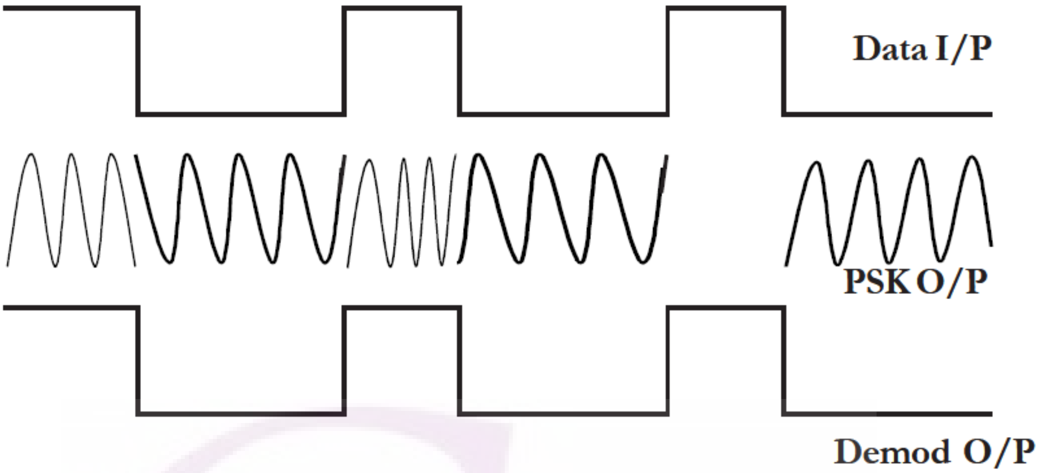
Channel : 1



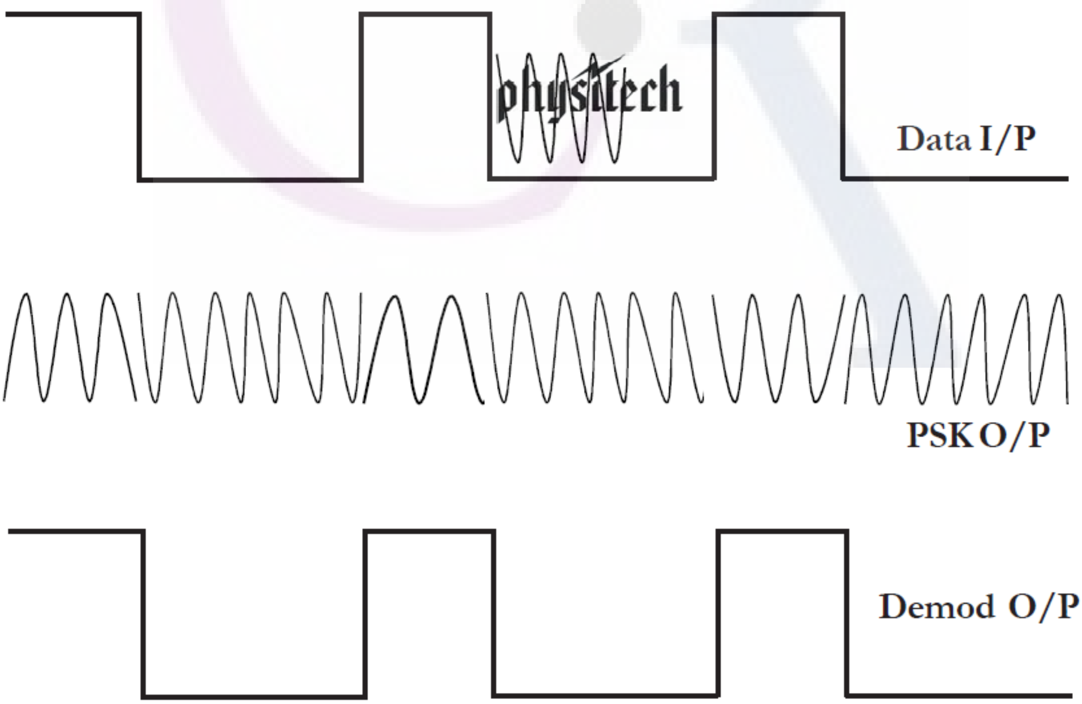

Channel : 2



Channel : 3




Channel : 4




Result:

# 12. DIFFERENTIAL PHASE SHIFT KEYING

**Aim:** To study the various steps involved in generating differential phase shift keyed signal at the modulator end and recovering the binary signal from the received DPSK signal.

**APPARATUS :**

1. Differential Phase shift keying Trainer.

2. CRO

3. Connecting Wires.

**Theory:**

DPSK may be viewed as the non-coherent version of PSK. It eliminates the need for a coherent reference signal at the receiver by combining two basic operations at the transmitter:

1. Differential encoding of the input binary wave and

2. Phase-Shift Keying hence, the name, differential phase shift keying (DPSK).

In effect to send symbol 0, we phase advance the current signal wave-form by 1800, and to send symbol 1, we leave the phase of the current signal waveform unchanged. The receiver is equipped with a storage capability, so that it can measure the relative phase difference between the waveforms received during two successive bit intervals. Provided that the unknown phase θ contained in the received wave varies slowly, the phase difference between wave forms received in two successive bit intervals will be independent of θ.

The block diagram of a DPSK transmitter is shown in fig.1 below. It consists, in part of a logic network and a one-bit delay element interconnected so as to convert the binary sequence {b k} into a differentially encoded sequence {d k}. This sequence is amplitude level encoded and then used to modulate a carrier wave of frequency fc, thereby producing the desired DPSK signal.

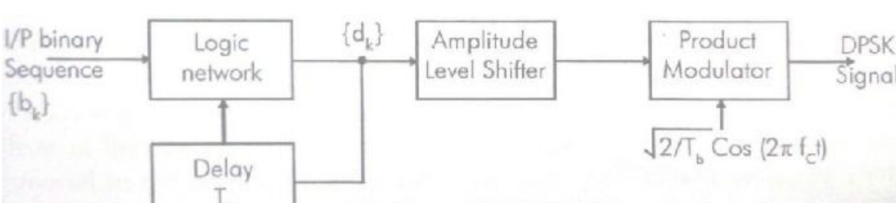



Fig.(1) Block diagram of DPSK Transmitter

The optimum receiver for differentially coherent detection of binary DPSK is as shown in fig.2 below. This implementation merely requires that sample values be stored, thereby avoiding the need for delay lines that may be needed otherwise. The equivalent receiver implementation that tests squared elements is more complicated, but its use makes the analysis easier to handle in that the two signals to be considered are orthogonal.

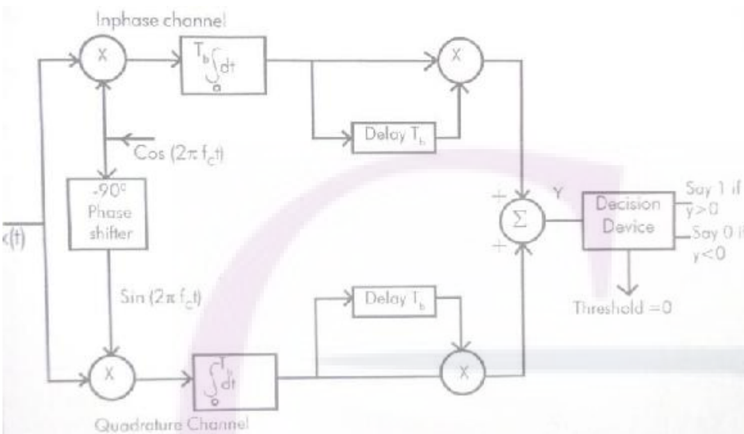



Fig2. Block diagram of DPSK receiver

In DPSK modulation and demodulation, the IC8038 is a basic waveform generator which generates sine, square, triangle waveforms. The sine wave generated by this 8038 IC is used as carrier signal to the system. The square wave generated by 8038 IC is at +/_ 12v level. So this is converted into a +5v signal with the help of a transistor and diode. This square wave is used as a clock input to a decade counter(IC 7490) which generates the modulating data outputs.

The differential signal to the modulating signal is generated using an exclusive-OR gate and a 1-bit delay circuit.CD 4051 is an analog multiplexer to which carrier is applied with and without 180 degrees phase shift(created by using an operational amplifier connected in inverting amplifier mode) to the two inputs of the IC741. Differential signal generated by EX-OR gate (IC 7486) is given to the multiplexers control signal input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered to the output. One-bit delay generation of differential signal to the input is created by using a D-flip-flop (IC 7474).

During the demodulation, the DPSK signal is converted into a +5v square wave signal using a transistor and is applied to one input of an EX-OR gate. To the second input of the gate, carrier signal is applied after conversion into a +5v signal. So the, EX-OR gate output is equivalent to the differential signal of the modulating data. This differential data is applied to the one input of an Exclusive-OR gate and to the second input, after one-bit delay the same signal is given. So the output of this EX-OR gate is modulating signal.

**PROCEDURE :**

1. Switch on differential Phase shift Keying trainer.
2. Connect the carrier output of carrier generator to the 13th pin of CD4051 (Analog mux) of modulator.
3. Connect the Bit clock output to the Bit clock input at pin 3 of 7474 (8-bit converter) of modulator.
4. Connect the data output of data generator to the input of modulator circuit.
5. Connect channel 1 of CRO to the data generator.
6. Observe the differential data output at pin 2 of 7474 IC on channel -1 of CRO.
7. Observe the DPSK modulated output on channel-2 of CRO.
8. During demodulation, connect the DPSK modulated output to the DPSK I/P of Demodulator.
9. Connect the Bit clock O/P to the Bit clock I/P of Demodulator and also connect the carrier O/P to the carrier I/P of demodulator.
10. Observe the demodulated data O/P at demodulator.
11. The frequency of modulation data signal should be equal to the demodulated O/P.

**Observations:**

Carrier voltage = 5.04volts; Carrier frequency = 5.618 K Hz.

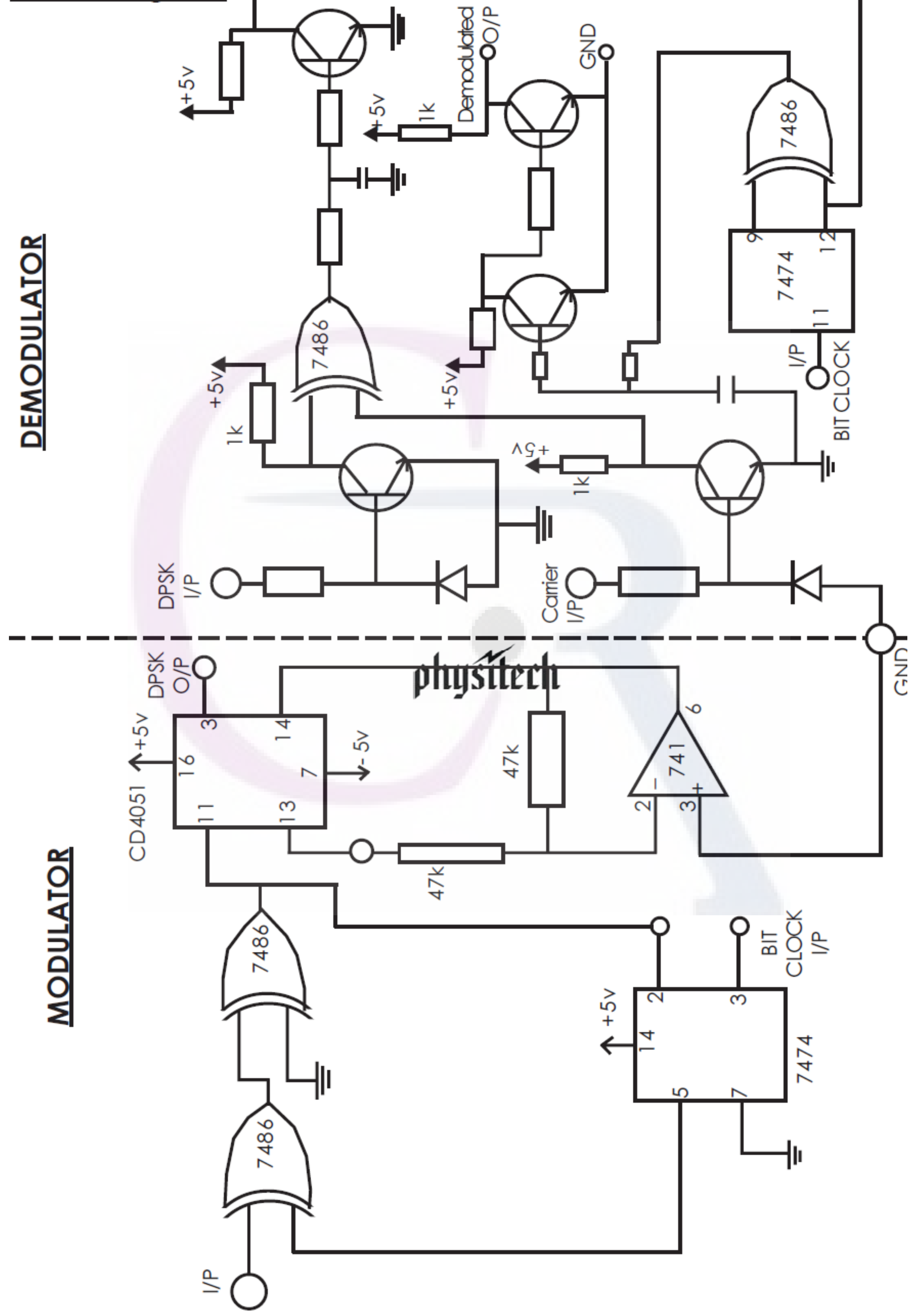
| Waves | Amplitude(volts) | Duration of Bits (micro seconds) | |
|---|---|---|---|
| | | Bit 1 | Bit 0 |
| Data input-1 | | | |
| Data input-2 | | | |
| Data input-3 | | | |
| Data input-4 | | | |

Bit clock voltage = ; clock on-time =
clock off-time =

| Differential output corresponding to | Amplitude(volts) | Duration of Bits (micro seconds) | |
|---|---|---|---|
| | | Bit 1 | Bit 0 |
| Data input-1 | | | |
| Data input-2 | | | |
| Data input-3 | | | |
| Data input-4 | | | |

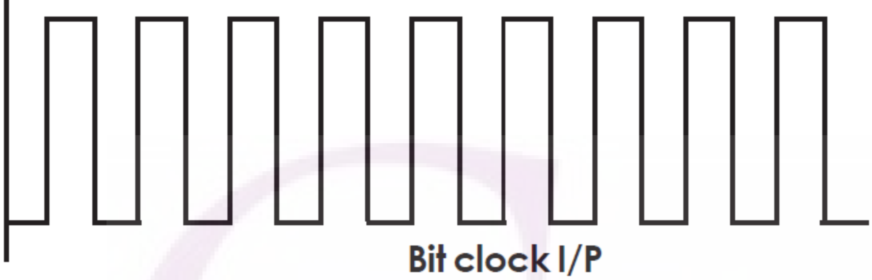
# Differential Phase Shift Keying

## Circuit Diagram:



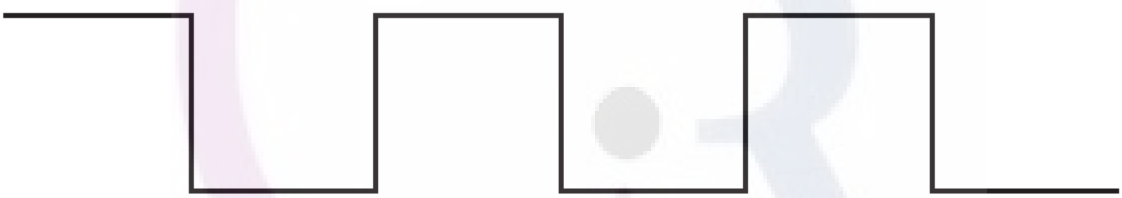
## EXPECTED WAVEFORMS :

Carrier I/P

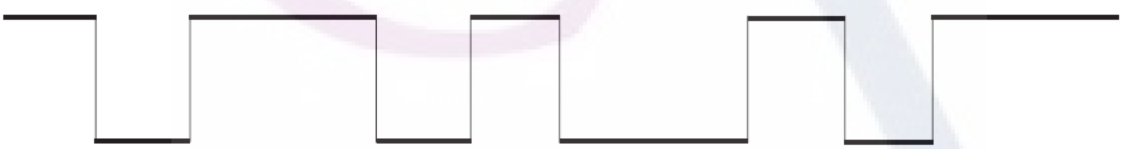


Bit clock I/P

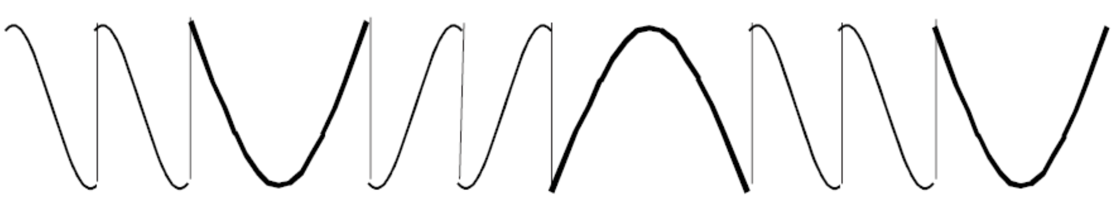
Channel : 1



Data I/P



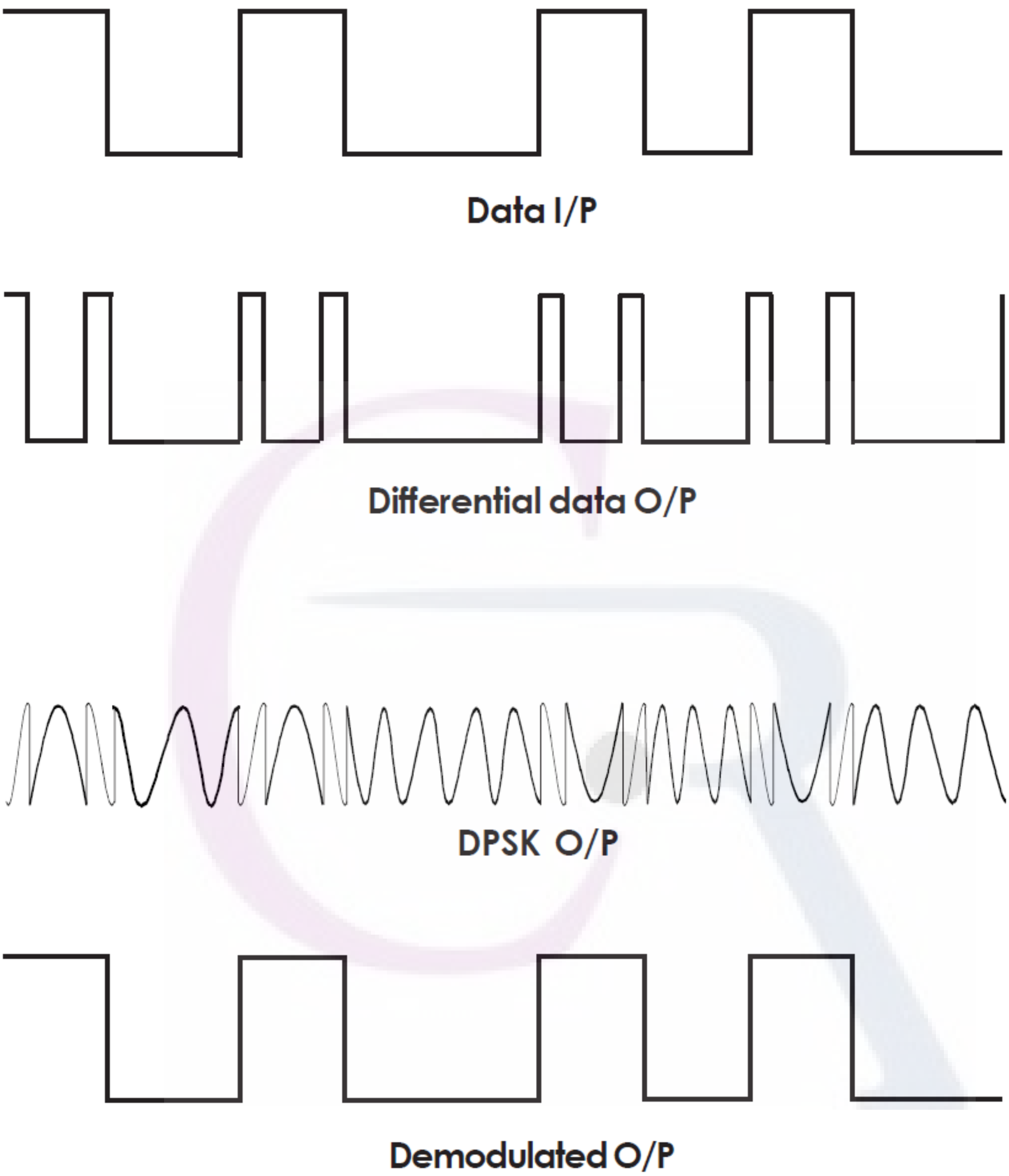
Differential data O/P



DPSK O/P

Demodulated O/P

**Channel :2**




## Result:

# 13. TIME DIVISION MULTIPLEXING

**Aim:** To verify the operation of Time Division Multiplexing

## Apparatus:

1. Time Division Multiplexing and De Multiplexing Trainer
2. CRO
3. BNC Probes & Connecting Wires

## Theory:

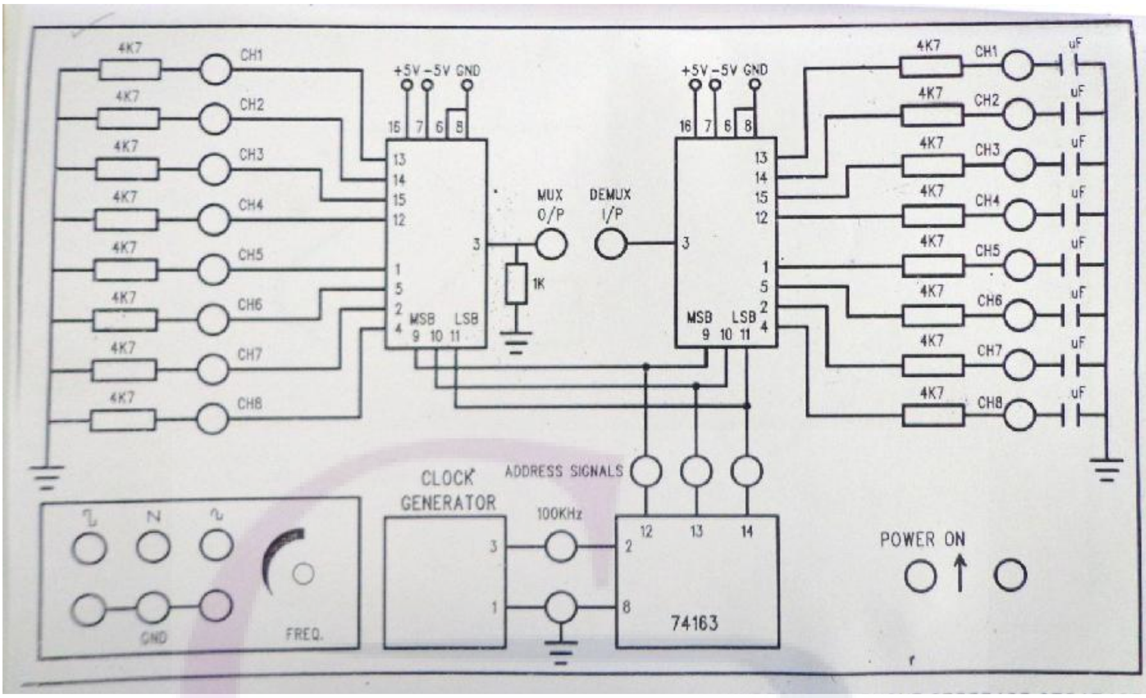
The Sampling Theorem provides the basis for transmitting the information contained in a band limited message signal m (t) as a sequence of samples of m (t) taken uniformly at a rate that is usually slighter higher than the nyquist rate. An important feature of the sampling process is a conservation of time. That is, the transmission the message samples engages the communication channel s for only a fraction of the sampling interval on a periodic basis, and in this way some of the time interval between adjacent samples is cleared for use by other independent message sources on a time shared basis. We there by obtain a time division multiplexing (TDM) system, which enables the joint utilization of a common communication channel by a plurality of independent message sources without mutual interference among them.

The TDM system is highly sensitive to dispersion in the common channel, that is, to variations of amplitude with frequency or lack of proportionality of phase with frequency. Accordingly, accurate equalization of both magnitude and phase response of a channel is necessary to ensure a satisfactory operation of the system. Unlike FDM, TDM is immune to non linearities in the channel as a source of cross talk. The reason for this is, the different message signals are not simultaneously applied to the channel.

The primary advantage of TDM is that several channels of information can be transmitted simultaneously over a single cable.

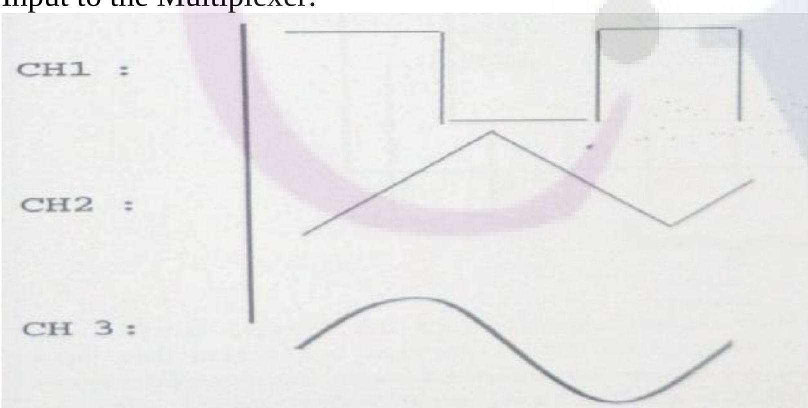
In the circuit diagram the 555 timer is used as a clock generator. This timer is a highly stable device for generating accurate time delays. In this circuit this timer generates clock signal, which is of 100 KHz frequency (approximately). This clock signal is connected to the 74163 IC, it is synchronous presettable binary counter. It divides the clock signal frequency into three parts and those are used as selection lines for multiplexer and de-multiplexer. Inbuilt signal generator is provided with sine, square and triangle outputs with variable frequency. These three signals can be used as inputs to the multiplexer. IC 4051 is an 8 to 1 Analog Multiplexer. It selects one-of-eight signal sources as a result of unique three bit binary code at the select inputs. Again IC 4051 is wired as one to eight de-multiplexers. Demux input receives the data source and transmits the data signals on different channels.

Kit Diagram:

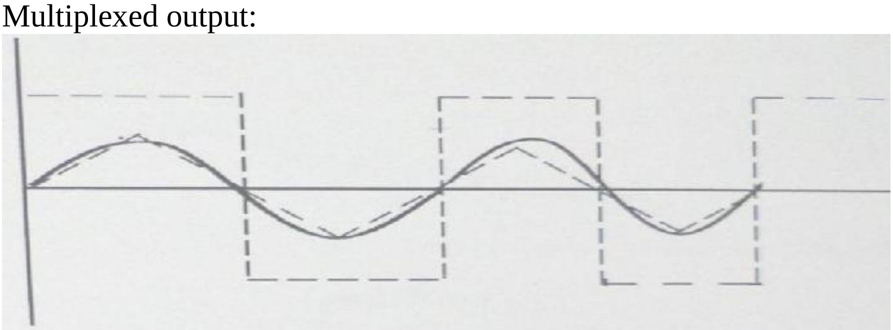



Waveforms:

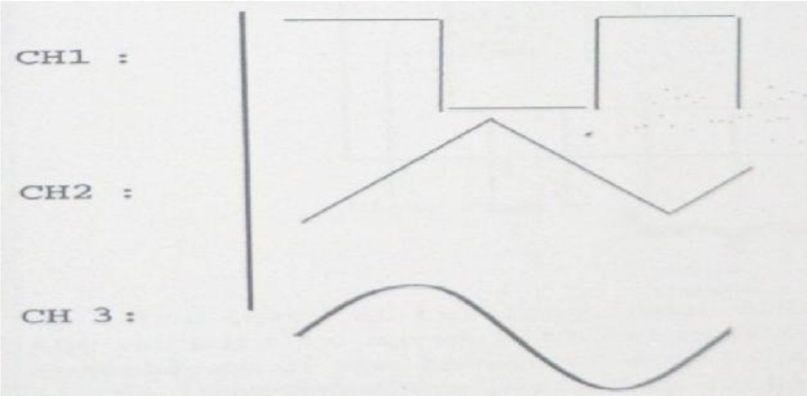
Input to the Multiplexer:




Multiplexed output:



Demultiplexed Output:




## Observations:

| S. No | Signals | Amplitude($v_{p-p}$) | Time period (milli seconds) |
|---|---|---|---|
| 1 | Square wave | | |
| 2 | Sinusoidal wave | | |
| 3 | Triangular wave | | |
| 4 | Clock signal | | |

## Result: