

Setup

↳ Disable Grub4 (remove and)

System Services → Select → NFS → OK
Enable

Gedit /etc/hosts

127.0.0.1 local host local host .localdomain
(Local host Glue)

(0.0.0.1 (Server IP) Cadenfe
<Tab> Same & Use window)

work space

↳ Ping Cadenfe

Cmd → terminal

Gtar -xzvf → Cad - tar. sz

Cad - Pg. mid - tar. sz
for Extract

cshrc

Copy ~~cshrc~~ file into the Cad folder

CMD :-

ifconfig

Server IP :- 10.66.4.1

root host :-

Ping 10.66.4.1 (server IP)

Terminal :-

Edit \leftrightarrow /etc/hosts \leftrightarrow

127.0.0.1

\rightarrow Delete from local host.

\$ localhost localhost.localdomain

(Add)
 \downarrow

System no :-
C01
System name

Server IP. 10.66.4.1 Cadence

~~start~~

-XZNF

09:09:25

stop

-XZNF - Cd. Bar. JZ

\leftrightarrow
Space

Commands for installing Cadence on Linux:-

cmd → terminal

tar -xvf Cad.tar.gz

Cad.tar.gz

Cad.Pg.mit.tai.gz

cd Extract

Copy cshrc file in to the Cad folder.

13/07/11

Start
↓
Specification
↓
RTL Coding
↓
to
functions Simulation
↓
Synthesis
↓
Timing Simulation

ASIC Flow
floor Planning
↓
Power planning (Power
balls)
Vss/Vdd
Placement
↓
CTS (clock tree
synthesis)
↓
Routing
↓
XRC (RC
corner)
↓, Peristed Capacit
GDS II
(Graphical Data Stream
information Interchange)

Contd → Open terminal

↓
Gitter test.v

↓
type csh < home/cad/
↓
source /home/cad/cshrc
cshrc

{ # csh

source |home/cad/cshrc

welcome to Cadence tools Suite

nc launch < - new
↓ space

↓ Select multiple Setup.

click → Create cde.lib file

↓
Save

Select ↓ option (Don't include
any libraries)
↓
vliblog design.

OK

↓
OK.

nc launch: (root) → window.

↳ Gitter.v (click launch vliblog Confirmed option)
↳ Gitter-test.v → (")

Right window

↳ work lib

↳ Counter

↳ (Counter test) Select

and Click

(Eject file in ~~menu~~
menu)
window

↳ snapshots

↳ work lib Counter module

Select

(and click launch

simulator with Client session)

Console sim vision

Design Browser 1

Simulator

+ Counter test

→ Right click → Set waveform

window.

Run

Waveform 1 - sim vision

Close all windows & keep terminal window

In Counter folder → (sc-script.tcl)
↓
used for synthesis.

Lib folder (Contain packages)
↳ (45, 90) 180
↓
Contains Library files

(sc → syncopy is design Counterpart)
↳ Contains in Counter folder

Go to terminal window:-
↳ # sc < -f > script file name

Cadence executed window

↳ Counter (doubt click) → display
(RTL Schematic)

Counter → before close all window.

Go to file → import design.

↓
window file click with button select
Counter - netlist.v → Add (close)

Left files \rightarrow ~~Get~~^{left} \rightarrow Select last 2 files

Power node \rightarrow V_{DD} ; V_{SS}

(Rejout .jobbook) \rightarrow sterilized \rightarrow

In mmnc \rightarrow Select load \rightarrow ~~load~~ (Rejout global)

(OK)

Press 'F'

menu \rightarrow Specify floor plan

Code to 15' 5 all 15' \rightarrow (OK)

4 Power \rightarrow Power Planning \rightarrow Add ring

Top & bottom \rightarrow metal - 9

left - Right \rightarrow metal - 8

width - 1'

Spacing \rightarrow 0.4

Select (centered on channel)

g g

Select (Center in channel)

Open
Cover
Close

Route → Board Planning → Add Strips

Net → (V_{DD} & V_{SS} · Add)

Layer :- Metal - 8 ;

No. of sets - 5

↓
OK

Menu → Route → Special Route

Notes: (V_{DD} & V_{SS}) → Add → OK

Top layer metal - 9 metal - 1

(OK)

Select '1' → Line Horizontal → Press '9'
(Display details)

Menu → Place → Place Std cell

Route Run full placement (OK)

Timing: - Report timing → Pre (OK)

OK

In technical window display timing report

Optimize → Optimal Design

→ Post CIS

→ OK

Violating paths are 0 0 0

clock → synthesis clock → browser
Select all CLK files
(OK)

Q1 defined

→ we have engine is not CK

→ Select TS S mode - Engine is not CK.

to be change to
Set IS mode - Engine CK

clock → Synthesis clock fine → OK

Timing → Report timing → Hold → OK
Setup

Timing → Report timing → Post CIS
→ Hold → OK

Optimize → Optimal design → Post CIS → Hold → OK

Timing → Report timing → Post CIS → Hold → OK.

Optimize → Optimize design → Post CIS → Hold → OK

Route → Nano route → Route I,

optimize via v

optimize via c

Timing → Report timing → Post CIS → Setup

and

again save route for

hold also

(check in terminal window)

If need is that:

+ analysis type on chip variation - CFS > both

click in terminal window

→ Optimize → Optimize design → Post Route
+ (OK)

Timing → Extract RC → Save SPT &
SPF

Standard Parasitic format

Standard Parasitic Object format

Place → physical cell → Add filled →
↑
(to fill empty
place) - Add all filled cells (dc)

file → save → ~~GASOGENS~~ G5/OASIS →
→ file name as (Counter.gds) ✓

file → save → netlist
Counter - Pd.V

file → save design → Enhance → ok

open → Counter - Pd.V & Counter-test.V

copy time scalar 1ns/1ps from
Counter-test.V to Counter - Pd.V

and charge module counter to Counter - Pd

* In Counter-test N

Cooker → change to Counter-Pd.

Open terminal → # n launch

↑
Cooker - Pd. ✓ → Confirms

Cooke - test ✓ → couple

Slow. ✓ → couple

↑
Cooke - test → globule

Snail shell → land snail called slugs

↑
Counter test → high disk → land snail

session - 2

Create new folder



Open terminal → type #CSH
source /home/ad/cshrc

Virtual window



Virtuoso < > 4

space



Tools → Library manager



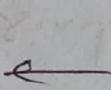
file → new library → type name

OK

Attach library to Technote library



Genetic



GBLK 180



Select lib → VLSI



file new → sel vise



QA Cell type → uncheck



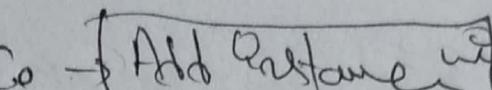
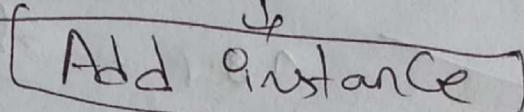
Type → schematic ← OK



Select → Always

To import Pmos & NMOS

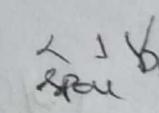
To import PMOS & NMOS

Create → Instance → Add instance 
↓
click browse →
mosfet → gtrak 180
cell → (NMOS) type
↓
Select symbol.
Add instance 
↓
click hide

To PMOS → Create → Instance → browse

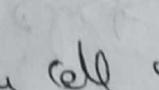
↓
Select PMOS
Place

↓
close.

Bes → W for narrow wire
P for Pin names → type A 
Q for Retake selection.

After this click and save 

wiring will be seen in virtoso window

Create → cell view → from cell view  OK
left A ; Right Y ; Top: Vdd ; Bottom: Vss
(OK)

(U - for unto),
remove rectangle box middle in schematic

→ Create Polygon symbol click

+

(close)

file → new → Cell - view ✓

use - test OK

Create → instance → Browse

library → VLSI → inter → symbols
↓
close

Create → instance → browse → Analog lib →
Vdc - close

dc voltage - 1.8v

browse → Vpulse - 1.8v

delay / cont period 20m

pulse width - cont

Launch
+

for simulate

ADEL → Setup → go to simulate (specie)

Setup → model library → ok.

Analysis → choose → (bar) ✓

↓
stop time 100 (modulate) ✓

Outputs → Setup → (click from design)
OK

Select Net & { → hen.
✓outs &

Select mode to default use 'Q' key button
type → voltage
delay

Tools → calculate → function panel
→ All functions delay (s)

on tick (clip) & select wave

Sing 1 → %p select

Signal 2 → click on off signal select

threshold value → 0.9 (say. of Vdd)

threshold val 2 → 0.9

Edge no: - 1 ; Edge no: 2 : 1

Edge type 1 :- Rising ; Edge type 2 :- Falling
(click on Apply)

Go to ADCL window \rightarrow Output Setup,

New Expression

Act Expression

Name :- tph1 (\$

Click Add \rightarrow ~~simulated~~ (tph)

Calculator \rightarrow (clear buffer button)

function Panel \rightarrow delay +

Select signal $\rightarrow \frac{1}{2}$

Edge :- 2

②

2

Rising

Falling

(Apply)

~~tph~~

ADCL \rightarrow Output Setup \rightarrow Act Express \rightarrow ~~tph~~
~~add above :- spd~~

Open:- $((tphl + tphy)/2)$

Add.

OK

Closes → calculation, waveform

ADEL window →

Analyze → choose → DC

✓ save DC operating point

Component Parameter → Select Component

Select DC → OK

QIP
(VDC) ✓

Start - Stop.

↓

↓

0

1.8

untick from Analysis

Select DC ✓ Renaming unselected.

(netu; ope) ✓
Select

Go to simulate →

ADEL window → close waveforms

Session → Save State

Cell view

(any name) ✓

OK

Close Schematic

Library manager $\xrightarrow{\text{VLSI}}$ ~~DK~~ \rightarrow Pinout & Schematic

Doing layout

aunch \rightarrow layout xl. \rightarrow OK

\downarrow
newfile (OK)

Connectivity \rightarrow Generated \rightarrow All from Schematic

\downarrow
Generated
 \downarrow
OK

Print & Netlist.

to GND and stretch 'S' to move

Connectivity \rightarrow nets \rightarrow Show/hide Selected
Incomplete nets

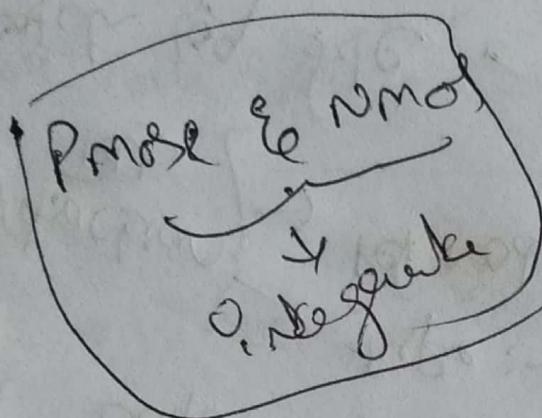
Green line is Polygigion

Type 'P' once more to

Make metal connection.

Nmol → Select → type 'Q'

Edit instance → Parameter ↴



Bodyfile

integrate

Place → for Placent → Select V_{DD} ; V_{DD}

Edge → iOP → (apply)

again

Select V_{SS} → Bottom

→
Apply

Close

H. Rail ✓

again H. Rail → V_{SS} →

close

Altium - Technology —

— Double click —

alt

A

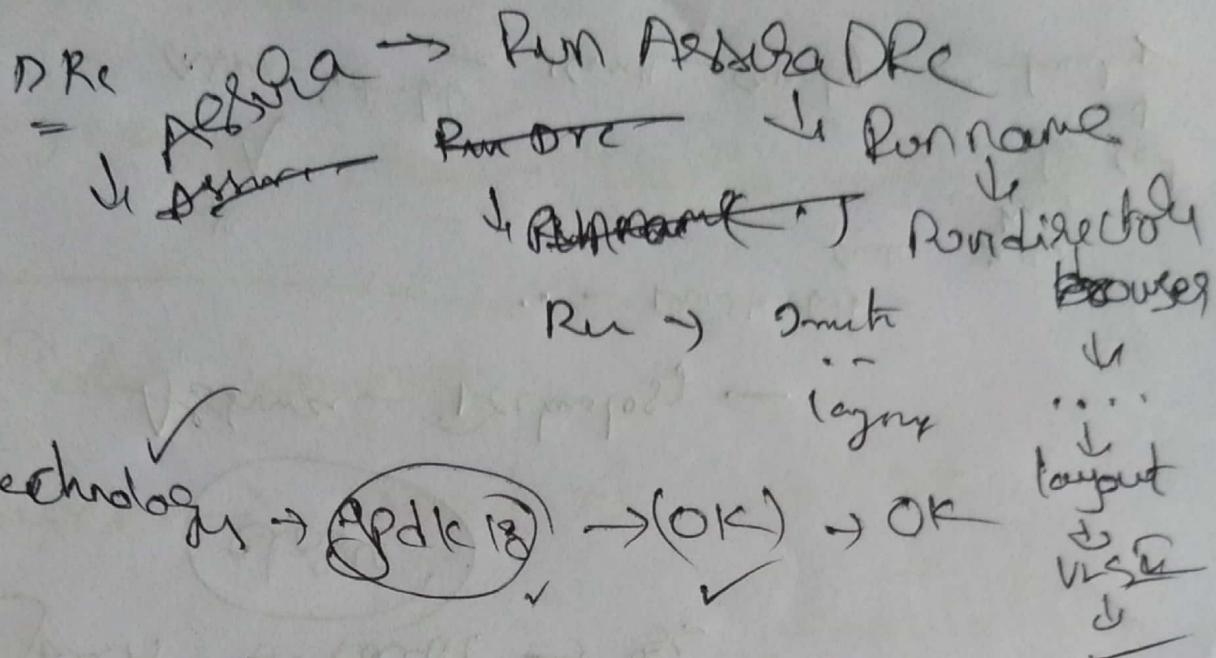
altia - tool - lib

ctrl - R click
- Name

- for card
+ font +

some analy

+ font



Assura → Run LVS

Run name → browser → Layout
 Technology → Gdk 180

Assura → Run QRC

{ Technology → GDK 180 ;
 { output → Extracted View
 tabs → Type :- FC
 Extraction → Ref node of gnd! → (OK)
 Tab

watch log file

(close layout)

Go to library manager → select ^{invoker} → Av Extender
VLSI ↗

control + A & shift A
we can see → (acceptance).

↓
Always
→
by sat.

file → library - VLSI → Invoker-test - schematic