CHIRANJEEVI REDDY INSTITUTE OF ENGINEERING & TECHNOLOGY

(Approved by AICTE,New Delhi & Affiliated to JNTU,ANANTAPUR)
Susheela Nagar, Bellary Road, ANANTAPUR.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING.

ELECTRONIC DEVICES & CIRCUITS LAB (9A04302)

(II B.Tech I Semester)

LAB-MANUAL

Head of the Department

S.Raghavendra Swami
M-Tech.,
Assistant professor in ECE.

LIST OF EXPERIMENTS

LIST OF EXPERIMENTS AS PER JNTUA, ANANTAPUR

ADDITIONAL EXPERIMENTS

1. P-N JUNCTION DIODE CHARACTERISTICS

AIM: To observe and draw the Forward and Reverse bias V-I Characteristics of a P-N Junction diode.

APPARATUS:

P-N Diode 1N4007

Regulated Power supply (0-15V)

Resistor 1KΩ

Ammeters (0-200mA, 0-200µA)

Voltmeter (0-20V)

Breadboard

Connecting wires

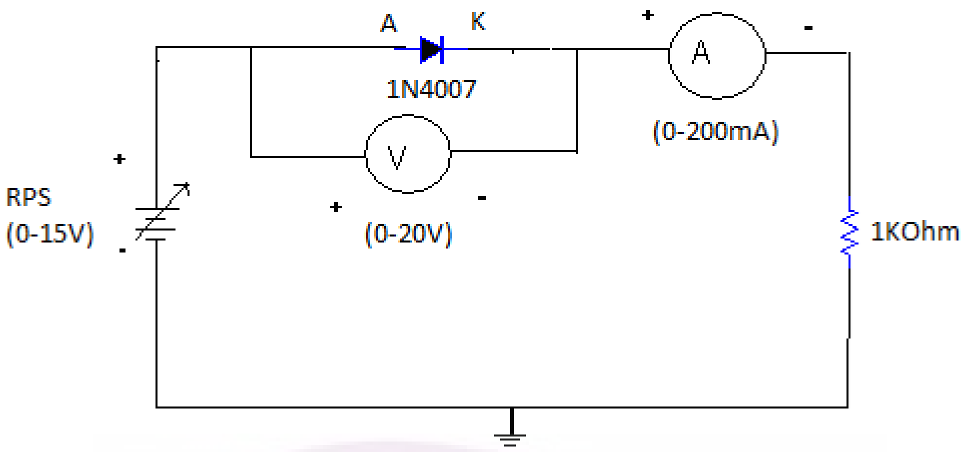
THEORY:

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

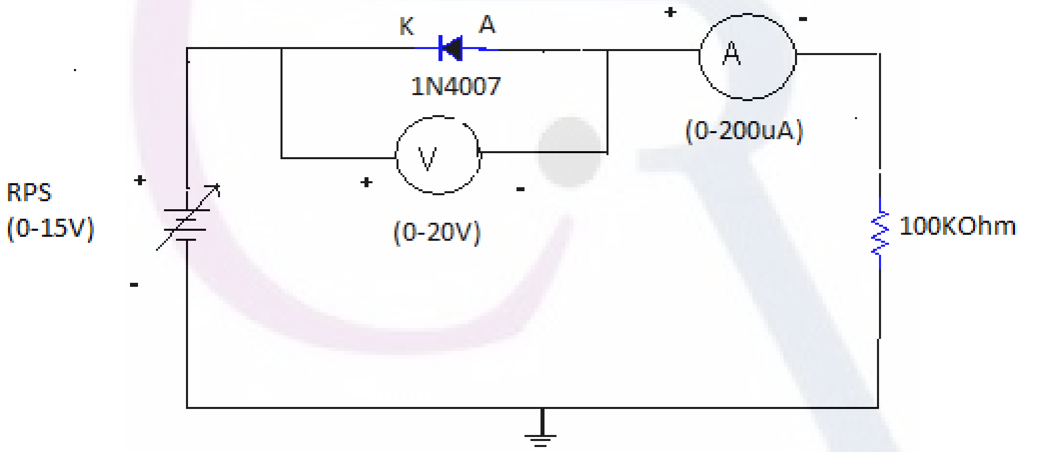
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to the minority charge carriers.

CIRCUIT DIAGRAM:

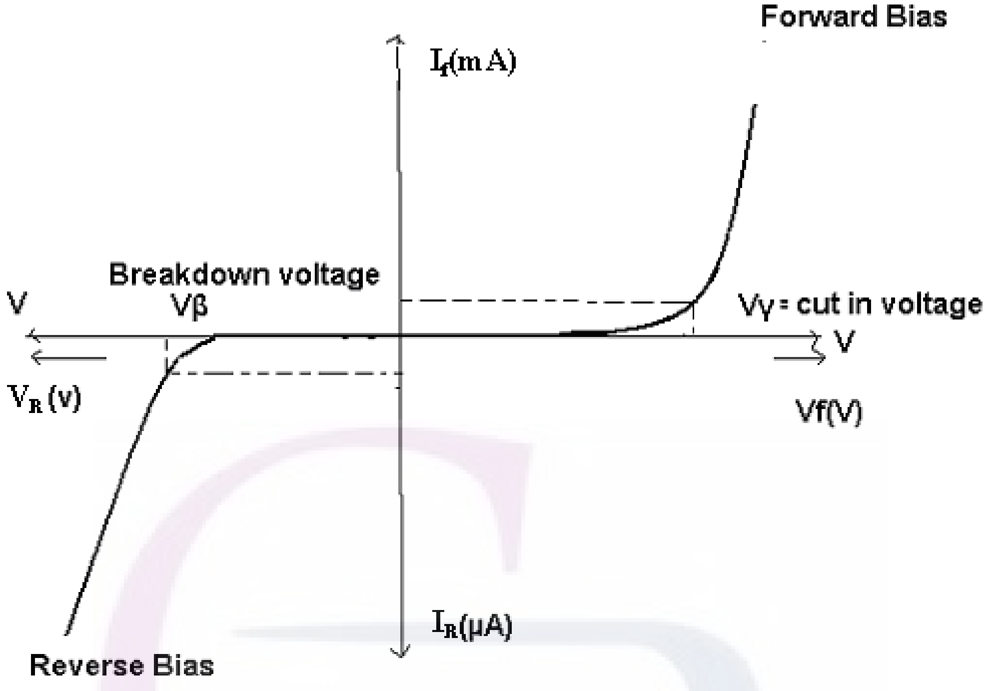
FORWARD BIAS:



REVERSE BIAS:



MODEL GRAPH:



PROCEDURE:

FORWARD BIAS:

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode,
3. Switch on the power supply and increases the input voltage (supply voltage) in steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The reading of voltage and current are tabulated.
6. Graph is plotted between voltage and current.

OBSERVATIONS:

S.NO	V_f (V)	I_f (mA)

PROCEDURE:

REVERSE BIAS:

1. Connections are made as per the circuit diagram.
2. For reverse bias, the RPS +ve are connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) in steps
4. Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated
6. Graph is plotted between voltage and current.

OBSEVATIONS:

S.NO	V_r (V)	I_r (mA)

RESULT: Forward and Reverse Bias characteristics for a p-n diode is observed

2. ZENER DIODE CHARACTERISTICS

AIM: To observe and draw the regulator characteristics of a zener diode at supply and load side.

APPARATUS:

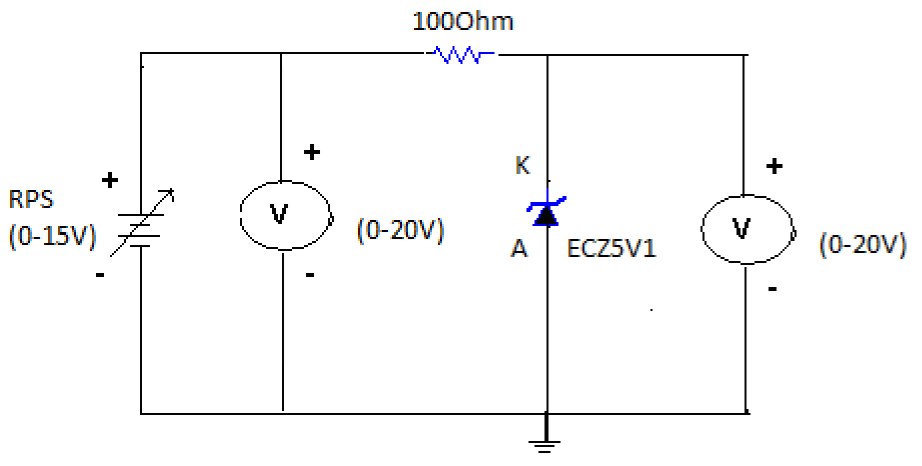
Zener diode – ECZ5V1
Regulated Power Supply (0-15V)
Voltmeter (0-20V)
Ammeter (0-200mA)
Resistor (1KΩ)
Breadboard
Connecting wires

THEORY:

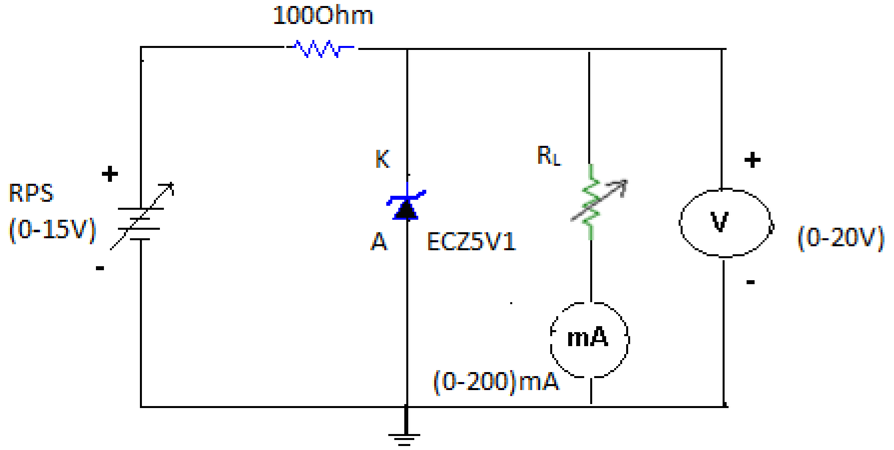
A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device. To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

CIRCUIT DIAGRAM:

SUPPLY SIDE:



LOAD SIDE:



PROCEDURE:

SUPPLY SIDE:

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. For different input voltages (V_i) corresponding output voltages (V_o) are observed and then noted in the tabular form.
4. A graph is plotted between input voltage (V_i) and the output voltage (V_o).

LOAD SIDE:

1. Connection are made as per the circuit diagram
2. The load is placed in full load condition and the output voltage (V_o), load current (I_L) are measured.
3. The above step is repeated by decreasing the value of the load in steps.
4. All the readings are tabulated and a graph is plotted between load current (I_L) and the output voltage (V_o).

OBSERVATIONS:-

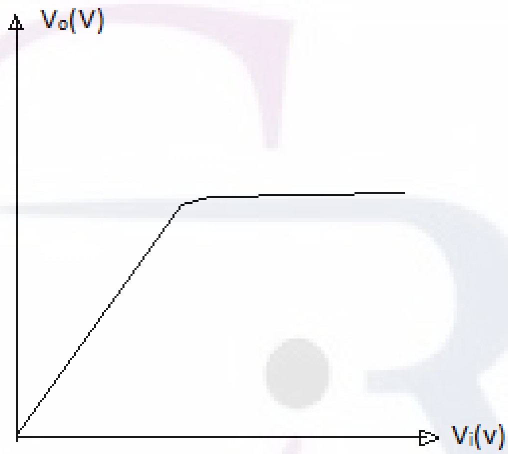
SUPPLY SIDE:-

S.NO	V_i (V)	V_o (V)

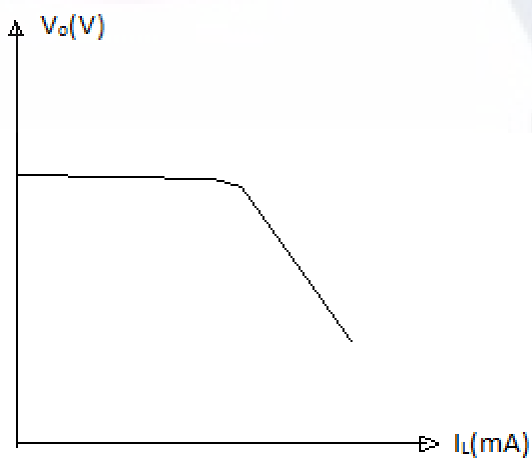
LOAD SIDE:-

S.NO	I_L (V)	V_o(V)

MODEL GRAPH:
SUPPLY SIDE:



LOAD SIDE:



RESULT: Regulator characteristics of zener diode are obtained and graphs are plotted for load and supply side.

3. CB CHARACTERSTICS OF A TRANSISTOR

AIM: To observe and draw the input and output characteristics of a transistor connected in common base configuration.

APPARATUS:

NPN-Transistor, BC107
Regulated Power Supply (0-15V)
Voltmeter (0-20V)
Ammeters (0-200mA)
Resistor, 1KΩ
Breadboard
Connecting wires

THEORY:

A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration, I_E is +ve, I_C is –ve and I_B is –ve. So,

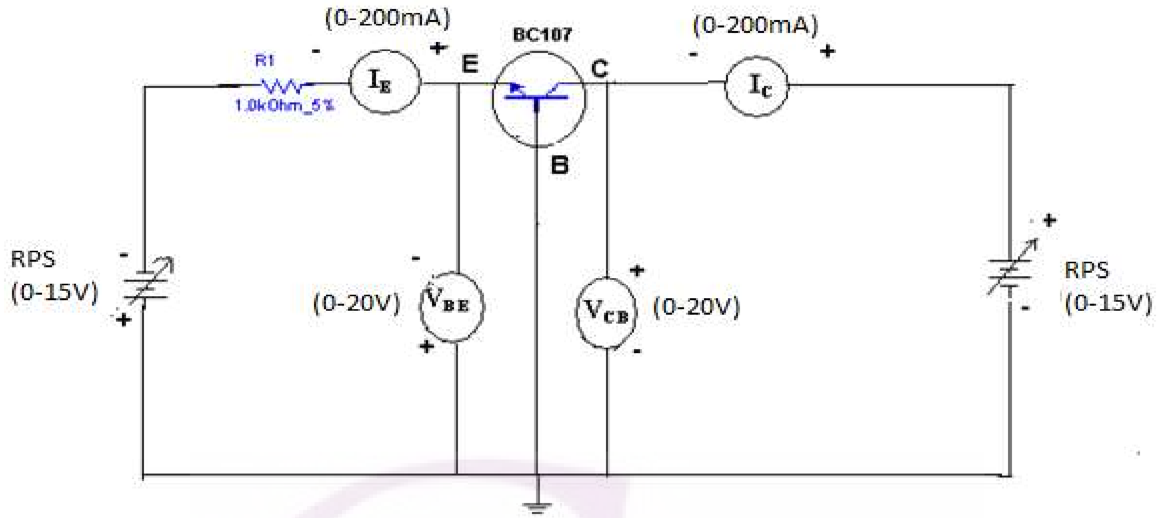
$V_{EB}=f1\ (V_{CB},I_E)$ and

$I_C=f2\ (V_{CB},I_B)$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by,

$$\alpha= \Delta I_C/ \Delta I_E$$

CIRCUIT DIAGRAM:



PROCEDURE:

INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, the output voltage V_{CE} is kept constant at 0V and for different values of V_{EB} note down the values of I_E.
3. Repeat the above step keeping V_{CB} at 2V, 4V, and 6V.All the readings are tabulated.
4. A graph is drawn between V_{EB} and I_E for constant $V_{CB.}$

OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input I_E is kept constant at 10mA and for different values of V_{CB}, note down the values of $I_{C.}$
3. Repeat the above step for the values of I_E at 20 mA, 40 mA, and 60 mA, all the readings are tabulated.
4. A graph is drawn between V_{CB} and I_C for constant I_E

OBSERVATIONS:

INPUT CHARACTERISTICS:

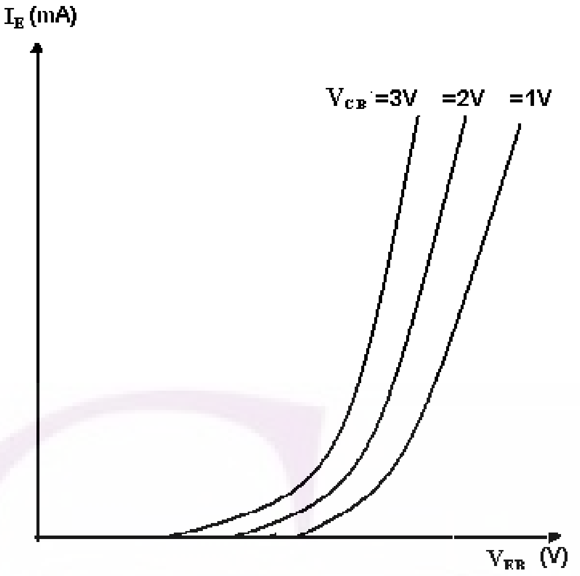
S.No	V_{CB}=0V		V_{CB}=1V		V_{CB}=2V	
	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

OUTPUT CHARACTERISTICS:

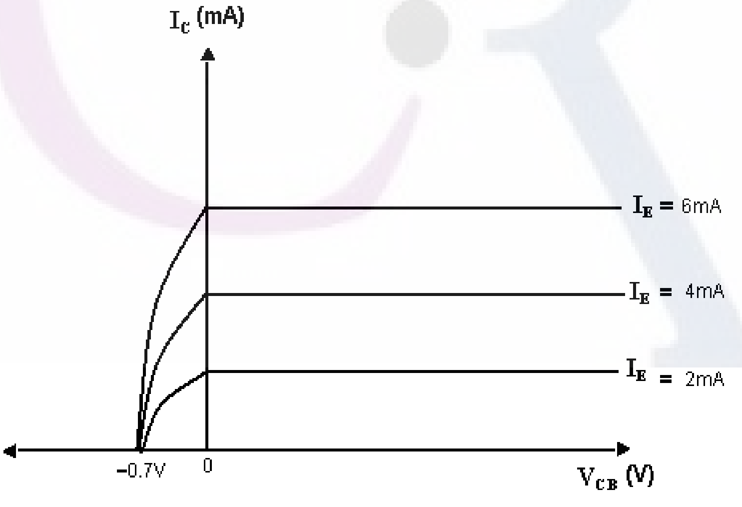
S.No	I_E=2mA		I_E=4mA		I_E=6mA	
	V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)

MODEL GRAPHS:

INPUT CHARACTERISTICS:



OUTPUT CHARACTERISTICS:



RESULT: The input and output characteristics of the transistor are drawn.

4. CE CHARACTERSTICS OF A TRANSISTOR

AIM: To draw the input and output characteristics of transistor connected in CE configuration

APPARATUS:

NPN-Transistor (BC107)
Regulated Power Supply (0-15V)
Voltmeters (0-20V)
Ammeters (0-200μA), (0-200mA)
Resistors 1KΩ
Breadboard
Connecting wires

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output.

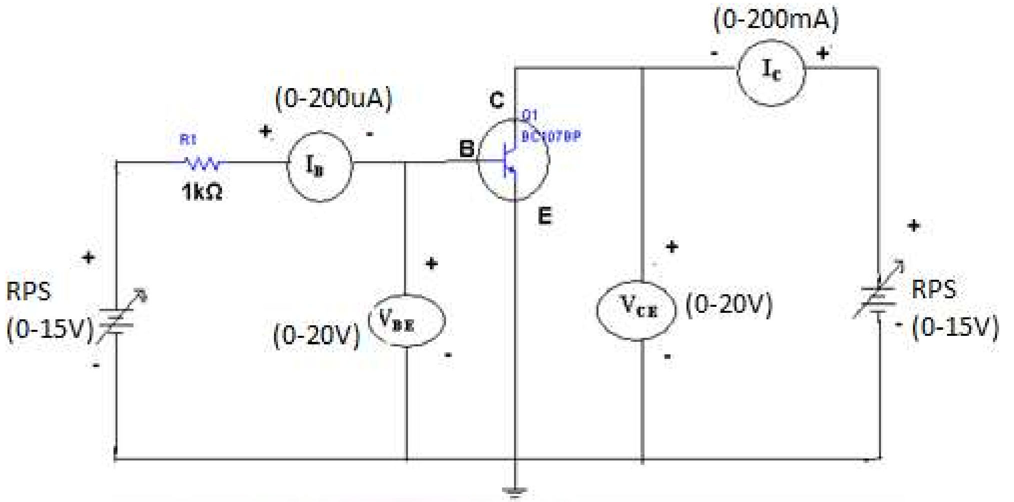
The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with $V_{BE.}$ Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant $I_{B.}$ the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of $V_{CE.}$ The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to $I_{B.}$

The current amplification factor of CE configuration is given by

$$B = \Delta I_C/\Delta I_B$$

CIRCUIT DIAGRAM:



PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of $V_{BE.}$ Note down the values of I_C
3. Repeat the above step by keeping V_{CE} at 2V and 4V.
4. Tabulate all the readings.
5. plot the graph between V_{BE} and I_B for constant V_{CE}

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current I_B is kept constant at 10μA and for different values of V_{CE} note down the values of I_C
3. repeat the above step by keeping IB at 75 μA, 100 μA
4. tabulate the all the readings
5. plot the graph between V_{CE} and I_C for constant I_B

OBSERVATIONS:

INPUT CHARACTERISTICS:

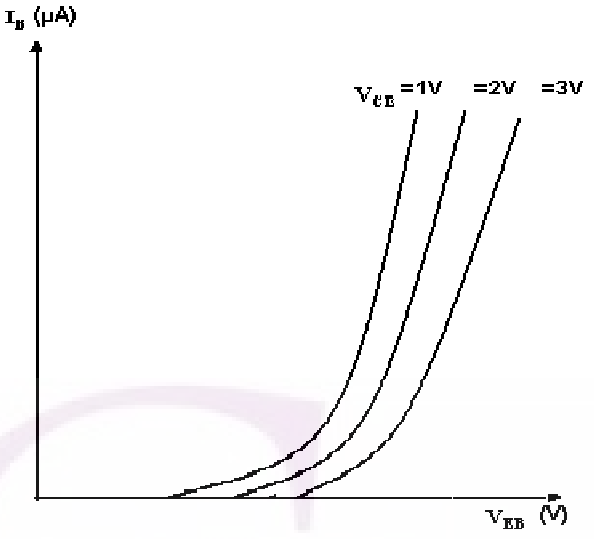
S.NO	V_{CE} = 1V		V_{CE} = 2V		V_{CE} = 4V	
	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

OUTPUT CHARACTERISTICS:

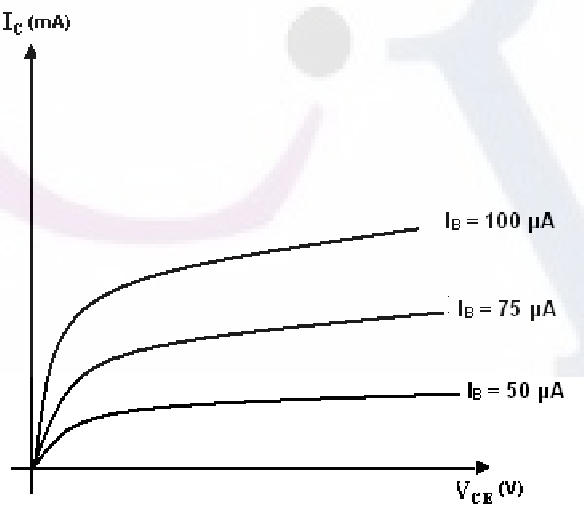
S.NO	I_B = 50 μA		I_B = 75 μA		I_B = 100 μA	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



RESULT: The input and output characteristics of a transistor in CE configuration are drawn

5. HALF WAVE RECTIFIER WITH & WITHOUT FILTER

AIM: To obtain the % regulation and ripple factor of a half wave rectifier with and without filter.

APPARATUS:

AC Supply 12V

PN Diode, 1N4007

Capacitor, 470µF

Variable Resistor (0-10) KΩ

Connecting wires

Breadboard

Multimeter

THEORY:

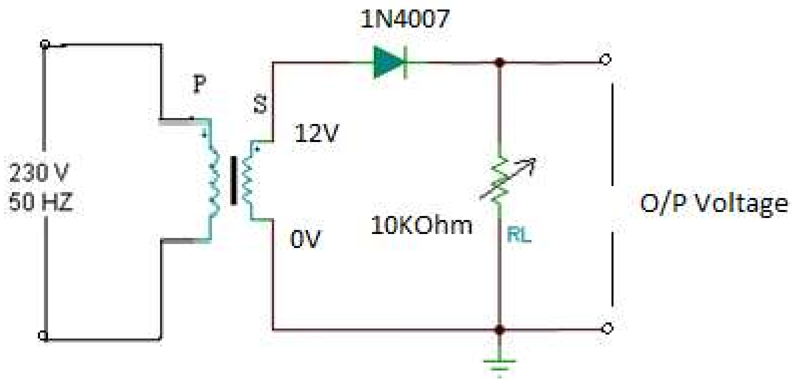
During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage. During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e., the voltage across R1 is zero.

The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter. For practical circuits, transformer coupling is usually provided for two reasons.

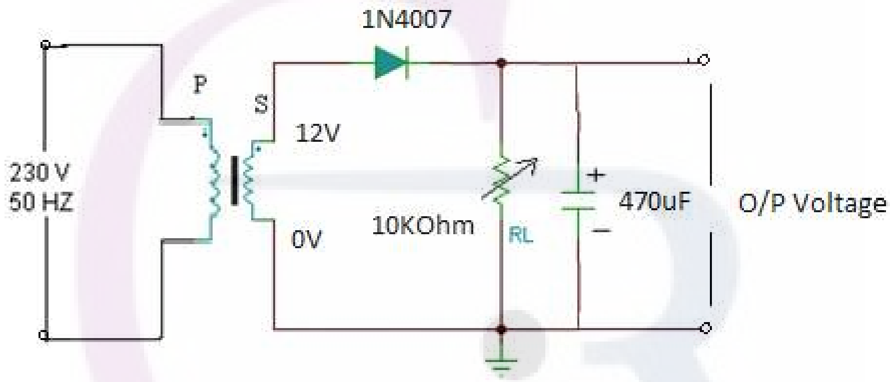
1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

CIRCUIT DIAGRAMS:

WITHOUT FILTER:



WITH FILTER:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Find the theoretical of dc voltage by using the formula,

$$V_{dc}=V_m/\pi$$

Where, V_m=2Vrms, (V_{rms}=output ac voltage.)

The Ripple factor is calculated by using the formula

r=ac output voltage/dc output voltage.

REGULATION CHARACTERSTICS:

1. Connections are made as per the circuit diagram.
2. By increasing the value of the rheostat, the voltage across the load and current flowing through the load are measured.
3. The reading is tabulated.
4. Draw a graph between load voltage (V_L and load current (I_L) taking V_L on X-axis and I_L on y-axis
5. From the value of no-load voltages, the % regulation is calculated using the formula,

OBSERVATIONS:

WITHOUT FILTER:

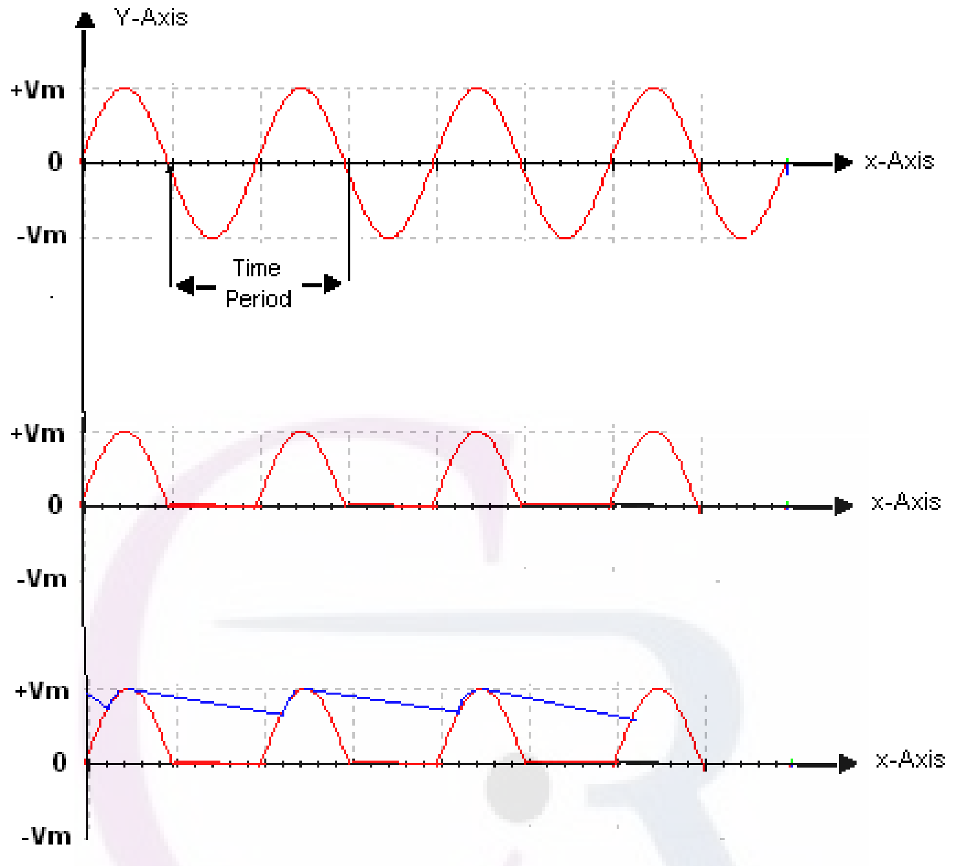
R_L (KΩ)	V_{ac} (Volts)	V_{dc} (Volts)	Ripple Factor $= V_{ac}/ V_{dc}$	% Regulation $(V_{NL}-V_{FL})/V_{FL}$ *100

WITH FILTER:

R_L (KΩ)	V_{ac} (Volts)	V_{dc} (Volts)	Ripple Factor $= V_{ac}/ V_{dc}$	% Regulation $(V_{NL}-V_{FL})/V_{FL}$ *100

MODEL GRAPHS:

HALFWAVE RECTIFIER (WITH & WITHOUT FILTER):



RESULT: The Ripple factor and % regulation for the Half-wave Rectifier with and without filters is measured.

6. FULL WAVE RECTIFIER WITH & WITHOUT FILTER

AIM: To find the Ripple factor and regulation of a Full-wave Rectifier with and without filter.

APPARATUS:

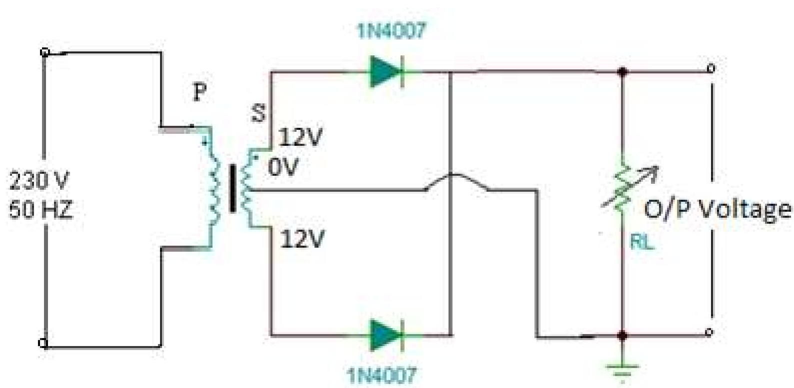
AC Supply (12V-0-12V)
PN Diodes 1N4007
Capacitor 470μF
Connecting Wires
Variable resistor (0-10) KΩ
Breadboard
Multimeter

THEORY:

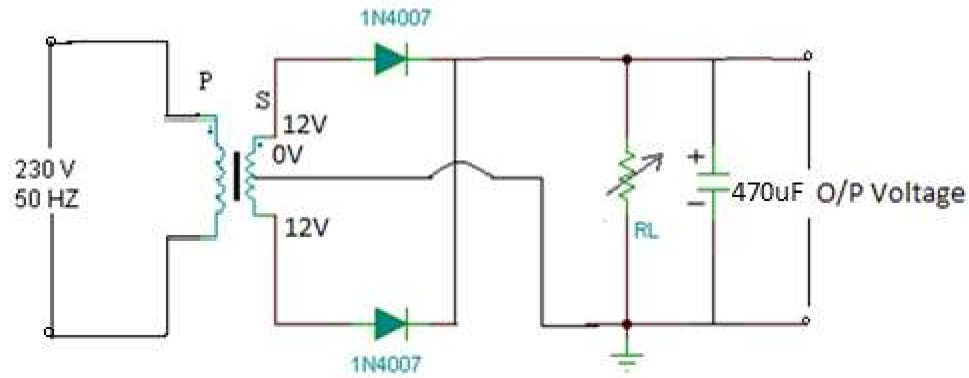
The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased. The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

CIRCUIT DIAGRAM:

WITHOUT FILTER:



WITH FILTER:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the ac mains to the primary side of the transformer and the secondary side to the rectifier.
3. Measure the ac voltage at the input side of the rectifier.
4. Measure both ac and dc voltages at the output side the rectifier.
5. Find the theoretical value of the dc voltage by using the formula $V_{dc}=2V_m/\pi$
6. Connect the filter capacitor across the load resistor and measure the values of V_{ac} and V_{dc} at the output.
7. The theoretical values of Ripple factors with and without capacitor are calculated.
8. From the values of V_{ac} and V_{dc} practical values of Ripple factors are calculated. The practical values are compared with theoretical values.

OBSERVATIONS:

WITHOUT FILTER:

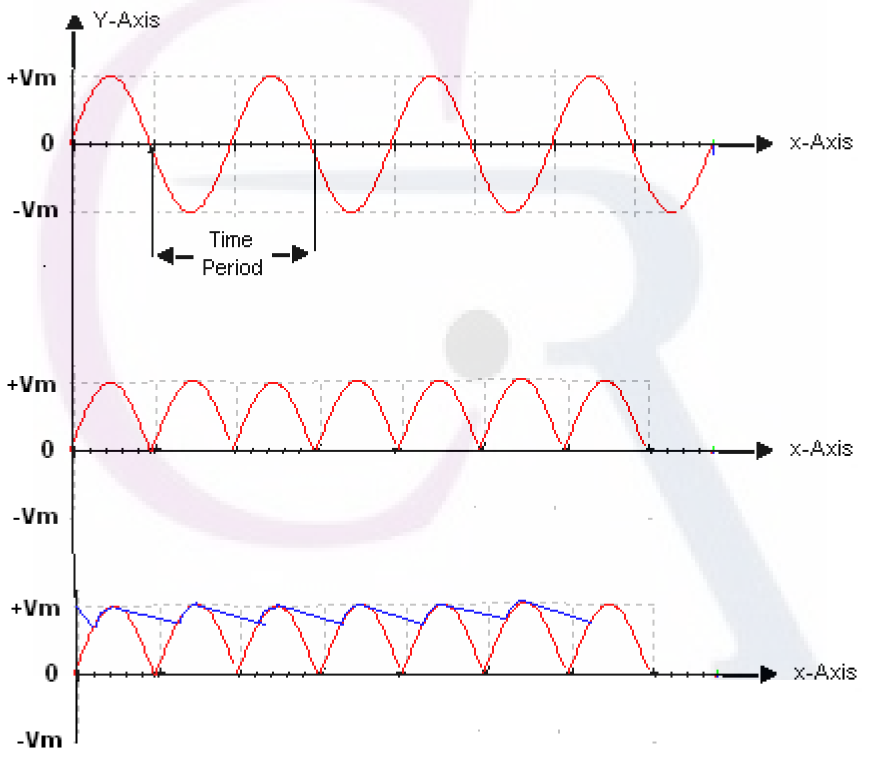
R_L (Ohms)	V_{ac} (Volts)	V_{dc} (Volts)	Ripple Factor $= V_{ac}/ V_{dc}$	% Regulation $(V_{NL}-V_{FL})/V_{FL}$ *100

WITH FILTER:

R_L (Ohms)	V_{ac} (Volts)	V_{dc} (Volts)	Ripple Factor $= V_{ac}/ V_{dc}$	% Regulation $(V_{NL}-V_{FL})/V_{FL}$ *100

MODEL GRAPHS:

FULLWAVE RECTIFIER (WITH & WITHOUT FILTER):



RESULT:

The ripple factor of the Full-wave rectifier (with filter and without filter) is calculated.

7. FET CHARACTERISTICS

AIM: To draw the drain and transfer characteristics of a given FET.

APPARATUS:

JFET (BFW11)

Regulated Power Supply (0-15V)

Voltmeter (0-20V)

Ammeter (0-200mA)

Breadboard

Connecting wires

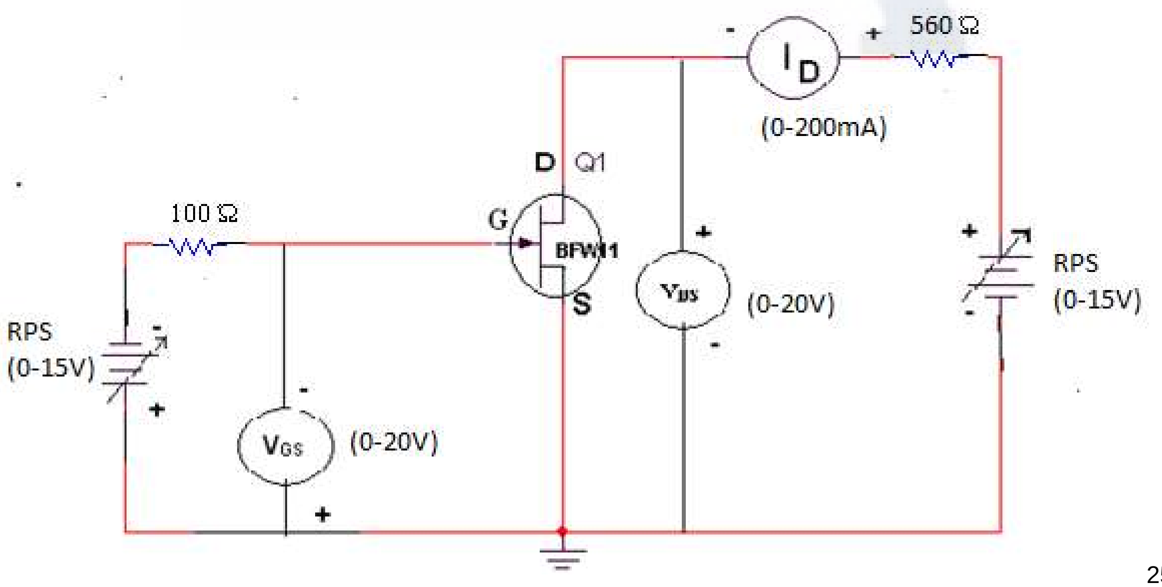
THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with $V_{DS.}$ With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called “pinch of voltage”.

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$$F_{DS} = I_{DSS}(1-V_{GS}/V_P)\text{^}2$$

CIRCUIT DIAGRAM:



PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at 0V.
3. Vary the V_{DD} and observe the values of V_{DS} and I_D.
4. Repeat the above steps 2, 3 for different values of V_{GS} at 0.1V and 0.2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 1V.
7. Vary V_{GG} and observe the values of V_{GS} and I_D.
8. Repeat steps 6 and 7 for different values of V_{DS} at 1.5 V and 2V.
9. The readings are tabulated.

OBSERVATIONS:

DRAIN CHARACTERISTICS:

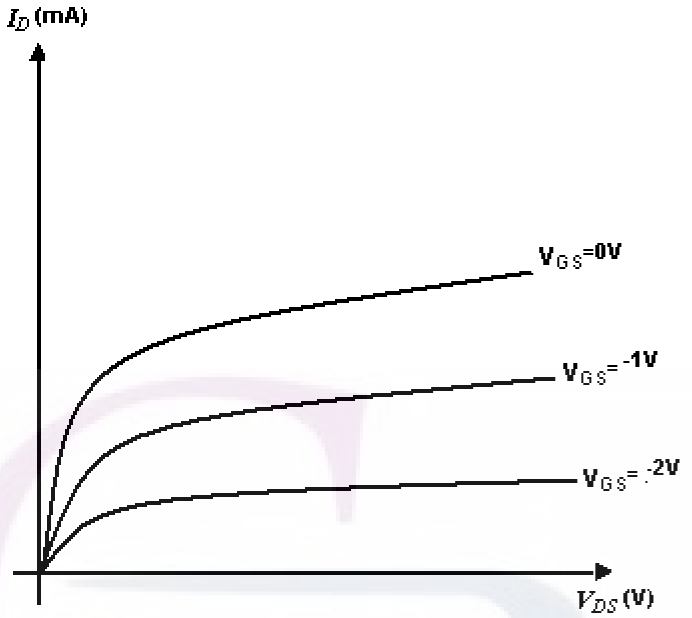
S.NO	V_{GS}=0V		V_{GS}=-1V		V_{GS}=-2V	
	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

TRANSFER CHARACTERISTICS:

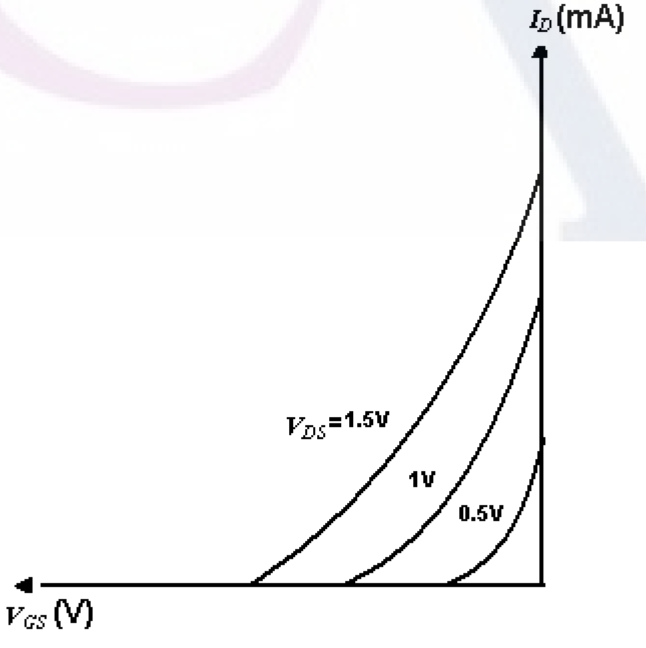
S.NO	V_{DS} =0.5V		V_{DS}=1V		V_{DS} =1.5V	
	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)

MODEL GRAPH:

DRAIN CHARACTERISTICS:



TRANSFER CHARACTERISTICS:



RESULT: The drain and transfer characteristics of a FET are drawn.

8. h-PARAMETERS OF CE CONFIGURATION

AIM: To calculate the h-parameters of a transistor in CE configuration.

APPRATUS:

Transistor BC 107

Resistors 100 K Ώ, 100 Ώ

Ammeter (0-200µA), (0-200mA)

Voltmeter (0-20V) - 2Nos

Regulated Power Supply (0-30V, 1A) - 2Nos

Breadboard

THEORY:

INPUT CHARACTERISTICS:

The two sets of characteristics are necessary to describe the behavior of the CE configuration one for input or base emitter circuit and other for the output or collector emitter circuit.

In input characteristics the emitter base junction forward biased by a very small voltage V_{BB} whereas collector base junction reverse biased by a very large voltage V_{CC}. The input characteristics are a plot of input current I_B V_s the input voltage V_{BE} for a range of values of output voltage V_{CE}. The following important points can be observed from these characteristics curves.

1. The characteristics resemble that of CE configuration.
2. Input resistance is high as I_B increases less rapidly with V_{BE}
3. The input resistance of the transistor is the ratio of change in base emitter voltage ΔV_{BE} to change in base current ΔI_B at constant collector emitter voltage (V_{CE}) i.e... Input resistance or input impedance hie = ΔV_{BE} / ΔI_B at V_{CE} constant.

OUTPUT CHARACTERISTICS:

A set of output characteristics or collector characteristics are a plot of out put current I_C V_S output voltage V_{CE} for a range of values of input current I_B .The following important points can be observed from these characteristics curves:-

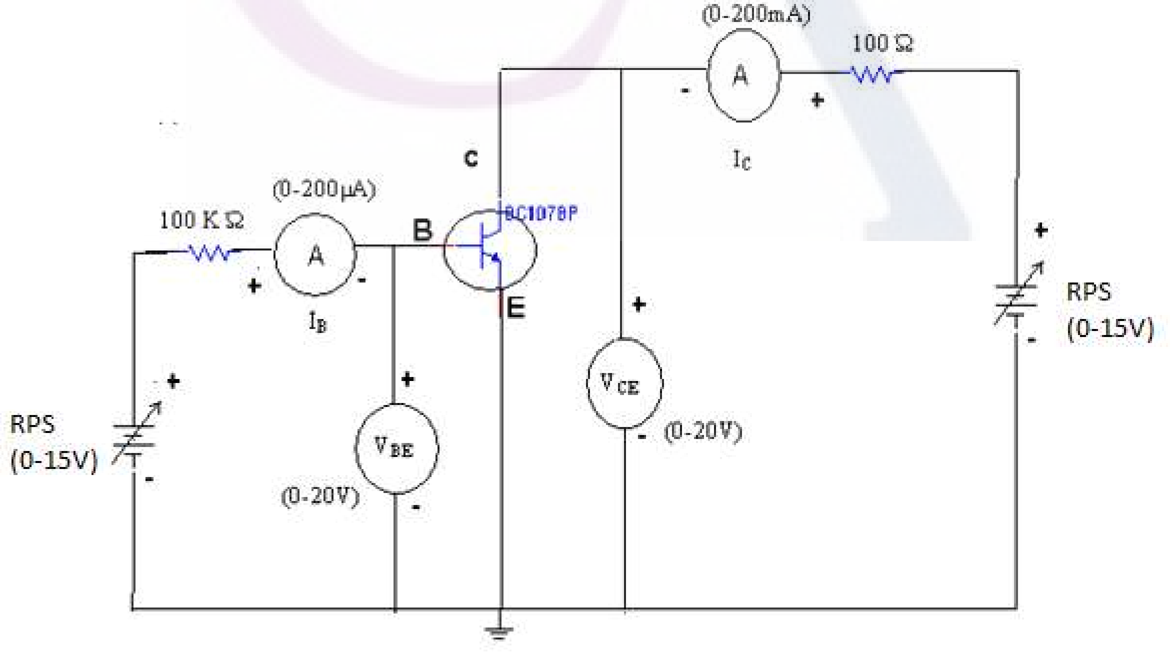
The transistor always operates in the active region. I.e. the collector current

I_C increases with V_{CE} very slowly. For low values of the V_{CE} the I_C increases rapidly with a small increase in V_{CE} .The transistor is said to be working in saturation region.

Output resistance is the ratio of change of collector emitter voltage ΔV_{CE} , to change in collector current ΔI_C with constant I_B. Output resistance or Output impedance hoe = $\Delta V_{CE} / \Delta I_C$ at I_B constant.

1. Input Impedance hie = $\Delta V_{BE} / \Delta I_B$ at V_{CE} constant
2. Output impedance hoe = $\Delta V_{CE} / \Delta I_C$ at I_B constant
3. Reverse Transfer Voltage Gain hre = $\Delta V_{BE} / \Delta V_{CE}$ at I_B constant
4. Forward Transfer Current Gain hfe = $\Delta I_C / \Delta I_B$ at constant V_{CE}

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect a transistor in CE configuration circuit for plotting its input and output characteristics.
2. Take a set of readings for the variations in I_B with V_{BE} at different fixed values of output voltage V_{CE}.
3. Plot the input characteristics of CE configuration from the above readings.
4. From the graph calculate the input resistance h_{ie} and reverse transfer ratio h_{re} by taking the slopes of the curves.
5. Take the family of readings for the variations of I_C with V_{CE} at different values of fixed I_B.
6. Plot the output characteristics from the above readings.
7. From the graphs calculate h_{fe} and h_{oe} by taking the slope of the curves.

TABULAR FORMS:

INPUT CHARACTERISTICS:

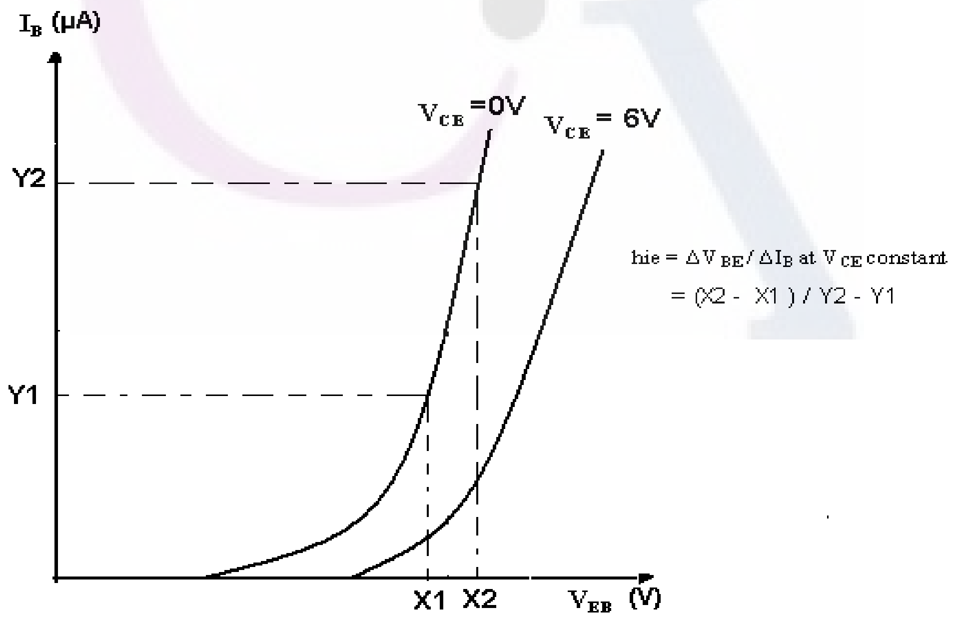
S.NO	V_{CE}=0V		V_{CE}=6V	
	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

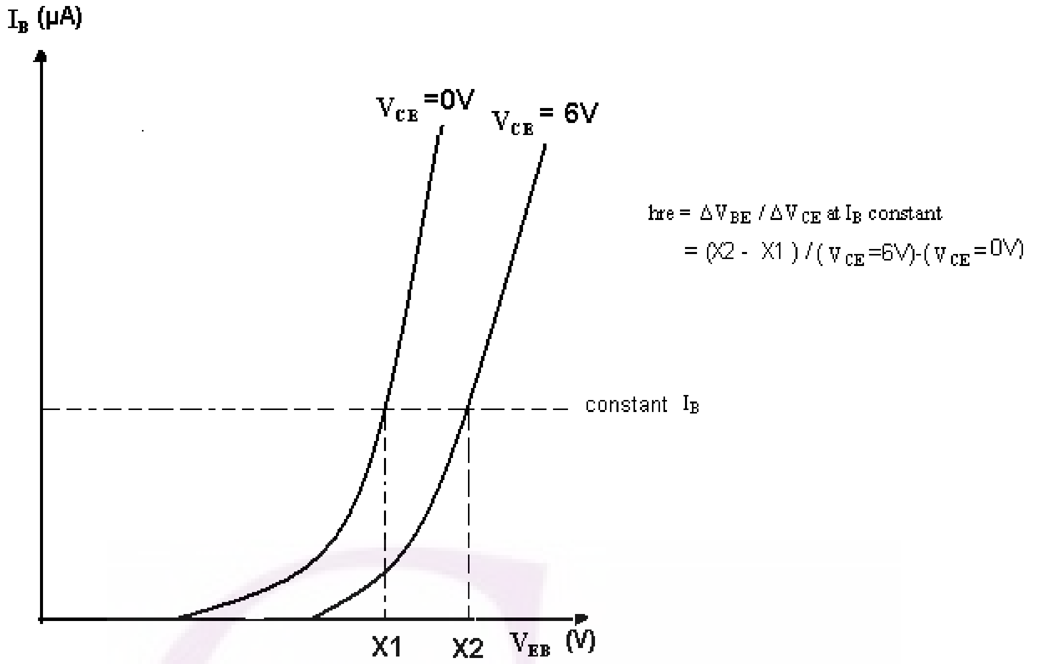
OUTPUT CHARACTERISTICS:

S.NO	$I_B = 20\ \mu A$		$I_B = 40\ \mu A$		$I_B = 60\ \mu A$	
	V_{CE} (V)	I_C(mA)	V_{CE} (V)	I_C(mA)	V_{CE} (V)	I_C(mA)

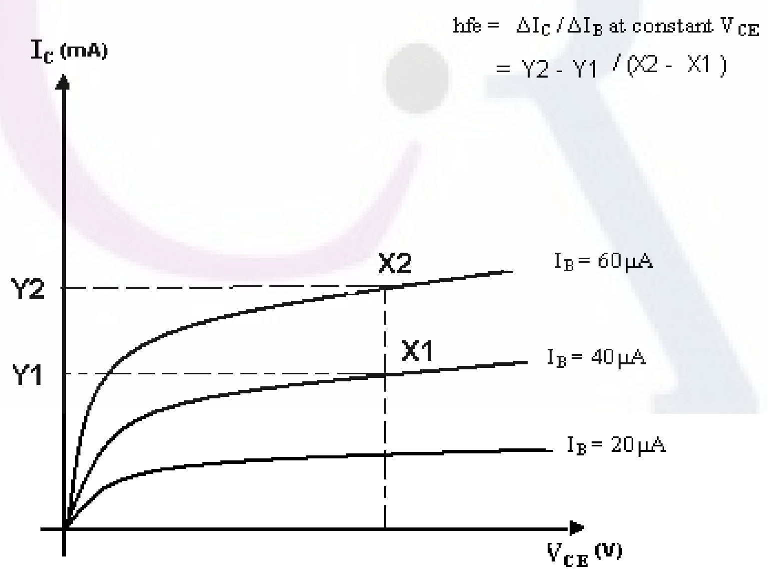
MODEL GRAPHS:

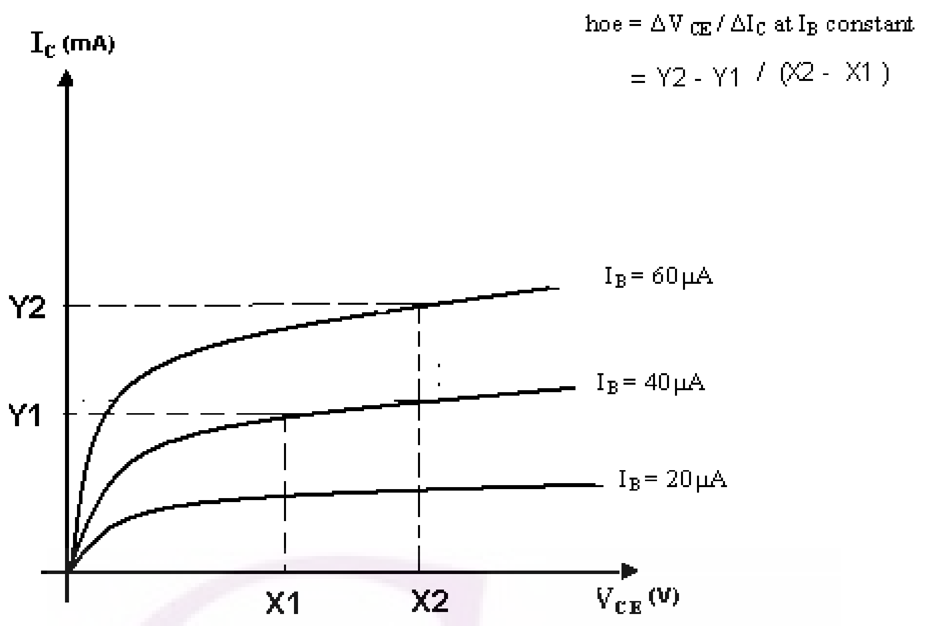
INPUT CHARACTERISTICS:





OUTPUT CHARACTERISTICS:





RESULT:

The H-Parameters for a transistor in CE configuration are calculated from the input and output characteristics.

1. Input Impedance h_{ie} =
2. Reverse Transfer Voltage Gain h_{re} =
3. Forward Transfer Current Gain h_{fe} =
4. Output conductance h_{oe} =

9. TRANSISTOR CE AMPLIFIER

AIM:

a. To Measure the voltage gain of a CE amplifier
b. To draw the frequency response curve of the CE amplifier

APPARATUS:

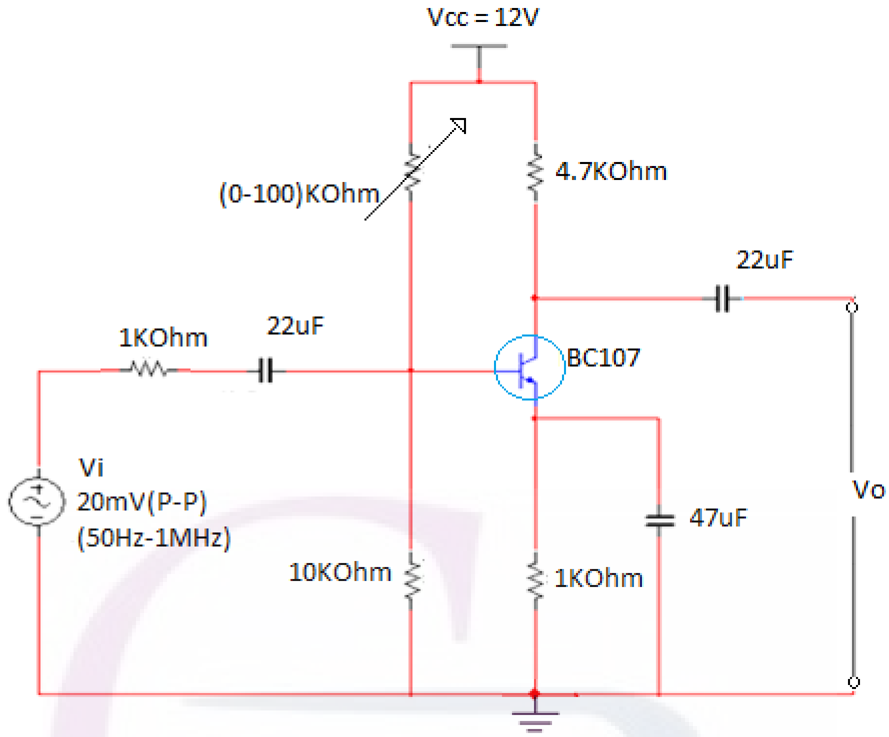
Transistor BC107
Regulated Power Supply (0-15V)
Function Generator
CRO
Resistors - 10KΩ, 1KΩ, 4.7KΩ
Variable Resistor – 100KΩ
Capacitors 22µF, 47µF
Breadboard
Connecting Wires

THEORY:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current.

When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in circuit diagram
2. Apply the input of 20mV peak-to-peak and 50Hz frequency using function generator.
3. Measure the Output Voltage V_O (p-p).
4. Tabulate the readings in the tabular form.
5. The voltage gain can be calculated by using the expression $A_v = (V_0/V_i)$
6. For plotting the frequency response the input voltage is kept Constant at 20mV peak-to-peak and the frequency is varied from 50Hz to 1MHz Using function generator.
7. All the readings are tabulated and voltage gain in dB is calculated by using the expression $A_v = 20 \log_{10} (V_0/V_i)$
8. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis on Semi-log graph.

The band width of the amplifier is calculated from the graph using the expression,

Bandwidth, $BW = f_2 - f_1$

Where f_1 lower cut-off frequency of CE amplifier, and

Where f_2 upper cut-off frequency of CE amplifier

The bandwidth product of the amplifier is calculated using the expression

Gain Bandwidth product = (3dB mid-band gain) X (Bandwidth)

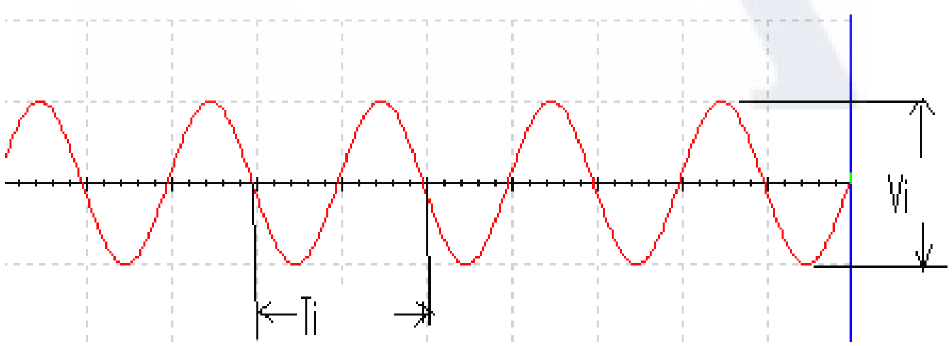
OBSERVATIONS:

FREQUENCY RESPONSE:

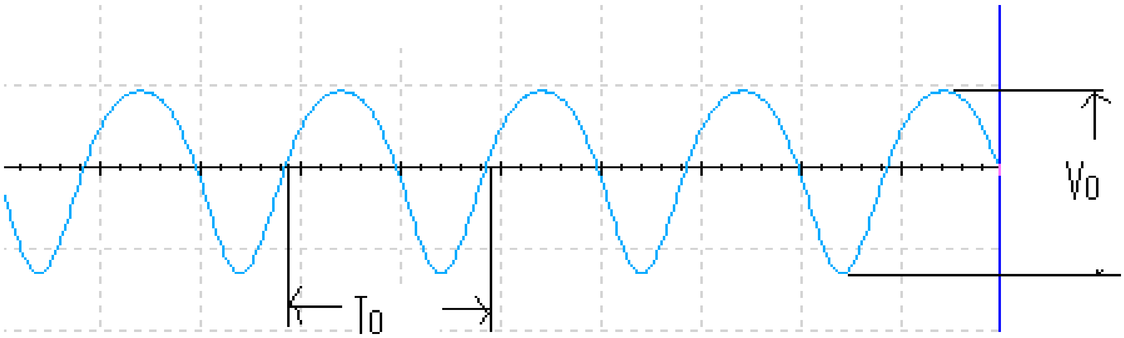
Frequency (Hz)	Input voltage (v_i)	Output voltage (v_0)	Gain in dB $A_v = 20 \log_{10} (v_0/v_i)$

MODEL WAVEFORMS:

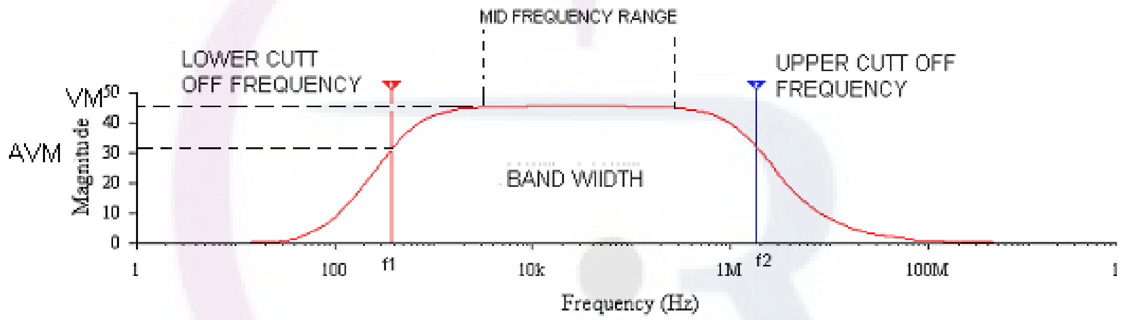
INPUT WAVEFORM:



OUTPUT WAVEFORM:



FREQUENCY RESPONSE:



RESULT:

The voltage gain and frequency response of the CE amplifier are obtained. Also gain bandwidth product of the amplifier is calculated.

9. TRANSISTOR CC AMPLIFIER

AIM:

a. To measure the voltage gain of a CC amplifier
b. To draw the frequency response of the CC amplifier

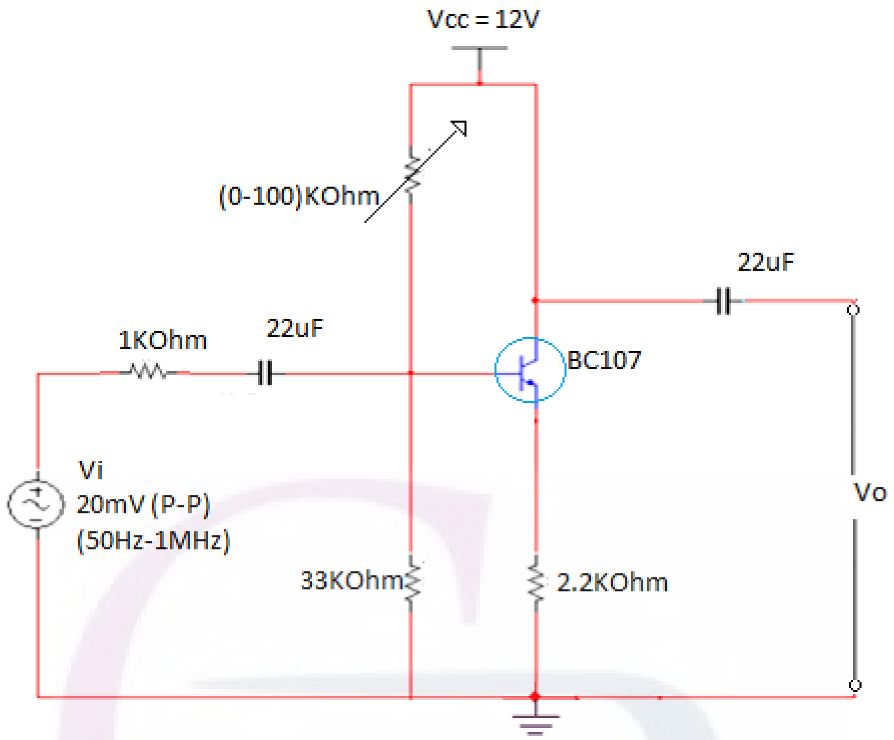
APPRATUS:

Transistor BC107
Regulated Power Supply (0-15V)
Function Generator
CRO
Resistors - 1KΩ, 33KΩ, 2.2KΩ
Variable Resistor – (0-100) KΩ
Capacitors - 22µF
Breadboard
Connecting wires

THEORY:

In common-collector amplifier the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation. This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as emitter follower.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in circuit diagram
2. Apply the input of 20mV peak-to-peak and 50Hz frequency using function generator.
3. Measure the Output Voltage V_O (p-p).
4. Tabulate the readings in the tabular form.
5. The voltage gain can be calculated by using the expression $A_v = (V_0/V_i)$
6. For plotting the frequency response the input voltage is kept Constant at 20mV peak-to-peak and the frequency is varied from 50Hz to 1MHz Using function generator.
7. All the readings are tabulated and voltage gain in dB is calculated by using the expression $A_v = 20 \log_{10} (V_0/V_i)$
8. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis on Semi-log graph.

The Bandwidth of the amplifier is calculated from the graph using the expression,

Bandwidth $BW = f_2 - f_1$

Where f_1 is lower cut-off frequency of CC amplifier

f_2 is upper cut-off frequency of CC amplifier

The gain Bandwidth product of the amplifier is calculated using the expression,

Gain -Bandwidth product = (3dB mid-band gain) X (Bandwidth)

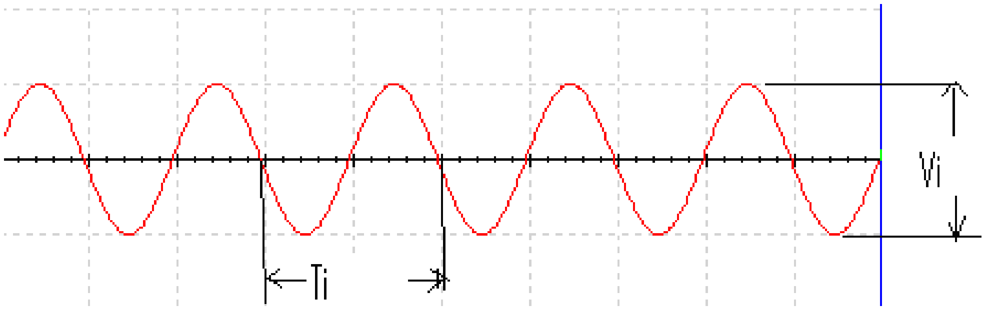
OBSERVATIONS:

FREQUENCY RESPONSE:

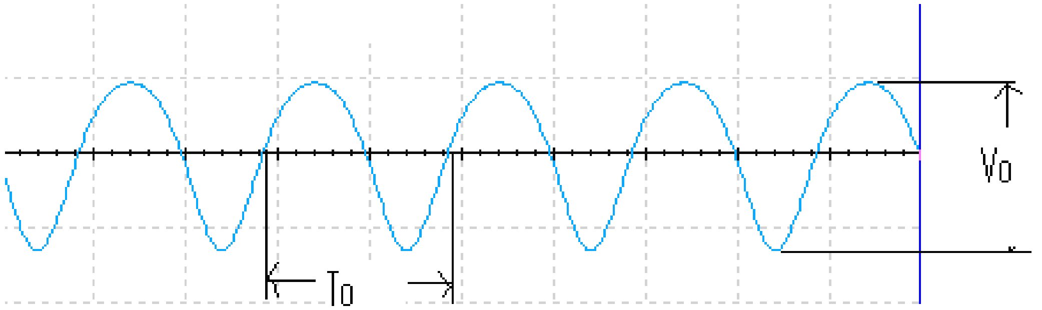
Frequency (Hz)	Input Voltage (V_i)	Output Voltage (V_0)	Gain in dB $A_v = 20*\log_{10}(V_o/V_i)$

MODEL WAVEFORMS:

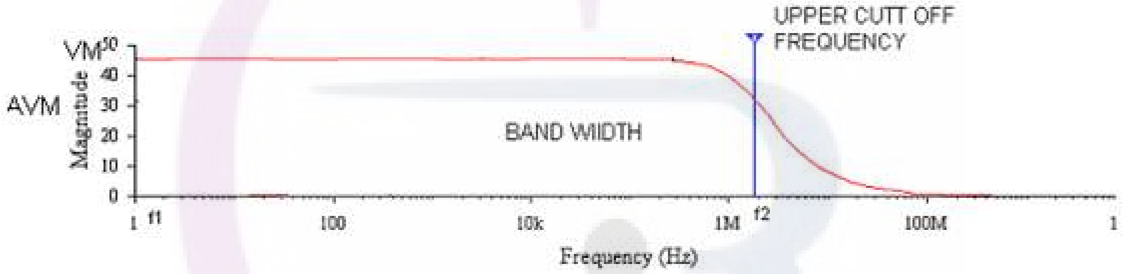
INPUT WAVEFORM:



OUTPUT WAVEFORM:



FREQUENCY RESPONSE:



RESULT:

The voltage gain and frequency response of the CC amplifier are obtained. Also gain Bandwidth product is calculated.

11. COMMON SOURCE (FET) AMPLIFIER

AIM: To find the frequency response and bandwidth of agiven single stage FET amplifier.

APPARATUS:

JFET - BFW11

Resistors - 1 KΩ, 10 KΩ, 10 KΩ, 470 Ω

Capacitors - 1 μ F, 0.01 μ F, 47μ F/40V

Regulated Power Supply – (0-15V)

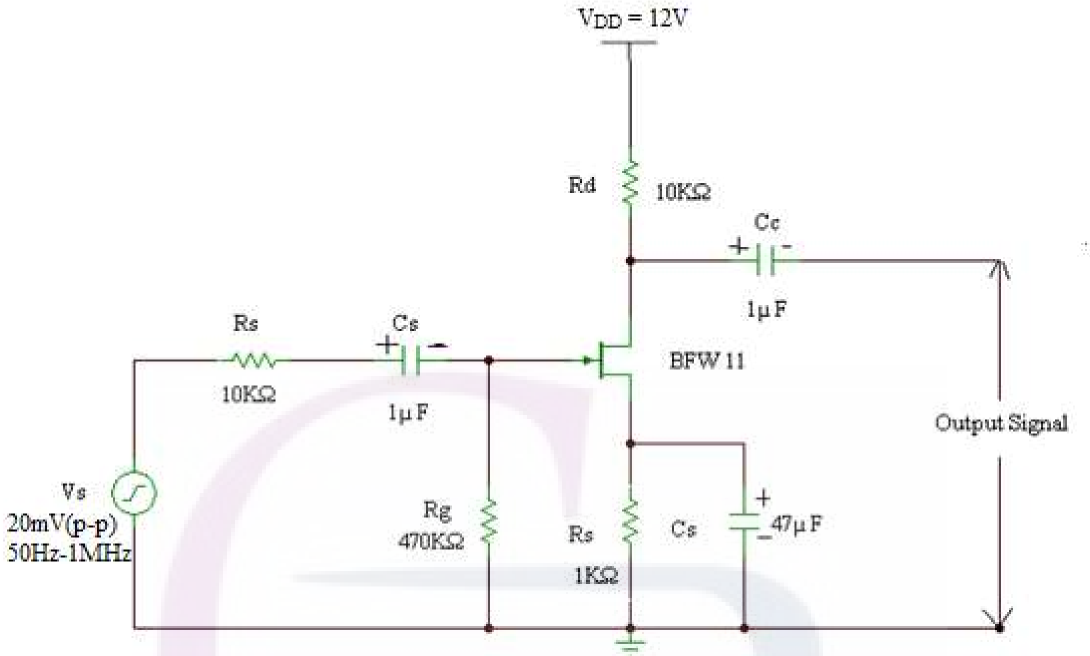
Signal Generator

CRO

THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide- semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle. The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

CIRCUIT DIAGRAM:



PROCEDURE:

1. As per the design specifications, connect the circuit as shown.
2. Set the frequency of I/P signal at 5 KHz and increase the amplitude, till O/P gets distorted. The value of I/P signal is maximum signal handling capacity.
3. Set I/P signal at a constant value, less than the maximum signal handling capacity, vary frequency in the range 50Hz to 1MHz and find O/P voltage for each and every frequency.
4. Calculate voltage gain at each and every frequency.
5. Plot the frequency versus gain and determine f_H and f_L.
6. Calculate bandwidth $f_H - f_L$.
7. Procedure for measuring input impedance: Set the signal generator frequency at 2KHz and measure V_s and V_i. Then $I_i = V_s - V_i \;/ R_S$.

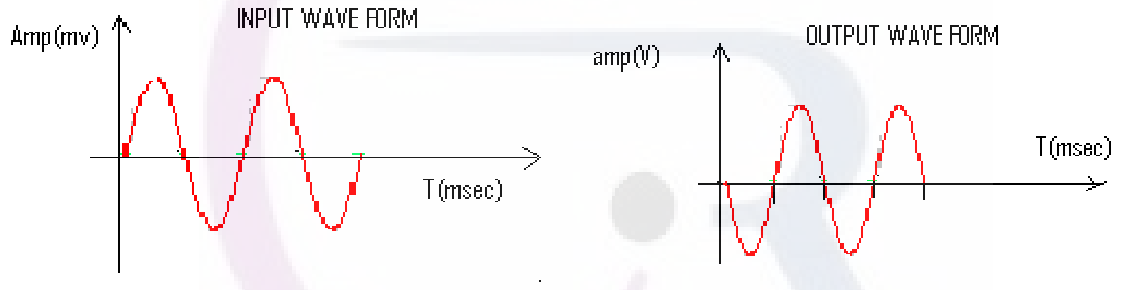
   I/P impedance = V_i / I_i
8. Procedure for measuring O/P impedance: Open the O/P circuit and measure voltage (V open) across O/P using CRO. After connecting variable resistor at O/P terminals, vary the resistance to make the O/P (V open) become to half of its value. Then

existing resistance is its O/P resistance.

OBSERVATIONS:

S. No	Frequency (Hz)	O/P voltage (V_0)	Gain (V_0/ V_I)	Gain in dB $20*\log_{10}(V_0 / V_I)$

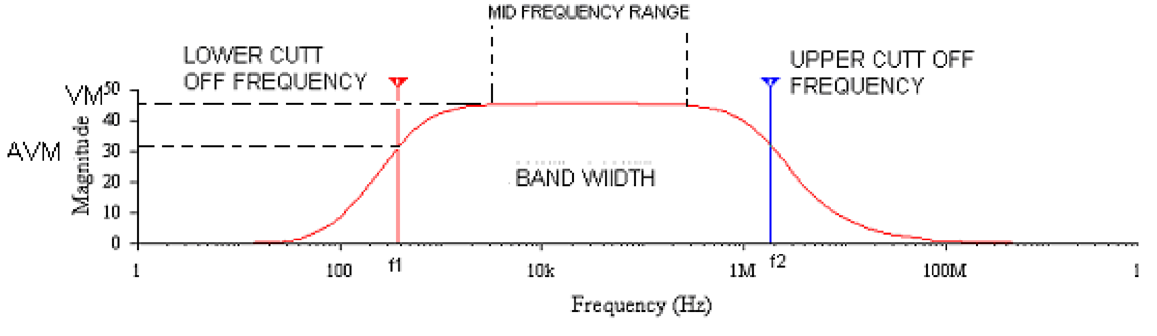
MODEL WAVEFORMS:



FREQUENCY PLOT:

A graph is plotted between f on X – axis and $20*\log_{10} (V_0 / V_I)$ on Y-axis on a semi-log sheet. It will be as shown in figure.

$BW = f_H - f_L$



RESULT: The frequency response curve for a common source FET Amplifier is plotted and its bandwidth is obtained.

12. SILICON CONTROLLED RECTIFIER (SCR) CHARACTERISTICS

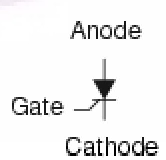
AIM: To draw the V-I Characteristics of SCR

APPARATUS:

SCR - TYN616
Regulated Power Supply (0-15V)
Resistors 10kΩ, 1kΩ
Ammeter (0-200) mA
Voltmeter (0-20V)
Bread Board
Connecting Wires

THEORY:

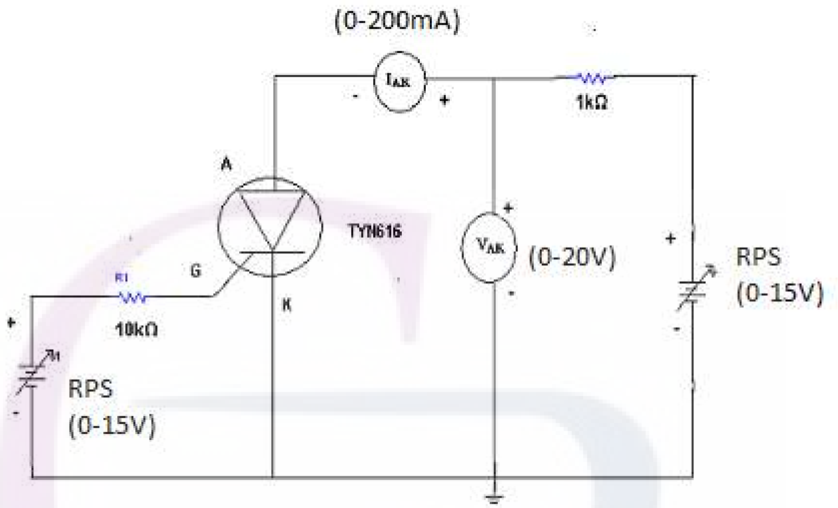
It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J_1, J_2, J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.



Schematic symbol

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cutt off. When anode voltage is increased J_2 tends to breakdown. When the gate positive, with respect to cathode J_3 junction is forward biased and J_2 is reverse biased .Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J_2 break down and SCR conducts heavily. When gate is open thee break-over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

CIRCUIT DIAGRAM:



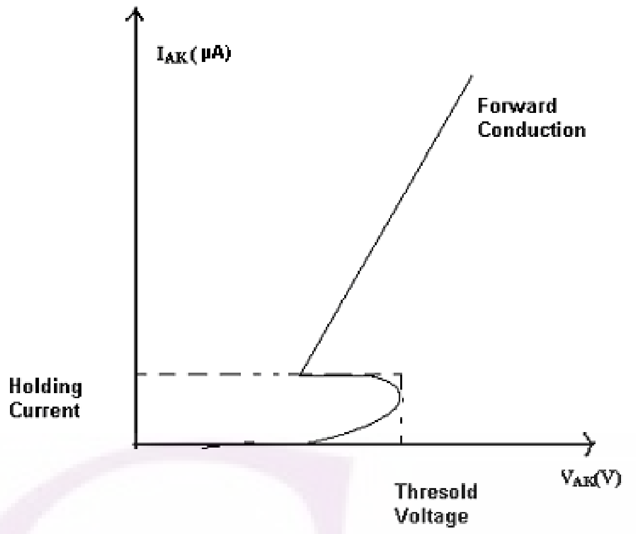
PROCEDURE:

1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter. Keep the gate voltage at standard value.
4. A graph is drawn between V_{AK} and I_{AK}.

OBSERVATIONS:

S.No	V_{AK}(V)	I_{AK} (μA)

MODEL GRAPH:



RESULT:

SCR Characteristics are observed.

13. UJT CHARACTERISTICS

AIM: To observe the characteristics of UJT and to find the negative resistance region.

APPARATUS:

Regulated Power Supply (0-15V)

UJT 2N2646

Resistors 10kΩ, 47Ω, 330Ω

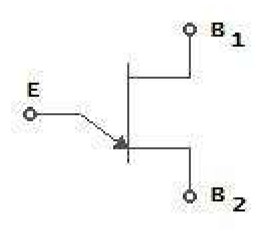
Multimeter

Breadboard

Connecting Wires

THEORY:

A Uni-junction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Uni-junction Transistor (UJT) has three terminals, an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called inter-base resistance. The original uni-junction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.

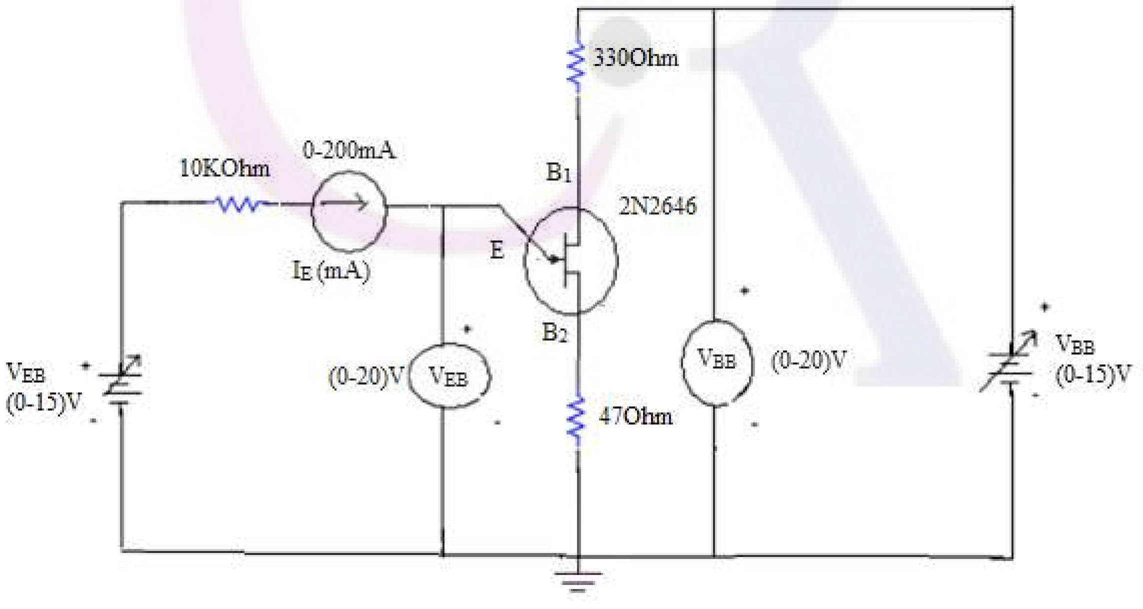


Circuit symbol

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal.

This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches V_p, the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point; R_{B1} reaches minimum value and this region, V_{EB} proportional to $I_{E.}$

CIRCUIT DIAGRAM:

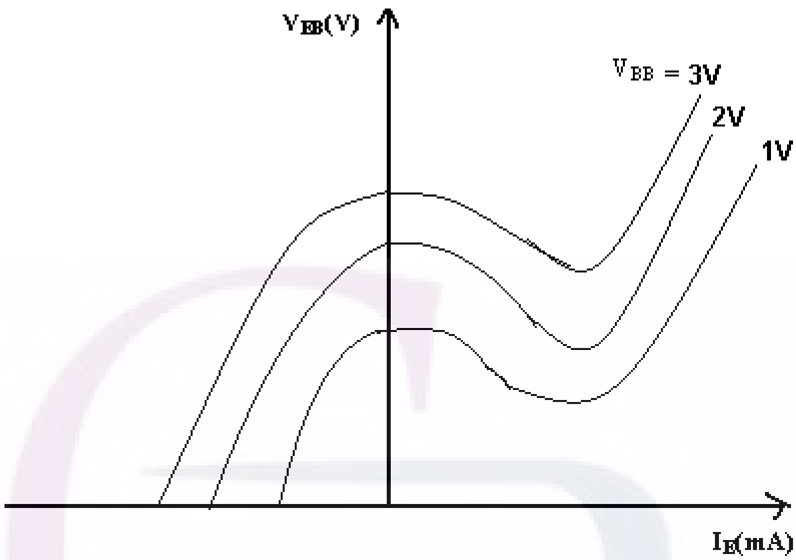


PROCEDURE:

1. Connection is made as per circuit diagram.
2. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.

3. This procedure is repeated for different values of output voltages.
4. All the readings are tabulated and a graph is plotted between V_{EE} and I_E for different values of $V_{BE.}$

MODEL GRAPH:



OBSEVATIONS:

S.No	V_{BB}=1V		V_{BB}=2V		V_{BB}=3V	
	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

RESULT:

The characteristics of UJT are observed and the values of Intrinsic Stand-Off Ratio are calculated.

14. RC COUPLED AMPLIFIER

AIM:

1. To calculate voltage gain,
2. To observe frequency response.

APPARATUS:

NPN Transistor BC107

Resistors - 3.3KΩ, 33KΩ, 330Ω, 1KΩ

Capacitors - 100uF, 10uF

Bread Board,

Regulated power supply (0-15V),

CRO

THEORY:

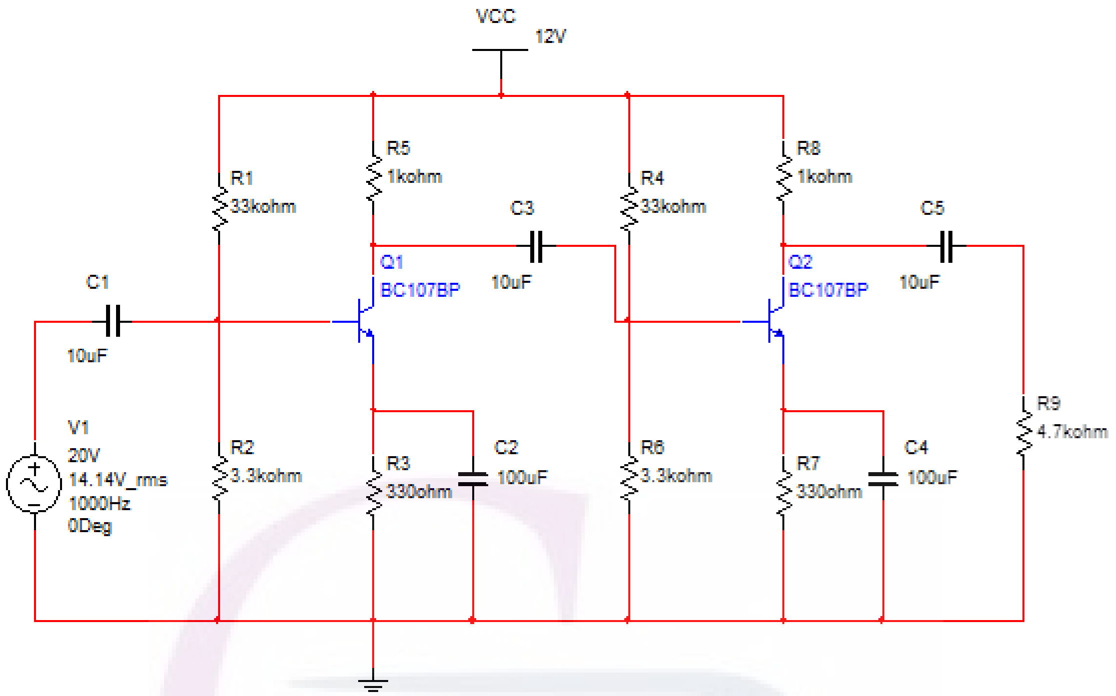
This is most popular type of coupling as it provides excellent audio fidelity. A coupling capacitor is used to connect output of first stage to input of second stage. Resistances R_1, R_2, R_E form biasing and stabilization network. Emitter bypass capacitor offers low reactance paths to signal coupling Capacitor transmits ac signal, blocks DC. Cascade stages amplify signal and overall gain is increased total gain is less than product of gains of individual stages. Thus for more gain coupling is done and overall gain of two stages equals to $A = A_1 * A_2$

A_1 = voltage gain of first stage

A_2 = voltage gain of second stage.

When ac signal is applied to the base of the transistor, its amplified output appears across the collector resistor R_C. It is given to the second stage for further amplification and signal appears with more strength. Frequency response curve is obtained by plotting a graph between frequency and gain in dB .The gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. The gain decreases in the low frequency range due to coupling capacitor C_C and at high frequencies due to junction capacitance C_{BE}.

CIRCUIT DIAGRAM:



PROCEDURE:

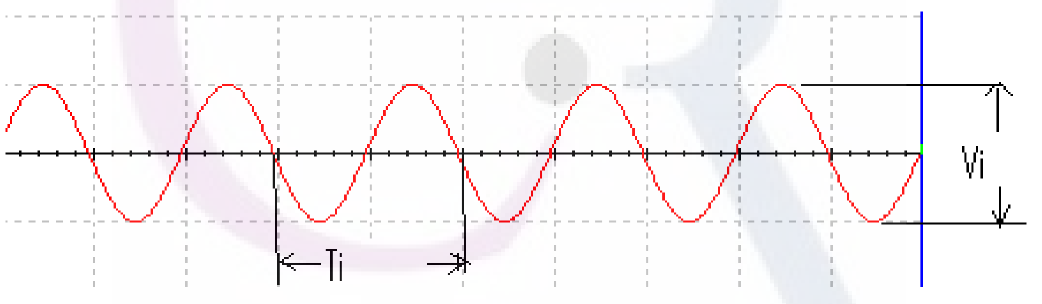
1. Apply input by using function generator to the circuit.
2. Observe the output waveform on CRO.
3. Measure the voltage at
   a. Output of first stage
   b. Output of second stage.
4. From the readings calculate voltage gain of first stage, second stage and overall gain of two stages. Disconnect second stage and then measure output voltage of first stage and calculate voltage gain.
5. Compare it with voltage gain obtained when second stage was connected.
6. Note down various values of gain for different frequencies.
7. A graph is plotted between frequency and voltage gain.

OBSERVATIONS:

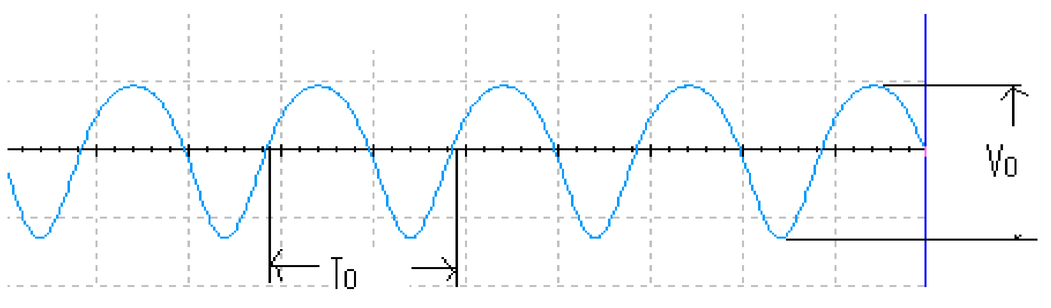
Frequency (Hz)	I/P Voltage (V_i)	O/P Voltage (V_o)	Voltage Gain $A_V = 20 \log_{10}(V_o/V_i)$ dB

MODEL WAVEFORMS:

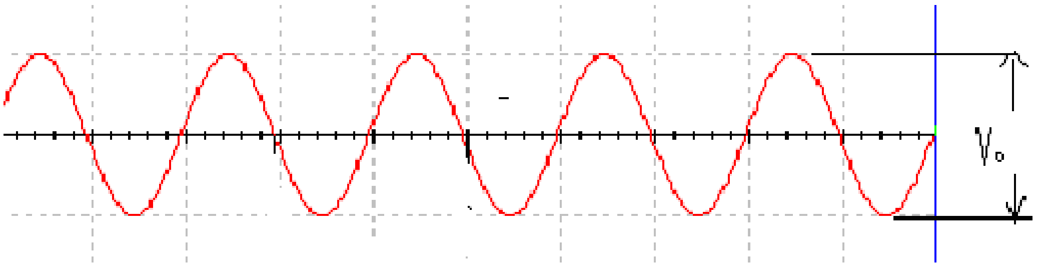
INPUT WAVEFORM:



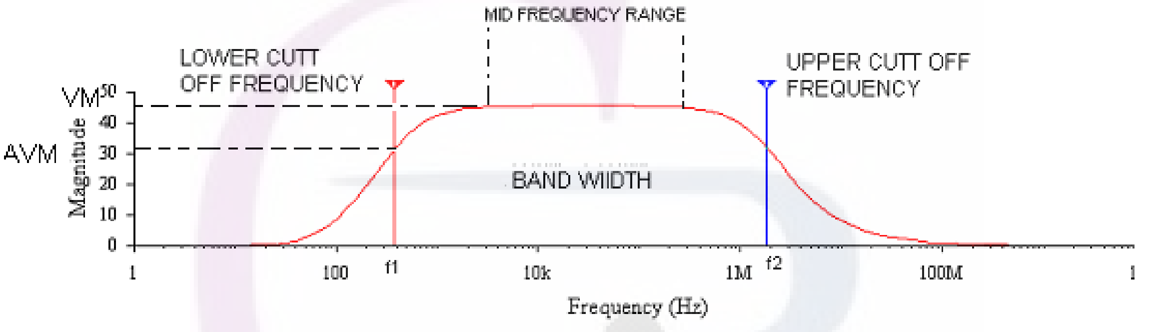
FIRST STAGE OUTPUT:



SECOND STAGE OUTPUT:



FREQUENCY RESPONSE:



RESULT:

Thus voltage gain is calculated and frequency response is observed along with loading affect.

15. RC PHASE SHIFT OSCILLATOR

AIM: To calculate the frequency of the RC phase shift oscillator & to measure the phase angles at different RC sections.

APPARATUS:

Transistor BC107

Resistors - 10KΩ, 8KΩ or 10KΩ, 22KΩ, 1.2KΩ, 100KΩ

Capacitors - 0.001µf, 10µF, 1µf

Regulated power Supply – (0-15V)

CRO

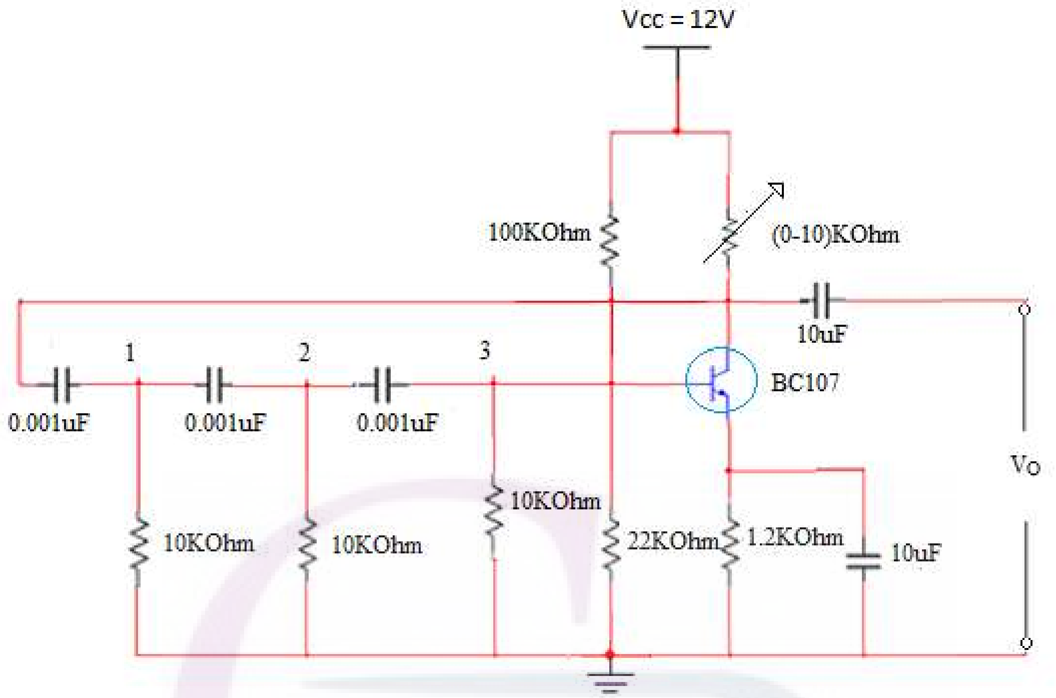
THEORY:

RC-Phase shift Oscillator has a CE amplifier followed by three sections of RC phase shift feedback Networks the output of the last stage is return to the input of the amplifier. The values of R and C are chosen such that the phase shift of each RC section is 60º.Thus The RC ladder network produces a total phase shift of 180º between its input and output voltage for the given frequencies.

Since CE Amplifier produces 180 º phases shift the total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360º or 0º. This satisfies the Barkhausen condition for sustaining oscillations and total loop gain of this circuit is greater than or equal to 1, this condition used to generate the sinusoidal oscillations. The frequency of oscillations of RC-Phase Shift Oscillator is,

$$f = 1/2\pi RC * \sqrt{6}$$

CIRCUIT DIAGRAM:



PROCEDURE:

1. Make the connection as per the circuit diagram as shown above.
2. Observe the output signal and note down the output amplitude and time period (T_d).
3. Calculate the frequency of oscillations theoretically and verify it practically ($f=1/T_d$).
4. Calculate the phase shift at each RC section by measuring the time shifts (T_p) between the final waveform and the waveform at that section by using the below formula.

OBSERVATIONS:

THEORITICAL CALCULATIONS:

.

R = 10KΩ, C = 0.001 μf

$$f = 1/2\pi RC * \sqrt{6} =$$

PRACTICAL CALCULATIONS:

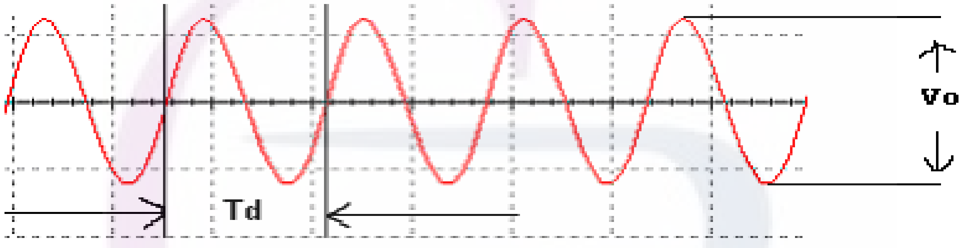
$T_d =$

$f = 1/T_d$

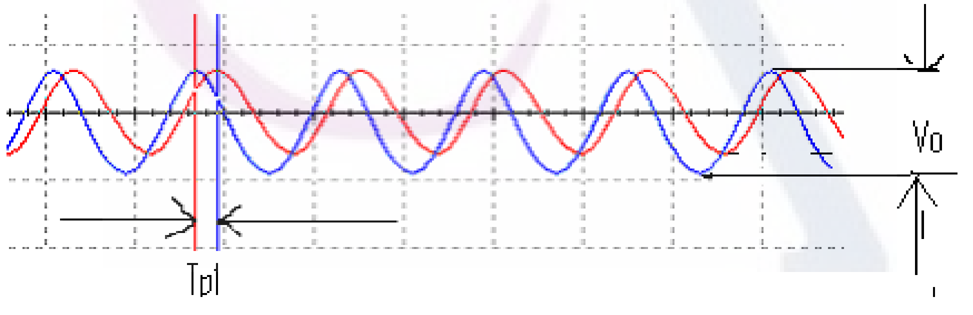
1) $\theta_1 = T_{p1}/T_d * 360° =$
2) $\theta_2 = T_{p2}/T_d * 360° =$
3) $\theta_3 = T_{p3}/T_d * 360° =$

MODEL WAVE FORMS:

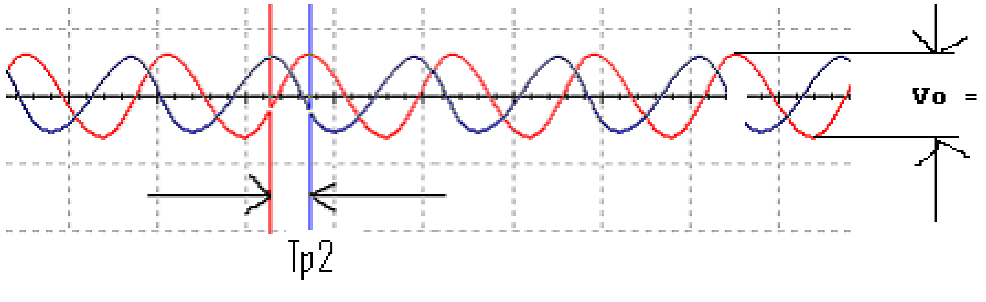
OUT PUT WAVEFORM:



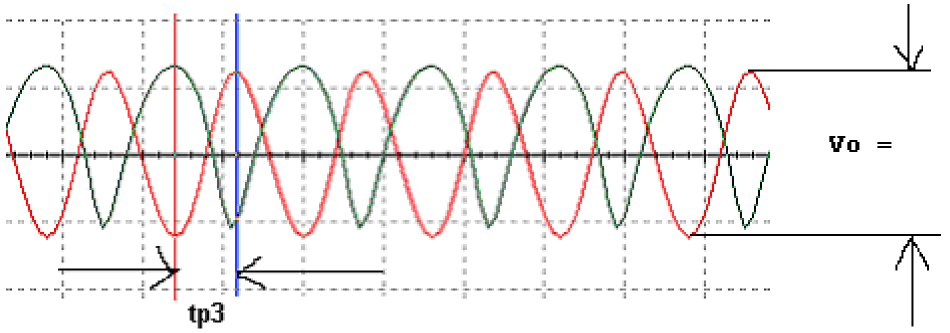
OUT PUT WAVEFORM: $\theta = 60^0$



OUT PUT WAVEFORM: $\theta = 120^0$



OUT PUT WAVEFORM: $\theta = 180^0$



RESULT:

The frequency of RC phase shift oscillator is calculated and the phase shift at different RC sections is noted.

16. BRIDGE RECTIFER

AIM: To calculate the ripple factor of a bridge rectifier, with and without filters.

APPARATUS:

Breadboard

Diodes, 1N4007

Variable Resistor, (0-10) KΩ

Capacitor 470µF

Multimeter

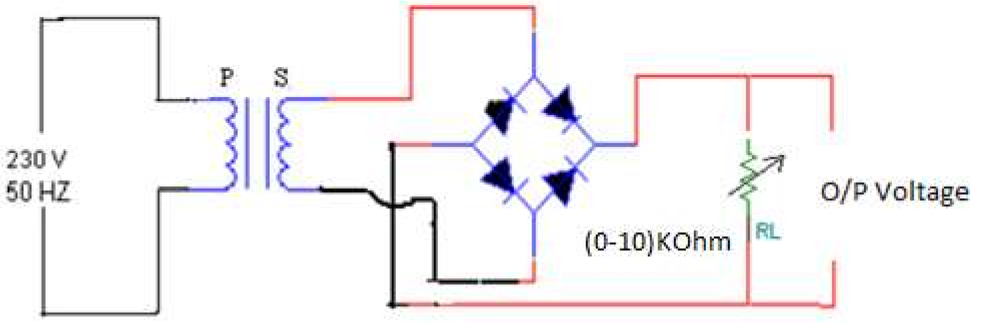
Connecting Wires

THEORY:

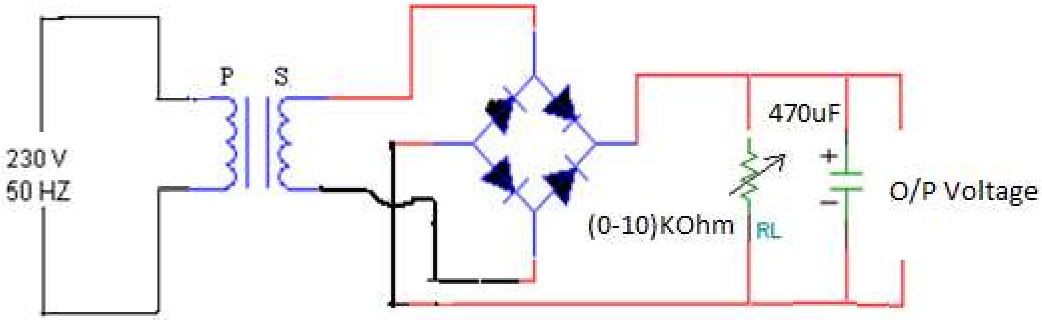
The bridge rectifier is also a full-wave rectifier in which four p-n diodes are connected in the form of a bridge fashion. The Bridge rectifier has high efficiency when compared to half-wave rectifier. During every half cycle of the input, only two diodes will be conducting while other two diodes are in reverse bias.

CIRCUIT DIAGRAM:

WITHOUT FILTER:



WITH FILTER:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the ac main to the primary side of the transformer and secondary side to the bridge rectifier.
3. Measure the ac voltage at the input of the rectifier using the multi meter.
4. Measure both the ac and dc voltages at the output of the Bridge rectifier.
5. Find the theoretical value of dc voltage by using the formula.

OBSERVATIONS:

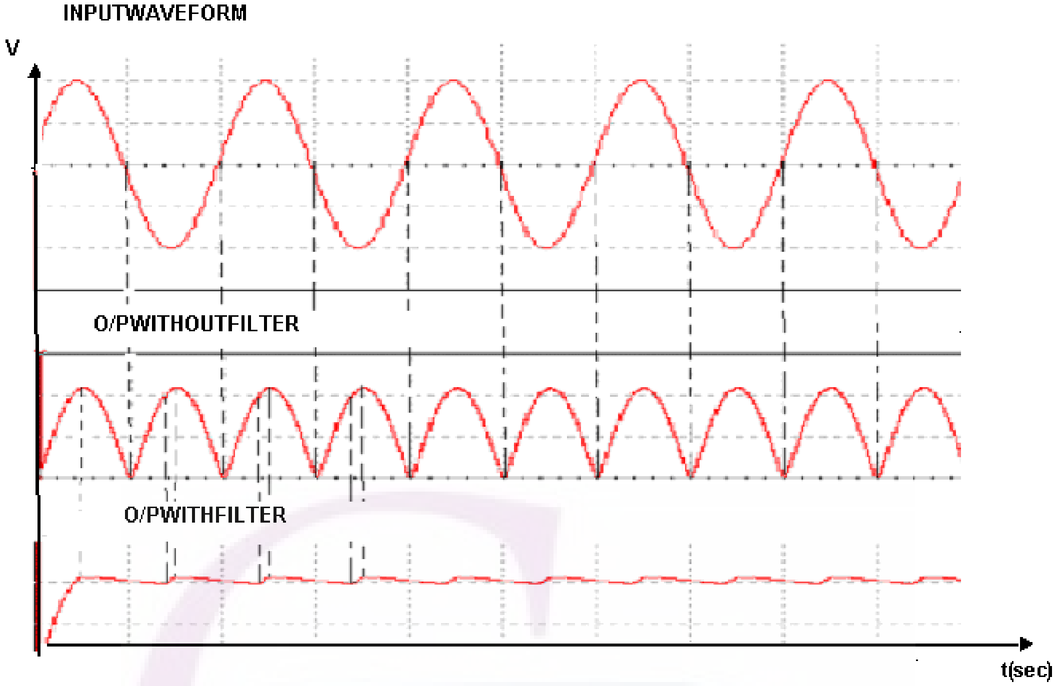
WITHOUT FILTER:

R_L (KOhms)	V_{ac} (Volts)	V_{dc} (Volts)	Ripple Factor $= V_{ac}/ V_{dc}$	% Regulation $(V_{NL}-V_{FL})/V_{FL} *100$

WITH FILTER:

R_L (KOhms)	V_{ac} (Volts)	V_{dc} (Volts)	Ripple Factor $= V_{ac}/ V_{dc}$	% Regulation $(V_{NL}-V_{FL})/V_{FL} *100$

MODEL WAVEFORM:



RESULT: The Ripple factor of Bridge rectifier is with and without filter calculated.

17. CURRENT-SERIES FEEDBACK AMPLIFIER

AIM: To measure the voltage gain of current - series feedback amplifier.

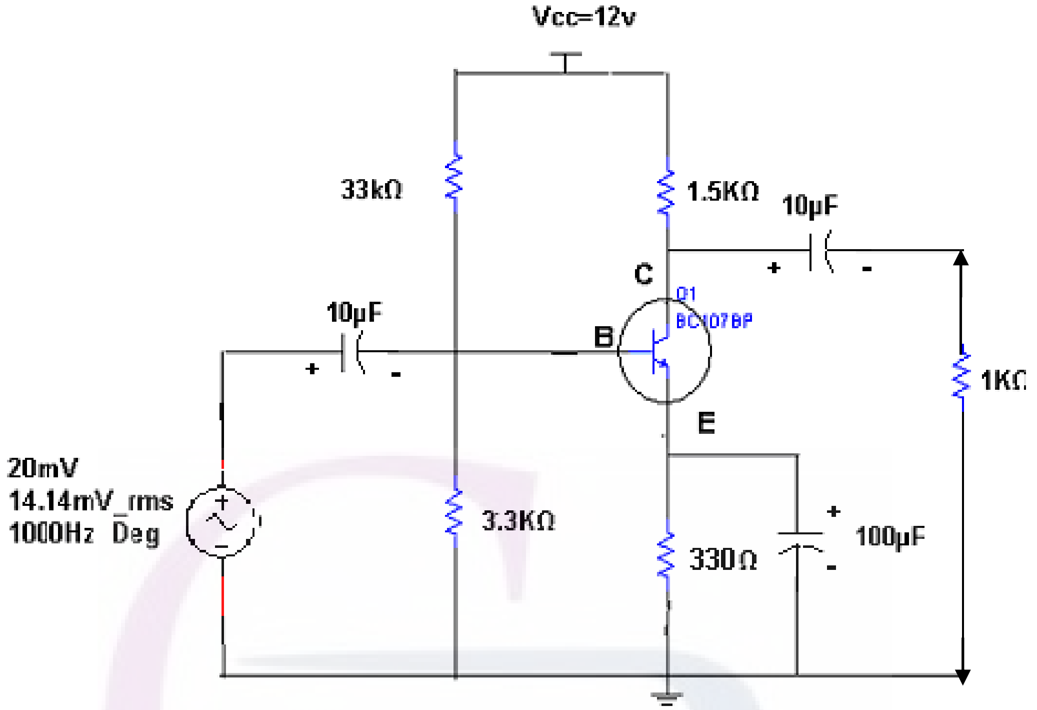
APPARATUS:

NPN Transistor BC107
Breadboard
Regulated Power Supply (0-15V)
Function Generator
CRO
Resistors 33kΩ, 3.3kΩ, 330Ω, 1.5kΩ, 2.2k Ω, 4.7k Ω, 1 k Ω
Capacitors 10µF, 100µF

THEORY:

When any increase in the output signal results into the input in such a way as to cause the decrease in the output signal, the amplifier is said to have negative feedback. The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by using this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased. In Current-Series Feedback, the input impedance and the output impedance are increased. Noise and distortions are reduced considerably.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are made as per circuit diagram.
2. Keep the input voltage constant at 20mV peak-peak and 1 KHz frequency. For different values of load resistance, note down the output voltage and calculate the gain by using the expression
3. $A_v = 20*\log_{10} (V_0 / V_i)$ dB
4. Remove the emitter bypass capacitor and repeat STEP 2.And observe the effect of feedback on the gain of the amplifier.
5. For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.
6. Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression $A_v = 20\log (V_0 / V_i)$ dB

7. A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph sheet

8. The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = $f_2 - f_1$.

9. Where f_1 is lower cutoff frequency of CE amplifier

10. f_2 is upper cutoff frequency of CE amplifier

11. The gain-bandwidth product of the amplifier is calculated by using the expression

Gain-Bandwidth Product = (3dB mid-band gain) X (Bandwidth).

OBSERVATIONS:

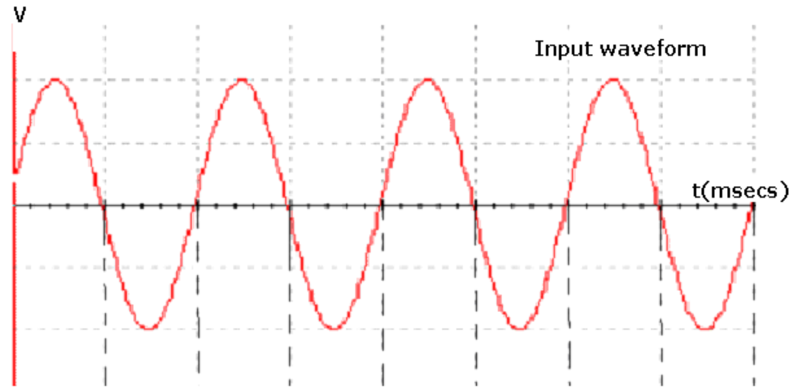
VOLTAGE GAIN:

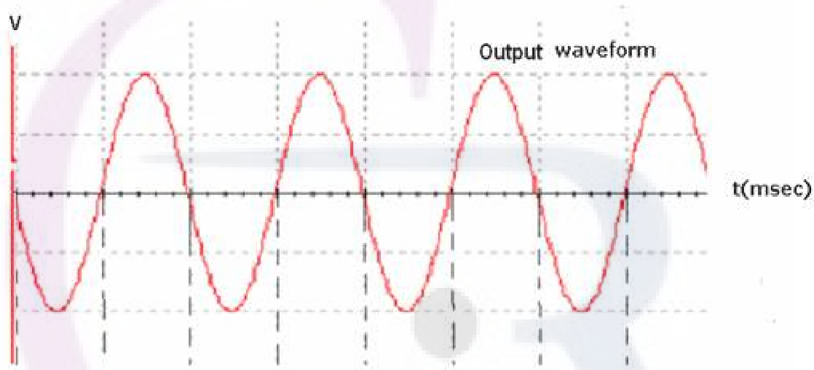
S.NO	Output Voltage (V_o) with feedback	Output Voltage (V_o) without feedback	Gain(dB) with feedback	Gain(dB) without feedback

FREQUENCY RESPONSE:

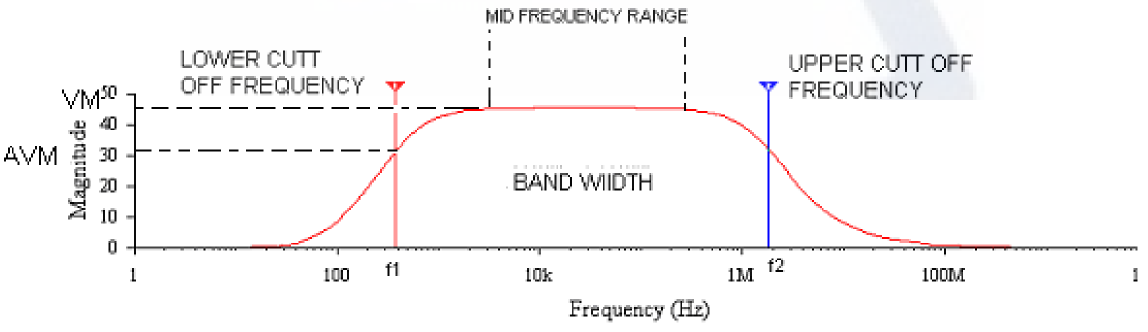
S.NO	Frequency (Hz)	Output Voltage (V_o)	Gain A = V_o/V_i	Gain in dB $20\log_{10}(V_o/V_i)$

MODEL WAVEFORM:





FREQUENCY RESPONSE:



RESULT:

The effect of negative feedback (Current-Series Feedback) on the amplifier is observed. The voltage gain and frequency response of the amplifier are obtained. Also gain-bandwidth product of the amplifier is calculated.

18. VOLTAGE-SERTES FEEDBACK AMPLIFIER

AIM: To study the effect of voltage series feedback on gain of the Amplifier.

APPARATUS:

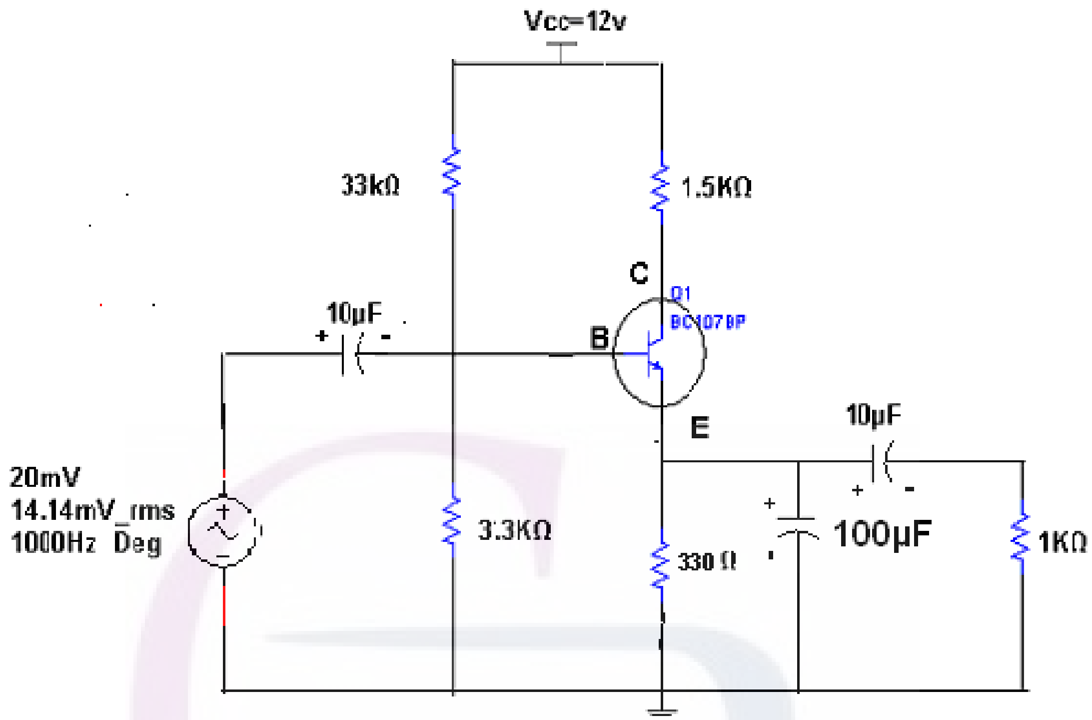
NPN-Transistor BC107
Breadboard
Regulated Power Supply (0-15V)
Function Generator
CRO
Resistors 33kΩ, 3.3kΩ, 1.5kΩ, 1kΩ, 2.2k Ω, 4.7k Ω, 330Ω
Capacitors 10µF, 100µF

THEORY:

When any increase in the output signal results into the input in such a way as to cause the decrease in the output signal, the amplifier is said to have negative feedback. The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters the transistor or the parameters of the other active devices used in the circuit.

The most advantage of the negative feedback is that by using this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased. In Voltage-Series feedback, the input impedance of the amplifier is decreased and the output impedance is increased. Noise and distortions are reduced considerably.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are made as per circuit diagram.
2. Keep the input voltage constant at 20mV peak-peak and 1kHz frequency.For different values of load resistance, note down the output voltage and calculate the gain by using the expression

   $A_v = 20*\log_{10} (V_0 / V_i)$ dB
3. Add the emitter bypass capacitor and repeat STEP 2.And observe the effect of Feedback on the gain of the amplifier
4. For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.
5. Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression $A_v = 20\log(V_0 / V_i)$ dB
6. A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph sheet
7. The Bandwidth of the amplifier is calculated from the graph using the expression

Bandwidth B.W = $f_2 - f_1$.

Where f_1 is lower cutoff frequency of CE amplifier

f_2 is upper cutoff frequency of CE amplifier

The gain-bandwidth product of the amplifier is calculated by using the expression

Gain-Bandwidth Product = (3dB mid-band gain) X (Bandwidth).

OBSERVATIONS:

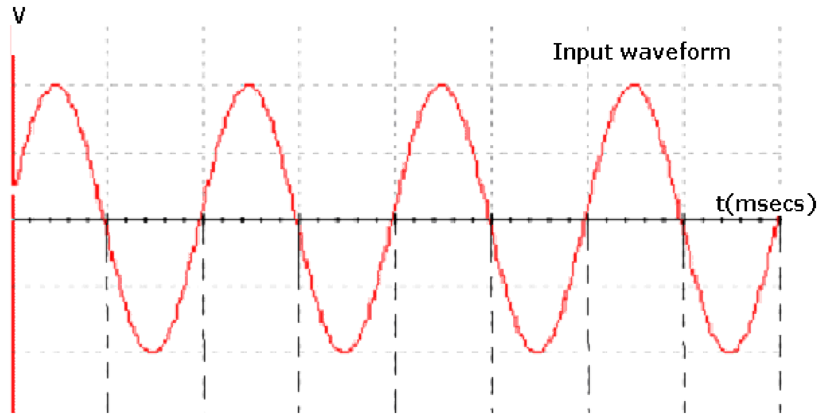
VOLTAGE GAIN:

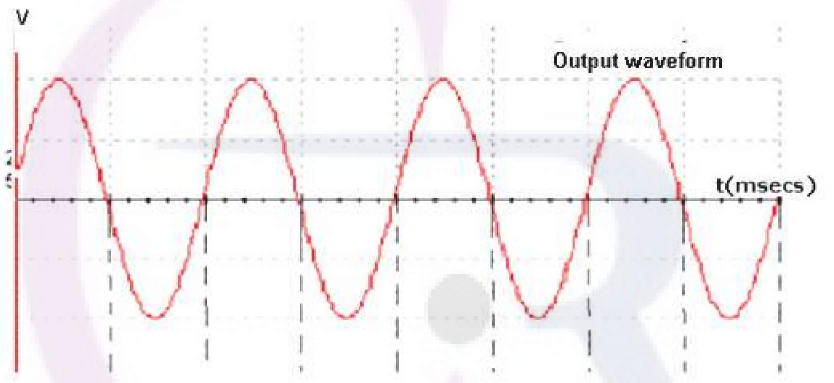
S.NO	Output Voltage (V_o) with feedback	Output Voltage (V_o) without feedback	Gain(dB) with feedback	Gain(dB) without feedback

FRQUENCY RESPONSE:

S.NO	Frequency (Hz)	Output Voltage (V_o)	Gain A = V_o/V_i	Gain in dB $20*\log_{10}(V_o/V_i)$

MODEL WAVEFORMS:





RESULT:

The effect of negative feedback (Voltage - Series Feedback) on the amplifier is observed. The voltage gain and frequency response of the amplifier are obtained. Also gain-bandwidth product of the amplifier is calculated.