IC APPLICATIONS LAB USING ASLK-PRO DEVELOPMENT KIT

USER MANUAL

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CONTENTS

❖ EXPERIMENTS USING ASLK-PRO

Expt. No.1 **Study the characteristics of negative feedback amplifier**

(Inverting, Non – Inverting & Unity gain Amplifiers)

1. a. INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using ASLK-PRO.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TLO82	3
5.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as,

$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

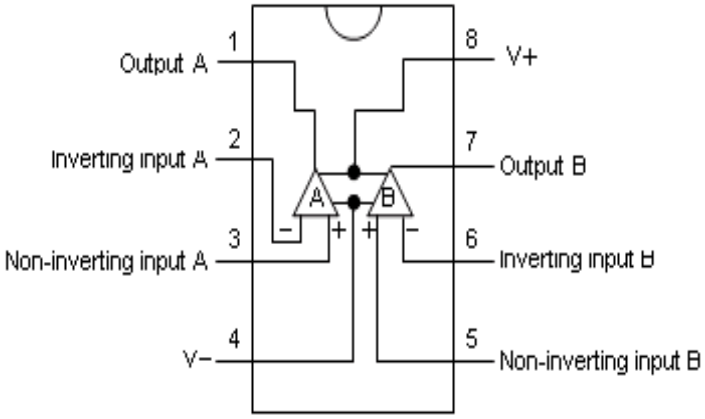
PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 10V.

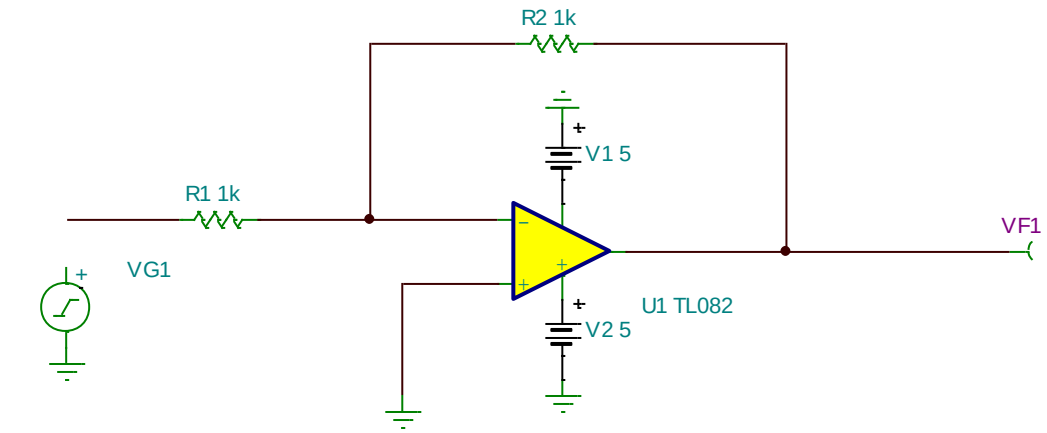
PROCEDURE:

1. **Connections are given as per the circuit diagram in the ASLK-PRO.**
2. **By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.**
3. **The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.**

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



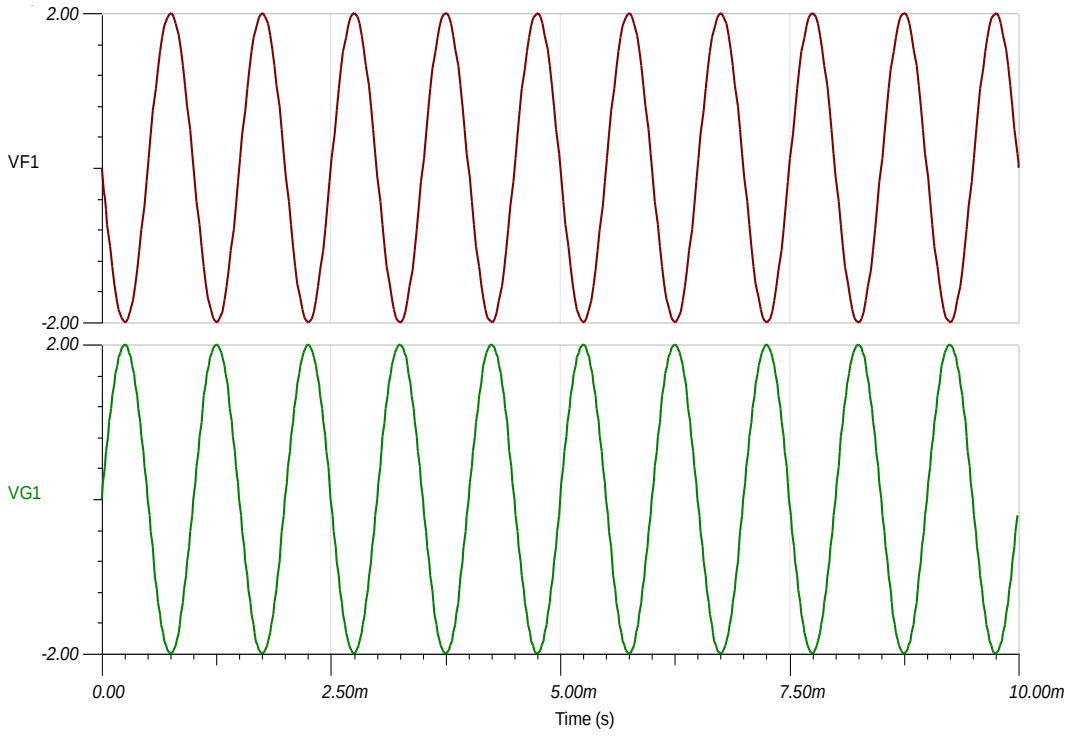
DESIGN:

We know for an inverting Amplifier $A_{CL} = R_F / R_1$
Assume R_1 (approx. 10 KΩ) and find R_f
Hence V_o(theoretical) = - A_{CL} V_i

OBSERVATIONS:

S.No.	Amplitude
Input	
Output	

MODEL GRAPH:



RESULT:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn.

1. b. NON - INVERTING AMPLIFIER

AIM:

To design a Non-Inverting Amplifier for the given specifications using ASLK-PRO.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TLO82	1
5.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

$$V_o = A_{CL} V_i$$

Here the output voltage is in phase with the input signal.

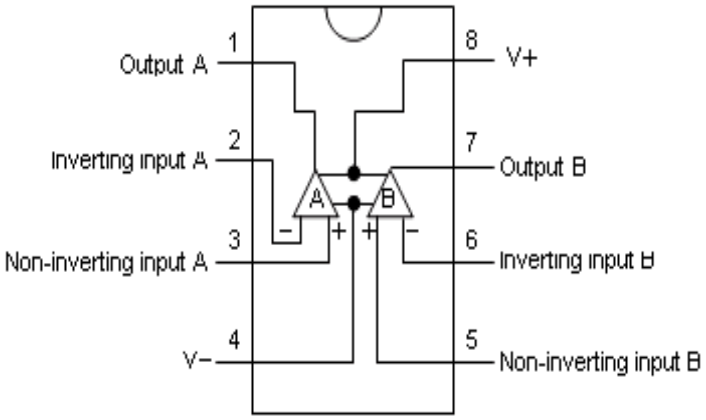
PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 10V.

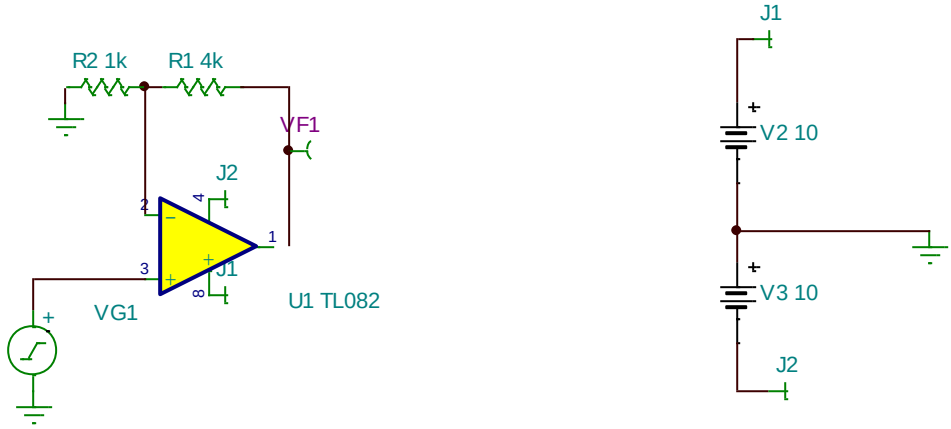
PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.**
3. **The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.**

PIN DIAGRAM:



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



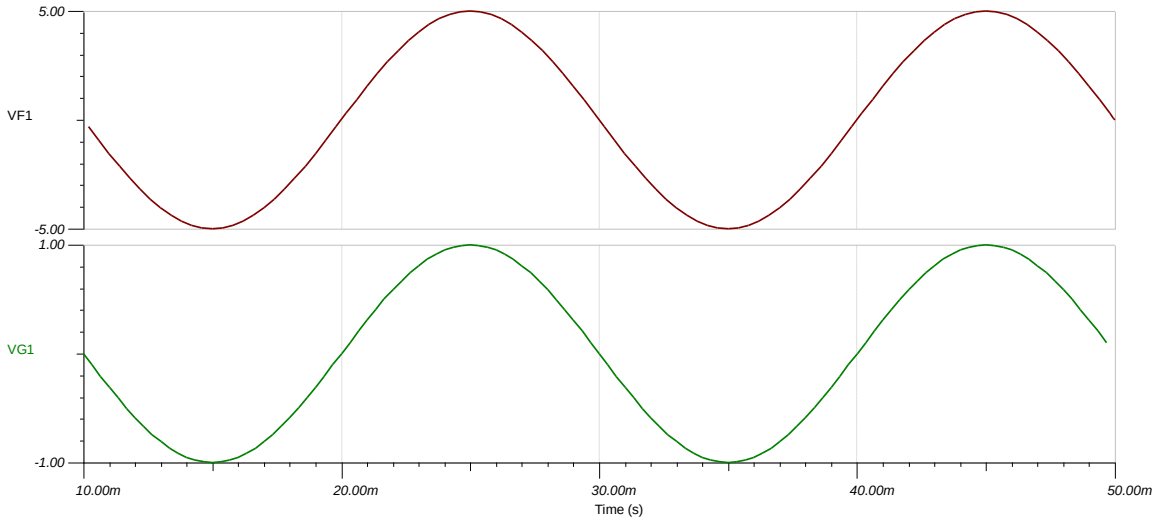
DESIGN:

We know for a Non-inverting Amplifier $A_{CL} = 1 + (R_F / R_1)$
Assume R_1 (approx. 10 KΩ) and find R_f
Hence $V_o = A_{CL}\ V_i$

OBSERVATIONS:

S.No.	Amplitude
Input	
Output	

MODEL GRAPH:



RESULT:

The design and testing of the Non-inverting amplifier is done and the input and output waveforms were drawn.

1.c. Unity Gain Amplifer

AIM:

To design an Unity Gain Amplifier for the given specifications using ASLK-PRO.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TLO82	3
5.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the Non- inverting input terminal. The output voltage V_o is fed back to the inverting input terminal. The output voltage is given as,

$$V_o = V_i$$

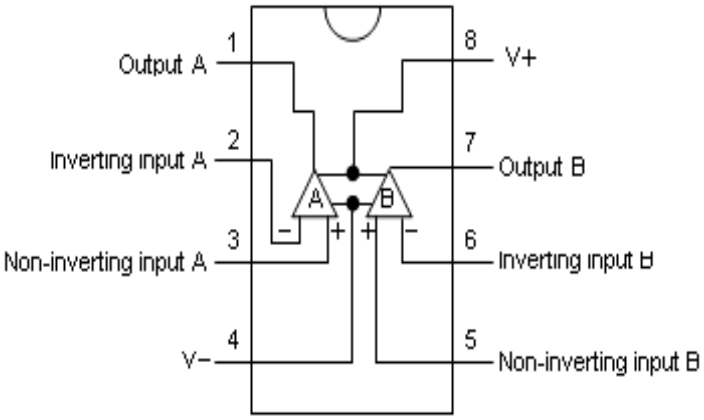
PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 10V.

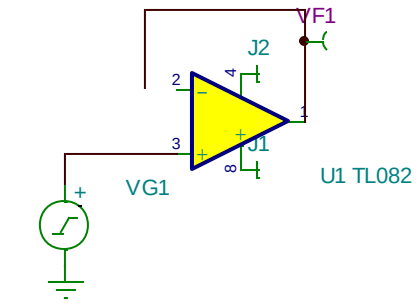
PROCEDURE:

4. **Connections are given as per the circuit diagram in the ASLK-PRO.**
5. **By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.**
6. **The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.**

PIN DIAGRAM:



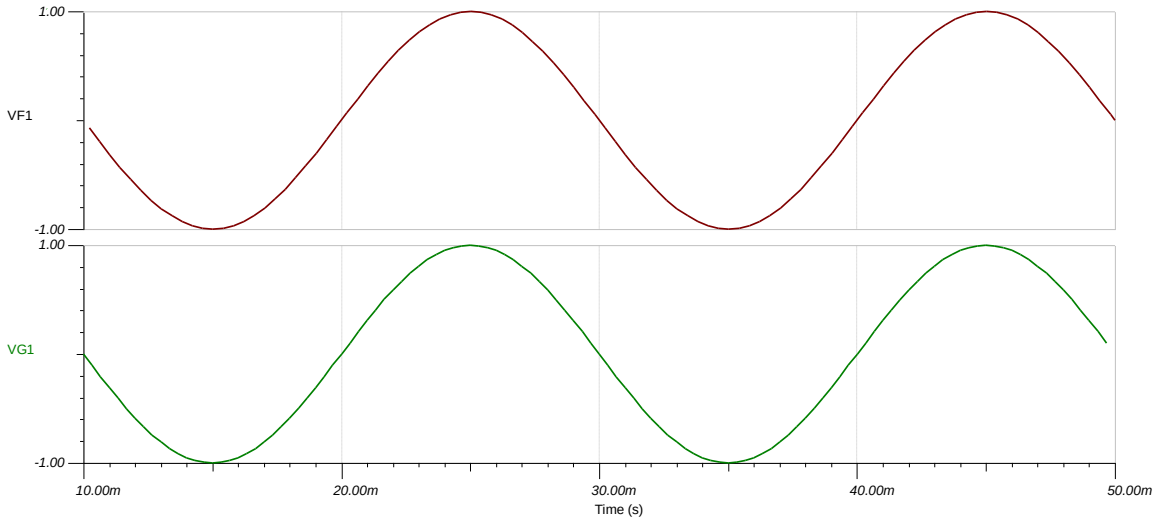
CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



OBSERVATIONS:

S.No.	**Amplitude**
Input	
Output	

MODEL GRAPH:



RESULT:

The design and testing of the unity gain amplifier is done and the input and output waveforms were drawn.

Expt. No.2

Instrumentation Amplifer

AIM:

Design an Instrumentation Amplifier of a Differential mode gain of 'A' using three Op-amp.

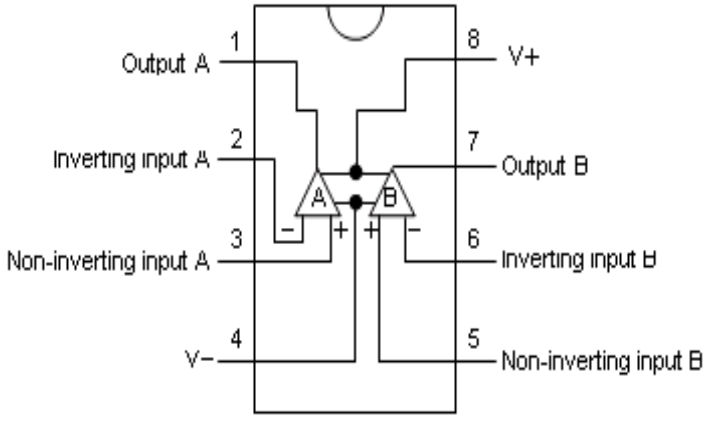
APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TLO82	3
5.	Connecting wires and probes	As required	

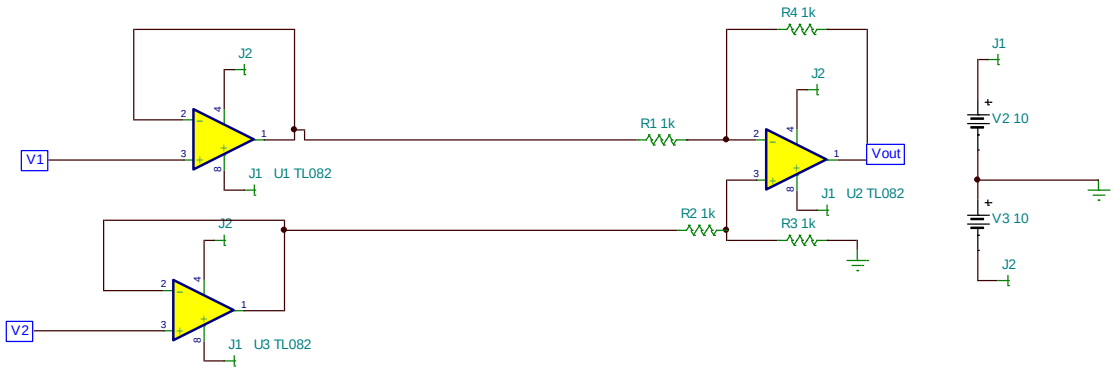
PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 10V.

PIN DIAGRAM:



Circuit Diagram of Instrumentation Amplifier:



OBSERVATIONS:

S.No.	Amplitude
Input	
Output	

RESULT:

The Design an Instrumentation Amplifier of a Differential mode gain of 'A' using three Op-amp was done.

Expt. No.3

INTEGRATOR

AIM:

To design an Integrator circuit for the given specifications using ASLK-PRO.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082	1
8.	Connecting wires and probes	As required	

THEORY:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as,

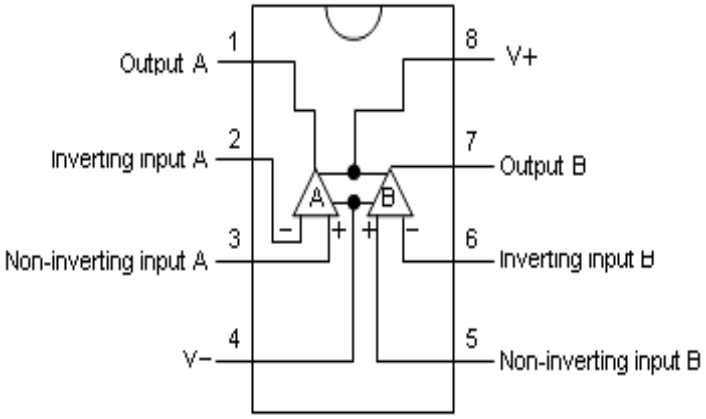
$$V_o = - (1/R_f C_1) \int V_i \, dt$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is,

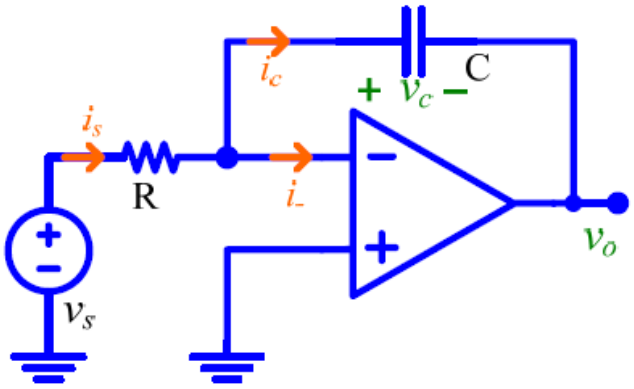
$$T \geq R_f C_f$$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INTEGRATOR:



PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.**
3. **The output waveform is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.**

RESULT:

The design of the Integrator circuit was done and the input and output waveforms were obtained.

Expt. No.4

ASTABLE MULTIVIBRATOR

AIM:

To design an astable multivibrator circuit for the given specifications using ASLK-PRO

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082	1
8.	Connecting wires and probes	As required	

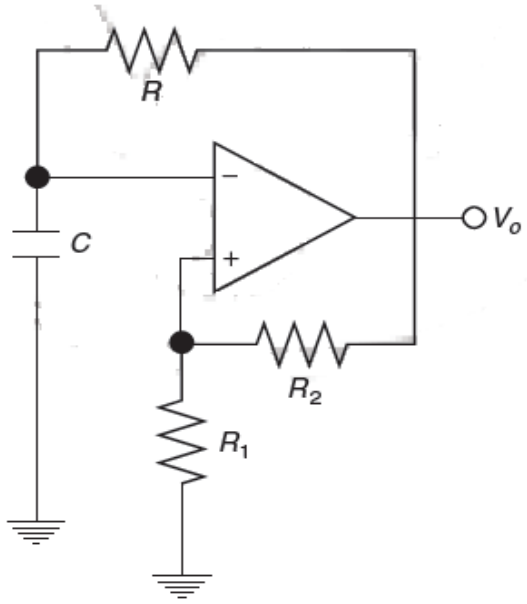
THEORY:

An astable multivibrator is shown in Figure below. The square and the triangular Waveforms shown in the figure are both generated using the astable multivibrator. We refer to β as the regenerative feedback factor. The time period of the square waveform generated by the multivibrator is given by

$$T = 2RC.ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\text{where } \beta = \frac{R_1}{R_1 + R_2}$$

CIRCUIT DIAGRAM OF ASTABLE MULTIVIBRATOR



DESIGN:

$$T = 2RC\ln[(1+\beta)/(1-\beta)]$$

$$\text{Where } \beta = R1/R1+R2$$

$$\text{Freq}=(1/T)=\text{----Hz}$$

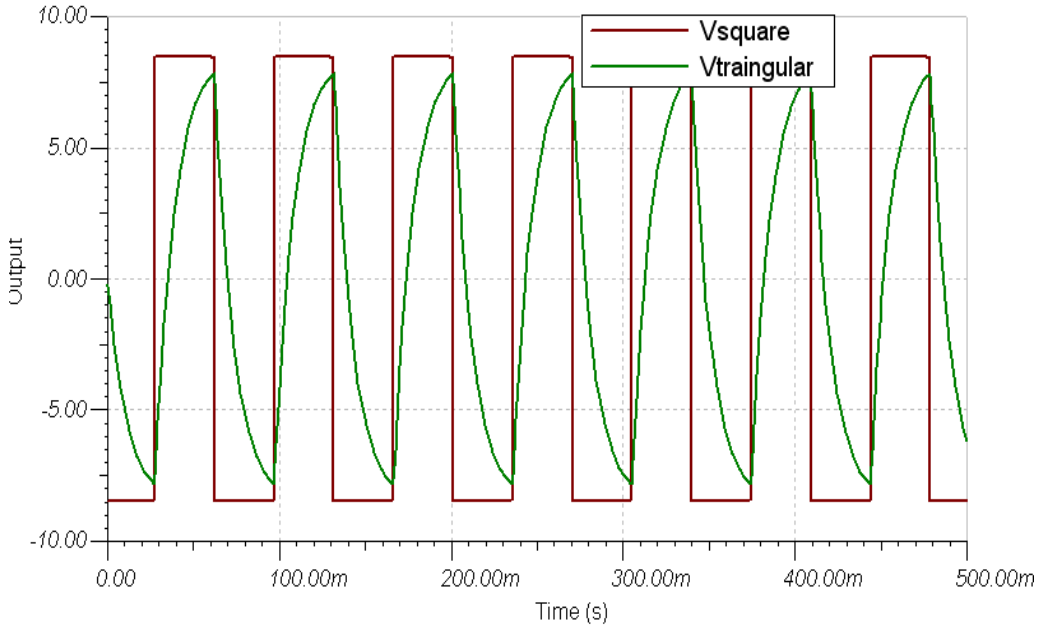
PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **the output waveform is observed with the help of a CRO**

OBSERVATIONS:

S.No	R,C	Time period	Frequency	
1.				
2.				

MODEL GRAPH:



RESULT:

The design of the Astable multivibrator circuit was done and the output voltage and capacitor voltage waveforms were obtained.

Expt. No.5

Automatic Gain Control (AGC)/Automatic Volume Control (AVC)

AIM:

Design a AGC system to maintain a peak amplitude of sine wave output at 2V.

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082,MPY634	1
8.	Connecting wires and probes	As required	

Theory:-

In the signal chain of an electronic system, the output of the sensor can vary depending on the strength of the input. To adapt to wide variations in the magnitude of the input, we can design an amplifier whose gain can be adjusted dynamically. This is possible when the input signal has a narrow bandwidth and the control system is called Automatic Gain Control or AGC. Since we may wish to maintain the output voltage of the amplifier at a constant level, we also use the term Automatic Volume Control (AVC). Figure 1 shows an AGC circuit. The typical I/O characteristics of AGC/AVC circuit are shown in Figure 2. As shown in Figure 2, the output value of the system remains constant at Vo

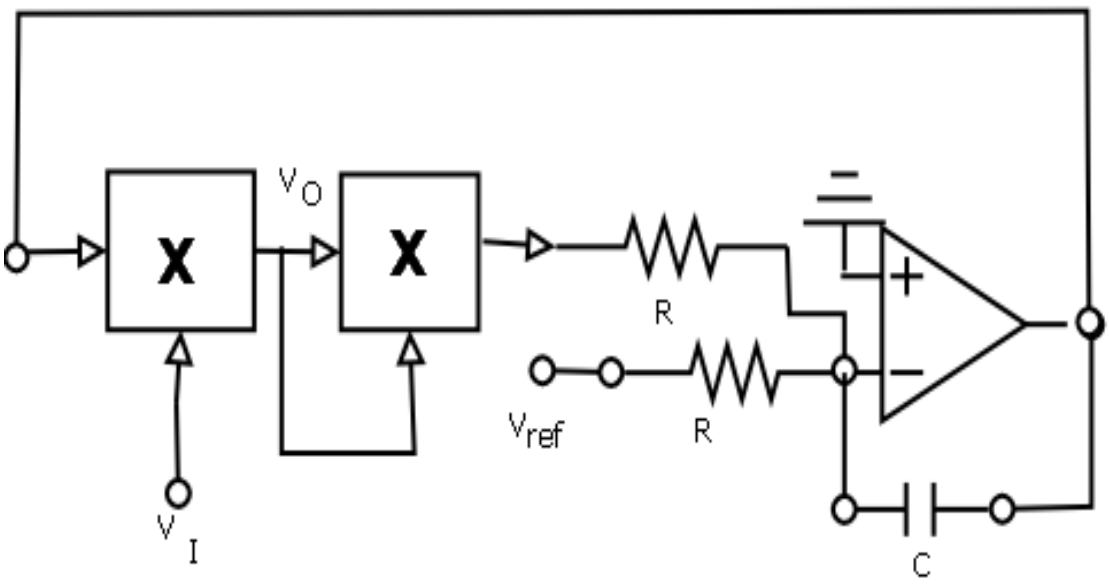


Fig:-AGC Circuit

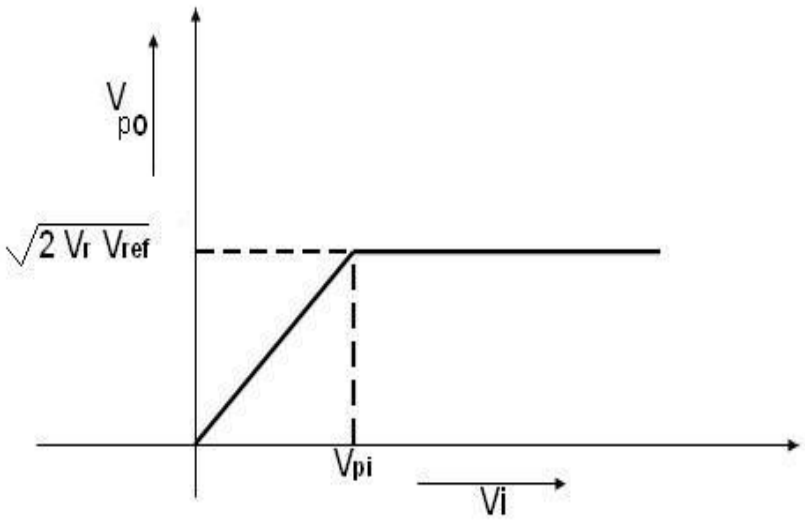
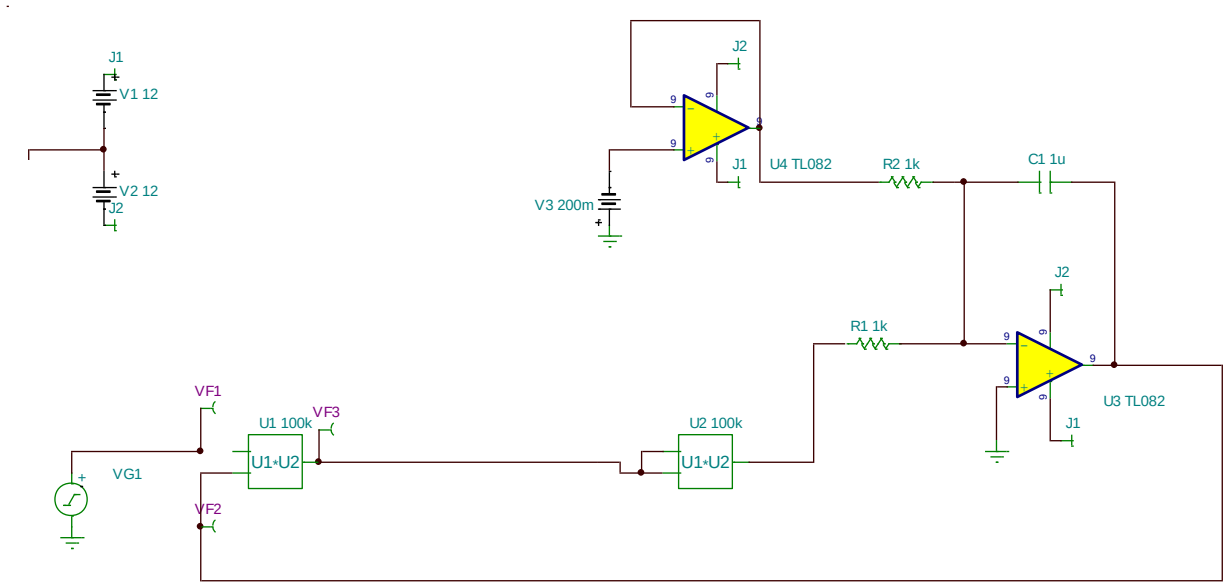


Fig2:- typical I/O characteristics of AGC/AVC circuit

CIRCUIT DIAGRAM OF AGC/AVC Circuit



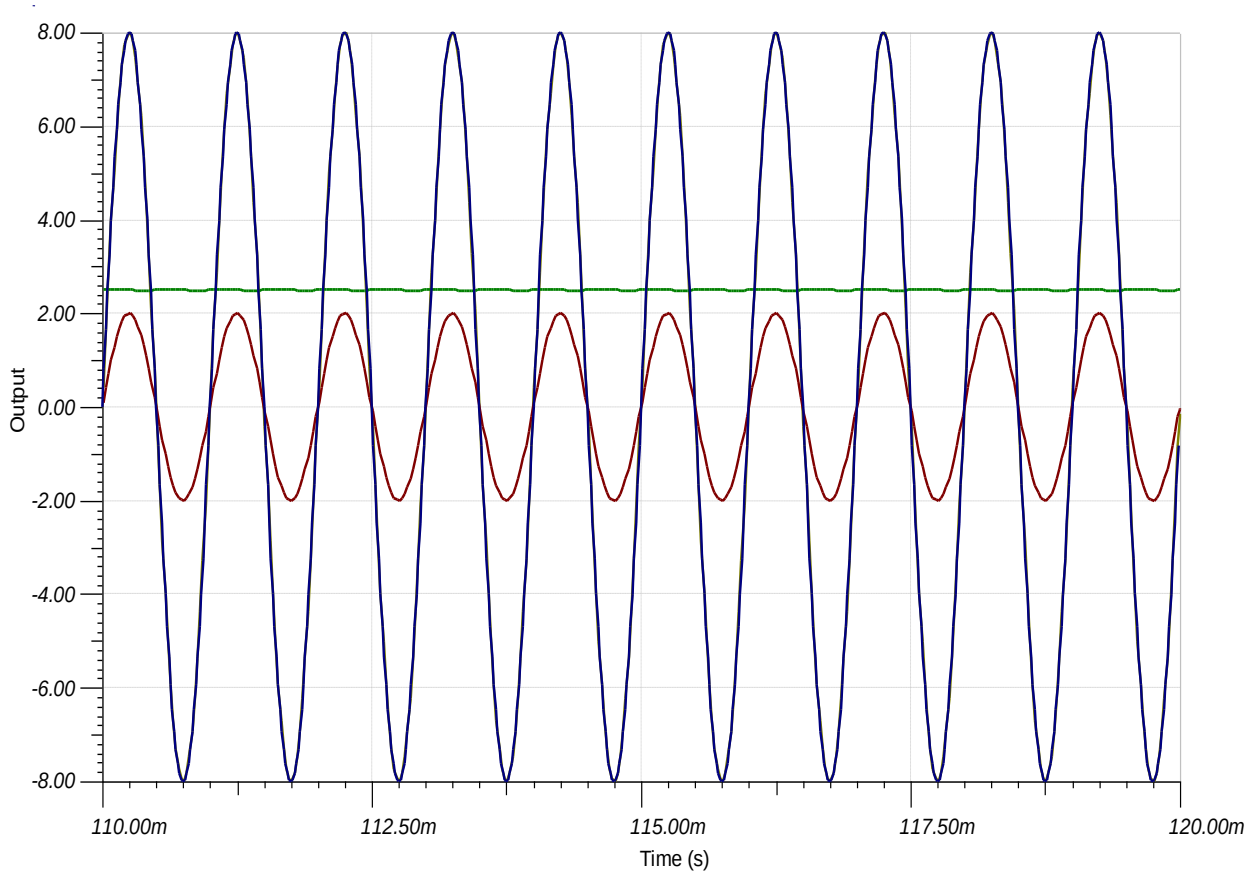
PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **The output waveform is observed with the help of a CRO**
3. **Apply a Sin wave input and observe the amplitude at output**
4. **Vary the input amplitude at fixed input frequency; the output amplitude should remain constant for varying input amplitude within the lock range of the system.**

OBSERVATIONS: Fixed Input Freuency=1khz

S.No	Input Voltage	Output Voltage
1.		
2.		

MODEL GRAPH:



RESULT:

The design of the AGC circuit was done and the output voltage waveforms were obtained.

Expt. No.6

Function generator

Aim:

Design and test function generator that can generator square wave and triangular wave output for a given frequency

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082	1
8.	Connecting wires and probes	As required	

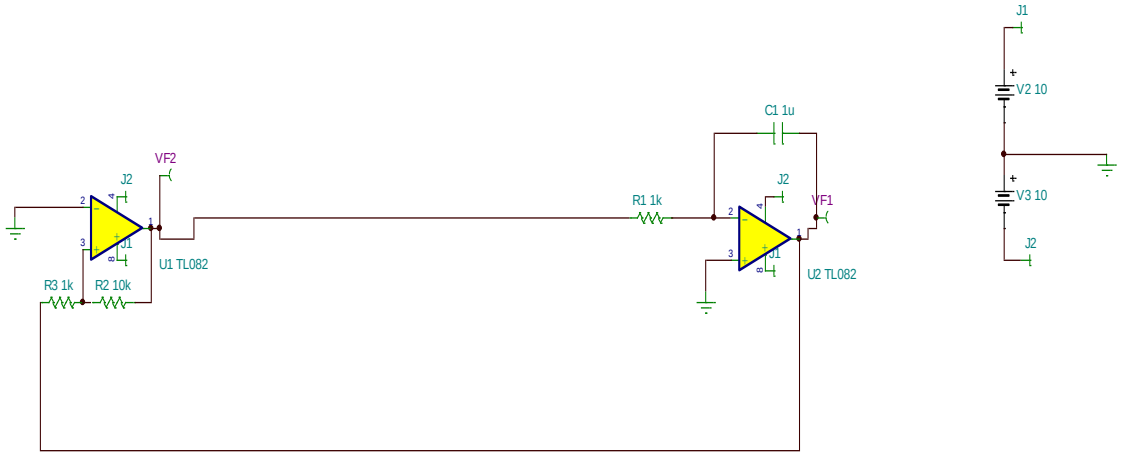
Theory:-

The Function generator circuit consists of a feedback loop, which includes a Schmitt trigger and a integrator.

The function generator produces a square wave at the Schmitt trigger output and a triangular wave at the integrator output with the frequency (F) equal to

$$f=(1/4RC).(R2/R1)$$

Circuit Diagram of Function generator Circuit



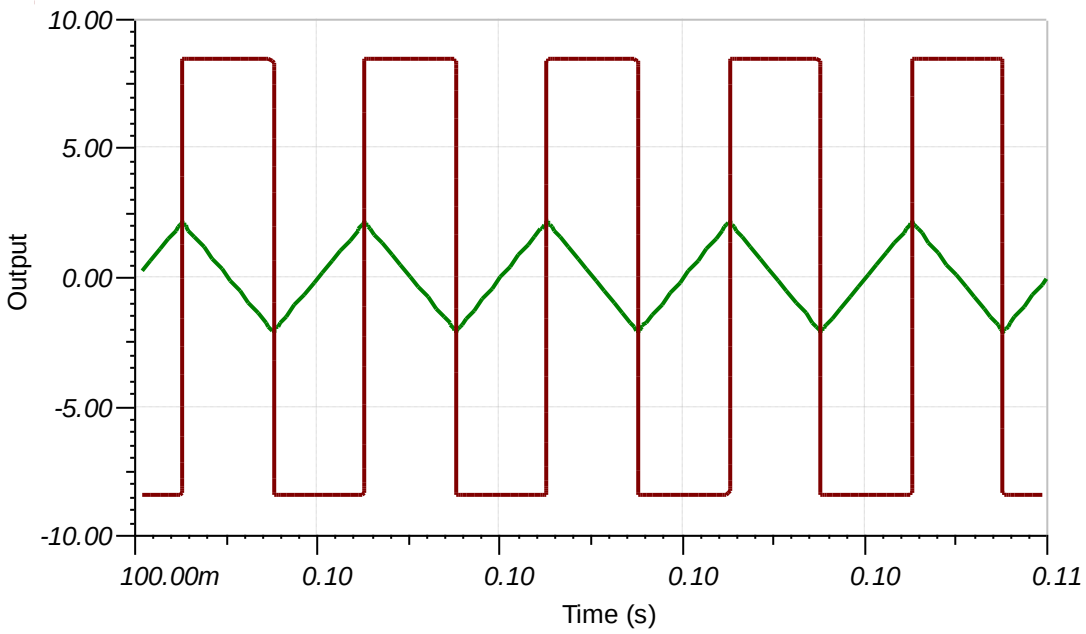
PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **The output waveform is observed with the help of a CRO**

OBSERVATIONS:

S.No	Frequency of Square wave	Frequency of Triangular wave
1.		
2.		

MODEL GRAPH:



RESULT:

The design of the Function generator circuit was done and the output waveforms Square & Triangular waveform obtained.

Expt. No.7

Voltage Control Oscillator(VCO)

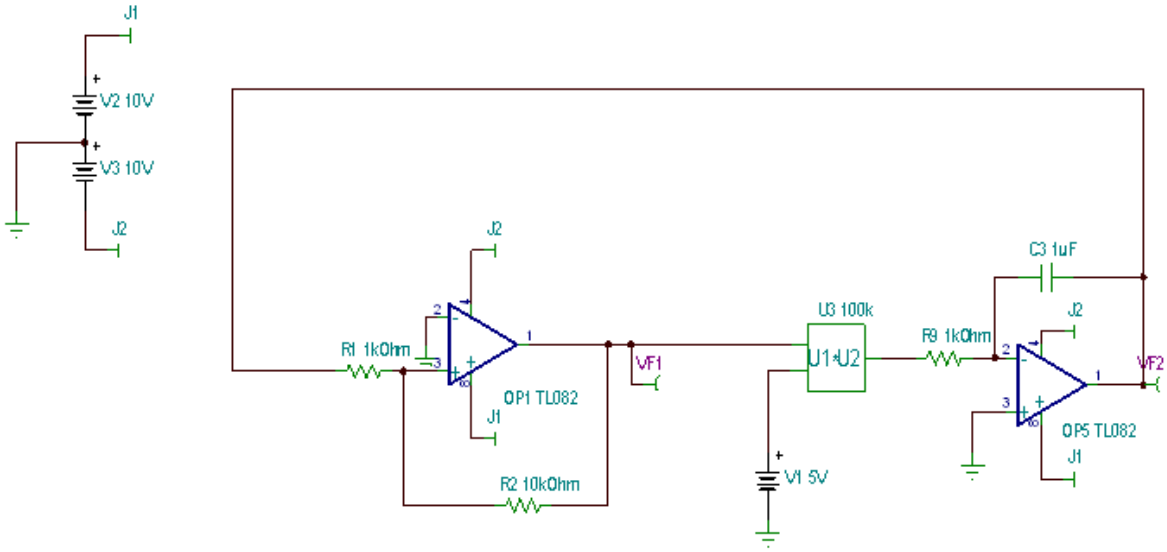
Aim:

Design and test Voltage Control Oscillator for a given specification

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082,MPY634	1
8.	Connecting wires and probes	As required	

Circuit Diagram of VCO Circuit



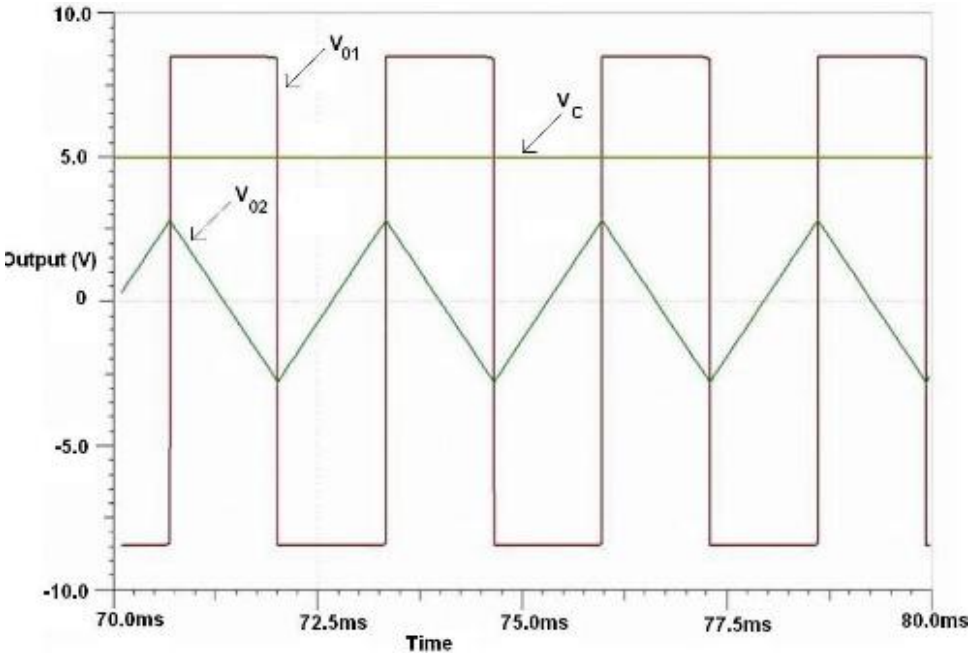
PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **The output waveform is observed with the help of a CRO**
3. **Vary the control Voltage(Vc) obtain the change in Frequency(F0)**

OBSERVATIONS:

S.No	Control voltage(Vc)	Change in frequency(F0)
1.		
2.		

MODEL GRAPH:



RESULT:

The design of the Voltage controlled oscillator circuit was done for a given specification.

Expt. No.8 **PLL**

Aim:

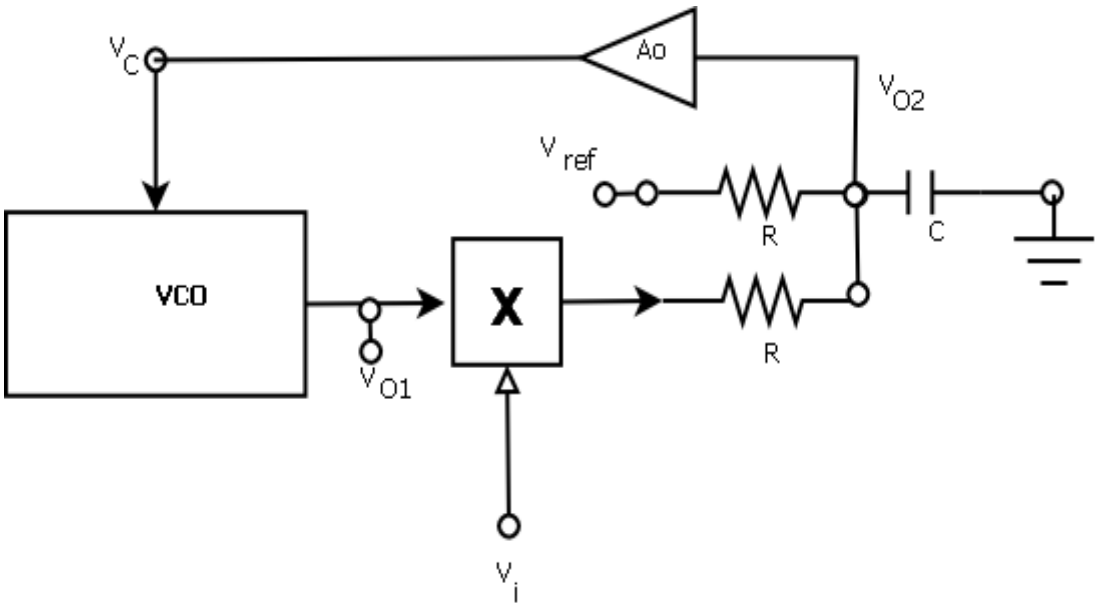
Design and test a PLL to get locked to a given frequency "f".

APPARATUS REQUIRED:

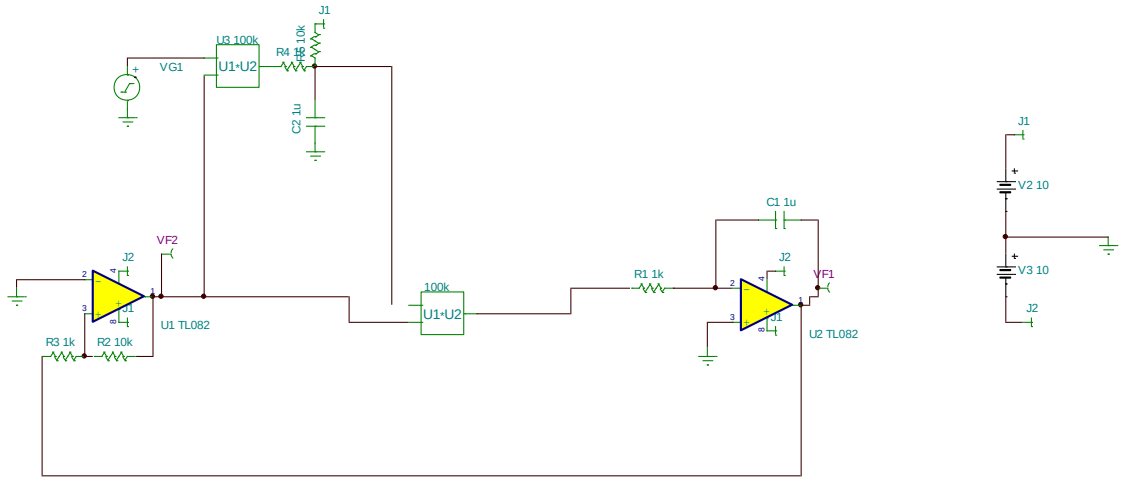
S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082,MPY634	1
8.	Connecting wires and probes	As required	

Theory:

Crystal can be used to generate stable clocks in the range of a few hundreds of kHz to a few mhz.if we need stable clocks of much larger frequency,we can use the clock waveform from the crystal source as a reference clock and additional analog circuits to multiply the frequency of the reference clock.such a circuit is called a Phase Locked Loop.



Circuit Diagram of PLL Circuit



PROCEDURE:

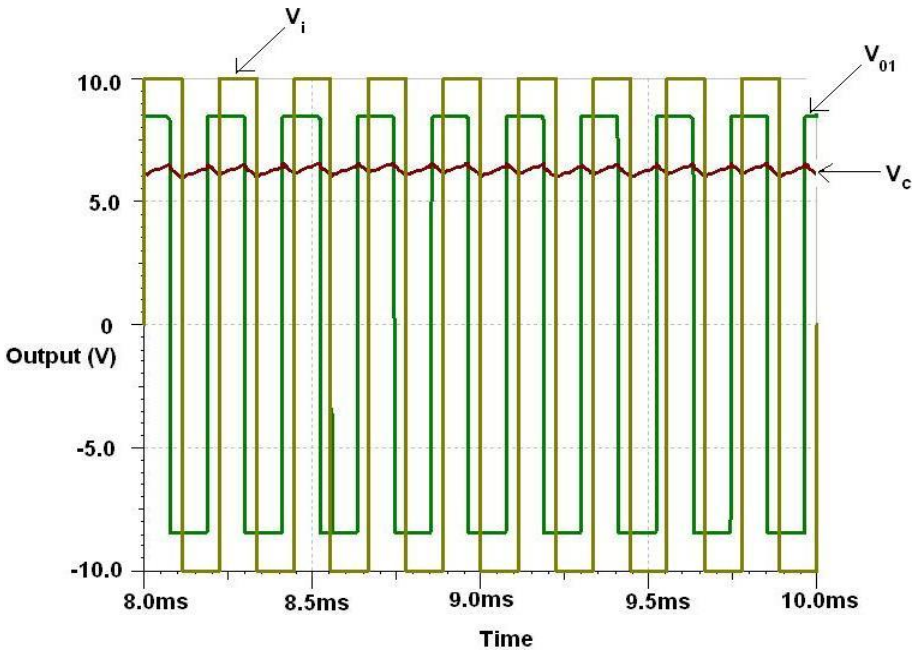
1. **Connections are given as per the circuit diagram.**

2. **the output waveform is observed with the help of a CRO**
3. **Measure the lock range of the system**
4. **Measure the change in the phase of the output signal as input frequency is varied with in the lock range**

OBSERVATIONS:

S.No	Input frequency	Output frequency
1.		
2.		

MODEL GRAPH:



RESULT:

The design of the phase lock loop circuit was done for a given specification.

Expt. No.9 **Analog Filters-1**

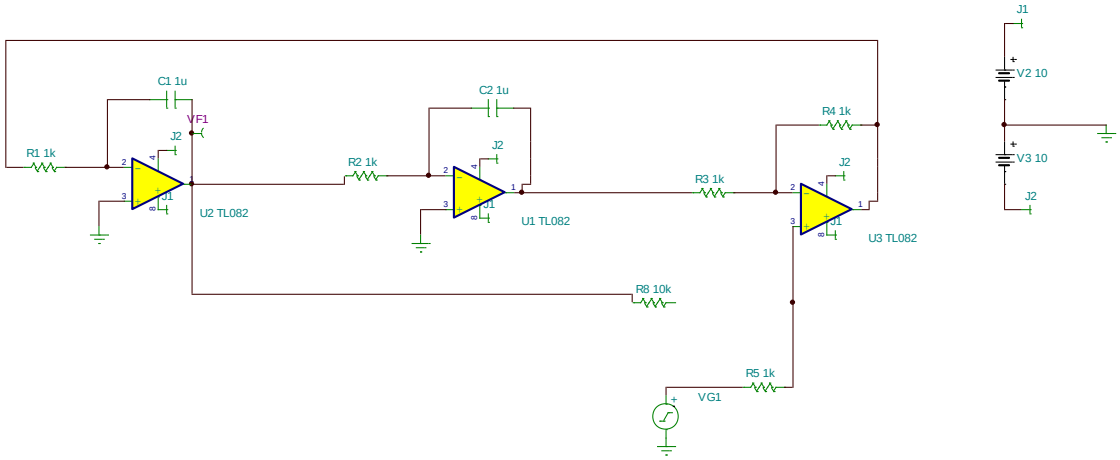
Aim:

Design a Second order Butterworth band-pass filter for a given center frequency.

APPARATUS REQUIRED:

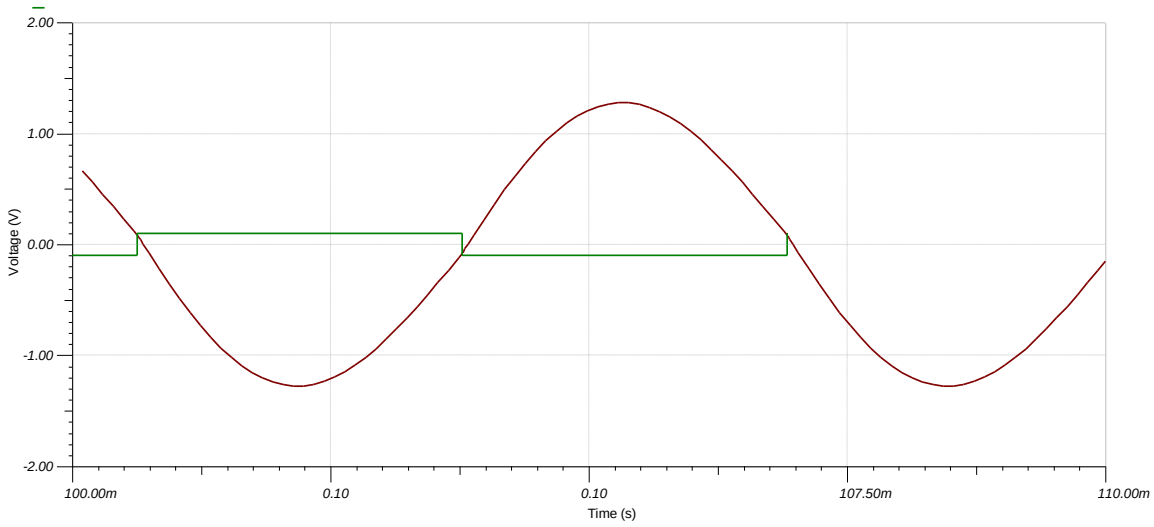
S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082,MPY634	1
8.	Connecting wires and probes	As required	

Circuit Diagram of second order Butterworth Band-Pass filter :



PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **the output waveform is observed with the help of a CRO**
3. **Steady-State response:Apply a Square-Wave input(F= 159HZ)**
4. **A Sample output is shown in figure below**



RESULT:

The design of the phase lock loop circuit was done for a given specification.

Expt. No.10 **Analog Filters-II**

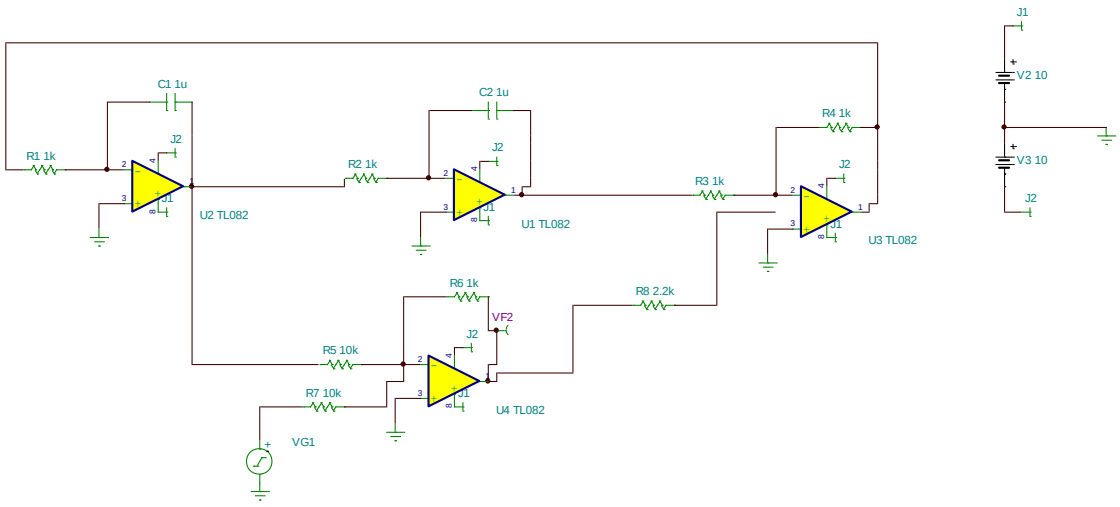
Aim:

Design a Notch filter for a given center frequency.

APPARATUS REQUIRED:

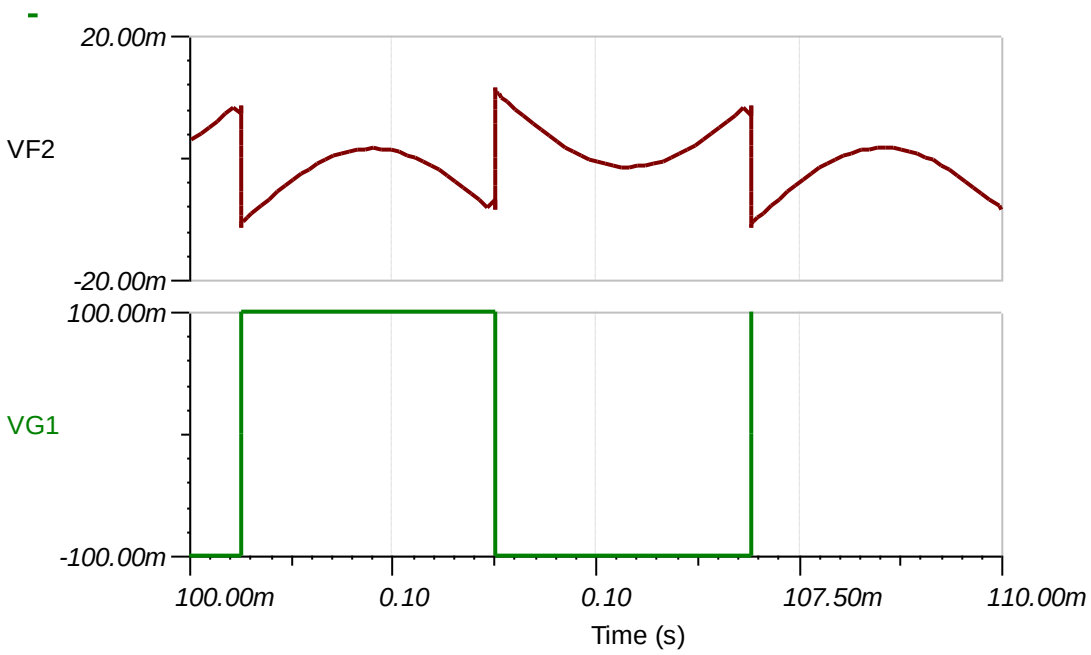
S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082,MPY634	1
8.	Connecting wires and probes	As required	

Circuit Diagram of Notch filter using KHN Network:



PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **the output waveform is observed with the help of a CRO**
3. **Steady-State response:Apply a Square-Wave input(F= 159HZ) to eliminate the 50hz power line frequency**
4. **A Sample output is shown in figure below**



RESULT:

The design of the Notch filter circuit was done for a given specification.

Expt. No.11 **Self-tuned Filter**

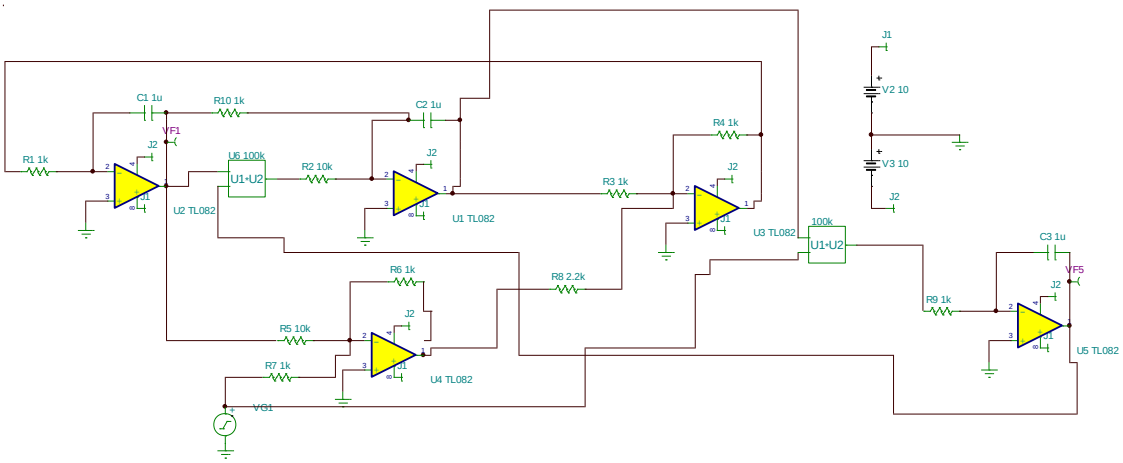
Aim:

Design and test a high-Q Band pass self-tuned filter for a given center frequency.

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TL082,MPY634	1
8.	Connecting wires and probes	As required	

Circuit Diagram of Self-tuned filter :



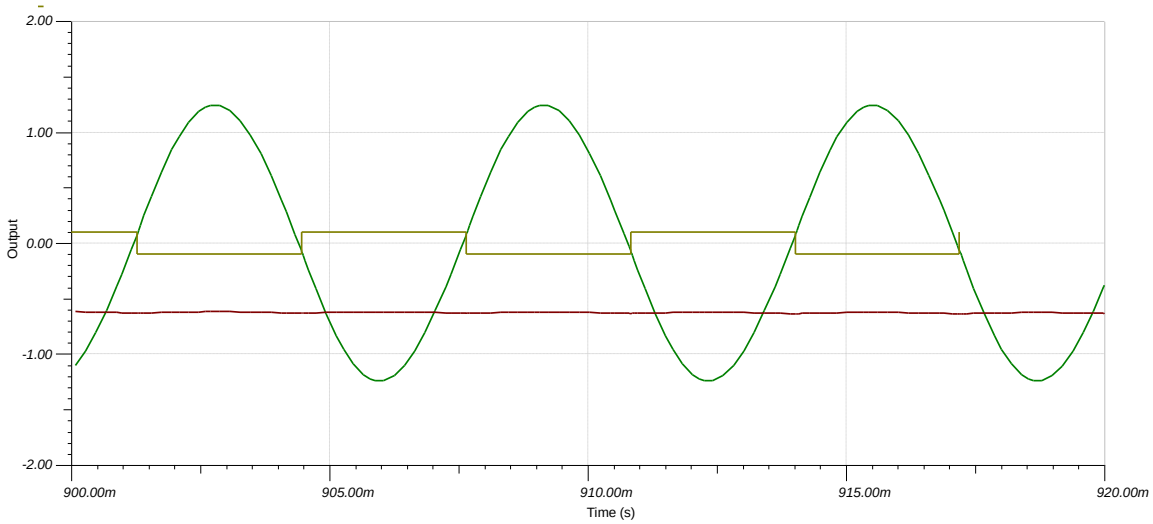
PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **the output waveform is observed with the help of a CRO**
3. **Apply a square wave input and observe the amplitude of the Band pass output**
4. **Vary the input frequency at fixed input amplitude; the output amplitude should remain constant for varying input frequency within the lock range of the system.**

OBSERVATIONS: Fixed Input Voltage=0.1 0r 0.2

S.No	Input frequency	Output Amplitude
1.		
2.		

MODEL GRAPH:



RESULT:

The design of the Self-Tuned Filter circuit was done for a given specification.

Expt. No.12 **DC-DC Converter**

Aim:

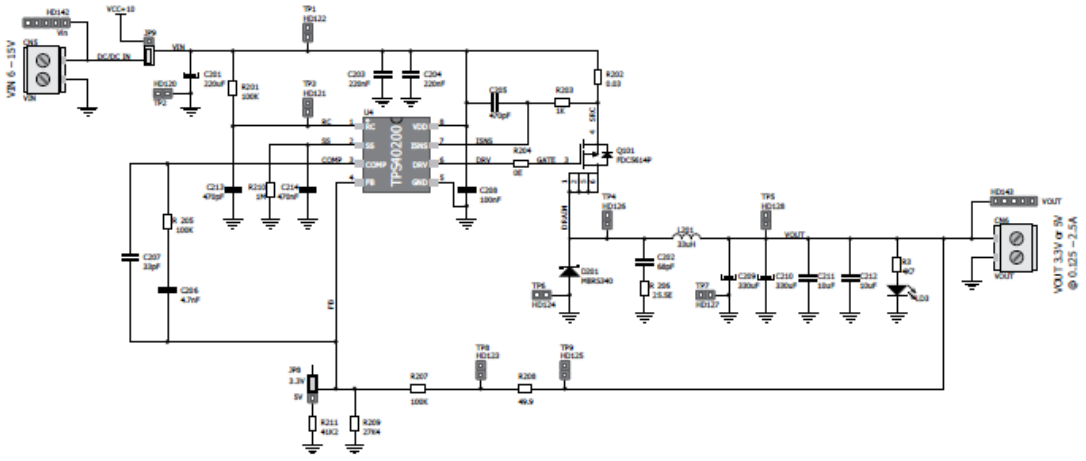
Design of a Switch mode power supply that can provide a regulated output voltage for a given input range using the TPS40200 IC

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TPS402000 IC	1
8.	Connecting wires and probes	As required	

Theory:

The TPS40200 evaluation module included on ASLK PRO. Kit uses the TPS40200 non synchronous buck converter to provide a resistor-selected, 3.3V or 5V output that delivers up to 2.5A from up to 16V input bus. See Figure 1 for a schematic diagram of the EVM. The evaluation module operates from a single supply and uses the single P–channel Power FET and Schottky diode to produce a low cost buck converter. The regulated output of the EVM is resistance-selected and can be adjusted within the limited range by making the changes in the feedback loop, as shown below



PROCEDURE:

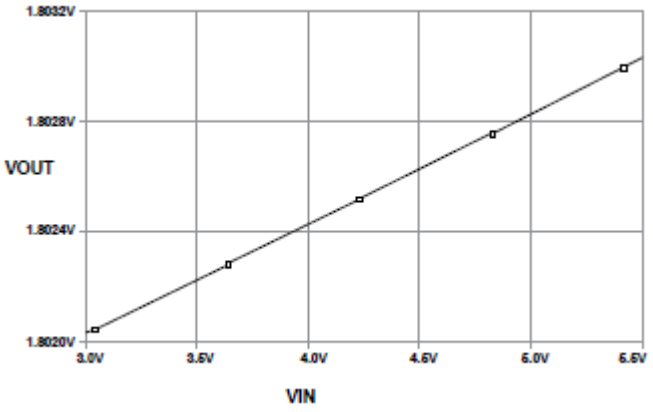
1. **Connections are given as per the circuit diagram.**

2. **Vary the input voltage from 6v to 15v and observed the ouput with the help of a Multimeter.**

OBSERVATIONS:

S.No	Input voltage	Output voltage
1.		
2.		

MODEL GRAPH:



Result:-

The design of the DC-DC Convertor circuit was done for a given specification.

Expt. No.13 **LDO**

Aim:

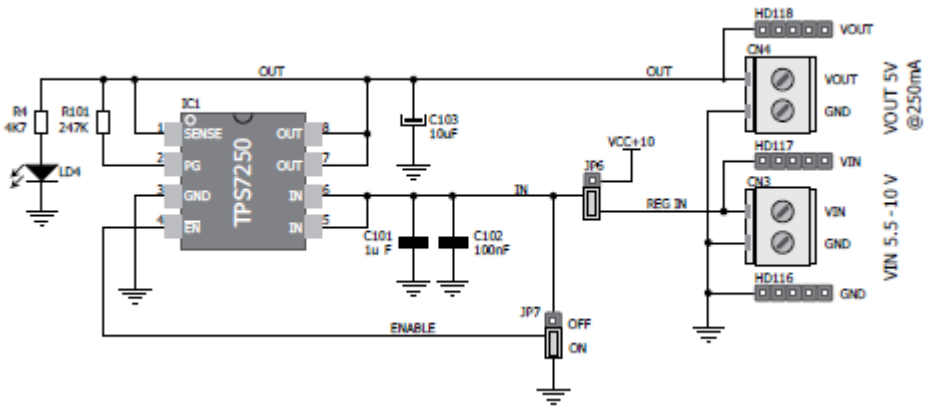
Design and test a Low Dropout regulator using TPS7250 IC

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	ASLK-PRO	TPS7250 IC	1
8.	Connecting wires and probes	As required	

Theory:

TPS7250 evaluation module helps us evaluate the operation and performance of the TPS7250 family of linear regulators. The linear regulator TPS7250 from Texas Instruments is capable of 200mA output current at 5V fixed output voltage level. It is a low quiescent current, low noise, high PSRR, fast start-up LDO with excellent line and transient response. See Figure 1 for the schematic diagram of the evaluation module. The input supply voltage VIN is fed at screw terminal CN3 and falls in the range 5.5V to 11V. The leads to the input supply must be as short as possible and must be twisted to reduce EMI transmission. The capacitor C102 improves the transient response of the regulator. The capacitor C101 helps to reduce the ringing on input when supply wires are too long.The regulator can be enabled/disabled using the ON/OFF jumper JP7. The "Enable"pin (EN) must never be left floating. Connecting a shorting jumper wire between pins 1 (GND) and pin 2 (EN) of JP7 enables the regulator. Connecting a jumper wire between pins 2 (EN) and pin 3 (VIN) disables the regulator. Output voltage is available on screw terminal CN4, or Vout pin header, and the typical load current is 200mA.



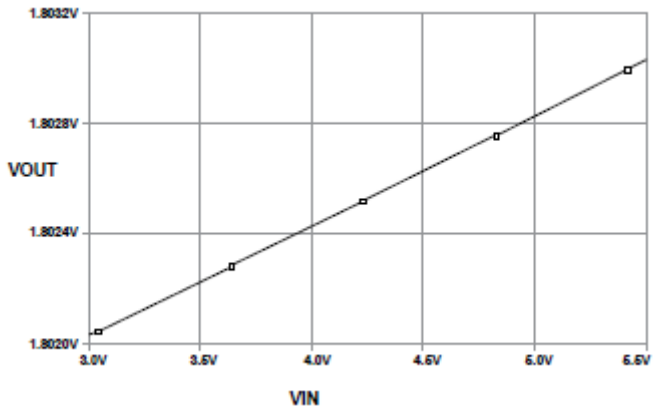
OBSERVATIONS:

S.No	Input voltage	Output voltage
1.		
2.		

PROCEDURE:

1. **Connections are given as per the circuit diagram.**
2. **Vary the input voltage from 5.5v to 10v and observed the outputs voltage with the help of a Multimeter.**

MODEL GRAPH:



Result:-

The design of the LDO circuit was done for a given specification.