G NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE
(FOR WOMEN)
SHAIKPET, HYDERABAD – 500008

DIGITAL IC
LABORATORY MANUAL

DEPARTMENT
OF
ELECTRONICS & COMMUNICATION ENGINEERING
MARCH - 2006

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INDEX

LOGIC GATES

Aim: 1) Study of logic gates using IC's & discrete components.
2) Realization of basic gates using NAND & NOR gates (Universal gates).

Apparatus: 1. Logic gates (IC) trainer kit.
2. Trainer kit for discrete circuit of gates
3. Connecting patch chords.

I. Verifying the logic gates using IC's:

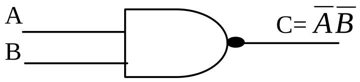
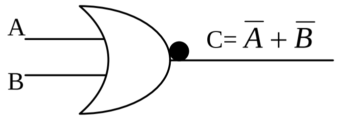
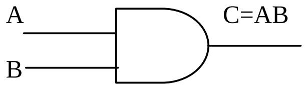
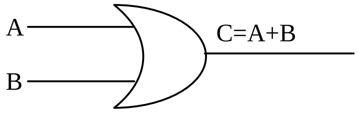
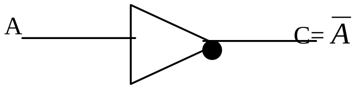
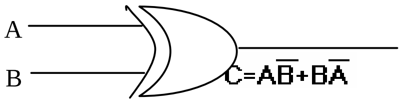
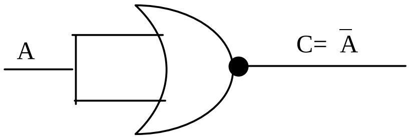
S.NO	GATE	SYMBOL	INPUTS		OUTPUT
			A	B	C
1.	NAND IC 7400		0	0	1
			0	1	1
			1	0	1
			1	1	0
2.	NOR IC 7402		0	0	1
			0	1	0
			1	0	0
			1	1	0
3.	AND IC 7408		0	0	0
			0	1	0
			1	0	0
			1	1	1
4.	OR IC 7432		0	0	0
			0	1	1
			1	0	1
			1	1	1
5.	NOT IC 7404		1	-	0
			0	-	1
6.	EX-OR IC 7486		0	0	0
			0	1	1
			1	0	1
			1	1	0

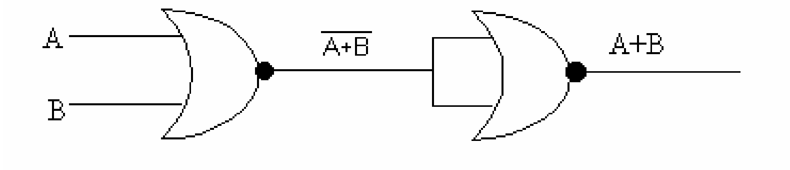
Fig (1)

Realization of all gates using NOR gate:

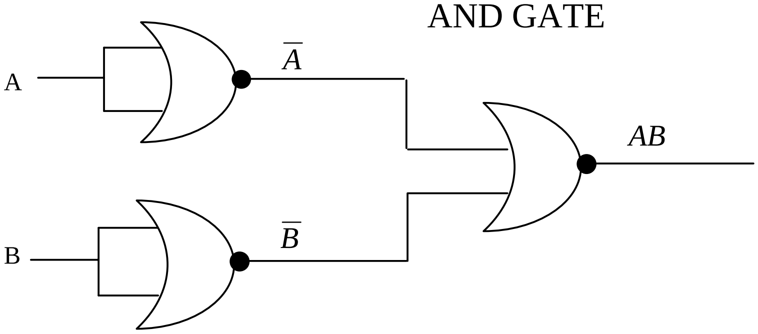
NOT GATE



OR GATE



AND GATE



NAND GATE

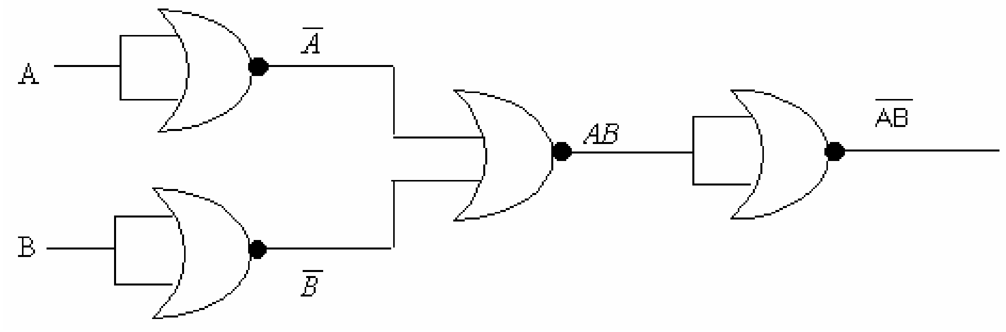
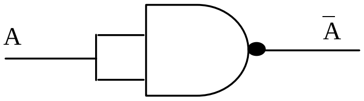


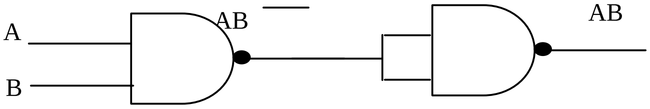
Fig (2.1)

<u>Realization using NAND gate:</u>

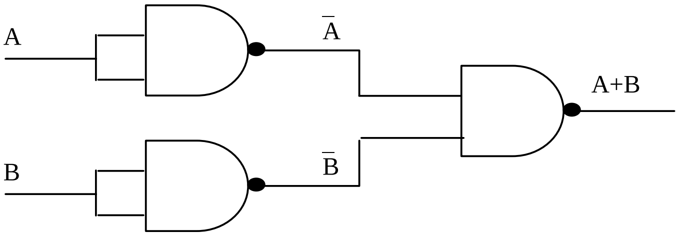
NOT GATE:



AND GATE:



OR GATE:



NOR GATE:

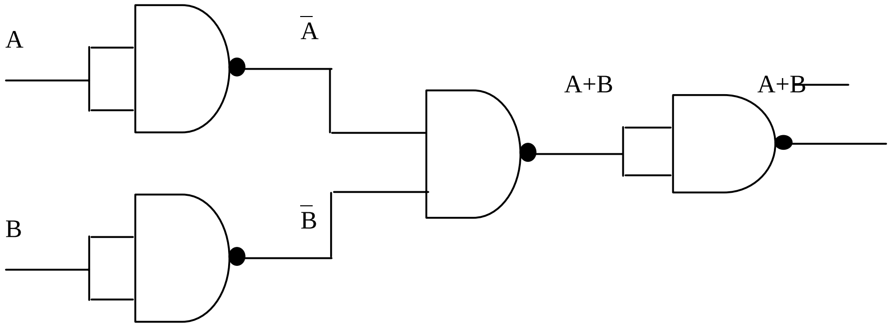
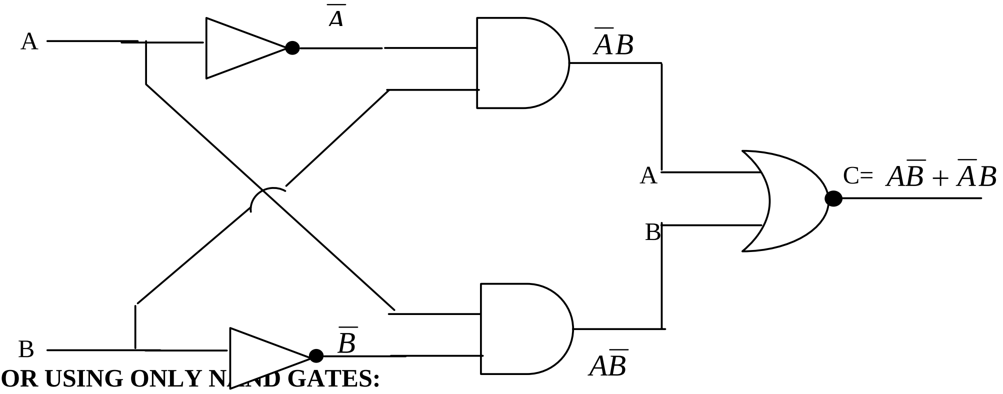


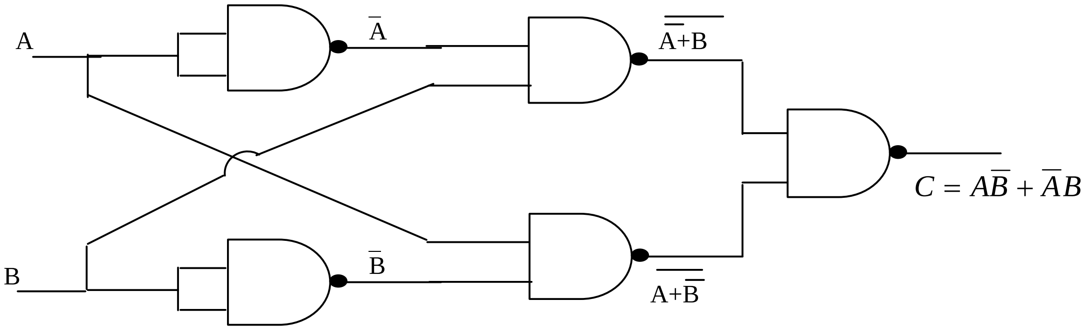
Fig (2.2)

Realization of basic ex-or gate using nand & nor gate:

Basic configuration of EX-OR gate:



EX-OR USING ONLY NAND GATES:



EX-OR USING ONLY NOR GATES:

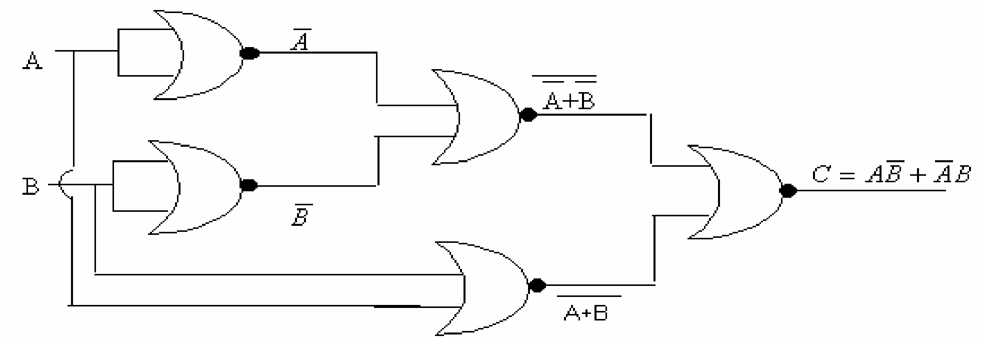
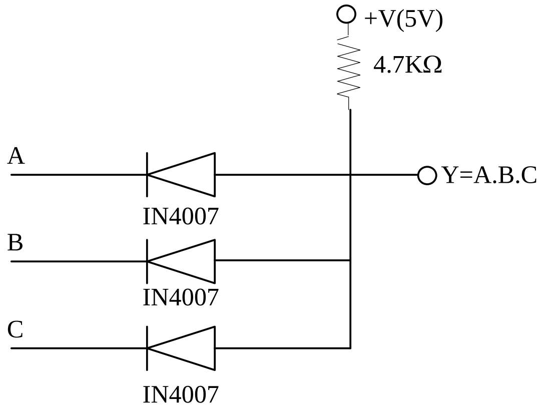


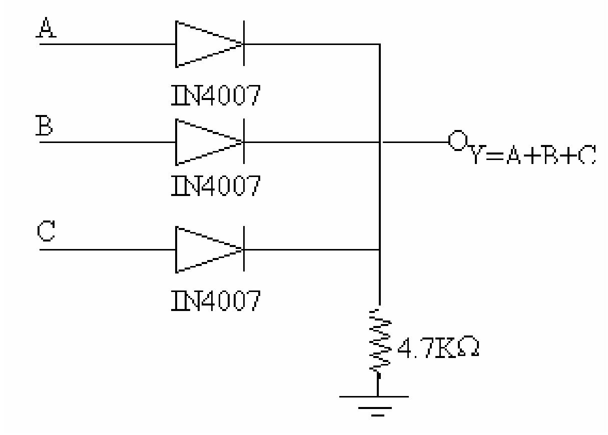
Fig (3)

II.Verifying the logic gates using discrete components:

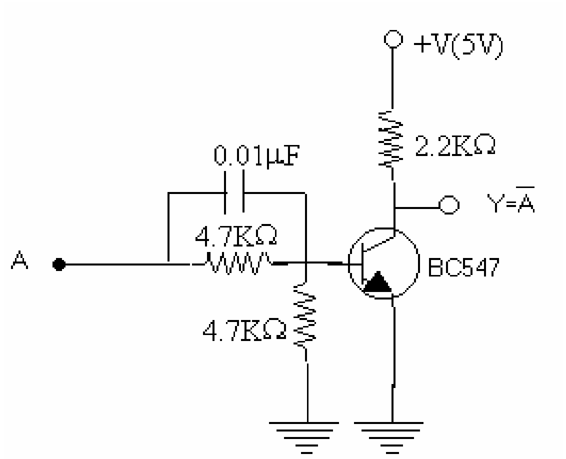
AND GATE:



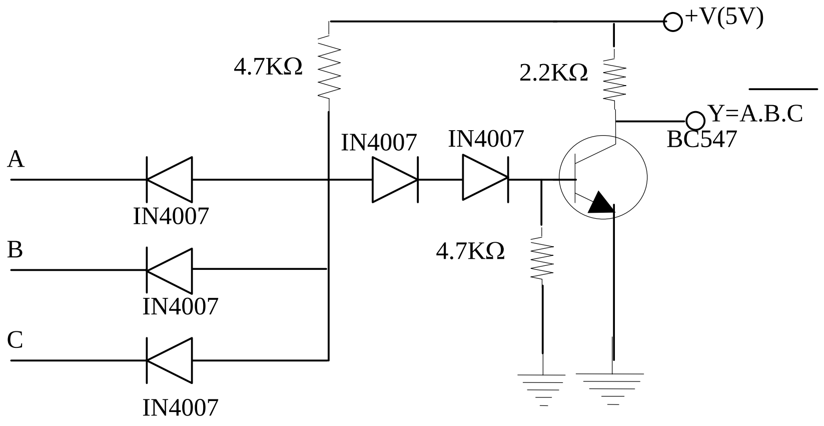
OR GATE:



_NOT GATE:



NAND GATE:



NOR GATE:

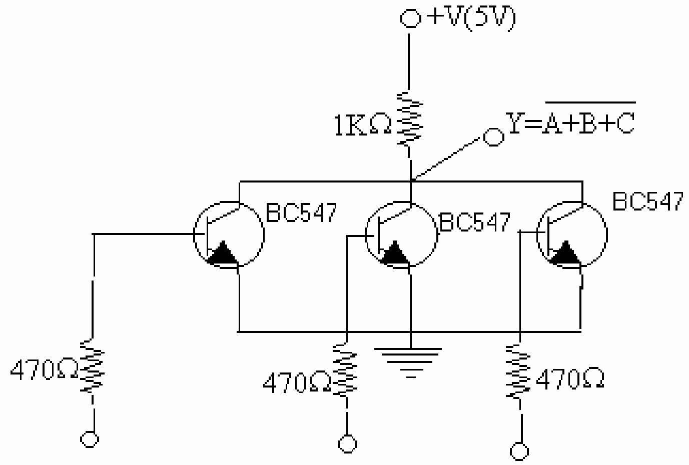


Fig (4)

Procedure:

1. Connect the logic gates as shown in the figure1.
2. Feed the logic signals 0 or 1 from the logic input switches at the inputs A & B.
3. Monitor the output using logic output LED indicators.
4. Repeat steps 1 to 3 for NOT, AND, OR & NOR operations.
5. Connect the logic gates as shown in figure 2.1 & 2.2 and repeat the steps 2 through 3.
6. Connect the logic gates as shown in figure 3 and repeat the steps 2 and 3 Verify the truth table for EX – OR gate.
7. Implement the logic gates using discrete components (fig 4) and verify the truth tables.

Result: Truth tables of all logic gates have been verified.

Questions:

1. Why NAND & NOR gates are called universal gates?

2. Realize the EX – OR gates using minimum number of NAND gates?

3. Give the truth table for EX-NOR (EX-OR+NOT) and realize using NAND gates?

4. Realize the given logic function using NAND and also using NOR gates?

$$f = \overline{A}BC + \overline{A}\overline{B}C + A\overline{B}\overline{C}$$

5. Explain the operation of NAND gate when realized using discrete components?

6. In what regions does the transistor is operated such that it behaves like a Switch?

7. What are the logic low and High levels of TTL IC’s and CMOS IC’s?

8. Compare TTL logic family with CMOS family?

9. Which logic family is called fastest and which logic family is called low power dissipated?.

10. Explain the operation of OR, NOR gates when realized using discrete Components?

11. Why the transistor operates as NOT gate?

RS, JK , D AND T FLIP – FLOP

Aim:

To verify the truth table of

a) RS Flip Flop using Logicgates c) D Flip Flop-IC 7474
b) JK Flip Flop-IC 7476 d) T Flip Flop using JKFlip-Flop.

Apparatus :-

1. RS, JK, D and T flip-flops Trainer Kit.
2. Set of Patch chords.

RS Flip-Flop:

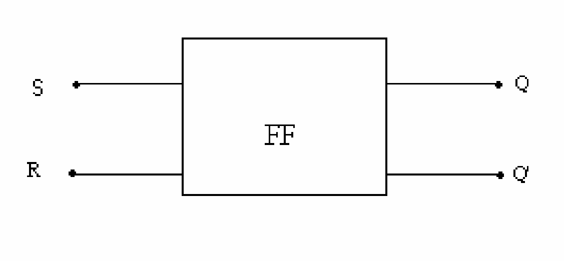
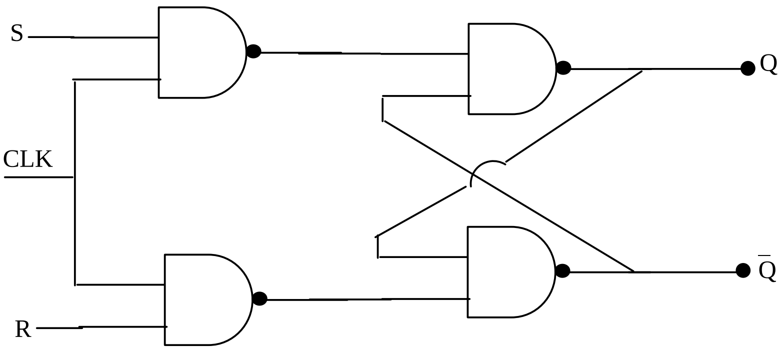


Fig1. RS Flip-Flop

RS Flip-Flop Clocked version:



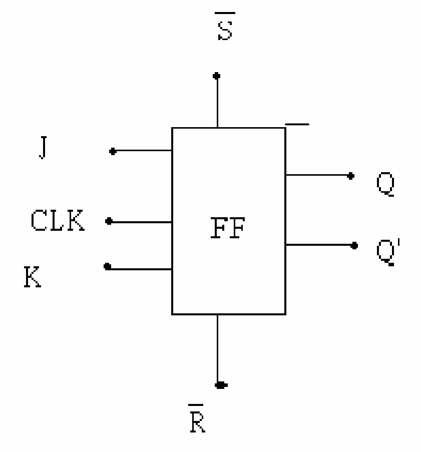
Truth table –1 for RS Flip Flop

INPUTS R	 S	OUTPUT Q	 Q’	COMMENT
0	0	1	1	Indeterminent
0	1	1	0	Set
1	0	0	1	Reset
1	1	Indeterminate		No change

Procedure:

1. Construct the RS flip flop as shown in figure.
2. Feed the logic signals from the logic input switches observe the logic outputs on the logic level LED indicators. Verify the truth table of clocked RS flip-flops.

JK Flip Flop:



Truth Table-2 for JK flip-flop:

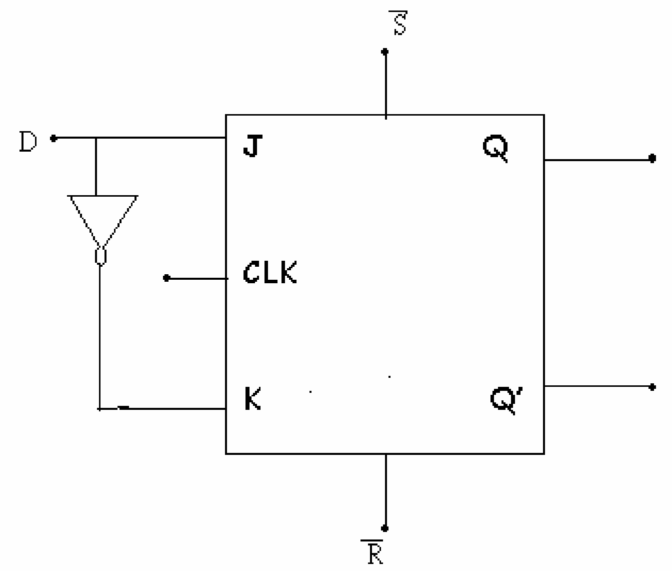
INPUTS					OUTPUTS		COMMENT
Set(s)	Reset(R)	Clock	J	K	Q	Q’	
0	0	X	X	X	1	1	Indeterminent
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	X	0	0	Q0	Q0'	Previous
1	1		0	1	0	1	Reset
1	1	↑	1	0	1	0	set
1	1	↑	1	1	Toggle		Race around

↑

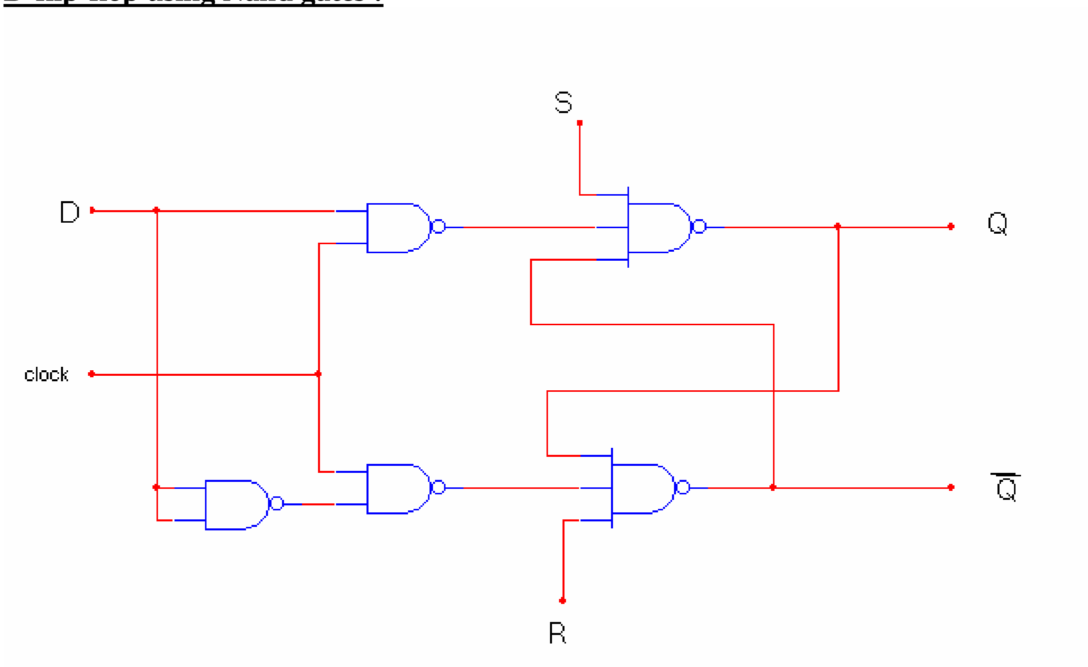
Procedure:

1. Connect S’ , R’, J and K terminals to the logic input switches.
2. Connect the clock terminals to bounceless pulser high or low.
3. Connect Q and Q’ terminals to logic output indicators.
4. Set the S’, R’, J and K Signals by means of the switches as per the truth table–2 verify the Q and Q’ outputs .

D-Flip -Flop:



D-flip-flop using Nand gates :



S’	R’	CLOCK	D	Q	Q’	COMMENT
0	0	X	X	1	1	Race
0	1	X	X	1	0	Set
1	0	X	X	0	1	Reset
1	1		1	1	0	Data Transfer
1	1	↑	0	0	1	Data Transfer

↑

Truth Table - 3

Procedure:

1. Connect S’, R’ and D terminal to the logic input switches.
2. Connect the clock terminals to bounceless pulser high or low.
3. Connect Q and Q’ terminals to logic output indicators.
4. Set the S’, R’ and D signals by means of the switches as per TruthTable–3. Verify the Q and Q’ outputs.

T – Flip Flop:

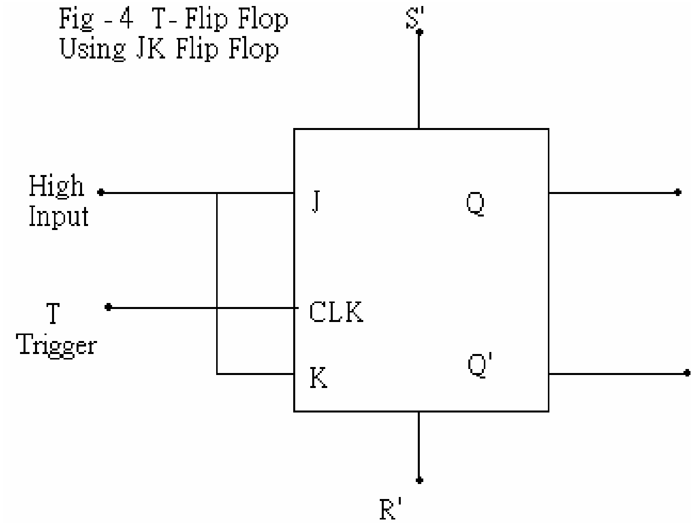


Fig - 4 T- Flip Flop
Using JK Flip Flop

J & K	S	R	CLOCK (T)	Q	Q’	COMMENT
1	0	0	X	1	1	Race
1	0	1	X	1	0	Set
1	1	0	X	0	1	Reset
1	1	1	↑	Q'_{n-1}	Q_{n-1}	Data Transfer

Truth Table - 4

Procedure:

1. Connect S’ and R’ Terminals to the logic input switches.
2. Set J and K permanently to high by means of input switches.
3. Connect the clock terminals (T) to the bounceless pulser high or low.
4. Connect Q and Q’ terminals to logic output indicators.
5. Set the S’ and R’ signals by means of the switches as per Truth Table – 4 verify the Q and Q’ outputs.

Result: **V**erified the truth tables of all Flip-Flops.

Questions:-

1. What is the difference between Flip-Flop & latch?
2. Give examples for synchronous & asynchronous i/P’s?
3. What are the applications of different Flip-Flops?
4. What is universal flip-flop?
5. What is the advantage of Edge triggering over level triggering?
6. What is the relation between propagation delay & clock frequency of flip-flop?
7. What is race around in flip-flop & how to over come it?
8. What are not allowed inputs for RS flip flop using NAND & NOR gates?
9. Connect the J K Flip-Flop into D flip-flop and T flip-flop?
10. List the functions of asynchronous inputs?

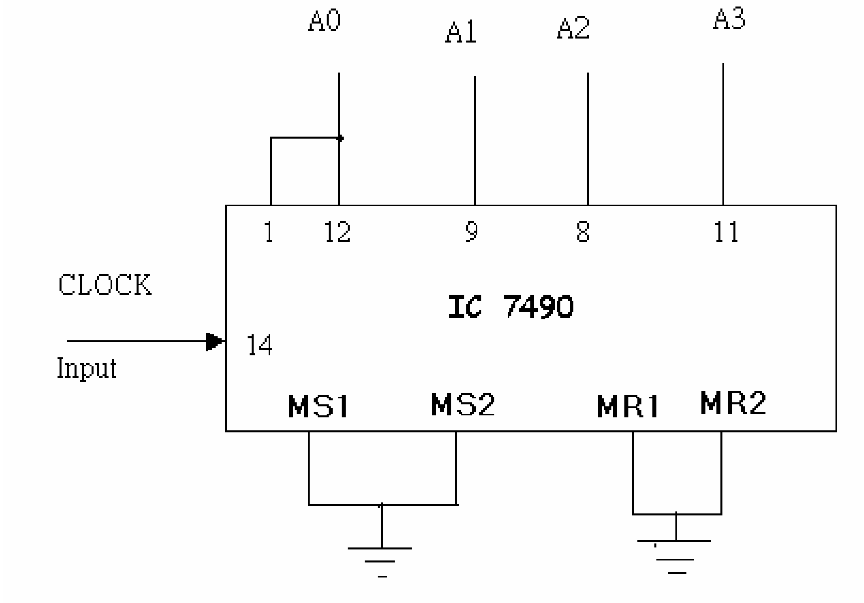
IC7490 DECADE COUNTER

Aim: To construct and verify the working of a single digit decade counter using IC 7490.

Apparatus: 1) IC7490 Decade counter kit

2) Connecting patch cards.

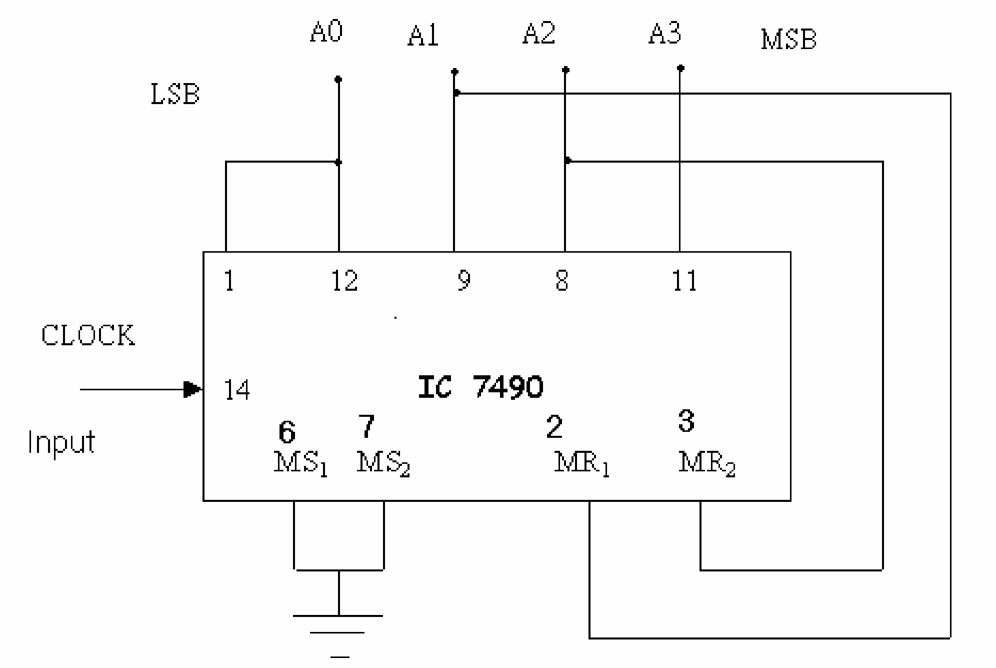
Circuit Diagram :- **OUTPUTS**



Procedure: Fig:1

1. Wire the circuit diagram shown in figure 1.
2. Connect the 1Hz clock to pin CPO.(14)
3. Connect the reset terminals (MR1 & MR2) to high and set terminals (MS1 & MS2) to zero and observe the output.
4. Now connect set and reset inputs to zero and observe the outputs.
5. Record the counter states for each clock pulse.
6. Design mod 6 counter using IC 7490 as shown in fig 2.
7. Record the counter states for each clock pulse.
8. Now Construct decade counter using J – K F/F’s and record the counter states.

MOD 6 COUNTER :

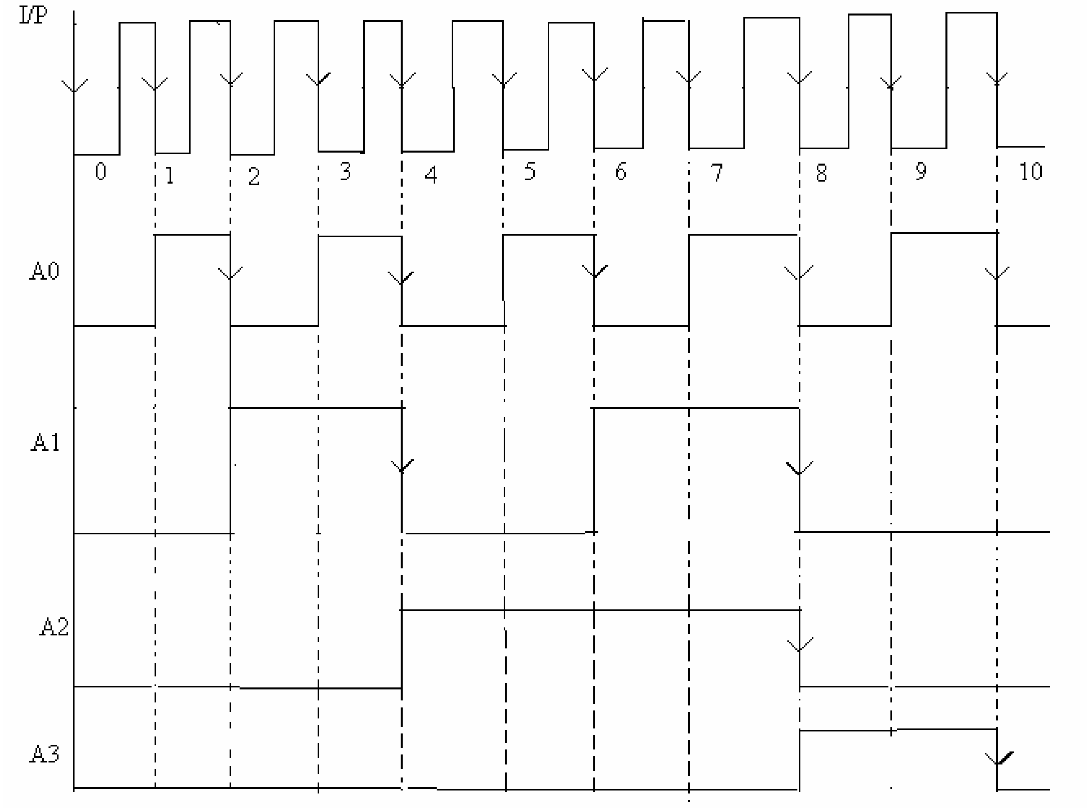


Truth Table:-

A3 Msb	A2	A1	A0 Lsb
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0 →

0000

Expected Wave Forms:-



Result:- Verified the working of a single digit decade counter using IC 7490.

Questions:-

1. Design Mod 7 and Mod 5 counter using IC 7490?`1`1
2. Design Mod 6 counter using JK F/F's?
3. What is the modulus counter?
4. How many numbers of flip-flops are there in decade counter?
5. What is up –down counter?
6. What is the difference between Register &counter?
7. What is BCD counter?
8. If the counter has n-flip-flops. What is the maximum count?
9. Which flip- flops are used in counter?
10. Design a divide –by-96 counter using 7490Ics?

4 – BIT BINARY RIPPLE COUNTER

Aim: To study the operation and working of a 4 – bit binary ripple counter using IC 7493

Apparatus:-

1. 4 – Bit binary ripple counter trainer kit.
2. Set of Patch chords

Theory: The ripple counter is simple and straightforward in operation and construction and usually requires a minimum of hardware. It does, however, have a speed limitation. Each flip-flop is triggered by the previous flip-flop, and thus the counter has a cumulative settling time. Counters such as these are called serial or asynchronous.

The output Q0 must be externally connected to the input CP_1. The input count pulses are applied to input CP_0. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q1, Q2 and Q_3 outputs as shown in the truth table.

A ripple counter can be constructed by use of clocked JK flip-flops. Fig shows four Master-Slaves, JK flip-flops connected in cascade. The system clock, a square wave, drives flip-flop A. the output of A drives B, and output of B drives flip-flop C and output of C drives flip-flop D. All the J and K inputs are tied to $+V_{CC.}$ This means that each flip-flop will change state (toggle) with a negative transition at its clock input. When the output of a flip-flop is used as the clock input for the next flip-flop, we call the counter a ripple counter, or asynchronous counter. The A flip-flop must change states before it can trigger the B flip-flop, and the B flip-flop has to change states before it can trigger the C flip-flop. And the C flip-flop has to change states before it can trigger the D flip-flop the triggers move through the flip-flops like a ripple in water.

The waveforms given in fig show the action of the counter as the clock runs. Every time there is a negative clock transition, flip-flop A change state., Notice that the waveform at the output of flip-flop A is one half the clock frequency. Since A acts as a clock for B, each time the waveform at A goes low, flip-flop B will toggle. notice that the waveform at the output of flip-flop B is one half the frequency of A and one fourth the clock frequency. Since B acts as the clock for C, each time the waveform at B goes low, flip-flop C will toggle .The frequency of the waveform at C is one half that at B, but it is only one eight the clock frequency. Now C acts as a clock for D. Each time the wave form at C goes low,flip-flop D will toggle . The frequency of the waveform at D is one half that at C, but it is only one sixteenth the clock frequency.

Procedure:

1. Switch ON the experimental board by connecting power chord to the AC mains.
2. Connect the Bounceless pulser output to the clock input of 7493 counter.
3. Verify the given mode selection table.

Mod selection table

RESET INPUTS		OUTPUT			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	COUNT			
H	L	COUNT			
L	L	COUNT			

Table - 1

4. Verify the truth table of the 7493 Ripple counter.

.

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H

4-bit Ripple counter pin diagram :

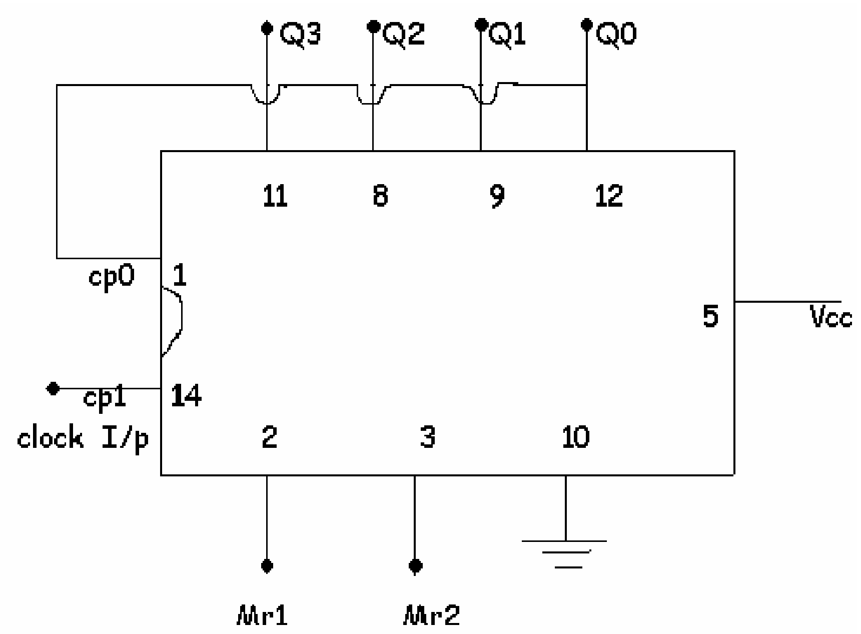


Fig:1

4-bit Ripple counter Logic diagram :

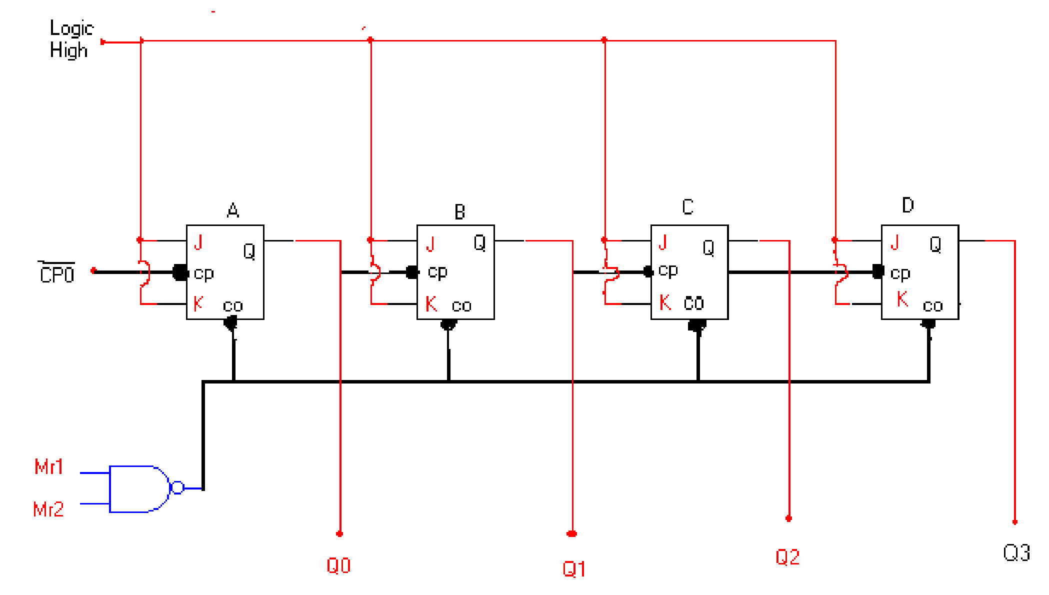
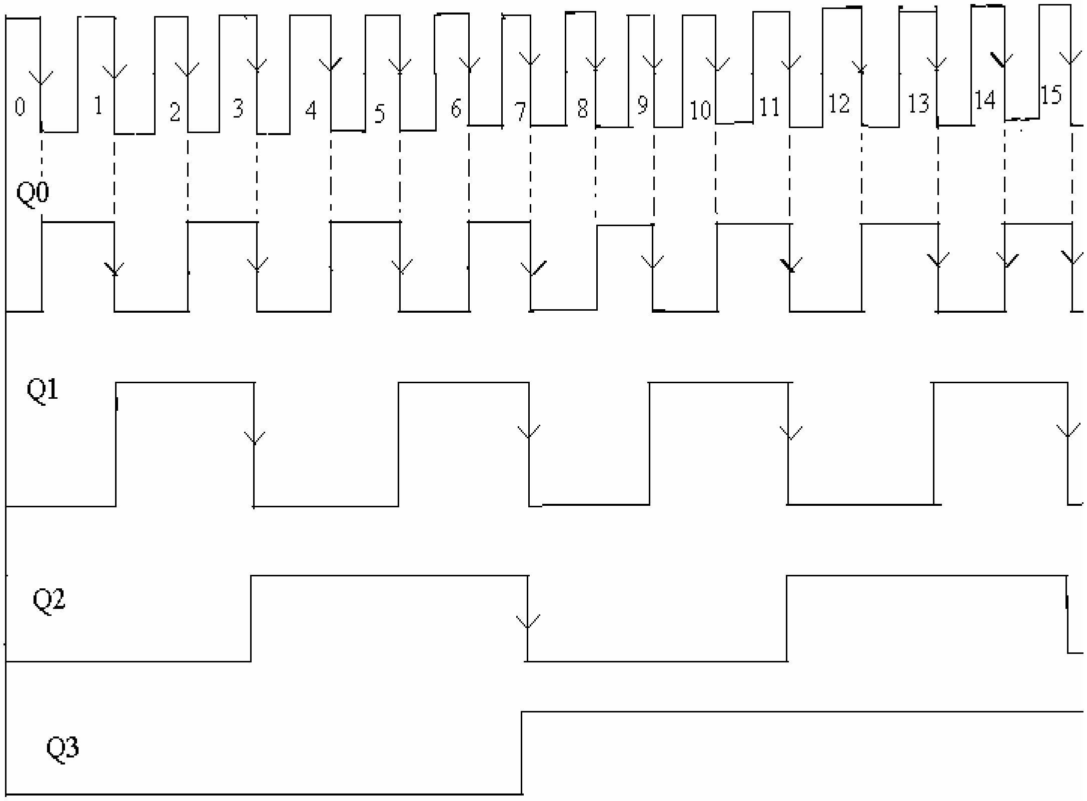


Fig:2

Expected wave forms:-



RESULT :- The operation and working of a 4 – bit binary ripple counter using IC 7493 is verified .

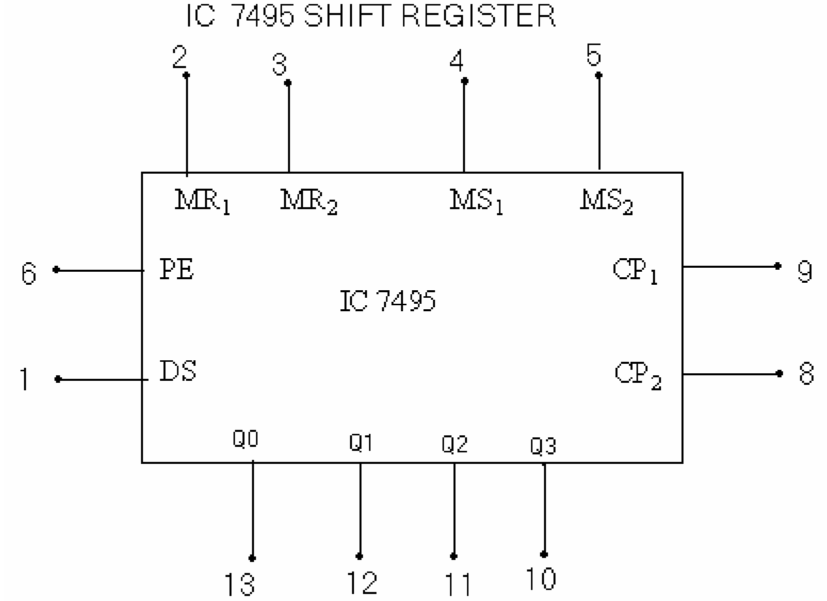
Questions :-

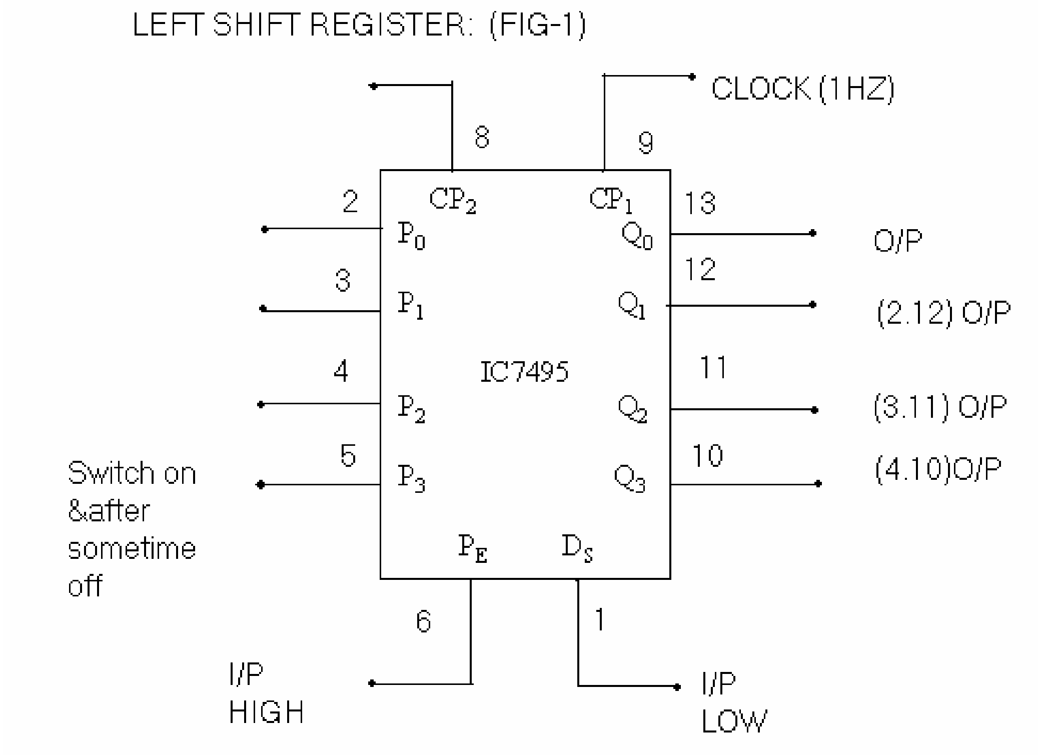
1. What is meant by a Ripple Counter?
2. What is the other name for ripple counter?
3. What is the difference between serial & parallel counter?
4. What is ring counter?
5. What are the applications of presettable counters?
6. What is modulus of counter?
7. What are the applications of counters?
8. What is the difference between Counter and Register?
9. Design a 4-bit binary UP/DOWN ripple counter using T F/Fs?
10. What is the primary disadvantage of asynchronous counters?

IC 7495 SHIFT REGISTER

Aim : To study the operation of the shift register using IC7495 .

Apparatus : 1.Shift register kit
2. Connecting wires.

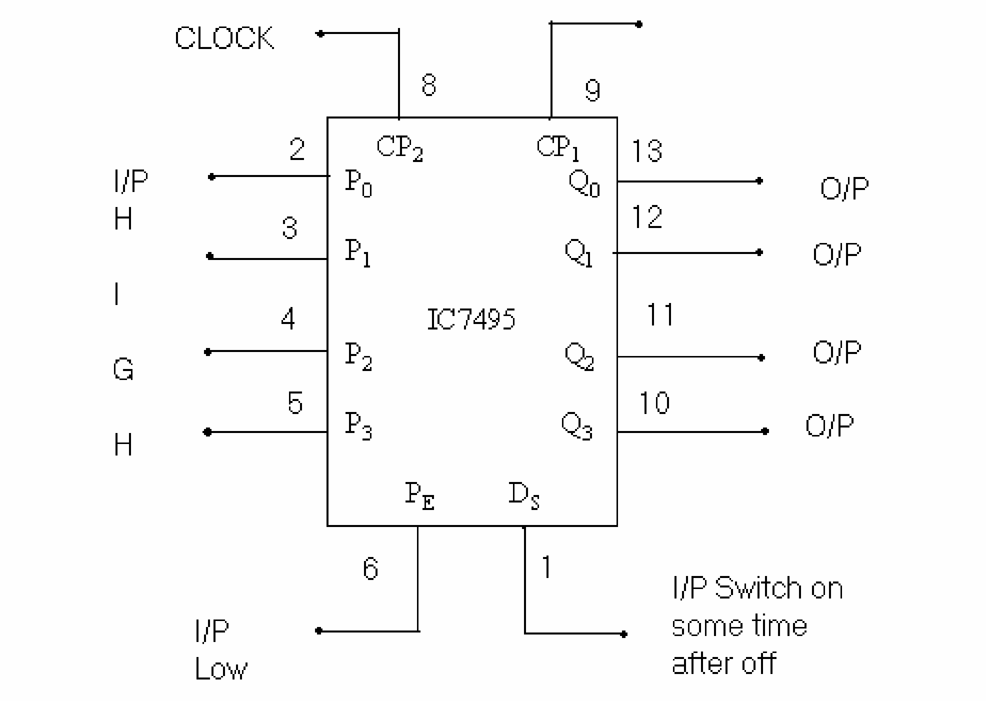




Truth table for left shift register:

Q0(MSB)	Q1	Q2	Q3(LSB)	Y
1	1	1	1	15
1	1	1	0	14
1	1	0	0	12
1	0	0	0	8
0	0	0	0	0

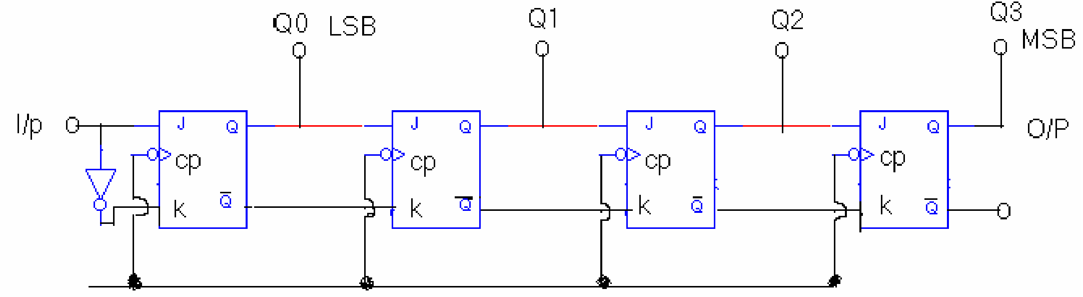
RIGHT SHIFT REGISTER: (FIG . 2)



Truth table for right shift register :

Q0(MSB)	Q1	Q2	Q3(LSB)	Y
0	1	1	1	7
0	0	1	1	3
0	0	0	1	1
0	0	0	0	0

Right shift logic diagram:-



Procedure:

1. Construct 4 – bit left shift register as shown in fig. Connect the output logic level indicators to the outputs of each stage of shift register.
2. Apply 1 Hz CLOCK C_P input to 9.
3. In left shift register 2&12, 3&11,4&10 pins shorted and given to the Output.
4. Switch ON 5th pin some time and after off it.
5. Put the 6th pin in high and 1st pin in low position.
6. Observe the left shifting through the shift register.

For right shift :

7. Apply 1 Hz CLOCK C_P input to 8.
8. Connect the pin nos. 1,2,3,4,5,6 to the logic inputs.
9. Put the 6th pin low position, 2, 3, 4, 5 pin nos. in high position.
10. Switch ON 1st pin some time and after off it.
11. Observe the Right shifting through the shift register.

Result:- The operation of the Right shift &left shiftregister using IC7495 has been verified.

Questions :-

1. What are the applications of shift registers?
2. Which flip flop is used in shift register?
3. What is universal shift register?
4. What are different types of shift registers?
5. Which shift gives multiplication by 2?
6. Which shift gives division by 2?
7. Can we use shift register as counter?
8. How timing sequences can be generated using shift registers?
9. Explain the working of 4-bit SIPOshift register?
10. What are glitches in digital circuits?

UNIVERSAL SHIFT REGISTER

Aim :- To study the following applications of the Universal shift register using IC 74194.

a . Shift Right Logic

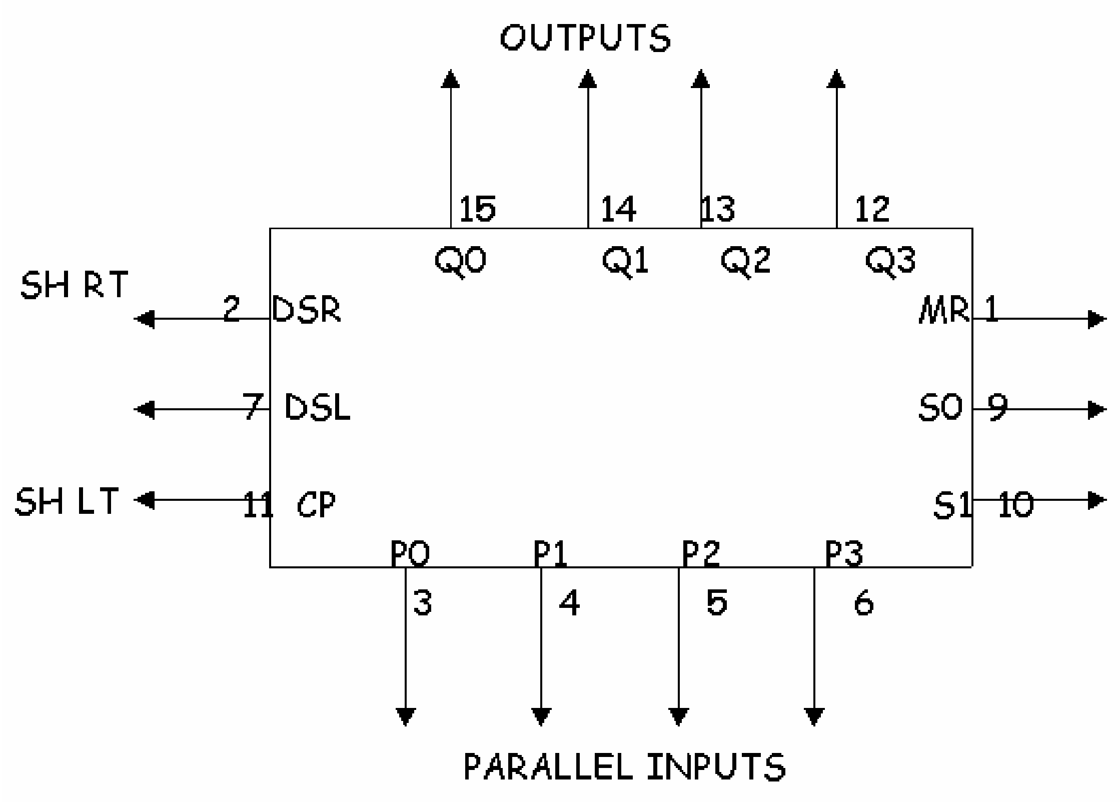
b . Shift Left Logic

c . Parallel Load

Apparatus :-

1. **Universal Shift Register using IC 74194 Trainer boards.**
2. **5v fixed DC power supply.**

Circuit Diagram:-



Procedure:-

STEP : 1. MASTER RESET

Set the inputs as below and observe the out puts as per table 1

MR	S1	S0	DSR	DSL	CP	P0	P1	P2	P3	Q0	Q1	Q2	Q3
0	X	X	X	X	X	X	X	X	X	0	0	0	0

Truth table –1

A logic ‘ 0 ‘ on MR resets all outputs to logic ‘ 0 ‘ irrespective of other inputs.

STEP :2 PARALLEL LOAD

In this step we load the data parallel. Set the inputs as below and observe the outputs.

MR	S1	S0	DSR	DSL	CP	P0	P1	P2	P3	Q0	Q1	Q2	Q3
1	1	1	x	x	CLK	1	1	1	1	1	1	1	1

Truth Table –2

Here when S1 & S0 are both logic ‘ 1 ‘ the input data is transferred parallely to output at the clock positive transition change the input data and observe the change at the output .

STEP : 3 . SHIFT LEFT LOGIC ‘ 0 ‘.

Set Q0 , Q1 , Q2 , Q3 to ‘ 1 1 1 1 ‘ by putting DSL to Logic ‘ 1 ‘ .

While running the above step, change the logic input DSL to logic ‘ 0 ‘

And S_0 to logic ‘ 0 ‘ in the same sequence .Observe the following outputs after each clock pulse and verify .

CONDITION	n CLOCK PULSES	**Q0**	**Q1**	**Q2**	**Q3**
MR = 1	0	1	1	1	1
S0 = 0	1	1	1	1	0
S1 = 1	2	1	1	0	0
DSL = 0	3	1	0	0	0
DSR = X	4	0	0	0	0

Truth Table – 3

In the sequence 4 clock pulses logic ‘ o ‘ s are shifted left successively with each clock pulse .

STEP : 4 . SHIFT LEFT LOGIC ‘ 1 ‘ S

Set the Q0 Q1 Q2 Q3 to 0 0 0 0 by setting DSL input to logic ‘ 0 ’.

Now switch DSL input to logic ‘ 1 ‘ and observe the shifting of logic ‘ 1 ‘ s to left as below . Observe the following outputs after each clock pulse and verify.

CONDITION	n CLOCK PULSES	Q0	Q1	Q2	Q3
MR = 1	0	0	0	0	0
S0 = 0	1	0	0	0	1
S1 = 1	2	0	0	1	1
DSL = 1	3	0	1	1	1
DSR = X	4	1	1	1	1

Truth Table – 4

STEP : 5 . SHIFT RIGHT LOGIC ‘ 0 ‘

Set the Q0 Q1 Q2 Q3 to 1 1 1 1 by setting DSR input to logic ‘ 1 ‘ .

Repeat step 4 and parallel load logic ‘ 1 ‘ s in all the 4 outputs .

Change the logic inputs of DSR to logic 0 and then of S1 to logic ‘ 0 ‘

in the same sequence . Observe the following outpus after each clock pulse and verify .

CONDITION	n CLOCK PULSES	Q0	Q1	Q2	Q3
MR = 1	0	1	1	1	1
S0 = 1	1	0	1	1	1
S1 = 0	2	0	0	1	1
DSL = X	3	0	0	0	1
DSR = 0	4	0	0	0	0

Truth Table –5

STEP : 6 SHIFT RIGHT LOGIC ‘1 ‘ s

Now at this condition of all ‘ 0 ‘ at the outputs switch DSR to logic ‘1’ this will enable all logic as serial data and logic ‘ 1 ‘ s will be shifted successively with each clock pulse as shown below .Observe the following table and verify the outputs .

CONDITION	n CLOCK PULSES	Q0	Q1	Q2	Q3
MR = 1	0	0	0	0	0
S0 = 1	1	1	0	0	0
S1 = 0	2	1	1	0	0
DSL = X	3	1	1	1	0
DSR = 1	4	1	1	1	1

STEP : 7 . In the above steps for shift left or shift right operation ,(step 3 4 5 6) if both the S0 &S1 switches are forced to logic ‘ 0 ‘, then shifting operation will cease and whatever is the output data it will freeze or hold . Observe this condition and verify .

CONDITION	n CLOCK PULSES	Q0 Q1 Q2 Q3

MR = 1
S0 = 0
S1 = 0
DSL = 0
DSR = 0
	1
	1
	1
	1
	1
		Previous data just before S0 &S1 both switched to logic ‘ 0 ‘.

Truth Table –7

Result:- Verified the applications of the Universal shift register using IC 74194

Questions: -

1. What is the universal shift register?
2. In which circuits shifting and rotating circuits are used?
3. Which flip-flops are used in shift registers?
4. Which flip-flop is universal flip-flop?
5. What is the difference between shifting and rotating data?
6. What is register?
7. What is meant by parallel in &parallel out Shift register?
8. State various applications of Shift register?
9. List the basic types of shift register in terms of data movement?
10. Determine the output status of a 4-bit SIPO shift register, after 3 clock pulses if the I/P terminal is held high?

3 TO 8 DECODER

Aim: To verify operation of the 3 to 8 decoder using Ic 74138**.**

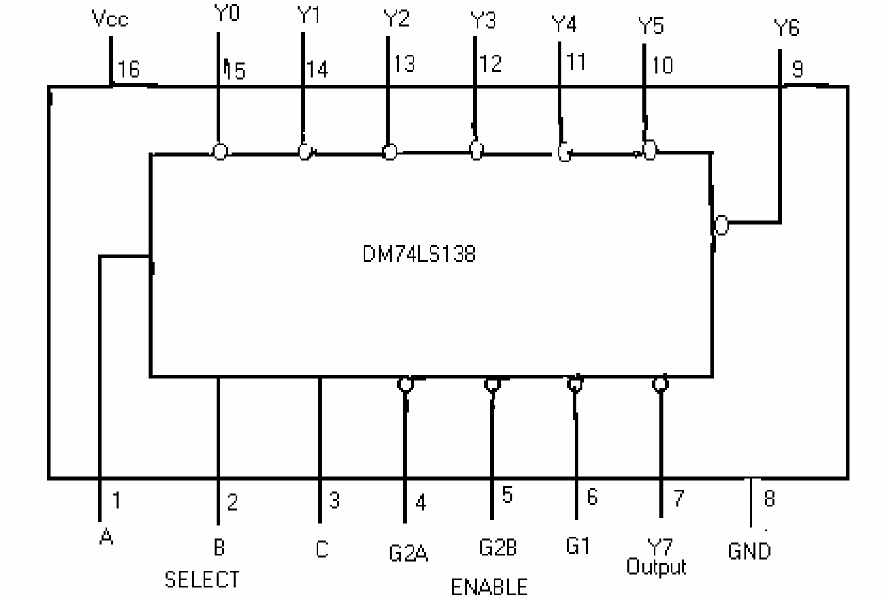
Apparatus : 1 .3 to 8 decoder Ic 74138 kit.

2 **.**Patch chords **.**

Theory:

- A decoder is a combinational circuit that connects the binary information from ‘n’ input lines to a maximum of 2^n unique out put lines .The IC 74138 accepts three binary inputs and when enable provides 8 individual active low outputs . The device has 3 enable inputs .Two active low and one active high.

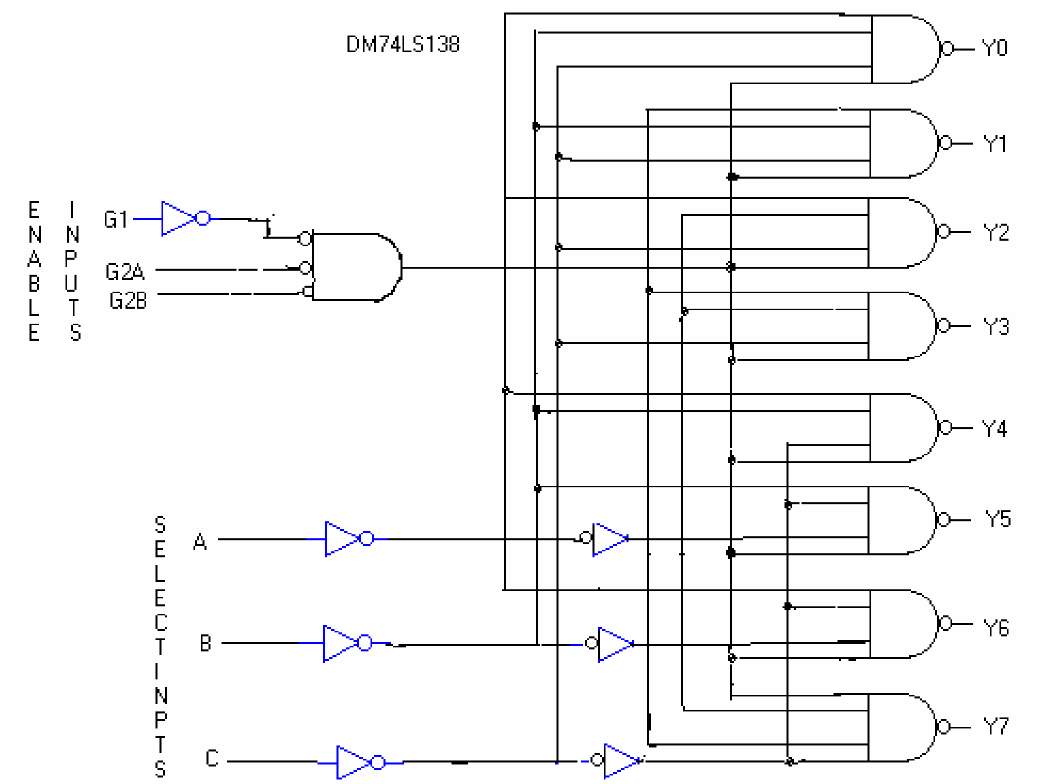
Circuit Diagram :



Truth Table: -

INPUTS						OUTPUTS							
ENABLES													
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
0	x	x	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

Logic Diagram:



Procedure :-

1. Make the connections as per the circuit diagram .

2. Change the values of G1,G2A,G2B,A,B,and C, using switches.

3. Observe status of Y0, to Y7 on LED’s.

4. Verify the truth table.

Result:- Verified the Operation of 3 to 8 Decoder.

Questions:-

1. What are the applications of decoder?
2. What is the difference between decoder & encoder?
3. For n- 2^n decoder how many i/p lines & how many o/p lines?
4. What are the different codes & their applications?
5. What are code converters?
6. What is even parity & odd parity?
7. Which gate can be used as parity generator & checker?
8. Using 3:8 decoder and associated logic, implement a full adder?
9. Implement a full subtract or using IC 74138?
10. What is the difference between decoder and demux?

4 – BIT COMPARATOR

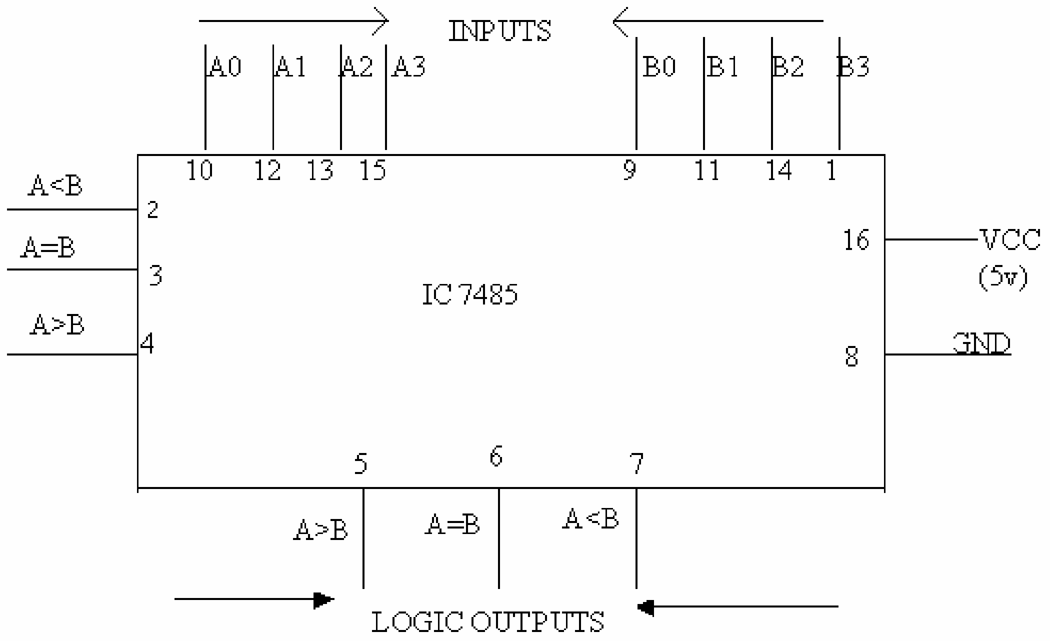
Aim:- To study the operation of 4-bit Magnitude Comparator using Ic7485.

Apparatus :- 1 . Power supply . 2. IC7485 4-bit Comparator kit.

Theory :-

Magnitude Comparator is a logical circuit , which compares two signals A and B and generates three logical outputs, whether A > B, A = B, or A < B . IC 7485 is a high speed 4-bit Magnitude comparator , which compares two 4-bit words . The A = B Input must be held high for proper compare operation.

CIRCUIT DIAGRAM -



Procedure:-

1. Connect the circuit as shown in fig. Feed the 4-bit binary words A0, A1 , A2 , A3 and B0 , B1 , B2 , B3 .from the logic input switches.

2 . Pin 3 of IC 7485 should be at logic 1 to enable compare operation.

3 . Observe the output A>B, A=B , and A<B on logic indicators. The outputs must be 1 or 0 respectively.

4 . Repeat the steps 1 ,2 and 3 for various inputs A0 ,A1 , A2 , A3 and B0 , B1 , B2 , B3 and observe the outputs at A>B , A=B and A<B .

Verification Table :

A3 A2 A1 A0	B3 B2 B1 B0	OUTPUT
1 1 1 1	1 1 1 0	A>B
1 0 0 0	1 0 0 0	A=B
0 0 0 0	1 1 1 1	A<B

Result:- Verified the operation of 4-bit magnitude comparator using Ic 7485 .

Questions :-

1. What is Comparator?
2. What are the applications of Comparator?
3. Which logic is used as 1 bit comparator?
4. What are different arithmetic comparisons?
5. Can we use subtractor & divider as comparators?
6. What is the significance of 74 on IC’s?
7. Design a 5 bit comparator using a single IC 7485, and one gate?
8. Design a 2 bit comparator using a single Logic gates?
9. Design a 8 bit comparator using a two numbers of IC 7485?
10. Design a 24 bit comparator using a six numbers of IC 7485? .

8:1 Multiplexer

Aim: To verify the truth table of a given 8 to 1 Multiplexer and 1 to 8 De-Multiplexer using IC 74151 and 74138 .

Apparatus:

1. 8 to 1 Multiplexer Trainer kit .
2. Connecting patch chords.

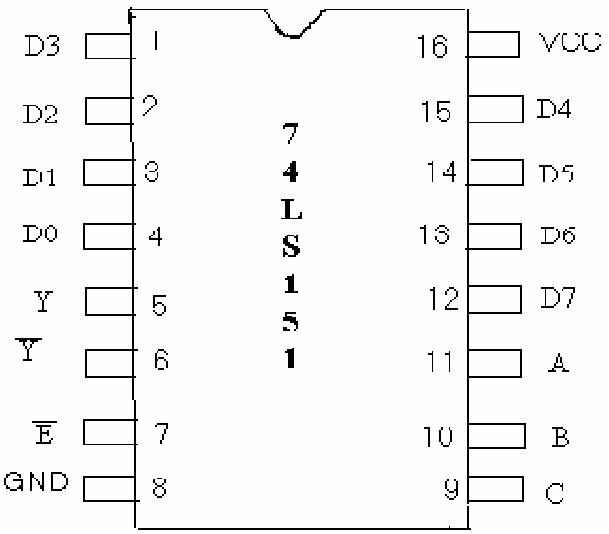
Theory:

Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called as data selector because the output bit depends on the input data bit that is selected.

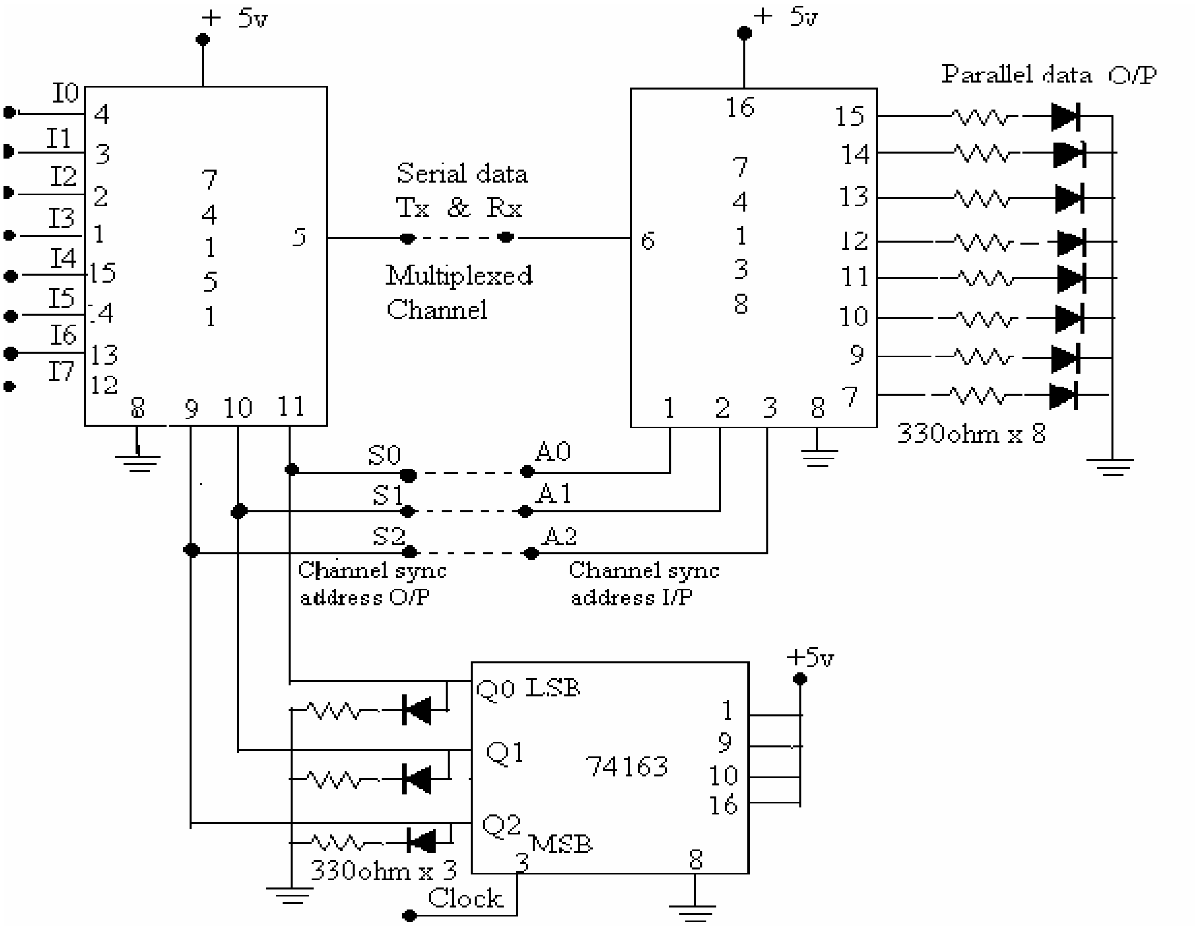
The general idea about the multiplexing the circuit has N input signals, M control signals and 1 output signal.

8 X 1 Multiplexer has 8 input signals and one output signal, three data control or select lines. These data control lines are nothing but 3-bit binary code on the data control signal inputs which will allow the data on the corresponding data input to pass through to the data output

Pin Diagram:-



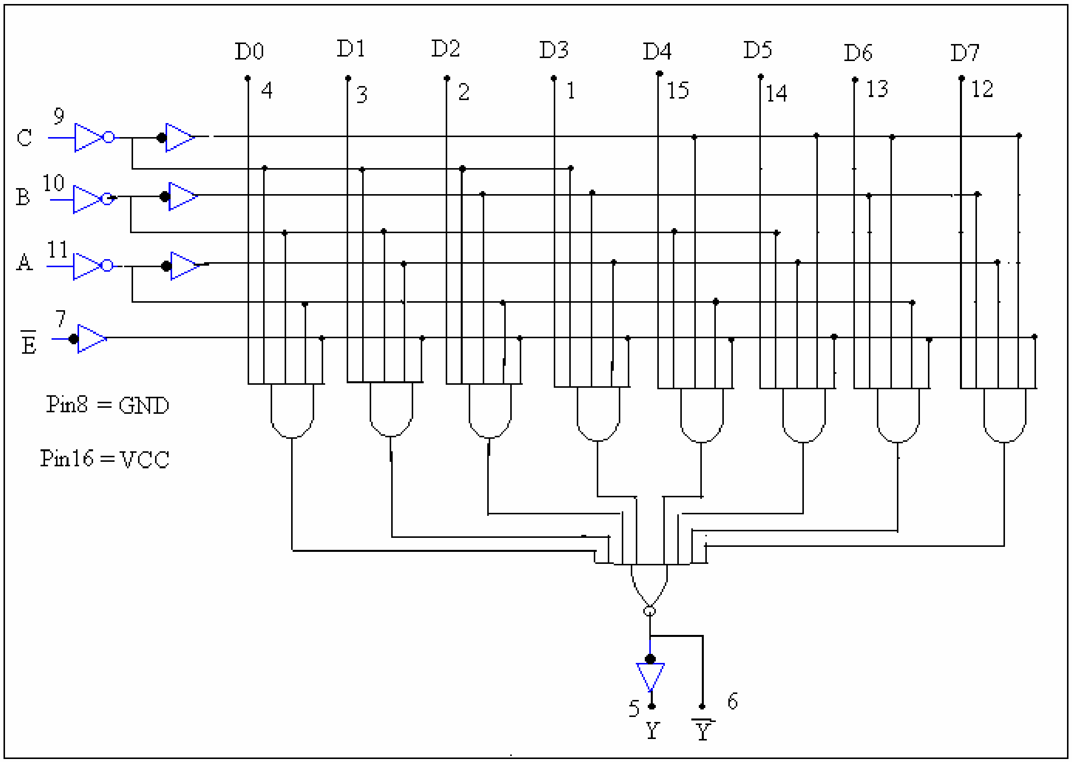
Circuit Diagram:



.**Truth Table:**

Q2	Q1	Q0	I0	I1	I2	I3	I4	I5	I6	I7	Y
0	0	0	0	X	X	X	X	X	X	X	L
0	0	0	1	X	X	X	X	X	X	X	H
0	0	1	X	0	X	X	X	X	X	X	L
0	0	1	X	1	X	X	X	X	X	X	H
0	1	0	X	X	0	X	X	X	X	X	L
0	1	0	X	X	1	X	X	X	X	X	H
0	1	1	X	X	X	0	X	X	X	X	L
0	1	1	X	X	X	1	X	X	X	X	H
1	0	0	X	X	X	X	0	X	X	X	L
1	0	0	X	X	X	X	1	X	X	X	H
1	0	1	X	X	X	X	X	0	X	X	L
1	0	1	X	X	X	X	X	1	X	X	H
1	1	0	X	X	X	X	X	X	0	X	L
1	1	0	X	X	X	X	X	X	1	X	H
1	1	1	X	X	X	X	X	X	X	0	L
1	1	1	X	X	X	X	X	X	X	1	H

Logic Diagram:-



Procedure:

1. Switch on the trainer by connecting power chord to the AC mains
2. By using pulsar switch reset the control signals (Q_2 Q_1 Q_0) to 0 0 0
3. Connect the output terminals (pin 5) to the output LEC indicator.
4. Apply logic 1 to I_0 input (pin 4) by using the switch. The output LED indicator glows
5. Apply logic 0 to I_0 input (pin 4) by using the switch. The output LEC indicator is off.
6. Verify the truth table by changing the control 3 signal states using pulsar switch from 000 to 111

Result:

The truth table of 8 to 1 multiplexer has been verified.

Questions:-

1. What is multiplexer?
2. What are the applications of multiplexer?
3. What is the difference between multiplexer & demultiplexer?
4. In 2^n to 1 multiplexer how many selection lines are there?
5. How to get higher order multiplexers?
6. Impliment full subtractor using demux?.
7. Impliment a 8:1 mux using 4:1 muxes?.
8. Design full adder using 8:1 Mux Ics?.
9. Design a BCD-to- gry code connecter using 8:1 muxes?
10. Draw and explain the design of a32:1 mux using 8:1 MUX and 4:1 MUX.?

16 – LINE TO 1 – LINE MULTIPLEXER

Aim: To study the circuit of 16 – line to 1- line multiplexer using 74150 .

Apparatus:-

1. 16 line to 1 line Multiplexer Trainer
2. Set of Patch Chords and User Manual.

Theory:- Multiplex means " Many to one " . A multiplexer is a circuit with many inputs but only one out put by applying control signals. We can steer any input to the output. Multiplexer is also called a data selector. The input data bits are D0 (I0) to D15 (I15), only one of these is transmitted to the output. Control word ABCD (S3 S2 S1 S0) determines which data bit is passed to the out put.

For example ABCD=0000 Output=D0(I0) when ABCD=1111 output =D15(I15).

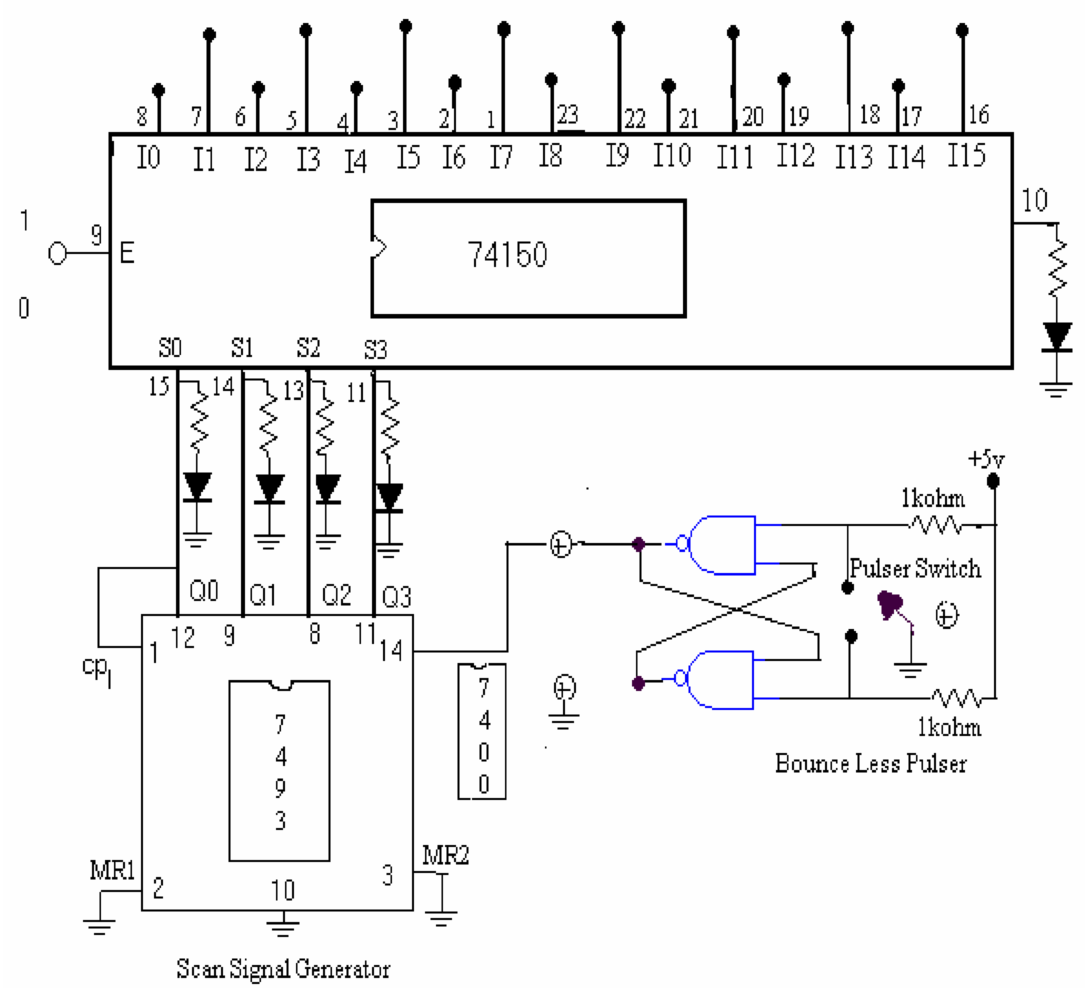
Procedure:-

1. Switch ON the experimental board by connecting power chord to the A C mains.
2. Connect the manual pulser output to the input of the scan signal generator and press the pulser switch until we get Q_3, Q_2, Q_1, $Q_{0,}$ equal to 0000.
3. Verify the Table – 2 by changing the counting sequence with pulser switch from 0000 to 1111.

S0	S1	S2	S3	E	Y(Channel selected at o/p)
0	0	0	0	0	I0
0	0	0	1	0	I1
0	0	1	0	0	I2
0	0	1	1	0	I3
0	1	0	0	0	I4
0	1	0	1	0	I5
0	1	1	0	0	I6
0	1	1	1	0	I7
1	0	0	0	0	I8
1	0	0	1	0	I9
1	0	1	0	0	I10
1	0	1	1	0	I11
1	1	0	0	0	I12
1	1	0	1	0	I13
1	1	1	0	0	I14
1	1	1	1	0	I15

Circuit Diagram:-

16-LINE TO 1-LINE MULTIPLEXER



Function Table: H - High voltage level; L – Low Voltage level X - Don’t care

					INPUTS																O / P
S_3	S_2	S_1	S_0	E’	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	Y ’
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

Result:- The circuit of 16 – line to 1- line multiplexer using 74150 is verified.

Questions:-

1) What is meant by a multiplexer?
2) List the applications of multiplexer?
3) Why scan signal generator is required for Multiplexer?.
4) How many number of 8x1 multiplexers is required to have 16x1 mux?.
5) Impliment a 16:1 mux using 4:1 Mux Ics .
6) Draw the circuit diagram of a 1:4 demux using AND .Explain its operation?
7) Design a BCD-to-7 segment decoder with active low out puts using dual 4:1 muxs and some gates.?
8) “Multiplexer is called universal logic gate” Justify it?.
9) How can multiplexer work as a parallel to serial converter?
10) Design a 1:40 demux using BCD-to-decimal decoders?.

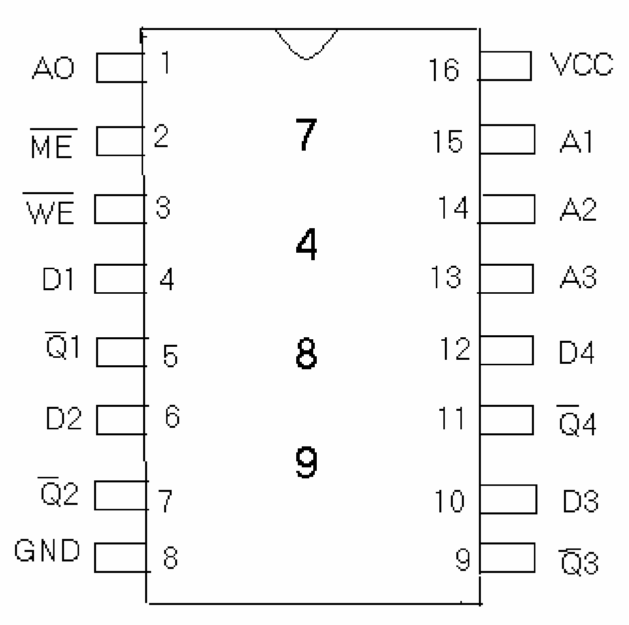
STUDY OF RAM IC 7489

Aim: **- To study the operation of the RAM Ic7489.**

Apparatus: **- 1. RAM IC 7489 Trainer kits.**

2. Connecting wires.

Pin Diagram: -



Operation:-

- **RAM IC 7489 is 16 words x 4-bit Read/WriteMemory.**
- **The Truth Table for the RAM IC 7489 is given below.**

Memory Enable	**Write Enable**	**Operation**
H	**X**	**All data outputs are high**
L	**H**	**Read mode (data outputs are compliment of the RAM content).**
L	**L**	**Write mode (data inputs are written on to the memory; dataoutputs are compliment of the RAM content).**

- **The memory Enable pin is used to select 1- of-n ICs i.e. like a Chip Select signal.**

For simply city, the memory enable pin is permanently held low.

- **The address lines are given through an up /down counter with preset capability.**
- **The set address switch is held high to allow the user choose any location in the RAM, using the address bits.**
- **The address and data bits are used to set an address and enter the data.**
- **The ‘ Read/Write ‘ switch is used to write data on to the RAM.**

Procedure:

This experiment has 3 stages – Clearing the memory, data entry (Write operation) and data verification (Read operation).

Clearing the Memory: -The RAM IC 7489 is a volatile memory. This means that it will lose the data stored in it, on loss of power. However, this dose not means that the content of the memory becomes 0h, but not always. The RAM IC 7489 does not come with a ‘ Clear Memory ‘ signal. The memory has to
be cleared manually.

1. Position the ‘ **Stack/Queue**’ switch in the **‘ Queue**’ position.
2. Position the ‘**Set Address’** switch in the ‘**1**’ position.
3. Set the address bits to 0h (first byte in the memory)
4. Position the **‘Set Address’** switch in the **‘0’** position to disable random access and enable the counter.
5. Position the **’ Read/Write ‘** switch in the ’ **Write** ’ position to write data on to the memory.
6. Set the data bits to 0h (clearing the content)
7. Observe that the LEDs (D3 to D0) glow. This is to indicate that the content is 0h. Refer the truth table above and observe that the data outputs of the RAM will be compliments of the data inputs.
8. Position the ‘ **Increment/Decrement** ‘ switch in the **‘Increment’** position.
9. Press the ‘**Clock**’ to increment the counter to the next address. As the ‘Read /Write ‘ switch is already in the ‘Write’ position, and the data bits are set to the 0h, the content in the new location is also replaced with 0h.
10. Repeat step 8 until the data in all the memory locations have been cleared.

Write Operation: -

1. Assume that the following data has to be written on to the RAM. The address and data are given in the hexadecimal format.

Address	Data
0h - 0000	Ah - 1010
1h - 0001	Bh - 1011
2h - 0010	4h - 0100
3h - 0011	7h - 0111
4h - 0100	Ch - 1100
5h - 0101	1h - 0001
6h - 0110	Fh - 1111
7h - 0111	5h - 0101
8h - 1000	8h - 1000
9h - 1001	3h - 0011
10h - 1010	Eh - 1110
11h - 1011	9h - 1001
12h - 1100	Dh - 1101
13h - 1101	0h - 0000
14h - 1110	2h - 0010
15h - 1111	6h - 0110

2. Position the ‘Stack/Queue’ switch in the **‘ Queue’**position.

3. Position the **’ Read/Write ‘** switch in the ’ **Write** ’ position to enable the entry of data in to the RAM.

4. Position the ‘**Set Address’** switch in the ‘**1**’ position to allow random access of memory.

5. Set the desired address (any address at random) using the address bit switches.

6. Set the desired data (refer table for the data to be entered in each location) using the data bit switches.

7. Observe that the data is indicated by the LEDs (D3 toD0). This is because the data is written on to the RAM.

8. Also observe that the data is indicated by the data outputs is the compliment of the data input (refer truth table condition ME =L and WE=L) .

9. After each data entry, make a note of the location where data is entered. This is to make sure that we are not re –entering data in the same location.

10. Repeat steps 4 and 5 until data has been entered in all the addresses listed in the above table

11. Position the **’ Read/Write ‘** switch in the ’ **Read**’ position, to disable data entry.

12. This completes data entry.

Read Operation: -

1. Position the ‘Stack/Queue’ switch in the ‘**Queue’** position.
2. Position the ‘**Set Address’** switch in the ‘0’ position to allow random access of memory.
3. Position **Read/Write ‘** switch in the **’ Read’** position, to disable unauthorized entry of data.
4. Set the desired address (any address at random).
5. Observe that the data entered in the location is indicated by the LEDs (D3 toD0). This is because the data was written during the data entry procedure.
6. Also observe that the data indicated by the data out puts is the compliment of the data input (refer truth table condition ME=L and WE=H).

Result: - Operation of the RAM Ic7489 has been verified.

Questions: -

1. What is the RAM? .
2. Give the applications of the RAM? .
3. What is the difference between RAM &ROM? .
4. What is the difference between static RAM &dynamic RAM?
5. Which can be used as 1-bit memory?
6. What are the different types of the ROM? .
7. What are the parameters of the RAM?
8. What is refreshing of memory? And where it is required?
9. What are sequential access memories?
10. What are charge-coupled devices?

UNIVERSAL SHIFT REGISTER

Aim :- To study the following applications of the Universal shift register using IC 74194.

a . Shift Right Logic

b . Shift Left Logic

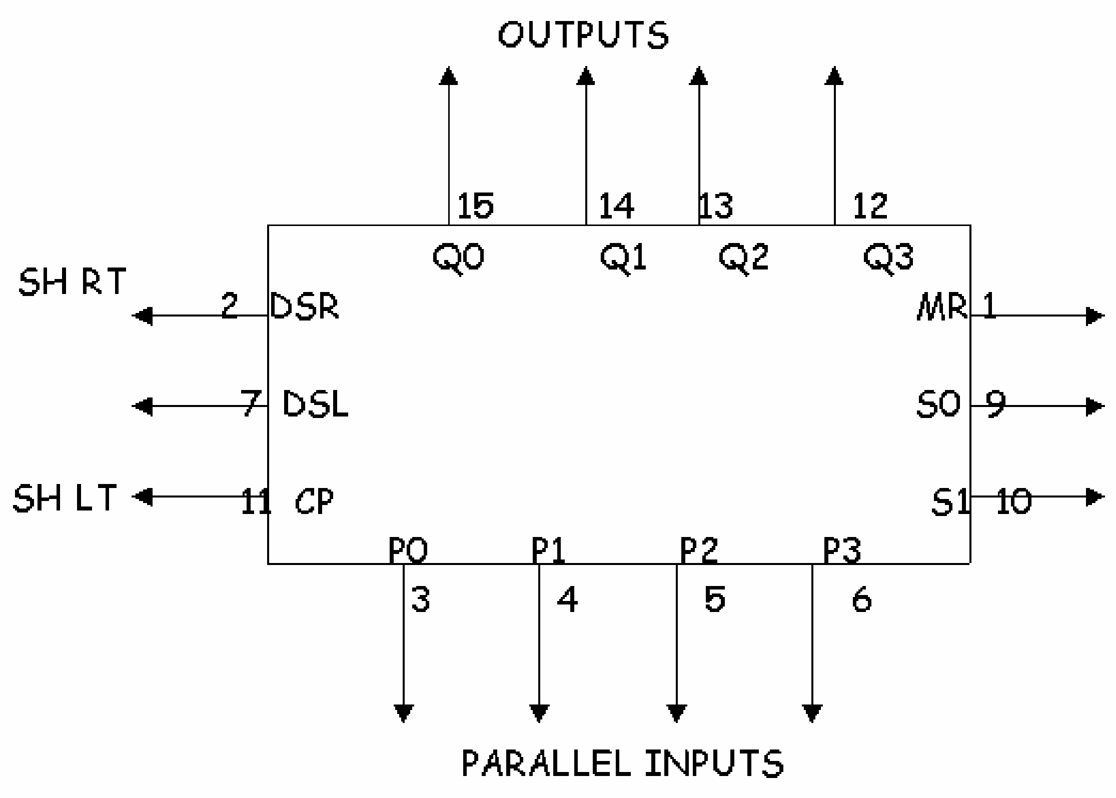
c . Parallel Load

Apparatus :-

1. **Universal Shift Register using IC 74194 Trainer boards.**

2. 5v fixed DC power supply.

Circuit Diagram:-



Procedure:-

STEP : 1. MASTER RESET

Set the inputs as below and observe the out puts as per table 1

MR	S1	S0	DSR	DSL	CP	P0	P1	P2	P3	Q0	Q1	Q2	Q3
0	X	X	X	X	X	X	X	X	X	0	0	0	0

Truth table –1

A logic ‘ 0 ‘ on MR resets all outputs to logic ‘ 0 ‘ irrespective of other inputs.

STEP :2 PARALLEL LOAD

In this step we load the data parallel. Set the inputs as below and observe the outputs.

MR	S1	S0	DSR	DSL	CP	P0	P1	P2	P3	Q0	Q1	Q2	Q3
1	1	1	x	x	CLK	1	1	1	1	1	1	1	1

Truth Table –2

Here when S1 & S0 are both logic ‘ 1 ‘ the input data is transferred parallely to output at the clock positive transition change the input data and observe the change at the output .

STEP : 3 . SHIFT LEFT LOGIC ‘ 0 ‘.

Set Q0 , Q1 , Q2 , Q3 to ‘ 1 1 1 1 ‘ by putting DSL to Logic ‘ 1 ‘ .

While running the above step, change the logic input DSL to logic ‘ 0 ‘

And S_0 to logic ‘ 0 ‘ in the same sequence .Observe the following outputs after each clock pulse and verify .

CONDITION	n CLOCK PULSES	**Q0**	**Q1**	**Q2**	**Q3**
MR = 1	0	1	1	1	1
S0 = 0	1	1	1	1	0
S1 = 1	2	1	1	0	0
DSL = 0	3	1	0	0	0
DSR = X	4	0	0	0	0

Truth Table – 3

In the sequence 4 clock pulses logic ‘ o ‘ s are shifted left successively with each clock pulse .

STEP : 4 . SHIFT LEFT LOGIC ‘ 1 ‘ S

Set the Q0 Q1 Q2 Q3 to 0 0 0 0 by setting DSL input to logic ‘ 0 ’.

Now switch DSL input to logic ‘ 1 ‘ and observe the shifting of logic ‘ 1 ‘ s to left as below . Observe the following outputs after each clock pulse and verify.

CONDITION	n CLOCK PULSES	**Q0**	**Q1**	**Q2**	**Q3**
MR = 1	0	0	0	0	0
S0 = 0	1	0	0	0	1
S1 = 1	2	0	0	1	1
DSL = 1	3	0	1	1	1
DSR = X	4	1	1	1	1

Truth Table – 4

STEP : 5 . SHIFT RIGHT LOGIC ‘ 0 ‘

Set the Q0 Q1 Q2 Q3 to 1 1 1 1 by setting DSR input to logic ‘ 1 ‘ .

Repeat step 4 and parallel load logic ‘ 1 ‘ s in all the 4 outputs .

Change the logic inputs of DSR to logic 0 and then of S1 to logic ‘ 0 ‘

in the same sequence . Observe the following outpus after each clock pulse and verify .

CONDITION	n CLOCK PULSES	**Q0**	**Q1**	**Q2**	**Q3**
MR = 1	0	1	1	1	1
S0 = 1	1	0	1	1	1
S1 = 0	2	0	0	1	1
DSL = X	3	0	0	0	1
DSR = 0	4	0	0	0	0

Truth Table –5

STEP : 6 SHIFT RIGHT LOGIC ‘1 ‘ s

Now at this condition of all ‘ 0 ‘ at the outputs switch DSR to logic ‘1’ this will enable all logic as serial data and logic ‘ 1 ‘ s will be shifted successively with each clock pulse as shown below .Observe the following table and verify the outputs .

CONDITION	n CLOCK PULSES	**Q0**	**Q1**	**Q2**	**Q3**
MR = 1	0	0	0	0	0
S0 = 1	1	1	0	0	0
S1 = 0	2	1	1	0	0
DSL = X	3	1	1	1	0
DSR = 1	4	1	1	1	1

STEP : 7 . In the above steps for shift left or shift right operation ,(step 3 4 5 6) if both the S0 &S1 switches are forced to logic ‘ 0 ‘, then shifting operation will cease and whatever is the output data it will freeze or hold . Observe this condition and verify .

CONDITION	n CLOCK PULSES	Q0 Q1 Q2 Q3
MR = 1	1	Previous data just before S0 &S1 both switched to logic ‘ 0 ‘.
S0 = 0	1	
S1 = 0	1	
DSL = 0	1	
DSR = 0	1	

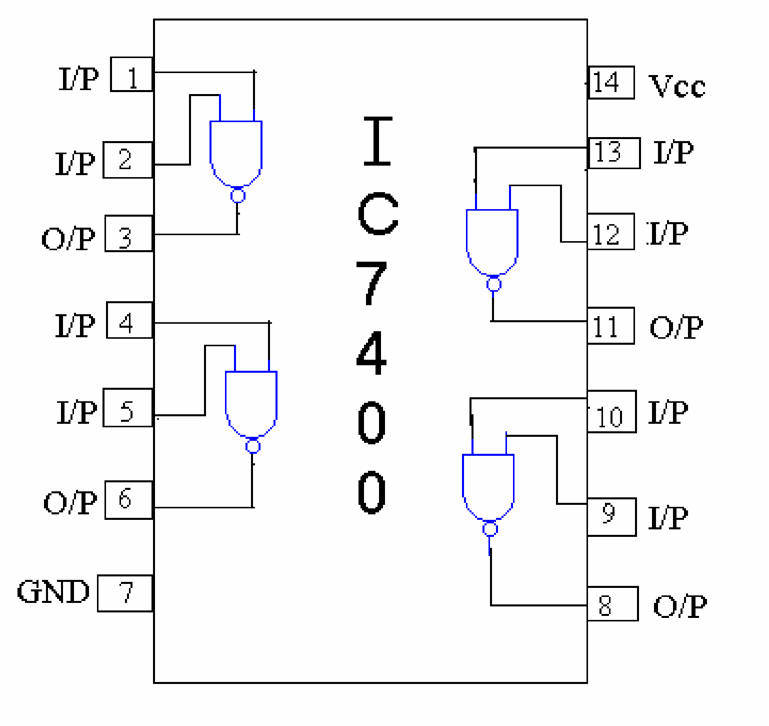
Truth Table –7

<u>Result</u>:- Verified the applications of the Universal shift register using IC 74194

Questions: -

11. What is the universal shift register?
12. In which circuits shifting and rotating circuits are used?
13. Which flip-flops are used in shift registers?
14. Which flip-flop is universal flip-flop?
15. What is the difference between shifting and rotating data?
16. What is register?
17. What is meant by parallel in &parallel out Shift register?
18. State various applications of Shift register?
19. List the basic types of shift register in terms of data movement?
20. Determine the output status of a 4-bit SIPO shift register, after 3 clock pulses if the I/P terminal is held high?

PIN CONFIGARATION OF DIGITAL IC'S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O/P 3
I/P 4
I/P 5
O/P 6
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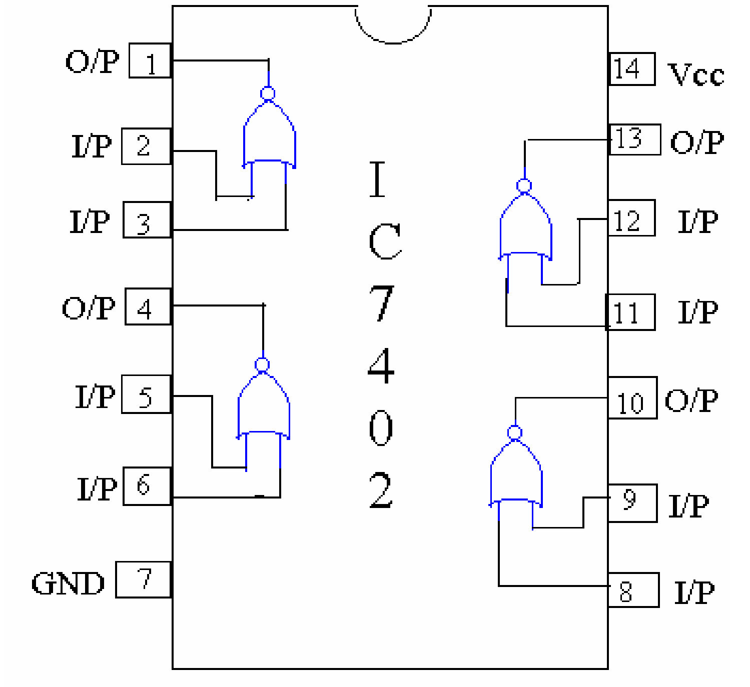
14 Vcc
13 I/P
12 I/P
11 O/P
10 I/P
9 I/P
8 O/P
IC7400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I/P 2
I/P 3
O/P 4
I/P 5
I/P 6
GND 7
14 Vcc
13 O/P
12 I/P
11 I/P
10 O/P
9 I/P
8 I/P
IC7402