CHIRANJEEVI REDDY INSTITUTE OF ENGINEERING & TECHNOLOGY

(Approved by AICTE,New Delhi & Affiliated to JNTU,ANANTAPUR)
Susheela Nagar, Bellary Road, ANANTAPUR.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING.

LINEAR & DIGITAL IC APPLICATIONS LAB (9A04505)

(III B.Tech I Semester)

LAB-MANUAL

Head of the Department

S.Raghavendra Swami
M-Tech.,
Assistant professor in ECE.

TILTLE OF LAB: LDICA LAB

LIST OF EXPERIMENTS (As per syllabus)

S. No.	Name of the Experiment
	LICA
1	ACTIVE FILTER APPLICATIONS-LPF AND HPF
2	FUNCTION GENERATOR USING 741 OP-AMP
3	VOLTAGE REGULATOR USING IC 723
4	ASTABLE AND MONOSTABLE MULTIVIBRATOR USING 555 TIMER
5	4 BIT DIGITALTO ANALOG CONVERTER
6	OP-AMP APPLICATION- ADDERS,SUBTRACTOR AND COMPARATOR
	DICA
7	LOGIC GATES
8	HALF ADDER AND HALF SUBTRACTOR
9	FULL ADDER AND FULL SUBTRACTOR
10	3X8 DECODER AND 8X3 ENCODER
11	8X1 MULTIPLEXER AND 1X4 DEMULTIPLEXER
12	4 BIT COMPARATOR-74X85
13	IC 74X74—POSITIVE EDGE TRIGGERED D FLIP FLOP
14	IC 74X109—JK FLIP FLOP
15	IC 74X90—DECADE COUNTER
16	IC 74X194—UNIVERSAL SHIFT REGISTER

Additional Experiments:

S. No.	Name of the Experiment
1	BARREL SHIFTER
2	16X1 MULTIPLEXER

Design Based Experiments:

S. No.	Name of the Experiment
	LICA
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18	BARREL SHIFTER
19	16X1 MULTIPLEXER

FACULTY IN-CHARGE

HEAD OF THE DEPARTMENT

1.ACTIVE FILTER APLLICATIONS-LPF,HPF [FIRST ORDER]

AIM:-

To study and design first order LPF and HPF using op-amp IC741 and to obtain frequency response.

.

EQUIPMENTS AND COMPONENTS:-

S.NO	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	OPAMP	741	-	1
2	RESISTOR	-	15KOhm	1
3	RESISTOR	-	10KOhm	3
4	CAPACITOR	-	0.01uf	1
5	SEMICNDUCTOR TRAINER KIT	-	-	1
6	FUNCTION GENERATOR	-	(0-3)MHz	1
7	CATHODE RAY OSCILLOSCOPE	-	(0-20)MHz	1

THEORY:

LOW PASS FILTER:

A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signals of frequencies outside the brand is called an electric filter. The first order low pass filter consists of a single RC network connected to the non-inverting input terminal of the operational amplifier. Resisters R1 and RF determine the gain of the filter in the pass band. The low pass filter as maximum gain at f = 0Hz. The frequency range from 0 to FH is called the pass band the frequency range f > fh is called the stop band.

The first order low pass butter worth filter uses an Rc network for filtering. Theop-amp is used in the non inverting configuration, hence it does not load down the RCnetwork. Resistor R1 and R2 determine the gain of the filter.

V0/Vin = Af /(1+ jf/f h)

Af = 1+ Rf /R1=passband gainof filter

F=frequency of the input signal

Fh=1/2ΠRC =High cutt off frequency of filter

V0/Vin=Gain of the filter as a function of frequency

The gain magnitude and phase angle equations of the LPF the can be obtained by converting V0/Vin into its equivalent polar form as follows|V0/Vin| = Af /(√1 +(f/f l2) Φ =-tan-1(f/f h)

Where Φ is the phase angle in degrees. The operation of the LPF can be verified

From the gain magnitude equation.

HIGH PASS FILTER:

High pass filters are often formed simply by interchanging frequency.Determining resistors and capacitors in LPFs that is ,a first order HPF is formed from afirst order LPF by interchanging components 'R' and 'C' figure. Shows a first order butter worth HPF with a lower cut off frequency of ' Fl'. This is the frequency at whichmagnitude of the gain is 0.707 times its pass band value. Obviously all frequencies, withthe highest frequency determinate by the closed loop band width of op-amp.For the first order HPF the output voltage is

V0= [1+Rf /R1]j2ΠRCVin/(1-j2ΠfRC)

V0/Vin=Af [j(f/f l)/(1=j(f/f l)]

WhereAf +Rf /R1pass band gain of the filter.

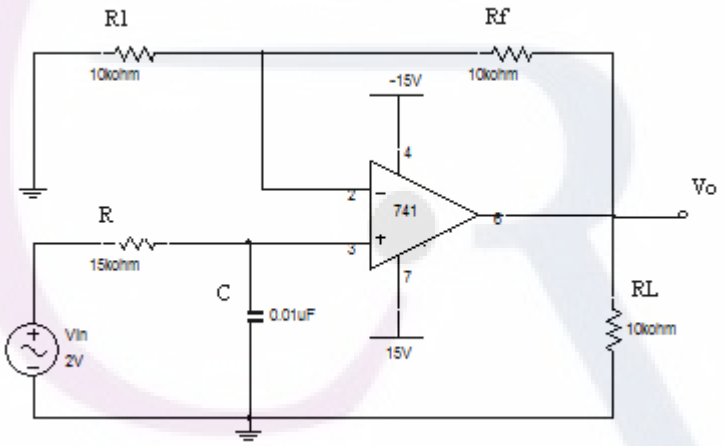
F =frequency of input signal.

Fl=1/2ΠRC = lower cutt off frequency

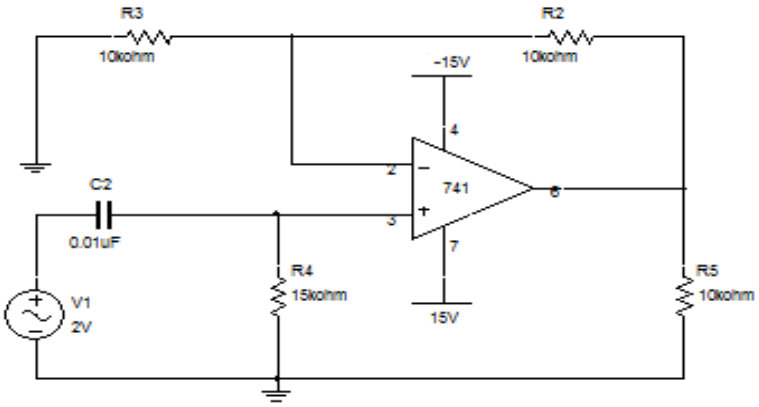
Since, HPFs are formed from LPFs simply by interchanging R's and C's .Thedesign and frequency scaling procedures of the LPFsare also applicable to HPFs.

CIRCUIT DIAGRAM:

LPF:



HPF:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Apply sine wave of amplitude 2Vp-p to the non inverting input terminal.
3. Values the input signal frequency.
4. Note down the corresponding output voltage.
5. Calculate gain in db.
6. Tabulate the values.
7. Plot a graph between frequency and gain.
8. Identify stop band and pass band from the graph.

.

OBSERVATIONS :(LPF)

S.NO	Input frequency	Output voltage	Gain in db 20 log Vo/Vi
1. 2 3 4. 5. 6. 7.			

OBSERVATIONS :(HPF)

S.NO	Input frequency	Output voltage	Gain in db 20 log Vo/Vi
1. 2 3 4. 5. 6. 7.			

CALCULATIONS-

LPF:

$F_h=1/2\pi RC$

$Fh=1/2\pi x15kx0.01\mu f$

$= 1k$

Choose $c=0.01\mu f$

$Av=1+Rf/R1$

With this
R1=10k

Rf=10k

HPF:

Choose a standard value of Capacitor C say 0.01 μF
Then $f_L=1/2\pi Rc$

$1/2\pi x15kx0.01\mu f$
$= 1k$

$F_L=1k$

$A=1+Rf/R1$

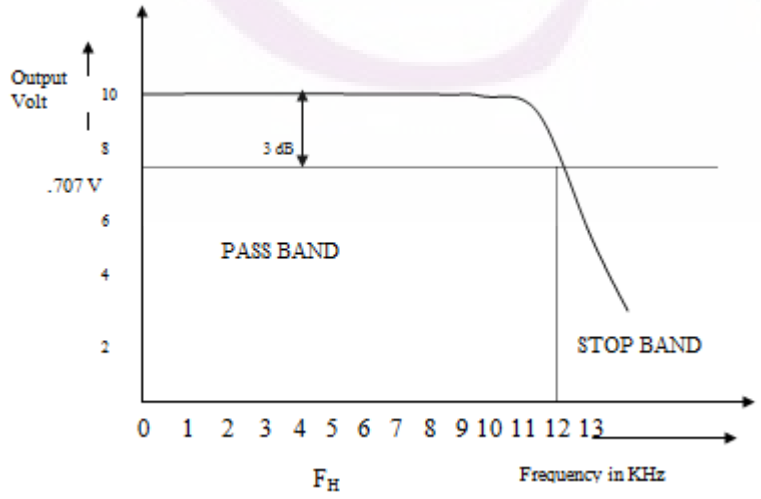
With this

R1=10k

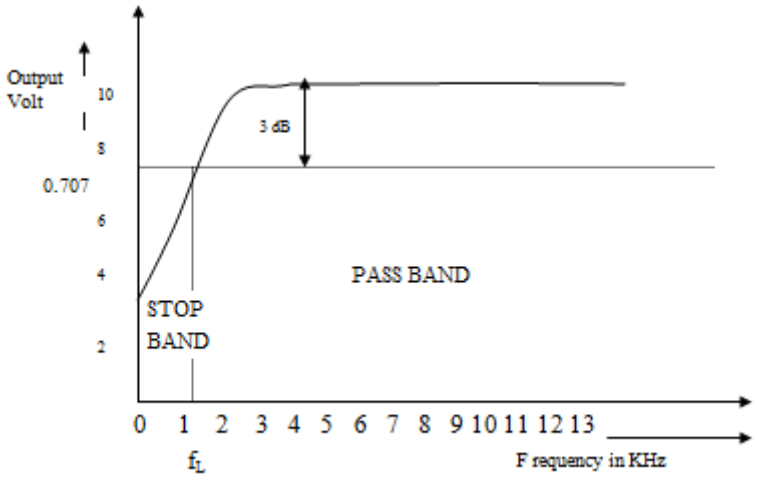
Rf=10k

MODEL GRAPH:

LPF:



HPF:



RESULT:-

HPF : The obtained gain A_v =_____
The band width =_____

LPF: The obtained gain A_v =_____
The band width =_____

The HPF and LPF filters are designed and obtained gain is found to be equal to the theoretical value of gain .The frequency response of LPF and HPF is plotted using IC741 Op-Amp

REVIEW QUESTIONS

1. Classify filters?
2. Discuss the disadvantages of passive filters?
3. Why are active filters preferred?
4. List the commonly used filters?

2.FUNCTION GENERATOR USING 741 OP-AMP

AIM: To generate triangular and square wave forms and to determine the time period and frequency of the waveforms.

EQUIPMENTS AND COMPONENTS:

S.NO	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	OPAMP	741	-	2
2	RESISTOR	-	15KOhm	1
3	RESISTOR	-	10KOhm	1
4	RESISTOR	-	1KOhm	1
5	CAPACITOR	-	0.1uf	1
6	SEMICNDUCTOR TRAINER KIT	-	-	1
7	CATHODE RAY OSCILLOSCOPE	-	(0-20)MHz	1

THEORY:

Function generator is a signal generator that produces various specific waveforms for test purposes over a wide range of frequencies. In laboratory type function generator generally one of the functions (sine, triangle, etc.) is generated using dedicated chips or standard circuits and converts it in to required signal.

Integrator (square to triangle converter):

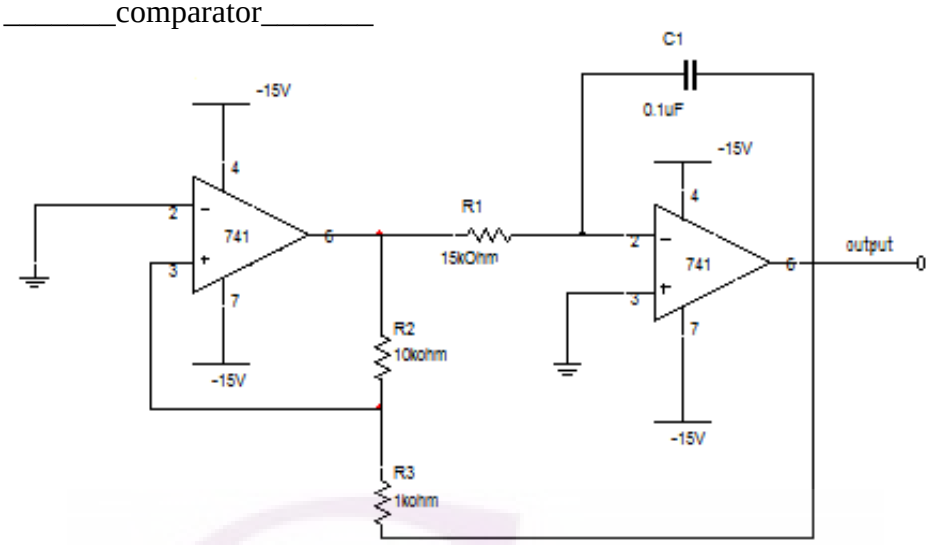
Figure shows integrator-using op-amp. Square wave from the zero crossing detector is fed to the integrator using op-amp. RC time constant of the integrator has been chosen in such a way it is a small value compared to time period of the incoming square wave. As you knew the operation of integrator, the output of the integrator is a triangle wave we feed square wave input.

The triangular wave output of the second op amp is then fed into the third op amp, which is also configured as an integrator. The output of the third op amp is a sine wave (the integral of a triangular wave).

CIRCUIT DIAGRAM:

_____ integrator_____

_____comparator_____



PROCEDURE:

1. The circuit is connected as shown in the figure.
2. The output of the comparator is connected to the CRO through chennal1, to generate a square wave.
3. The output of the comparator is applied to integrator and is connected to the CRO through chennal2, to generate a triangular wave.
4. The time periods of the square wave and triangular waves are noted and they are found to be equal.

THEORITICAL CALCULATIONS:

$T=4R_1R_2C_1/R_3$

$T=4x15Kx10Kx0.1\mu f$

$T=0.6ms$

$f = R_3/4R_1R_2C_1$

(OR) 1/T

= 1.6 KHz

$Vsat=Vcc-2v$

$=15-2v$

13V

$+Vramp=R2/R3Vsat$

$=10k/1kx13v$

$=1.3v$

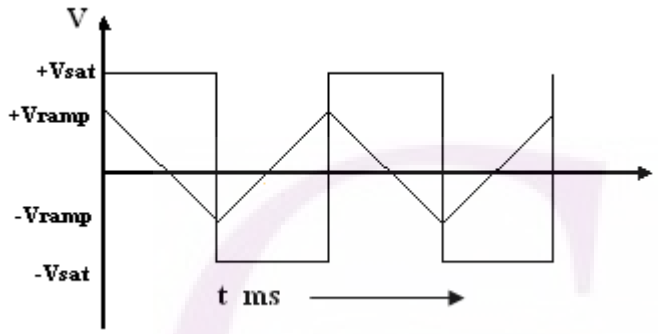
-Vramp= - R2/R3Vsat

=-1.3v

Theoretical VALUES:

Frequency of triangular wave =1.6KHZ
Positive peak ramp =1.2v

GRAPH:-



RESULT:

The obtained value Time period of triangular wave = _____ms
Frequency of triangular wave = _____Hz
Positive peak ramp Vramp =_____V
Voltage of square wave = _____V

The theoretical and practical values of time periods are found to be equal and graphs are drawn.

REVIEW QUESTIONS:

1. Define integrator?
2. Write about triangular wave generator?
3. Derive equation for output frequency of triangular wave?
4. Define function generator?
5. Write some applications of function generator?
6. What is the function of function generator?
7. Draw the block diagram of function generator?

3.VOLTAGE REGULATOR USING IC723

AIM:-

To study the operation of IC723 voltage regulator

EQUIPMENTS AND COMPONENTS:-

S.NO	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	REGULATOR	LM723	-	1
2	RESISTOR	-	7.5KOhm	2
3	RESISTOR	-	3.9KOhm	1
4	CAPACITOR	-	100pf	1
5	VARIABLE RESISTOR	-	(0-10)KOhm	1
6	SEMICNDUCTOR TRAINER KIT	-	-	1

THEORY:-

The three-terminal regulators have the following limitations

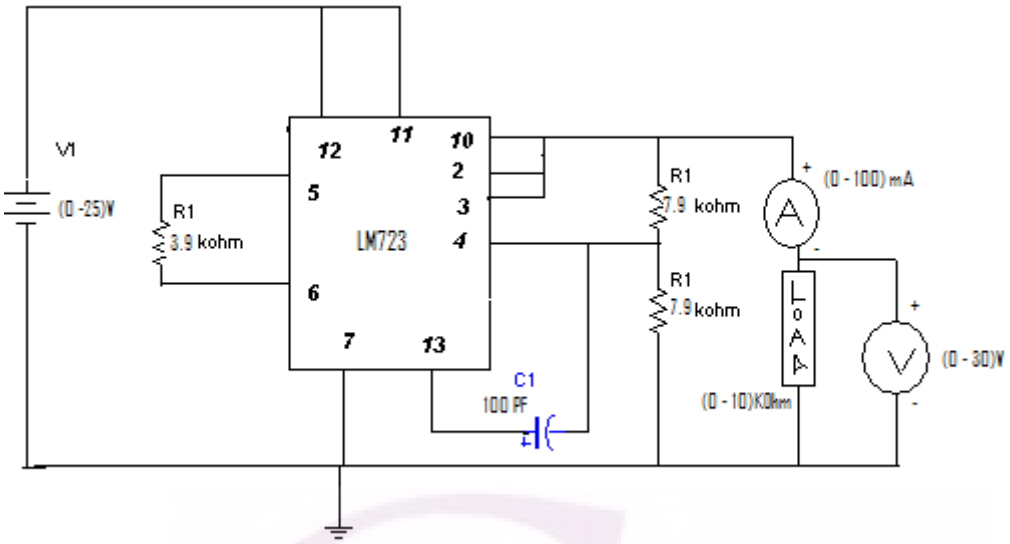
1. No short-circuit protection
2. Output voltage (+ve or –ve) is fixed

These limitations have been overcome in 723 general purpose regulator. This IC is inherently low current device but can be boosted to provide 5 amps or more currentby connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short-circuit current limits. The IC723 has two sections. The first section consists of Zener Diode constant current source and a reference amplifier. The other section of the IC consists of an error amplifier series pass transistor and a current limit transistor. This is a 14-pin DIP package. The main Features of 723 include an input voltage of 40v max, output voltage is adjustable from 2V to 37V, 150 mA output current without external pass resistor, can be used as either a linear or a switching regulator.

A voltage regulator is a circuit that supplies constant voltage regardless of changes in load currents. Except for the switching regulators, all other types of regulators are called linear regulators. IC LM 723 is general purpose regulator. The input voltage of this 723 IC is 40 V maximum. Output voltage adjustable from 2V to 30V. 150mA output current external pass transistor. Ou put current in excess of 10Ampere possible by adding external transistors. It can be used as either a linear or a switching regulator. The variation of DC output voltage as a function of DC load current is called regulation.

% Regulation =[(Vnl - Vfl) / Vfl]*100

CIRCUIT DIAGRAM



PROCEDURE:

1. LINE REGULATION:

1. Connections are made as per the circuit diagram.
2. Power supply is connected to 12 and 7 terminals.
3. Volt meter is connected to 10 and 7 terminals.
4. By increasing the input voltage corresponding volt meter reading is noted.

2. LOAD REGULATION:

1. Connect the load to the terminals 10 and GND.
2. Keep the input voltage constant at which line regulation is obtained
3. The maximum load value is calculated from IC ratings.
4. Now, we decrease the load resistance and note down the corresponding value of the output in volt meter.
5. Plot the graph for load verses load regulation.

. **OBSERVATIONS:**

(1).LINE REGULATION:

V_{nl}=17.2V

%REGULATION = $[(V_{nl}-V_{fl})/V_{fl}]*100$

$=[(17.2-14.6)/14.6]*100$

$=17.8$

To find Vo $=Vref(1+R_1/R_1)$

Vo=14v

Line Voltage(V)	Output Voltage(V)

(2). LOAD REGULATION:

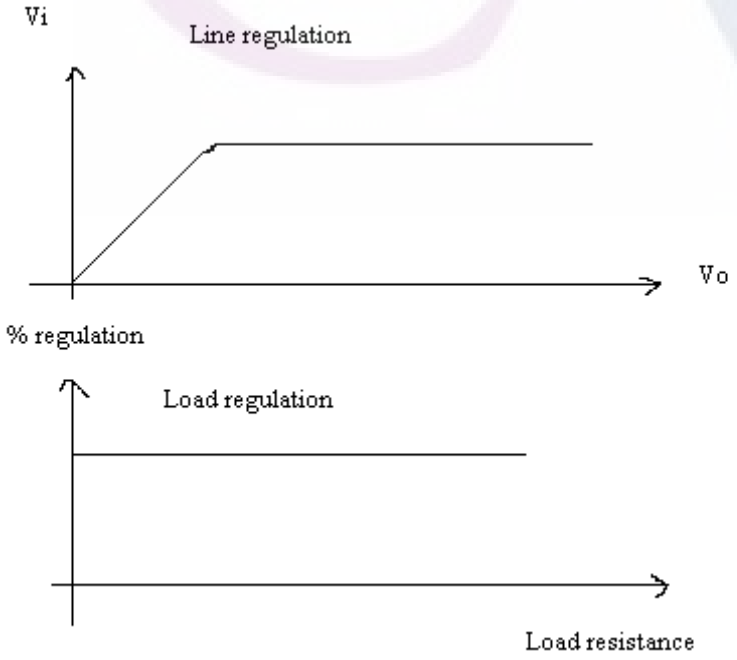
Regulated Output(V)	Load Current(mA)	Load Resistance(KΩ)	Load Regulation

%REGULATION = $[(V_{nl}-V_{fl})/V_{fl}]*100$

$=[(17.2-14.6)/14.6]*100$

$=17.8$

GRAPH:



RESULT:

The obtained value of output voltage Vo =_____

%Regulation is =_____

The regulation characteristics of the given IC LM 723 are successfully plotted.

REVIEW QUESTIONS:

1. What is the maximum input voltage that we can give to 723 regulator?
2. What output voltage range we can obtain from 723 regulator?
3. What is the output current in case of 723 regulator?
4. What are the applications of 723 regulator?
5. Define line regulation?
6. Define load regulation?
7. Define ripple rejection?
8. Define long term stability?
9. What is the current limit protection?
10. What are the ideal values of load and line regulations?

4. IC 555 TIMER- ASTABLEOPERATION CIRCUIT

AIM:-

To construct and study the operation of astable multivibrator using 555 timer.

EQUIPMENTS AND COMPONENTS:-

S.NO	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	TIMER	555	-	1
2	RESISTOR	-	1.2KOhm	1
3	RESISTOR	-	1.7KOhm	1
4	CAPACITOR	-	0.1uf	1
5	CAPACITOR	-	0.01uf	1
6	SEMICNDUCTOR TRAINER KIT	-	-	1
7	CATHODE RAY OSCILLOSCOPE	-	(0-20)MHz	1

THEORY:

The 555 timer can be used with supply voltage in the range of + 5 v to + 18 v and can drive upto 200 mAmps. It is compatible with both TTL and CMOS logic circuits because of the wide range of supply voltage the 555 timer is versatile and easy to use in the astable multivibrator. The timer is oscillated between two threshold levels 1/3 Vcc and 2/3 Vcc in order to generate a square wave form. No external signal source is required for such generation and hence this is called as a free running multivibrator.

MONOSTABLE MULTIVIBRATOR:

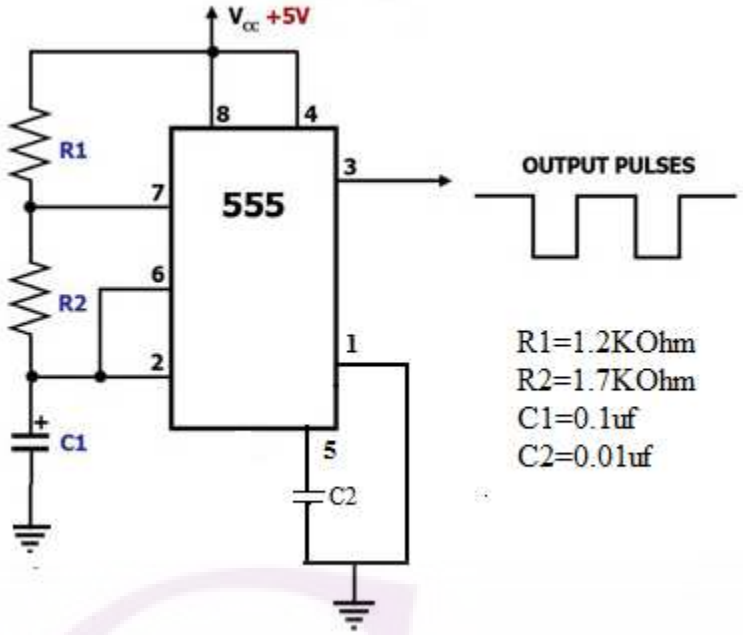
Monostable multivibrator is also known as triangular wave generator. It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V. then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal. Let us assume that the circuit is instable state. The output V0i is at +Vsat. Thediode D1 conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V.the voltage at the positive input terminal through R1R2 potentiometer divider is +ßVsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V.the output of the Op-Amp will switch from +Vsat to –Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vsat. When the capacitor charge Vc becomes slightly more negative than –ßVsat, the output of the op-amp switches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

$$V0 = Vf + (Vi - Vf)\, e^{-t/RC}$$

$$ß = R2/(R1+R2)$$

If Vsat>> Vp and R1=R2 and ß = 0.5,Then, T = 0.69RC

CIRCUIT DIAGRAM:-



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Pins 4 and 8 are shorted and connected to power supply Vcc (+5V)
3. Between pins 8 and 7 resistor R1 of 10KΩ is connected and between 7 and 6 resistor R2 of 4.7K Ω is connected. Pins 2 and 6 short circuited.
4. In between pins 1 and 5 a Capacitor of 0.01µF is connected.
5. The output is connected across the pin 3 and GND.
6. In between pins 6 and GND a Capacitor of 0.1µF is connected.
7. Theoretically without diode charging time Tc is given byTc=0.69(R1+R2) C1, Discharging time Td is given by Td= 0.69R2C1The frequency f is given by f= 1.45/(R1+2R2)C1% of Duty cycle is (Tc/(Tc+Td))*100
8. Practically Td and Tc are measured and wave forms are noted and theoreticalValues are verified with practical values
9. Connect diode between pins 7 and 2.
10. Theoretically with diode connected charging time is given by Tc=0.69R1C1Discharging time is given by Td=0.69R2C1.
11. Practically Td and Tc are noted and verified with theoretical values.

OBSERVATIONS:-

1. $t_{ON} = 0.69 (R_1 + R_2) C$

$=0.69(1.2k+1.7k)0.01\mu f$

$t_{ON} = 0.2ms$

2.$t_{OFF} = 0.69 R_2C$

=0.69x1.7k0.01µf

t_{OFF} =0.17ms

T= t_{ON+} t_{OFF}

=0.37ms

% Dutycycle = $t_{on/}$ $t_{on+}t_{off}$ x100

=37%

. Design of astable multivibrator to produce 1 KHz output waveform with adjustable duty cycle of 10% to 90%

The circuit is as shown in Fig. 2

During the charging period, the diode 'D' is forward biased, RB is bypassed

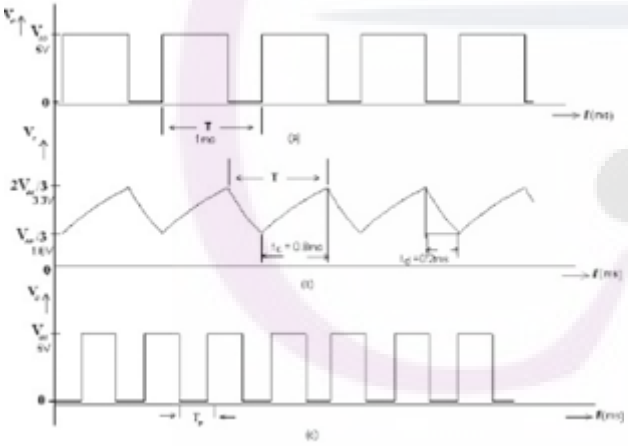
Hence ton = 0.69 R_1C.

During the discharge period, the discharging transistor is shorted (ON) and the diode 'D' is reverse biased.

Hence t_{OFF} = 0.69R_2 C

Output frequency f= 1 KHz is assumed.

MODELGRAPH:



RESULT:

The obtained value of duty cycle =_____%

Output waveforms of astable multivibrator is observed and the duty cycle is calculated the practical value is found to be equal to the theoretical value.

REVIEW QUESTIONS:

1Explain the functional block diagram of a 555 timer

2. Explain the function of reset

3. What are the modes of operation of timer?

4. What is the expression of time delay of a astable multivibrator?

5. Discuss some applications of timer in astable mode?

555 TIMER-MONOSTABLE MULTI-VIBRATOR

AIM: To construct and study the operation of a monostable multivibrator using 555 ICtimer.

EQUIPMENTS AND COMPONENTS:

S.NO	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	TIMER	555	-	1
2	RESISTOR	-	10KOhm	1
3	CAPACITOR	-	0.1uf	1
4	CAPACITOR	-	0.01uf	1
5	SEMICNDUCTOR TRAINER KIT	-	-	1
6	CATHODE RAY OSCILLOSCOPE	-	(0-20)MHz	1
7	FUNCTION GENERATOR	-	(0-3)MHz	1

THEORY:-

The 555 timer can be used with supply voltage in the range of +5 v to +18 v and can drive upto 200 mAmps. It is compatible with both TTL and CMOS logic circuits because of the wide range of supply voltage the 555 timer is versatile and easy to use in monostable multivibrator we will provide external triggering in order to make the timer to switch over to high state (unstable). This is also called as one-short multivibrator.

MONOSTABLE MULTIVIBRATOR:

Monostable multivibrator is also known as triangular wave generator. It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V. then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal. Let us assume that the circuit is instable state. The output V0i is at +Vsat. The diode D1 conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V.the voltage at the positive input terminal through R1R2 potentiometer divider is +ßVsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V.the output of the Op-Amp will switch from +Vsat to –Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vsat. When the capacitor charge Vc becomes slightly more negative than –ßVsat, the output of the op-amp switches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

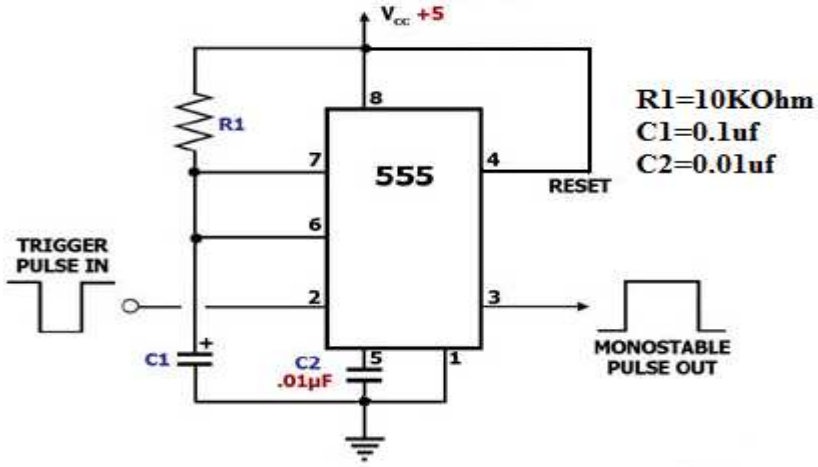
$$V0= Vf +(Vi-Vf) e^{-t/RC}$$

$$ß = R2/(R1+R2)$$

If $Vsat >> Vp$ and $R1=R2$

and $ß = 0.5$, Then, $T = 0.69RC$

CIRCUIT DIAGRAM:-



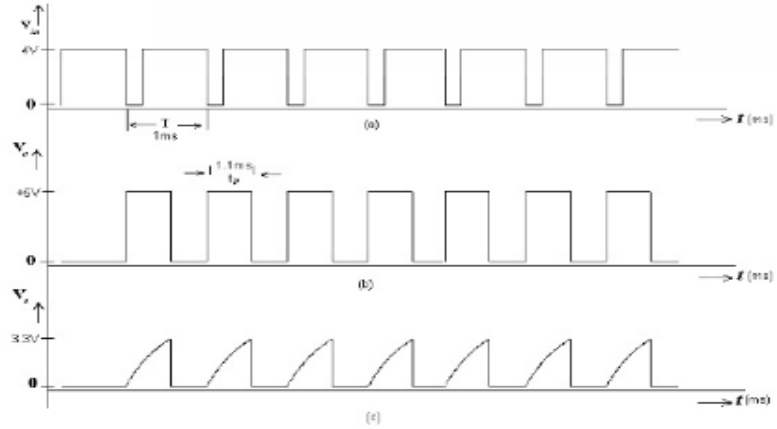
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Negative triggering is applied at the terminal 2.
3. The output voltage is measured by connecting the channel-1 at pin3.
4. The output voltage across capacitor is measured by connecting the channel-2 at the point
5. Theoretically the time period is calculated by $T= 1.1R_1C_1$ where $R_1= 10K\Omega$ $C_1=0.1\mu F$.
6. Practically the charging and discharging timers are measured and theoretical value of time period is measured with practical value

OBSERVATIONS:

1. $T_P = 1.1\ R_1C_1$
   $= 1.1x10kx0.1\mu f$
   $=1.1ms$

MODEL GRAPH:



(a): Trigger signal (b): Output Voltage (c): Capacitor Voltage

RESULT:

The obtained value of time constant =_____ms

The output Waveforms of monostable multivibrator are observed and time constant is calculated and the practical value found to be equal to the theoretical value.

REVIEW QUESTIONS:

1. Explain the functional block diagram of a 555 timer
2. Explain the function of reset
3. What are the modes of operation of timer?
4. What is the expression of time delay of a monostable multivibrator?
5. Discuss some applications of timer in monostable mode.
6. Define duty cycle
7. Give methods of obtaining symmetrical waveform.
8. How is an monostable multivibrator connected into a pulse position modulator
9. How Schmitt trigger circuit is constructed using 555 timer
10. Draw the pin diagram of 555 timer.

5. 4 BIT D/A CONVERTER

AIM:

To construct a 4-bit R – 2 R ladder type D/A converter. Plot the transfer characteristics, that is, binary input vs output voltage. Calculate the resolution and linearity of the converter from the graph.

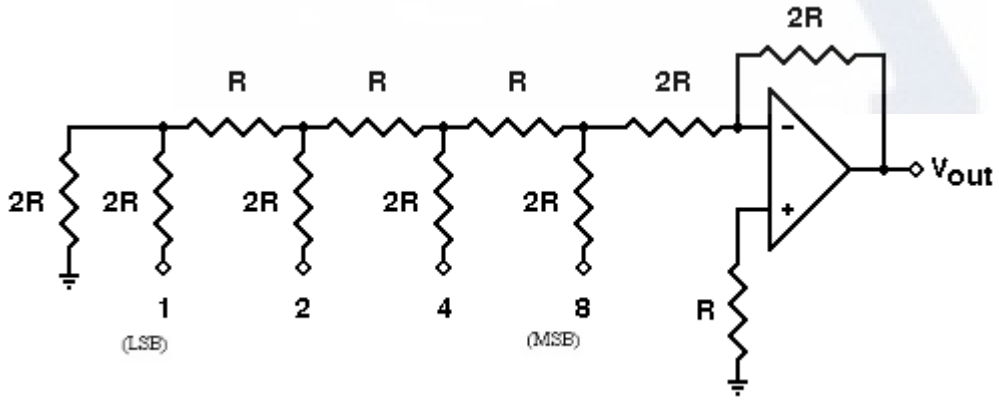
EQUIPMENTS AND COMPONENTS:

S.NO	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	OPAMP	741	-	1
2	RESISTOR	-	10KOhm	4
3	RESISTOR	-	22KOhm	6
5	SEMICNDUCTOR TRAINER KIT	-	-	1

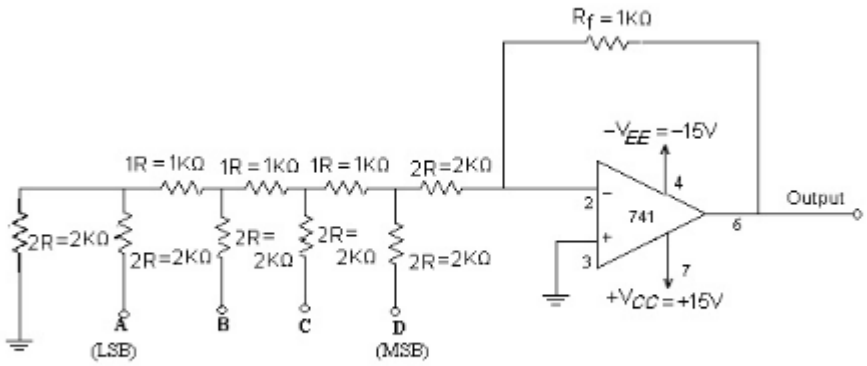
THEORY:

Most of the real world physical quantities such as voltage current temperature pressure are available in analog form. It is very difficult to process the signal in analog form, hence ADC and DAC are used. The DAC is to convert digital signal into analog and hence the functioning of DAC is exactly opposite to that of ADC. The DAC is usually operated at the same frequency as the ADC. The output of the DAC is commonly staircase. This staircase like digital output is passed through a smoothing filter to reduce the effect of quantization noise. There are three types of DAC techniques (i) Weighted resistor DAC (ii) R-2R ladder. (iii) Inverted R-2R ladder. Wide range of resistors is required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required it is well suited for integrated circuit realization.

CIRCUIT DIAGRAM:-



(OR)



R – 2R Ladder DAC

PROCEDURE:

1. Set up the circuit shown in Fig.
2. With all inputs (d0 to d3) shorted to ground, adjust the 20 kΩ pot until the output is 0V. This will nullify any offset voltage at the input of the op-amp.
3 .Measure the output voltage for all binary input states (0000 to 1111) and plot a Graph of binary inputs vs output voltage.
4. .Measure the size of each step and hence calculate resolution
5. Calculate linearity.

OBSERVATIONS:

D3	D2	D1	D0	R-2R LADDER DAC	
				THEORITICAL(V)	PRACTICAL(V)

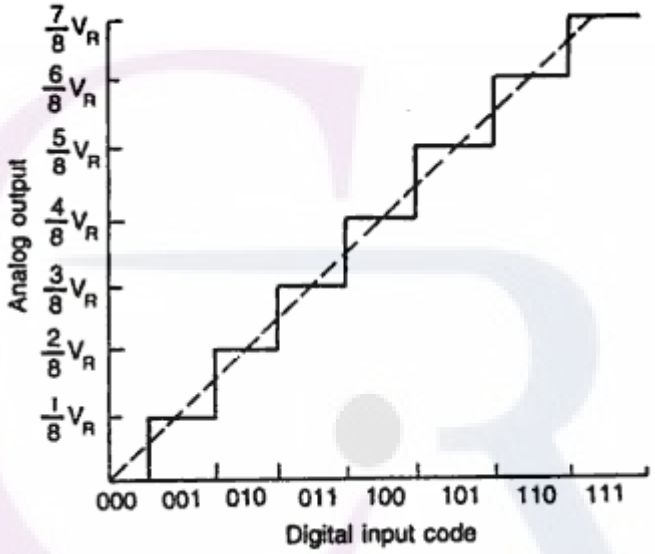
CALCULATIONS:

VO = Vref [D3/R3+D2/R2+D1/R1+D0/R0]

For data bit 0001
Vo=0.9v
And for 0010
Vo=1.87v

Resolution (in volts) = VFS / (2n –1) = 1 LSB increment.
=14/8-1=2

GRAPH:-



RESULT:-
The obtained output voltage of DAC =_____V

The 4 bit DAC is constructed Vo is calculated for different data bits and Vo is verified practically both values are found to be equal.

REVIEW QUESTIONS:
1. Classify DAC on the basis of their output?
2. Name the essential parts of a DAC?
3. What is meant by accuracy of DAC?
4. How many resistors are required in 12 bit weighted resistor DAC?
5. Why is an inverted R-2R ladder network DAC is better than R-2R ladder DAC.
6. Define resolution?
7. Define linearity?
8 .Define monotonicity?
9 . Define step size?
10. Define settling time?

6.OP-AMP APPLICATIONS

AIM: To study and verify the adder , subtractor and comparator applications using IC741 operational amplifier.

EQUIPMENTS AND COMPONENTS:

S.NO	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	OPAMP	741	-	1
2	RESISTOR	-	1KOhm	4
3	SEMICNDUCTOR TRAINER KIT	-	-	1

THEORY:

ADDER:

The Operational Amplifier is probably the most versatile Integrated Circuit available. It is very cheap especially keeping in mind the fact that it contains several hundred components. The most common Op-Amp is the 741 and it is used in many circuits.The OP AMP is a 'Linear Amplifier' with an amazing variety of uses. Its main purpose is to amplify (increase) a weak signal - a little like a Darlington Pair. The OP-AMP has two inputs, INVERTING (-) and NON-INVERTING (+), and one output at pin 6.Op-Amp may be used to design a circuit whose output is the sum of several inputsignals such as circuit is called a summing amplifier or summer. We can obtain either inverting or non inverting summer.The circuit diagrams shows a two input inverting summing amplifier. It has two input voltages V1and V2, two input resistors R1,R2and a feedback resistor Rf .Assuming that op-amp is in ideal conditions and input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp.And hence non inverting input terminal of op-amp is at ground potential and by taking nodal equations we have,

V1/R1+V2/R2+V0/Rf =0
V0= - [(R f /R1) V1+(Rf /R2) V2] And here
R1= R2= Rf =1KΩ
V0= -(V1+V2)Thus output is inverted and sum of input

SUBTRACTOR:

A basic differential amplifier can be used as a sub tractor. It has two inputsignals V1 and V2 and two input resistances R1 and R2 and a feedback resistor Rf . The input signals scaled to the desired values by selecting appropriate values for theexternal resistors.From the figure, the output voltage of the differential amplifier with a gain of '1' is
V0= -R1/Rf (V2-V1)
V0= V1-V2
Also R1=R2= Rf =1KΩ
Thus, the output voltage V0 is equal to the voltage V1applied to the non inverting terminal minus voltage V2 applied to inverting terminal.Hence the circuit is sub tractor.

COMPARATOR:

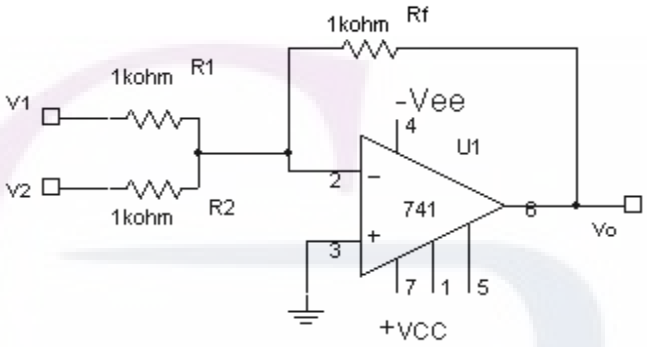
A comparator is a circuit which compares a signal voltage applied at one inputof an op-amp with a known reference voltage at the other input . It is basically an openloop op-amp with output ±Vsat as in the ideal transfer characteristics.It is clear that the change in the output state takes place with an increment in input Vi of only 2mv. This is the uncertainty region where output cannot be directly defined Thereare basically 2 types of comparators.

1. Non inverting comparator and.
2. Inverting comparator.

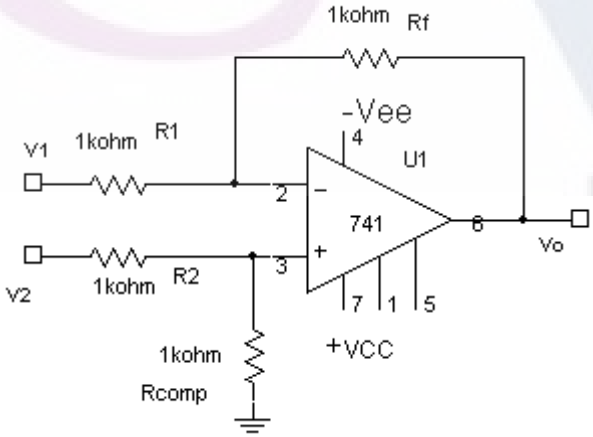
The applications of comparator are zero crossing detector, window detector, timemarker generator and phase meter.

CIRCUIT DIAGRAMS:

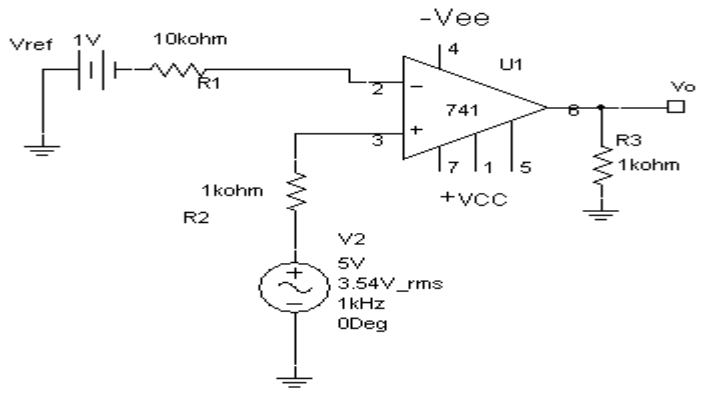
ADDER:



SUBTRACTOR:



COMPARATOR:



PROCEDURE:

COMPARATOR:

1. Connections are made as per the circuit diagram.
2. Select the sine wave of 5V peak to peak, 1K Hz frequency.
3. Apply the reference voltage 1V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to Vref.
5. Repeat steps 3 and 4 with reference voltages as 2V, 4V, -2V, -4V and observe thewaveforms.
6. Replace sine wave input with 5V dc voltage and Vref = 0V.
7. Observe dc voltage at output using CRO.
8. Slowly increase Vref voltage and observe the change in saturation voltage.
9. To make a zero crossing detector, set Vref = 0V and observe the output waveforms.

ADDER AND SUBTRACTOR

1. Connections are made as per the circuit diagram.
2. Apply input voltage 1) V1= 5v, V2=2v 2) V1= 5v,V2=5v
3. Using Millimeter measure the dc output voltage at the output terminal.
4. For different values of V1 and V2 measure the output voltage.

OBSERVATIONS:

ADDER:

V_1 (Volts)	V_2 (Volts)	Theoretical $Vo=-(V_1+V_2)$	Practical $Vo=-(V_1+V_2)$

$Vo=-(V_1+V_2)$
$=-(2+3)$
$=-5v$

SUBTRACTOR:

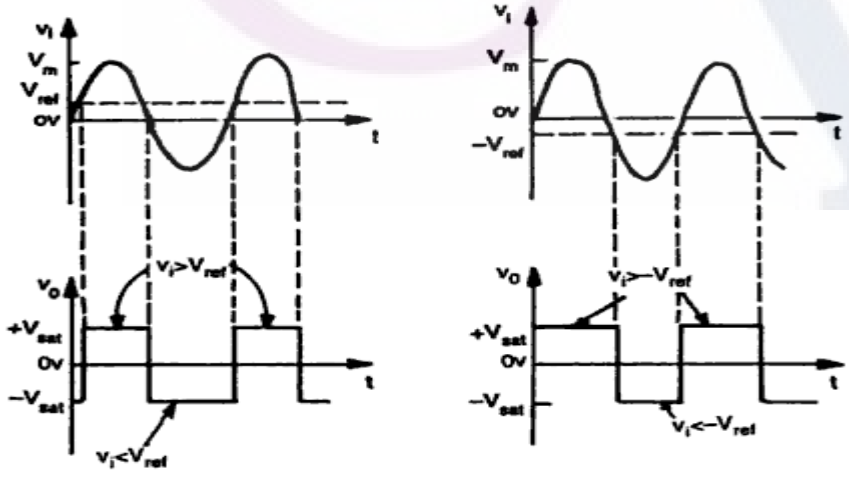
V_1 (Volts)	V_2 (Volts)	Theoretical $Vo=(V_1-V_2)$	Practical $Vo=(V_1-V_2)$

$Vo=(V_1-V_2)$
$=(4-2)$
$=2v$

COMPARATOR:

Voltage input	V_{ref}	Observed square wave amplitude

MODEL GRAPH:



RESULT:

ADDER: The obtained value of addition of two voltages =_____

SUBTRACTOR: The obtained value of subtraction of two voltages =_____

The operation of IC 741 Op-Amp as adder, subtractor and comparator is studied and the practical values found to be equal to the theoretical value.

REVIEW QUESTIONS:

1. What is an op-amp?
2. What are ideal characteristics of op amp?
3. What is the function of adder?
4. What is meant by comparator?
5. What is window detector?
6. What is zero crossing detector?

7. IC 566 –VCO APPLICATIONS

AIM: To operate the NE/SE 566 as Voltage Controlled Oscillator and to find the frequencies for various values of R_1 and C_1.

EQUIPMENTS AND COMPONENTS:

	NAME OF EQUIPMENT/COMPONENT	TYPE	RANGE	QUANTITY
1	C NE/SE 566		-	1
2	RESISTORs	-	(1KΩ, 5KΩ, 4KΩ, 6KΩ, 8KΩ)	Each one
3	SEMICNDUCTOR TRAINER KIT CRO	- -	- -	1 1

THEORY:

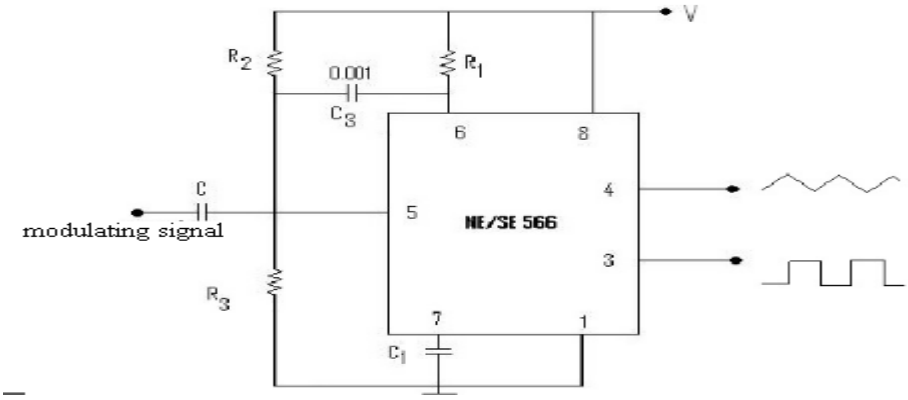
Voltage Controlled Oscillator is also called as voltage to frequency converter. It provides the simultaneous square wave and triangular wave output. The frequency of output wave is the function of input voltage, hence the name Voltage Controlled Oscillator. Output frequency is also the function of external resistor R_1 and capacitor C_1
The output frequency fo is given by,

$$fo=2(V-Vc)/R_1C_1V$$

Where $3/4V<=Vc<V$; $2K\Omega<R_1<20\ K\Omega$

The triangular wave is generated by alternately charging the external capacitor C_1 by one current source and then linearly discharging it by another. The charge discharge levels are determined by Schmitt trigger action. The external modulating signal is ac coupled with capacitor C at the pin 5. Now the output frequency is varied according to the amplitude of this applied modulating voltage. VCO is commonly used in converting low-frequency signals such as electroenphalograms (EEG) or electrocardiograms (ECG) into an audio frequency range signals, which can be transmitted over telephone lines or two way radio communications for diagnostic purposes.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Measure the output voltage and frequency of both triangular and squares.
3. Vary the values of R_1 and C_1 and measure the frequency of the waveforms.
4. Compare the measured values with the theoretical values.

OBSERVATIONS:

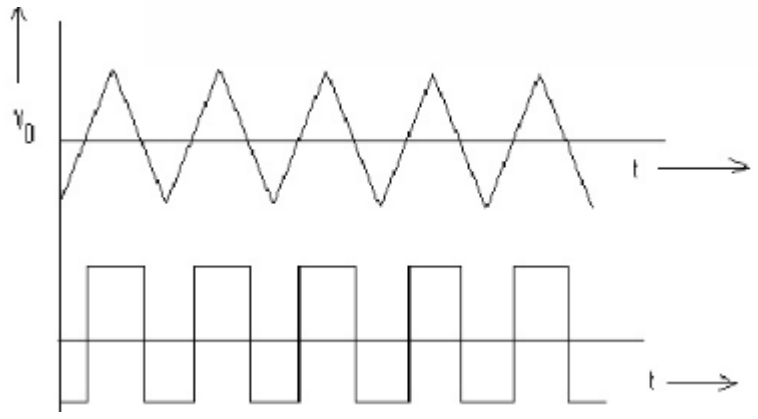
$$fo=2(V-Vc)/R_1C_1V$$

$$=2(15-5)/30kx0.01\mu f$$

$$=66kHz$$

R_1	C_1	Output Voltage (V)		Theoretical Frequency(KHz)	Practical Frequency(KHz)
		Square wave	triangular wave		

MODEL GRAPH:



RESULT:

The obtained output frequency of triangular wave = _____

The obtained output frequency of square wave = _____

The NE/SE 566 is operated as Voltage Controlled Oscillator also the output frequency for various values of R_1 and C_1 are observe and the values are equal theoretically also practically.

REVIEW QUESTIONS:

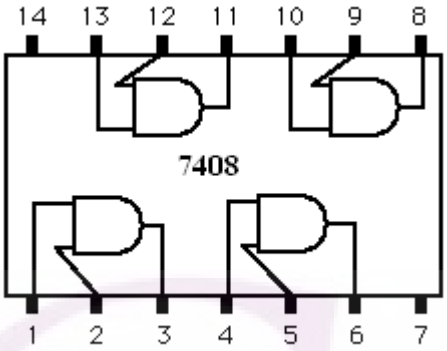
1. What are the applications of VCO?
2. Draw the pin diagram of NE/SE 566?
3. What is the need of connecting 0.001μF capacitor between pin 5 and pin 6?
4. What is time maker generator?
5. What are the differences between ideal and practical comparator?
6. What are the applications of comparator?
7. In which mode the operational amplifier is connected in the comparator circuit.

1.LOGIC GATES

AIM: Design following logic gates using VHDL and verify its functionality by writing test bench.

1) IC7408 2) IC7432 3) IC7404 4) IC7400 5) IC7402 6) IC7486

#1-TITLE: AND gate



LOGIC GATE SYMBOL:

TRUTH TABLE:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

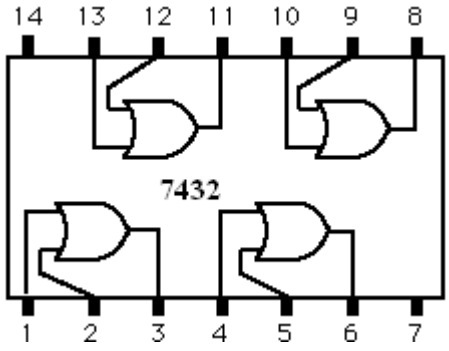
VHDL CODE:

AND 7408:

Test Bench

OUT PUT WAVE FORM:

LOGIC GATE SYMBOL:



TRUTH TABLE:

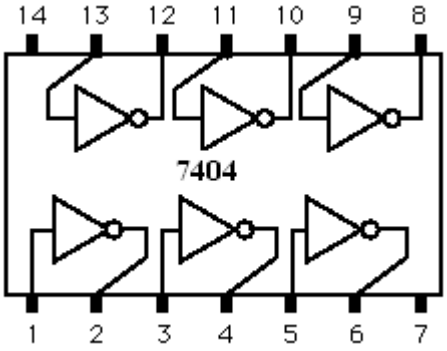
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

VHDL CODE:

Test Bench

OUTPUT WAVEFORM:

LOGIC GATE SYMBOL:



TRUTH TABLE:

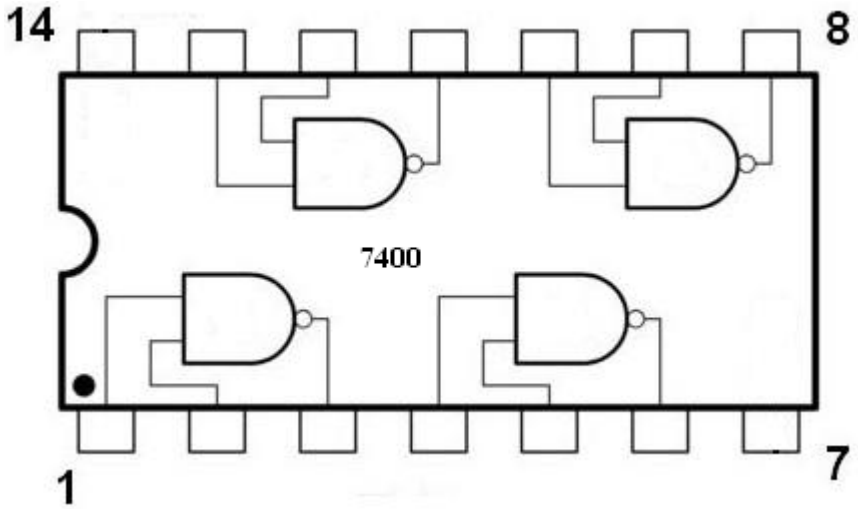
A	Y
0	1
1	0

VHDL CODE:
NOT GATE

Test Bench

OUTPUT WAVEFORM:

LOGIC GATE SYMBOL:



TRUTH TABLE:

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

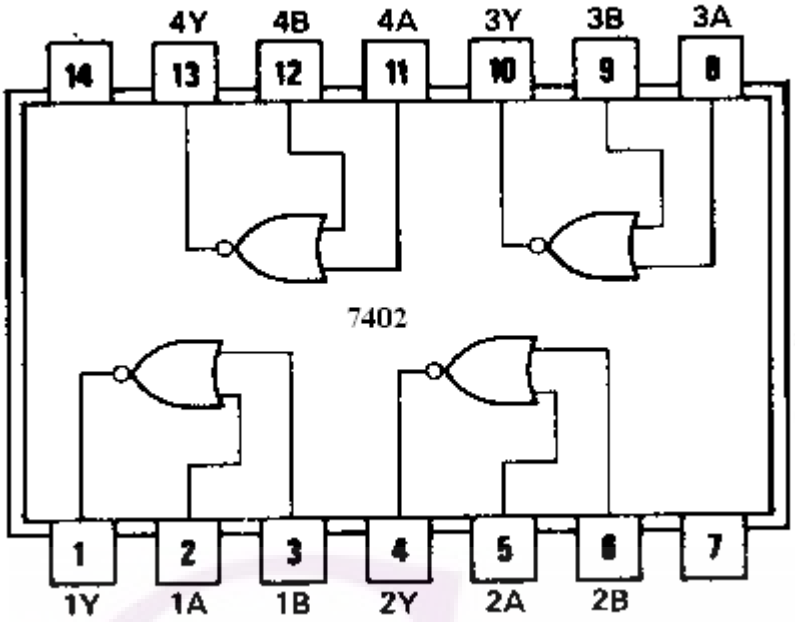
VHDL CODE:

NAND GATE

Test Bench

OUTPUT WAVEFORM:

LOGIC GATE



SYMBOL:

TRUTH TABLE:

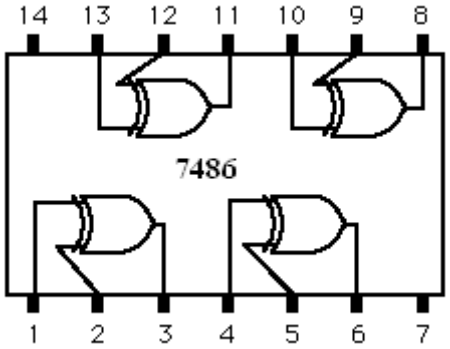
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

VHDL CODE:

TEST BENCH

OUTPUT WAVEFORM:

LOGIC GATE SYMBOL:



TRUTH TABLE:

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

VHDL CODE:

Test Bench

OUTPUT WAVEFORM:

VIVA QUESTIONS:

1. Implement the following function using VHDL coding. (Try to minimize if you can).

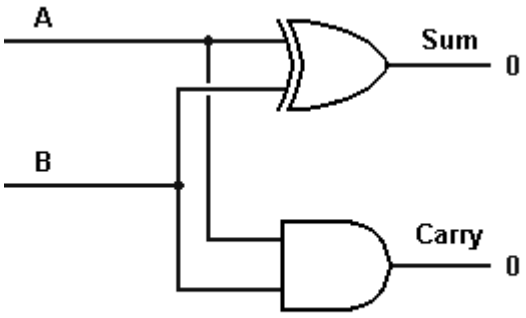
   F(A,B,C,D)=(A′+B+C) . (A+B′+D′). (B+C′+D′) . (A+B+C+D)

2. What will be the no. of rows in the truth table of N variables?
3. What are the advantages of VHDL?
4. Design Ex-OR gate using behavioral model?
5. Implement the following function using VHDL code
   f=AB+CD.
6. What are the differences between half adder and full adder?
7. What are the advantages of minimizing the logical expressions?
8. What does a combinational circuit mean?
9. Implement the half adder using VHDL code?
10. Implement the full adder using two half adders and write VHDL program in structural model?

2.HALF ADDER AND FULL ADDER

AIM: Design Half adder and verify its functionality by writing test bench.

LOGIC DIAGRAM



VHDL CODE:

Test Bench

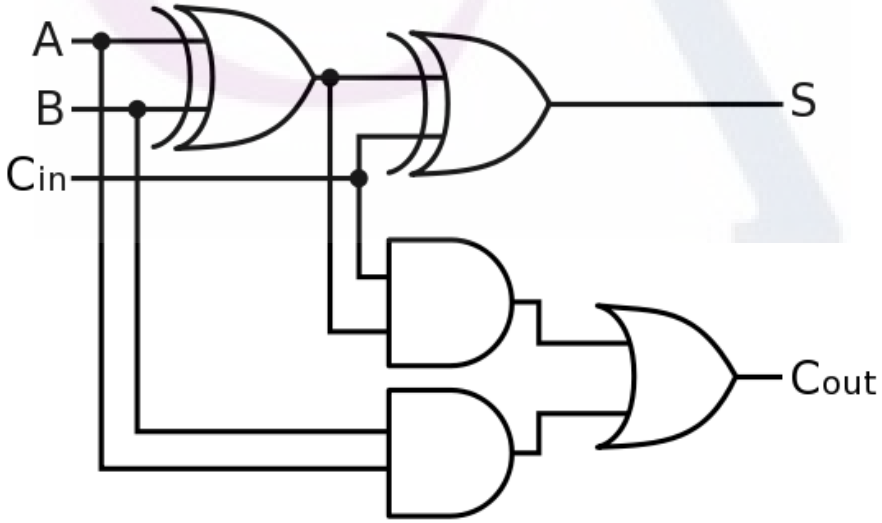
OUTPUT WAVEFORMS:

FULL ADDER

AIM:

Design Full adder and verify its functionality by writing test bench.

LOGIC DIAGRAM



VHDL CODE:

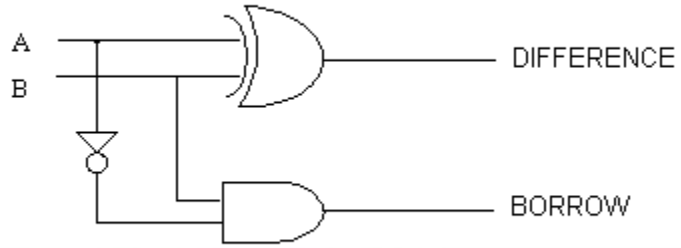
Test Bench

OUTPUT WAVEFORMS:

3.HALF SUBTRACTOR AND FULL SUBTRACTOR

AIM: Design Half subtractor and verify its functionality by writing test bench.

LOGIC DIAGRAM



VHDL CODE:

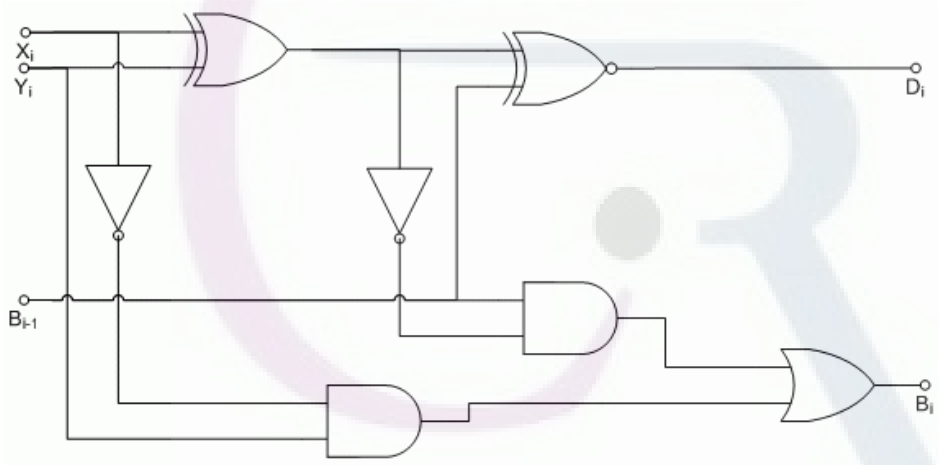
Test Bench

OUTPUT WAVEFORMS:

FULL SUBTRACTOR

AIM: Design Full subtractor and verify its functionality by writing test bench.

LOGIC DIAGRAM



VHDL CODE:

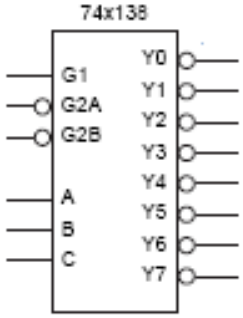
Test Bench

OUTPUT WAVEFORMS:

4.3x8 DECODER AND 8X3 ENCODER

AIM: Design IC74X138 and verify its functionality by writing test bench.

LOGIC SYMBOL:



TRUTH TABLE:

S.No	Enable inputs			Encoded inputs			Decoded output
	g1	g2a_l	g2b_l	A	B	C	
1	0	X	X	X	X	X	11111111
2	1	1	X	X	X	X	11111111
3	1	X	1	X	X	X	11111111
4	1	0	0	0	0	0	01111111
5	1	0	0	0	0	1	10111111
6	1	0	0	0	1	0	11011111
7	1	0	0	0	1	1	11101111
8	1	0	0	1	0	0	11110111
9	1	0	0	1	0	1	11111011
10	1	0	0	1	1	0	11111101
11	1	0	0	1	1	1	11111110

VHDL CODE:

TEST BENCH

OUTPUT WAVEFORMS:

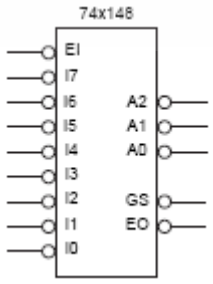
VIVA QUESTIONS
:

1. Write the behavioral code for the IC 74x138.
2. Write the VHDL code for the IC 74x138 using CASE statement.
3. Write the VHDL code for the IC 74x138 using WITH statement.
4. Write the VHDL code for the IC 74x138 using WHEN--ELSE statement.
5. Write the structural program for IC 74x138.
6. What does priority encoder mean?
7. How many decoders are needed to construct 4X16 decoder?
8. What is the difference between decoder and encoder?
9. Write the syntax for exit statement?
10. Explain briefly about next statement?

8x3 ENCODER

AIM: Design IC74X148 and verify its functionality by writing test bench.

LOGIC SYMBOL:



VHDL CODE:

TEST BENCH

OUTPUT WAVEFORMS:

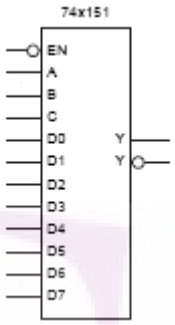
OUTPUT WAVEFORMS FOR IC74X148 (ENCODER)

5.8x1 MULTIPLEXER AND DEMULTIPLEXER

AIM: Design IC74X151 and verify its functionality by writing test bench.

TITLE: IC74151—8x1 multiplexer.

LOGIC SYMBOL:



TRUTH TABLE:

S.No	en_l	Data select lines			Output Y
		A	B	C	
1	0	0	0	0	I(0)
2	0	0	0	1	I(1)
3	0	0	1	0	I(2)
4	0	0	1	1	I(3)
5	0	1	0	0	I(4)
6	0	1	0	1	I(5)
7	0	1	1	0	I(6)
8	0	1	1	1	I(7)
9	1	X	X	X	0

VHDL CODE:

TEST BENCH

OUTPUT WAVEFORMS:

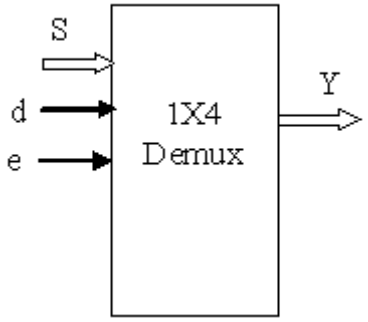
VIVA QUESTIONS
:

1. Write the behavioral code for the IC 74x151.
2. Write the VHDL code for the IC 74x151 using IF statement.
3. Write the VHDL code for the IC 74x151 using WITH statement.
4. Write the VHDL code for the IC 74x151 using WHEN--ELSE statement.
5. Write the structural program for IC 74x151.
6. What is meant by multiplexer?
7. What does demultiplexer mean?
8. How many 8X1 multiplexers are needed to construct 16X1 multiplexer?
9. Compare decoder with demultiplexer?
10. Design a full adder using 8X1 multiplexer?

DEMULTIPLEXER

AIM: Design 1 to 4 demultiplexer and verify its functionality by writing test bench.

BLOCK DIAGRAM



TRUTH TABLE:

E	S1	S0	Y0	Y1	Y2	Y3
0	X	X	0	0	0	0
1	0	0	D	0	0	0
1	0	1	0	D	0	0
1	1	0	0	0	D	0
1	1	1	0	0	0	D

VHDL CODE:

TEST BENCH

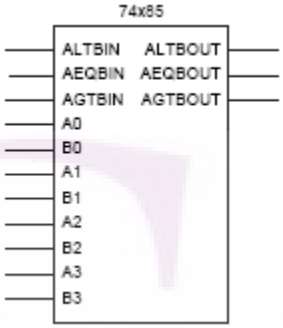
OUTPUT WAVEFORMS:

6.IC 74x85 – 4-BIT COMPARATOR

AIM: Design IC74X85 and verify its functionality by writing test bench.

.

BLOCK DIAGRAM:



TRUTH TABLE:

S.No.	Cascade inputs	Present input condition			AGTBOUT	AEQBOUT	ALTBOUT
		A>B	A=B	A<B			
1	AGTBIN=1	X	X	X	1	0	0
2	AEQBIN=1	1	0	0	1	0	0
		0	1	0	0	1	0
		0	0	1	0	0	1
5	ALTBIN=1	X	X	X	0	0	1

VHDL CODE:

TEST BENCH

OUTPUT WAVEFORMS:

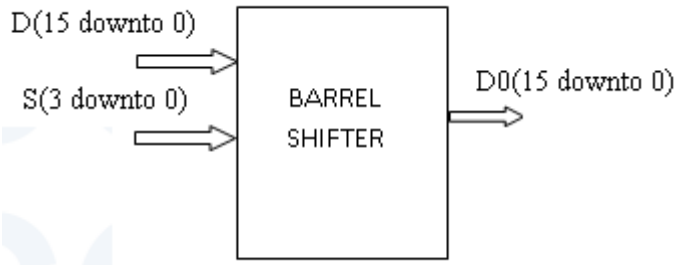
VIVA QUESTIONS:

1. Write the dataflow model for the IC 74x85.
2. Write the VHDL code for the IC 74x85 using CASE statement.
3. Write the VHDL code for the IC 74x85 using WITH statement.
4. Write the VHDL code for the IC 74x85 using WHEN--ELSE statement.
5. Write the structural program for IC 74x85.
6. How many 4-bit comparators are needed to construct 12-bit comparator?
7. What does a digital comparator mean?
8. Design a 2-bit comparator using gates?
9. Explain the phases of a simulation?
10. Explain briefly about wait statement?

7.BARREL SHIFTER

AIM: Design Barrel shifter for left circular shift and verify its functionality by writing test bench.

BLOCK DIAGRAM:



VHDL CODE:

TEST BENCH

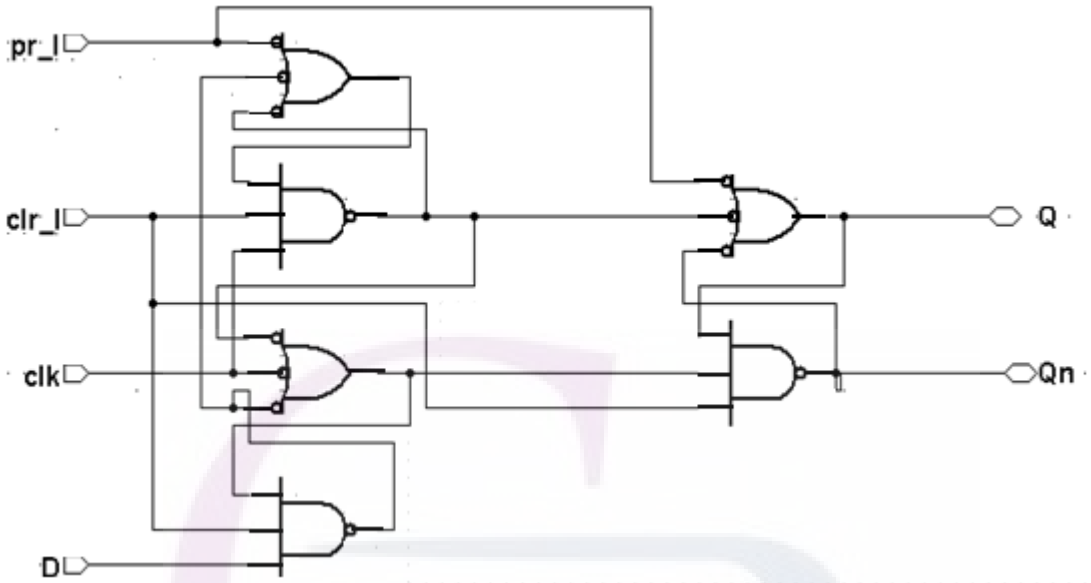
OUTPUT WAVEFORMS:

8.IC7474—A POSITIVE EDGE TRIGGERING D FLIP FLOP

AIM: Write a VHDL code for IC7474—a positive edge triggering D flip flop.

TITLE: IC7474—a positive edge triggering D flip flop.

CIRCUIT DIAGRAM:



TRUTH TABLE:

clr_l	pr_l	Clk	d	q	qn
0	0	X	X	1	1
0	1	X	X	0	1
1	0	X	X	1	0
1	1	↑	0	0	1
1	1	↑	1	1	0

VHDL CODE:

OUTPUT WAVEFORMS:

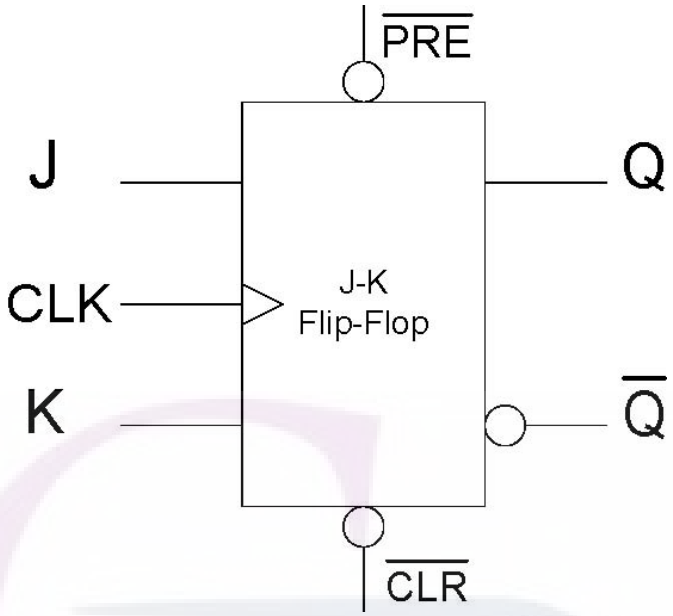
D FLIPFLOP

NAND GATE

9.IC 74X109 JK FLIP FLOP

AIM: Design Barrel JK Flip-Flop 74X109 and verify its functionality by writing test bench.

BLOCK DIAGRAM:



CHARACTERISTIC TABLE:

	INPUTS					OUTPUTS	
	PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
1	0	0	X	X	X	1	1
2	0	1	X	X	X	1	0
3	1	0	X	X	X	0	1
4	1	1	↓	0	0	0	$\overline{Q}$
5	1	1	↓	1	0	1	0
6	1	1	↓	0	1	0	1
7	1	1	↓	1	1	TOGGLE	
8	1	1	0	X	X	Q	$\overline{Q}$

X = IRRELEVANT

VHDL CODE:

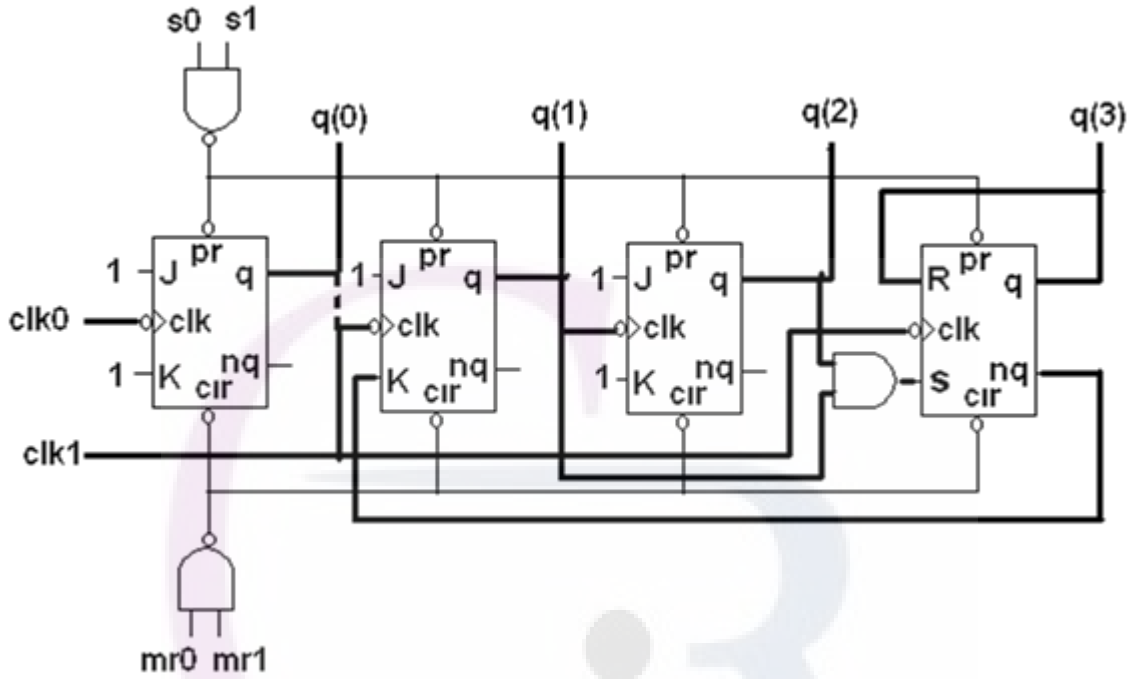
TEST BENCH:

OUTPUT WAVEFORMS:

10.IC 74x90 – DECADE COUNTER

AIM: To write the VHDL code for IC 74x90 – decade counter.

CIRCUIT DIAGRAM OF IC 74x90:



TRUTH TABLE:

OUTPUT			
Q(0)	Q(3)	Q(2)	Q(1)
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0

VHDL CODE:

OUTPUT WAVEFORMS:

JK FLIP FLOP:

OUTPUT WAVEFORMS:

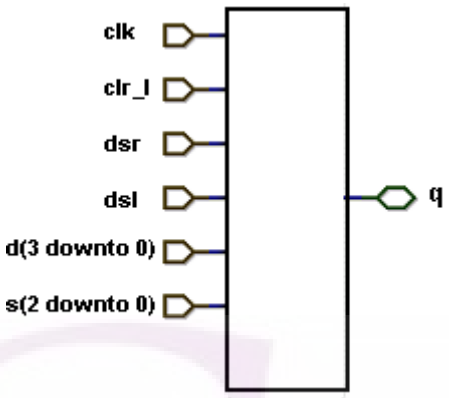
VIVA QUESTIONS:

1.Write the behavioral code for IC 74x90.
1.What is a sequential circuit?
2.Differentiate between synchronous and asynchronous counter?
3.How many no.of flip-flops are required for decade counter?
4.What is meant by excitation table?
5.What are the meanings of different types of values in std_ulogic?
6.What are the objects in VHDL?
7.Write the syntax for a signal?
8.Write the difference between signal and variable?
9.Explain about enumeration types?
10.If the modulus of a counter is 12 how many flip-flops are required?

11.IC 74x194 –UNIVERSAL SHIFT REGISTER

AIM: To write the VHDL code for IC 74x194 –universal shift register.

BLOCK DIAGRAM:



TRUTH TABLE:

Clr_l	S(1)	S(0)	Clk	Output function
0	X	X	X	1
1	0	0	↑	no change
1	0	1	↑	shift right (dsr to q(0))
1	1	0	↑	shift left (dsl to q(3))
1	1	1	↑	load data (parallel shifting)

VHDL code:

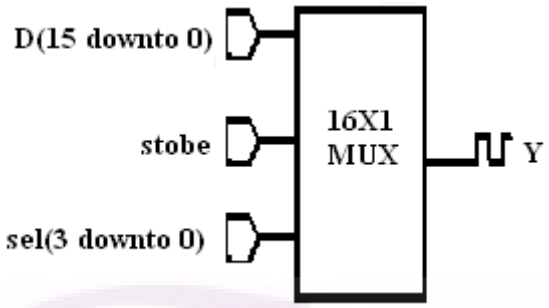
OUTPUT WAVEFORMS:

12.16X1 MULTIPLEXER

AIM: Write a VHDL code for IC74150—16x1 multiplexer.

TITLE: IC74150—16x1 multiplexer.

BLOCK DIAGRAM:



TRUTH TABLE:

S.No.		Data select lines				output
	strobe	A	B	C	D	Y
1	0	0	0	0	0	d'(0)
2	0	0	0	0	1	d'(1)
3	0	0	0	1	0	d'(2)
4	0	0	0	1	1	d'(3)
5	0	0	1	0	0	d'(4)
6	0	0	1	0	1	d'(5)
7	0	0	1	1	0	d'(6)
8	0	0	1	1	1	d'(7)
9	0	1	0	0	0	d'(8)
10	0	1	0	0	1	d'(9)
11	0	1	0	1	0	d'(10)
12	0	1	0	1	1	d'(11)
13	0	1	1	0	0	d'(12)
14	0	1	1	0	1	d'(13)
15	0	1	1	1	0	d'(14)
16	0	1	1	1	1	d'(15)
17	1	X	X	X	X	1

VHDL CODE:

OUTPUT WAVEFORMS: