DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

***COURSE*: LINEAR AND DIGITAL IC APPLICATIONS**

***BRANCH**: Electrical and Electronics Engineering*

LECTURE NOTES

INDEX

UNIT I

INTEGRATED CIRCUITS

1.1 INTEGRATED CIRCUITS

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

1.2 Advantages of integrated circuits

1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

Depending upon the number of active devices per chip,there are different levels of integration

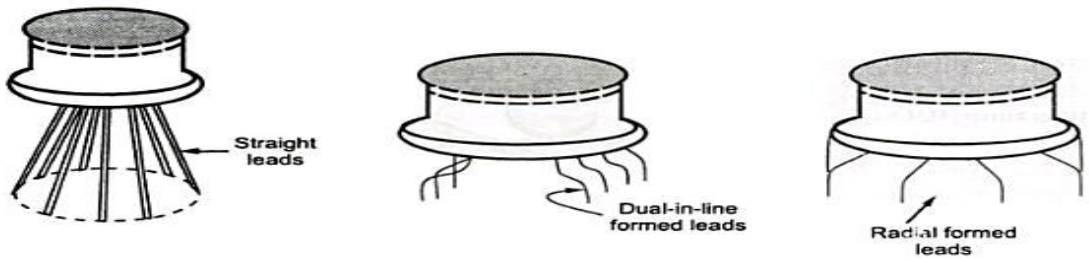
	Level of Integration	Number of active devices per chip
1.	Small scale integration (SSI)	Less than 100
2.	Medium scale integration (MSI)	100 - 10000
3.	Large scale integration (LSI)	1000 - 100,000
4.	Very large scale integration (VLSI)	Over 100,000
5.	Ultra large scale integration (ULSI)	Over 1 million

1.3 IC Package Types

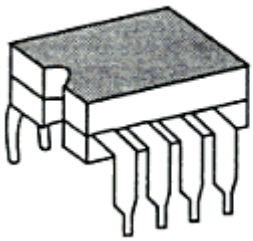
The op-amp ICs are available in various packages. The IC packages are classified as,

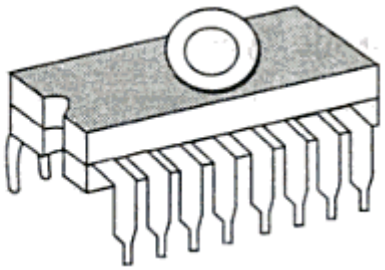
1. Metal Can
2. Dual In Line
3. Flat Pack

1.4 Metal Can package:

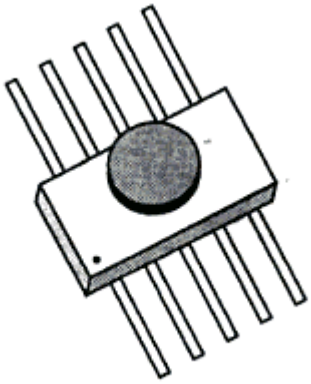


1.5 Dual- in- Line Package:





1.6 Flat Pack:



10 lead version

1.7 DIFFERENTIAL AMPLIFIER:

The differential amplifier consists of two symmetrical common-emitter sections and is capable of amplifying the difference between two input signals. The differential amplifier can amplify ac as well as dc input signals because it employs direct coupling.

There are four types of differential amplifier configurations:

(a)The dual Input, Balanced output differential amplifier

DC Analysis------ $I_E = V_{EE} - V_{BE}/2R_E$,

$V_{CE} = Vcc + V_{BE} - R_c I_c$

AC Analysis------- $A_d = R_C/r_e$

$R_{i1} = R_{i2} = 2\beta_{ac} r_e$

$R_{01} = R_{02} = R_c$

(b)The dual input, unbalanced output differential Amplifier

DC Analysis--------- $I_E = V_{EE} - V_{BE}/(2R_E + R_{in}/\beta_{dc})$

$V_{CE} = Vcc + V_{BE} - R_c I_{CQ}$

AC Analysis---------- $A_d=R_C/2r_e$

$R_{i1}= R_{i2}=2\beta_{ac}r_e$

$R_0= R_c$

(c) The single input, balanced output differential Amplifier

DC Analysis ---------$I_E =V_{EE} - V_{BE}/(2R_E+R_{in}/\beta_{dc})$

$V_{CE}=Vcc+ V_{BE}-R_cI_{CQ}$

AC Analysis---------- $I_E =V_{EE} - V_{BE}/(2R_E+R_{in}/\beta_{dc})$

$R_i=2\beta_{ac}r_e$

$R_{01}=R_{02}=R_c$

(d)The single input, unbalanced output differential Amplifier

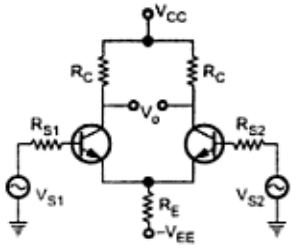
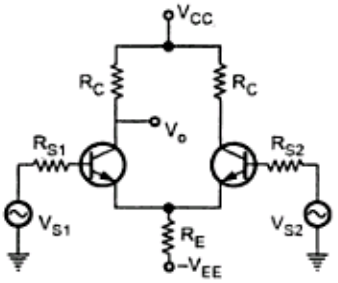
DC Analysis--------- $I_E =V_{EE} - V_{BE}/(2R_E+R_{in}/\beta_{dc})$

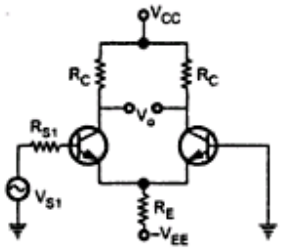
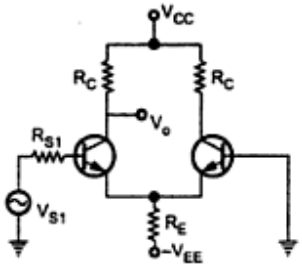
$V_{CE}=Vcc+ V_{BE}-R_cI_{CQ}$

AC Analysis--------- $A_d=R_C/2r_e$

$R_{i=}2\beta_{ac}r_e$

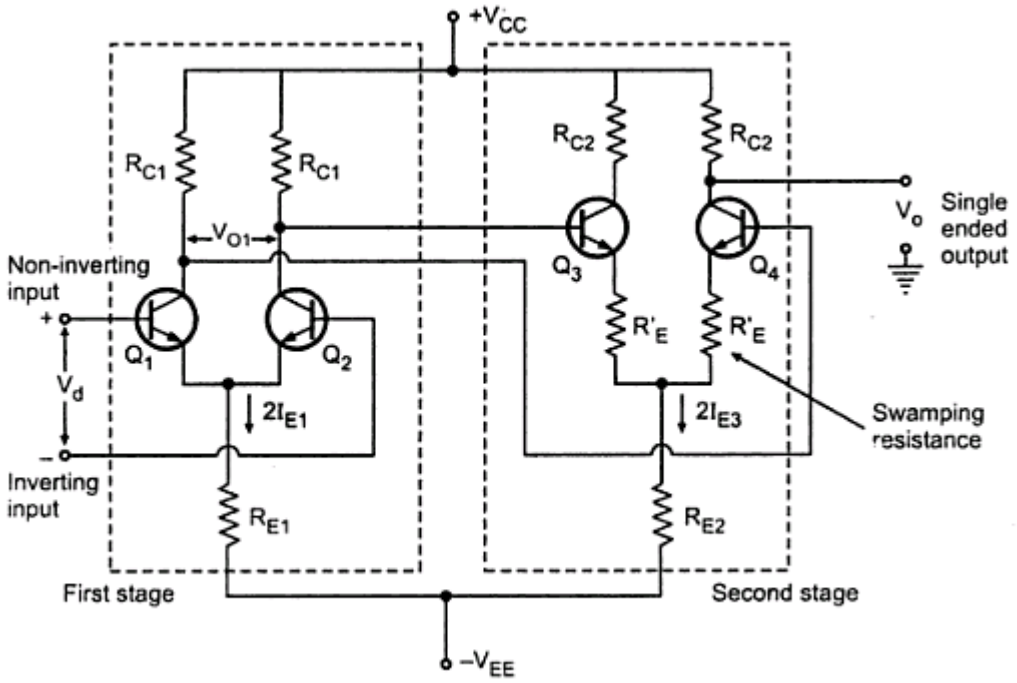
$R_0=$ R_c

Configuration	Circuit	A_d voltage gain	R_{in} Input Resistance	R_o Output Resistance
Dual Input Balanced Output		$\frac{h_{fe} R_C}{R_S + h_{ie}}$	$2(R_S + h_{ic})$	R_C
Dual Input Unbalanced Output		$\frac{h_{fe} R_C}{2(R_S + h_{ie})}$	$2(R_S + h_{ic})$	R_C

Single Input Balanced Output		$\frac{h_{fe} R_C}{R_S + h_{ie}}$	$2(R_S + h_{ic})$	R_C
Single Input Unbalanced Output		$\frac{h_{fe} R_C}{2(R_S + h_{ie})}$	$2(R_S + h_{ic})$	R_C

1.8 Cascade Differential Amplifier Stages:

In cascaded differential amplifier, the output of the first stage is used as an input for the second stage, the output of the second stage is applied as an input to the third stage, and so on. Because of direct coupling between the stages, the operating point of succeeding stages changes



UNIT-II

CHARACTERISTICS OF OP-AMP

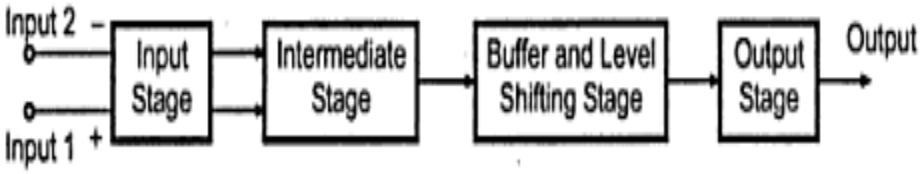
2.1 Ideal OP-AMP

An ideal OP-AMP would have the following characteristics:

1. The input resistance R_{IN} would be infinite
2. The output resistance R_{OUT} would be zero
3. The voltage gain, V_G would be infinite
4. The bandwidth (how quickly the output will follow the input) would be infinite
5. If the voltages on the two inputs are equal than the output voltage is zero (If the output is not zero it is said to have an offset)

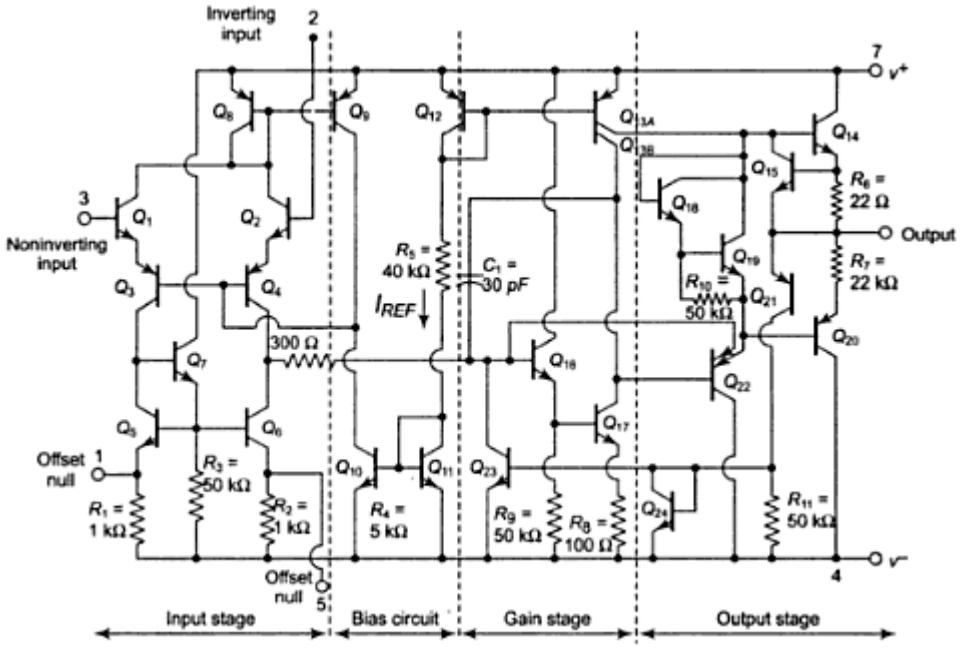
2.2. Block diagram of op-amp:

The block diagram of IC op-amp is as shown in figure



2.3 Op-amp 741:

The IC 741 is high performance monolithic op-amp IC .It is available in 8 pin, 10 pin or 14 pin configuration. It can operate over a temperature of -55 to 125 centigrade.op-amp 741 equivalent circuit is as shown in figure.



2.4 Features of IC-741

i. No frequency compensation required.
ii. Short circuit protection provided.
iii. Offset voltage null capability.
iv. Large common mode and Differential voltage range.
v. No latch up.

2.5 PSRR:

PSRR is Power Supply Rejection Ratio. It is defined as the change in the input offset voltage due to the change in one of the two supply voltages when other voltage is maintained constant. It's ideal value should be Zero.

2.6 Slew Rate:

The maximum rate of change of output voltage with respect to time is called Slew rate of the Op-amp.

It is expressed as, $S = \text{——}_{max}$ and measured in V/sec.

The Slew rate equation is, $S = 2\pi f V_m$ V/sec

2.7 Frequency compensation technique:

In application where one desires large bandwidth and lower closed loop gain, suitable compensation technique are used: Two types of compensation techniques are used

1. External compensation
2. Internal compensation

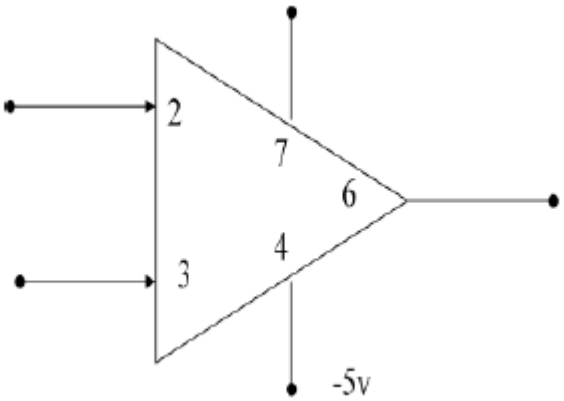
UNIT III

APPLICATIONS OF OP-AMPS

3.1 OPERATION AMPLIFIER

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage. It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

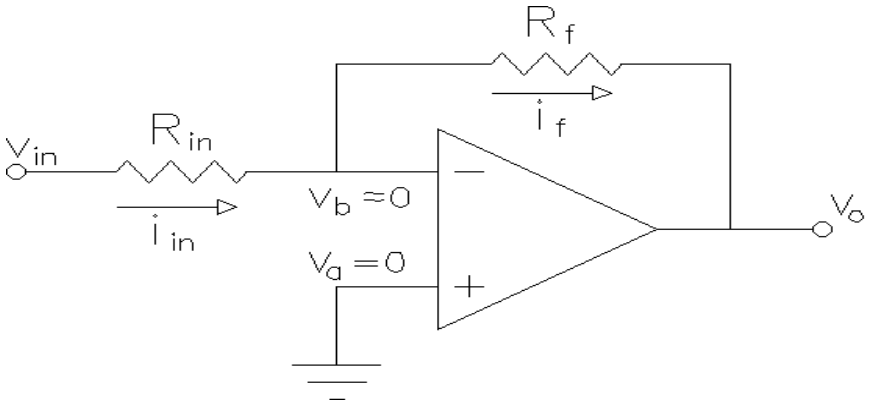
3.2 Op-amp symbol



3.3 Ideal characteristics of OPAMP

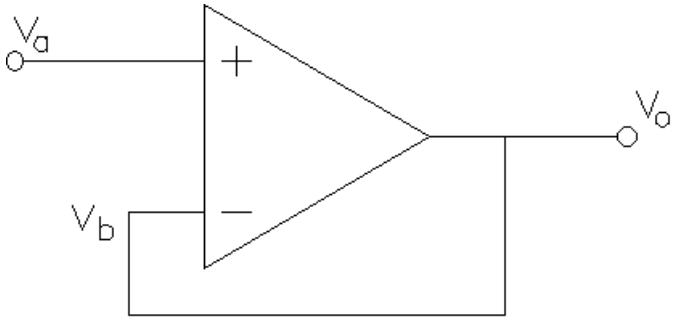
1. Open loop gain infinite
2. Input impedance infinite
3. Output impedance low
4. Bandwidth infinite
5. Zero offset, ie, Vo=0 when V1=V2=0

3.4 Inverting Op-Amp



$$V_{OUT} = -V_{IN}\frac{R_f}{R_1}$$

3.5 Voltage follower



$$V_{OUT} = V_{IN}$$

3.6 DC characteristics

3.6.1 Input offset current

The difference between the bias currents at the input terminals of the op- amp is called as input offset current. The input terminals conduct a small value of dc current to bias the input transistors. Since the input transistors cannot be made identical, there exists a difference in bias currents

3.6.2 Input offset voltage

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage

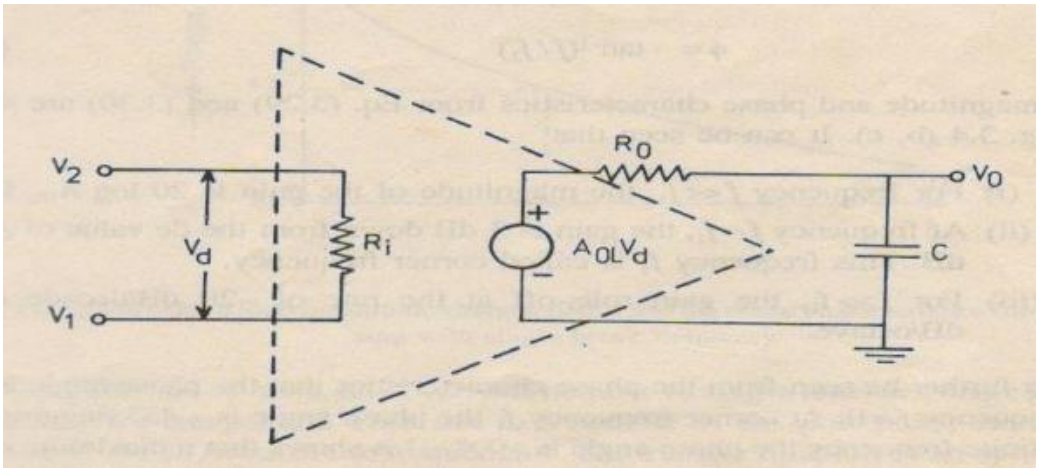
3.6.3 Input bias current

Input bias current IB as the average value of the base currents entering into terminal of an op-amp

$$\mathbf{I_B = I_B^+ + I_B^-}$$

3.7 AC characteristics

3.7.1 Frequency Response



3.7.2 HIGH FREQUENCY MODEL OF OPAMP

3.7.2.1. Need for frequency compensation in practical op-amps

• Frequency compensation is needed when large bandwidth and lower closed loop gain is desired.

• Compensating networks are used to control the phase shift and hence to improve the stability

3.7.2.2. Frequency compensation methods

• Dominant- pole compensation

• Pole- zero compensation

3.7.2.3. Slew Rate

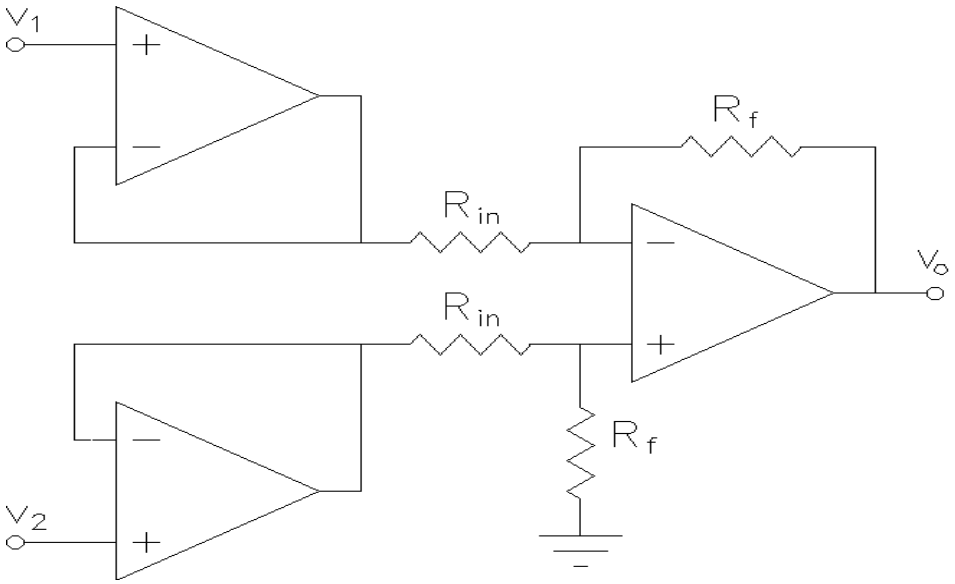
• The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage.

• An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage

3.8 Instrumentation Amplifier

In a number of industrial and consumer applications, the measurement of physical quantities

is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

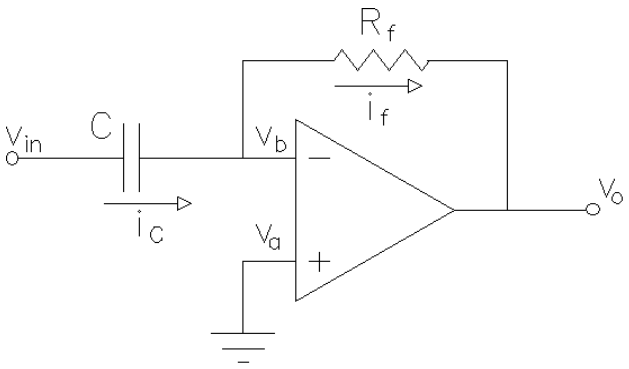


3.9 Features of instrumentation amplifier

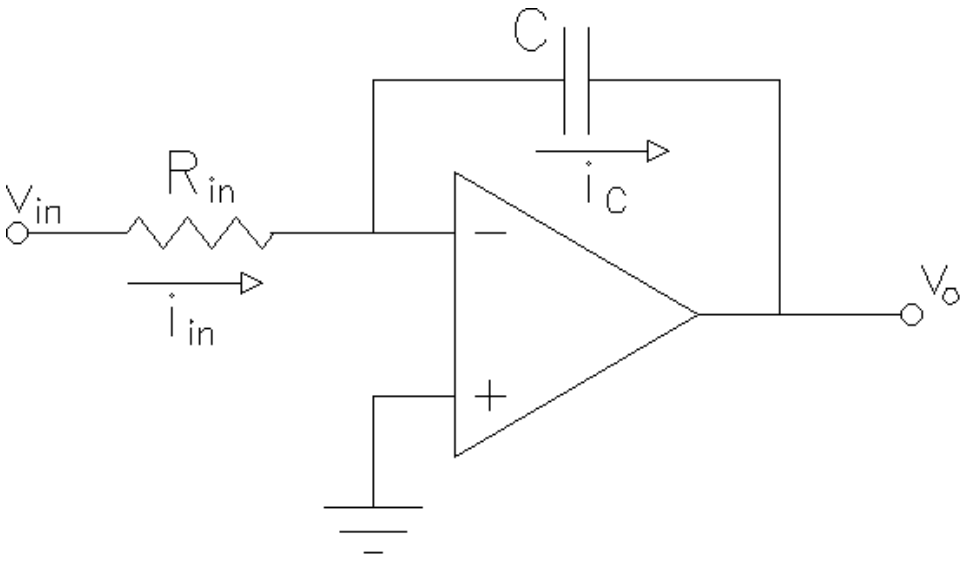
1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co- efficient
4. low dc offset
5. low output impedance

3.10 Differentiator

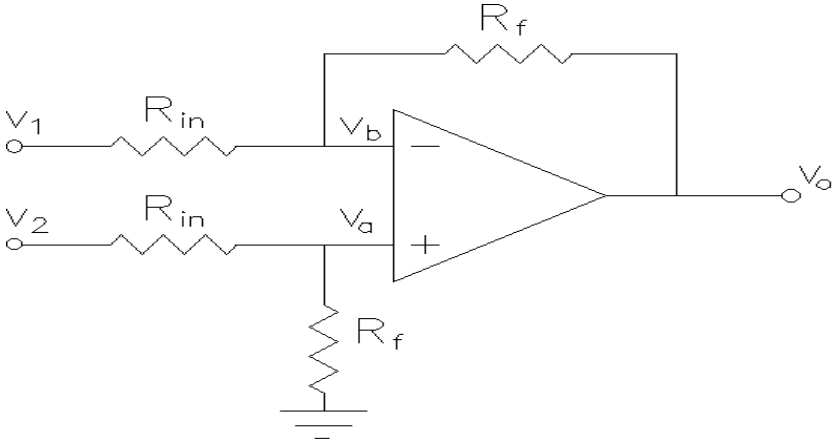
The circuit which produces the differentiation of the input voltage at its output is called differentiator. The differentiator circuit which does not use any active device is called passive differentiator. While the differentiator using an active device like op-amp is called an active differentiator.



3.11 Integrator:



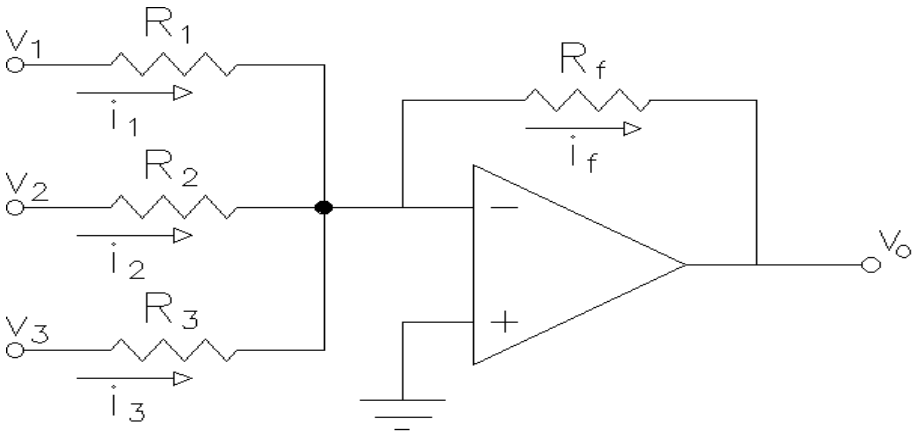
3.12 Differential amplifier:



This circuit amplifies only the difference between the two inputs. In this circuit there are two

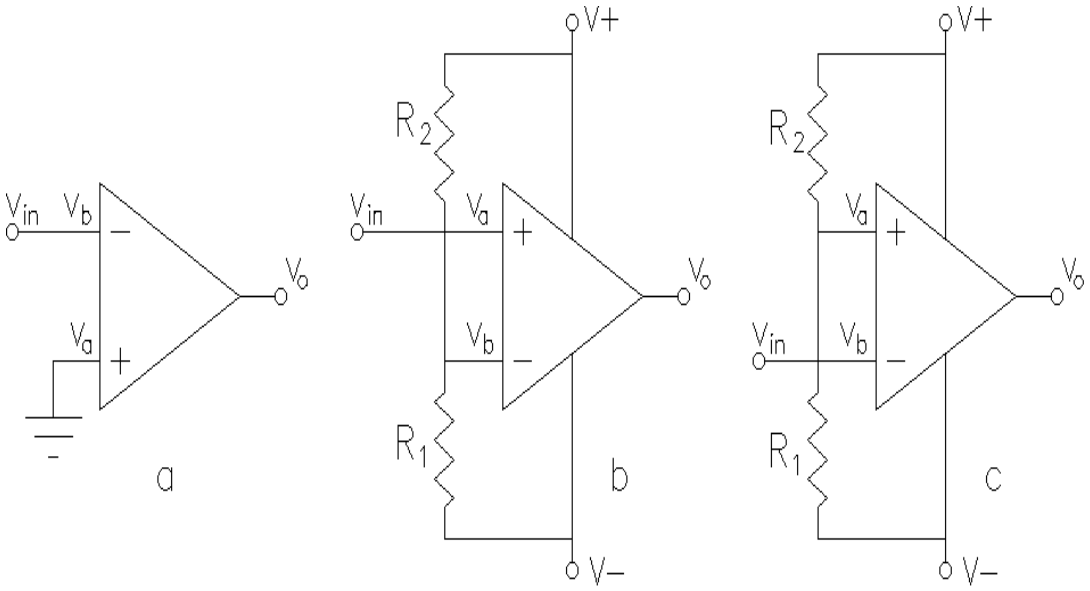
resistors labeled R IN Which means that their values are equal. The differential amplifier amplifies the difference of two inputs while the differentiator amplifies the slope of an input

3.13 Summer:



3.14 Comparator:

A comparator is a circuit which compares a signal voltage applied at one input of an op- amp with a known reference voltage at the other input. It is an open loop op - amp with output.



3.15 Applications of comparator:

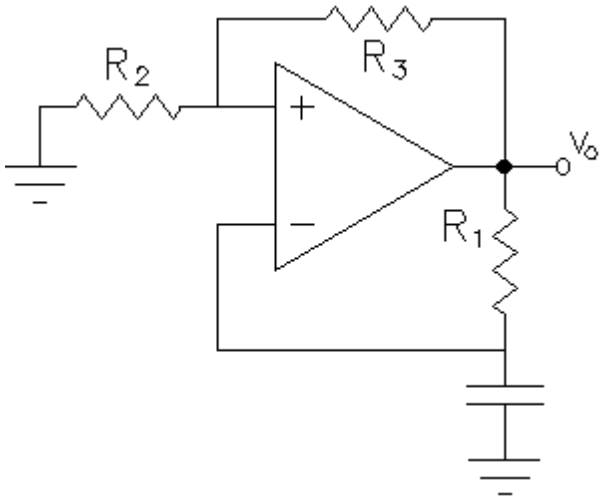
1. Zero crossing detector
2. Window detector
3. Time marker generator
4. Phase detector

3.15 Triangular wave Generator:

The output of the integrator is triangular if the input is a square wave. This means that a triangular wave generator can be formed by simply connecting an integrator to the square wave generator.

3.17 Square wave generator:

Square wave outputs are generated when the op-amp is forced to operate in the saturated region. That is, the output of the op-amp is forced to swing repetitively between positive saturation and negative saturation. The square wave generator is also called as free-running or Astable mutivibrator



UNIT IV

TIMERS & PHASE LOCKED LOOPS

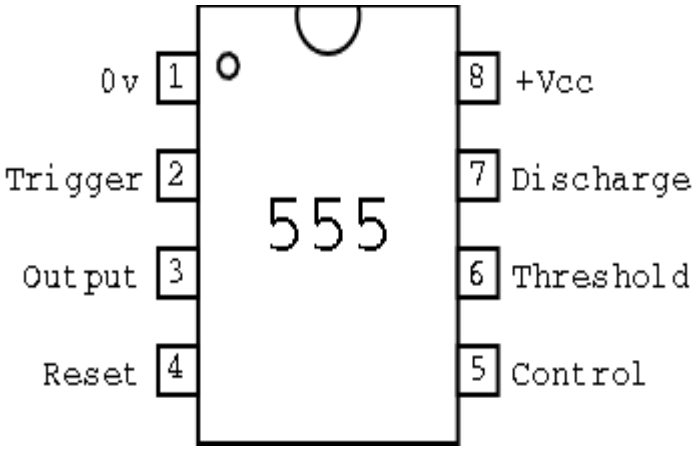
4.1 555 Timer:

The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions. IC NE/SE 555 is a highly stable device for generating accurate time delays. Commercially, this IC is available in 8-pin circular, TO-99 or 8-pin DIP or 14-pin DIP packages.

The salient features of 555 Timer IC's are:

- ✓ Compatible with both TTL and CMOS logic families.
- ✓ The maximum load current can go up to 200 mA.
- ✓ The typical power supply is from +5V to +18 V
- ✓

Pin diagram of 555 timer is as shown in figure:



4.2 Features of 555 Timer Basic blocks

1. It has two basic operating modes: monostable and astable
2. It is available in three packages. 8 pin metal can , 8 pin dip, 14 pin dip.
3. It has very high temperature stability

4.3 Applications of 555 Timer

1. astable multivibrator
2. monostable multivibrator
3. Missing pulse detector
4. Linear ramp generator

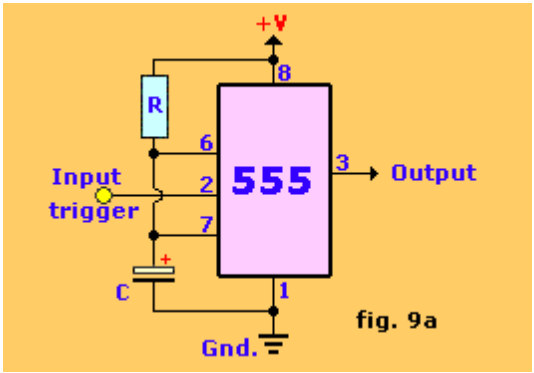
5. Frequency divider
6. Pulse width modulation
7. FSK generator
8. Pulse position modulator
9. Schmitt trigger

4.4 Multivibrator

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator

4.4.1 Monostable multivibrator

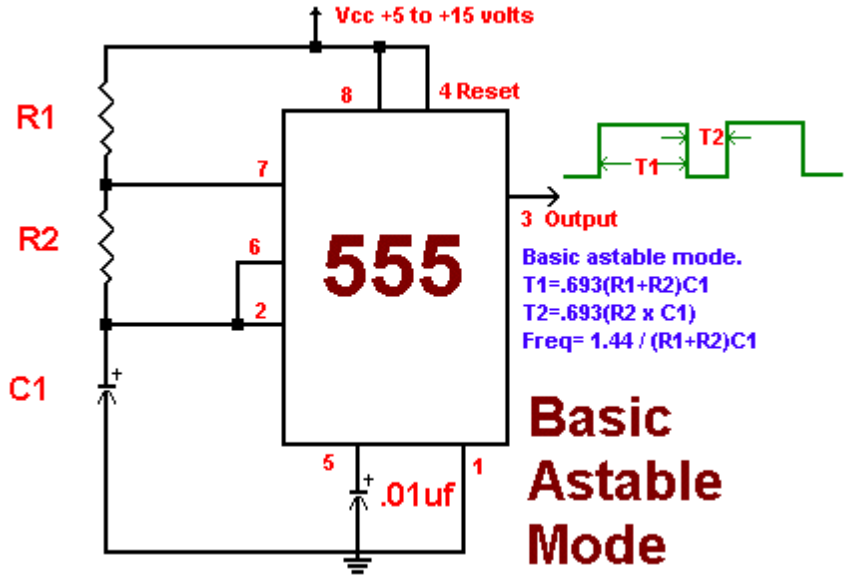
Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi- stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state



4.4.2 Astable multivibrator

Astable multivibrator is a free running oscillator having two quasi- stable states. Thus, there is oscillations between these two states and no external signal are required to produce the in state Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state,

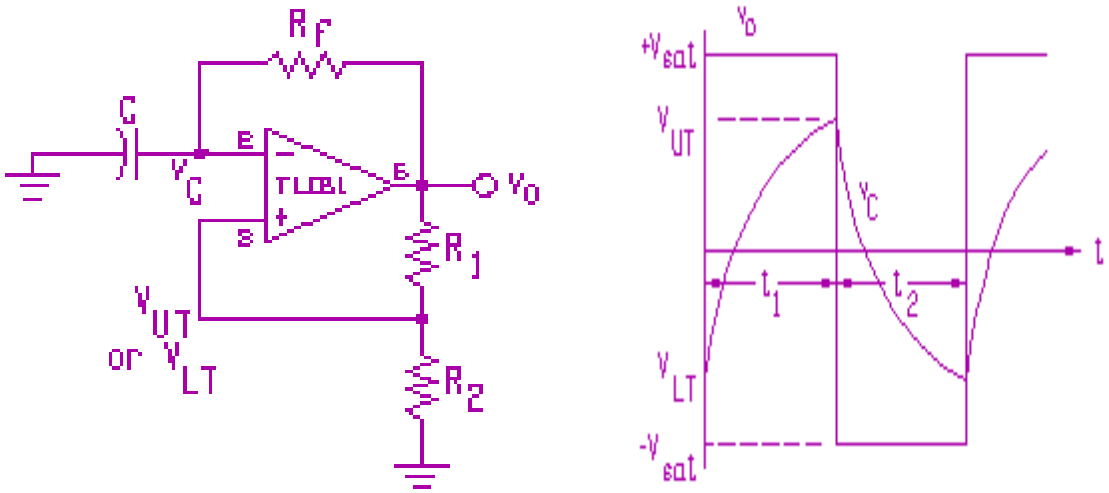
and this output level is maintained indefinitely until an second trigger is applied. Thus, it requires two external triggers before it returns to its initial state



4.4.3 Bistable multivibrator

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied. Thus, it requires two external triggers before it returns to its initial state

4.5 Astable Multivibrator or Relaxation Oscillator



4.5.1 Equations for Astable Multivibrator

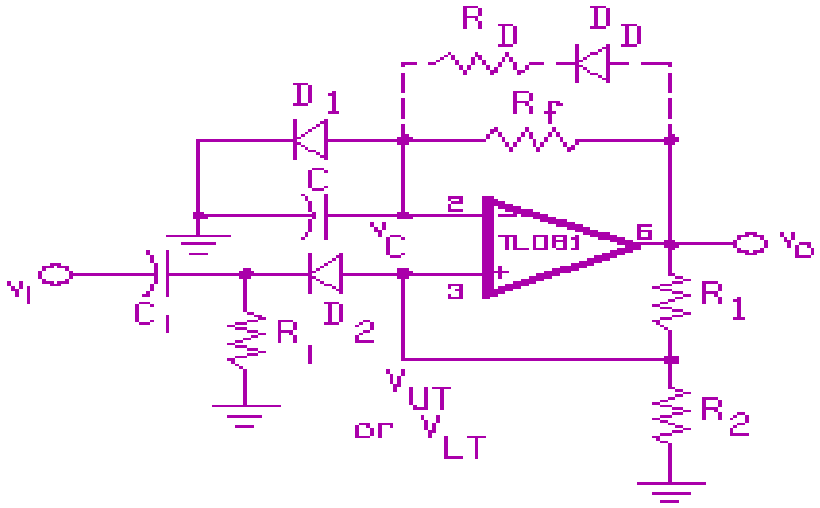
$$V_{UT} = \frac{+V_{sat}R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat}R_2}{R_1 + R_2}$$

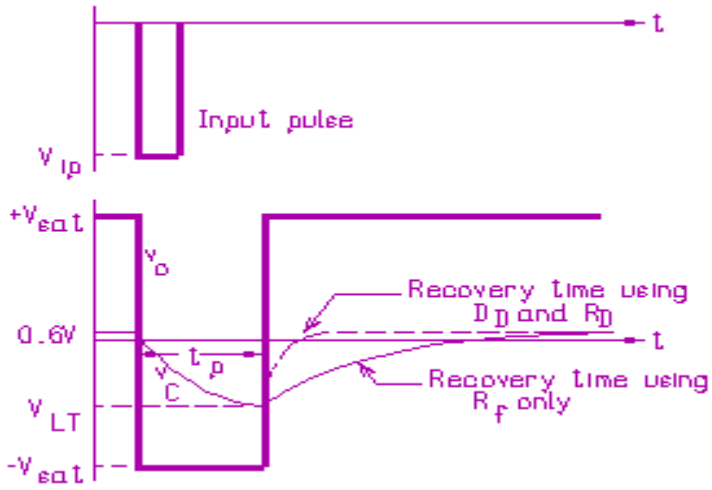
$$V_{UT} = \frac{+V_{sat}R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat}R_2}{R_1 + R_2}$$

$$T = t_1 + t_2 = 2\tau \ln\left(\frac{R_1 + 2R_2}{R_1}\right)$$

$$f = \frac{1}{2R_fC}$$

4.6 Monostable (One-Shot) Multivibrator





4.6.1 Notes on Monostable Multivibrator:

• Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V

• Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$. Best to select $R_iC_i \# 0.1R_fC$.

• Timing state: C charges negatively from 0.6 V through R_f. Width of timing pulse is:Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V

• Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$. Best to select $R_iC_i \# 0.1R_fC$. Timing state: C charges negatively from 0.6 V through R_f.

Recovery state: $v_o = +V_{sat}$; circuit is not ready for retriggering until $V_C = 0.6$ V. The *recovery time* t_p. To speed up the recovery time, R_D (= $0.1R_f$) & C_D can be added.

4.7 Voltage controlled oscillator

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage

4.7.1 The features of 566 VCO

1. Wide supply voltage range(10- 24V)
2. Very linear modulation characteristics
3. High temperature stability

4.8 Phase Lock Looped

A PLL is a basically a closed loop system designed to lock output frequency and phase to the frequency and phase of an input signal

4.8.1 Applications of 565 PLL

1. Frequency multiplier
2. Frequency synthesizer
3. FM detector

UNIT V

ACTIVE FILTERS

5.1 Filter

Filter is a frequency selective circuit that passes signal of specified Band of frequencies and attenuates the signals of frequencies outside the band

5.2 Type of Filter

1. Passive filters
2. Active filters

5.2.1. Passive filters

Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive.For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation

5.2.2. Active filters

Active filters used op- amp as the active element and resistors and capacitors as passive elements. By enclosing a capacitor in the feed back loop , inductor less active filters can be obtained

5.3 Some commonly used active filters

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter

5.4 Active Filters

• Active filters use op-amp(s) and RC components.

• Advantages over passive filters:

– op-amp(s) provide gain and overcome circuit losses

– increase input impedance to minimize circuit loading

– higher output power

– sharp cutoff characteristics can be produced simply and efficiently without bulky inductors

• Single-chip universal filters (e.g. switched-capacitor ones) are available that can be configured for any type of filter or response.

5.5 Review of Filter Types & Responses

• 4 major types of filters: low-pass, high-pass, band pass, and band-reject or band-stop

• 0 dB attenuation in the pass band (usually)

• 3 dB attenuation at the *critical* or *cutoff frequency*, f_c (for Butterworth filter)

• Roll-off at 20 dB/dec (or 6 dB/oct) per *pole* outside the passband (# of poles = # of reactive elements). Attenuation at any frequency, f, is

• Bandwidth of a filter: BW = f_{cu} - f_{cl}

• Phase shift: 45o/pole at f_c; 90o/pole at >> f_c

• 4 types of filter responses are commonly used:

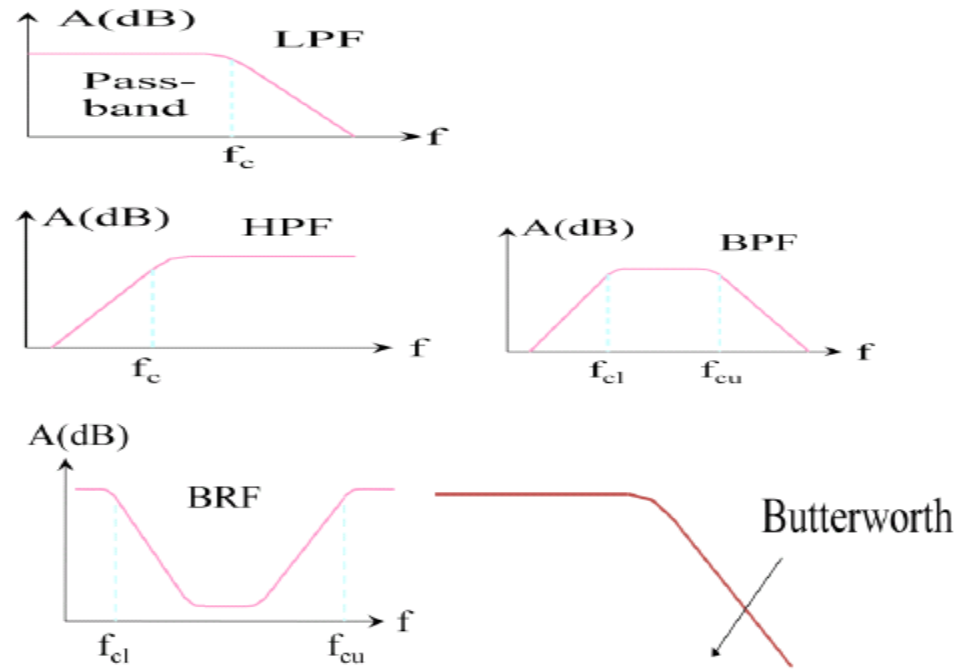
– Butterworth - maximally flat in passband; highly non-linear phase response with frequency

– Bessel - gentle roll-off; linear phase shift with freq.

– Chebyshev - steep initial roll-off with ripples in passband

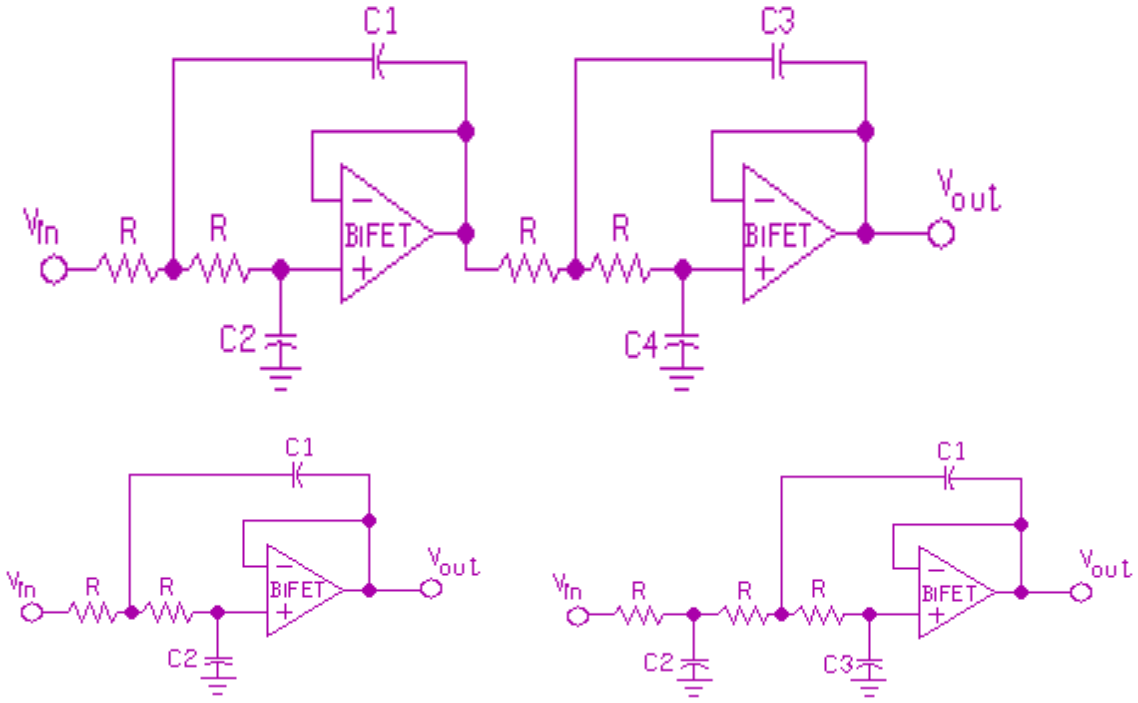
– Cauer (or elliptic) - steepest roll-off of the four types but has ripples in the passband and in the stop band

5.6 Frequency Response of Filters



Unity-Gain Low-Pass Filter Circuits

5.7 Unity-Gain Low-Pass Filter Circuits



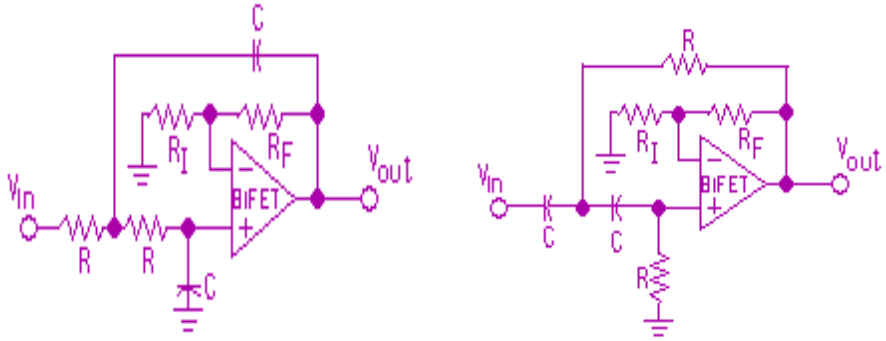
5.8 Design Procedure for Unity-Gain HPF

• The same procedure as for LP filters is used except for step #3, the normalized C value of 1 F is divided by K_f. Then pick a desired value for C, such as 0.001 mF to 0.1 mF, to calculate K_x. (Note that all capacitors have the same value).

• For step #6, multiply all normalized R values (from table) by K_x.

E.g. Design a unity-gain Butterworth HPF with a critical frequency of 1 kHz, and a roll-off of 55 dB/dec. (Ans.: C = 0.01 mF, R_1 = 4.49 kW, R_2 = 11.43 kW, R_3 = 78.64 kW.; pick standard values of 4.3 kW, 11 kW, and 75 kW).

5.9 Equal-Component Filter Design



Design an equal-component LPF with a critical frequency of 3 kHz and a roll-off of 20 dB/oct.

Minimum # of poles = 4

Choose C = 0.01 mF; ˆ R = 5.3 kW

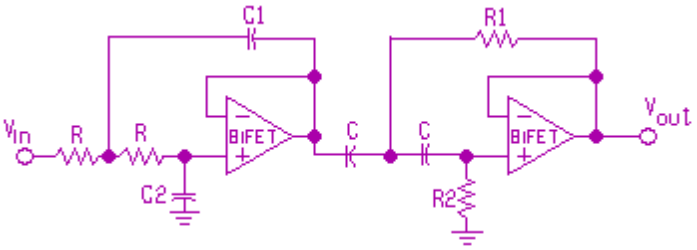
From table, A_{v1} = 1.1523, and A_{v2} = 2.2346.

Choose R_{I1} = R_{I2} = 10 kW; then R_{F1} = 1.5 kW, and R_{F2} = 12.3 kW .

Select standard values: 5.1 kW, 1.5 kW, and 12 kW**.**

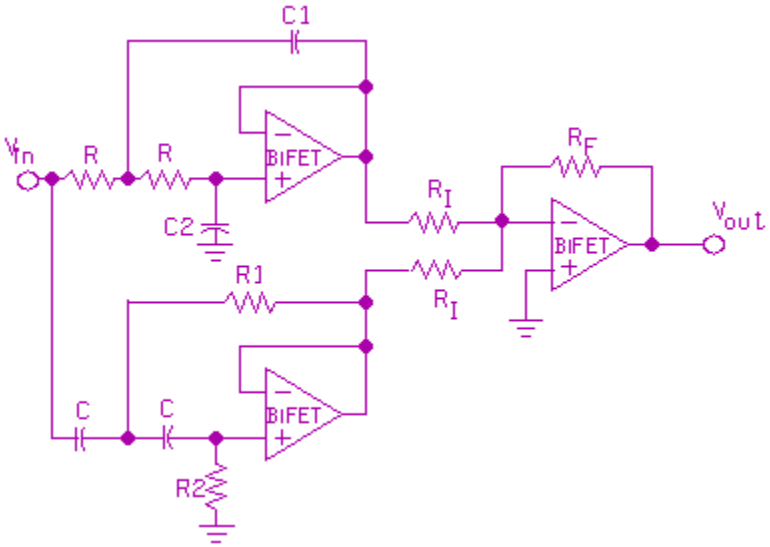
5.10 Bandpass and Band-Rejection Filter

5.10.1 A *broadband* BPF can be obtained by combining a LPF and a HPF

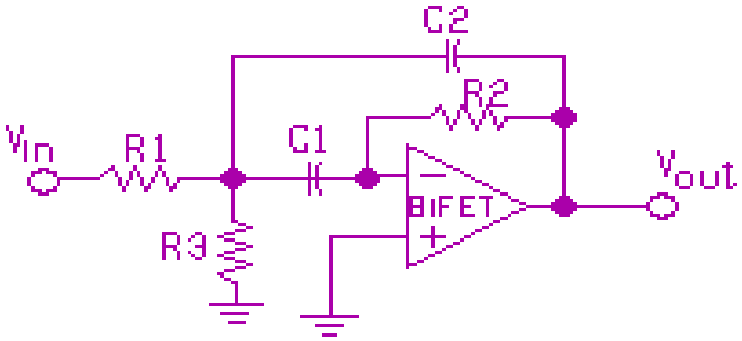


5.10.2 Broadband Band-Reject Filter

A LPF and a HPF can also be combined to give a broadband BRF

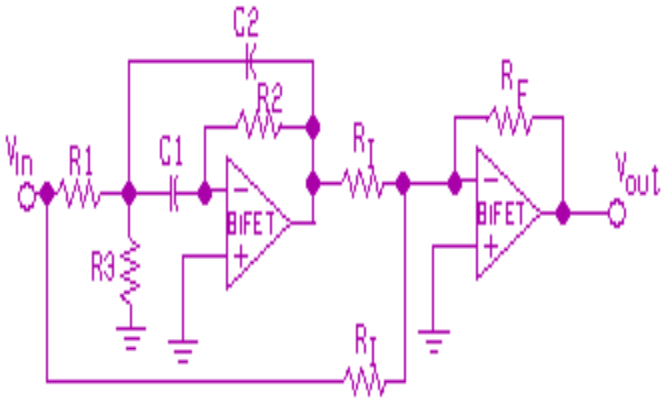


5.10.3 Narrow-band Bandpass Filter



5.10.4 Narrow-band Band-Reject Filter

Easily obtained by combining the inverting output of a narrow-band BRF and the original signal



The equations for R1, R2, R3, C1, and C2 are the same as before.

$R_I = R_F$ for unity gain and is often chosen to be >> R1.

5.11 Classification of ADCs

1. Direct type ADC.
2. Integrating type ADC

5.11.1 Direct type ADCs

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter.
4. Successive approximation type converter

5.11.2 Integrating type converters

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter

5.12 Sample and hold circuit

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems

5.12.1 Dual slope ADC:

Dual slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrator, and then measured by a counter. The speed of this conversion is slow but the accuracy is high

Advantages of dual slope ADC are

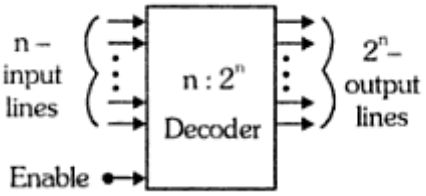
1. It is highly accurate
2. Its cost is low
3. It is immune to temperature caused variations in R1 and C1

UNIT VI

COMBINATIONAL LOGIC DESIGN

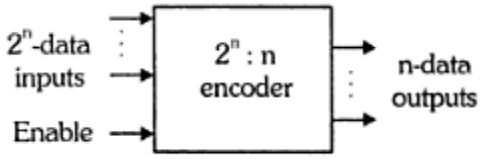
6.1 Decoder:

A decoder is a multiple-input and multiple output combinational logic circuit which converts coded input into coded output where the input and output codes are different. A decoder has n-input lines and 2^n output lines



6.2 Encoder:

An encoder is multiple input and multiple output combinational circuit it performs reverse operation of a decoder .An encoder has 2^n (or fewer) input lines and n output lines



6.3 Multiplexer:

Multiplexer is a digital switch. it allows digital information from several sources to be routed onto a single output line

6.3.1 Applications of multiplexer:

1. The logic function generator
2. Digital counter with multiplexed displays
3. Data selection and data routing
4. Parallel to serial conversion

6.4 Demutiplexers:

A demutiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines.

6.4.1 Applications of Demultiplexer:

1. Data distributor
2. Secuirity monitoring system
3. Synchronous data transmission system

6.5 Code converter

There is a wide variety of binary codes used in digital systems. Some of these codes are binary –coded-decimal (BCD), Excess-3, gray, and so on. Many times it is required to convert one code to another

6.6 Comparator

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers

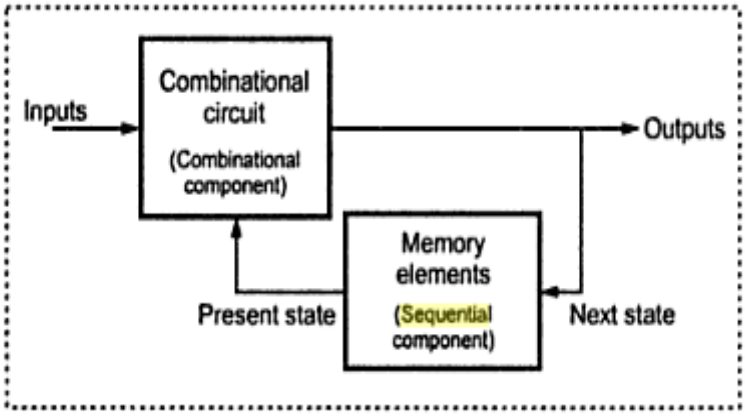
Adders & sub tractors, Ripple Adder, Binary Parallel Adder, Binary Adder-Subtractor**,** Combinational multipliers, ALU Design considerations of the above combinational logic circuits with relevant Digital ICs.

UNIT –VII

SEQUENTIAL LOGIC DESIGN

7.1 Sequential circuit:

The block diagram of sequential circuit is as shown in figure.a memory element is connected in the feedback of combinational circuit



Sequential circuit

Comparison of combinational circuits and sequential circuits

Sr. No.	Combinational circuits	Sequential circuits
1.	In combinational circuits, the output variables are at all times dependent on the combination of input variables.	In sequential circuits, the output variables dependent not only on the present input variables but they also depend upon the past history of these input variables.
2.	Memory unit is not required in combinational circuits.	Memory unit is required to store the past history of input variables in the sequential circuit.
3.	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits.
4.	Combinational circuits are easy to design.	Sequential circuits are comparatively harder to design.
5.	Parallel adder is a combinational circuit.	Serial adder is a sequential circuit.

Sequential circuits are again classified in to two types

1. Asynchronous sequential circuit
2. Synchronous sequential circuit

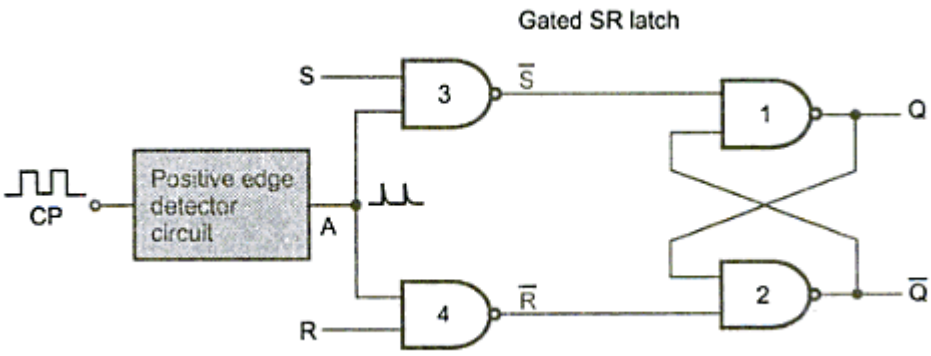
Comparison of synchronous sequential circuit and asynchronous sequential circuit

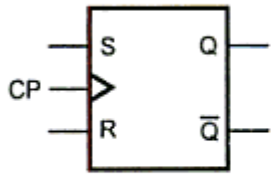
Sr. No.	Synchronous sequential circuits	Asynchronous sequential circuits
1.	In synchronous circuits, memory elements are clocked flip-flops.	In asynchronous circuits, memory elements are either unclocked flip-flops or time delay elements.
2.	In synchronous circuits, the change in input signals can affect memory element upon activation of clock signal.	In asynchronous circuits change in input signals can affect memory element at any instant of time.
3.	The maximum operating speed of clock depends on time delays involved.	Because of absence of clock, asynchronous circuits can operate faster than synchronous circuits.
4.	Easier to design.	More difficult to design.

7.2 Latches and Flip-flops:

Latches are *asynchronous*, which means that the output changes very soon after the input changes. Most computers today, on the other hand, are *synchronous*, which means that the outputs of all the sequential circuits change simultaneously to the rhythm of a global *clock signal*.

7.3 Clocked SR Flipflop:



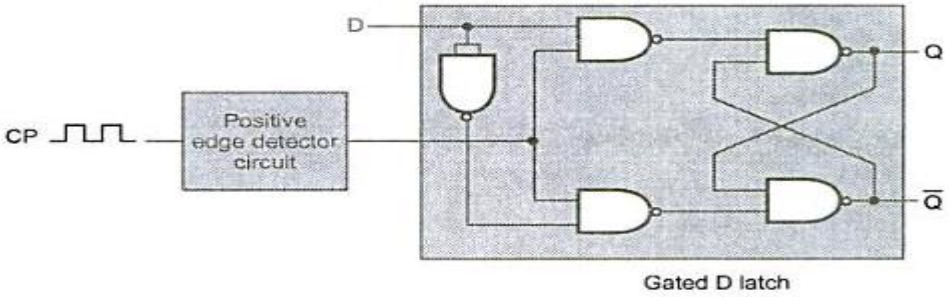


(a) Logic symbol

CP	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	No change(NC)
↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	X	Indeterminate
↑	1	1	1	X	
0	X	X	0	0	No change(NC)
0	X	X	1	1	

(b) Truth table for positive edge clocked SR flip-flop

7.4 Clocked Flip-flop:



Gated D latch

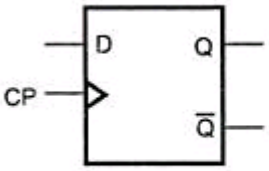


Fig. 6.21 (a) Logic symbol

CP	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	Q_n

Fig. 6.21 (b) Truth table of D flip-flop

7.5 JK Flip-Flop:

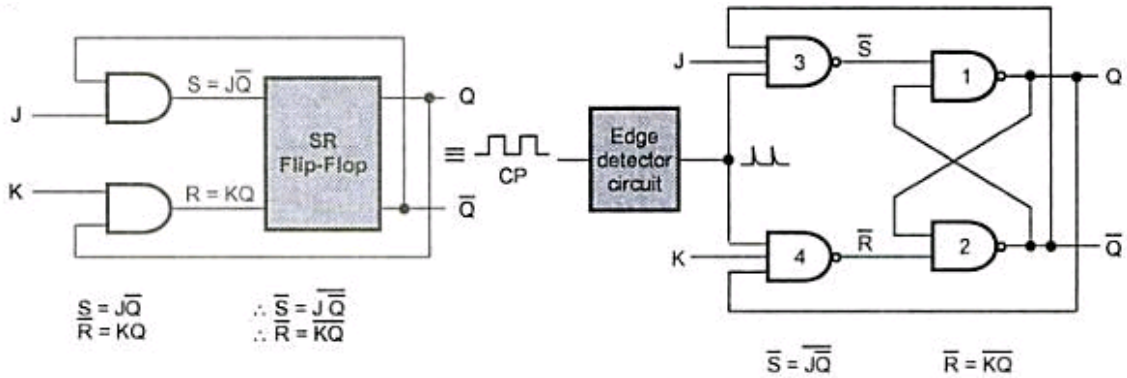


Fig. 6.27 JK Flip-flop using NAND gates

7.6 Shift register:

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. The movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to a group of registers called shift register

Applications of shift register:

1. Delay line
2. parallel to serial converter
3. Serial to parallel converter
4. Sequence generator
5. Shift register counters

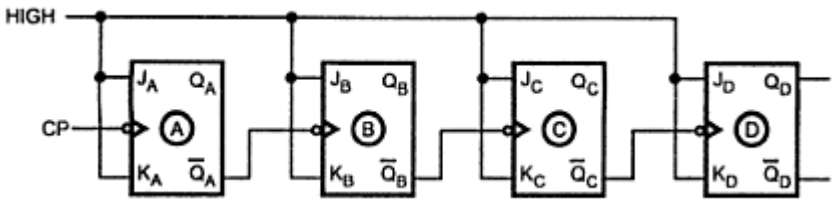
7.7 Counter

Counters are basically classified in to two types

1. Asynchronous counter
2. Synchronous counter

7.7.1 Asynchronous counter:

A 4-bit asynchronous counter is as shown in figure



Comparison between Asynchronous counter and Synchronous counter

Sr. No.	Asynchronous counters	Synchronous counters
1.	In this type of counter flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2.	All the flip-flops are not clocked simultaneously.	All the flip-flops are clocked simultaneously.
3.	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop.	As clock is simultaneously given to all flip-flops there is no problem of propagation delay. Hence they are high speed counters and are preferred when number of flip-flops increases in the given design.

7.8 Ring counter:

A ring counter is a Shift Register (a cascade connection of flip-flops) with the output of the last flip flop connected to the input of the first. It is initialised such that only one of the flip flop output is 1 while the remainder is 0. The 1 bit is circulated so the state repeats every n clock cycles if n flip-flops are used. The "MOD" or "MODULUS" of a counter is the number of unique states. The MOD of the n flip flop ring counter is n.

7.9 Johnson counter:

A Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first. The register cycles through a sequence of bit-patterns. The MOD of the Johnson counter is 2n if n flip-flops are used. The main advantage of the Johnson counter counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD.

UNIT –VIII

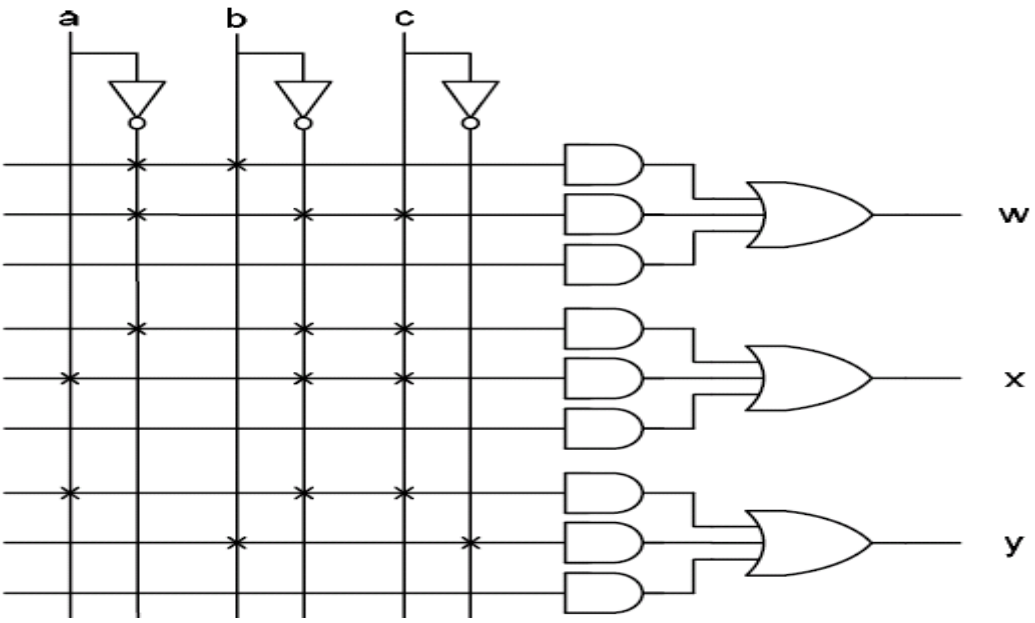
PROGRAMMABLE LOGIC DEVICES AND MEMORIES

8.1 PROM (Programmable Read Only Memory):

Programmable Read Only Memory has a fixed AND array (constructed as a decoder) and programmable connections for the output OR gates array. The PROM implements Boolean functions in sum-of-minterms form.

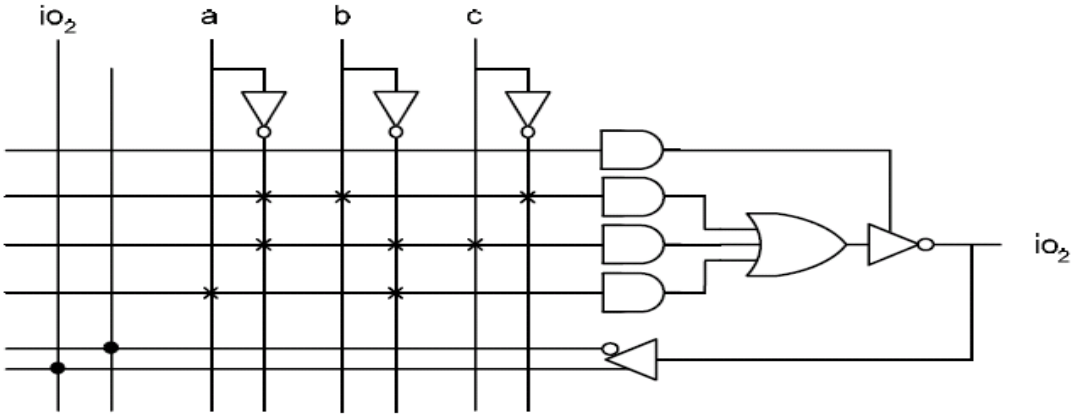
8.2 PAL (Programmable Array Logic):

Programmable Array Logic device has a programmable AND array and fixed connections for the OR array.



8.3 Three-State Outputs

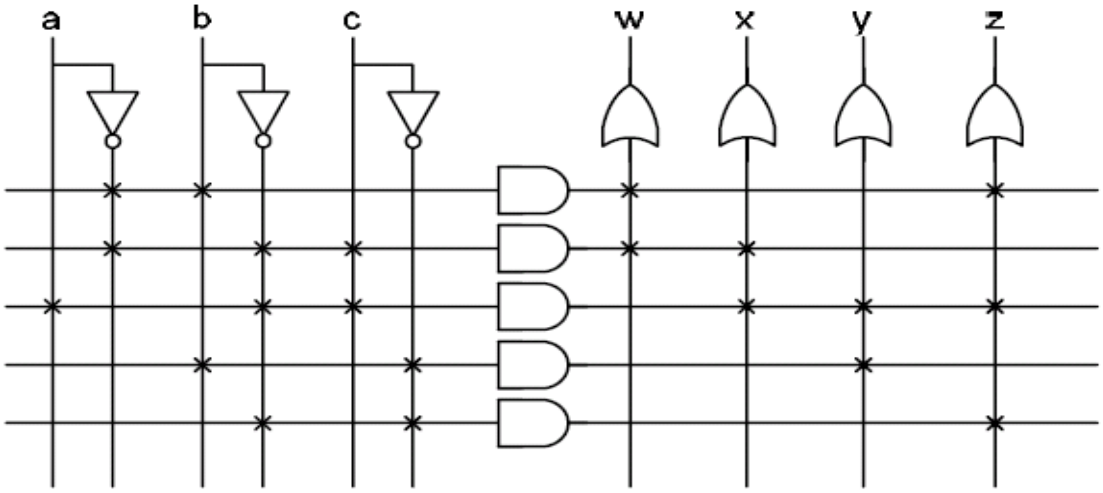
A further improvement to the original PAL structure of Figure is done by adding three-state controls to its outputs as shown in the partial structure of figure



PAL Structure with Three Output Control

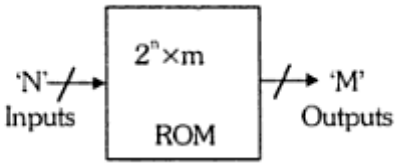
8.4 PLA (Programmable Logic Array) :

Programmable Logic Array has programmable connections for both AND and OR arrays. So it is the most flexible type of PLD.



8.5 Read only memory:

Rom is an abbreviation for read only memory. It is non-volatile memory i.e.it can hold data even if power is turned off. Generally, ROM is used to store the binary codes for the sequence of instructions



It consists of n input lines and m output lines. Each bit combination of the input variables is called on 'address'. Each bit combination that comes out of the output lines is called a 'word'

8.6 ROM Variations

The acronym, ROM is generic and applies to most read only memories. What is today implied by ROM may be ROM, PROM, EPROM, EEPROM or even flash memories. These variations are discussed here.

8.6.1 ROM. ROM is a mask-programmable integrated circuit, and is programmed by a mask in IC manufacturing process. The use of mask-programmable ROMs is only justified when a large volume is needed. The long wait time for manufacturing such circuits makes it a less attractive choice when time-tomarket is an issue.

8.6.2 PROM. Programmable ROM is a one-time programmable chip that, once programmed, cannot be erased or altered. In a PROM, all minterms in the AND-plane are generated, and connections of all AND-plane outputs to ORplane gate inputs are in place. By applying a high voltage, transistors in the

OR-plane that correspond to the minterms that are not needed for a certain output are burned out. a fresh PROM has all transistors in its OR-plane connected. When programmed, some will be fused

out permanently. Likewise, considering the diagram of Figure 4.8, an unprogrammed PROM has X's in all wire crossings in its OR-plane.

8.6.3 EPROM. An Erasable PROM is a PROM that once programmed, can be completely erased and reprogrammed. Transistors in the OR-plane of an EPROM have a normal gate and a floating gate . The non-floating gate is a normal NMOS transistor gate, and the floating-gate is surrounded by insulating material that allows an accumulated charge to remain on the gate for a long time.

When not programmed, or programmed as a '**1**', the floating gate has no extra charge on it and the transistor is controlled by the non-floating gate (access gate). To fuse-out a transistor, or program a '**0**' into a memory location, a high voltage is applied to the access gate of the transistor which causes accumulation of negative charge in the floating-gate area. This negative charge prevents logic **1** values on the access gate from turning on the transistor. The transistor, therefore, will act as an unconnected transistor for as long as the negative charge remains on its floating-gate.

To erase an EPROM it must be exposed to ultra-violate light for several minutes. In this case, the insulating materials in the floating-gates become conductive and these gates start loosing their negative charge. In this case, all transistors return to their normal mode of operation. This means that all EPROM memory contents become **1**, and ready to be reprogrammed. Writing data into an EPROM is generally about a 1000 times slower than reading from it. This is while not considering the time needed for erasing the entire EPROM.

8.6.4 EEPROM. An EEPROM is an EPROM that can electrically be erased, and hence the name: Electrically Erasable Programmable ROM. Instead of using ultraviolate to remove the charge on the non-floating gate of an EPROM transistor, a voltage is applied to the opposite end of the transistor gate to remove its accumulated negative charge. An EEPROM can be erased and reprogrammed without having to remove it. This is useful for reconfiguring a design, or saving system configurations. As in EPROMs, EEPROMs are non-volatile

memories. This means that they save their internal data while not powered. In order for memories to be electrically erasable, the insulating material surrounding the floating-gate must be much thinner than those of the EPROMS. This makes the number of times EEPROMs can be reprogrammed much less than that of EPROMs and in the order of 10 to 20,000. Writing into a byte of an EEPROM is about 500 times slower than reading from it.

8.6.5 Flash Memory. Flash memories are large EEPROMs that are partitioned into smaller fixed-size blocks that can independently be erased. Internal to a system, flash memories are used for saving system configurations. They are used in digital cameras for storing pictures. As external devices, they are used for temporary storage of data that can be rapidly retrieved. Various forms of ROM are available in various sizes and packages. The popular 27xxx series EPROMs come in packages that are organized as byte addressable memories. For example, the 27256 EPROM has 256K bits of memory that are arranged into 32K bytes.

8.7 Random Access memory:

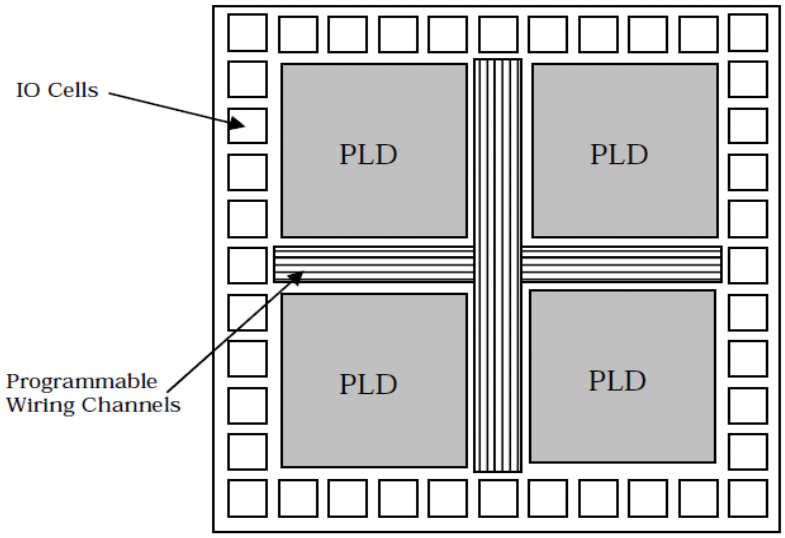
Unlike ROM, we can read from or write in to the RAM, so it is often called read/write memory. The numerical and character data that are to be processed by the computer change frequently. But it is a volatile memory, i.e. it cannot hold data when power is turned off

There are two types of RAMS

- Static RAM
- Dynamic RAM

8.8 Complex Programmable Logic Devices

The next step up in the evolution and complexity of programmable devices is the CPLD, or Complex PLD. Extending PLDs by making their AND-plane larger and having more macrocells in order to be able to implement larger and more complex logic circuits would face difficulties in speed and chip area utilization. Therefore, instead of simply making these structures larger, CPLDs are created that consist of multiple PLDs with programmable wiring channels between the PLDs. Figure shows the general block diagram of a CPLD.



8.9 FPGA

FPGAs (Field-Programmable Gate Arrays) are PLDs with large numbers of small macro-cells each of which can be interconnected to only a few neighboring cells. A typical FPGA might have 100 cells, each with only 8 inputs and 2 outputs. The output of each cell can be programmed to be an arbitrary function of its inputs. FPGAs typically have a large number ( ) of I/O pins.