10 Phase Locked Loop

10.1 INTRODUCTION

The phase locked loop, commonly called PLL, is a closed loop feedback system, whose output frequency and phase are in lock with the frequency and phase of the input signal. The PLL is an important building block of a linear system, which can detect the phases of two signals and reduce the difference in the presence of a phase difference. The realization of PLL had been very costly in most industrial and consumer applications. However, the evolution achieved in monolithic IC technology has made the fabrication of IC PLL inexpensive, and the use of PLL is constantly expanding in many applications such as satellite communication systems, FM demodulators, stereo demodulators, tone detectors and frequency synthesizers. This chapter discusses the operation and closed loop analysis of the PLL and the widely used monolithic IC 565. The generation of signals is a basic requirement for a number of commonly used applications. The voltage controlled oscillator (VCO) forms an integral part of the PLL. The commonly used VCO IC 566, and important applications of IC NE/SE565 are also discussed.

10.2 OPERATION OF THE BASIC PLL

The basic block diagram of a phase locked loop is shown in Fig.10.1. The main elements of the PLL are a phase detector/comparator, a low-pass filter, an error amplifier (A) and a voltage controlled oscillator (VCO). The phase detector is fundamentally a multiplier, which generates the sum and difference of the two input signals.

The free running frequency f_o of the VCO is determined by an externally connected resistor and a timing capacitor. When the loop is locked, the frequency f_o is directly proportional to an externally applied voltage v_c, called the *dc control voltage*. When an input periodic signal v_i of frequency f_i and VCO output signal v_o of frequency f_o are applied to the PLL, the phase detector produces a dc or low frequency signal v_d which is proportional to the phase difference between the input signal v_i and the VCO output signal v_o.

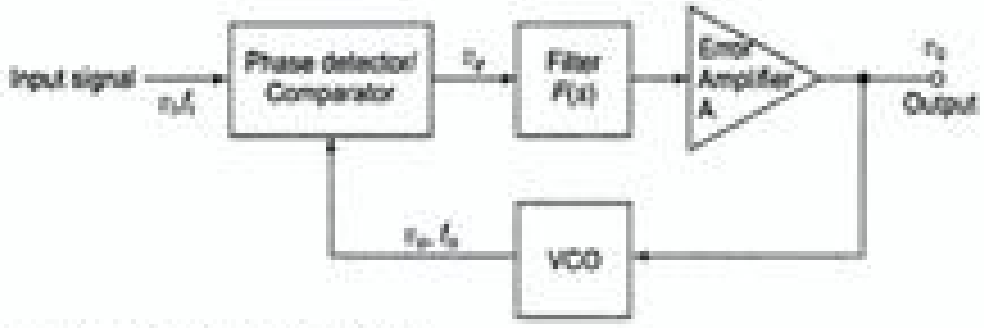

Fig. 10.1 *Basic block diagram of PLL*

When the phase sensitive signal from the phase detector is passed through the low-pass filter $F(s)$, the high frequency sum component is filtered out. The low frequency difference component passes out of the filter and then amplified by the error amplifier A. This amplified signal is applied to the input of VCO as control voltage v_c, which changes the VCO frequency f_o in such a way that the difference between f_o and f_i is reduced. If the two frequencies are brought almost identical by this feedback action, then the circuit is said to be *locked*. Once the lock is achieved, the VCO frequency f_o becomes equal to the input signal frequency f_i with a finite phase difference ϕ.

Process of Capture It is an important aspect of PLL, by which the loop achieves the condition of being *in-lock* with a signal from a free-running and unlocked condition. In the unlocked condition of the PLL, the VCO operates at a frequency f_c, called *center frequency* or *free running frequency*. This corresponds to an applied voltage of 0V dc at its control input. The capture process is inherently non-linear and starts occurring as described below.

Let us assume that the feedback loop of the PLL is initially open between the loop-filter and VCO control input. An input signal of frequency f_i, which is assumed to be closer to the VCO center frequency, f_c is applied to the input of the phase detector. The phase detector is usually an analog multiplier that multiplies the two sinusoids together, and it produces the sum and difference of the two signals at its output. Since the high frequency sum component is filtered out by the low-pass filter, the output of the LPF is a sinusoid, whose frequency is equal to the difference between the VCO center frequency f_c and incoming signal frequency f_i.

Considering that the loop is suddenly closed, the difference frequency sinusoid is applied to the VCO input as the control voltage, v_c. Thus this will make the VCO frequency f_o, a sinusoidal function of time. Therefore, it alternately moves closer and farther away from f_i. The output frequency of the phase detector, being the difference between f_o and f_i, moves to a higher frequency when f_o moves away from f_i, and moves to a lower frequency when f_o moves closer to f_i. This fact is reflected in the phase detector output having an asymmetrical wave shape during the capture process as shown in Fig. 10.2. This asymmetry in the waveform produces a dc component in the phase detector output. This dc component shifts the VCO frequency f_o towards f_i

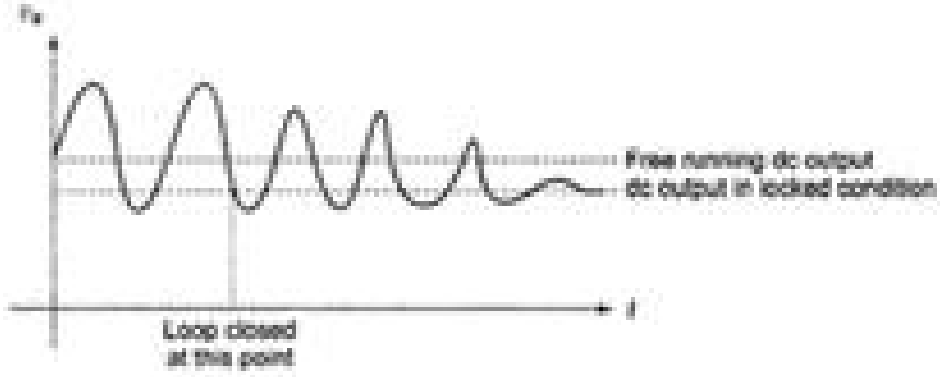

Fig. 10.2 *Output of phase detector during capture process*

and the frequency difference gradually diminishes. When the loop is locked, the frequency difference becomes zero, and a dc voltage remains at the loop-filter output.

The low-pass loop-filter filters out the difference frequency components resulting from interfering signals, which are far away from the center frequency. It also acts as a memory for the loop, when the lock is momentarily lost due to a large interfering transient signal. Therefore, the capture-range and pull-in time are dependent on the amount of gain in the loop and the bandwidth of the filter. The signal will be out of capture range when the beat frequency is too high due to the VCO frequency which is far away from the center frequency. Once lock is achieved, the VCO can track the signal well beyond the capture-range. Reducing the bandwidth of the filter thus improves the *rejectivity* of out-of-band signals, but it reduces the capture range; the pull-in time increases and loop phase margin become less.

The capture range of a PLL is defined as the range of input frequencies around the center frequency within which the loop can get locked from an unlocked condition. *The pull-in time* is the total time required for the loop to get captured with the input signal.

An important feature of PLL is its ability to suppress the noise such as those superimposed on the input signal and the noise generated by the VCO.

10.3 CLOSED LOOP ANALYSIS OF PLL

To study the closed loop analysis of PLL, a more detailed block diagram is used as shown in Fig. 10.3.

Assume that the PLL is initially in locked condition. Also assume that the gain of the phase detector is K_d Volt/rad of phase difference, the transfer function of the loop-filter is $F(s)$ and the gain in the forward loop is A.

The input sinusoidal signal v_i is represented by

$$v_i = V_p \sin(\omega t + \theta_i) \tag{10.1}$$

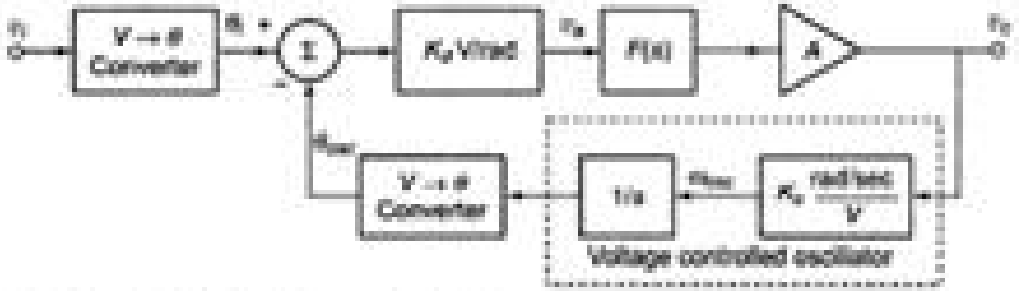

Fig. 10.3 *Detailed block diagram of PLL*

If the phase shift of the signal at the VCO output is θ_{OSC}, then the average value of the output of the phase detector is

$$v_d = K_d(\theta_i - \theta_{OSC}) \tag{10.2}$$

where θ_i and θ_{OSC} are phase shifts with respect to an arbitrarily assumed reference. The phase of the signal at the output of VCO as a function of time is

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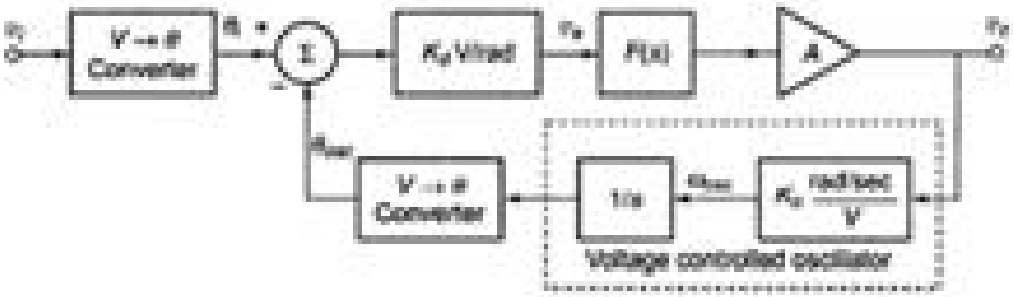

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where θ_i and θ_{OSC} are phase shifts with respect to an arbitrarily assumed reference. The phase of the signal at the output of VCO as a function of time is equal to the integral of the VCO output frequency, and it can be expressed as

$$\omega_{OSC}(t) = \frac{d\theta_{OSC}(t)}{dt}$$

Thus,
$$\theta_{OSC}(t) = \int_0^t \omega_{OSC}(t)\,dt + \theta_{OSC}|_{t=0}$$

Therefore, the integral component is represented as 1/s inside the VCO block of Fig.10.3. The oscillator frequency ω_{OSC} and the dc control voltage v_c are actually related by

$$\omega_{OSC} = \omega_c + K_o v_c \tag{10.3}$$

where ω_c is the *center* or *free-running angular frequency* that results when v_c = 0 and K_o is the VCO gain in rad/s per volt. Then the closed-loop transfer function of the PLL becomes

$$\frac{V_c(s)}{\theta_i(s)} = \frac{K_d F(s) A}{1 + K_d A F(s)\frac{K_o}{s}}$$

$$= \frac{s K_d F(s) A}{s + K_d K_o A F(s)} \tag{10.4}$$

To study the response of the loop to *frequency* variations at the input rather than *phase*, the above equation can be represented as

$$\frac{V_c(s)}{\omega_i(s)} = \frac{V_c(s)}{s\theta_i(s)} = \frac{K_d F(s) A}{s + K_d K_o A F(s)} \tag{10.5}$$

since $\omega_i = d\theta_i/dt$ and $\omega_i(s) = s\theta_i(s)$.

Considering $F(s) = 1$ with the loop having a first order low-pass frequency response, we have

$$\frac{V_c(s)}{\omega_i(s)} = \frac{K_v}{s + K_v} \approx \frac{1}{K_o} \tag{10.6}$$

where K_v, the *loop bandwidth* is given by $K_v = K_o K_d A$. Then the loop bandwidth K_v is the effective bandwidth, and the loop and capture ranges are very much dependent on K_v. If K_v decreases, the capture time rises, and the capture-range reduces. Therefore, the property of interference rejection improves.

Second order PLL The first order loop without loop-filter has several limitations such as

(i) both the sum and difference frequency components are fed to the output from the phase detector and

(ii) all *out-of-band* interfering signals from the input will appear shifted in frequency at the output.

Therefore, a loop-filter is highly desirable in applications where interfering signals are present. The most common configuration of monolithic PLL is the second-order loop with a loop-filter $F(s)$ of a simple single-pole, low-pass filter

realized with a resistor R and a capacitor C as shown in Fig.10.4.

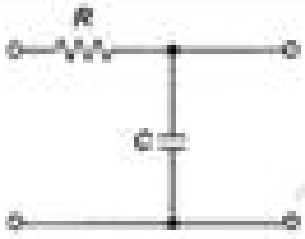

Fig. 10.4 *Single-pole loop-filter (lag filter)*

Then, $$F(s) = \frac{1}{1+s/\omega} = \frac{1}{1+s\tau} \qquad (10.7)$$

where $$\omega = \frac{1}{RC} = \frac{1}{\tau}.$$

The resulting block diagram of the second order PLL using single-pole loop-filter is shown in Fig. 10.5. The various dynamic performance requirements of PLL are achieved by the use of different types of filters.

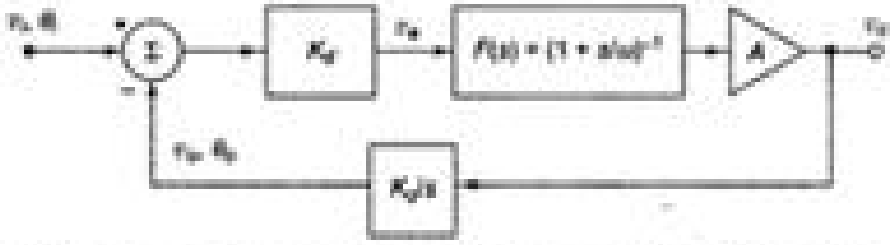

Fig. 10.5 *Block diagram of second order PLL using single-pole loop filter*

Loop lock-range and capture-range The loop *lock-range* is represented as the range of frequencies about ω_i for which the PLL maintains the relationship $\omega_i = \omega_{OSC}$. If the phase detector can determine the phase difference between θ_i and θ_{OSC} over a $\pm\pi/2$ range, then the lock-range is defined as

$$\begin{aligned}\omega_L &= \pm\Delta\omega_{OSC} \\ &= K_d A K_v (\pm\pi/2) \\ &= \pm K_v (\pi/2).\end{aligned} \qquad (10.8)$$

The *capture-range* is the range of input frequencies within which an initially unlocked loop will get locked with an input signal. When $F(s) = 1$, the capture-range equals the lock-range. If $F(s) = \frac{1}{(1+s/\omega_c)}$, then the capture-range is smaller than the lock-range. The lock-range and capture-range for such a loop are shown in Fig. 10.6

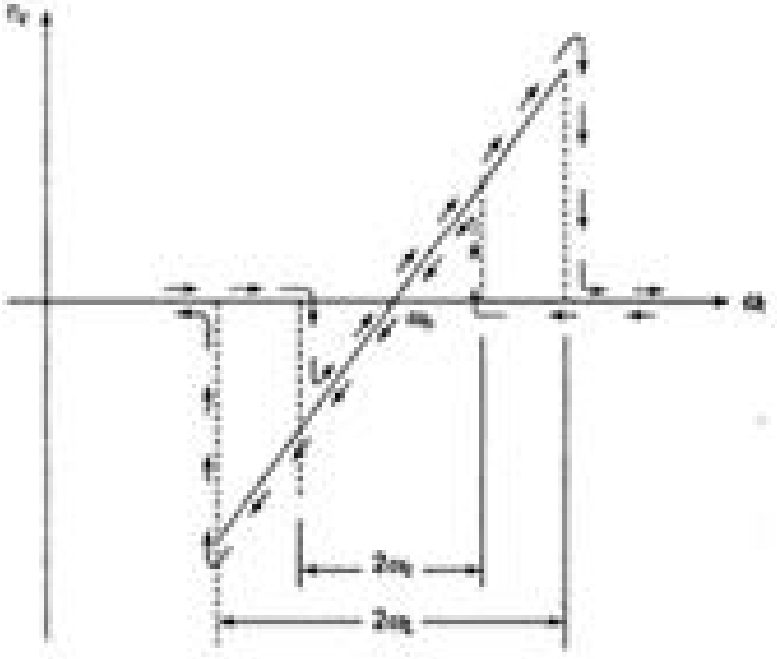

Fig. 10.6 *Lock and capture processes of PLL*

10.4 INTEGRATED CIRCUIT PHASE-LOCKED LOOP

The main reason that the PLL has been widely used as an integrated system component is its feasibility of getting fabricated on a single chip for all the individual PLL components. The component blocks of PLL are discussed in this section.

10.4.1 Phase Detector/Phase Comparator

There are two types of phase detectors namely (i) analog phase detector and (ii) digital phase detector.

Analog phase detector The analog phase detector realized by using an electronic switch is shown in Fig.10.7 (a) and (b). Assuming that the signal from VCO operates the electronic switch, the input sinusoid v_i is chopped by the VCO frequency. The input sinusoid and the VCO output square wave produce different values of filtered error voltages with respect to various values of phase error v_e, which is shown as cross-hatched area in the waveform of Fig 10.7(b). The output of the phase detector when passed through the filter gives out an average error signal shown as dotted line.

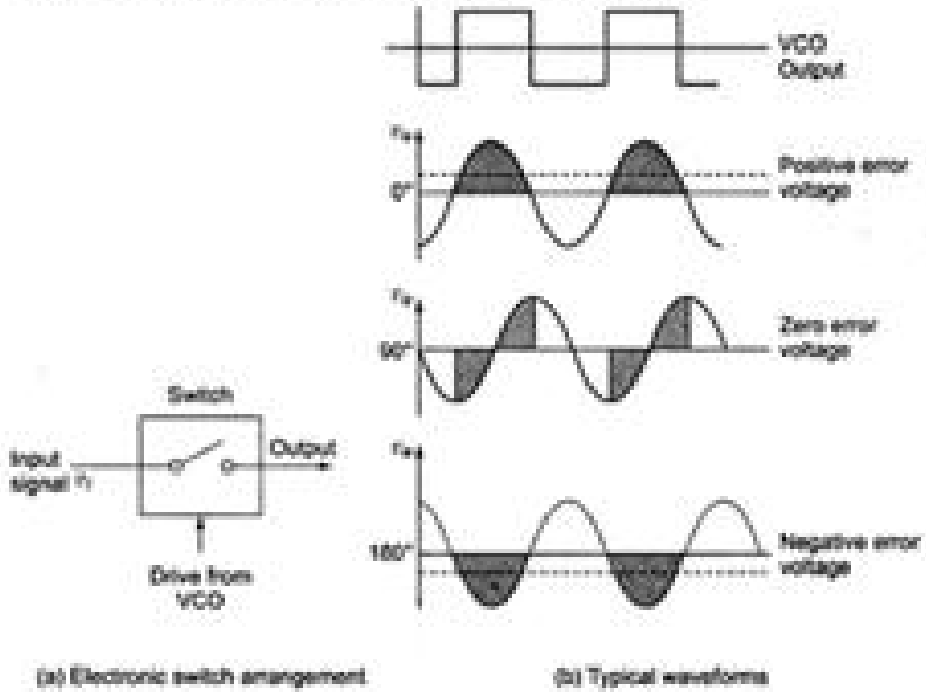

Fig. 10.7 *Analog phase detector using electronic switch*

The error voltage is zero when the phase difference between the two inputs equals 90°; the error voltage is positive for a phase difference of 0° and negative for a phase difference of 180°. In a PLL system configured by this type of phase detector, the PLL achieves a perfect lock when VCO output is in phase quadrature or 90° out of phase with the input.

Considering the input signal $v_i = V_i \sin \omega_i t$ and VCO output

$$v_o = V_o \sin (\omega_o t + \phi),$$

the phase detector output v_e becomes

$$v_e' = K v_i v_o = K V_i V_o \sin(\omega_i t)\sin(\omega_o t + \phi)$$

where K is the gain of the phase comparator and ϕ is the phase difference between input signal v_i and VCO output v_o. Then,

$$v_e = \frac{KV_iV_o}{2}[\cos(\omega_i t - \omega_o t - \phi) - \cos(\omega_i t + \omega_o t + \phi)].$$

When locked, $\omega_i = \omega_o$. Hence,

$$v_e = \frac{KV_iV_o}{2}[\cos(-\phi) - \cos(2\omega_o t + \phi)] \qquad (10.9)$$

The double frequency term is eliminated by low-pass filter and the dc error voltage is due to the term $\cos\phi$. It can be observed that when $\phi = 90°$, perfect lock is achieved and hence the error voltage $v_e = 0$. From the above equation, it is clear that the output error voltage v_e is dependent on

(i) the input signal amplitude V_i, which makes the phase detector gain and loop gain also dependent on V_i and
(ii) $\cos\phi$, that makes the response non-linear.

Analog phase detector using Gilbert multiplier cell The problem of non-linearity is eliminated in the Gilbert multiplier circuit shown in Fig.10.8(a). The input signal v_i is applied to the differential pair $Q_1 - Q_2$. The VCO output v_o is connected to the pairs $Q_3 - Q_4$ and $Q_5 - Q_6$ which act as Single-Pole Double-Throw (SPDT) switches. It is assumed that both the phase detector inputs v_i and v_o have large amplitudes and that all the transistors behave like switches.

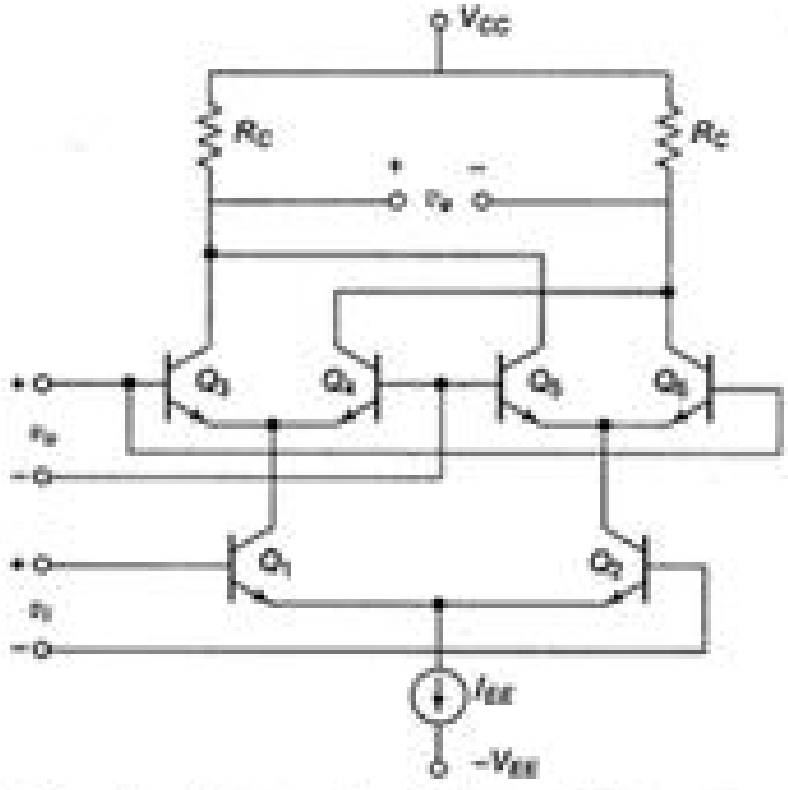

Fig.10.8 *(a) Analog phase detector using Gilbert multiplier cell*

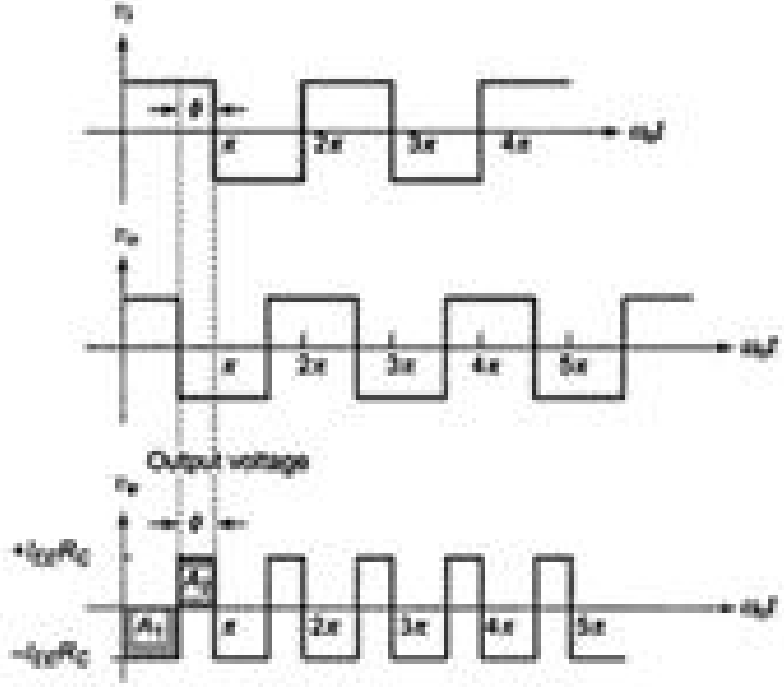

Fig. 10.8 *(b) Typical input and output waveforms of the analog phase detector*

The typical input and output waveforms of the analog phase detector using Gilbert multiplier cell is shown in Fig. 10.8 (b). During the interval from 0 to $(\pi - \phi)$, both v_1 and v_2 are high. Then, the transistors Q_3 and Q_3 are ON and current I_{EE} flows through Q_3 and Q_1 providing an output voltage $v_y = -I_{EE} R_C$. During the period from $(\pi - \phi)$ to π, when v_1 is HIGH and v_2 is LOW, transistors Q_1 and Q_4 are ON resulting in an output voltage, $v_y = I_{EE} R_C$ as shown in the waveform of Fig.10.8(c).

The average value or the dc component found from the area A_1 and A_2 of the waveform of v_y is given by

$$v_y = -\frac{1}{\pi}[A_1 - A_2]$$

$$= -\left[\frac{I_{EE} R_C (\pi - \phi)}{\pi} - \frac{I_{EE} R_C \phi}{\pi}\right]$$

$$= I_{EE} R_C \left(\frac{2\phi}{\pi} - 1\right)$$

$$= \frac{2I_{EE} R_C}{\pi}\left(\phi - \frac{\pi}{2}\right)$$

$$= K_\phi \left(\phi - \frac{\pi}{2}\right) \qquad (10.10)$$

where the *phase-angle to voltage* conversion ratio $K_\phi = \frac{2I_{EE} R_C}{\pi}$. The linear relationship between v_y and ϕ is shown in Fig. 10.8(c).

A 0.001 μF capacitor is connected between pins 7 and 8 to avoid oscillations due to parasitic effects. The *free running* or *center frequency* of VCO is

$$f_o = \frac{1.2}{4R_1C_1} \tag{10.19}$$

where R_1 and C_1 are external resistor connected to pin 8 and external capacitor connected to pin 9 respectively as shown in Fig. 10.15(b).

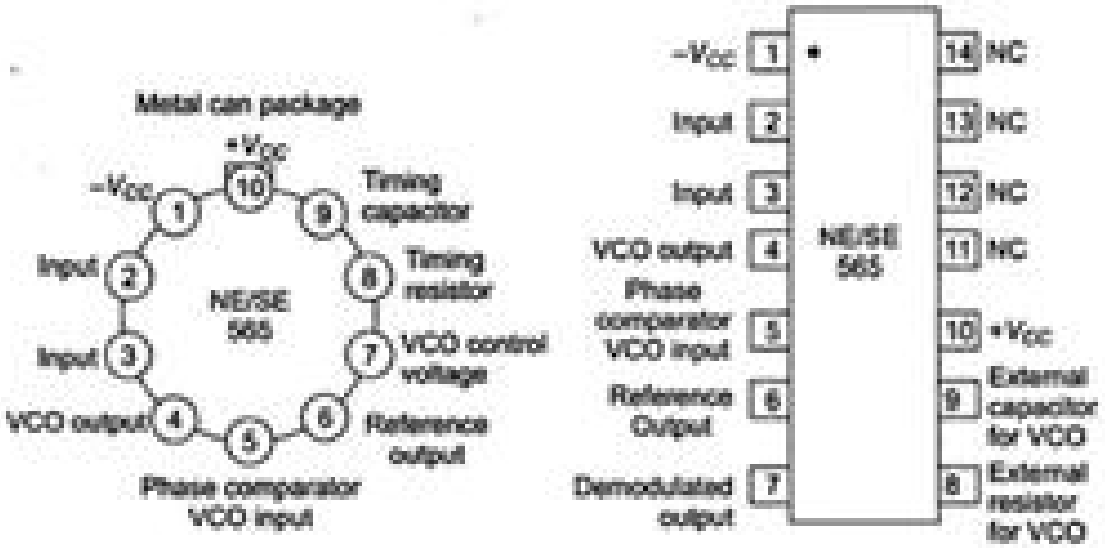

Fig. 10.15 *NE/SE565 PLL (a) 10 pin and 14 pin diagrams*

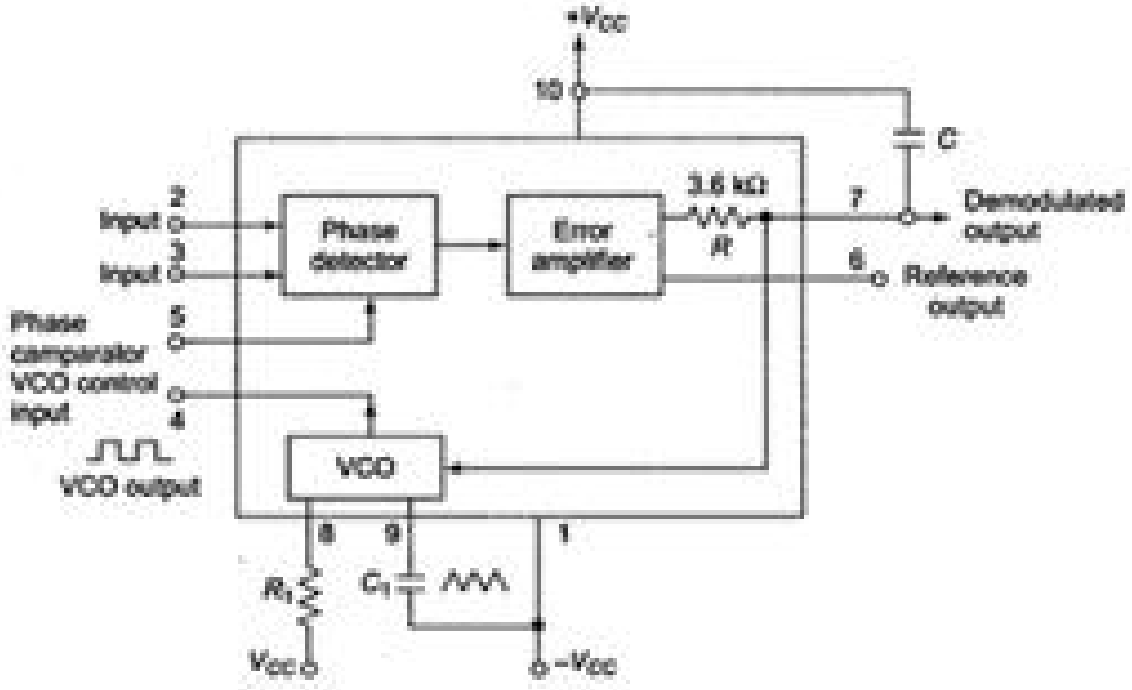

Fig. 10.15 *(b) Block diagram of IC LM565*

The values of R_1 and C_1 determine the center frequency of VCO. The value of R_1 is chosen between 2kΩ and 20kΩ. The device can achieve lock with an

input signal over ± 60% of bandwidth with respect to the center frequency. Pins 2 and 3 form the two input terminals of IC565. The input signal can also be direct-coupled without any dc voltage difference between the pins, and the dc resistances seen from pins 2 and 3 being equal.

Derivation of lock-in range Assume ϕ radians is the phase difference between the input signal and the VCO voltage. Then the output voltage v_c of the analog phase detector is given by

$$v_c = K_d\left(\phi - \frac{\pi}{2}\right) \tag{10.20}$$

where K_d is the *phase angle-to-voltage transfer coefficient* of the phase detector. Therefore, the control voltage to VCO is

$$v_c = AK_d\left(\phi - \frac{\pi}{2}\right) \tag{10.21}$$

where A is the voltage gain of the amplifier. This control voltage v_c shifts VCO frequency from its free running frequency f_o to a frequency f represented by

$$f = f_o + K_o v_c$$

where K_o is the *voltage to frequency transfer coefficient* of the VCO.

When PLL achieves *lock* with signal frequency f_i, we have

$$f = f_i = f_o + K_o v_c \tag{10.22}$$

From Eqs. (10.21) and (10.22) we get

$$v_c = \frac{(f_i - f_o)}{K_o} = AK_d\left(\phi - \frac{\pi}{2}\right) \tag{10.23}$$

Therefore,

$$\phi = \frac{\pi}{2} + \frac{(f_i - f_o)}{K_o K_d A} \tag{10.24}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian as shown in Fig.10.16 and $v_{c(max)} = \pm K_d \frac{\pi}{2}$ from Eq. (10.10). Then, the corresponding value of the maximum control voltage available to drive the VCO is given by

$$v_{c(max)} = \pm\left(\frac{\pi}{2}\right) K_d A \tag{10.25}$$

The maximum VCO swing in frequency that can be achieved is given by

$$(f - f_o)_{max} = K_o v_{c(max)} = K_d K_o A\left(\frac{\pi}{2}\right) \tag{10.26}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be

$$f_i = f_o \pm (f - f_o)_{max}$$

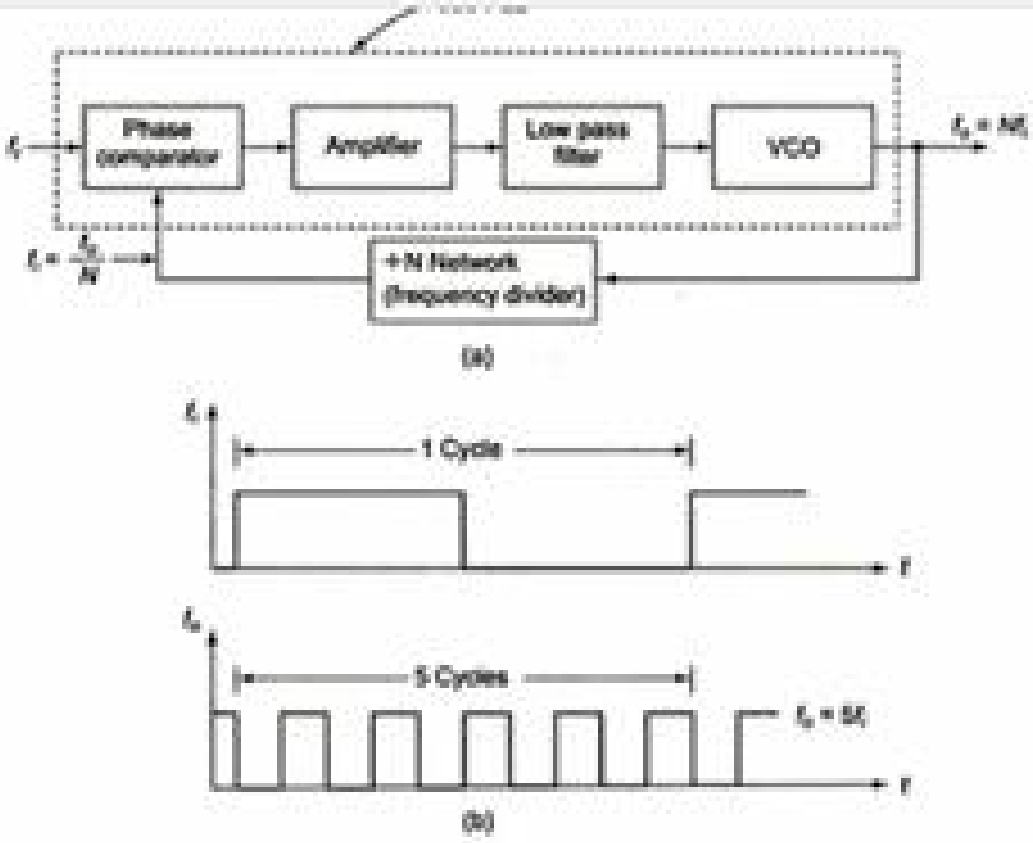

Fig. 10.17 *Frequency multiplier using IC 565 (a) Block connection diagram and (b) Input and output waveforms*

The frequency multiplication can also be obtained by operating the PLL in harmonic locking mode for input signals, which are rich in harmonics such as a square-wave. Then, the VCO can get directly locked-on to the *n*th harmonic of the input signal without the use of a frequency divider network. The value of *n* is normally limited to 10 since the amplitude of higher order harmonics decreases as the order increases. Therefore, effective locking may become difficult to achieve.

The circuit shown in Fig.10.17(a) can also be used for frequency division by locking the *m*th harmonic of the square-wave output of VCO with the input signal. Then the output of VCO is given by $f_o = \frac{f_i}{m}$. Figure 10.17(b) shows the output waveform of the frequency divider *for divide-by-5* circuit.

Example 10.7 A PLL IC 565 connected as an FM demodulator has $R_1 = 10k\Omega$, $C_1 = 0.01\mu F$ and $C = 0.04\mu F$. The supply voltage is +12V. Determine the (a) Free-running frequency, (b) Lock-range and (c) Capture-range.

Solution

The *free running* or *center frequency* of VCO is

$$f_o = \frac{1.2}{4R_1C_1} = \frac{1.2}{4 \times 10 \times 10^3 \times 0.01 \times 10^{-6}} = 300\text{kHz}$$

The lock range is given by

$\Delta f_L = \pm 7.8 f_o / V = 7.8 \times 300 \times 10^3 / 12 = 195\text{kHz}$

The capture range is given by

$$\Delta f_C = \pm\left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3)C}\right]^{\frac{1}{2}} = \left[\frac{195\times10^3}{(2\pi)(3.6)(10^3)(4\times10^{-9})}\right]^{\frac{1}{2}}$$

$$= 14.68\text{kHz}$$

10.9.2 AM Detection

The PLL can be used as an AM detector for demodulating the amplitude-modulated signals. Assume the AM signal is given by

$$v_m(t) = V_p[1+m(t)]\sin\omega_c t \tag{10.40}$$

The signal $v_m(t)$ can be demodulated by multiplying the signal with a local oscillator signal of the same carrier frequency f_c, as shown in Fig. 10.18.

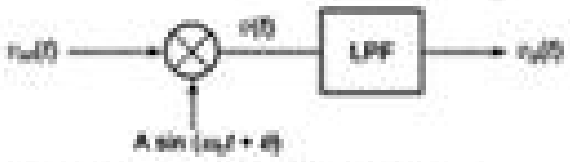

Fig. 10.18 *Simple AM detector*

Then the multiplier output is given by

$$V(t) = AV_p\left[1+m(t)\sin\omega_c t\sin(\omega_c t+\theta)\right]$$

$$= AV_p\left[1+m(t)\right]\frac{\cos\theta-\cos(2\omega_c t+\theta)}{2}$$

The high-frequency second term can be removed by a low-pass filter, and hence the filter output becomes

$$v_o(t) = V\left[1+m(t)\cos\theta\right] \tag{10.41}$$

where $V = AV_p$. This application can be implemented using the PLL as shown in Fig.10.19. Here the local oscillator signal generated in the PLL is phase-locked with the input signal.

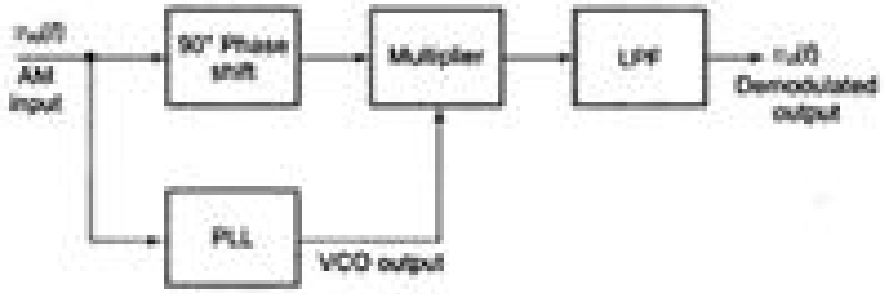

Fig. 10.19 *AM detector using PLL*

The PLL is locked to the carrier frequency of amplitude-modulated signal. The VCO output of the PLL, which has the same frequency value as the carrier, but unmodulated, is applied as one input to the multiplier. It is to be recalled that under locked condition, the VCO output signal of PLL is 90° out of phase with the input signal. Hence, the AM input signal is phase-shifted by 90° before being applied to the multiplier. The two signals applied to the multiplier, namely, the amplitude-modulated signal and the carrier signal generated in the PLL are

10.9.4 FSK Modulation / Demodulation

The Frequency Shift Keying (FSK) is a type of frequency modulation, in which the binary data or code is transmitted by means of a carrier frequency that is shifted between two fixed frequency values, namely, f_1 representing logic 0 and f_2 representing logic 1. The frequencies corresponding to logic 1 and logic 0 are called *mark* and *space* respectively.

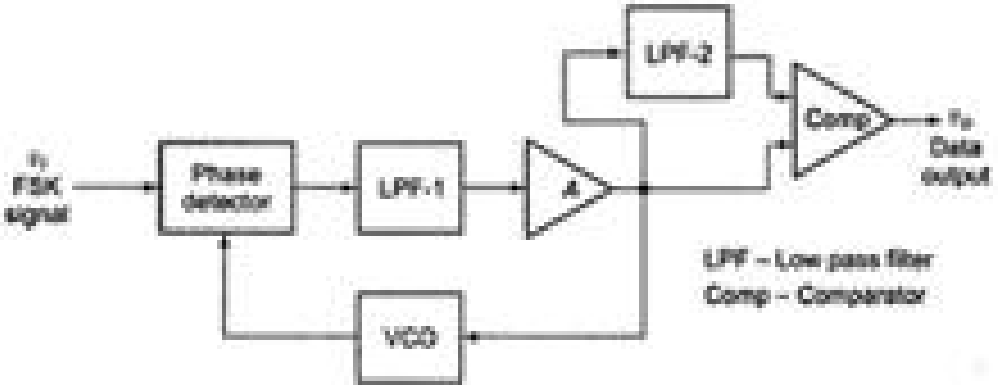

Fig. 10.21 *FSK demodulator using PLL*

The block diagram of Fig.10.21 shows the schematic arrangement for FSK demodulation using PLL. The PLL is designed to remain in-lock with the FSK signal for both the frequencies f_1 and f_2. Then the VCO control voltage fed to the comparator is given by

$$V_{f1} = \frac{f_1 - f_c}{K_v} \tag{10.44}$$

and

$$V_{f2} = \frac{f_2 - f_c}{K_v} \tag{10.45}$$

The difference between the two control voltage levels is

$$\Delta V_f = \frac{f_2 - f_1}{K_v} \tag{10.46}$$

Two inputs V_{f1} and V_{f2} are applied to the comparator. One of the inputs passes through a second low-pass filter (LPF-2). The filter is designed for a time constant which is longer than the FSK pulse duration to obtain a dc voltage. This dc voltage will have a value midway between V_{f1} and V_{f2}.

When the FSK signal v_i is applied to the input, the loop gets locked to the input frequency and tracks it in between the two frequencies f_1 and f_2. The corresponding dc shift at the output is made *logic* compatible by adjusting the saturation voltages of the voltage comparator.

A typical and simple circuit diagram for FSK generation and FSK demodulation is shown in Fig.10.22. The FSK generation is done by an IC 555 timer operated in astable mode, whose frequency at the output is controlled by ON/OFF state of transistor Q_1. The transistor Q_1 in turn is switched ON by the input digital data applied at its base.