Integrated Circuit:

It is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.

Classification:

1. Based on mode of operation

a. Digital IC's
b. Linear IC's

Digital IC's: Digital IC's are complete functioning logic networks that are equivalents of basic transistor logic circuits.

Ex:- gates ,counters, multiplexers, demultiplexers, shift registers.

Linear IC's: Linear IC's are equivalents of discrete transistor networks, such as amplifiers, filters, frequency multipliers, and modulators that often require additional external components for satisfactory operation.

Note: Of all presently available linear ICs, the majority are operational amplifiers.

2. Based on fabrication

a. Monolithic IC's
b. Hybrid IC's

a. Monolithic IC's : In monolithic ICs all components (active and passive) are formed simultaneously by a diffusion process. Then a metallization process is used in interconnecting these components to form the desired circuit.

b. Hybrid IC's: In *hybrid ICs,* passive components (such as resistors and capacitors) and the interconnections between them are formed on an insulating substrate. The substrate is used as a chassis for the integrated components. Active components such as transistors and diodes as well as monolithic integrated circuits, are then connected to form a complete circuit.

3. Based on number of components integrated on IC's

a. SSI <10 components
b. MSI <100 components
c. LSI >100 components
d. VLSI >1000 components

Integrated circuit Package types:

1. The flat pack
2. The metal can or transistor pack
3. The dual in line package or DIP

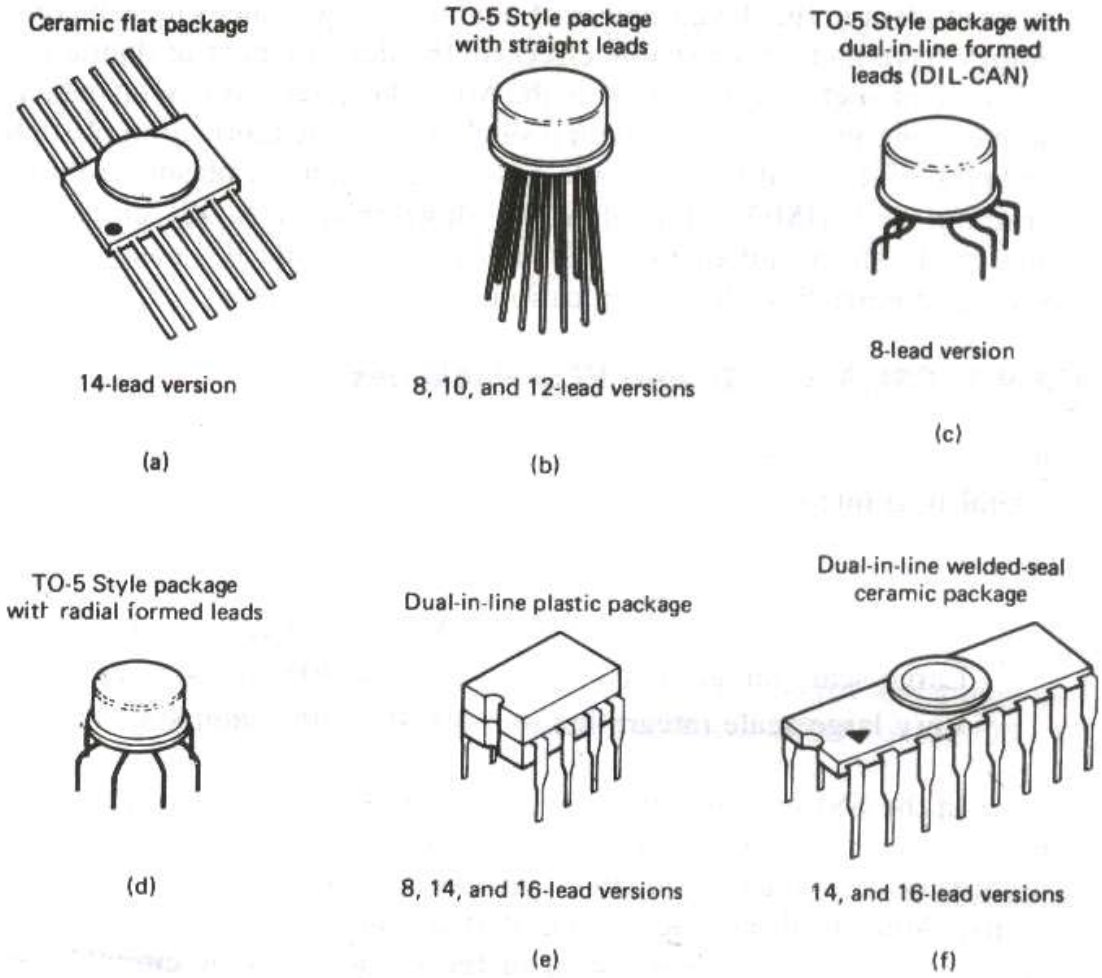


Figure 2–5 Types of IC packages. (a) Flat pack. (b)–(d) Metal can. (e) and (f) Dual-in-line package. (Courtesy of RCA Corporation.)

Temperature Ranges

All ICs manufactured fall into one of the three basic temperature grades:

1. Military temperature range: −55° to +125°C (or −55° to +85°C)
2. Industrial temperature range: −20° to +85°C (or −40° to +85°C)
3. Commercial temperature range: 0° to +70°C (or 0° to +75°C)

THE OPERATIONAL AMPLIFIER:

An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package.

The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication, and integration. Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as ac and dc signal amplification, active filters, oscillators, comparators, regulators, and others.

BLOCK DIAGRAM REPRESENTATION OF A TYPICAL OP-AMP

Since an op-amp is a multistage amplifier, it can be represented by a block diagram as shown in Figure 2-1.

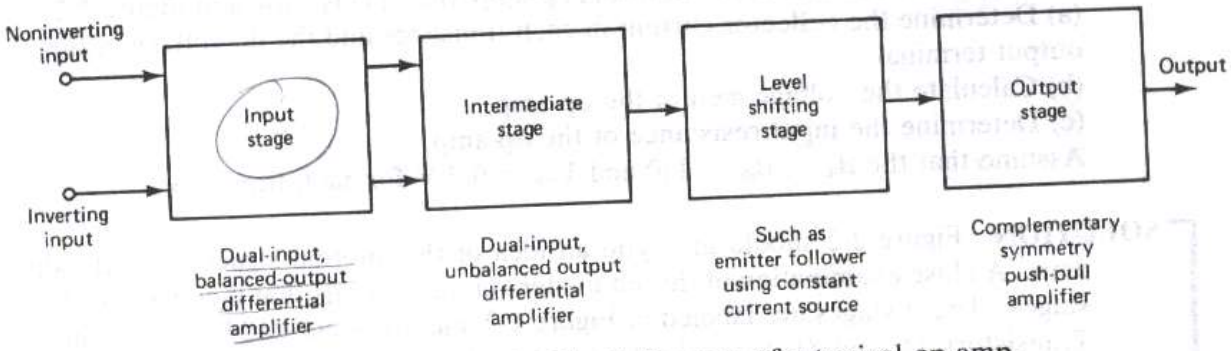


Figure 2–1 Block diagram of a typical op-amp.

The basic amplifier used in Op-Amp is a differential amplifier.

Differential amplifier

Let us consider the emitter-biased circuit. Figure 1-1 shows two identical emitter biased circuits in that transistor Q1 has the same characteristics as transistor Q2, $R_{E1} = R_{E2}$, $R_{C1} = R_{C2}$, and the magnitude of $+V_{CC}$ is equal to the magnitude of $-V_{EE}$. Remember that the supply voltages +

+VCC and -VEE are measured with respect to ground. To obtain a single circuit such as the one in Figure 1-2, we should reconnect these two circuits as follows:

1. Reconnect +VCC supply voltages of the two circuits since the voltages are of the same polarity and amplitude. Similarly, reconnect -VEE supply voltages.
2. Reconnect the emitter E1 of transistor Q1 to the emitter E2 of transistor Q2. (This reconnection places RE1 in parallel with RE2)
3. Show the input signal vin1 applied to the base B1 of transistor Q1 and vin2 applied to the base B2 of transistor Q2.
4. Label the voltage between the collectors C1 and C2 as v0. (The v0 is the output voltage.)

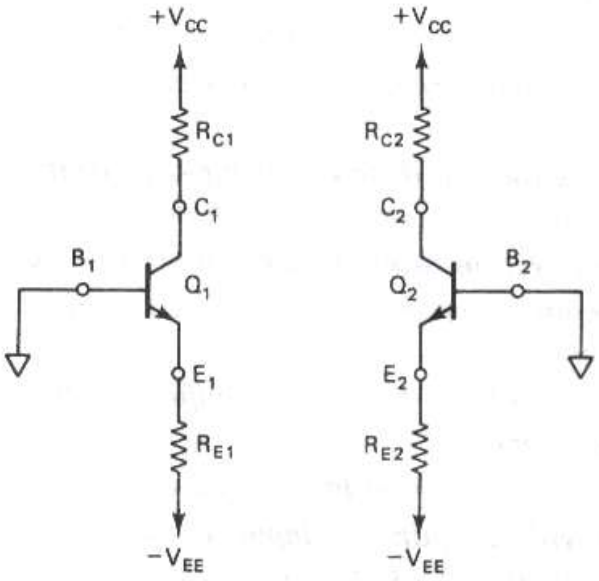


Figure 1–1 Two identical emitter-biased circuits.

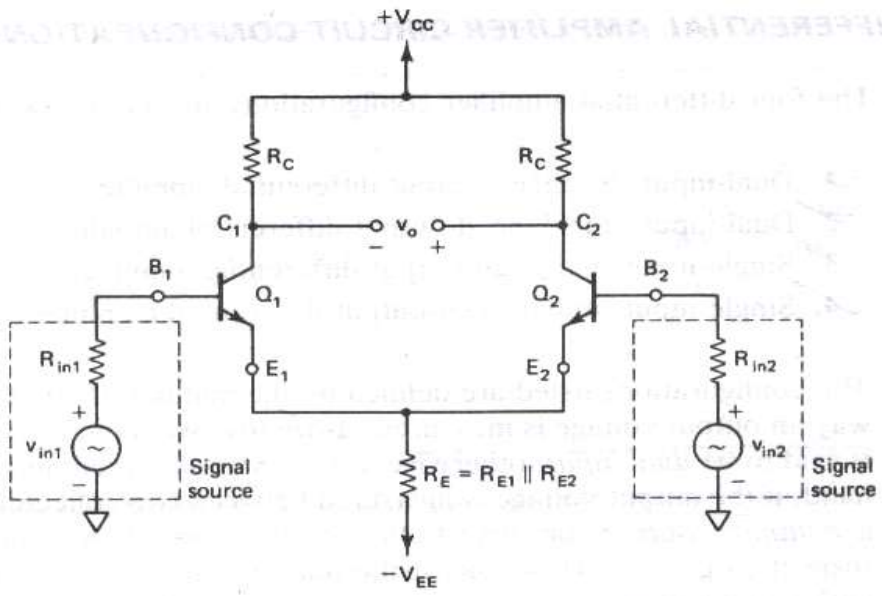


Figure 1–2 Dual-input, balanced-output differential amplifier.

DIFFERENTIAL AMPLIFIER CIRCUIT CONFIGURATIONS

The four differential amplifier configurations are the following:
1. Dual-input, balanced-output differential amplifier
2. Dual-input, unbalanced-output differential amplifier
3. Single-input, balanced-output differential amplifier.
4. Single-input, unbalanced-output differential amplifier

DUAL-INPUT, BA LANCED-OUTPUT DIFFERENTIAL AMPLIFIER

1. DC Analysis

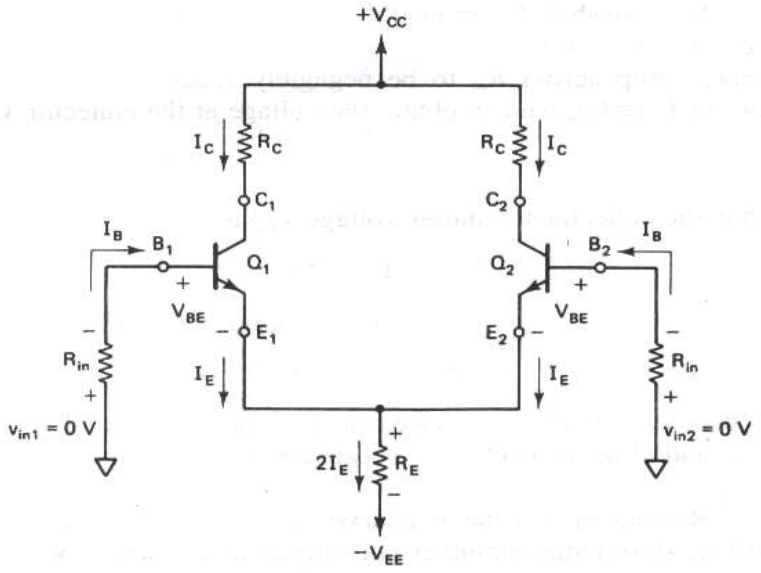


Figure 1–3 DC equivalent circuit of the dual-input, balanced-output differential amplifier.

The dc equivalent circuit can be obtained simply by reducing the input signals vin1 and vin2 to zero. To determine the operating point values *ICQ* and *VCEQ,*

Applying Kirchhoff's voltage law to the base–emitter loop of the transistor Q_1 (see Figure 1-3),

$$-R_{in}I_B - V_{BE} - R_E(2I_E) + V_{EE} = 0 \tag{1-1}$$

But

$$I_B = \frac{I_E}{\beta_{dc}} \qquad \text{since } I_C \cong I_E$$

Thus the emitter current through transistor Q_1 is determined directly from Equation (1-1) as follows:

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + R_{in}/\beta_{dc}} \tag{1-2}$$

where $V_{BE} = 0.6$ V for silicon transistors
$V_{BE} = 0.2$ V for germanium transistors
Generally, $R_{in}/\beta_{dc} \ll 2R_E$. Therefore, Equation (1-2) can be rewritten as

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \tag{1-3}$$

From Equation (1-3) we see that the value of R_E sets up the emitter current in transistors Q_1 and Q_2 for a given value of V_{EE}. In other words, by selecting a proper value of R_E, we can obtain a desired value of emitter current for a knov value of $-V_{EE}$. Notice that the emitter current in transistors Q_1 and Q_2 is indepe dent of collector resistance R_C.

Next we shall determine the collector-to-emitter voltage V_{CE}. The voltage the emitter of transistor Q_1 is approximately equal to $-V_{BE}$ if we assume tl voltage drop across R_{in} to be negligibly smaN. Knowing the value of emitter current I_E ($\cong I_C$), we can obtain the voltage at the collector V_C, as follows:

$$V_C = V_{CC} - R_C I_C$$

Thus the collector-to-emitter voltage V_{CE} is

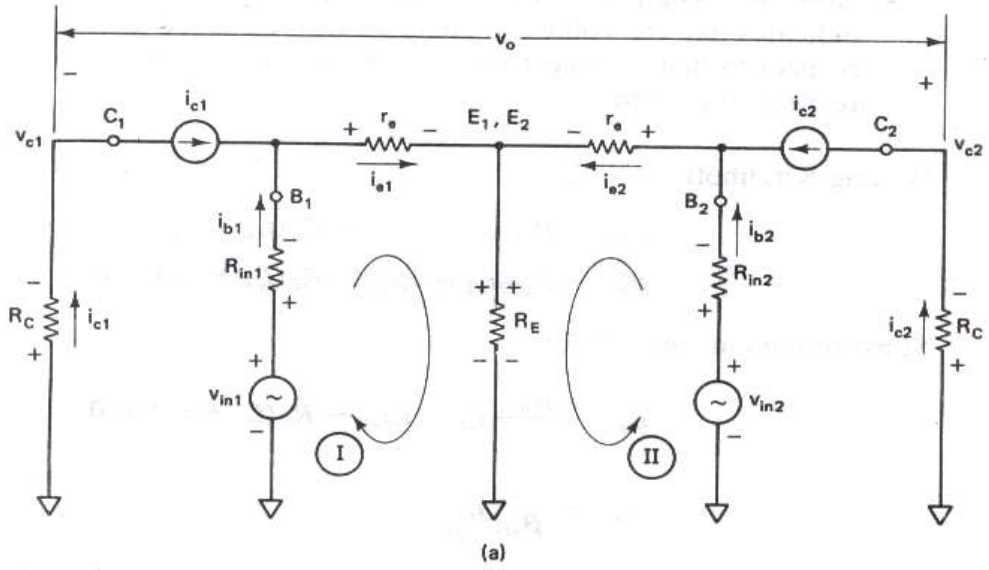
$$\begin{aligned} V_{CE} &= V_C - V_E \\ &= (V_{CC} - R_C I_C) - (-V_{BE}) \end{aligned}$$

$$V_{CE} = V_{CC} + V_{BE} - R_C I_C \tag{1-4}$$

AC Analysis:

To perform ac analysis to derive the expression for the voltage gain Ad and the input resistance Ri of the differential amplifier shown in Figure 1-2:
1. Set the dc voltages + Vcc and -VEE at zero.
2. Substitute the small-signal T-equivalent models for the transistors.

Figure 1-4(a) shows the resulting ac equivalent circuit of the dual-input, balanced- output differential amplifier.



(a) Voltage gain: The following should be noted about the circuit in Figure 1-4(a):
1. $I_{E1} = I_{E2}$; therefore, $r_{e1} = r_{e2}$. For this reason, the ac emitter resistance of transistor Q1 and Q2 is simply denoted by *re.*

2. The voltage across each collector resistor is shown out of phase by 180^0 with respect to the input voltages v_{in1} and v_{in2}. This polarity assignment is in accordance with the common-emitter configuration.

3. Note the assigned polarity of the output voltage v_0. This polarity simply indicates that the voltage at collector C_2 is assumed to be more positive with respect to that at collector C_1, even though both of them are negative with respect to ground.

Writing Kirchhoff's voltage equations for loops I and II in Figure 1-4(a) gives u

$$v_{in\,1} - R_{in\,1} i_{b1} - r_e i_{e1} - R_E(i_{e1} + i_{e2}) = 0 \qquad (1\text{-}5$$

$$v_{in\,2} - R_{in\,2} i_{b2} - r_e i_{e2} - R_E(i_{e1} + i_{e2}) = 0 \qquad (1\text{-}6$$

Substituting current relations $i_{b1} = i_{e1}/\beta_{ac}$ and $i_{b2} = i_{e2}/\beta_{ac}$ yields

$$v_{in\,1} - \frac{R_{in\,1}}{\beta_{ac}} i_{e1} - r_e i_{e1} - R_E(i_{e1} + i_{e2}) = 0$$

$$v_{in\,2} - \frac{R_{in\,2}}{\beta_{ac}} i_{e2} - r_e i_{e2} - R_E(i_{e1} + i_{e2}) = 0$$

Generally, $R_{in\,1}/\beta_{ac}$ and $R_{in\,2}/\beta_{ac}$ values are very small; therefore, we shall neglec them here for simplicity and rearrange these equations as follows:

$$(r_e + R_E) i_{e1} + (R_E) i_{e2} = v_{in\,1} \qquad (1\text{-}$$

$$(R_E) i_{e1} + (r_e + R_E) i_{e2} = v_{in\,2} \qquad (1\text{-}$$

Equations (1-7) and (1-8) can be solved simultaneously for i_{e1} and i_{e2} by usir Cramer's rule:

$$i_{e1} = \frac{\begin{vmatrix} v_{in\,1} & R_E \\ v_{in\,2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} \qquad (1\text{-}9$$

$$= \frac{(r_e + R_E) v_{in\,1} - (R_E) v_{in\,2}}{(r_e + R_E)^2 - (R_E)^2}$$

Similarly,

$$i_{e2} = \frac{\begin{vmatrix} r_e + R_E & v_{in\,1} \\ R_E & v_{in\,2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} \qquad (1\text{-}9b)$$

$$= \frac{(r_e + R_E) v_{in\,2} - (R_E) v_{in\,1}}{(r_e + R_E)^2 - (R_E)^2}$$

The output voltage is

$$\begin{aligned} v_o &= v_{c2} - v_{c1} \\ &= -R_C i_{c2} - (-R_C i_{c1}) \\ &= R_C i_{c1} - R_C i_{c2} \\ &= R_C(i_{e1} - i_{e2}) \qquad \text{since } i_c \cong i_e \end{aligned} \qquad (1\text{-}10)$$

Substituting the current relations i_{e1} and i_{e2} in Equation (1-10), we get

$$\begin{aligned} v_o &= R_C \left[\frac{(r_e + R_E) v_{in\,1} - (R_E) v_{in\,2}}{(r_e + R_E)^2 - (R_E)^2} - \frac{(r_e + R_E) v_{in\,2} - (R_E) v_{in\,1}}{(r_e + R_E)^2 - (R_E)^2} \right] \\ &= R_C \frac{(r_e + R_E)(v_{in\,1} - v_{in\,2}) + (R_E)(v_{in\,1} - v_{in\,2})}{(r_e + R_E)^2 - (R_E)^2} \\ &= R_C \frac{(r_e + 2R_E)(v_{in\,1} - v_{in\,2})}{(r_e^2 + 2r_e R_E + R_E^2 - R_E^2)} \qquad (1\text{-}11) \\ &= R_C \frac{(r_e + 2R_E)(v_{in\,1} - v_{in\,2})}{r_e(r_e + 2R_E)} \\ &= \frac{R_C}{r_e} (v_{in\,1} - v_{in\,2}) \end{aligned}$$

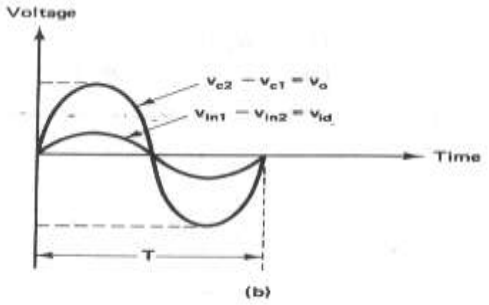


Figure 1–4 Dual-input, balanced-output differential amplifier. (a) AC equivalent circuit. (b) Input and output waveforms.

(b) Differential input resistance. Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded.

$$R_{i1} = \left|\frac{v_{in\,1}}{i_{b1}}\right|_{v_{in\,2}=0}$$

$$= \left|\frac{v_{in\,1}}{i_{e1}/\beta_{ac}}\right|_{v_{in\,2}=0}$$

Substituting the value of i_{e1} from Equation (1-9a), we get

$$R_{i1} = \frac{\beta_{ac} v_{in\,1}}{(r_e + R_E)v_{in\,1} - (R_E)(0)}$$

$$(r_e + R_E)^2 - (R_E)^2$$

$$= \frac{\beta_{ac}(r_e^2 + 2r_e R_E)}{(r_e + R_E)} \qquad (1\text{-}13)$$

$$R_{i1} = \frac{\beta_{ac} r_e (r_e + 2R_E)}{(r_e + R_E)}$$

Generally, $R_E \gg r_e$, which implies that $(r_e + 2R_E) \cong 2R_E$ and $(r_e + R_E) \cong R_E$. Therefore, Equation (1-13) can be rewritten as

$$R_{i1} = \frac{\beta_{ac} r_e (2R_E)}{(R_E)} \qquad (1\text{-}14)$$

$$R_{i1} = 2\beta_{ac} r_e$$

Similarly, the input resistance R_{i2} seen from the input signal source $v_{in\,2}$ is defined as

$$R_{i2} = \left|\frac{v_{in\,2}}{i_{b2}}\right|_{v_{in\,1}=0}$$

$$= \left|\frac{v_{in\,2}}{i_{e2}/\beta_{ac}}\right|_{v_{in\,1}=0}$$

Substituting the value of i_{e2} from Equation (1-9b), we obtain

$$R_{i2} = \frac{\beta_{ac} v_{in\,2}}{(r_e + R_E)v_{in\,2} - (R_E)(0)}$$

$$(r_e + R_E)^2 - (R_E)^2 \qquad (1\text{-}15)$$

$$R_{i2} = \frac{\beta_{ac} r_e (r_e + 2R_E)}{(r_e + R_E)}$$

However, $(r_e + 2R_E) \cong 2R_E$, and $(r_e + R_E) \cong R_E$ if $R_E \gg r_e$. Therefore, Equation (1-15) can be rewritten as

$$R_{i2} = \frac{\beta_{ac} r_e (2R_E)}{R_E} \qquad (1\text{-}16)$$

$$R_{i2} = 2\beta_{ac} r_e$$

(c) Output resistance. Output resistance is defined as the equivalent resistance that would be measured at either output terminal with respect to ground. Therefore, the output resistance R_{01} measured between collector C_1 and ground is equal to that of the collector resistor R_C. Similarly, the output resistance R_{02} measured at collector C_2 with respect to ground is equal to that of the collector resistor R_c. Thus

$$R_{01} = R_{02} = R_C$$

FET DIFFERENTIAL AMPLIFIERS

In the differential amplifier configurations just discussed we have used BJTs. But if we require very high input resistance, we can use FETs instead. Fortunately, the voltage-gain equations derived for these configurations using BJTs can also be used for configurations using FETs, except for the following replacements:

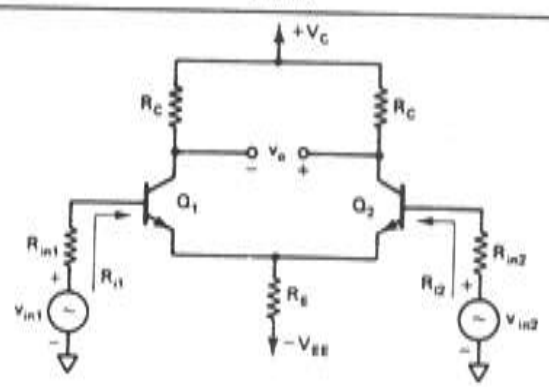
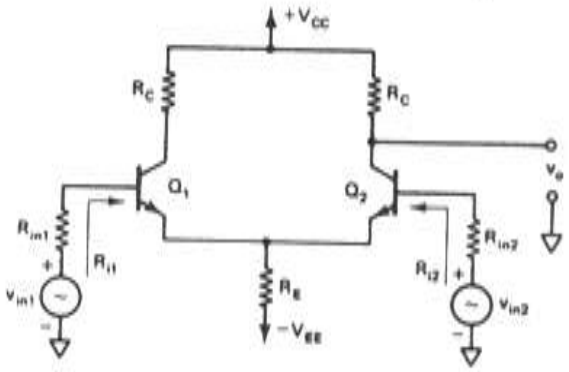
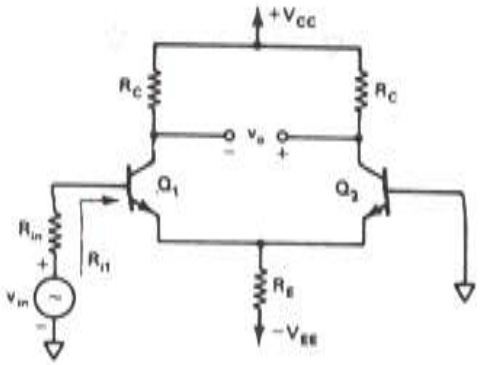
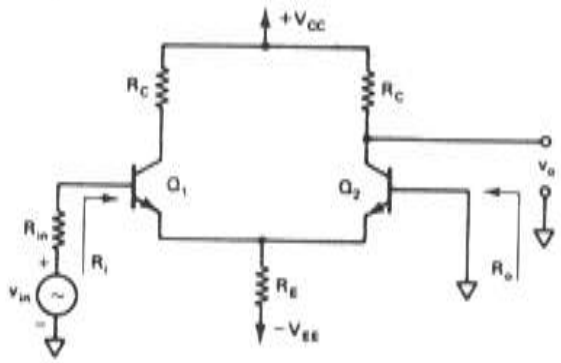
$$R_C \rightarrow R_D$$

$$r_e \rightarrow \frac{1}{g_m}$$

For instance, the voltage gain of the JFET dual-input, balanced-output differential amplifier obtained from Equation (1-12) is

$$A_d = \frac{v_o}{v_{id}} = \frac{R_D}{1/g_m} = g_m R_D$$

TABLE 1–1 PROPERTIES OF THE DIFFERENTIAL AMPLIFIER CIRCUIT CONFIGURATIONS

Configuration	Circuit	Voltage gain	Input resistance	Output resistance
1. Dual input, balanced output		$A_d = \frac{R_C}{r_e}$	$R_{i1} = 2\beta_{ac} r_e$ $R_{i2} = 2\beta_{ac} r_e$	$R_{o1} = R_C$ $R_{o2} = R_C$
2. Dual input, unbalanced output		$A_d = \frac{R_C}{2r_e}$	$R_{i1} = 2\beta_{ac} r_e$ $R_{i2} = 2\beta_{ac} r_e$	$R_o = R_C$
3. Single input, balanced output		$A_d = \frac{R_C}{r_e}$	$R_i = 2\beta_{ac} r_e$	$R_{o1} = R_C$ $R_{o2} = R_C$
4. Single input, unbalanced output		$A_d = \frac{R_C}{2r_e}$	$R_i = 2\beta_{ac} r_e$	$R_o = R_C$

LEVEL TRANSLATOR:

From the results of the cascaded differential amplifier, the following observations can be made:
1. Because of the direct coupling, the dc level at the emitters rises from stage to stage. This increase in dc level tends to shift the operating point of the succeeding stages and, therefore, limits the output voltage swing and may even distort the output signal..
Therefore, the final stage should be included to shift the output dc level at the second stage down to about zero volts to ground. Such a stage is referred to as a *level translator* or *shifter*.

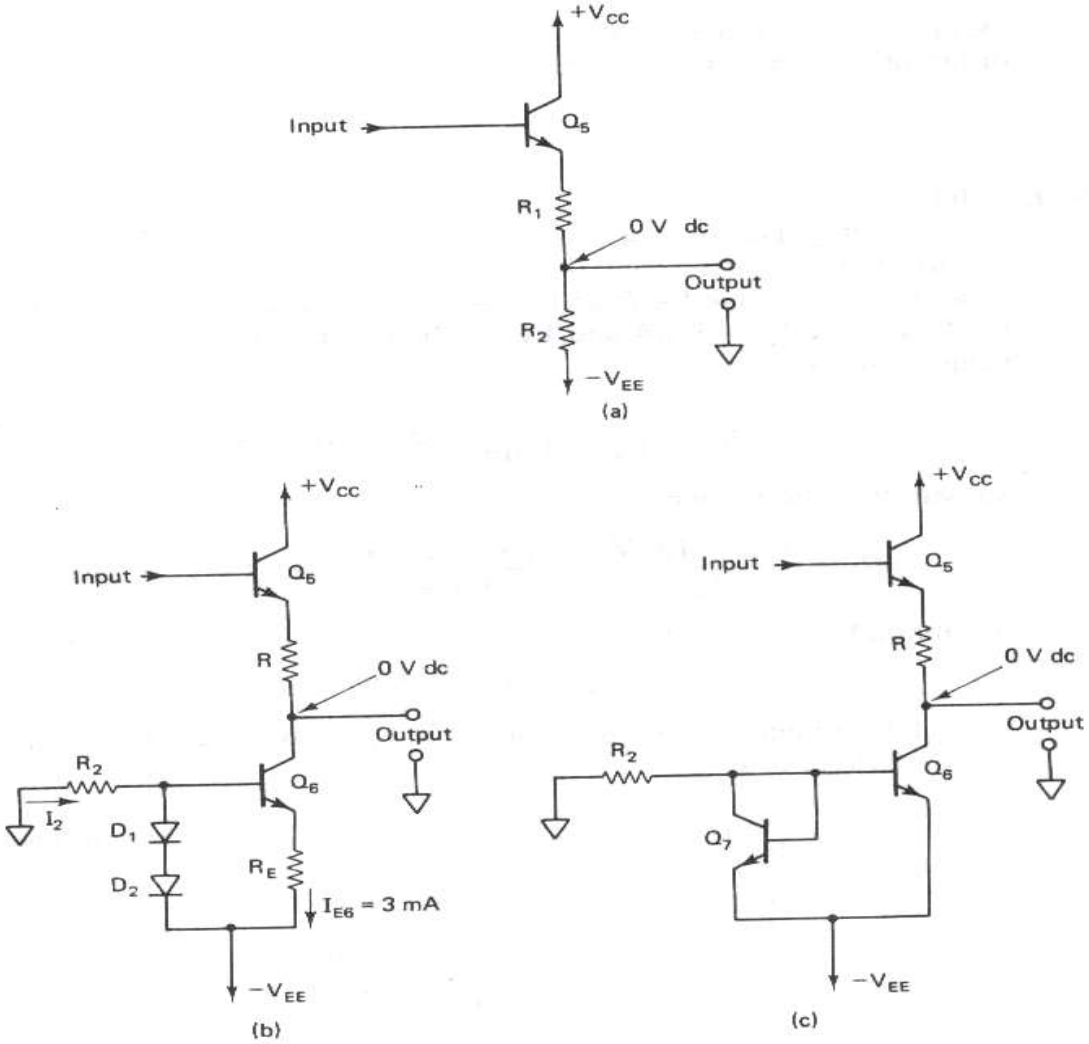


Figure 1–20 Level translator circuits. (a) Emitter follower with voltage divider. (b) Emitter follower with constant current bias. (c) Emitter follower with current mirror.

The voltage at the junction will be zero by selecting proper values of R_1 and R_2. Better results are obtained by using an emitter follower either with a diode constant current bias or a current mirror instead of the voltage divider, as shown in Figure 1-20(b) and (c), respectively.

The output stage is generally a push-pull or push-pull complementary-symmetry pair.

Inverting and Non-inverting Inputs

In the differential amplifier circuit the non-inverting input because a positive voltage v_{in1} acting alone produces a positive output voltage. This can be seen from voltage-gain equation (1-1 1). Similarly, the positive voltage v_{in2} alone produces a negative output voltage; hence v_{in2} is called the inverting input [see Equation (1-11)]. Consequently, the base terminal B_1 to which v_{in1} is applied is referred to as the non-inverting input terminal, and the base terminal B_2 is called the inverting input terminal.

SCHEMATIC SYMBOL

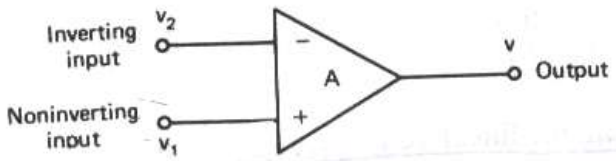


Figure 2–4 Schematic symbol for the op-amp.

In Figure 2-4,

v_1 = voltage at the noninverting input (volts)

v_2 = voltage at the inverting input (volts)

v_o = output voltage (volts)

All these voltages are measured with respect to ground.

A = large-signal voltage gain, which is specified on the data sheet for an op-amp

THE IDEAL OP-AMP

An ideal op-amp would exhibit the following electrical characteristics:

1. Infinite voltage gain A.
2. Infinite input resistance R, so that almost any signal source can drive it and there is no loading of the preceding stage.
3. Zero output resistance R, so that output can drive an infinite number of other devices.
4. Zero output voltage when input voltage is zero.
5. Infinite bandwidth so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.
6. Infinite common-mode rejection ratio so that the output common-mode noise voltage is zero.
7. Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

EQUIVALENT CIRCUIT OF AN OP-AMP

The output voltage is

$$v_o = Av_{id} = A(v_1 - v_2)$$

Where A = large-signal voltage gain
v_{id}= difference input voltage
v_1= voltage at the non-inverting input terminal with respect to ground
v_2= voltage at the inverting terminal with respect to ground

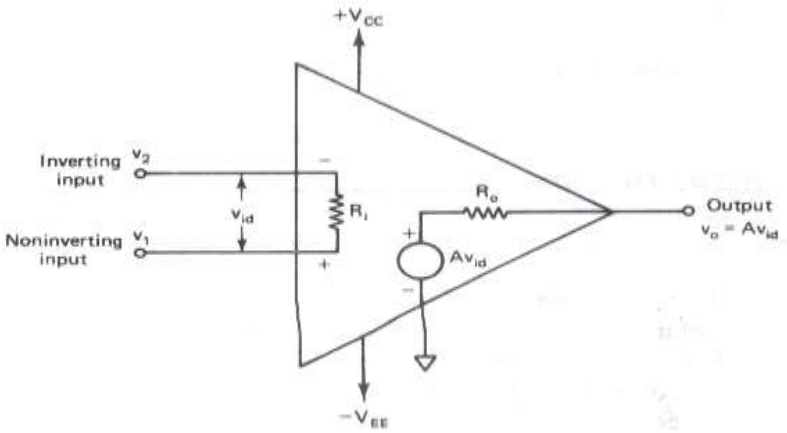


Figure 3–7 Equivalent circuit of an op-amp.

IDEAL VOLTAGE TRANSFER CURVE

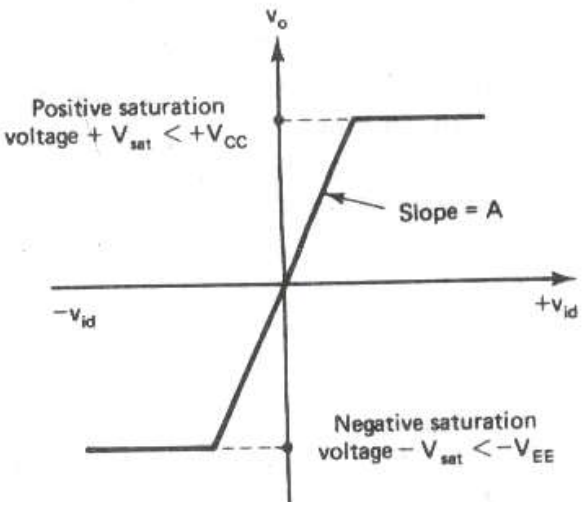


Figure 3–8 Ideal voltage transfer curve.

OPEN-LOOP OP-AMP CONFIGURATIONS

1. Differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

The Differential Amplifier

$$v_o = A(v_{\text{in 1}} - v_{\text{in 2}})$$

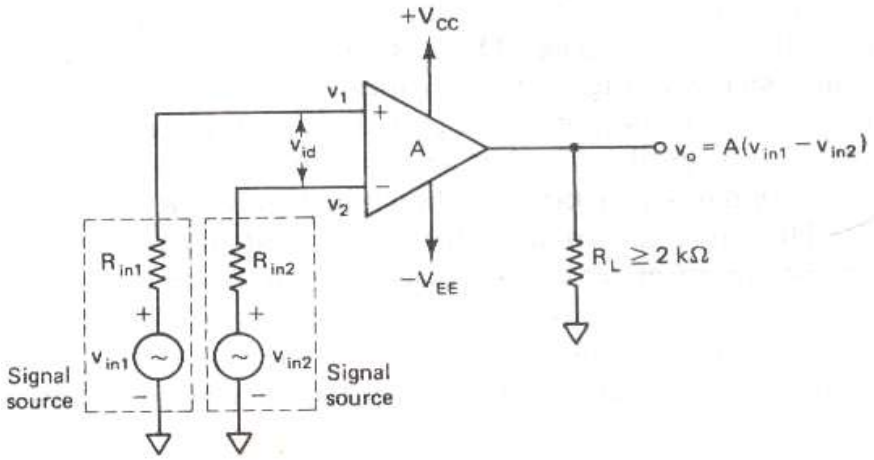


Figure 3–9 Open-loop differential amplifier.

The Inverting Amplifier

$$v_o = -Av_{in}$$

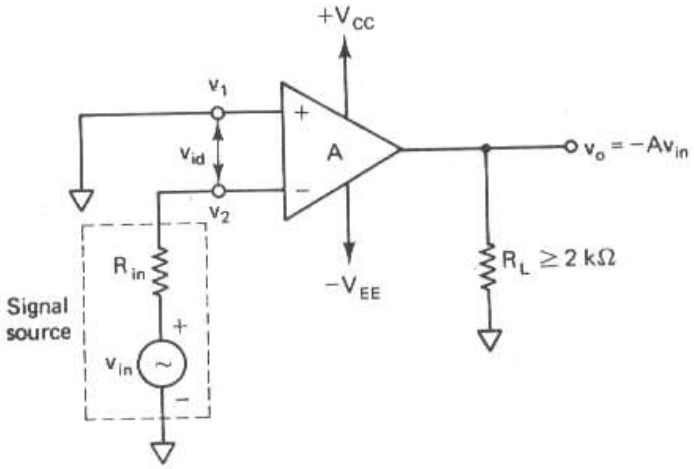


Figure 3–10 Inverting amplifier.

The Non-inverting Amplifier

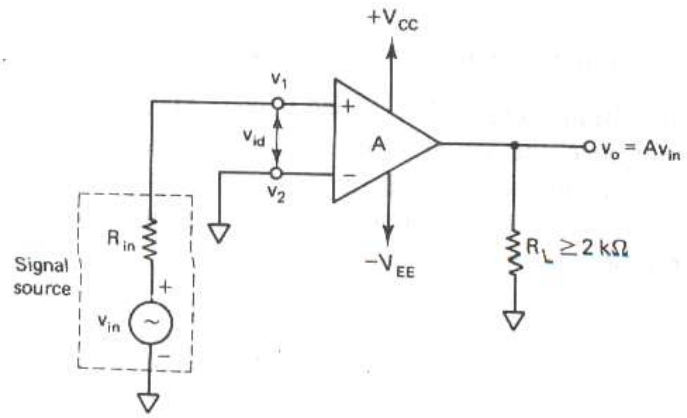


Figure 3–11 Noninverting amplifier.

$$v_o = Av_{in}$$

BLOCK DIAGRAM REPRESENTATION OF FEEDBACK CONF1GURA TIONS

An op-amp that uses feedback is called a feedback amplifier. A closed-loop amplifier can be represented by using two blocks, one for an op-amp and another for a feedback circuit. There are four ways to connect these two blocks. These connections are classified according to whether the voltage or current is fed back to the input in series or in parallel, as follows:

1. Voltage-series feedback
2. Voltage-shunt feedback
3. Current-series feedback
4. Current-shunt feedback

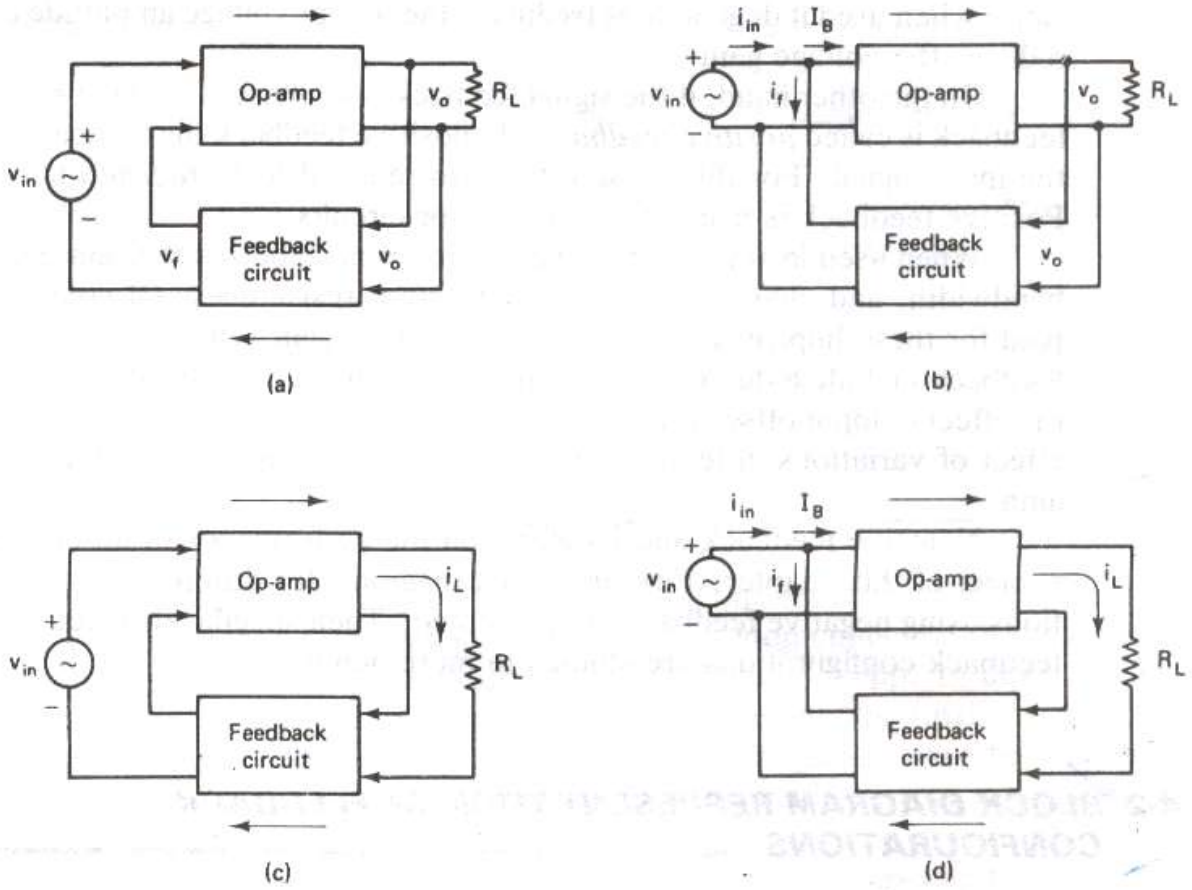


Figure 4–1 Feedback configurations. (a) Voltage-series. (b) Voltage-shunt. (c) Current-series. (d) Current-shunt. Arrows indicate the signal flow directions.

VOLTAGE-SERIES FEEDBACK AMPLIFIER

The schematic diagram of the voltage-series feedback amplifier is shown in Figure 4-2. The op-amp is represented by its schematic symbol, including its large-signal voltage gain A, and the feedback circuit is composed of two resistors, R_1 and R_F.

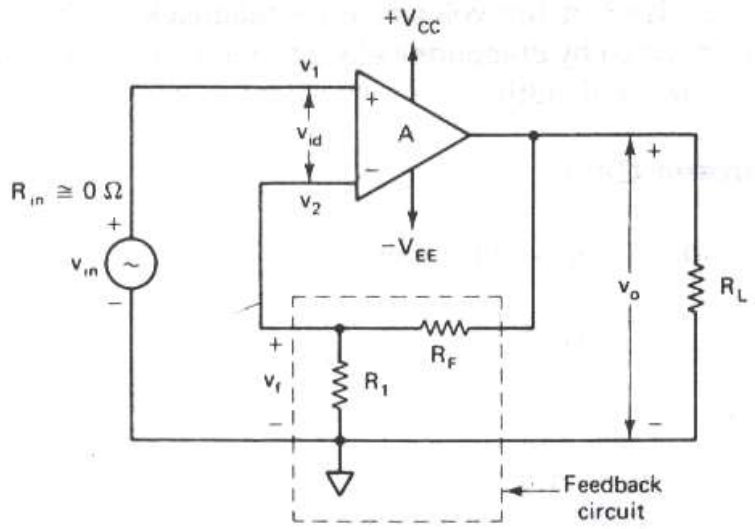


Figure 4–2 Voltage-series feedback amplifier (or noninverting amplifier with feedback).

The circuit shown in Figure 4-2 is commonly known as a non-inverting amplifier with feedback (or closed-loop non-inverting amplifier) because it uses feedback, and the input signal is applied to the non-inverting input terminal of the op-amp.

open-loop voltage gain (or gain without feedback) $A = \frac{v_o}{v_{id}}$

closed-loop voltage gain (or gain with feedback) $A_F = \frac{v_o}{v_{in}}$

gain of the feedback circuit $B = \frac{v_f}{v_o}$

where v_{in} = input voltage
v_f= feedback voltage
v_{id}= difference input voltage

it will be performed by computing closed-loop voltage gain, input and output resistances, and the bandwidth.

4-3.2 Closed-Loop Voltage Gain

As defined previously, the closed-loop voltage gain

$$A_F = \frac{v_o}{v_{in}}$$

However, by Equation (3-9),

$$v_o = A(v_1 - v_2)$$

Referring to Figure 4-2, we see that

$$v_1 = v_{in}$$

$$v_2 = v_f = \frac{R_1 v_o}{R_1 + R_F} \qquad \text{since } R_i \gg R_1$$

Therefore,

$$v_o = A\left(v_{in} - \frac{R_1 v_o}{R_1 + R_F}\right)$$

Rearranging, we get

$$v_o = \frac{A(R_1 + R_F)v_{in}}{R_1 + R_F + AR_1}$$

Thus

$$A_F = \frac{v_o}{v_{in}} = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1} \quad \text{(exact)} \tag{4-2}$$

Generally, A is very large (typically 10^5). Therefore,

$$AR_1 \gg (R_1 + R_F) \quad \text{and} \quad (R_1 + R_F + AR_1) \cong AR_1$$

Thus

$$A_F = \frac{v_o}{v_{in}} = 1 + \frac{R_F}{R_1} \qquad \text{(ideal)} \tag{4-3}$$

Equation (4-3) is important because it shows that the gain of the voltage- series feedback amplifier is determined by the ratio of two resistors, R_F, and R_1

Another interesting result can be obtained from Equation (4-3). As defined previously, the gain of the feedback circuit (B) is the ratio of v_f and v_0. Referring to Figure 4-2, this gain is

$$B = \frac{v_f}{v_o} = \frac{R_1}{R_1 + R_F} \tag{4-4}$$

Comparing Equations (4-3) and (4-4), we can conclude that

$$A_F = \frac{1}{B} \quad \text{(ideal)} \tag{4-5}$$

Finally, the closed-loop voltage gain AF can be expressed in terms of open- loop gain A and feedback circuit gain B as follows. Rearranging Equation (4-2), we get

$$A_F = \frac{A\left(\frac{R_1 + R_F}{R_1 + R_F}\right)}{\frac{R_1 + R_F}{R_1 + R_F} + \frac{AR_1}{R_1 + R_F}}$$

Using Equation (4-4) yields

$$A_F = \frac{A}{1 + AB} \tag{4-6}$$

where AF = closed-loop voltage gain
A = open-loop voltage gain
B = gain of the feedback circuit
AB = loop gain
A one-line block diagram of Equation (4-6) is shown in Figure 4-3. This block diagram illustrates a standard form for representing a system with feedback and also indicates the relationship between different variables of the system. The block-diagram approach helps to simplify the analysis of complex closed-loop networks, particularly if they are composed of non-resistive feedback circuits.

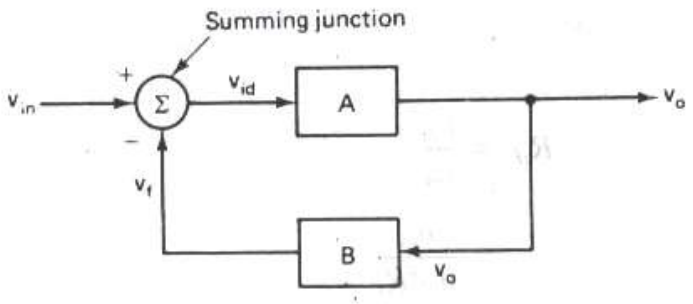


Figure 4–3 Block diagram representation of noninverting amplifier with feedback.

Difference Input Voltage Ideally Zero:

$$v_{id} = \frac{v_o}{A}$$

Since A is very large (ideally infinite),

$$v_{id} \cong 0 \qquad (4\text{-}7a)$$

That is,

$$v_1 \cong v_2 \qquad \text{(ideal)} \qquad (4\text{-}7b)$$

Equation (4-7b) says that the voltage at the non-inverting input terminal of an op-amp is approximately equal to that at the inverting input terminal provided that A is very large. This concept is useful in the analysis of closed-loop op-amp circuits. For example, ideal closed-loop voltage gain Equation (4-3) can be obtained using the preceding results as follows. In the circuit of Figure 4-2,

$$v_1 = v_{in}$$

$$v_2 = v_f$$

$$= \frac{R_1 v_o}{R_1 + R_F}$$

Substituting these values of v_1 and v_2 in Equation (4-7b), we get

$$v_{in} = \frac{R_1 v_o}{R_1 + R_F}$$

That is,

$$A_F = \frac{v_o}{v_{in}} = 1 + \frac{R_F}{R_1}$$

Input Resistance with Feedback :

Figure 4-4 shows a voltage-series feedback amplifier with the op-amp equivalent circuit. In this circuit R_i is the input resistance (open loop) of the op-amp, and R_{iF} is the input resistance of the amplifier with feedback. The input resistance with feedback is defined as

$R_{iF}=v_{in}/i_{in} = v_{in}/(v_{id}/R_i)$

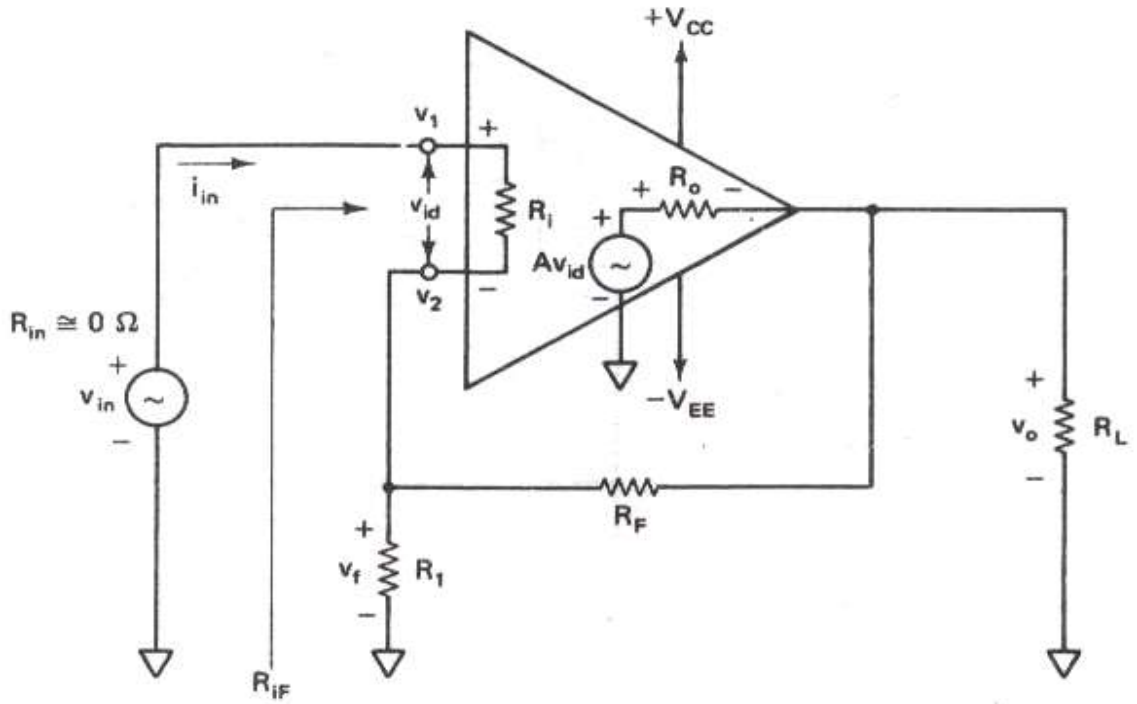


Figure 4–4 Derivation of input resistance with feedback.

However,

$$v_{id} = \frac{v_o}{A} \quad \text{and} \quad v_o = \frac{A}{1 + AB} v_{in}$$

Therefore,

$$R_{iF} = R_i \frac{v_{in}}{v_o/A}$$

$$= AR_i \frac{v_{in}}{Av_{in}/(1 + AB)} \qquad (4\text{-}8)$$

$$= R_i(1 + AB)$$

This means that the input resistance of the op-amp with feedback is $(1 + AB)$ times that without feedback.

Output Resistance with Feedback :

Output resistance is the resistance determined looking back into the feedback amplifier from the output terminal as shown in Figure 4-5. This resistance can be obtained by using Thevenin's theorem for dependent sources. Specifically, to find output resistance with feedback R_{oF}, reduce independent source v_{in} to zero, apply an external voltage v_o, and then calculate the resulting current i_o. In short, the R0F is defined as follows: $R_{oF}=v_o/i_o$

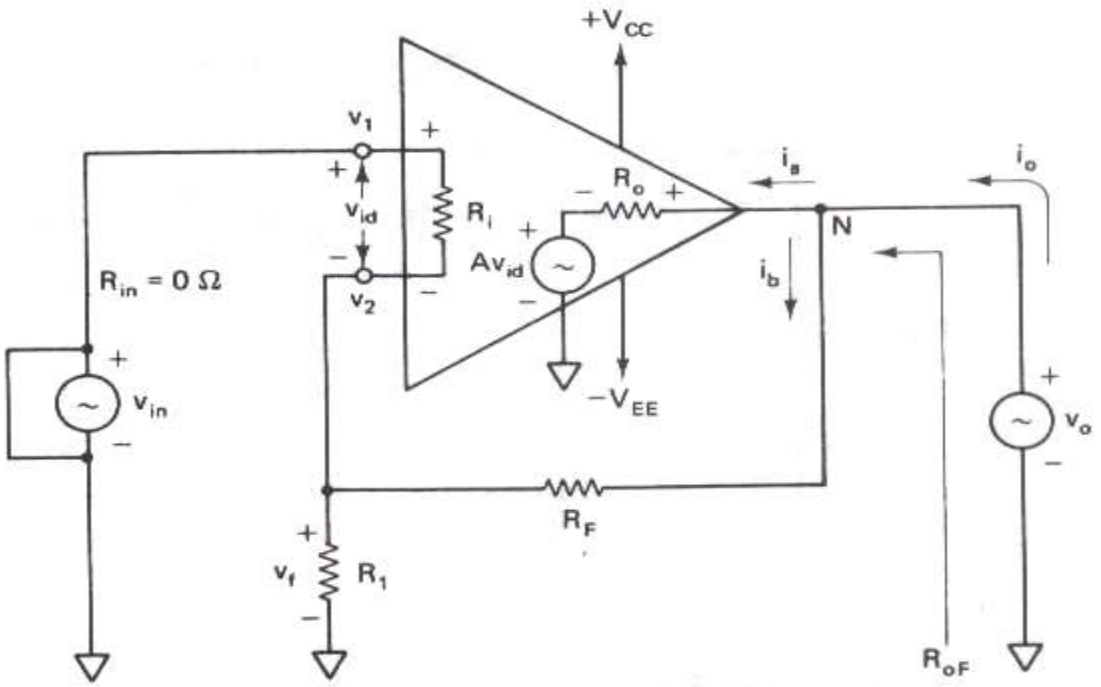


Figure 4–5 Derivation of output resistance with feedback.

Writing Kirchhoff's current equation at output node N, we get

$$i_o = i_a + i_b$$

since $[(R_F + R_1) \parallel R_i] \gg R_o$ and $i_a \gg i_b$. Therefore,

$$i_o \cong i_a$$

The current i_o can be found by writing Kirchhoff's voltage equation for the output loop:

$$v_o - R_o i_o - A v_{id} = 0$$

$$i_o = \frac{v_o - A v_{id}}{R_o}$$

However,

$$v_{id} = v_1 - v_2$$

$$= 0 - v_f$$

$$= -\frac{R_1 v_o}{R_1 + R_F} = -B v_o$$

Therefore,

$$i_o = \frac{v_o + AB v_o}{R_o}$$

Substituting the value of i_o in Equation (4-9a), we get

$$R_{oF} = \frac{v_o}{(v_o + ABv_o)/R_o} \qquad (4\text{-}9b)$$

$$= \frac{R_o}{1 + AB}$$

Bandwidth with Feedback :

The bandwidth of an amplifier is defined as the band (range) of frequencies for which the gain remains constant.

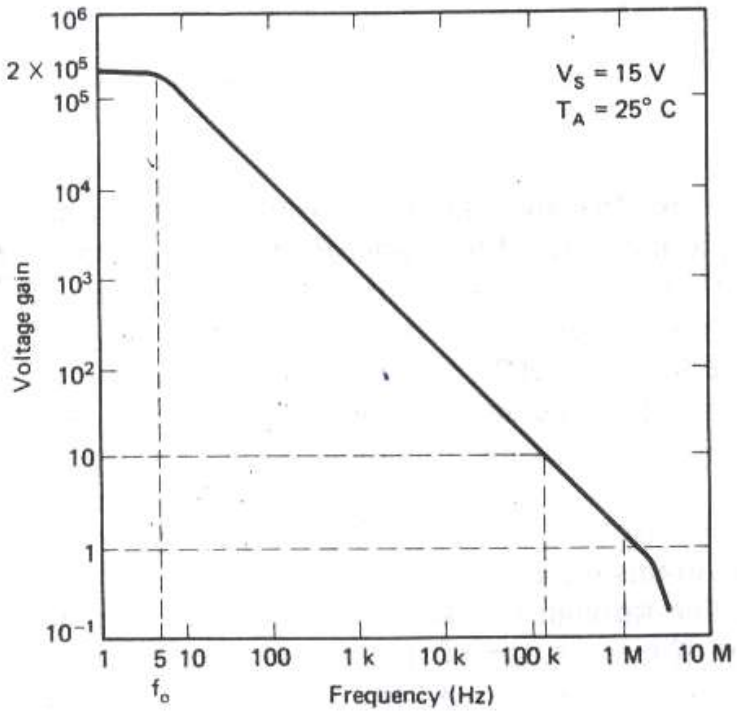


Figure 4–6 Open-loop gain versus frequency curve of the 741C.

The frequency at which the gain equals 1 is known as the unity gain—bandwidth (UGB). The relationship between the break frequencyf_0, open-loop voltage gain A, bandwidth with feedback f_F, and the closed-loop gain A_F can be established as follows. Since for an op-amp with a single break frequencyf_0, the gain-bandwidth product is constant, and equal to the unity gain bandwidth (UGB), we can write,

$$\text{UGB} = (A)(f_o) \tag{4-10a}$$

where A = open-loop voltage gain
f_o = break-frequency of an op-amp
or, alternatively, only for a single break frequency op-amp,

$$\text{UGB} = (A_F)(f_F) \tag{4-10b}$$

where A_F = closed-loop voltage gain
f_F = bandwidth with feedback
Therefore, equating Equations (4-10a) and (4-10b),

$$(A)(f_o) = (A_F)(f_F)$$

or

$$f_F = \frac{(A)(f_o)}{A_F} \tag{4-10c}$$

However, for the noninverting amplifier with feedback,

$$A_F = \frac{A}{1 + AB}$$

Therefore, substituting the value of A_F in Equation (4-10c), we get

$$f_F = \frac{(A)(f_o)}{A/(1 + AB)}$$

or

$$f_F = f_o(1 + AB) \tag{4-10d}$$

Equation (4-lOd) indicates that the bandwidth of the noninverting amplifier with feedback,fF, is equal to its bandwidth without feedbackqf0, times (1 + AB).

Total Output Offset Voltage with Feedback :

In an op-amp when the input is zero, the output is also expected to be zero. However, because of the effect of input offset voltage and current, the output is significantly larger, a result in large part of very high open-loop gain. Since with feedback the gain of the non-inverting amplifier changes from A to A/(1 + AB) [Equation (4-6)1, the total output offset voltage with feedback must also be 1/(1 + AB) times the voltage without feedback. That is,

$$\begin{pmatrix}\text{total output offset}\\ \text{voltage with feedback}\end{pmatrix} = \frac{\text{total output offset voltage without feedback}}{1 + AB}$$

or

$$V_{ooT} = \frac{\pm V_{sat}}{1 + AB} \tag{4-11}$$

Voltage Follower :

The lowest gain that can be obtained from a non-inverting amplifier with feedback is 1. When the non-inverting amplifier is configured for unity gain, it is called a voltage follower because the output voltage is equal to and in phase with the input. In other words, in the voltage follower the output follows the input. Since the voltage follower is a special case of the non-inverting amplifier, all the formulas developed for the latter are indeed applicable to the former except that the gain of the feedback circuit is 1 (B =1). The applicable formulas are

$$A_F = 1$$

$$R_{iF} = AR_i$$

$$R_{oF} = \frac{R_o}{A}$$

$$f_F = Af_o$$

$$V_{ooT} = \frac{\pm V_{sat}}{A}$$

since $(1 + A) \cong A$.

The voltage follower is also called a non-inverting buffer because, when placed between two networks, it removes the loading on the first network.

VOLTAGE-SHUNT FEEDBACK AMPLIFIER:

Figure 4-8 shows the voltage-shunt feedback amplifier using an op-amp. The input voltage drives the inverting terminal, and the amplified as well as inverted output signal is also applied to the inverting input via the feedback resistor RF. This arrangement forms a negative feedback because any increase in the output signal results in a feedback signal into the inverting input, causing a decrease in the output signal.

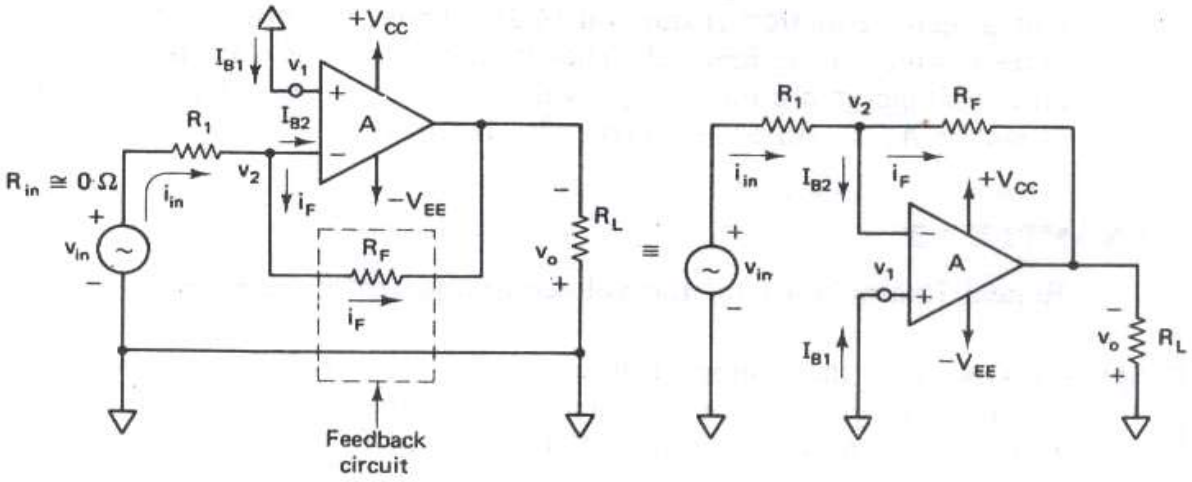


Figure 4–8 Voltage-shunt feedback amplifier (or inverting amplifier with feedback).

Closed-Loop Voltage Gain :

The closed-loop voltage gain AF of the voltage-shunt feedback amplifier can be obtained by writing Kirchhoff's current equation at the input node v_2 (see Figure 4-8) as follows:

$$i_{in} = i_F + I_B \tag{4-12a}$$

Since R_i is very large, the input bias current I_B is negligibly small. For instance, $R_i = 2\ M\Omega$ and $I_B = 0.5\ \mu A$ for the 741C. Therefore,

$$i_{in} \cong i_F$$

That is,

$$\frac{v_{in} - v_2}{R_1} = \frac{v_2 - v_o}{R_F} \tag{4-12b}$$

However, from Equation (3-9),

$$v_1 - v_2 = \frac{v_o}{A}$$

Since $v_1 = 0$ V,

$$v_2 = -\frac{v_o}{A}$$

Substituting this value of v_2 in Equation (4-12b) and rearranging, we get

$$\frac{v_{in} + v_o/A}{R_1} = \frac{-(v_o/A) - v_o}{R_F}$$

$$A_F = \frac{v_o}{v_{in}} = -\frac{AR_F}{R_1 + R_F + AR_1} \quad \text{(exact)} \tag{4-13}$$

Since the internal gain A of the op-amp is very large (ideally infinity), $AR_1 >> R_1 + R_F$. This means that Equation (4-13) can be rewritten as

$$A_F = \frac{v_o}{v_{in}} = -\frac{R_F}{R_1} \quad \text{(ideal)} \tag{4-14}$$

This equation shows that the gain of the inverting amplifier is set by selecting a ratio of feedback resistance R_F to the input resistance R_1. Let us now rewrite Equation (4-13) in the feedback form of Equation (4-6), for a couple of reasons. First, it facilitates analysis of the inverting amplifier with feedback. Second, it helps compare and contrast inverting and non-inverting amplifier configurations, as we shall soon see. To begin with, we divide both numerator and denominator of Equation (4-13) by $(R_1 + R_F)$:

$$A_F = -\frac{AR_F/R_1 + R_F}{1 + \frac{AR_1}{R_1 + R_F}} \qquad (4\text{-}15)$$

$$= -\frac{AK}{1 + AB}$$

where $K = \frac{R_F}{R_1 + R_F}$, a voltage attenuation factor

$B = \frac{R_1}{R_1 + R_F}$, gain of the feedback circuit

A comparison of Equation (4-15) with the feedback Equation (4-6) indicates that, in addition to the phase inversion (-sign), the closed-loop gain of the inverting amplifier is K times the closed-loop gain of the non-inverting amplifier, where K <1.

The one-line block diagram of the inverting amplifier with feedback is shown in Figure 4-9. The reason for the block diagram is twofold: (1) to facilitate the analysis of the inverting amplifier, and (2) to express the performance equations in the same form as those for the non-inverting amplifier.

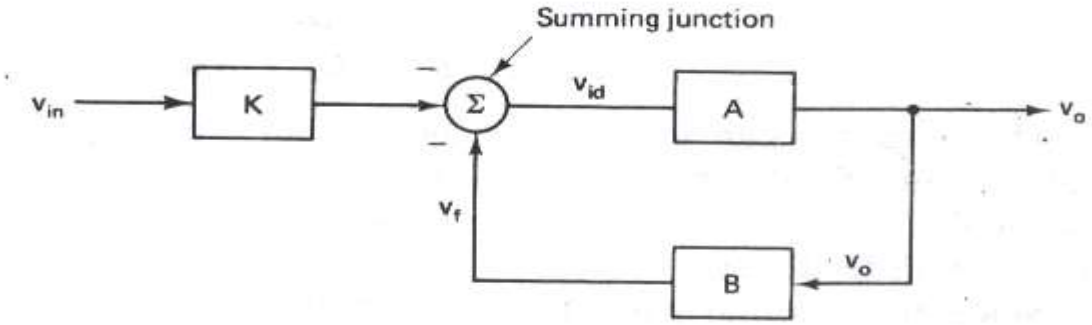


Figure 4–9 Block diagram of inverting amplifier with feedback using a voltage-summing junction as a model for current summing.

To derive the ideal closed-loop gain, we can use Equation (4-15) as follows. If AB>> 1, then (1+AB)= AB and

$$A_F = -\frac{K}{B} \qquad (4\text{-}16)$$

$$= -\frac{R_F}{R_1}$$

Inverting Input Terminal at Virtual Ground:

Refer again to the inverting amplifier of Figure 4-8. In this figure, the non-inverting terminal is grounded, and the input signal is applied to the inverting terminal via resistor R1. The difference input voltage is ideally zero; that is, the voltage at the inverting terminal (v_2,) is approximately equal to that at the non-inverting terminal (v_1). In other words, the inverting terminal voltage v_2 is approximately at ground potential. Therefore, the inverting terminal is said to be at virtual ground. This concept is extremely useful in the analysis of closed-loop inverting amplifier circuits. For example, ideal closed- loop gain Equation (4-14)1 can be obtained using the virtual-ground concept as follows:

$$i_{in} \cong i_F \tag{4-17}$$

That is,

$$\frac{v_{in} - v_2}{R_1} = \frac{v_2 - v_o}{R_F}$$

However,

$$v_1 = v_2 = 0 \text{ V}$$

Therefore,

$$\frac{v_{in}}{R_1} = -\frac{v_o}{R_F}$$

or

$$A_F = \frac{v_o}{v_{in}} = -\frac{R_F}{R_1}$$

Input Resistance with Feedback :

The easiest method of finding the input resistance is to Millerize the feedback resistor R_F; that is, split R_F into its two Miller components as shown in Figure 4-10.

In the circuit of Figure 4-10, the input resistance with feedback $R_{iF}=(R_1+R_F/(1+A))\|(Ri)$

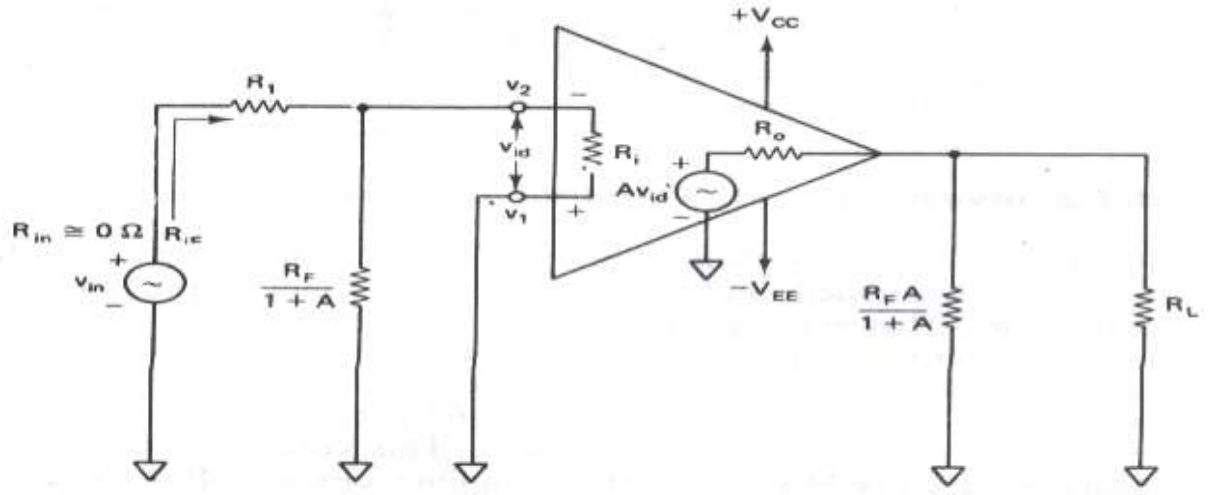


Figure 4–10 Inverting amplifier with Millerized feedback resistor.

Since R_i and A are very large,

$$\frac{R_F}{1 + A} \| R_1 \cong 0\ \Omega$$

Hence

$$R_{iF} = R_1 \quad \text{(ideal)} \tag{4-19}$$

Output Resistance with Feedback :

The output resistance with feedback R_{oF} is the resistance measured at the output terminal of the feedback amplifier. The output resistance of the non-inverting amplifier was obtained by using Thevenin's theorem, and we can do the same for the inverting amplifier. Thévenin's equivalent circuit for R_{0F} of the inverting amplifier is shown in Figure 4-11. Note that this Thvenin's equivalent circuit is exactly the same as that for non-inverting amplifier (Figure 4-5) because the output resistance R_{0F} of the inverting amplifier must be identical to that of the non-inverting amplifier [Equation (4-9b)].

$$R_{oF} = \frac{R_o}{1 + AB} \tag{4-20}$$

where R_o = output resistance of the op-amp
A = open-loop voltage gain of the op-amp
B = gain of the feedback circuit

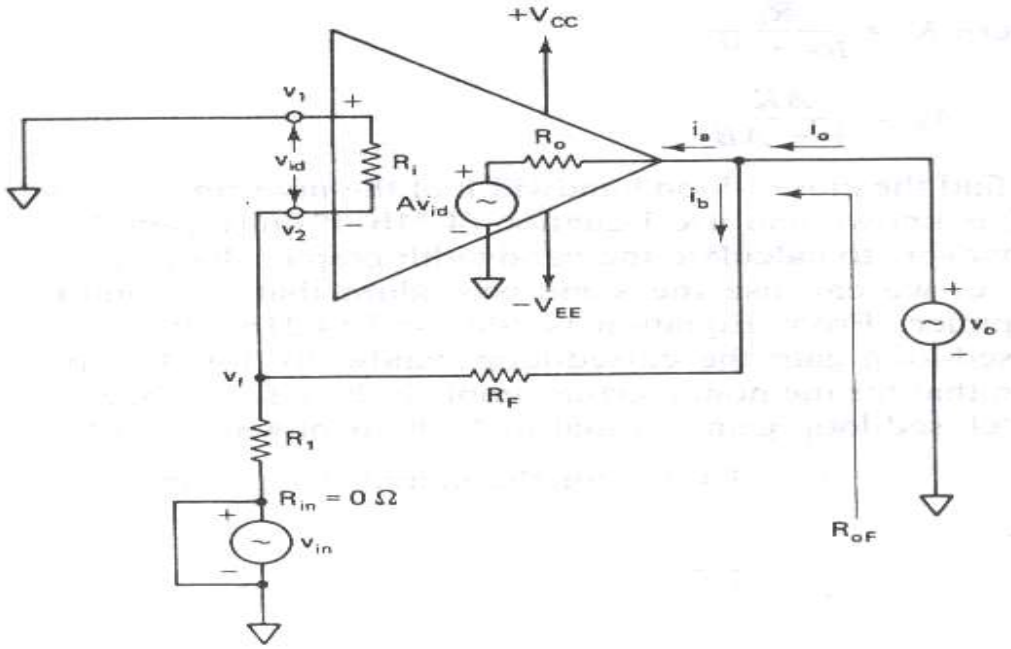


Figure 4–11 Thévenin's equivalent circuit for R_{oF} of the inverting amplifier.

Bandwidth with Feedback :

As mentioned previously, the gain bandwidth product of a single break frequency op-amp is always constant.

$$f_F = f_o(1 + AB) \tag{4-21a}$$

where f_o = break frequency of the op-amp

$$= \frac{\text{unity gain bandwidth}}{\text{open-loop voltage gain}}$$

$$= \frac{\text{UGB}}{A}$$ (true only for the single break frequency op-amp such as the 741).

Substituting the value of f_o in Equation (4-21a), we get

$$f_F = \frac{\text{UGB}}{A}(1 + AB) \tag{4-21b}$$

$$f_F = \frac{(\text{UGB})(K)}{A_F}$$

where $K = \dfrac{R_F}{R_1 + R_F}$

$$A_F = \frac{AK}{1 + AB}$$

$f_F = \text{UGB}$ for the noninverting amplifier

and

$f_F = \dfrac{\text{UGB}}{2}$ for the inverting amplifier, since $R_1 = R_F$.

Total Output Offset Voltage with Feedback :

$$\begin{pmatrix}\text{total output offset}\\ \text{voltage with feedback}\end{pmatrix} = \frac{\text{total output offset voltage without feedback}}{1 + AB}$$

That is,

$$V_{ooT} = \frac{\pm V_{sat}}{1 + AB} \tag{4-22}$$

where $\pm V_{sat}$ = saturation voltages

A = open-loop voltage gain of the op-amp

B = gain of the feedback circuit

$$B = \frac{R_F}{R_1 + R_F}$$

The output voltage of the op-amp without feedback can be either $+V_{sat}$ or $-V_{sat}$ because of its very high voltage gain A, which is typically on the order of 10^5.

Note that the V_{ooT} equation for the inverting amplifier is the same as that for the noninverting amplifier. This is because, when the input signal v_{in} is reduced to zero, both inverting and non-inverting amplifiers result in the same circuit.

Current-to-voltage Converter:
Let us reconsider the ideal voltage-gain Equation (4-14) of the inverting amplifier,

$$\frac{v_o}{v_{in}} = -\frac{R_F}{R_1}$$

Therefore,

$$v_o = -\left(\frac{v_{in}}{R_1}\right)R_F$$

However, since $v_1 = 0$ V and $v_1 = v_2$.

$$\frac{v_{in}}{R_1} = i_{in}$$

and

$$v_o = -i_{in}R_F \qquad (4\text{-}23)$$

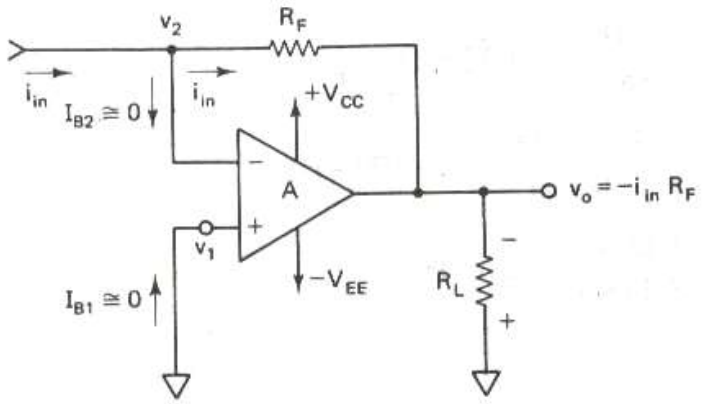


Figure 4–12 Current-to-voltage converter.

Inverter:
If we need an output signal equal in amplitude but opposite in phase to that of the input signal, we can use the inverter. The inverting amplifier of Figure 4-8 works as an inverter if $R_1 = R_F$. Since the inverter is a special case of the inverting amplifier, all the equations developed for the inverting amplifier are also applicable here. The equations can be applied by merely substituting (A/2) for (1 + AB), since B = 1/2.

TABLE 4-1 SUMMARY OF RESULTS OBTAINED FOR NONINVERTING AND INVERTING AMPLIFIERS

Parameter	Noninverting amplifier	Inverting amplifer
1. Voltage gain	$A_F = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1}$ (exact) $= \frac{A}{1 + AB}$ $= 1 + \frac{R_F}{R_1}$ (ideal)	$A_F = \frac{-AR_F}{R_1 + R_f + AR_1}$ (exact) $= \frac{-AK}{1 + AB}$, where $K = \frac{R_F}{R_1 + R_F}$ $= -\frac{R_F}{R_1}$ (ideal)
2. Gain of the feedback circuit	$B = \frac{R_1}{R_1 + R_F}$	$B = \frac{R_1}{R_1 + R_F}$
3. Input resistance	$R_{iF} = R_i(1 + AB)$	$R_{iF} = R_1 + \left(\frac{R_F}{1 + A} \Vert R_i\right)$
4. Output resistance	$R_{oF} = \frac{R_o}{1 + AB}$	$R_{oF} = \frac{R_o}{1 + AB}$
5. Bandwidth	$f_F = f_o(1 + AB)$ $f_F = \frac{\text{UGB}}{A_F}$	$f_F = f_o(1 + AB)$ $f_F = \frac{(\text{UGB})(K)}{A_F}$
6. Total output offset voltage	$V_{ooT} = \frac{\pm V_{sat}}{1 + AB}$	$V_{ooT} = \frac{\pm V_{sat}}{1 + AB}$

DIFFEREPETIA L AMPLIFIERS:

1. Differential amplifier with one op-amp
2. Differential amplifier with two op-amps
3. Differential amplifier with three op-amps

Differential Amplifier with One Op-Amp

Figure 4-14 shows the differential amplifier with one op-amp. We will analyze this circuit by deriving voltage gain and input resistance. A close examination of

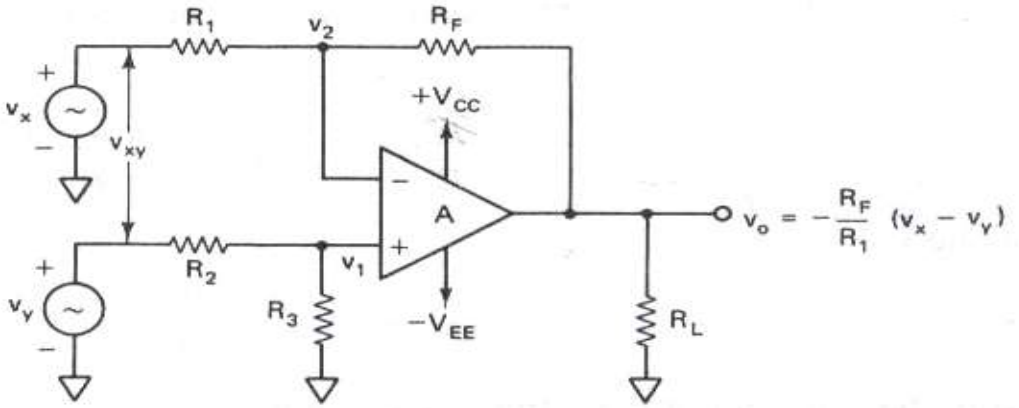


Figure 4–14 Differential amplifier with one op-amp. $R_1 = R_2$ and $R_F = R_3$.

Figure 4-14 reveals that differential amplifier is a combination of inverting and non-inverting amplifiers.

Voltage gain: The circuit in Figure 4-14 has two inputs, v_x and v_y; we will, therefore, use the superposition theorem in order to establish the relationship between inputs and output. When v_y = 0 V. the configuration becomes an inverting amplifier; hence the output due to v_x only is

$$v_{ox} = -\frac{R_F(v_x)}{R_1} \qquad (4\text{-}24a)$$

Similarly, when $v_x = 0$ V, the configuration is a noninverting amplifier having a voltage-divider network composed of R_2 and R_3 at the noninverting input. Therefore,

$$v_1 = \frac{R_3(v_y)}{R_2 + R_3}$$

and the output due to v_y then is

$$v_{oy} = \left(1 + \frac{R_F}{R_1}\right) v_1$$

That is,

$$v_{oy} = \frac{R_3}{R_2 + R_3}\left(\frac{R_1 + R_F}{R_1}\right) v_y$$

Since $R_1 = R_2$ and $R_F = R_3$,

$$v_{oy} = \frac{R_F(v_y)}{R_1} \qquad (4\text{-}24b)$$

Thus, from Equations (4-24a) and (4-24b), the net output voltage is

$$v_o = v_{ox} + v_{oy}$$

$$v_o = -\frac{R_F}{R_1}(v_x - v_y) = -\frac{R_F(v_{xy})}{R_1}$$

or the voltage gain

$$A_D = \frac{v_o}{v_{xy}} = -\frac{R_F}{R_1} \qquad (4\text{-}25)$$

Note that the gain of the differential amplifier is tne same as that of the inverting amplifier.

Input resistance: The input resistance R_{iF} of the differential amplifier is the resistance determined looking into either one of the two input terminals with the other grounded. Therefore, with v_y = 0 V, the circuit in Figure 4-14 is an inverting amplifier the input resistance of which is

$$R_{iFx} = R_1$$

Similarly, with v_x=0 V. the differential amplifier of Figure 4-14 becomes a non-inverting amplifier whose input resistance can then be written as

$$R_{iFy} = R_2 + R_3$$

Differential Amplifier with Two Op-Amps:

Voltage gain: A close examination of the circuit of Figure 4-16 shows that it is composed of two stages: (1) the non-inverting amplifier, and (2) the differential amplifier with unequal gains. By finding the gain of these two stages, we can obtain the overall gain of the circuit as follows:
The output v_z of the first stage is

$$v_z = \left(1 + \frac{R_3}{R_2}\right) v_y \qquad (4\text{-}27a)$$

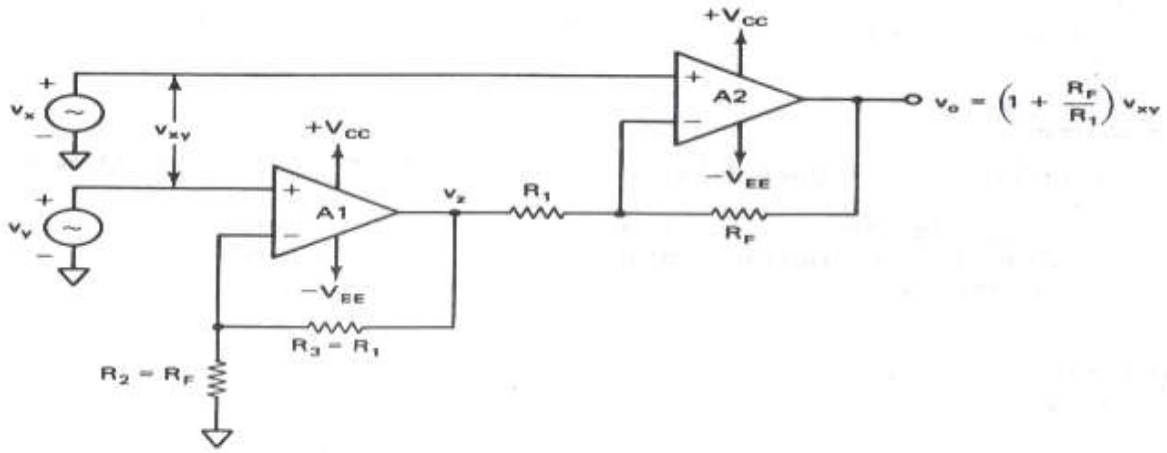


Figure 4–16 Differential amplifier with two op-amps.

By applying the superposition theorem to the second stage, we can obtain the output voltage:

$$v_o = -\frac{R_F(v_z)}{R_1} + \left(1 + \frac{R_F}{R_1}\right) v_x \qquad (4\text{-}27b)$$

Substituting the value of v_z from Equation (4-27a), we get

$$v_o = -\left(\frac{R_F}{R_1}\right)\left(1 + \frac{R_3}{R_2}\right) v_y + \left(1 + \frac{R_F}{R_1}\right) v_x$$

Since $R_1 = R_3$ and $R_F = R_2$,

$$v_o = \left(1 + \frac{R_F}{R_1}\right)(v_x - v_y)$$

Therefore,

$$A_D = \frac{v_o}{v_{xy}} = 1 + \frac{R_F}{R_1} \qquad (4\text{-}28)$$

where $v_{xy} = v_x - v_y$.

Input resistance: The input resistance R_{IF} of the differential amplifier is the resistance determined looking into either one of the two non-inverting input terminals with the other grounded (see Figure 4-16). Note, however, that the first stage (A1) is a non-inverting amplifier; therefore [from Equation (4-8)j, its input resistance is

$$R_{iFy} = R_i(1 + AB) \qquad (4\text{-}29a)$$

where R_i = open-loop input resistance of the op-amp

$$B = \frac{R_2}{R_2 + R_3}$$

Similarly, with v_y shorted to ground ($v_y = 0$ V), the second stage (A_2) also becomes a noninverting amplifier whose input resistance can then be written as

$$R_{iFx} = R_i(1 + AB) \qquad (4\text{-}29b)$$

where R_i = open-loop input resistance of the op-amp

$$B = \frac{R_1}{R_1 + R_F}$$

However, since $R_1 = R_3$ and $R_F = R_2$, the $R_{iFy} \neq R_{iFx}$. This is the drawback of the differential amplifier of Figure 4-16. Nevertheless, with proper selection of components, both R_{iFy} and R_{iFx} can be made much larger than the source resistances so that the loading of the input sources does not occur.

Differential Amplifier with Three Op-Amps:

Voltage gain: The differential op-amp of Figure 4-17 consists of two stages. The first stage is composed of op-amps A_1 and A_2, while the second stage is formed by op-amp A_3. Therefore, to find the overall voltage gain A_D of the amplifier, the voltage gain of each stage must be determined. To begin with, the first stage can be viewed as two separate differential amplifiers, as shown in Figure 4-18. The output voltages of these differential amplifiers can be found by applying the superposition theorem. For Figure 4-18(a),

$$v_z = \frac{2R_4 + R_5}{R_4 + R_5} v_x - \frac{R_4}{R_4 + R_5} v_t \qquad (4\text{-}30a)$$

and for Figure 4-18(b),

$$v_t = \frac{2R_4 + R_5}{R_4 + R_5} v_y - \frac{R_4}{R_4 + R_5} v_z \qquad (4\text{-}30b)$$

However, the output voltage of the first stage is

$$v_{zt} = v_z - v_t$$

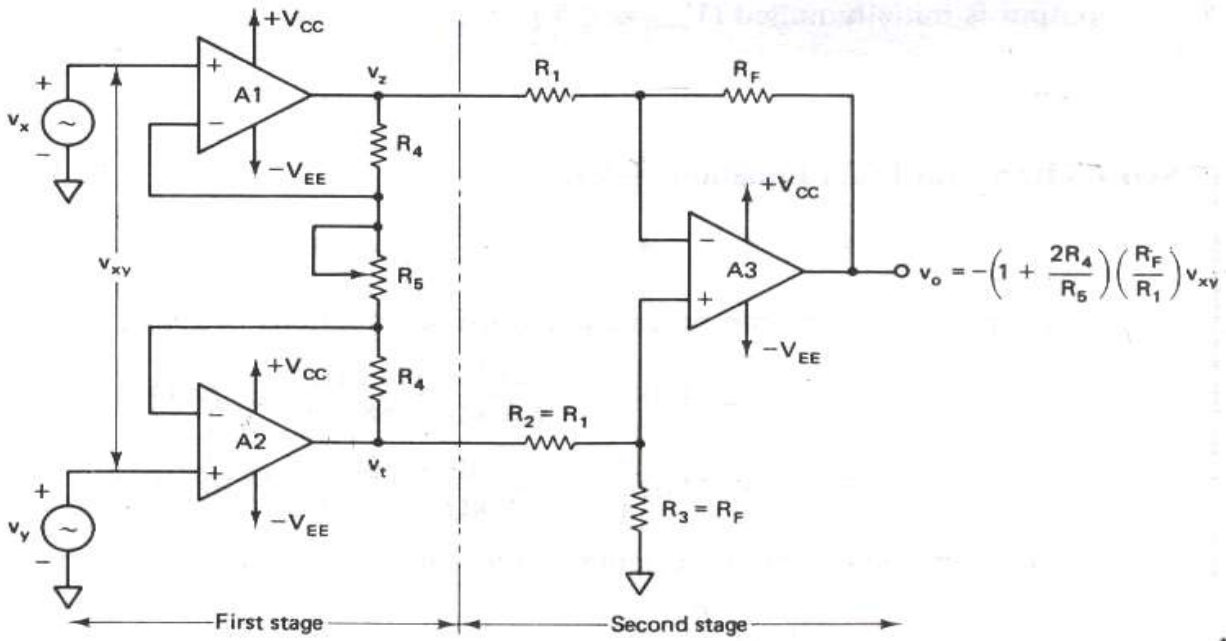


Figure 4–17 Differential amplifier with three op-amps.

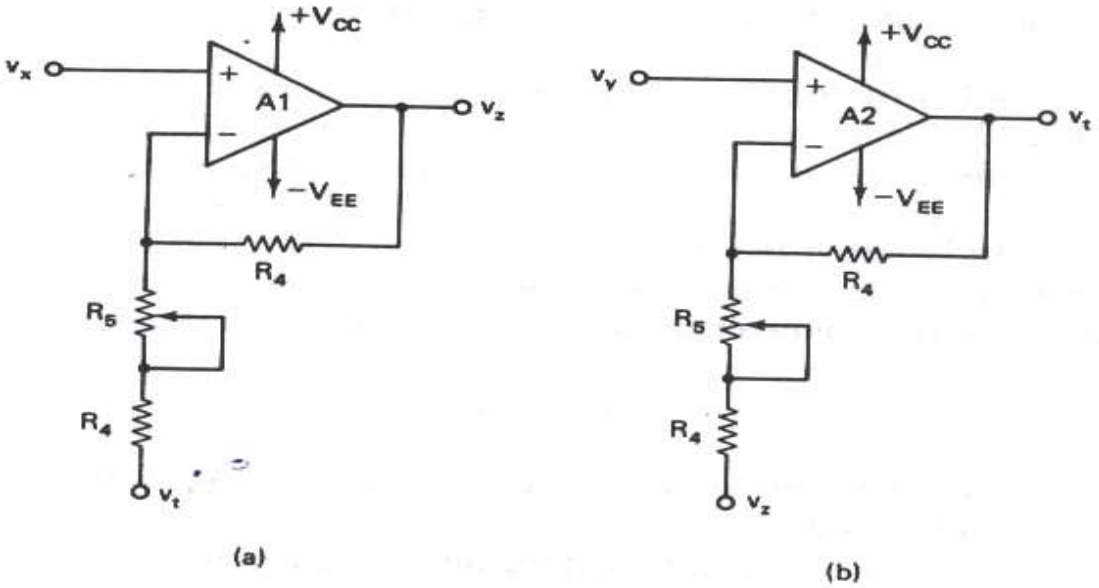


Figure 4–18 Deriving the voltage gain of the first stage of the circuit in Figure 4-17.

Therefore, from Equations (4-30a) and (4-30b),

$$v_{zt} = \frac{2R_4 + R_5}{R_4 + R_5}(v_x - v_y) + \frac{R_4}{R_4 + R_5}(v_z - v_t)$$

$$= \frac{2R_4 + R_5}{R_4 + R_5} v_{xy} + \frac{R_4}{R_4 + R_5} v_{zt}$$

Simplifying and rearranging, the voltage gain of the first stage is

$$\frac{v_{zt}}{v_{xy}} = \frac{2R_4 + R_5}{R_5} \tag{4-30c}$$

Next, using Equation (4-25), the gain of the second stage is

$$\frac{v_o}{v_{zt}} = -\frac{R_F}{R_1} \tag{4-30d}$$

Thus, from Equations (4-30c) and (4-30d), the overall voltage gain is

$$A_D = \frac{v_{zt}}{v_{xy}} \frac{v_o}{v_{zt}} = -\left(\frac{2R_4 + R_5}{R_5}\right) \frac{R_F}{R_1}$$

or

$$A_D = \frac{v_o}{v_{xy}} = -\left(1 + \frac{2R_4}{R_5}\right) \frac{R_F}{R_1} \tag{4-31}$$

Input resistance: The input resistance R_{iF} of the differential amplifier in Figure 4-17 is the same as the input resistance of the first stage, that is, the resistance determined at input v_x and v_y, looking into the circuit with the other terminal grounded.
In Figure 4-18a, for instance, when v_t, is reduced to zero, that is, when v_y, is grounded, the circuit is a non-inverting amplifier. Applying the concepts developed for the non-inverting amplifier, the input resistance determined at input v_x is

$$R_{iF} = R_i\left(1 + A \frac{R_4 + R_5}{2R_4 + R_5}\right) \tag{4-32}$$

Similarly, the input resistance determined at input v_y will be the same as that given in Equation (4-32).

DC and AC characteristics:

DC characteristics of Op-Amp

1. INPUT OFFSET VOLTAGE

Input offset voltage Vio is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero. Let us denote the output offset voltage due to input offset voltage Vio as Voo. The output offset voltage Voo is caused by mismatching between two input terminals. Even though all the components are integrated on the same chip, it is not possible to have two transistors in the input differential amplifier stage with exactly the same characteristics. This means that the collector currents in these two transistors are not equal, which causes a differential output voltage from the first stage. The output of first stage is amplified by following stages and possibly aggravated by more mismatching in them.

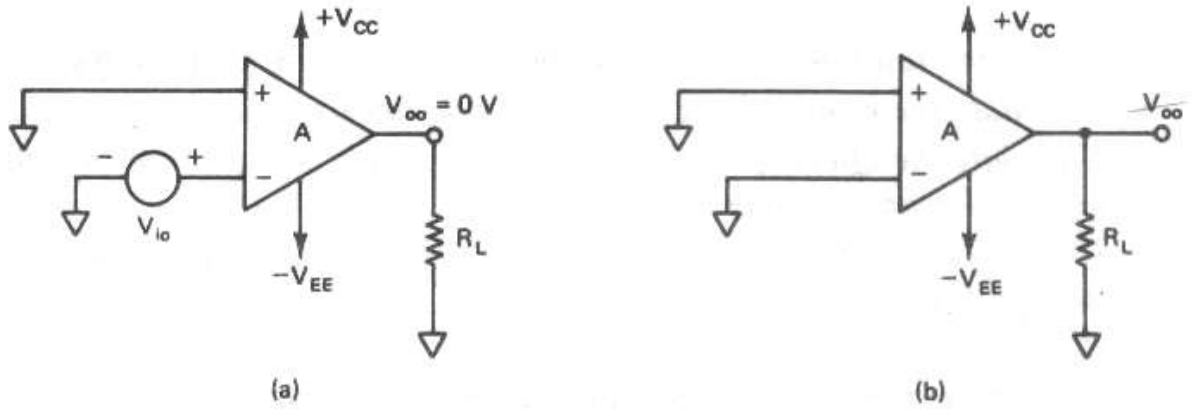


Figure 5–1 (a) Input offset voltage in an op-amp. (b) Output offset voltage in an op-amp.

Offset-Voltage Compensating Network Design

The op-amp with offset-voltage compensating network is shown in Figure *5-3.* The compensating network consists of potentiometer R_a and resistors R_b and R_e.

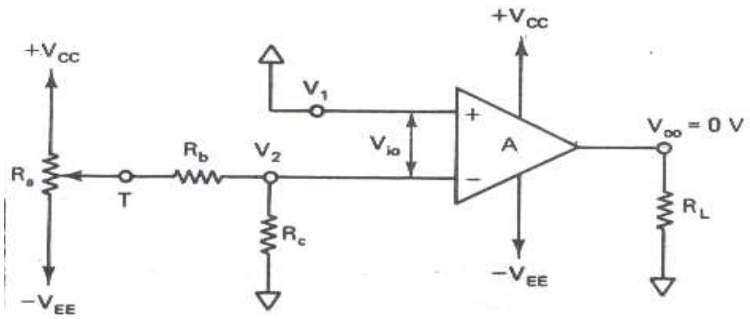
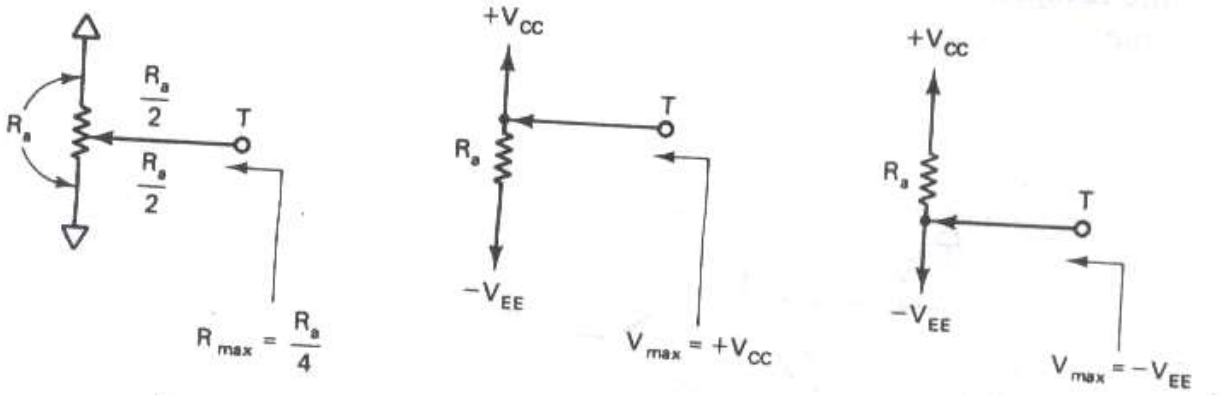


Figure 5–3 Op-amp with offset voltage-compensating network.

To establish a relationship between *Vio*, supply voltages, and the compensating components, first Thevenize the circuit, looking back into R_a from point *T*. The maximum Thevenin's equivalent resistance *Rmax*, occurs when the wiper is at the center of the Potentiometer, as shown in Figure.

$$R_{max} = \frac{R_a}{2} \parallel \frac{R_a}{2} = \frac{R_a}{4}.$$



Supply voltages V_{CC} and $-V_{EE}$ are equal *in* magnitude therefore; let us denote their magnitude by voltage *V*. Thus $V_{max} = V$.

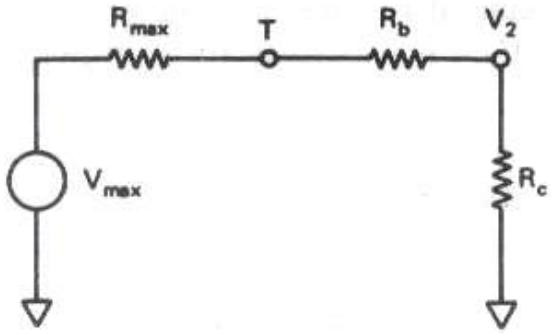


Figure 5–5 Compensating network with maximum Thévenin's equivalent resistance and voltage.

$$V_2 = \frac{R_c}{R_{max} + R_b + R_c} V_{max}$$

where *V2* has been expressed as a function of maximum Thevenin's voltage *Vmax* and maximum Thevenin's resistance, But the maximum value of *V2* can be equal to *Vio* since *V1 — V2 = Vio.* Thus Equation (5-1) becomes

$$V_{io} = \frac{R_c}{R_{max} + R_b + R_c} V_{max}$$

Assume $R_b > R_{max} > R_c$, where $R_{max} = R_a/4$. Using this assumption $R_{max}+R_b+R_c=R_b$

Therefore

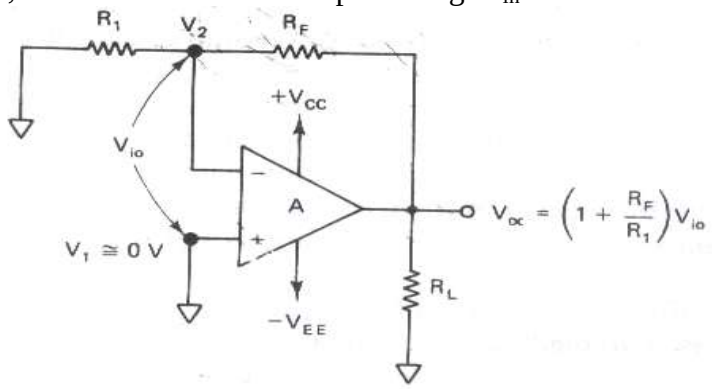
$$V_{io} = \frac{R_c V_{max}}{R_b}$$

where

$$V_{max} = V = |V_{CC}| = |-V_{EE}|$$

$$V_{io} = \frac{R_c V}{R_b}$$

Let us now examine the effect of *Vio* in amplifiers with feedback. The non-inverting and inverting amplifiers with feedback are shown in Figure. To determine the effect of Vio, in each case, we have to reduce the input voltage v_{in} to zero.



Closed-loop non-inverting or inverting amplifier with $v_{in} = 0$ V.

With vin reduced to zero, the circuits of both non-inverting and inverting amplifiers are the same as the circuit in Figure. The internal resistance Rin of the input signal voltage is negligibly small. In the figure, the non-inverting input terminal is connected to ground; therefore, assume voltage *V1* at input terminal to be zero. The voltageV2 at the inverting input terminal can be determined by applying the voltage-divider rule:

$$V_2 = \frac{R_1 V_{oo}}{R_1 + R_F}$$

Therefore,

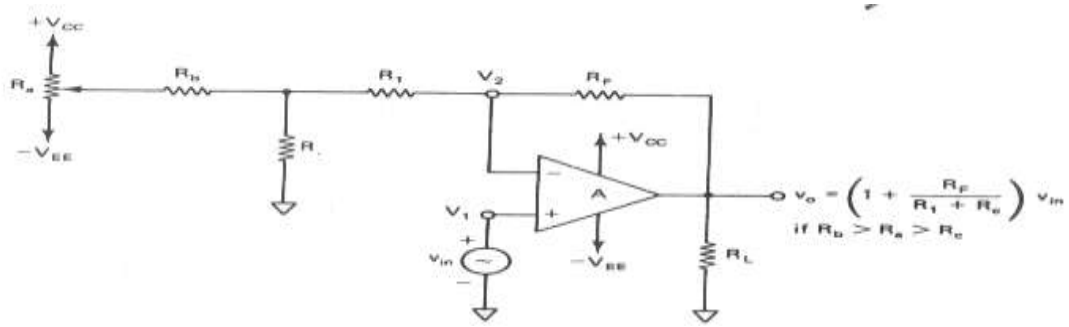
$$V_{oo} = \frac{R_1 + R_F}{R_1} V_2$$

Since $V_{io} = |V_1 - V_2|$ and $V_1 = 0$ V,

$$V_{io} = |0 - V_2| = V_2$$

Therefore,

$$V_{oo} = \left(1 + \frac{R_F}{R_1}\right) V_{io} = (A_{oo})\, V_{io}$$



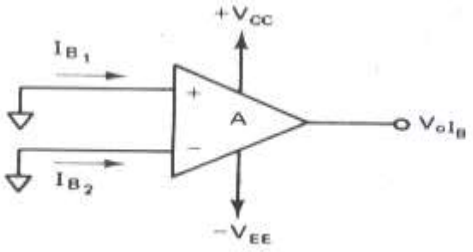
Compensated non-inverting amplifier with feedback

2 .INPUT BIAS CURRENT

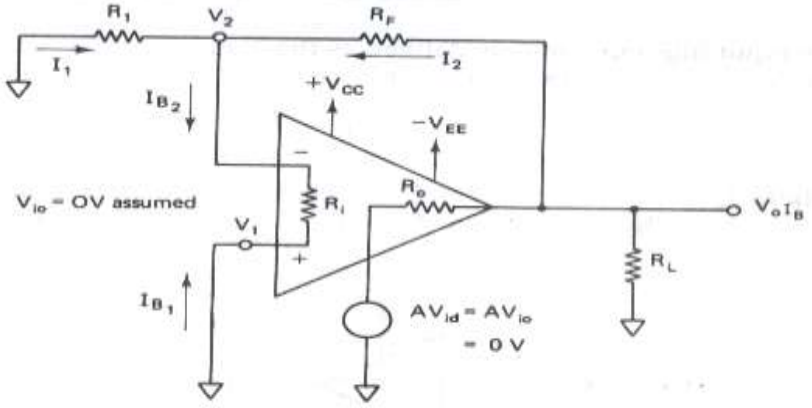
An input bias cuent I_B is defined as the average of the two input bias currents, $I_{B1}$and I_{B2}, as shown in Figure that is,

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where I_{B1} = dc bias current flowing into the noninverting input
I_{B2} = dc bias current flowing into the inverting input



$I_B = I_{B1} = I_{B2}$ Obtaining the expression for the output offset voltage caused by the input bias current I_B in the inverting and non-inverting amplifiers and then devise some scheme to eliminate or minimize it.



Output offset voltage due to input bias current in a noninverting or inverting amplifier.

In the figure, the input bias currents '81 and *1* are flowing into the non-inverting and inverting input leads, respectively. The non-inverting terminal is connected to ground; therefore, the voltage V_1 = 0 V. The controlled voltage source *A Vio* =0 V since Vio= 0 V is assumed. With output resistance Ro is negligibly small, the right end of R_F is essentially at ground potential; that is, resistors R_1, and R_F are in parallel and the bias current *I,* flows through them. Therefore, the voltage at the inverting terminal is

$$V_2 = (R_1 \| R_F) I_{B2} \tag{5-11}$$

$$V_2 = \frac{R_1 R_F}{R_1 + R_F} I_{B2} \tag{5-12}$$

Writing a node voltage equation for node V_2, we get

$$I_1 + I_2 = I_{B2}$$

$$\frac{0 - V_2}{R_1} + \frac{V_{oI_B} - V_2}{R_F} = \frac{V_2}{R_i} \tag{5-13}$$

where V_{oI_B} = output offset voltage due to input bias current
R_i = input resistance of the op-amp (see Figure 5-16)
Rearranging Equation (5-13), we get

$$\frac{V_{oI_B}}{R_F} = V_2 \left(\frac{1}{R_1} + \frac{1}{R_F} + \frac{1}{R_i} \right)$$

Since R_i is extremely high (ideally ∞), $1/R_i \cong 0$ siemens. Therefore,

$$\frac{V_{oI_B}}{R_F} = V_2 \frac{R_1 + R_F}{R_1 R_F} \tag{5-14}$$

Substituting in Equation (5-14) the value of V_2 from Equation (5-12), we get

$$V_{oI_B} = \frac{R_1 R_F I_{B2}}{R_1 + R_F} \left(\frac{R_1 + R_F}{R_1} \right) \tag{5-15}$$

$$V_{oI_B} = R_F I_{B2}$$

From Equation

$$V_{oI_B} = R_F I_B \tag{5-16}$$

According to Equation (5-16), the amount of output offset voltage V_{oI_B} is a function of feedback resistor R_F for a specified value of input bias current I_B. The amount of V_{oI_B} can be increased by the use of relatively large feedback resistors. Therefore, the use of small feedback resistors is recommended.

To eliminate or reduce the output offset voltage V_{oI_B} due to input bias current I_B, we have to devise some scheme at the input by which voltage V_1 can be made equal to V_2. In other words, if voltages V_1 and V_2 caused by the currents I_{B1} and I_{B2} can be made equal, there will be no output voltage V_{oI_B}. From Equation (5-12), we have

$$V_2 = R_p I_{B2} \tag{5-17}$$

where

$$R_p = \frac{R_1 R_F}{R_1 + R_F}$$

Equation (5-17) implies that we must express voltage V_1 at the noninverting input terminal as a function of I_{B1} and some specific resistor R_{OM}. This can be accomplished as follows. The input bias current I_{B1} does not produce any voltage at the noninverting input terminal because this terminal is directly connected to ground (see Figure 5-16). If we could connect the proper value of resistor R_{OM} in the noninverting terminal, the voltage V_1 would be

$$V_1 = R_{OM} I_{B1} \tag{5-18}$$

To have voltage V_1 equal to V_2, the right-hand sides of Equations (5-17) and (5-18) must be equal; that is,

$$R_p I_{B2} = R_{OM} I_{B1} \tag{5-19}$$

Now if the currents I_{B1} and I_{B2} are equal, Equation (5-19) implies that

$$R_p = R_{OM} \tag{5-20}$$

or

$$\frac{R_1 R_F}{R_1 + R_F} = R_{OM} \tag{5-21}$$

Thus the proper value required of an R_{OM} resistor connected in the noninverting terminal is the parallel combination of resistors R_1 and R_F. However, the use of R_{OM} may not completely eliminate the output offset voltage V_{oI_B} because the currents I_{B1} and I_{B2} are not exactly equal. Nevertheless, the use of R_{OM} will minimize the amount of output offset voltage V_{oI_B}; therefore, the R_{OM} resistor is referred to as the *offset minimizing resistor* (see Figure 5-17).

Note that if we reduce both the inputs to zero (that is, $v_{in\,1} = v_{in\,2} = 0$ V) in the closed-loop differential amplifier, the resulting circuit becomes the same as in Figure 5-17. This means that there is no need to use a separate resistor R_{OM} in the

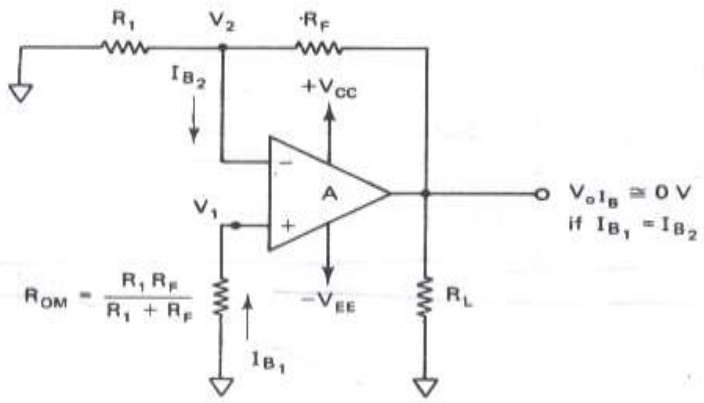


Figure 5–17 R_{OM} reduces the output offset voltage V_{oI_B} caused by the input bias current I_B.

3. INPUT OFFSET CURRENT

The input offset current I_{io} is defined as the algebraic difference between two input bias currents I_{B1} and I_{B2}. In equation form,

$$I_{io} = |I_{B1} - I_{B2}| \tag{5-22}$$

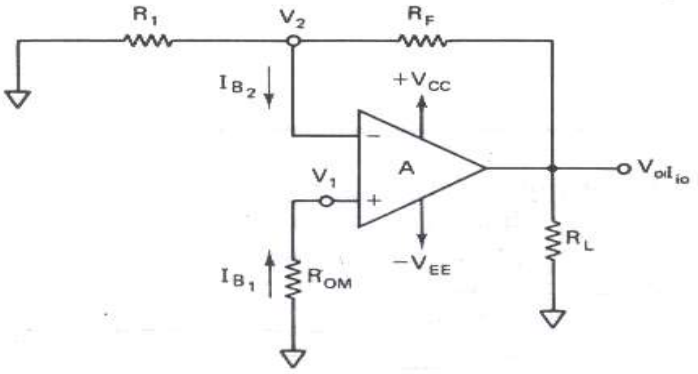


Figure 5–20 Output offset voltage $V_{oI_{io}}$ caused by the input offset current I_{io} in an inverting or noninverting amplifier.

Referring to Figure 5-20, we will express the voltages V_1 and V_2 as a function of I_{B1} and I_{B2}, for given values of R_1 and R_F, as follows:

$$V_1 = R_{OM} I_{B1} \tag{5-18}$$

$$V_2 = R_p I_{B2} \tag{5-17}$$

where

$$R_{OM} = R_p = \frac{R_1 R_F}{R_1 + R_F}$$

Applying the superposition theorem, we will now find the output offset voltage due to V_1 and V_2 in terms of I_{B1}, I_{B2}, and R_F. We know, from Equation (5-15), that

$$V_{oI_{B2}} = -R_F I_{B2}$$

Here the negative sign is used because V_2 is the voltage at the inverting input terminal. This output offset voltage $V_{oI_{B2}}$ is due to voltage V_2 only in terms of I_{B2} and R_F. Similarly, the output offset voltage $V_{oI_{B1}}$ due to V_1 only in terms of I_{B1} and R_F can be obtained as follows:

$$V_{oI_{B1}} = V_1\left(1 + \frac{R_F}{R_1}\right) \tag{5-23}$$

where V_1 = voltage at the noninverting input terminal

$\left(1 + \frac{R_F}{R_1}\right)$ = gain of the noninverting amplifier

Substituting in Equation (5-23) the value of V_1 from Equation (5-18), we get

$$V_{oI_{B1}} = R_{OM} I_{B1} \left(1 + \frac{R_F}{R_1}\right) \tag{5-24}$$

$$= \frac{R_1 R_F}{R_1 + R_F} I_{B1} \frac{R_1 + R_F}{R_1}$$

$$V_{oI_{B1}} = R_F I_{B1} \tag{5-25}$$

Therefore, the maximum magnitude of the output offset voltage due to I_{B1} and I_{B2} is

$$V_{oI_{B1}} + V_{oI_{B2}} = R_F I_{B1} - R_F I_{B2}$$

$$= R_F (I_{B1} - I_{B2}) \tag{5-26}$$

$$V_{oI_{io}} = R_F (I_{io})$$

TOTAL OUTPUT OFFSET VOLTAGE

We know that in a circuit like the one in Figure 5-19, the output offset voltage V_{oo} caused by V_{io} could be either positive or negative with respect to ground. Similarly, the output offset voltage V_{oI_B} caused by I_B could also be either positive or negative with respect to ground. If these output offset voltages are of different polarities, the resultant output offset will be very little. On the other hand, if both of these output offset voltages are of the same polarity, the maximum amplitude of the total output offset would be

$$V_{ooT} = V_{oo} + V_{oI_B}$$

$$V_{ooT} = \left(1 + \frac{R_F}{R_1}\right) V_{io} + (R_F) I_B \tag{5-27}$$

By the same token, in a circuit such as that in Figure 5-21, the total output offset voltage V_{ooT} can be given by the expression

$$V_{ooT} = V_{oo} + V_{oI_{io}}$$

$$V_{ooT} = \left(1 + \frac{R_F}{R_1}\right) V_{io} + (R_F) I_{io} \tag{5-28}$$

THERMAL DRIFT

In previous sections we learned to compensate for the effects of input offset voltage and input bias currents. In our discussion so far, we have assumed that the parameters V_{io}, I_B, and I_{io} are constant for a given op-amp. However, in practice, the values of V_{io}, I_B, and I_{io} vary with:

1. Change in temperature
2. Change in supply voltages: $+V_{CC}$ and $-V_{EE}$
3. Time

The average rate of change of input offset voltage per unit change in temperature is called *thermal voltage drift* and is denoted by $\Delta V_{io}/\Delta T$. It is expressed in μV/°C. By the same concept, we can also define the thermal drift in the input offset current and input bias current as follows:

$\frac{\Delta I_{io}}{\Delta T}$ = thermal drift in the input offset current (pA/°C)

$\frac{\Delta I_B}{\Delta T}$ = thermal drift in the input bias current (pA/°C)

$\frac{\Delta V_{io}}{\Delta T}$ = thermal voltage drift

$\frac{\Delta I_{io}}{\Delta T}$ = thermal current drift

Error Voltage

Let us define this maximum possible change in total output offset voltage ΔV_{ooT} as the *error voltage* and denote it by E_v.

$$\Delta V_{ooT} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{\Delta V_{io}}{\Delta T}\right)\Delta T + (R_F)\left(\frac{\Delta I_{io}}{\Delta T}\right)\Delta T$$

$$E_v = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{\Delta V_{io}}{\Delta T}\right)\Delta T + (R_F)\left(\frac{\Delta I_{io}}{\Delta T}\right)\Delta T \qquad (5\text{-}30)$$

SVRR: It is defined as the

$$20 \log\left(\frac{1}{\text{SVRR}}\right) = 20 \log\left(\frac{1}{\Delta V_{io}/\Delta V}\right) = 20 \log\left(\frac{1}{150\ \mu\text{V/V}}\right) = 20 \log\left(\frac{10^6}{150}\right)$$

$$= 76.48 \text{ dB}$$

Similarly, an SVRR of 96 dB is equivalent to 15.85 μV/V as follows.

$$20 \log(1/\text{SVRR}) = 96 \text{ dB},$$

$$\log\left(\frac{1}{\text{SVRR}}\right) = \frac{96}{20}$$

$$\frac{1}{\text{SVRR}} = 10^{4.8}$$

$$\text{SVRR} = \frac{1}{10^{4.8}}$$

$$= 15.85\ \mu\text{V/V}$$

CMRR

Generally, it can be defined as the ratio of the differential gain A_D to the common-mode gain A_{cm}, that is,

$$\text{CMRR} = \frac{A_D}{A_{cm}} \tag{5-38}$$

Note that, in Figure 5-33(a), A_D is equal to the internal gain A of the op-amp.

The CMRR can also be expressed as the ratio of the change in input offset voltage to the total change in common-mode voltage. Thus

$$\text{CMRR} = \frac{V_{io}}{v_{cm}} \tag{5-39}$$

From Equations (5-37) and (5-38), we can then establish the relationship between the v_{ocm} and CMRR:

$$\text{CMRR} = \frac{A_D}{A_{cm}} = \frac{A_D}{v_{ocm}/v_{cm}}$$

$$= \frac{A_D v_{cm}}{v_{ocm}} \tag{5-40}$$

$$v_{ocm} = \frac{A_D v_{cm}}{\text{CMRR}}$$

AC CHARACTERISTICS OF OP-AMP

Two major sources are responsible for capacitive effects on op-amp.

1. *Physical characteristics of semiconductor devices*. Recall that op-amps are composed of BJTs and FETs which contain junction capacitors. These junction capacitors are very small (on the order of picofarads) and act as open circuits at low frequencies but take finite values at higher frequencies. In fact, as frequency increases, the reactances of these capacitors decrease.
2. The *internal construction* of the op-amp is a second source of capacitive effects. In op-amps a number of transistors as well as resistors and sometimes a capacitor are integrated on the same material, called a *substrate*. In fact, the substrate acts as an insulator and helps to separate these components. The various components are connected by conducting paths, and the paths are separated by insulators. However, whenever two conducting paths are separated by an insulator, it acts as a capacitor. This means that because of its construction the op-amp may contain a number of such stray capacitors.

The cumulative effect of these capacitors due to the characteristics of semiconductor devices and the internal construction of the op-amp causes the gain to decrease as the frequency increases.

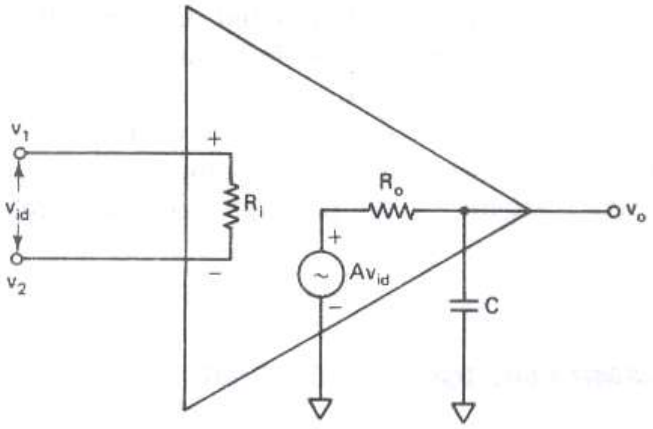


Figure High-frequency model of an op-amp with single break frequency.

OPEN-LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

Let us now obtain an expression for the gain as a function of frequency. From Figure 6-2, using a voltage-divider rule, we get

$$v_o = \frac{-jX_C}{R_o - jX_C}(Av_{id})$$

Since $-j = 1/j$ and $X_C = 1/2\pi fC$,

$$v_o = \frac{1/j2\pi fC}{R_o + 1/j2\pi fC}(Av_{id})$$

$$= \frac{Av_{id}}{1 + j2\pi fR_oC}$$

Hence the open-loop voltage gain is

$$A_{OL}(f) = \frac{(v_o)}{(v_{id})}$$

$$A_{OL}(f) = \frac{A}{1 + j2\pi fR_oC}$$

Let $f_o = 1/2\pi R_oC$; then

$$A_{OL}(f) = \frac{A}{1 + j(f/f_o)}$$

where $A_{OL}(f)$ = open-loop voltage gain as a function of frequency
A = gain of the op-amp at 0 Hz (dc)
f = operating frequency (Hz)
f_o = break frequency of the op-amp (Hz)

Note that the break frequency f_o depends on the value of C and on output resistance R_o. Therefore, f_o is fixed for a given op-amp.

The open-loop gain magnitude is

$$|A_{OL}(f)| = \frac{A}{\sqrt{1 + (f/f_o)^2}}$$

and phase angle

$$\phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$$

CIRCUIT STABILITY

A circuit or a group of circuits connected together as a system is said to be stable if its output reaches a fixed value in a finite time. On the other hand, a circuit/system is said to be unstable if its output increases with time instead of achieving a fixed value. In fact, the output keeps on increasing until the system breaks down. Therefore, unstable systems are impractical and need to be made stable.

Any system whose stability is to be determined can be represented by the block diagram of Figure 4-3. In fact, in control system analysis the block diagram of Figure 4-3 is the *standard* form of representing a system. The standard block diagram is composed of two blocks, as shown in Figure 6-7. The block between the output and the input is referred to as the *forward block* (a block in the forward path), and the block between the output signal and the feedback signal is referred to as the *feedback block* (a block in the feedback path). The content of each block commonly referred to as the *transfer function* (in control system theory) depends on the complexity of a system.

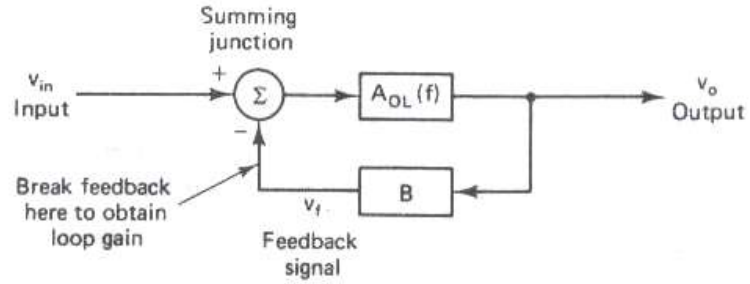


Figure A typical closed-loop system (noninverting amplifier).

$$A_{OL}(f) = \frac{v_o}{v_{in}} \qquad \text{if } v_f = 0$$

where $A_{OL}(f)$ = open-loop voltage gain

Similarly the closed-loop gain A_F is given by

$$A_F = \frac{v_o}{v_{in}}$$

$$A_F = \frac{A_{OL}}{1 + (A_{OL})(B)}$$

Once the magnitude versus frequency and the phase angle versus frequency plots are drawn, system stability may be determined as follows:

Method 1.

Determine the phase angle when the magnitude of (A_{OL}) (B) is 0 dB or 1. If the phase angle is $> -180°$, the system is stable. However, for some systems the magnitude may never be 0 dB; in that case, method 2 must be used to determine the system stability.

Method 2.

Determine the magnitude of (A_{OL}) (B) when the phase angle is $-180°$. If the magnitude is negative decibels, then the system is stable. However, sometimes the phase angle of a system may never reach $-180°$; under such conditions, method 1 must be used to determine the system stability.

SLEW RATE: It is the maximum rate of change of output voltage with respect to time,usually specified in V/μs

Slew Rate Equation

Since the slew rate on a data sheet is generally listed for a unity gain, let us consider the voltage follower shown in Figure 6-11. Furthermore, let us assume that the input is a large-amplitude and high-frequency sine wave. The equation for the sine wave is

$$v_{in} = V_P \sin \omega t$$

or

$$v_o = V_P \sin \omega t$$

The rate of change of the output is

$$\frac{dv_o}{dt} = V_P \omega \cos \omega t$$

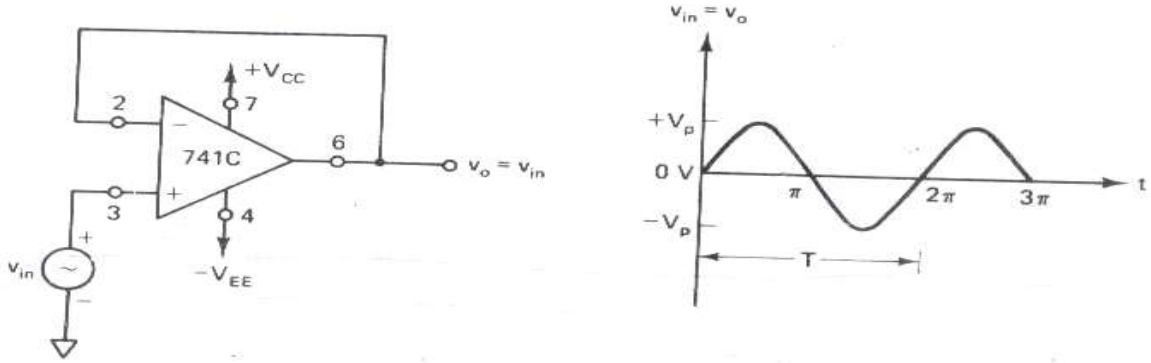
and the maximum rate of change of the output occurs when $\cos \omega t = 1$. That is,

$$\left.\frac{dv_o}{dt}\right|_{max} = V_P \omega$$

$$SR = 2\pi f V_P \quad \text{V/s}$$

$$= \frac{2\pi f V_P}{10^6} \quad \text{V/}\mu\text{s}$$

where SR = slew rate (V/μs)
f = input frequency (Hz)
V_P = peak value of the output sine wave (volts)



Deriving the slew rate equation.

Effect of Slew Rate in Applications

The 741C has a typical slew rate of 0.5 V/μs; therefore

$$\frac{28 \text{ V}}{0.5 \text{ V}/\mu\text{s}} = 56\ \mu\text{s}$$

must be the minimum time between the two zero crossings. Hence the maximum input frequency f_{max} at which the output will be distorted is given by

$$f_{max} = \frac{1}{(2)(56\ \mu\text{s})} = 8.93 \text{ kHz}$$

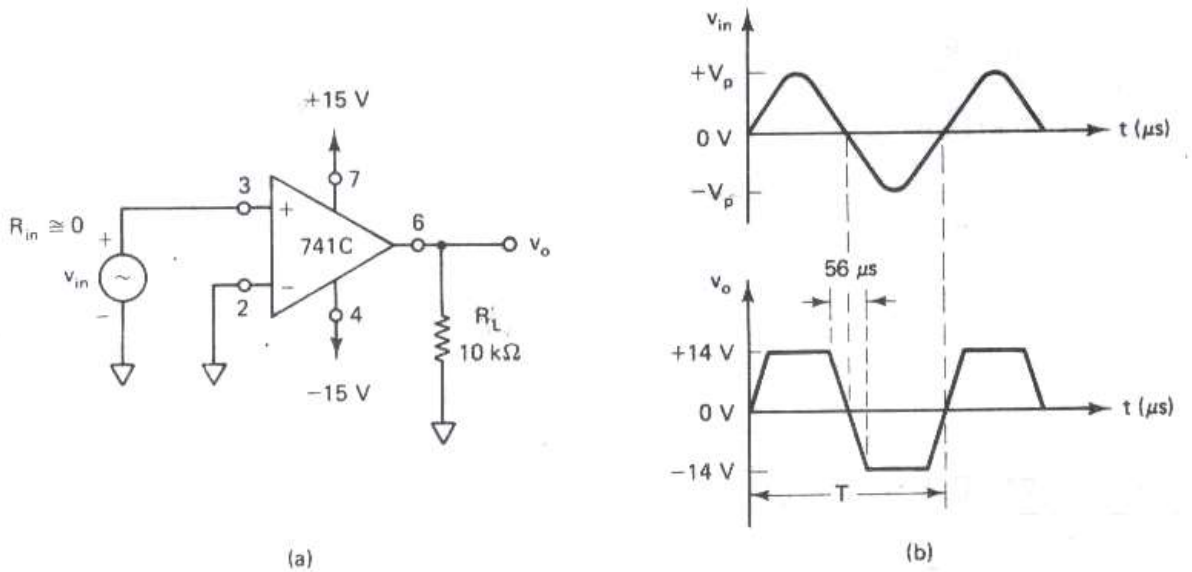


Figure (a) Open-loop configuration using the 741C. (b) Input and output waveforms.