

LINEAR IC's and APPLICATION'S

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OPERATIONAL AMPLIFIER FUNDAMENTALS

❖ Definition of operational amplifier (OP-AMP)

Op-Amp is a directly coupled high gain IC amplifier with two high impedance I/P terminals and one low output impedance. The op-amp consists of a differential amplifier input stage and an emitter follower output stage.

❖ Op-Amp Symbol :

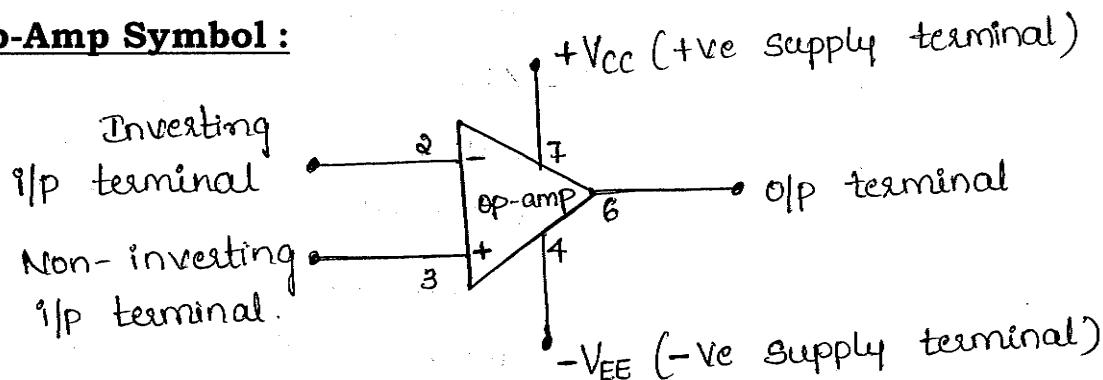


fig 1 @ : symbol.

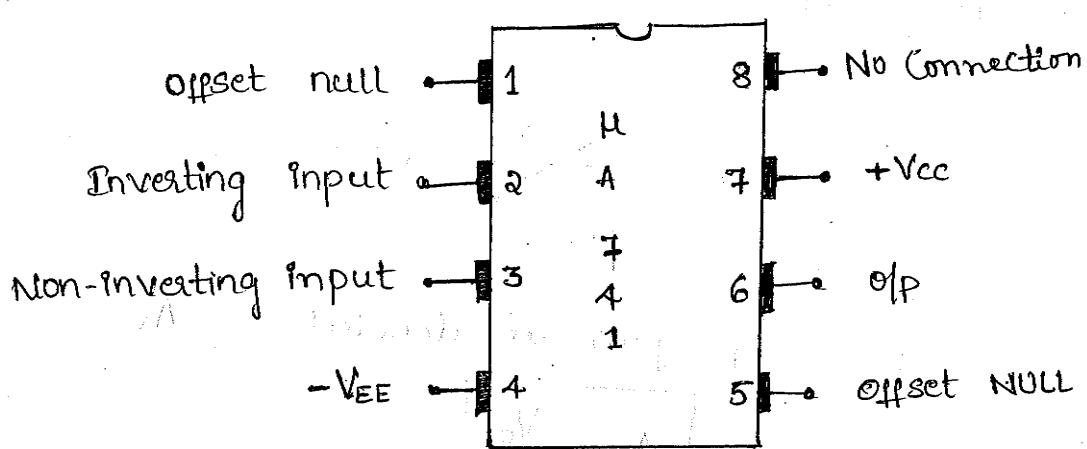


fig 1 ⑥ : Op-Amp IC



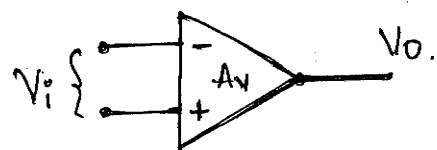
fig 1. (a) shows the symbol of op-amp.
It consists of 5 - terminals as shown above.

NOTE :-

The letter prefix code identifies the manufacturer as shown in table below:

Letter prefix	Manufacturer
AD.	Analog devices.
CA.	RCA.
LM	National semiconductor corporation.
MC	Motorola.
SN	Texas instruments.
HA	Fair child corporation.

OPEN - LOOP AMPLIFIER :-



open - Loop gain is denoted by A_v .

i.e

$$A_v = \frac{V_o}{V_i}$$



MODES OF OPERATION OF OP-AMP :-

1) Inverting Mode :-

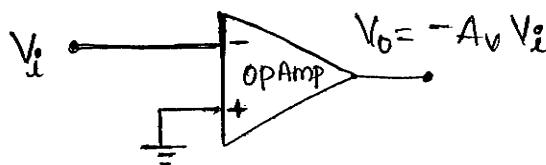
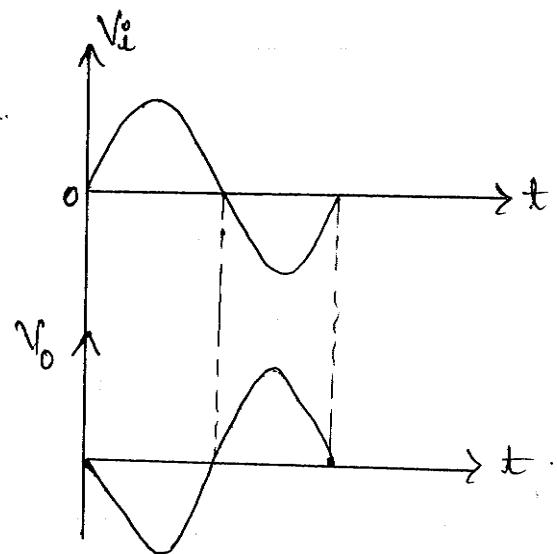


fig : INV Mode.



In. INV mode, the AIP voltage V_i is applied to the INV AIP terminal & the Non-INV AIP terminal is grounded. The OIP signal of the INV amplifier is 180° out of phase with the applied AIP signal.

thus OIP voltage

$$V_o = -A_v V_i$$

2) Non-Inverting Mode :-

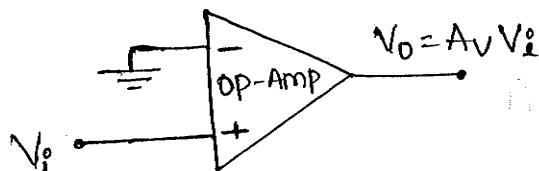
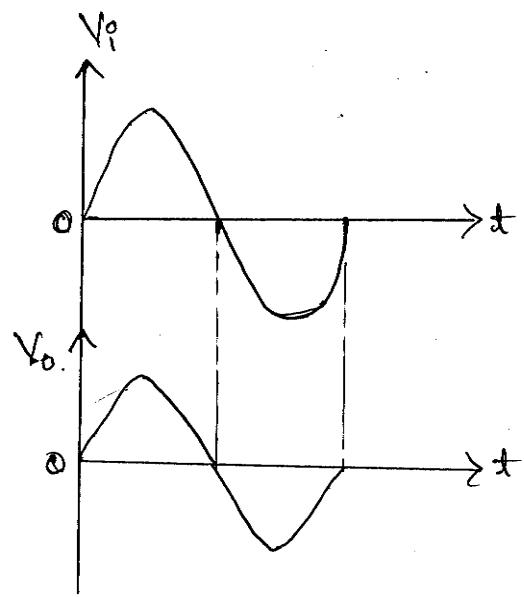


fig : Non-INV mode.



In Non-INV mode, the IIP voltage is applied to the Non-INV IIP terminal and the INV IIP terminal is grounded. The OLP signal of the Non-INV amplifier is in-phase with the applied IIP signal.

Thus OLP voltage

$$V_o = A_v V_i$$

3) Differential Mode :-

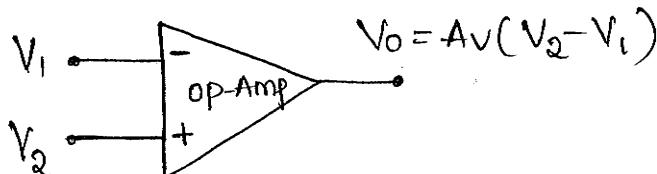


fig : Differential Mode.

$$\therefore A_v = \frac{V_o}{V_i}$$

where $V_i = (V_2 - V_1)$

$$V_o = A_v V_i$$

$$V_o = A_v (V_2 - V_1)$$

In differential mode, the voltages V_1 & V_2 are applied to the inverting and Non-inverting IIP terminals respectively.

The OLP voltage is proportional to the difference between V_2 & V_1 & hence the name differential mode.

BLOCK DIAGRAM OF OP-AMP :-

- * Explain the block-diagram of an operational amplifier with the help of a diagram indicating the various building blocks

Jan-10, 8M.





fig ① : Internal block schematic of op-amp.

An op-amp is basically a difference amplifier having very high gain, directly coupled amplifier with high IIP impedance & low - OLP impedance.

fig ① shows the block diagram of IC op-Amp.

The op-Amp basically consists of 4-stages as shown in fig ①.

i) IIP stage :-

The IIP stage requires two IIP terminals with high IIP impedance & low OLP impedance. These requirements are achieved by using dual-IIP, balanced OLP differential amplifier.

The function of a differential amplifier is to amplify the difference between the two IIP signals.

This stage provides a major part of the voltage gain.

ii) Intermediate stage :-

The OLP of the IIP stage is directly fed to the intermediate stage. This is another differential amplifier with dual IIP, unbalanced OLP (i.e. single ended OLP).



(The IIP stage alone cannot provide such a high gain).

The main function of the intermediate stage is to provide an additional voltage gain required. practically, the intermediate stage is a chain of cascaded amplifiers called Multistage amplifiers.

iii) Level-shifting stage :-

since the IIP stage amplifier & the intermediate stage amplifiers are directly coupled the dc voltage at the OIP of the intermediate stage tends to rise above the ground, which is not desirable.

To bring down this dc voltage to zero, a level shifter is employed. This is usually an emitter follower. which also acts as a buffer with very large IIP resistance & low OIP resistance.

iv) OIP stage :-

The OIP stage consists of a complementary push-pull amplifier, which helps to increase the OIP voltage swing & the current supplying capacity of the op-Amp.



Ideal characteristics of an Op-Amp :-

An ideal op-amp exhibits the following characteristics :-

- 1) The voltage gain is infinite ($A_v = \infty$)
- 2) The IIP impedance is infinite
- 3) The OIP impedance is zero.
- 4) The bandwidth is infinite
- 5) There is no change in the characteristic features with change of temperature.
- 6) When equal voltages are applied at the two input terminals, the oip is zero.

BASIC OPERATIONAL AMPLIFIER CIRCUIT :-

- * With a neat circuit diagram explain basic operational amplifier circuit.

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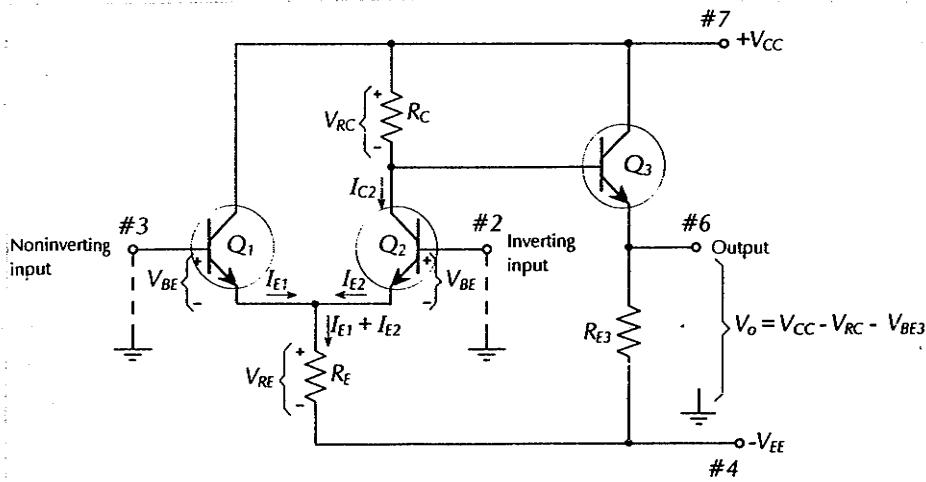


Figure 1 The basic circuit of an operational amplifier has a differential amplifier input stage and an emitter follower output.



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fig ① : Basic circuit of an operational amplifier has a differential amplifier i/p stage & an emitter follower o/p.

The basic circuit of an op-amp is shown in fig ①.

- * It is provided with $+V_{CC}$ & $-V_{EE}$ supply voltages and the two i/p terminals are grounded. Transistors Q_1 & Q_2 forms a differential amplifier.
- * When a difference i/p voltage is applied to the base of Q_1 & Q_2 , it produces a voltage change at the collector of Q_2 . Transistor Q_3 acts as an emitter follower to provide a low o/p impedance.

The dc o/p voltage at pin 6 is
(applying KVL from V_{CC} , R_C , Q_3 base & o/p we get)

$$V_{CC} - I_{C2} R_C - V_{BE3} - V_o = 0$$

$$V_o = V_{CC} - I_{C2} R_C - V_{BE3}.$$

- * Assuming that Q_1 & Q_2 are matched (identical) transistors, which provides equal V_{BE} levels & current gains.

With both transistors base at ground level, the emitter currents I_{E1} & I_{E2} are equal & flow through common emitter resistor ' R_E '

\therefore The total emitter current is given by,

$$I_{E1} + I_{E2} = \frac{V_{RE}}{R_E}$$



* Applying KVL from base of Q_2 to $-V_{EE}$ supply.

$$-V_{BE} - (I_{E1} + I_{E2})R_E + V_{EE} = 0.$$

$$(I_{E1} + I_{E2})R_E = V_{EE} - V_{BE}.$$

$$(I_{E1} + I_{E2}) = \frac{V_{EE} - V_{BE}}{R_E}$$

NOTE :-

i) $I_{E1} = I_{E2}$.

ii) $V_{BE1} = V_{BE2} = V_{BE3}$.

iii) operating point values $\rightarrow I_{CQ}$ & V_{CEQ} .

Here *

$$I_E \approx I_C \approx I_{CQ}.$$

* The collector voltage of Q_2 is given by

$$V_C = V_{CC} - I_C R_C$$

WKT $V_{CE} = V_C - V_E$

& $V_{BE} = V_B - V_E$

as $V_B = 0$.

$$V_{BE} = -V_E$$

$$V_E = -V_{BE}$$

$$V_{CE} = V_C - V_E$$

$$= V_{CC} - I_C R_C - (-V_{BE})$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C$$



FORMULAE

1) operating point value ① $I_{CQ} = I_E$

② $V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$

3) $V_o = V_{CC} - I_{C2} R_C - V_{BE}$

3) $I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E}$

Problems :

1. calculate the o/p voltage for basic op-amp.

Given $V_{CC} = +10V$, $V_{EE} = -10V$, $R_E = 4.7k\Omega$,
 $R_C = 6.8k\Omega$ & all transistors have $V_{BE} = 0.7V$.

SOL%:-

Given :- $V_{CC} = 10V$, $V_{EE} = -10V$, $R_E = 4.7k\Omega$,
 $R_C = 6.8k\Omega$, $V_{BE} = 0.7V$.

WKT $I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E} = \frac{10V - 0.7V}{4.7k\Omega}$

$I_{E1} + I_{E2} = 2mA$

∴ $I_{C2} \approx I_{E2} \approx 1mA$.

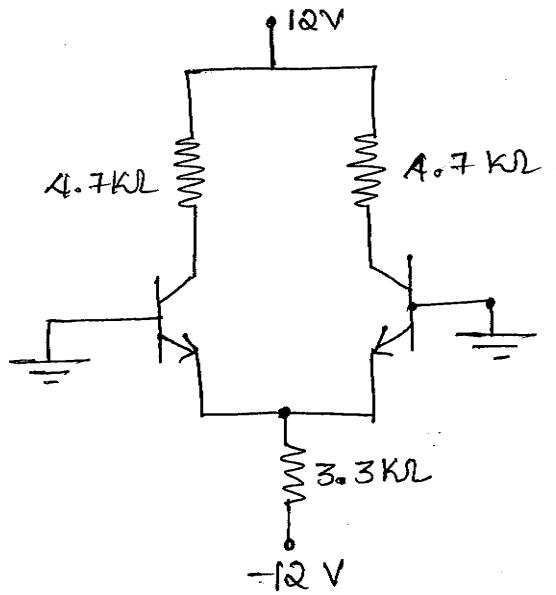
* O/P voltage V_o is given by.

$$\begin{aligned} V_o &= V_{CC} - (I_{C2} R_C) - V_{BE} \\ &= 10V - (1mA \times 6.8k\Omega) - 0.7V \end{aligned}$$

$V_o = 2.5V$



Q) calculate the dc operating point values & the o/p voltage for the circuit shown in the fig ①.
 Assume $V_{BE} = 0.7 \text{ V}$ for both the transistors.



Given :- $V_{CC} = +12 \text{ V}$, $-V_{EE} = -12 \text{ V}$, $R_C = 4.7 \text{ k}\Omega$,
 $V_{BE} = 0.7 \text{ V}$.

SOL:- $I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E}$

$$I_{E1} + I_{E2} = 3.42 \text{ mA}$$

$$I_{E1} + I_{E2} = 1.71 \text{ mA}$$

$$I_E \approx I_{CQ} = 1.71 \text{ mA}$$

* $V_{CEQ} = V_{CC} + V_{BE} - I_C R_C = 12 \text{ V} + 0.7 \text{ V} - (1.71 \text{ mA} \times 4.7 \text{ k}\Omega)$

$$V_{CEQ} = 1.6536 \text{ V}$$

* O/P voltage.

$$\begin{aligned} V_o &= V_{CC} - (I_C R_C) - V_{BE} \\ &= 12 \text{ V} - (1.71 \text{ mA} \times 4.7 \text{ k}\Omega) - 0.7 \text{ V} \end{aligned}$$

$$V_o = 3.9536 \text{ V}$$



OP-AMP PARAMETERS :-

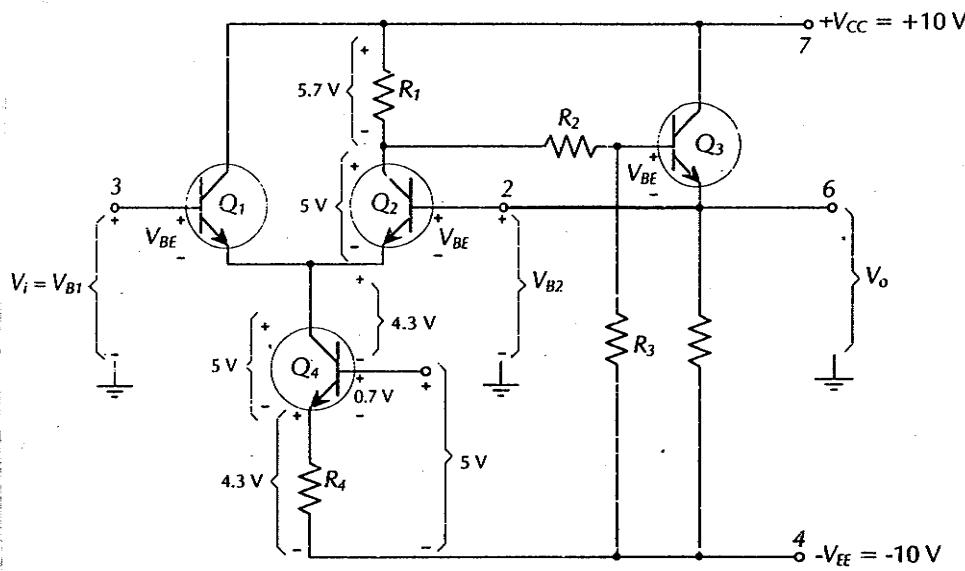


Figure ① There are limits to the input and output voltage ranges of an operational amplifier. In the basic op-amp circuit these limits occur when any of the transistors approach saturation or cutoff.





COMMON MODE REJECTION :-

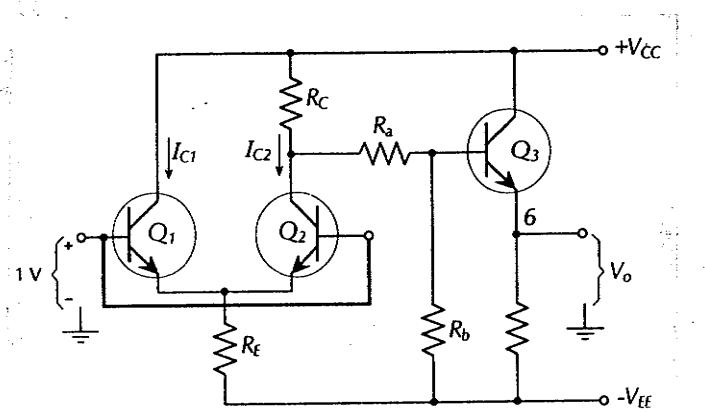


fig ① : Basic circuit of an op-Amp with the two IP's short circuited and a common input voltage V_i applied to them.

The two input terminals are shorted together & a dc voltage of 1V is applied to it. This is known as a common mode IP.

Since there is no differential input, & both input terminals are at the same potential. So ideally the o/p should be zero.

Since base voltage of Q_1 & Q_2 are raised by 1V, the voltage drop across R_E also increases by 1V. This increases I_{C1} & I_{C2} . Thus voltage drop across R_C also increases, which results in a change in the o/p.

Similarly, if a -1V common mode IP is applied, I_{C2} falls & again a change is produced at o/p.



- * The common-mode voltage gain 'A_{cm}' is defined as the ratio of change in o/p voltage to change in common mode i/p voltage.

i.e.

$$A_{cm} = \frac{V_o(cm)}{V_i(cm)}$$

- * The ability of the op-amp in rejecting common mode i/p's is defined as common mode rejection ratio (CMRR).
- * CMRR is defined as the ratio of the open-loop gain 'M' to the common mode gain A_{cm}.

i.e.

$$CMRR = \frac{M}{A_{cm}}$$

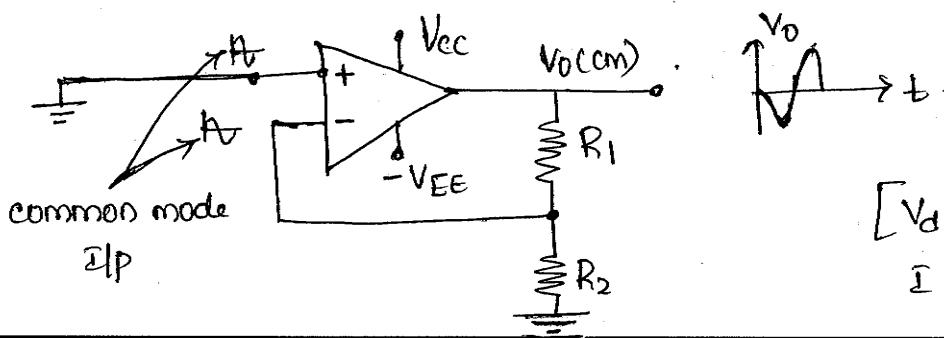
The CMRR is usually expressed in decibels.

i.e.

$$(CMRR)_{dB} = 20 \log_{10} \left(\frac{M}{A_{cm}} \right) dB.$$

Typical value of CMRR for 741 IC is 90 dB.

- * The effect of common mode gain can be modified with feedback. consider the non-invert amplifier circuit as shown in fig. ②.



$$\begin{aligned} V_d &= I R_2 \\ I &= \frac{V_o(cm)}{R_1 + R_2} \end{aligned}$$



WKT $A_{cm} = \frac{V_o(\text{cm})}{V_i(\text{cm})}$

$$V_o(\text{cm}) = A_{cm} \cdot V_i(\text{cm}) \rightarrow \textcircled{1}$$

The differential input voltage required to cancel $V_o(\text{cm})$

i.e.,

$$V_d = \frac{V_o(\text{cm})}{M} \rightarrow \textcircled{2}$$

Sub. eq. ① in eq. ②, we get

$$V_d = \frac{A_{cm} \times V_i(\text{cm})}{M} \rightarrow \textcircled{3}$$

from fig ②, the feedback vtg ' V_d ' across R_2 is

$$V_d = I R_2.$$

$$V_d = \frac{V_o(\text{cm})}{R_1 + R_2} \cdot R_2 \rightarrow \textcircled{4}$$

where:

$$I = \frac{V_o(\text{cm})}{R_1 + R_2}$$

Equating eq. ③ & ④

$$\frac{V_o(\text{cm})}{R_1 + R_2} \cdot R_2 = \frac{A_{cm} \times V_i(\text{cm})}{M}$$

$$V_o(\text{cm}) = \frac{A_{cm} V_i(\text{cm})}{M} \cdot \frac{R_1 + R_2}{R_2}$$

$$V_o(\text{cm}) = \frac{A_{cm} V_i(\text{cm}) \cdot A_V}{M}$$

where $A_V = \frac{R_1 + R_2}{R_2}$



CMRR → FORMULAE

1) Mode gain $A_{cm} = \frac{V_o(\text{cm})}{V_i(\text{cm})}$.

2) Differential slp $V_d = \frac{V_o(\text{cm})}{M}$.

3) $V_o(\text{cm}) = A_{cm} \cdot V_i(\text{cm})$

4) $\text{CMRR} = \frac{M}{A_{cm}}$.

$$(\text{CMRR})_{\text{dB}} = 20 \log_{10} \left(\frac{M}{A_{cm}} \right) \text{dB}$$

5) $V_o(\text{cm}) = \frac{V_i(\text{cm})}{\text{CMRR}} \cdot A_v$

6) $V_i(\text{cm}) = \frac{V_o(\text{cm}) \cdot \text{CMRR}}{A_v}$.

CMRR PROBLEMS.

- 1) A 741 op-amp is used in a non-inverting amplifier with a voltage gain of 50. calculate the typical o/p voltage that would result from a common mode slp with a peak level of 100mV.

Given : $A_v = 50$, $V_i(\text{cm}) = 100 \text{ mV}$.

From the 741 datasheet: Typical CMRR = 90 dB.

Sol: - WKT, $(\text{CMRR})_{\text{dB}} = 20 \log_{10} (\text{CMRR})$.

$$(\text{CMRR}) = \text{antilog} \left(\frac{(\text{CMRR})_{\text{dB}}}{20} \right)$$



$$\boxed{CMRR = 31623}$$

WKT

$$V_o(\text{cm}) = \frac{V_i(\text{cm})}{CMRR} \times A_v \\ = \frac{100 \text{ mV}}{31623} \times 50$$

$$\boxed{V_o(\text{cm}) = 158 \mu\text{V}}$$

- 2) Define CMRR of an op-amp. An LM 308 op-amp circuit with a closed loop gain of 33 has a common-mode IIP of 1.5V. calculate the maximum op voltage this might produce. The minimum CMRR for LM308 is 80dB.

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CMRR is defined as the ratio of the open-loop gain 'M' to the common mode gain A_{cm} .

$$\boxed{CMRR = \frac{M}{A_{cm}}}$$

(IM)

In terms of dB,

$$\boxed{(CMRR)_{dB} = 20 \log_{10} \left(\frac{M}{A_{cm}} \right)}$$

Given : $(CMRR)_{dB} = 80 \text{ dB}$, $A_v = 33$, $V_i(\text{cm}) = 1.5 \text{ V}$

Sol:- $(CMRR)_{dB} = 20 \log_{10} (CMRR)$

$$80 \text{ dB} = 20 \log_{10} (CMRR)$$

$$CMRR = \text{antilog} \left(\frac{80}{20} \right)$$



$$\text{CMRR} = 10000$$

WKT $V_o(\text{cm}) = \frac{V_i(\text{cm})}{\text{CMRR}} \cdot A_v = \frac{1.5 \text{ V}}{10000} \times 33$

$$V_o(\text{cm}) = 5 \text{ mV}$$

3) When a 741 op-amp having a typical CMRR of 90 dB, is used in a non-inverting amplifier with a voltage gain of 100, the o/p voltage was measured to be 15.8mV with some common-mode IIP. Determine the common mode IIP voltage.

Given: $A_v = 100$, $V_o(\text{cm}) = 15.8 \text{ mV}$, $V_i(\text{cm}) = ?$

SOL: WKT for $\mu\text{A}-741$, $(\text{CMRR}) = 90 \text{ dB}$

$$(\text{CMRR}) = \text{Antilog} \left(\frac{90}{20} \right)$$

$$\text{CMRR} = 31622.78$$

WKT. $V_i(\text{cm}) = \frac{V_o(\text{cm}) \cdot \text{CMRR}}{A_v}$

$$= \frac{15.8 \text{ mV} \times 31622.78}{100}$$

$$V_i(\text{cm}) = 5 \text{ V}$$



Power Supply Rejection Ratio (PSRR) :-

In basic op-amp circuit, a variation in $-V_{EE}$ have the same effect as an o/p voltage change. These variations in V_{CC} & V_{EE} do produces some changes at o/p.

The PSRR is the ability of the op-amp to reject variations in the power supply voltages.

Ideally, the o/p voltage should not vary with variations in the power supply voltage.

$$\boxed{PSRR = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}}$$

- * If a variation of 1V in V_{CC} or V_{EE} causes the o/p to change by 1V, then PSRR is 1V per Volt i.e. (1V/V).
- * If the o/p changes by 10mV when one of the supply voltage changes by 1V, then PSRR is 10mV/V .

for LM-741, the PSRR is typically 30mV/V .
For the LM-708, the PSRR is expressed in decibels.

- 1) A 741 op-amp uses a $\pm 15\text{V}$ supply with a $\pm 2\text{mV}$, 120Hz ripple voltage superimposed. calculate the amplitude of the o/p voltage produced by the power supply ripple.

Given :- $V_s(\text{ripple}) = 2\text{mV}$.



Sol: NKT for op-amp 741, PSRR = 30 μV/V.

NKT. $PSRR = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$

$$V_o(\text{ripple}) = PSRR \times V_s(\text{ripple})$$
$$= 30 \mu\text{V}/\text{V} \times 2 \text{mV}$$

$$V_o(\text{ripple}) = 60 \text{nV}$$

2). An LM 108 op-amp has a typical PSRR of -80dB. working with ±15V supply having 3mV ac ripple. calculate the maximum level of the op vtg ripple.

Given: $(PSRR)_{dB} = -80 \text{dB}$, $V_s(\text{ripple}) = 3 \text{mV}$, $V_o(\text{ripple}) = ?$

Sol:- $(PSRR)_{dB} = 20 \log_{10} (PSRR)$

$$(-80) = 20 \log_{10} PSRR$$

$$(PSRR) = \text{Antilog} \left(\frac{-80}{20} \right)$$

$$PSRR = 10^4$$

NKT. $PSRR = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$

$$V_o(\text{ripple}) = PSRR \times V_s(\text{ripple})$$
$$= 10^4 \times 3 \text{mV}$$

$$V_o(\text{ripple}) = 0.3 \mu\text{V}$$



* A 741 op-amp having a PSRR of $30 \mu\text{V/V}$, has a minimum o/p signal level of 100mV . O/p ripple voltage produced by the ripple on the supply voltages is not to exceed 0.1% of the minimum o/p signal level. Determine the maximum permissible supply voltage ripple.

Given :-

$$\text{PSSR} = 30 \mu\text{V/V},$$

$$\text{Minimum o/p signal} = 100\text{mV}$$

$$\therefore V_o(\text{ripple}) = 0.1\% \text{ of minimum o/p signal}$$

$$= \frac{0.1}{100} \times 100\text{mV}$$

$$V_o(\text{ripple}) = 0.1\text{mV}$$

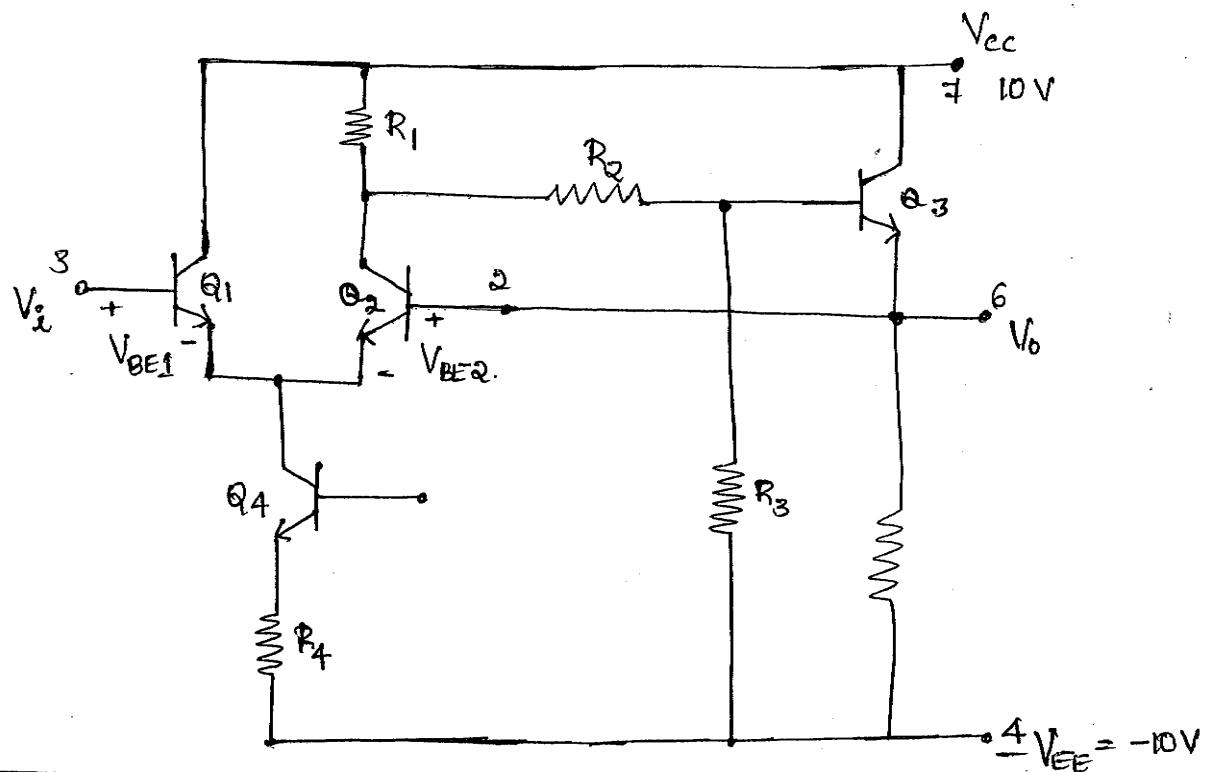
$$V_s(\text{ripple}) = \frac{V_o(\text{ripple})}{\text{PSSR}}$$

$$= \frac{0.1\text{mV}}{30 \mu\text{V/V}}$$

$$\therefore V_s(\text{ripple}) = 3.33\text{V}$$



OFFSET Voltages & current :-



O/P offset voltage :-

for the o/p voltage to be exactly equal to the I/P, the transistors Q_1 & Q_2 must be perfectly matched.

The o/p voltage can be calculated as
(applying KVL from V_i , V_{BE1} , V_{BE2} , & o/p V_o)

$$V_i - V_{BE1} + V_{BE2} - V_o = 0$$

$$V_o = V_i - V_{BE1} + V_{BE2}$$

With $V_{BE1} = V_{BE2}$ and $V_i = 0$

$$\text{O/P } V_o = V_i = 0$$



Now suppose that the transistors are not perfectly matched and that $V_{BE1} = 0.7V$ & $V_{BE2} = 0.6V$ with $V_i = 0$, then o/p ($V_o = V_i - V_{BE1} + V_{BE2}$)

$$V_o = 0 - 0.7V + 0.6V$$

$$\boxed{V_o = -0.1V}$$

This unwanted o/p is known as an o/p offset voltage.

IIP offset voltages:-

Now suppose that the transistors Q₁ & Q₂ are not perfectly matched and that $V_{BE1} = 0.7V$ and while $V_{BE2} = 0.6V$.

with the IIP $V_i = 0V$,

WRT $V_o = V_i - V_{BE1} + V_{BE2}$

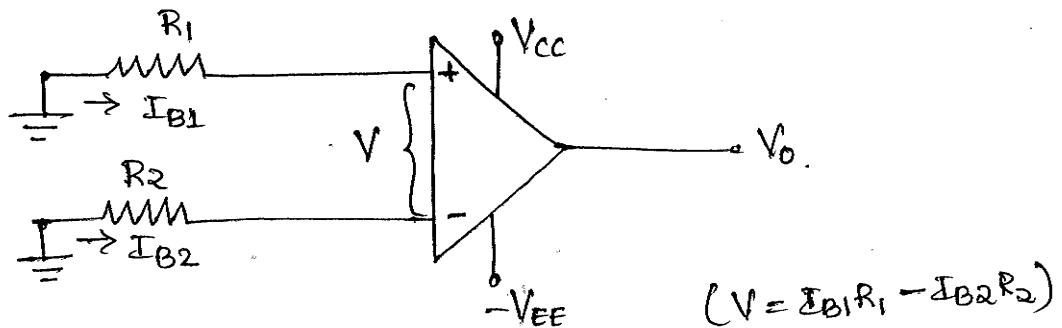
$$= 0 - 0.7V + 0.6V$$

$$\boxed{V_o = -0.1V}$$

* To set V_o to ground level, the IIP would have to be raised to $+0.1V$. This is termed as IIP offset voltage V_{ios} .

For 741 op-amp, typical value of $V_{ios} = 1mV$ & maximum value of $V_{ios} = 5mV$.

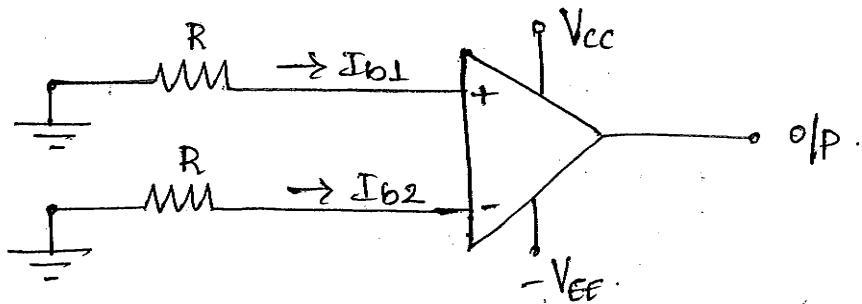


IIP offset current :-

* The algebraic difference between the currents flowing into the two IIP terminals of the op-amp is called IIP offset current & denoted as I_{ios} .

$$I_{ios} = |I_{b1} - I_{b2}|$$

For TAA op-amp, maximum value of I_{ios} is 200nA.

IIP bias current :-

The average value of the two currents flowing into the op-amp IIP terminals is called IIP bias current.

$$I_b = \frac{I_{b1} + I_{b2}}{2}$$



for 541 op-amp, maximum value of I_b is 500nA,

OFFSET Nulling :-

I - Method 6 :-

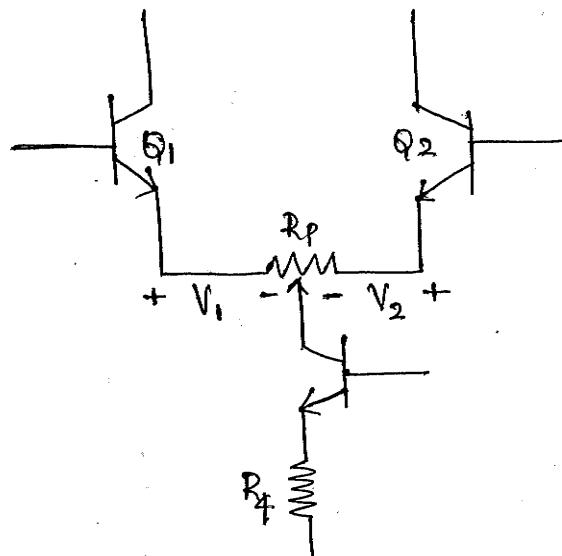


fig ① : use of potentiometer for offset Nulling

* To minimize the effect of offset voltages and currents a variable resistance is introduced b/w the emitters of Q_1 & Q_2 as shown in fig.

The variable resistance R_p is the low resistance potentiometer which alters the voltage drop from base of each transistor to the common moving point of potentiometer. Hence the I_{bp} base current also get altered.

As I_{bp} offset current produces an offset voltage by adjusting R_p , both I_{bp} offset current as well as I_{bp} offset voltage can be nulled.



II - Method :-

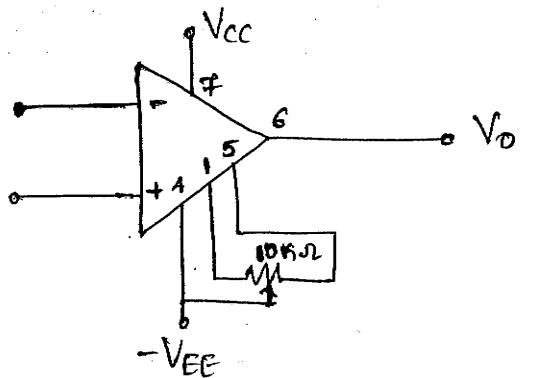


fig ⑥ : Manufacturer recommended method of offset nulling for the 741.

- * A $10\text{k}\Omega$ potentiometer is connected to offset nulling terminals 1 and 5 & its moving contact is connected to the negative supply ($-V_{EE}$).

The potentiometer is adjusted to null the op-amp offset voltage to zero, thus nulling both I_{IP} offset current & I_{OP} offset voltage.

Resistor Tolerance Effect :-

- * The discussions of offset voltages and currents assumed that either there were no resistors at the op-amp I_{IP} terminals or else that exactly equal resistors were connected to the I_{IP} terminal.

Most op-amp circuits have resistors at their I_{IP} terminals and sometimes those resistors may not have equal resistance values.



The resistor tolerance might be almost as effective in producing an op-amp offset voltage as the op-amp input offset voltage & I_{IP} offset current.

FORMULAE :-

* I_{IP} offset voltage due to I_{IP} offset current.

$$V_{i(\text{offset})} = I_{i(\text{offset})} \times (R_1 \text{ or } R_2)$$

* op-amp voltage : $V_{\text{out}} = V_{i(\text{offset})} \times A_v$

* Resistor tolerance.

$$R_1 = R_1 + \text{tolerance}$$

$$R_2 = R_2 - \text{tolerance}$$

$$V_{i(\text{offset})} = I_B R_1 - I_B R_2 = I_B [R_1 - R_2]$$

NOTE :-

i) for 741 IC, $V_{i(\text{offset})} = 5 \text{ mV}$

$$I_{i(\text{offset})} = 200 \text{nA}$$

$$I_B = 500 \text{nA}$$



- 1) The ckt in fig ① uses a 741 op-amp and has $R_1 = R_2 = 22\text{ k}\Omega$ with a resistor tolerance of $\pm 20\%$. Determine the maximum IIP offset voltage due to,
- ① the 741 specified IIP offset voltage,
 - ② the 741 IIP offset current,
 - ③ the resistor tolerance.

Sol :-

- ① For 741 IC, $V_{i(\text{offset})} = 5\text{ mV}$ maximum
- ② For 741 IC, $I_{i(\text{offset})} = 200\text{nA}$ maximum.

$$\begin{aligned} V_{i(\text{offset})} &= I_{i(\text{offset})} \times (R_1 \text{ or } R_2) \\ &= 200\text{nA} \times 22\text{k}\Omega. \end{aligned}$$

$$V_{i(\text{offset})} = 4.4\text{ mV}$$

- ③ Tolerance :-

$$R_1 = 22\text{k}\Omega + 20\%$$

$$R_1 = 26.4\text{k}\Omega$$

$$R_2 = 22\text{k}\Omega - 20\%$$

$$R_2 = 17.6\text{k}\Omega$$

$$\begin{aligned} * V_{i(\text{offset})} &= I_B R_1 - I_B R_2 = I_B (R_1 - R_2) \\ &= 500\text{nA} (26.4\text{k}\Omega - 17.6\text{k}\Omega) \end{aligned}$$

$$V_{i(\text{offset})} = 4.4\text{ mV}$$



- Q) The resistors $R_1 = R_2 = 18\text{ k}\Omega$ have tolerance of $\pm 5\%$. Calculate the maximum IIP offset voltage due to resistor tolerance at 25°C ,
- When LM 108 is used having IIP bias current 2 nA maximum.
 - When the op-amp is an LM 308 with IIP bias current of 7 nA maximum.

Given :- $R_1 = R_2 = 18\text{ k}\Omega$, tolerance $= \pm 5\%$, $I_B = 2\text{ nA}$.

Sol :- Because of the $\pm 5\%$ resistor tolerance.

$$R_2 = 18\text{ k}\Omega - 5\% = 17.1\text{ k}\Omega$$

$$R_1 = 18\text{ k}\Omega + 5\% = 18.9\text{ k}\Omega$$

- i) When LM 108 is used with $I_B = 2\text{ nA}$ maximum, the maximum IIP offset voltage is given by

$$\begin{aligned} V_{\text{I}}(\text{offset}) &= I_B R_1 - I_B R_2 \\ &= I_B [R_1 - R_2] \\ &= 2 \times 10^{-9} [18.9\text{ k}\Omega - 17.1\text{ k}\Omega] \end{aligned}$$

$V_{\text{I}}(\text{offset}) = 3.6\text{ mV}$

- ii) When LM 308 is used with $I_B = 7\text{ nA}$ maximum, the maximum IIP offset voltage is given by

$$\begin{aligned} V_{\text{I}}(\text{offset}) &= I_B [R_1 - R_2] \\ &= 7 \times 10^{-9} [18.9\text{ k}\Omega - 17.1\text{ k}\Omega]. \end{aligned}$$

$V_{\text{I}}(\text{offset}) = 12.6\text{ }\mu\text{V}$



3) In fig ①, a 741 op-amp is used with resistances $R_1 = R_2 = 27\text{ k}\Omega$ each having a tolerance of $\pm 20\%$. calculate the maximum ΔV_{p} offset voltage due to

- the 741 specified ΔV_{p} offset voltage.
- the 741 input offset current
- the resistor tolerance.

Given that $V_{\text{i}}(\text{offset}) = 6\text{ mV}$ maximum, $I_{\text{i}}(\text{offset}) = 200\text{nA}$ maximum & ΔV_{p} bias current $I_B = 500\text{nA}$ maximum.

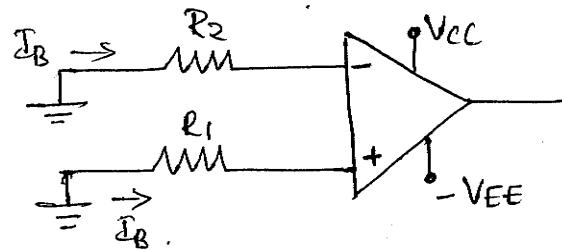
Given :- $R_1 = R_2 = 27\text{ k}\Omega$

Tolerance $= \pm 20\%$

$V_{\text{i}}(\text{offset}) = 6\text{ mV}$,

$I_{\text{i}}(\text{offset}) = 200\text{nA}$

$I_B = 500\text{nA}$ maximum.



Sol :-

i) the maximum ΔV_{p} offset voltage $= 6\text{ mV}$ max

ii)
$$\begin{aligned} V_{\text{i}}(\text{offset}) &= I_{\text{i}}(\text{offset}) \times (R_1 \text{ or } R_2) \\ &= 200\text{nA} \times 27\text{k}\Omega \end{aligned}$$

$$\therefore V_{\text{i}}(\text{offset}) = 5.4\text{ mV}$$

iii) Given $I_B(\text{max}) = 500\text{nA}$

Due to $\pm 20\%$ tolerance of resistors

$$R_2 = 27\text{k}\Omega - 20\% = 21.6\text{k}\Omega$$

$$R_1 = 27\text{k}\Omega + 20\% = 32.4\text{k}\Omega$$

$$\begin{aligned} V_{\text{i}}(\text{offset}) &= I_B (R_1 - R_2) \\ &= 500\text{nA} (32.4\text{k}\Omega - 21.6\text{k}\Omega) \end{aligned}$$

$$V_{\text{i}}(\text{offset}) = 5.4\text{ mV}$$



4) In the circuit of fig ①, a LM 108 op-amp is used with resistances $R_1 = R_2 = 18 \text{ k}\Omega$. calculate the maximum ZLP voltage due to i) the op-amp specified ZLP offset voltage and ii) the ZLP offset current.

Given that $V_{i(\text{offset})} = 3\text{mV}$ maximum & $I_{i(\text{offset})} = 0.2\text{nA}$ at 25°C for LM 108.

Given :- $R_1 = R_2 = 18 \text{ k}\Omega$, $V_{i(\text{offset})} = 3\text{mV}$, $I_{i(\text{offset})} = 0.2\text{nA}$

Sol:- i) the maximum ZLP offset voltage = 3mV maximum

$$\begin{aligned} \text{ii)} \quad V_{i(\text{offset})} &= I_{i(\text{offset})} \times (R_1 \text{ or } R_2) \\ &= 0.2 \times 10^{-9} \times 18 \text{ k}\Omega \end{aligned}$$

$$V_{i(\text{offset})} = 3.6 \mu\text{V}$$

5) What is meant by offset in an op-amp, how does it effect the performance of the op-amp? If an op-amp has an bias current of 200nA & two equal resistances of $20\text{k}\Omega$ are connected between inverting terminal & ground as well as non-inverting terminal & ground respectively what will be the ZLP offset vltg for a tolerance of $\pm 20\%$ in resistor values? what will be OLP voltage under open loop gain of 10^5 ?

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Sol:-

When the two-transistors of the ZLP stage are not perfectly matched then the two base currents are different i.e. $I_{B1} \neq I_{B2}$ & there is some difference between their base-emitter voltages $V_{BE1} \neq V_{BE2}$. Due to this, there is presence of unwanted voltage & currents which are called offset voltages & currents.



IIP offset voltage (V_{Ios}) :-

The differential voltage that must be applied between the two input terminals of an op-amp, to make the oip voltage zero is called input offset voltage and denoted as V_{Ios} .

IIP offset current (I_{Ios}) :-

The algebraic difference between the current flowing into the two input terminals of the op-amp is called input offset current and denoted as I_{Ios} .

$$I_{Ios} = |I_{B1} - I_{B2}|$$

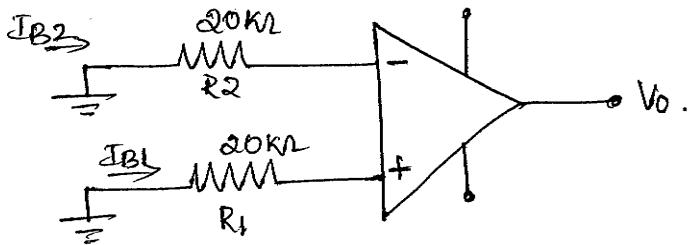
OIP offset voltage (V_{Ios}) :-

The presence of dc voltage at the oip terminals when both the iip terminals are grounded is called output offset voltage.

4-Marks

Given :- $I_B = 200\text{nA}$, $R_1 = R_2 = 20\text{k}\Omega$,
Tolerance $= \pm 20\%$. $A_v = 10^5$.

Sol:-



4-Marks

$$R_1 = 20\text{k}\Omega + 20\% = 24\text{k}\Omega$$

$$R_2 = 20\text{k}\Omega - 20\% = 16\text{k}\Omega$$

$$V_i(\text{offset}) = I_B [R_1 - R_2] = 200\text{nA} [24\text{k}\Omega - 16\text{k}\Omega]$$

$$V_i(\text{offset}) = 1.6\text{mV}$$



$$V_{out} = V_{i(\text{offset})} \times A_v = 1.6 \text{ mV} \times 10^5$$

$$V_{out} = 160$$

I/P & O/p Impedances :-

Input impedance :-

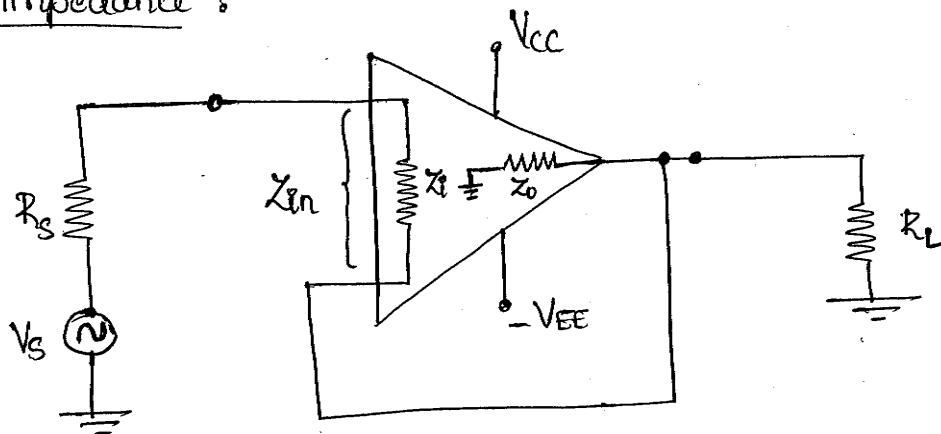


fig ① :-

In most op-amp applications, some form of negative feedback is normally provided by the externally connected components.

From negative feedback, the IIP impedance of the op-amp IIP terminal becomes

$$Z_{in} = (1 + M\beta) Z_e$$

Where, Z_e = the op-amp IIP impedance without negative feedback.

M = op-amp open-loop gain.

β = feedback factor = 1 for a Voltage follower.



The impedance of signal sources connected at the input of an op-amp circuit should be very much smaller than the amplifier input impedance to avoid a loss of signal across 'Rs'.

Output impedance :-

The typical op-amp resistance specified for the 741 op-amp is 75Ω . Any stray capacitance in parallel with this is certain to have a much larger reactance than 75Ω .

- * The output impedance of the op-amp is affected by negative feedback.

$$Z_{out} = \frac{Z_0}{1 + MB}$$

Where,

Z_0 = op-amp open-loop impedance without negative feedback.

M = op-amp open-loop gain

B = feedback factor.

Load impedance connected at the output of an op-amp should be much larger than the circuit open-loop impedance. This is to avoid any significant loss of o/p as a voltage drop across Z_{out} .



NOTE :-

from 741 op-amp datasheet.

1) $R_i(\text{min}) = Z_i = 0.3 \text{ M}\Omega$

2) $M(\text{min}) = 50,000$

3) $Z_o = 75\Omega$

4) Typical value of $M = 200000 = 2 \times 10^5$

5) For voltage follower, $\boxed{\beta=1}$

6) For INV amplifier & Non - INV amplifier,

$$\boxed{\beta = \frac{1}{A_V}}$$

FORMULAE

1) Input impedance $Z_{in} = (1+MB)Z_i$

2) output impedance $Z_{out} = \frac{Z_o}{1+MB}$

3) For voltage follower $\boxed{\beta=1}$

4) For INV & Non INV amplifier $\beta = \frac{1}{A_V}$

5). $A_V = \frac{R_1 + R_2}{R_2}$ & $\frac{1}{A_V} = \frac{R_2}{R_1 + R_2}$.

PROBLEMS

1) calculate the minimum input impedance of a 741 op-amp employed as a voltage follower.

Sol:- WKT for 741 the minimum value of Z_i is

$$Z_i(\text{min}) = 0.3 \text{ M}\Omega \quad \& \quad M(\text{min}) = 50,000$$



for voltage follower $B=1$

$$Z_{in} = (1 + MB) Z_{in(min)}$$

$$= (1 + 50000 \times 1) 0.3 M\Omega$$

$$Z_{in} = 15000 M\Omega$$

- 2) calculate the typical o/p impedance of a 741 op-amp connected to function as a voltage follower

sol:- WRT for 741 op-amp, the typical value of

$$Z_0 = 75\Omega \text{ & } M = 200000$$

for voltage follower $\boxed{B=1}$

$$Z_{out} = \frac{Z_0}{1+MB} = \frac{75\Omega}{(1+200000 \times 1)}$$

$$Z_{out} = 0.004 \Omega$$

- 3) From data sheet of LM 108, the minimum value of input resistance is $30 M\Omega$ and large signal voltage gain (open-loop) is 50,000. Determine the minimum input impedance of an LM 108 op-amp when it is used as i) voltage follower ii) a non-inverting amplifier with a voltage gain of 60.

Given :- $Z_i = 30 M\Omega$, $M = 50,000$

i) For voltage follower $\boxed{B=1}$



$$Z_{in} = (1 + MB) Z_L = (1 + 50000 \times 1) 30M\Omega$$

$$Z_{in} = 1.5 \times 10^{12} \Omega$$

ii) when used as a non-INV amplifier with a voltage gain of 60, we have $B = \frac{1}{Av} = \frac{1}{60}$

$$Z_{in} = (1 + MB) Z_L = (1 + 50000 \times \frac{1}{60}) 30 \times 10^6$$

$$Z_{in} = 2.5 \times 10^{10} \Omega$$

- 4) From the data sheet of LM 308, having input resistance of $10M\Omega$ minimum & open-loop gain of 15,000 minimum. Determine the minimum Z_{in} impedance of an LM 308 op-amp when it is used as
 i) Voltage follower ii) a non-INV amplifier with a voltage gain of 60.

Given :- $Z_L = 10M\Omega$, $M = 15000$, $Av = 60$.

Sol :-

i) When used as voltage follower, $B = 1$

$$Z_{in} = (1 + MB) Z_L = (1 + 15000 \times 1) 10 \times 10^6$$

$$Z_{in} = 1.5 \times 10^{11} \Omega$$

ii) When used as a non-INV amplifier with a voltage gain of 60 ie. $B = \frac{1}{Av} = \frac{1}{60}$

$$Z_{in} = (1 + MB) Z_L = \left(1 + M + \frac{1}{Av}\right) Z_L$$



$$Z_{in} = \left(1 + 15,000 \times \frac{1}{60}\right)$$

$$Z_{in} = 2.5 \times 10^9 \Omega$$

- 5) Determine the typical o/p resistance for a 715 op-amp (with typical o/p resistance of 75Ω & open-loop large signal gain of 30,000)
- i) When used as a voltage follower and
 ii) When used as a non-INV amplifier with a gain of 100.

Given: $Z_o = 75\Omega$, $M = 30,000$, $A_v = 100$

- i) When used as a voltage follower $[B=1]$

$$Z_{out} = \frac{Z_o}{1+MB} = \frac{75\Omega}{(1+30000 \times 1)} = \underline{\underline{2.5 \times 10^3 \Omega}}$$

- ii) When used as non-INV amplifier with a gain of 100,

$$B = \frac{1}{A_v} = \frac{1}{100}$$

$$Z_{out} = \frac{Z_o}{(1+MB)}$$

$$= \frac{Z_o}{\left(1 + M \cdot \frac{1}{A_v}\right)} = \frac{75\Omega}{\left(1 + 30000 \cdot \frac{1}{100}\right)}$$

$$\boxed{Z_{out} = 0.25 \Omega}$$



- Q) Determine the typical IIP & OIP impedances of a non-INV amplifier with a voltage gain of 40,
- Using a 741 op-amp (having typical $Z_i = 2M\Omega$, $Z_o = 75\Omega$, $M = 2 \times 10^5$).
 - Using a 715 op-amp (having typical $Z_i = 1M\Omega$, $Z_o = 75\Omega$, $M = 30,000$)

Given :- $A_v = 40$.

Sol :-

- For 741 op-amp :

Given $Z_i = 2M\Omega$, $Z_o = 75\Omega$, $M = 2 \times 10^5$

For Non-INV amplifier $B = \frac{1}{A_v} = \frac{1}{40}$

IIP impedance is

$$Z_{in} = (1 + MB) Z_i = \left(1 + 2 \times 10^5 \left(\frac{1}{40}\right)\right) 2M\Omega$$

$$Z_{in} = 10 \times 10^9 \Omega$$

OIP Impedance is :-

$$Z_{out} = \frac{Z_o}{(1 + MB)} = \frac{75\Omega}{\left[1 + 2 \times 10^5 \left(\frac{1}{40}\right)\right]}$$

$$Z_{out} = 15 \times 10^{-3} \Omega$$

- For 715 op-amp :-

Given : $Z_i = 1M\Omega$, $Z_o = 75\Omega$, $M = 30000$, $B = \frac{1}{A_v} = \frac{1}{40}$

IIP impedance is

$$Z_{in} = (1 + MB) Z_i = \left(1 + 30000 \left(\frac{1}{40}\right)\right) 1M\Omega$$



$$Z_{in} = 7.5 \times 10^8 \Omega$$

OIP impedance is.

$$Z_{out} = \frac{Z_0}{1+M\beta} = \frac{75 \Omega}{[1 + 30000(\frac{1}{40})]}$$

$$Z_{out} = 0.1 \Omega$$

- Q) calculate the typical IIP & OIP resistance of a non-inverting amplifier with a voltage gain of 25,
 i) Using a 741 op-amp ii) Using a 715 op-amp.

for 741 : $Z_i = 2M\Omega$, $M = 2 \times 10^5$, $Z_0 = 75 \Omega$

for 715 : $Z_i = 1M\Omega$, $M = 3 \times 10^4$, $Z_0 = 75 \Omega$.

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Given :- $A_v = 25$

Sol:-

i) Using a 741 op-amp.

Given : $Z_i = 2M\Omega$, $M = 2 \times 10^5$, $Z_0 = 75 \Omega$

for Non-INV amplifier

$$\beta = \frac{1}{A_v} = \frac{1}{25}$$

Input impedance is

$$Z_{in} = (1 + M\beta) Z_i = [1 + 2 \times 10^5 (\frac{1}{25})] 2M\Omega$$

$$Z_{in} = 16 \times 10^9 \Omega$$

← **QMark**

Output impedance is

$$Z_{out} = \frac{Z_0}{1+M\beta} = \frac{75 \Omega}{[1 + 2 \times 10^5 (\frac{1}{25})]}$$



$$Z_{out} = 9.4 \text{ m}\Omega$$

← [1 mark]

9) Using a 715 op-amp :-

Given : $Z_i = 1 \text{ M}\Omega$, $M = 3 \times 10^4$, $Z_o = 75 \Omega$, $B = \frac{1}{A_V} = \frac{1}{25}$

Input impedance is

$$Z_{in} = (1 + MB) Z_i = \left[1 + 3 \times 10^4 \cdot \left(\frac{1}{25} \right) \right] \times 1 \text{ M}\Omega$$

$$Z_{in} = 1.2 \times 10^9 \Omega$$

← [2 marks]

Output impedance is

$$Z_{out} = \frac{Z_o}{[1 + MB]} = \frac{75 \Omega}{\left[1 + 3 \times 10^4 \left(\frac{1}{25} \right) \right]}$$

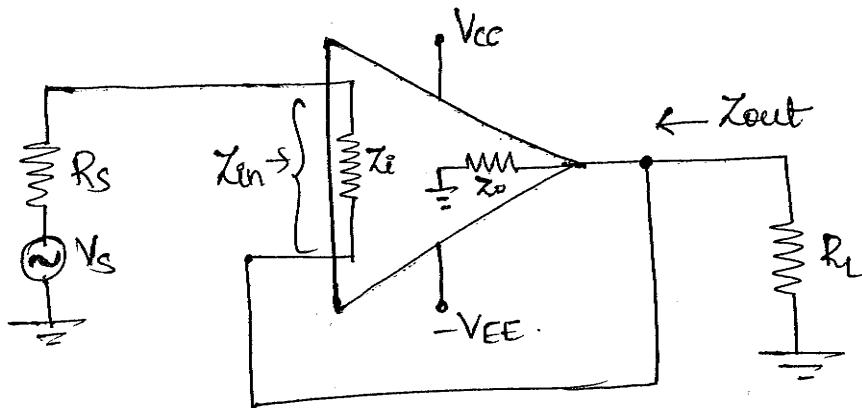
$$Z_{out} = 63 \text{ m}\Omega$$

← [1 mark]

8) prove that the open loop zlp & o/p impedance of an op-amp under closed loop condition change due to feedback. Determine these impedances for an non-invert amplifier with a closed loop gain of 200. The op-amp has differential zlp impedance of $2 \times 10^6 \Omega$ & o/p impedance 50Ω . The open loop gain of op-amp $A_{vo} = 10^6$

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Proof e -

If Z_i & Z_o are the open loop impedance, then
closed loop impedance is given by

$$\begin{aligned} Z_{in} &= [1 + M\beta] Z_i \quad \} \\ Z_{out} &= \frac{Z_o}{1 + M\beta} \end{aligned} \quad \leftarrow \boxed{2 \text{ Marks}}$$

Given e - $A_v = 200$, $Z_i = 2 \times 10^6 \Omega$, $Z_o = 50 \Omega$, $A_{vo} = 19 = 10^6$
for non-INV amplifier $\beta = \frac{1}{A_v} = \frac{1}{200}$

$$\begin{aligned} Z_{in} &= [1 + M\beta] Z_i \\ &= [1 + 10^6 \times \frac{1}{200}] 2 \times 10^6 \end{aligned}$$

$$Z_{in} = 10^{10} \Omega \quad \leftarrow \quad \boxed{1 \text{ Mark}}$$

$$Z_{out} = \frac{Z_o}{1 + M\beta} = \frac{50 \Omega}{[1 + 10^6 \times \frac{1}{200}]} \quad \leftarrow$$

$$Z_{out} = 9.9 \text{ m}\Omega \quad \leftarrow \quad \boxed{1 \text{ Mark}}$$



Slew Rate :-

The slew rate 's' of an op-amp is the maximum rate at which the output voltage can change.

When the slew rate is too slow for the I/O, distortion results.

To understand the concept of slew rate, let us consider an op-amp voltage follower circuit as shown in fig below :

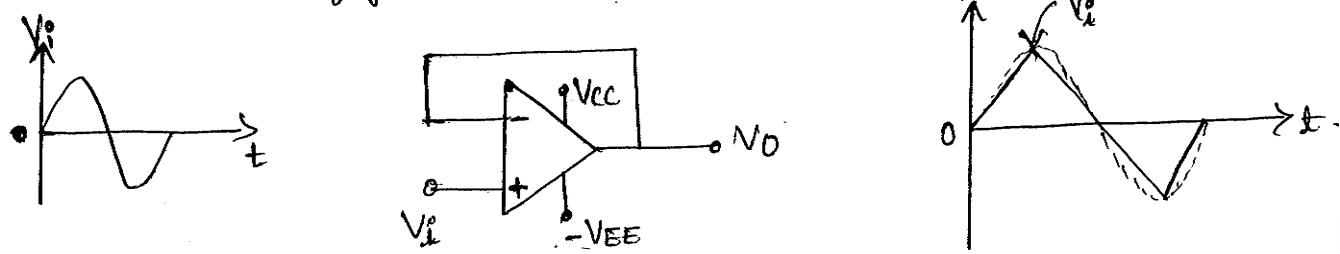


fig ① : Illustrates slew rate being too slow compared to fast rising I/O voltage.

fig ② illustrates a sine wave I/O to a voltage follower producing a triangular O/P waveform.

The triangular wave results because the op-amp simply cannot move fast enough to follow the sine wave I/O.

i.e.,
$$\text{Slew rate} = \frac{\Delta V}{\Delta t}$$

- * The typical slew rate of the 741 op-amp is 0.5 V/ μ sec.
- * If 's' represents the slew rate and ΔV_o is the change in the O/P voltage, then the minimum time required



for satisfactory operation of op-amp is given by

$$\Delta t = \frac{\Delta V_o}{S}$$

FORMULAE

1) Slew rate 'S' = $\frac{\Delta V}{\Delta t}$

2) $\Delta t = \frac{\Delta V_o}{S}$

PROBLEMS

- 1) Determine the typical time required for a 741 op-amp having a 10V O/P change.

Sol:- $t = \frac{\Delta V_o}{S}$

WKT for 741 opamp

$$S = 0.5 \text{ V} / \mu\text{sec.}$$

Given: $\Delta V_o = 10 \text{ V}$

$$\therefore \Delta t = \frac{10 \text{ V}}{0.5 \text{ V} / \mu\text{sec}}$$

$$\Delta t = 20 \mu\text{sec}$$



2) Determine the typical time required for a 741 op-amp o/p to shift from its negative extreme to the positive extreme. The op-amp uses $\pm 12V$ supply & has a typical slew rate of $0.5V/\mu\text{sec}$.

Given :- $\Delta V_o = +12V - (-12V)$

$$\boxed{\Delta V_o = 24V}$$

for 741 op-amp :- $\boxed{S = 0.5V/\mu\text{sec}}$

$$* t = \frac{\Delta V_o}{S} = \frac{24V}{0.5V/\mu\text{sec}} \leftarrow$$

$$\therefore \boxed{t = 48 \mu\text{sec}}$$

3) An op-amp with slew rate of $0.5V/\mu\text{sec}$ is used in an application. find the minimum time required for the circuit to change the o/p by $7V$.

Given :- $S = 0.5V/\mu\text{s}$, $\Delta V_o = 7V$

Sol :- WKT $\Delta t = \frac{\Delta V_o}{S} = \frac{7V}{0.5V/\mu\text{s}}$.

$$\boxed{\Delta t = 14 \mu\text{sec}}$$

4) In response to a square wave I/p, the o/p of an op-amp changed from $-3V$ to $+3V$ over a time interval of $0.25 \mu\text{sec}$. Determine the slew rate of the op-amp.

Given :- $\Delta t = 0.25 \mu\text{sec}$.

$$\Delta V_o = 3 - (-3) = 6V$$

$$S = \frac{\Delta V_o}{\Delta t} = \frac{6}{0.25 \mu\text{sec}}$$

$$\boxed{S = 24V/\mu\text{sec}}$$



Q) How fast can the o/p of an op-amp change by 10V if its slew rate is 1V/ μ sec?

Given :- $\Delta V_o = 10V$, $S = 1V/\mu\text{sec}$.

Sol :- $\Delta t = \frac{\Delta V_o}{S} = \frac{10V}{1V/\mu\text{sec}}$

$\Delta t = 10\mu\text{sec}$

IIP bias current :-

It is defined as the average value of the individual currents flowing into the INV(-) & Non-INV(-) IIP terminals of the op-amp.

$\therefore I_B = \frac{I_{B1} + I_{B2}}{2}$

For 741 :

Typical value is 80nA

Maximum value is 500nA

- i) If the base currents for the emitter coupled transistors of a differential amplifier are $18\mu\text{A}$ & $22\mu\text{A}$, determine
- ii) IIP bias current iii) IIP offset current for an op-amp.

Given :- $I_{B1} = 18\mu\text{A}$, $I_{B2} = 22\mu\text{A}$

i) IIP bias current

$$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{18\mu\text{A} + 22\mu\text{A}}{2} = \underline{\underline{20\mu\text{A}}}$$

ii) IIP offset current

$$I_{os} = |I_{B1} - I_{B2}| = |18\mu\text{A} - 22\mu\text{A}| = \underline{\underline{4\mu\text{A}}}$$



Frequency limitations :-

Sketch & explain a typical gain versus frequency graph for an op-amp.

Jan-10, 4M

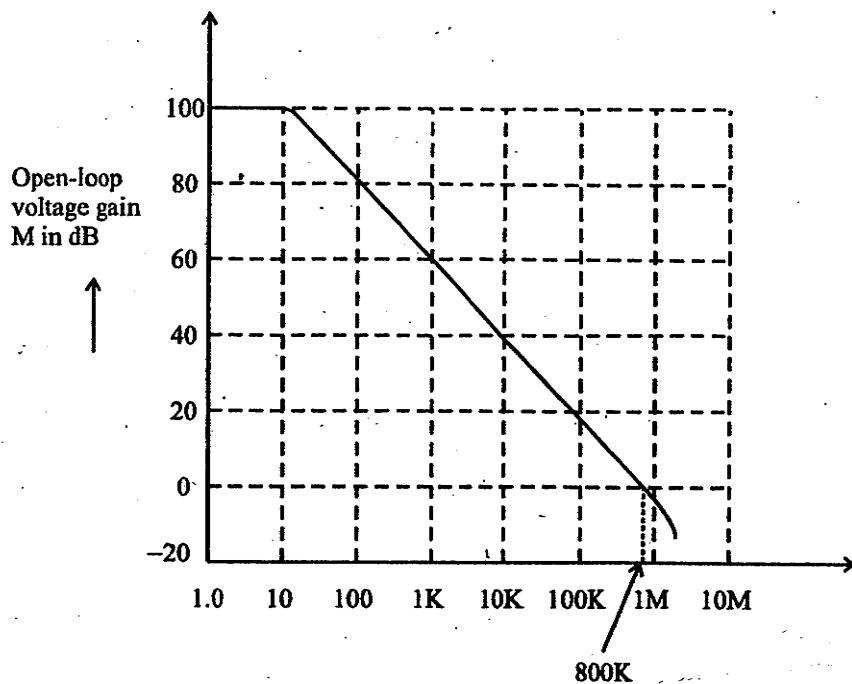


fig ① :- plot of open-loop gain M versus signal frequency ' f ' for a 741 op-amp.

Fig ① : shows the graph of the open-loop gain (M) plotted versus frequency ' f ' for a 741 op-amp.

The frequency is plotted to a logarithmic base & that ' M ' falls linearly as ' f ' increases logarithmically.
 * It is seen that M is 100dB when the signal frequency is 1Hz. At 10Hz the gain has fallen below 100dB and M continues to fall as the signal frequency increases.

$$\text{At } f = 100 \text{ Hz}, \quad M \approx 80 \text{ dB}.$$

$$\text{At } f = 1 \text{ KHz}, \quad M \approx 60 \text{ dB}.$$



* 'M' falls by 20dB when 'f' increases from 100Hz to 1KHz. The ten times increase in frequency is termed a decade.

so, the rate of fall of the gain is said to be 20dB per decade.

* fig ① shows that the 'M' falls to zero at approximately 800KHz

When a gain of around 80dB is required for a particular application, then the 741 op-amp is to be operated upto a frequency of 100Hz only.

When a gain of 20dB is sufficient, then the highest frequency of operation is only 90KHz.

To get larger gains at much higher frequencies, other op-amps must be used.



OP-Amp as DC Amplifiers :-

The op-amps must be correctly biased if they are to function properly. The IIP's of most op-amps are the base terminals of the transistors in a differential amplifier.

Bias currents must flow into these terminals for the transistors to be operational. consequently, the IIP terminals must be directly connected to suitable dc bias voltage source.

Bias current paths :- (DC Biasing)

- * In most of the op-amp applications, the dc bias voltage to be applied to the op-amp IIP terminals will be the average value of the positive & negative supply voltages.

i.e. $\left(\frac{V_{cc}}{2} \text{ or } -\frac{V_{ee}}{2} \right)$

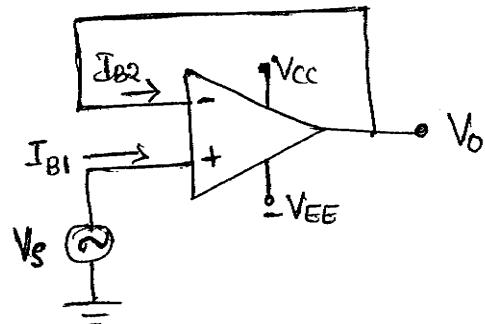
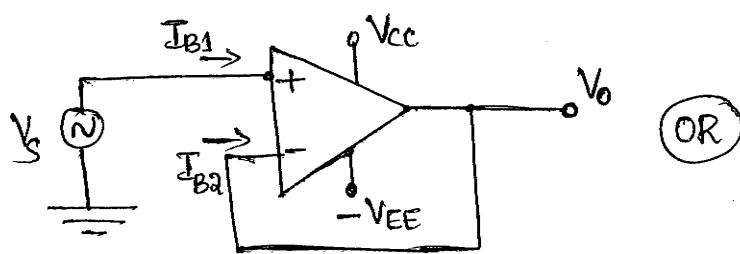


fig 1 : Directly coupled vltg follower.

- * One of the two IIP terminals is usually connected to the op-amp opp to facilitate negative feedback. The other IIP might be biased directly to ground via a signal source as shown in fig ①.



Base current I_{B1} flows into the op-amp via the signal source while I_{B2} flows from the O/p terminal as shown in fig ①.

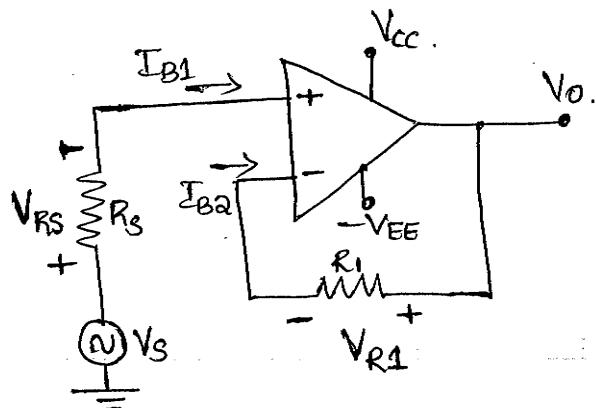


fig ④: R_1 included to match R_g

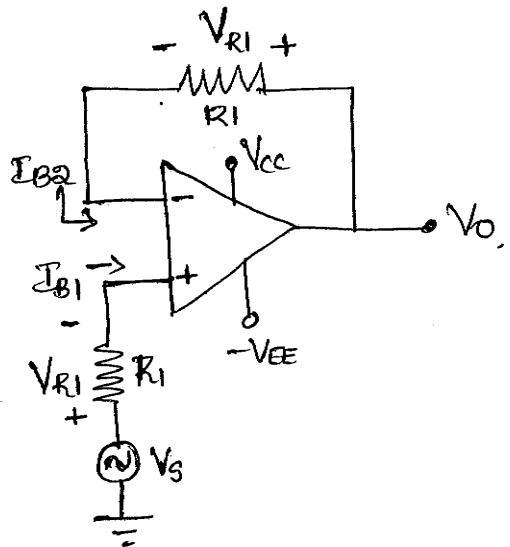


fig ⑤: R_1 included to match R_g .

fig ⑥ shows a resistor ' R_1 ' is included in series with the inverting terminal to match signal source resistance ' R_g ' in series with the non-inverting terminal.

* The op-amp ZIP currents produces voltage drops

$$\text{i.e } V_{Rg} = I_{B1} R_g \text{ & }$$

$$V_{R1} = I_{B2} R_1$$

* R_g & R_1 should be selected as equal resistors. so that the resistor voltage drop are approximately equal. Any difference in these voltage drops will have the same effect as an ZIP offset voltage.



Maximum bias resistor value :-

In fig ⑧, If very small values of resistances R_s & R_i are selected then voltage drop across them will be small. On the other hand if R_s & R_i are very large, the voltage drop $V_{R1} = I_B R_s$ & $V_{R2} = I_B R_i$ might be several volt.

* For good bias stability, the maximum voltage drop across these resistors should be much smaller than the typical forward bias 'V_{BE}' drops across op-amp JFET transistors.

Usually, the voltage drop across these resistors must be made at least ten times smaller than V_{BE}.

$$\text{i.e. } I_B(\text{max}) \cdot R(\text{max}) = \frac{V_{BE}}{10} = \frac{0.7\text{V}}{10} = 0.07\text{V}$$

for 741 op-amp

$$I_B(\text{max}) = 500\text{nA}$$

$$I_B(\text{max}) \cdot R(\text{max}) = 0.07\text{V}$$

$$R(\text{max}) = \frac{0.07\text{V}}{I_B(\text{max})} = \frac{0.07\text{V}}{500\text{nA}}$$

$$\therefore R(\text{max}) = 140\text{k}\Omega$$

In general,

$$R(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})}$$



Potential divider bias :- (voltage follower potential divider bias)

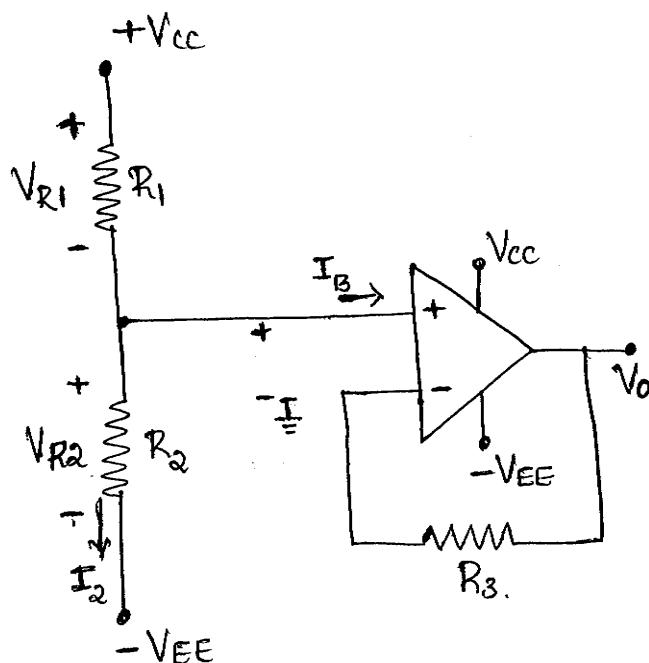


fig ① : Illustrates potential divider

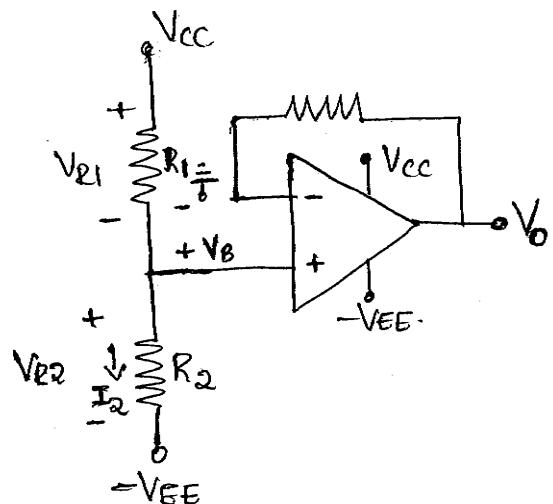


fig ② : Illustrates potential divider.

fig ① shows a potential divider (R_1 & R_2) employed to derive a bias voltage from the two supply voltages, V_{CC} & $-V_{EE}$.

The potential divider current ' I_2 ' should be much larger than the op-amp maximum ZIP bias current.

- * Usually I_2 is made more than 100 times the maximum bias current $I_B(\text{max})$ of op-amp.

Then,

$$R_1 = \frac{V_{R1}}{I_2} \quad \text{and}$$

$$R_2 = \frac{V_{R2}}{I_2}$$



From data sheet of 741 :

$$I_B(\text{max}) = 500 \text{nA}$$

$$\therefore I_2 \geq 100 I_B(\text{max}) \\ \geq 100 \times 500 \text{nA}$$

$$I_2 = 50 \mu\text{A}$$

This is a minimum level for I_2 when 741 is used. In practice, I_2 can be chosen as high as 1mA.

- * The resistance seen when looking out of the Non-INV i/p terminal in fig ① is $R_1 \parallel R_2$.

To equalize the voltage drop at the IIP terminal.

$$I_{B2}R_3 \approx I_{B1}(R_1 \parallel R_2)$$

$$R_3 \approx R_1 \parallel R_2$$

NOTE :-

For op-amp 741 : the IIP voltage range is minimum of $\pm 12\text{V}$ for a $\pm 15\text{V}$ supply.



Potential divider bias with single polarity supply :-

OR

Voltage follower potential divider bias with single polarity supply :-

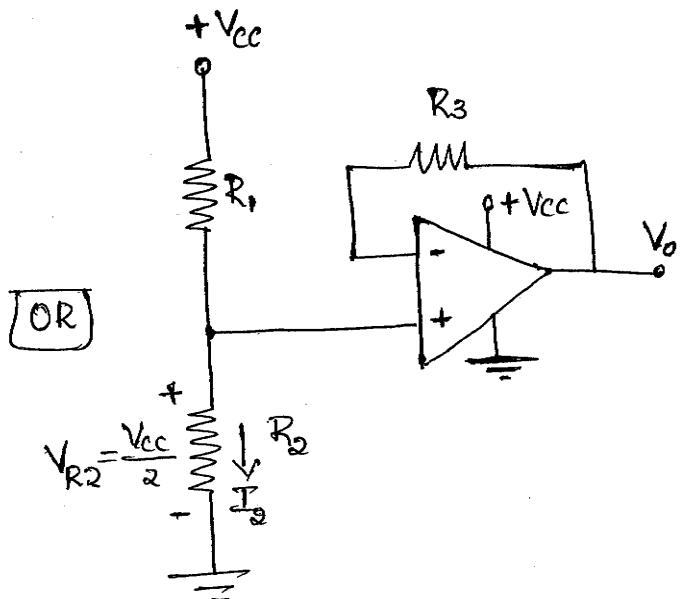
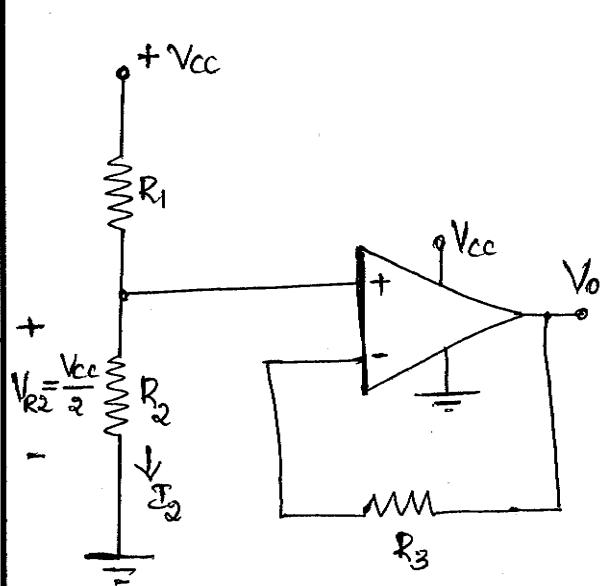


fig ⑤ : Voltage follower potential divider bias with single polarity supply.

- * A single polarity supply voltage can be employed with an op-amp. for 741 op-amp a +30V supply can be used as shown in fig ⑤.
- * In this case, the Zin terminal bias voltage should be approximately half the supply voltage (i.e. $\approx +15V$ for a 30V supply).
- * V_b might be within the Zin voltage range i.e. $\pm 12V$ for a 741 using a $\pm 15V$ supply.
- * fig ⑤ is a voltage follower, the dc off voltage will be equal to the bias voltage level.



Exam Questions :-

- 1) Explain potential divider bias for an op-amp ZILP, with the necessary design steps.

June - 09, 6m

- 2) Explain, with circuit diagram how a dual supply op-amp can be configured to operate with single supply.

Jan - 09, 8m

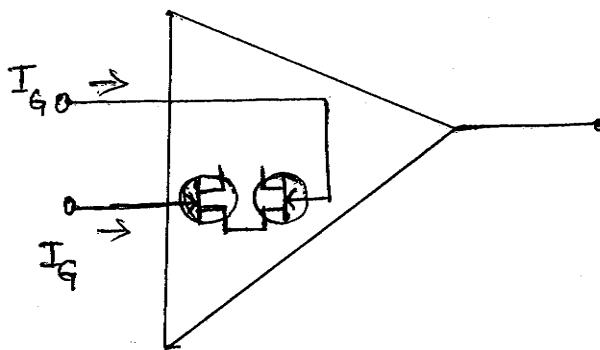
Biasing BIFET OP-Amps :-

fig ① : BIFET op-amp with FET ZILP stages.

- * BIFET op-amps are op-amps with BIFET ZILP stages as shown in fig ①. They draw very low-levels of ZILP bias current i.e 50pA & offer very-high ZILP impedance.
- * The usual design approach of selecting resistors current $100 \times I_B(\text{max})$ would result in very large values of resistors which are undesirable due to the following reasons.



- 1) When the bias resistors at the gate terminal of a FET are extremely large, a charge can accumulate at the gate & this might take a relatively long time to discharge. Then the gate voltage would not be a stable quantity & the op-amps bias conditions would be uncertain.
- 2) If the bias resistors are large, then stray capacitance becomes more effective resulting in unwanted ckt oscillations.

Because of above reasons, the maximum value of resistance when looking out from the TIP of BIFET op-amps should not exceed $1M\Omega$.



Directly Coupled Voltage follower :-

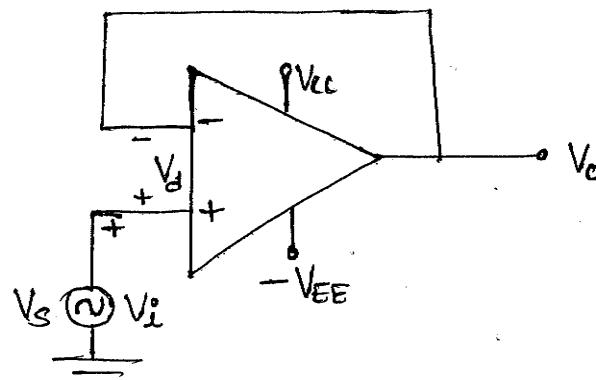


fig ① : Directly coupled voltage follower circ.

* Without using any external components, it is possible to use op-amp as a direct coupled voltage follower circuit as shown in fig ①.

{ Due to very high open loop gain (M) of the op-amp, there will be a very very small difference b/w the IIP vrg ' V_i ' & the O/P voltage V_o . }

The differential IIP should be such as to produce an o/p close to V_i & is given by:

$$V_d = \frac{V_i}{M} \rightarrow ①$$

Where

$M \rightarrow$ open loop gain of op-amp

Applying KVL from IIP to O/P

$$V_i - V_d - V_o = 0$$

$$V_o = V_i - V_d \rightarrow ②$$

Substituting eq ① in eq ②, we get

$$V_o = V_i - \frac{V_i}{M}$$



$$V_o = V_i \left[1 - \frac{1}{M} \right]$$

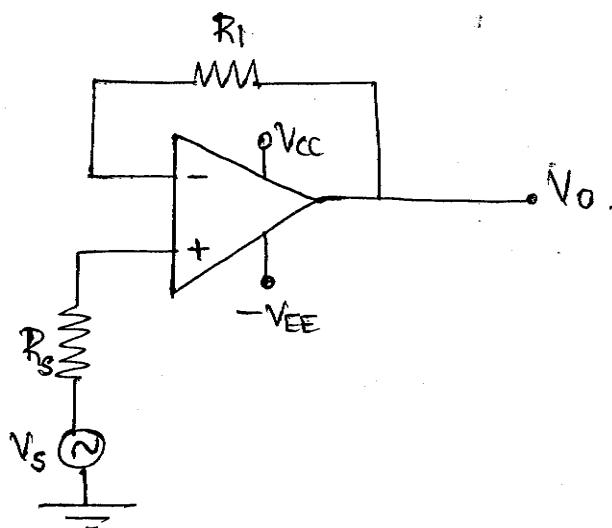


Fig ② : Directly coupled voltage follower with external resistor R_1 .

In directly coupled voltage follower, the resistor R_1 is used between o/p & inverting terminal to match the source resistance R_s .

* Let maximum values of I_{B1} & I_{B2} are $I_{B1(\max)}$ & $I_{B2(\max)}$, then the maximum voltage drop across each resistor is

$$\frac{R_s}{I_{B1(\max)}} = I_{B2(\max)} \cdot R_1$$

* The IIP offset voltage produced is given by

$$V_{ios} = I_{ios} \times (R_s \text{ or } R_1)$$



- * The ZIP impedance of voltage follower is given by,

$$Z_{in} = (1 + M) Z_i$$

$$\therefore [B=1]$$

- * The OIP impedance is given by:

$$Z_{out} = \frac{Z_o}{(1+M)}$$

$$\therefore [B=1]$$

NOTE :-, for voltage follower is $[B=1]$



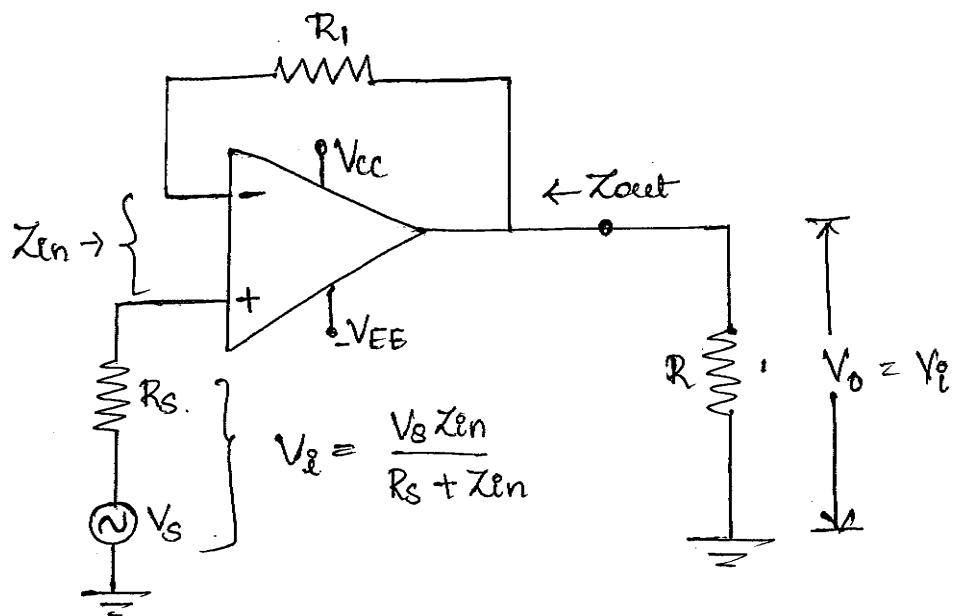
Performance :-Reducing loading effect using voltage follower :-

Fig ① ② : The high o/p impedance of the voltage follower prevents any significant signal loss.

- * The o/p impedance of a voltage follower is very high & is given by

$$Z_{in} = [1 + M] Z_l$$

$$\therefore B=1$$

- * The o/p impedance of a voltage follower is very low & is given by :

$$Z_{out} = \frac{Z_0}{(1+M)}$$

$$\therefore P=1$$

- * Because of high Z_{in} & low Z_{out} , voltage follower is used to convert high impedance source to a low o/p impedance thus acting as a Buffer.



thus voltage follower is also called as Buffer amplifier

- * The load voltage is given by

$$V_L = IR_L$$

where,

$$V_L = \frac{V_0}{R_L + Z_{out}} \cdot R_L$$

$$I = \frac{V_0}{R_L + Z_{out}}$$

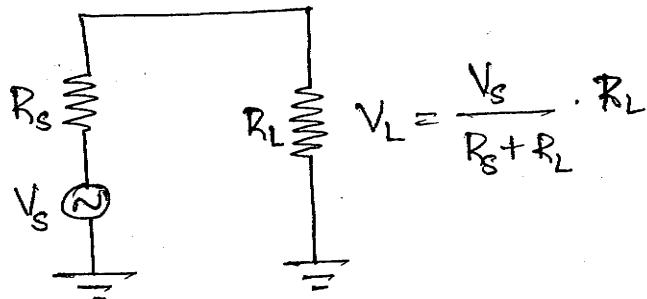
- * Z_{out} is normally much smaller than any load resistance. i.e. $R_L \gg Z_{out}$. thus neglecting Z_{out}

$$V_L = \frac{V_0}{R_L} \cdot R_L$$

$$V_L = V_0$$

thus there is effectively no signal loss & all of opv voltage V_0 appears across load resistance.

- * Consider that load resistor R_L is directly connected to the source as shown in fig ② below



$$V_L = \frac{V_s}{R_s + R_L} \cdot R_L$$

fig ②: part of signal is lost when a load is directly connected.

- * The load voltage is given by :

$$V_L = I R_L$$



$$V_L = \frac{V_s}{R_s + R_L} \cdot R_L$$

where,

$$I = \frac{V_s}{R_s + R_L}$$

Hence some part of V_s gets lost, when load is directly connected.

Directly coupled voltage follower ckt.

FORMULAE

i) Maximum Voltage drop across each resistor

i) $I_{B1}(\text{max}) R_s$

ii) $I_{B2}(\text{max}) R_i$

2) I/p offset voltage produced by the I/p offset current.

$$V_{i(\text{offset})} = I_{i(\text{offset})} \times (R_s \text{ or } R_i)$$

3) S/p Impedance : $Z_{in} = (1 + M) Z_i$

4) O/p Impedance : $Z_{out} = \frac{Z_o}{(1 + M)}$

5) I/p voltage : $V_i = \frac{V_s \times Z_{in}}{R_s + Z_{in}}$

6) Load voltage :

i) When load is directly connected to source

$$V_L = \frac{V_s \times R_L}{R_s + R_L}$$



ii) When the Vtg follower is b/w the load & the source.

$$V_L = \frac{V_o \times R_L}{R_L + Z_{out}}$$

7) o/p voltage : $V_o = V_i \left(1 - \frac{1}{M}\right)$

8) $\beta = 1$

PROBLEMS

1) A voltage follower using a 741 op-amp is connected to a signal source via a $47\text{k}\Omega$ resistor as shown in fig ①. Select a suitable value for resistor R_1 . Also, calculate the maximum voltage drop across each resistor & the maximum I/p offset voltage produced by the I/p offset current.

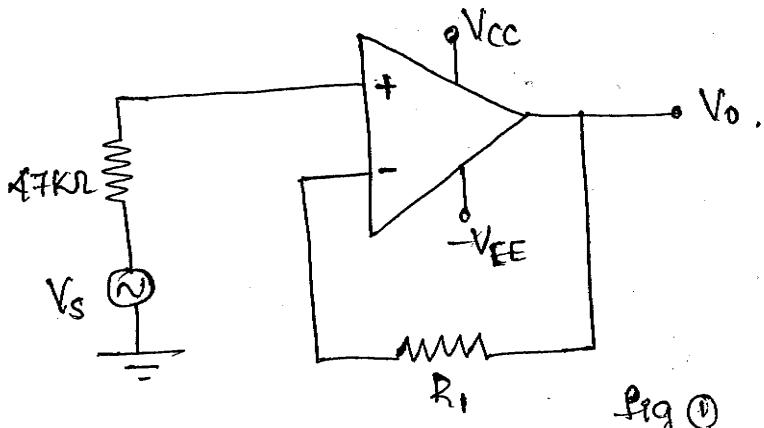


Fig ①

Sol :

$$\text{Given } R_g = 47\text{k}\Omega \quad \therefore R_g = R_1 = 47\text{k}\Omega$$

For op-amp 741, $I_{B(\max)} = 500\text{nA}$ &

$$I_{pos} = 20\text{nA}$$



* The voltage drop across each resistor is

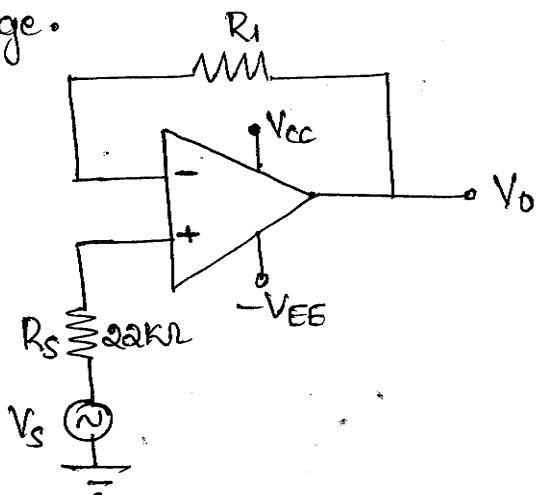
$$\begin{aligned} I_{B1(\max)} \cdot R_S &= I_{B2(\max)} \cdot R \\ &= 500 \text{ nA} \times 47 \text{ k}\Omega \\ &= \underline{\underline{23.5 \text{ mV}}} \end{aligned}$$

* EIP offset voltage

$$\begin{aligned} V_i(\text{offset}) &= I_i(\text{offset}) \times (R_S \text{ or } R_1) \\ &\approx 20 \text{ nA} \times 47 \text{ k}\Omega \end{aligned}$$

$$V_i(\text{offset}) = 0.94 \text{ mV}$$

Q) For the voltage follower circuit shown in fig① select the value of R_1 , calculate the maximum voltage drop across each resistor & maximum input offset voltage.



Given : $R_S = 20 \text{ k}\Omega$

for op-amp 741 : $I_B(\max) = 500 \text{ nA}$

$$I_{ios} = 20 \text{ nA}$$



Sol :-

- * For matching, the voltage drops, R_1 must be selected equal to R_S

$$\therefore R_1 = R_S = 22\text{ k}\Omega$$

- * The voltage drop across each resistor is.

$$I_{B1(\max)} \cdot R_S = I_{B2(\max)} R_1 = 500\text{ nA} \times 22\text{ k}\Omega = 11\text{ mV}$$

- * IIP offset voltage :

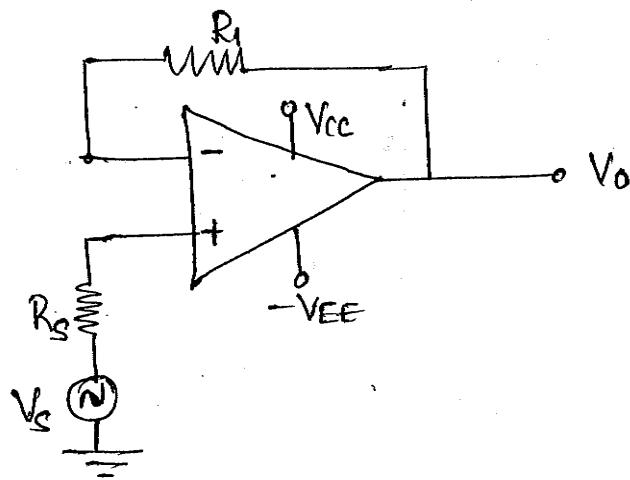
$$V_{ios} = I_i(\text{offset}) \times (R_S \text{ or } R_1)$$

$$= 20\text{ nA} \times 22\text{ k}\Omega$$

$$V_i(\text{offset}) = 0.44\text{ mV}$$

$$\left\{ V_{ios} = V_i(\text{offset}) \right\}$$

- 3) A signal source with a resistance of $15\text{ k}\Omega$ is connected to a LM 108 op-amp working as a direct coupled voltage follower of fig ①. Select a suitable value for R_1 & determine the maximum voltage drop across each resistor. Also determine the maximum IIP offset voltage produced by the IIP offset current. Assume $I_B(\max) = 2\text{nA}$ & $I_i(\text{offset}) = 0.2\text{nA}$ for LM 108 op-amp.



Given : $R_S = 15 \text{ k}\Omega$, $I_B(\text{max}) = 2 \text{ mA}$, $I_E(\text{offset}) = 0.2 \text{ mA}$.

Sol :-

* The value of R_I is chosen same as equal to R_S

$$\therefore R_S = R_I = 15 \text{ k}\Omega$$

* Maximum voltage drop across each collector

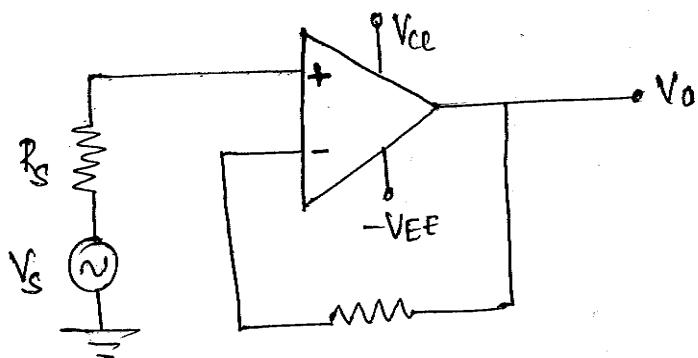
$$= I_B(\text{max}) \cdot R_I = I_B(\text{max}) \cdot R_S = 2 \times 10^{-3} \times 15 \times 10^3 = 30 \mu\text{V}$$

* Maximum Z_{IP} offset voltage :

$$\begin{aligned} V_{E(\text{offset})} &= I_E(\text{offset}) \times (R_I \text{ or } R_S) \\ &= 0.2 \times 10^{-3} \times 15 \times 10^3 \end{aligned}$$

$$V_{E(\text{offset})} = 3 \mu\text{V}$$

- 4) A voltage follower using a 741 op-amp is connected to a signal source via a $50 \text{ k}\Omega$ resistor, as in fig @. Select a suitable value for resistor R_I . Also calculate the maximum voltage drop across each collector & the maximum Z_{IP} offset voltage produced by the Z_{IP} offset current.



Given : $R_S = 50 \text{ k}\Omega$

For op-amp 741 : $I_B(\text{max}) = 500 \text{ nA}$ & $I_{IO} = 20 \text{ nA}$

Sol :-

* The value of R_I is chosen same as equal to R_S

$$\therefore R_S = R_I = 50 \text{ k}\Omega$$

* Maximum voltage drop across each resistor

$$= I_B(\text{max}) R_I = I_B(\text{max}) R_S = 2 \times 10^{-9} \times 50 \times 10^3 = 25 \text{ mV}$$

* Maximum input offset voltage :

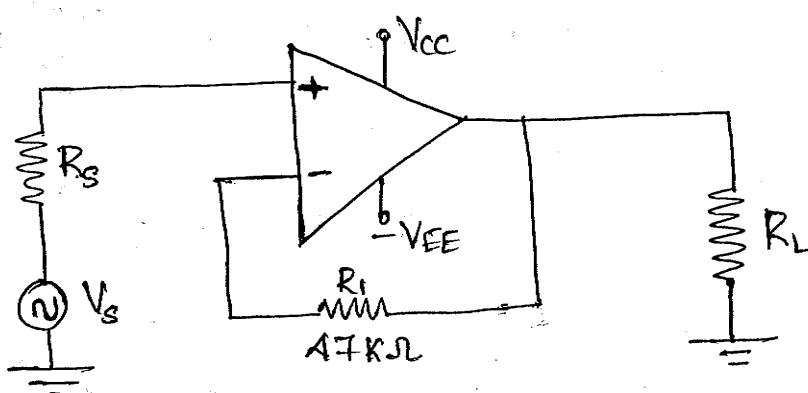
$$V_i(\text{offset}) = I_{i(\text{offset})} \times (R_I \text{ or } R_S)$$

$$\approx 20 \text{ nA} \times 50 \text{ k}\Omega$$

$$V_i(\text{offset}) = 1 \text{ mV}$$

5) The voltage follower in fig ① has a 1V Signal & a $20\text{k}\Omega$ load. calculate the load voltage.

- ② When the load is directly connected to source.
 ⑥ When the voltage follower is between the load & the source.



Given :- $V_s = 1V$, $R_s = 47k\Omega$, $R_L = 20k\Omega$

For 741 op-amp : $M = 200000$, $Z_i = 2M\Omega$ & $Z_o = 75\Omega$.

a) When the load is directly connected to the source

$$V_L = \frac{V_s \times R_L}{R_s + R_L} = \frac{1V \times 20k\Omega}{47k\Omega + 20k\Omega}$$

$$\boxed{V_L = 298mV}$$

b) When the voltage follower is between the load & the source :

$$V_i = \frac{V_s \times Z_{in}}{R_s + Z_{in}}$$

$$Z_{in} = (1+M) Z_i = (1+200000) 2M\Omega$$

$$\boxed{Z_{in} = 4 \times 10^{11}\Omega}$$

$$\therefore V_i = \frac{1V \times (4 \times 10^{11}\Omega)}{47k\Omega + 4 \times 10^{11}\Omega}$$

$$\boxed{V_i = 1V}$$

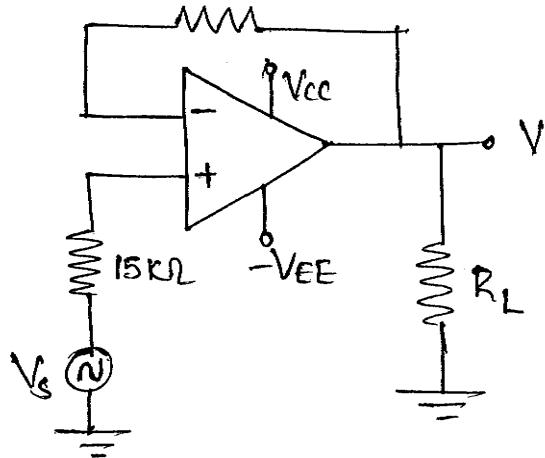
$$* V_o = V_i \left(1 - \frac{1}{M}\right) = 1V \left(1 - \frac{1}{200000}\right) \therefore \boxed{V_o = 1V}$$

$$* \text{ O/p Impedance : } Z_{out} = \frac{Z_o}{(1+M)} = \frac{75\Omega}{(1+200000)} = \underline{\underline{37 \times 10^{-5}\Omega}}$$

$$* \text{ Load voltage : } V_L = \frac{V_o \times R_L}{R_L + Z_{out}} = \frac{1V \times 20k\Omega}{20k\Omega + (37 \times 10^{-5}\Omega)} = \underline{\underline{1V}}$$



- 6) If the voltage follower of fig ① has a 200mV sinp signal & a 5k Ω load, determine the load voltage
 i) when the load is directly connected to the source.
 ii) when the voltage follower is used. for LM 108,
 $M = 3,00,000$, $Z_i = 70M\Omega$ and $Z_o = 75\Omega$



Given :- $V_s = 200\text{mV}$, $R_s = 15\text{k}\Omega$, $R_L = 5\text{k}\Omega$, $M = 300000$,
 $Z_i = 70M\Omega$ & $Z_o = 75\Omega$

- i) When the load is directly connected to the source

$$V_L = \frac{V_s R_L}{R_s + R_L} = \frac{200\text{mV} \times 5\text{k}\Omega}{15\text{k}\Omega + 5\text{k}\Omega}$$

$$\boxed{V_L = 50\text{mV}}$$

- ii) When the voltage follower is between the load & the source:

$$V_i = \frac{V_s \cdot Z_{in}}{R_s + Z_{in}}$$

$$Z_{in} = (1+M) Z_i = (1+300000) 70 \times 10^3 \Omega$$

$$\boxed{Z_{in} = 201 \times 10^{13} \Omega}$$



$$* V_i = \frac{V_s \times Z_{in}}{R_s + Z_{in}} = \frac{(200 \text{ mV}) \times (201 \times 10^{13})}{15 \times 10^3 + 201 \times 10^{13}}$$

$$V_i = 200 \text{ mV}$$

$$* V_o = V_i \left(1 - \frac{1}{M}\right) = 200 \text{ mV} \left(1 - \frac{1}{300000}\right)$$

$$V_o = 200 \text{ mV}$$

$$* Z_{out} = \frac{Z_0}{(1+M)} = \frac{75 \Omega}{(1+300000)}$$

$$Z_{out} = 2.5 \times 10^{-4} \Omega$$

* The load voltage is given by:

$$V_L = \frac{V_o \times R_L}{R_L + Z_{out}} = \frac{200 \text{ mV} \times 5 \times 10^3}{5 \times 10^3 + 2.5 \times 10^{-4}}$$

$$V_L = 200 \text{ mV}$$

7) A load resistance of $22 \text{ k}\Omega$ is to be connected to a source of 1.5 V with source resistance of $56 \text{ k}\Omega$. calculate the load voltage if

i) Load is directly connected.

ii) Load is connected through voltage follower using o-p op-amp with $Z_0 = 75 \Omega$, $Z_i = 2 \text{ M}\Omega$ & $M = 2 \times 10^5$.



Given :- $R_L = 22\text{ k}\Omega$, $R_S = 56\text{ k}\Omega$, $V_S = 1.5\text{ V}$, $Z_0 = 75\text{ V}$,
 $Z_i = 2\text{ M}\Omega$. & $M = 2 \times 10^5$.

Sol :- i) When load is directly connected :

$$V_L = \frac{V_S R_L}{R_S + R_L} = \frac{1.5\text{ V} \times 22\text{ k}\Omega}{56\text{ k}\Omega + 22\text{ k}\Omega}$$

$$V_L = 0.42307\text{ V}$$

ii) When load is connected through voltage follower:

* $Z_{in} = (1+M) Z_i = (1+2 \times 10^5) 2 \times 10^6$

$$Z_{in} = 4 \times 10^{11}\Omega$$

* $V_i = \frac{V_S \times Z_{in}}{R_S + Z_{in}} = \frac{1.5\text{ V} \times 4 \times 10^{11}}{56 \times 10^3 + 4 \times 10^{11}} = 1.4999\text{ V}$

$$V_i \approx 1.5\text{ V}$$

* $V_o = V_i \left[1 - \frac{1}{M} \right] = 1.5\text{ V} \left(1 - \frac{1}{2 \times 10^5} \right)$

$$V_o = 1.4999\text{ V}$$

* $Z_{out} = \frac{Z_0}{1+M} = \frac{75\Omega}{1+2 \times 10^5} = \underline{\underline{3.7499 \times 10^{-4}\Omega}}$

* $V_L = \frac{V_o R_L}{R_L + Z_{out}} = \frac{1.4999 \times 22 \times 10^3}{22 \times 10^3 + 3.7499 \times 10^{-4}} = \underline{\underline{1.4999\text{ V}}}$

$$V_L \approx 1.4999\text{ V}$$



Voltage follower using potential divider bias :-

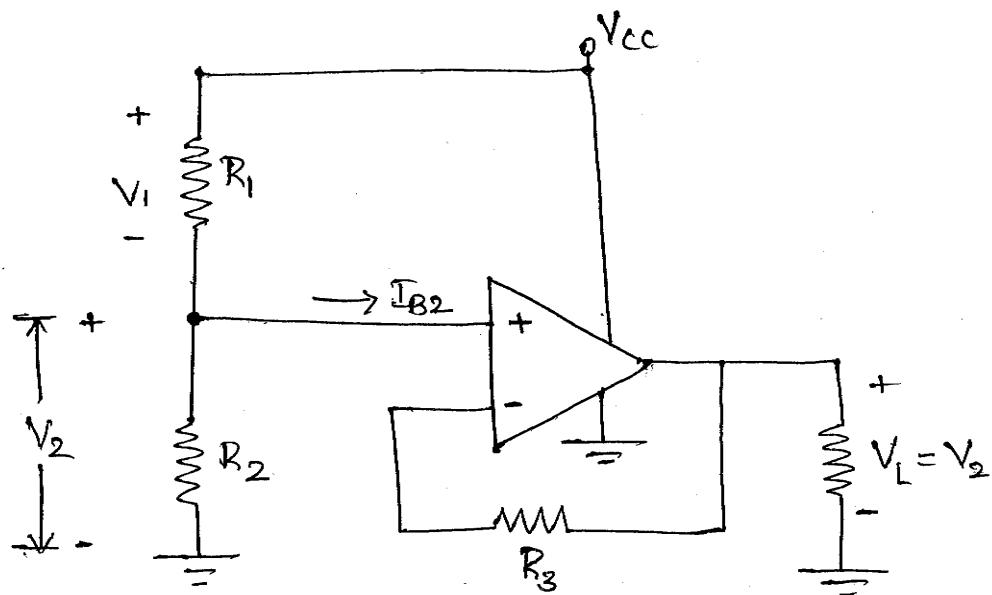


fig 1 @ : A potential divider & voltage follower produces a constant V_L .

{
OR

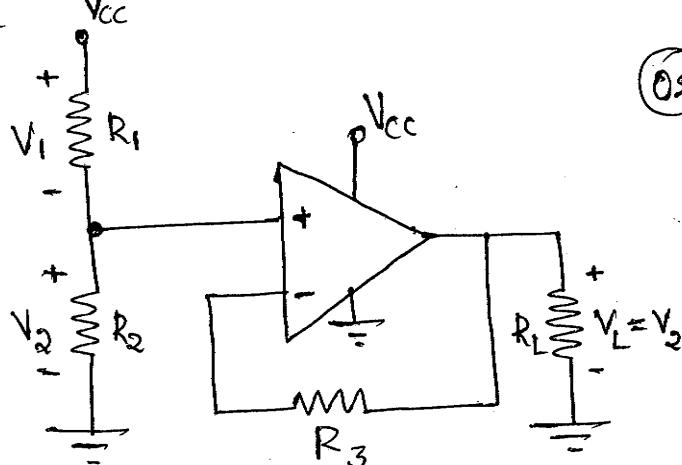


fig 1 @

OR

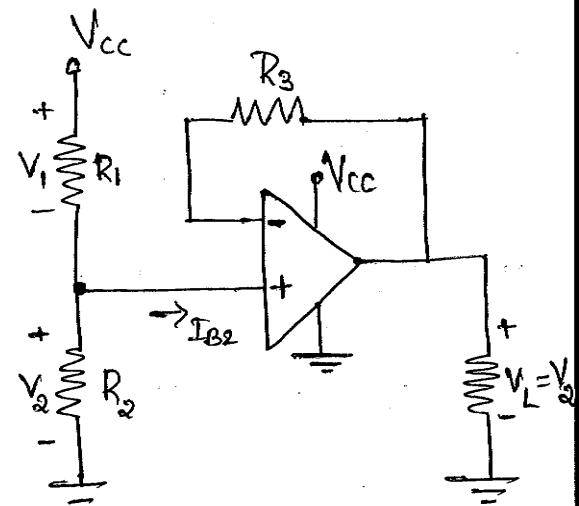


fig 1 @

}

A potential divider bias can be used to bias a voltage follower circuit as shown in fig ①@ with negative supply terminal of op-amp being grounded.



The presence of the voltage follower maintains the load voltage constant regardless of the load resistor value.

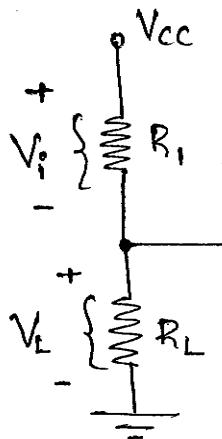
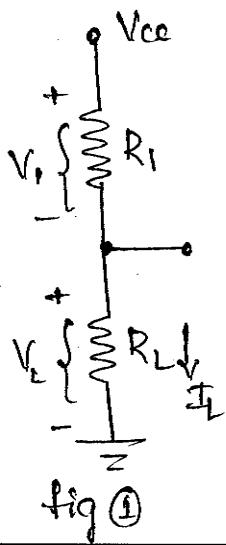


fig 1⑥ shows load R_L directly connected to supply through R_1 without using voltage follower.

In fig 1⑥, load R_L is directly connected in series with resistor R_1 to derive a voltage V_L from the supply V_{cc} . The arrangement has the disadvantage that the load varies if the load resistance changes.

Design procedure :-

- 1) A potential divider bias directly connected to load ' R_L ' (without voltage divider)



$$1) I_L = \frac{V_L}{R_L}$$

2) Applying KVL to the ckt

$$V_{cc} - V_i - V_L = 0$$

$$\boxed{V_L = V_{cc} - V_i}$$

$$3) R_1 = \frac{V_i}{I_L}$$



4) $V_L = I_L R_L$

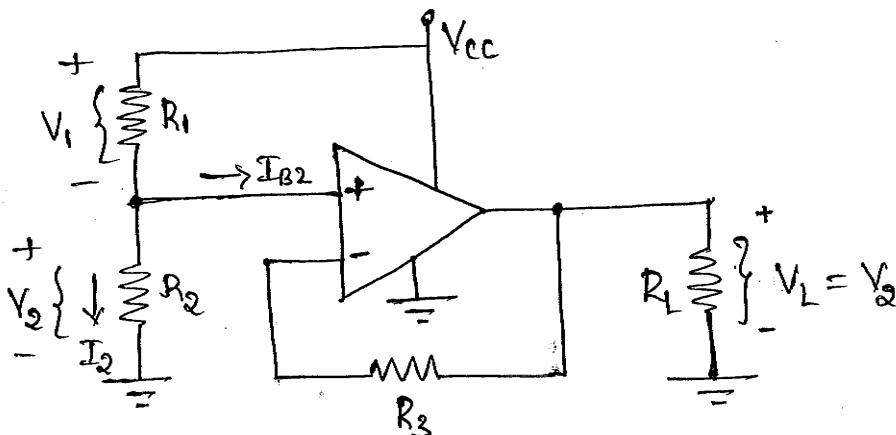
where $I_L = \frac{V_{CC}}{R_1 + R_L}$

$$\therefore V_L = \frac{V_{CC} R_L}{R_1 + R_L}$$

5) When R_L changes (say -10%).

$$V_L = \frac{V_{CC} (R_L - 10\% \text{ of } R_L)}{R_1 + (R_L - 10\% \text{ of } R_L)}$$

ii) potential divider bias used to bias voltage follower.



1) $V_2 = V_L$

2) $V_1 = V_{CC} - V_L$

3) $I_2 = 100 I_B (\text{max})$

4) $R_2 = \frac{V_2}{I_2}$

5) $R_1 = \frac{V_1}{I_2}$

6) when R_L changes (by say -10%)

$$V_L = V_2$$

7) $R_3 = R_1 \parallel R_2$.



1) A $1\text{k}\Omega$ load is to have 5V developed across it from a 15V source. Design suitable circuit & calculate the load voltage variation in each case when the load resistance varies by -10%. Use a 741 op-amp.

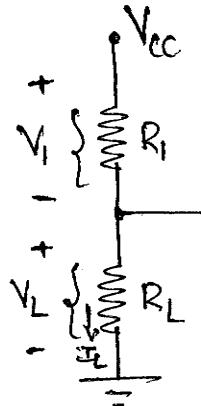


fig 1@

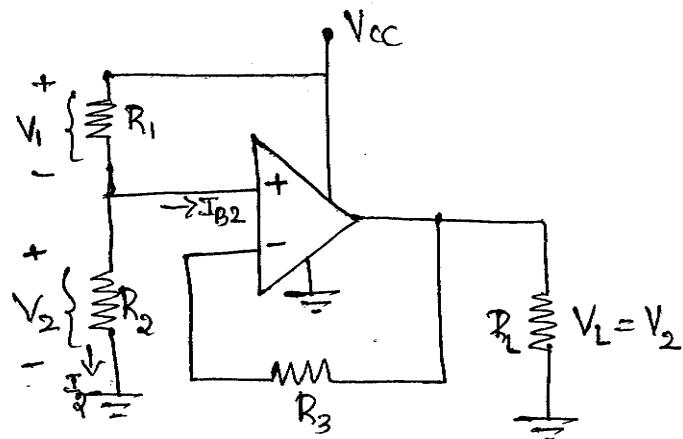


fig 1(b)

Given :-

$$R_L = 1\text{k}\Omega, V_L = 5\text{V}, V_{cc} = 15\text{V}$$

Sol :-

i) For fig 1@ :

$$\star I_L = \frac{V_L}{R_L} = \frac{5\text{V}}{1\text{k}\Omega} = 5\text{mA} \quad \therefore I_L = 5\text{mA}$$

$$\star V_1 = V_{cc} - V_L = 15\text{V} - 5\text{V} = 10\text{V} \quad \therefore V_1 = 10\text{V}$$

$$\star R_1 = \frac{V_1}{I_L} = \frac{10\text{V}}{5\text{mA}} = 2\text{k}\Omega \quad \therefore R_1 = 2\text{k}\Omega$$

\star When R_L changes by -10%

$$V_L = \frac{V_{cc} \times (R_L - 10\% \text{ of } R_L)}{R_1 + (R_L - 10\% \text{ of } R_L)} = \frac{15\text{V} \times (1\text{k}\Omega - 100\Omega)}{2\text{k}\Omega + (1\text{k}\Omega - 100\Omega)}$$

$$= \frac{15\text{V} \times 900\Omega}{2900\Omega}$$

$$V_L = 4.655\text{V}$$



ii) For fig 1 (b): Here $V_L = V_2 = 5V$

WKT for op-amp 741: $I_B(\text{max}) = 500\text{nA}$

* Let $I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA} = 50\mu\text{A}$

$$I_2 = 50\mu\text{A}$$

$$R_2 = \frac{V_2}{I_2} = \frac{5V}{50\mu\text{A}}$$

$$R_2 = 100\text{k}\Omega$$

$$R_1 = \frac{V_1}{I_2} = \frac{10V}{50\mu\text{A}}$$

$$R_1 = 200\text{k}\Omega$$

* When R_L changes by -10%

$$V_L = V_2 = 5V \quad \therefore V_L = 5V$$

$$* R_3 = R_1 \parallel R_2 = 200\text{k}\Omega \parallel 100\text{k}\Omega$$

$$R_3 = 66.66\text{k}\Omega$$

2) A voltage of 3 volts is needed across a load resistor of value $12\text{k}\Omega$. The supply voltage available is +24 volts. Design the resistor values in the circuits of fig 1 & fig 3 and determine the load voltage variation in each case when the load resistance increases by 20%. Use op-amp with parameters: $I_B(\text{max}) = 500\text{nA}$, $Z_o = 75\Omega$, $M = 2 \times 10^5$.



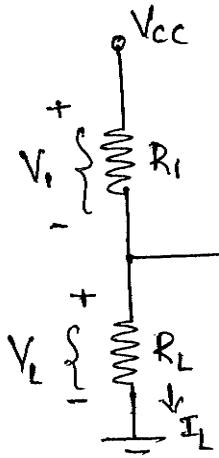


fig ①

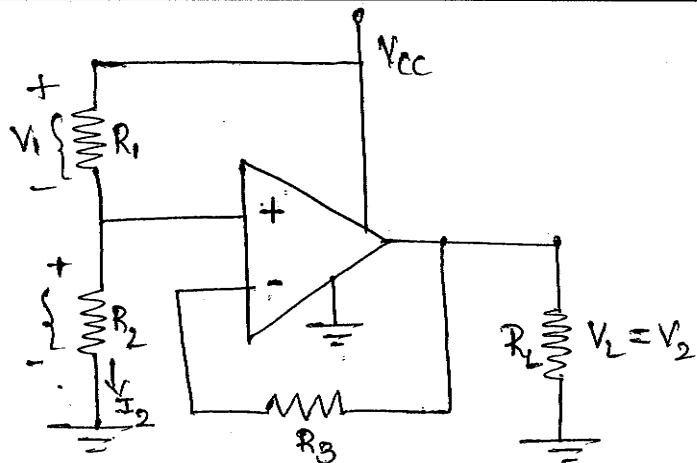


fig ②

Given :- $V_L = 3V$, $R_L = 12\text{ k}\Omega$, $V_{CC} = 24V$

$I_B(\text{max}) = 500\text{nA}$, $Z_0 = 75\Omega$, $M = 2 \times 10^5$

SOL:-

i) For fig ①

$$\ast I_L = \frac{V_L}{R_L} = \frac{3V}{12\text{ k}\Omega} = 250\mu\text{A} \quad \therefore I_L = 250\mu\text{A}$$

$$\ast V_I = V_{CC} - V_L = 24V - 3V \quad V_I = 21V$$

$$\ast R_I = \frac{V_I}{I_L} = \frac{21V}{250\mu\text{A}} = 84\text{ k}\Omega \quad R_I = 84\text{ k}\Omega$$

* When R_L changes by +20%

$$\text{i.e } R_L = 12\text{ k}\Omega + (0.2 \times 12\text{ k}\Omega) = 14.4\text{ k}\Omega$$

$$R_L = 14.4\text{ k}\Omega$$

$$V_L = \frac{V_{CC} \cdot R_L}{R_I + R_L} = \frac{24V \times 14.4\text{ k}\Omega}{84\text{ k}\Omega + 14.4\text{ k}\Omega}$$

$$V_L = 3.51V$$



ii) for fig ③ : Here $V_L = V_2 = 3V$

$$V_1 = V_{CC} - V_2 = 24V - 3V = \underline{\underline{21V}}$$

* Let $I_2 = I_B(\text{max}) \times 100$

$$\approx 100 \times 500 \mu A$$

$$I_2 = 50 \mu A$$

$$* R_2 = \frac{V_2}{I_2} = \frac{3V}{50 \mu A} = \underline{\underline{60 k\Omega}}$$

$$\therefore R_2 = 60 k\Omega$$

$$* R_1 = \frac{V_1}{I_2} = \frac{21V}{50 \mu A} = \underline{\underline{420 k\Omega}}$$

$$\therefore R_1 = 420 k\Omega$$

$$* R_3 = R_1 \parallel R_2 = \frac{420 k\Omega \times 60 k\Omega}{420 k\Omega + 60 k\Omega} = 52.5 k\Omega$$

$$R_3 = 52.5 k\Omega$$

* When R_L changes by +20%

$$V_L = V_2 = 3V$$

$$\therefore V_L = 3V$$

3) It is required to obtain 2V across 1kΩ load from 10V supply voltage. Design the circuit without & with voltage follower. Hence calculate the change in load voltage if R_L changes by -5%. Use 741 op-amp.

Given: $R_L = 1k\Omega$, $V_L = 2V$, $V_{CC} = 10V$.



For op-amp 441 : $I_B(\text{max}) = 500\text{nA}$

i) potential divider without using voltage divider.

$$* I_L = \frac{V_L}{R_L} = \frac{2V}{1k\Omega} = 2\text{mA} \quad \therefore I_L = 2\text{mA}$$

$$* V_i = V_{cc} - V_L = 10V - 2V = 8V \quad \therefore V_i = 8V$$

$$* R_i = \frac{V_i}{I_L} = \frac{8V}{2\text{mA}} = 4k\Omega \quad \therefore R_i = 4k\Omega$$

* When R_L changes by -5%.

$$R_L' = R_L - (5\% \text{ of } R_L) = 1k\Omega - 50\Omega$$

$$R_L' = 950\Omega$$

$$V_L' = \frac{V_{cc} \cdot R_L'}{R_i + R_L'} = \frac{10V \times 950\Omega}{4k\Omega + 950\Omega} = 1.9191V$$

ii) potential divider bias with voltage follower

$$\text{Here } V_2 = V_L = 2V$$

$$* I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA} = 50\mu\text{A}$$

$$I_2 = 50\mu\text{A}$$

$$* R_2 = \frac{V_2}{I_2} = \frac{2V}{50\mu\text{A}} \quad \therefore R_2 = 40k\Omega$$

$$* R_1 = \frac{V_i}{I_2}$$

$$V_i = V_{cc} - V_L = 10V - 2V$$

$$V_i = 8V$$



$$R_1 = \frac{V_1}{I_2} = \frac{8V}{50\mu A} = \underline{\underline{160k\Omega}} \quad \therefore R_1 = 160k\Omega$$

* When R_L changes by -5%.

$$V_L = V_2 = 2V$$

$$\therefore V_L = 2V$$

- * Comparison of voltage follower and Emitter follower.
- * Compare a voltage follower and an emitter follower.

Jcne - 08, 4M

<u>Voltage follower</u>	<u>Emitter follower</u>
1)	1)
2) Voltage follower are buffer amplifier.	2) Emitter follower are also buffer amplifier.
3) Much higher Z/p impedance than emitter follower	3) Z/p impedance is lesser than voltage follower.
4) Much lower o/p impedance than emitter follower	4) o/p impedance is higher than voltage follower.
5) The dc loss is $\frac{V_i}{M}$ which is very small.	5) The dc loss is the voltage drop of the transistor i.e V_{BE}
6) Ac signal voltage loss is very less compared to emitter follower	6) Ac signal voltage loss is more than voltage follower.



Directly - coupled Non-Inverting amplifiers :-

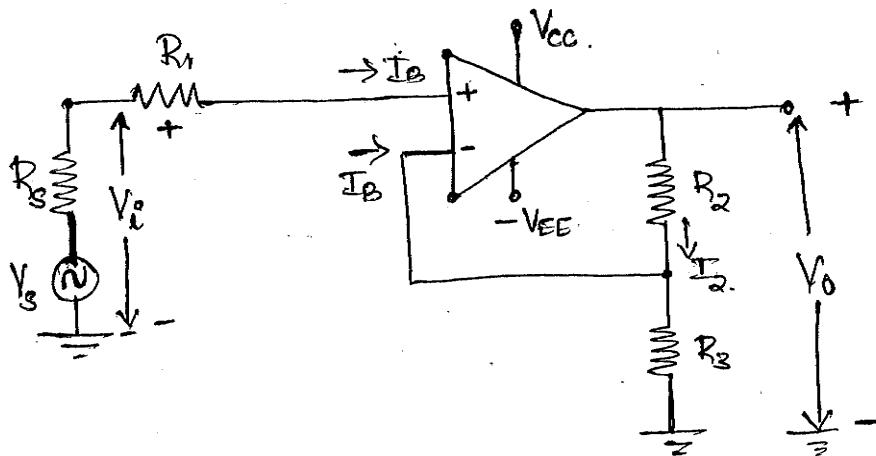


Fig ① : Directly - coupled Non-INV amplifier.

* The voltage gain of Non-INV amplifier is

$$A_V = \frac{R_2 + R_3}{R_3}$$

$$\therefore A_V = 1 + \frac{R_2}{R_3}$$

Design steps :-

→ The potential divider resistor values are determined by using V_i , V_o and I_2

$$\ast R_3 = \frac{V_{R3}}{I_2} \quad \text{but} \quad V_{R3} = V_o \quad \therefore R_3 = \frac{V_o}{I_2}$$

* The o/p voltage 'V_o' appears across $(R_2 + R_3)$
Applying KVL to o/p circuit

$$V_o - I_2 R_2 - I_2 R_3 = 0.$$

$$V_o = I_2 (R_2 + R_3)$$

$$R_2 + R_3 = \frac{V_o}{I_2}$$

$$\therefore R_2 = \frac{V_o}{I_2} - R_3$$



3) To equalize the $I_B R$ voltage drop at the op-amp IIP's, R_1 is calculated as :

$$R_1 = (R_2 \parallel R_3)$$

3) If R_1 as determined from above equation is not very much larger than the source resistance i.e. $R_1 \ll R_S$ then,

$$(R_S + R_1) = (R_2 \parallel R_3)$$

PROBLEMS

1) Using a 741 op-amp, design a non-inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15 mV.

Given : $A_v = 66$, $V_i = 15 \text{ mV}$

For 741 op-amp : $I_B(\text{max}) = 500 \text{nA}$.

Sol: Let $I_Q = 100 \times I_B(\text{max})$
 $= 100 \times 500 \text{nA}$

$$I_Q = 50 \mu\text{A}$$

* $R_3 = \frac{V_i}{I_Q} = \frac{15 \text{ mV}}{50 \mu\text{A}} = 300 \Omega$

∴ $R_3 = 300 \Omega$

* Use a standard value resistor i.e. $R_3 = 270 \Omega$

Now I_Q level changes i.e.

I_Q becomes $I_Q = \frac{V_i}{R_3} = \frac{15 \text{ mV}}{270 \Omega}$

$$I_Q = 55.6 \text{ mA}$$



* WKT $A_V = \frac{V_o}{V_i}$

$$V_o = A_V V_i = 66 \times 15 \text{ mV}$$

$V_o = 990 \text{ mV}$

* $R_2 + R_3 = \frac{V_o}{I_2}$

$$R_2 = \left(\frac{V_o}{I_2} - R_3 \right) = \left(\frac{990 \text{ mV}}{55.6 \mu\text{A}} - 270 \Omega \right)$$

$$R_2 = 17.80 \text{ k}\Omega - 270 \Omega$$

$R_2 = 17.53 \text{ k}\Omega$

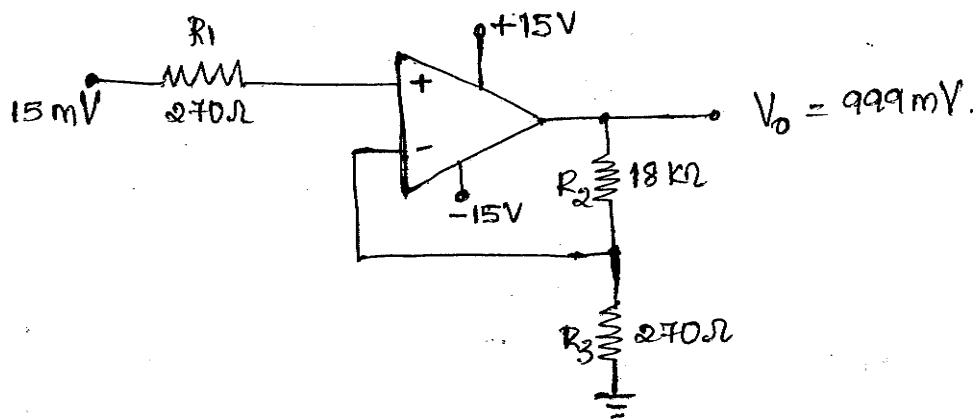
Use standard value of R_2 i.e.

$R_2 = 18 \text{ k}\Omega$

* $R_1 = (R_2 \parallel R_3) = \frac{18 \text{ k}\Omega \times 270 \Omega}{18 \text{ k}\Omega + 270 \Omega}$

$R_1 = 265.2 \Omega$

Use standard value of R_1 i.e. $R_1 = 270 \Omega$



2) Design a Non-INV amplifier with a voltage gain of 51 and signal voltage of 10 mV. use Op-amp 741.

Given :- $A_V = 51$, $V_i = 10 \text{ mV}$

for 741 op-amp : $I_B(\text{max}) = 500 \text{nA}$

Sol :- Let $I_2 = 100 \times I_B(\text{max}) = 100 \times 500 \text{nA}$

$$I_2 = 50 \mu\text{A}$$

* $R_3 = \frac{V_o}{I_2} = \frac{10 \text{ mV}}{50 \mu\text{A}} = 200 \Omega$

$$R_3 = 200 \Omega$$

Use standard value $R_3 = 180 \Omega$

Now I_2 becomes :

$$I_2 = \frac{V_i}{R_3} = \frac{10 \text{ mV}}{180 \Omega}$$

$$I_2 = 55.5 \mu\text{A}$$

* WKT $V_o = A_V \times V_i = 51 \times 10 \text{ mV}$

$$V_o = 510 \text{ mV}$$

* $(R_2 + R_3) = \frac{V_o}{I_2}$

$$= \frac{510 \text{ mV}}{55.5 \mu\text{A}}$$

$$= 9.18 \text{ k}\Omega$$

$$R_2 = 9.18 \text{ k}\Omega - R_3 = 9.18 \text{ k}\Omega - 180 \Omega$$

$$R_2 = 9 \text{ k}\Omega$$

Use standard value of

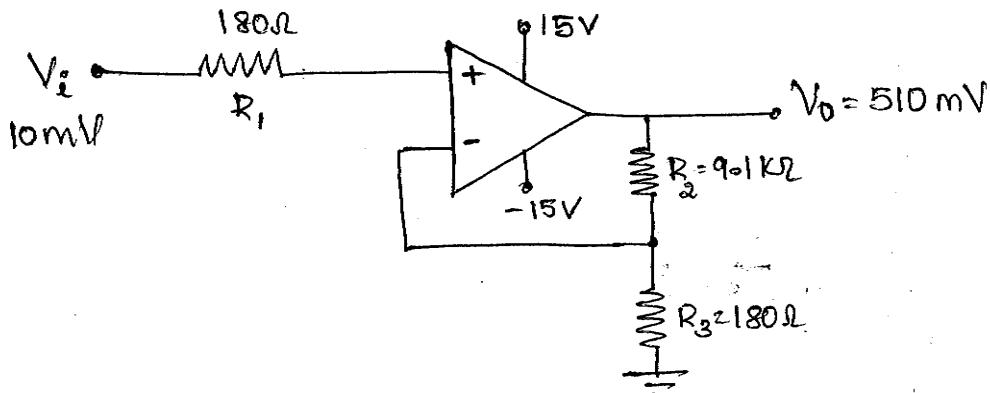
$$R_2 = 9.1 \text{ k}\Omega$$



$$* R_1 = (R_2 \parallel R_3) = \frac{9.1\text{k}\Omega \times 180\Omega}{9.1\text{k}\Omega + 180\Omega}$$

$$R_1 = 176.5\Omega$$

Use standard value of $R_1 = 180\Omega$



3) Design a Non-INV amplifier to have a voltage gain of 40 using a 741 op-amp. The signal amplitude is to be 2mV.

Given :- $V_i = 12\text{mV}$, $A_V = 40$

for 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

Sol :- Let $I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$I_2 = 50\mu\text{A}$$

$$* R_3 = \frac{V_o}{I_2} = \frac{12\text{mV}}{50\mu\text{A}} = 240\Omega$$

$$R_3 = 240\Omega$$

* Use a standard value resistor i.e.

$$R_3 = 220\Omega$$

Now I_2 becomes.

$$I_2 = \frac{V_o}{R_3} = \frac{12\text{mV}}{220\Omega}$$

$$I_2 = 54.5\mu\text{A}$$



* O/P voltage : $V_o = A_v V_i = 70 \times 12mV = \underline{840mV}$

$$V_o = 840 \text{ mV}$$

$$* R_2 = \frac{V_o}{I_2} - R_3 = \left(\frac{840 \text{ mV}}{54.5 \mu\text{A}} - 220\Omega \right)$$

$$R_2 = 15.18 \text{ k}\Omega$$

Use standard value.

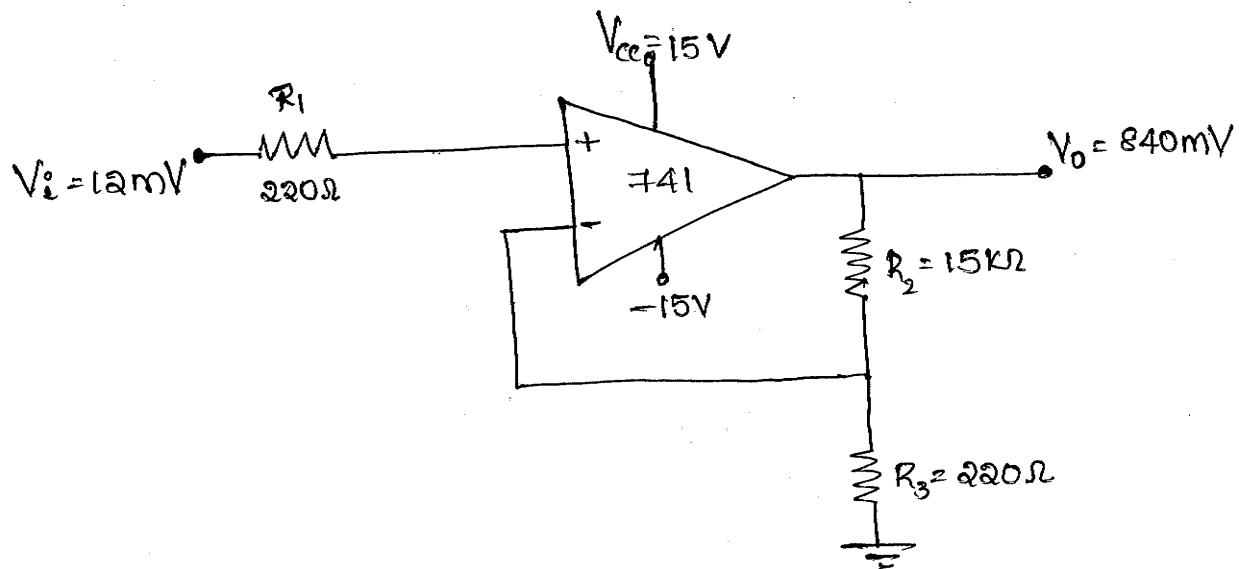
$$R_2 = 15 \text{ k}\Omega$$

$$* R_1 = (R_2 \parallel R_3) = \frac{220\Omega \times 15 \text{ k}\Omega}{220\Omega + 15 \text{ k}\Omega}$$

$$R_1 = 216.8 \Omega$$

Use standard value :

$$R_1 = 220\Omega$$



4). Design a Non-INV amplifier to amplify a 100mV signal to a level of 4 Volts. Using a 741 op-amp Assume $I_{B(\max)} = 500\text{nA}$ & $R_s = 1\text{k}\Omega$

Given :- $V_i = 100\text{ mV}$, $V_o = 4\text{V}$, $R_s = 1\text{k}\Omega$ & $I_{B(\max)} = 500\text{nA}$

Sol :- Let $I_2 = 100 \times I_{B(\max)} = 100 \times 500\text{nA}$

$$I_2 = 50\text{\mu A}$$

* $R_3 = \frac{V_o}{I_2} = \frac{100\text{mV}}{50\text{\mu A}} = 2\text{k}\Omega$

$$R_3 = 2\text{k}\Omega$$

Use standard value : $R_3 = 1.8\text{k}\Omega$

* Now I_2 becomes: $I_2 = \frac{V_i}{R_3} = \frac{100\text{mV}}{1.8\text{k}\Omega}$

$$I_2 = 55.6\text{\mu A}$$

* $R_2 = \frac{V_o}{I_2} - R_3 = \frac{4\text{V}}{55.6\text{\mu A}} - 1.8\text{k}\Omega$

$$R_2 = 70.14\text{k}\Omega$$

use standard value : $R_2 = 68\text{k}\Omega$

* $R_i = (R_2 \parallel R_3) = \frac{68\text{k}\Omega \times 1.8\text{k}\Omega}{68\text{k}\Omega + 1.8\text{k}\Omega}$

$$R_i = 1.75\text{k}\Omega$$

* R_i is Not very much greater than R_s

Thus

$$(R_i + R_s) = (R_2 \parallel R_3)$$

$$(R_i + R_s) = (68\text{k}\Omega \parallel 1.8\text{k}\Omega)$$

$$(R_i + R_s) = 1.75\text{k}\Omega$$

$$R_i = 1.75\text{k}\Omega - R_s.$$

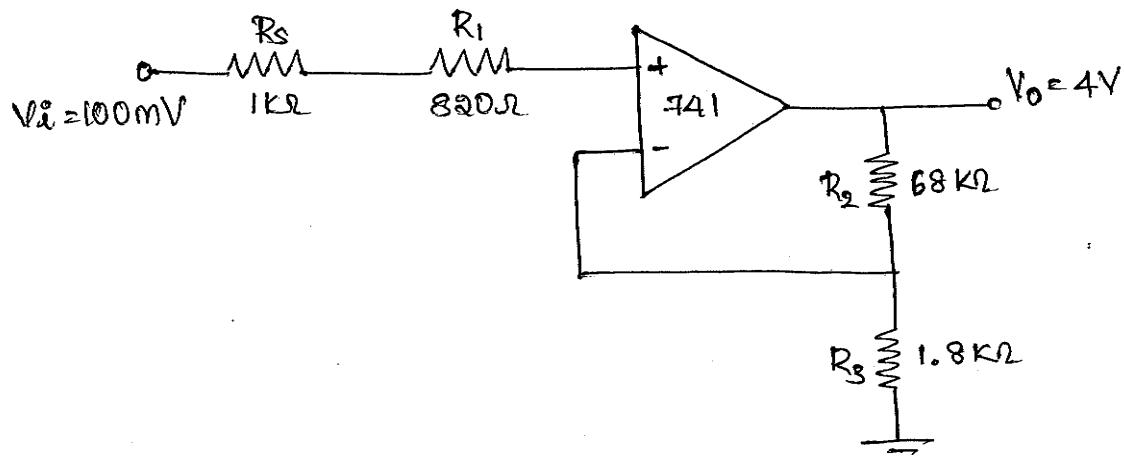


$$R_1 = 1.75 \text{ k}\Omega - 1 \text{ k}\Omega$$

$$R_1 = 750 \Omega$$

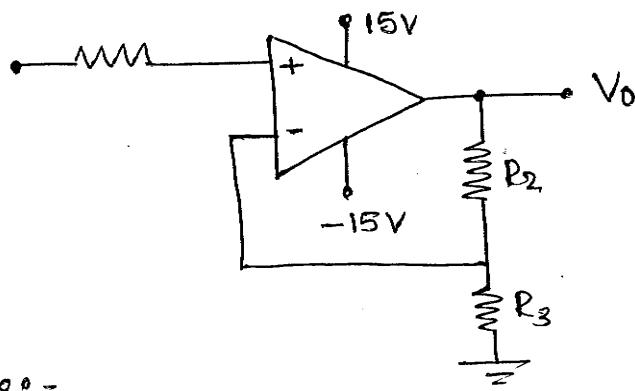
use standard value :

$$R_1 = 820 \Omega$$



FOR BIFET OP-AMP (LF - 353)

Directly-coupled Non-INV amplifier using LF353-BIFET



Design steps :-

1) First select higher resistance of the potential divider resistor :

$$R_3 = 1M\Omega$$

$$2) \text{ WKT } A_V = \frac{R_2 + R_3}{R_3} = \frac{R_2}{R_3} + \frac{R_3}{R_3} = \frac{R_2}{R_3} + 1$$

$$\frac{R_2}{R_3} = A_V - 1$$

$$R_3 = \frac{R_2}{A_V - 1}$$

$$* R_1 = (R_2 \parallel R_3)$$



1) Design the non-INV. amplifier using a LF-353 BIFET.
The gain is 66 and signal amplitude is to be 15mV.

Given :- $A_V = 66$, $V_i = 15 \text{ mV}$.

For LF-353 op-amp : $I_B(\text{max}) = 200 \mu\text{A}$

SOL :-

* Select $R_2 = 1 \text{ M}\Omega$

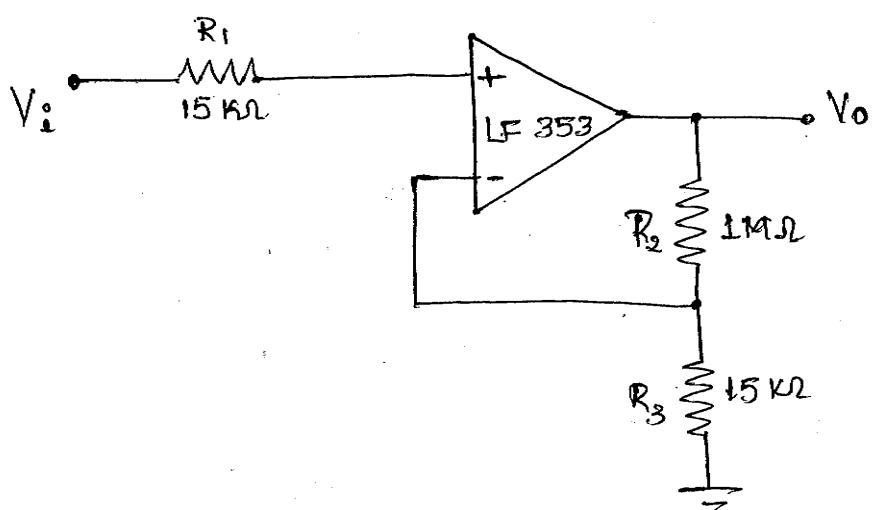
$$* R_3 = \frac{R_2}{A_V - 1} = \frac{1 \text{ M}\Omega}{66 - 1}$$

$$R_3 = 15.38 \text{ k}\Omega$$

use standard value : $R_3 = 15 \text{ k}\Omega$

$$* R_1 = (R_2 \parallel R_3) = (1 \text{ M}\Omega \parallel 15 \text{ k}\Omega)$$

$$R_1 = 15 \text{ k}\Omega$$



a) Design the Non-inverting amplifier using a LF-353 BIFET. The gain is 70. and signal amplitude is to be 12 mV.

Given:- $V_i = 12 \text{ mV}$, $A_v = 70$

for LF-353 Op-amp :

$$I_B(\text{max}) = 200 \text{ pA}$$

Sol:-

* select $R_2 = 1 \text{ M}\Omega$

$$* R_3 = \frac{R_2}{A_v - 1} = \frac{1 \text{ M}\Omega}{70 - 1} = 14.49 \text{ k}\Omega$$

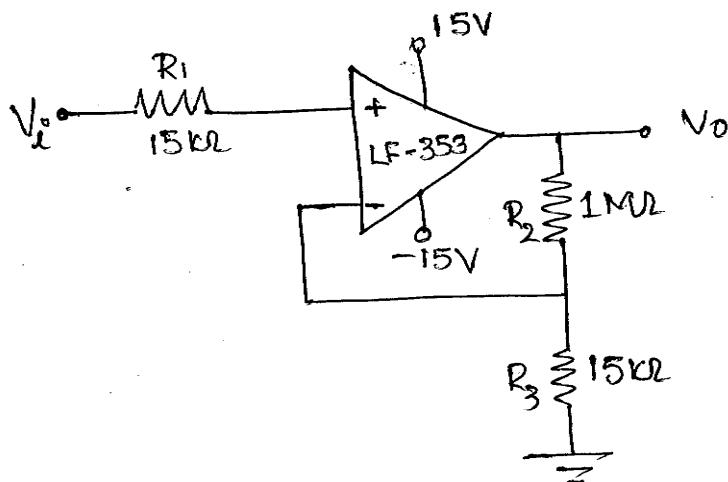
$$R_3 = 14.49 \text{ k}\Omega$$

Use standard value : $R_3 = 15 \text{ k}\Omega$

$$* R_1 = (R_2 \parallel R_3) = (1 \text{ M}\Omega \parallel 15 \text{ k}\Omega)$$

$$R_1 = 14.78 \text{ k}\Omega$$

Use standard value : $R_1 = 15 \text{ k}\Omega$



IIP & OIP Impedance of Non-INV amplifier :-

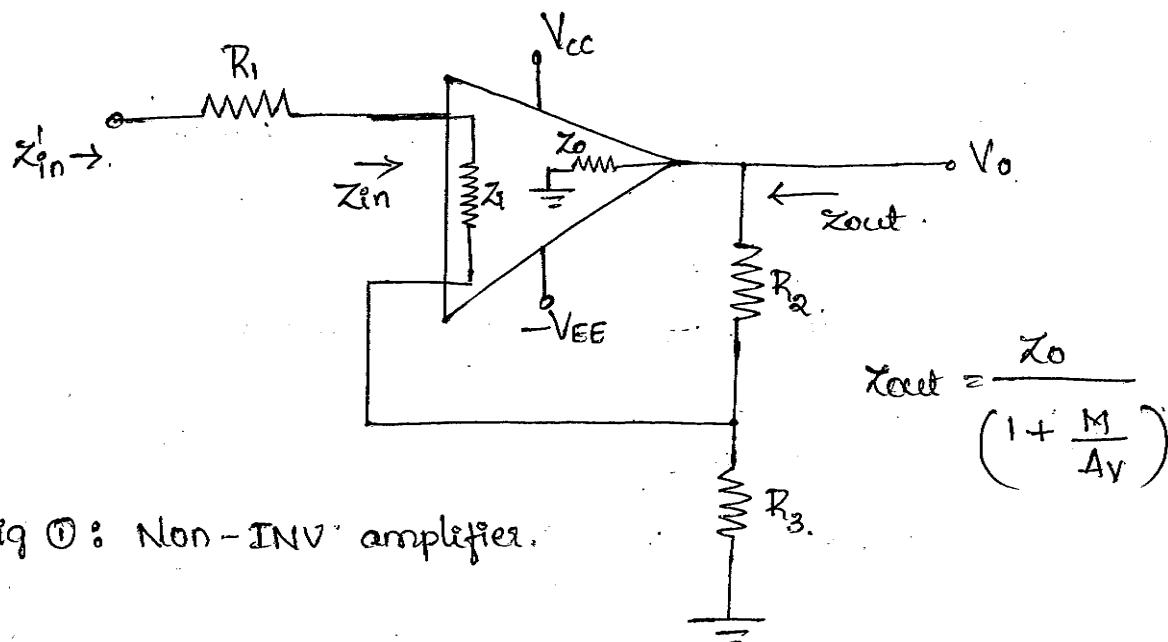


fig ① : Non-INV amplifier.

* for NON-INV amplifier feedback factor B is given by

$$B = \frac{R_3}{R_2 + R_3} = \frac{1}{A_V}$$

$$\left\{ \therefore A_V = \frac{R_2 + R_3}{R_3} \right.$$

$$\therefore B = \frac{1}{A_V}$$

* The IIP Impedance of an op-amp circuit given by

$$Z_{in} = (1 + MB) Z_i$$

\therefore IIP Impedance of Non-INV amplifier is.

$$Z_{in} = \left(1 + \frac{M}{A_V}\right) Z_i$$

* The IIP Impedance when seen from the signal source is

$$Z_{in} = R_1 + Z_{in}$$

* The OIP Impedance of an op-amp circuit is given by:

$$Z_{out} = \frac{Z_0}{1 + MB}$$



* Since $B = \frac{1}{A_V}$

\therefore o/p impedance of Non-INV amplifier is

$$Z_{out} = \frac{Z_0}{\left(1 + \frac{M}{A_V}\right)}$$

$$\left\{ \because B = \frac{1}{A_V} \right\}$$

NOTE :-

typical values for LF 353 BIFET op-amp :

- 1) $M = 100000$
- 2) $Z_i = 10^{12} \Omega$
- 3) $Z_0 = 75 \Omega$
- 4) $I_B(\text{max}) = 200 \mu\text{A}$.

- 1) calculate the IIP & o/p impedance of an Non-INV amplifier having gain 66. use the typical parameters of LF 353 op-amp. Assume $R_i = 15 \text{ k}\Omega$

Given :- $A_V = 66$, $R_i = 15 \text{ k}\Omega$.

Typical values for op-amp LF 353 :

$$M = 100000, Z_i = 10^{12} \Omega, Z_0 = 75 \Omega$$

Sol :- IIP impedance :-

$$* Z_{in} = \left(1 + \frac{M}{A_V}\right) Z_i = \left(1 + \frac{100000}{66}\right) \times 10^{12} \Omega$$

$$Z_{in} = 1.5 \times 10^{15} \Omega$$

$$* Z_{in} = R_i + Z_i = 15 \text{ k}\Omega + 1.5 \times 10^{15} \Omega$$

$$Z_{in} = 1.5 \times 10^{15} \Omega$$



O/P Impedance :-

$$\ast Z_{out} = \frac{Z_0}{\left(1 + \frac{M}{A_V}\right)} = \frac{75}{\left(1 + \frac{100000}{66}\right)}$$

$$Z_{out} = 49.46 \text{ m}\Omega$$

- Q) A Non-INV amplifier is to be designed using a LF 353A BIFET op-amp having parameters given by $I_B(\text{max}) = 200\text{pA}$, $M = 10^5$, $Z_i = 10^{12} \Omega$, $Z_o = 75 \Omega$. The source voltage used has $V_s = 50\text{mV}$ having a source resistance of $R_s = 2.2\text{k}\Omega$. The O/p voltage required is 3.3 volts. Find the values of all resistors R_1 , R_2 & R_3 . Also determine Z_{in} , Z_{out} and Z_{in}' of the designed circuit.

Given :- $I_B(\text{max}) = 200\text{pA}$, $M = 10^5$, $Z_i = 10^{12} \Omega$, $Z_o = 75 \Omega$,
 $R_s = 2.2\text{k}\Omega$, $V_s = V_i = 50\text{mV}$, $V_o = 3.3\text{V}$.

SOL :-

$$\ast \text{select } R_2 = 1\text{M}\Omega$$

$$\ast R_3 = \frac{R_2}{A_V - 1}$$

$$\ast A_V = \frac{V_o}{V_i} = \frac{3.3\text{V}}{50\text{mV}} = 66 \therefore A_V = 66$$

$$\ast R_3 = \frac{1\text{M}\Omega}{66 - 1} = 15.385\text{k}\Omega \therefore R_3 = 15.385\text{k}\Omega$$

Use standard value $R_3 = 15\text{k}\Omega$

$$\ast R_1 = (R_2 \parallel R_3) = (1\text{M}\Omega \parallel 15\text{k}\Omega) = 12.58\text{k}\Omega$$

Use standard value:

$$R_1 = 12\text{k}\Omega$$



* EIP Impedance :

$$Z_{in} = \left(1 + \frac{M}{A_V}\right) Z_i = \left(1 + \frac{10^5}{66}\right) 10^{12} \Omega$$

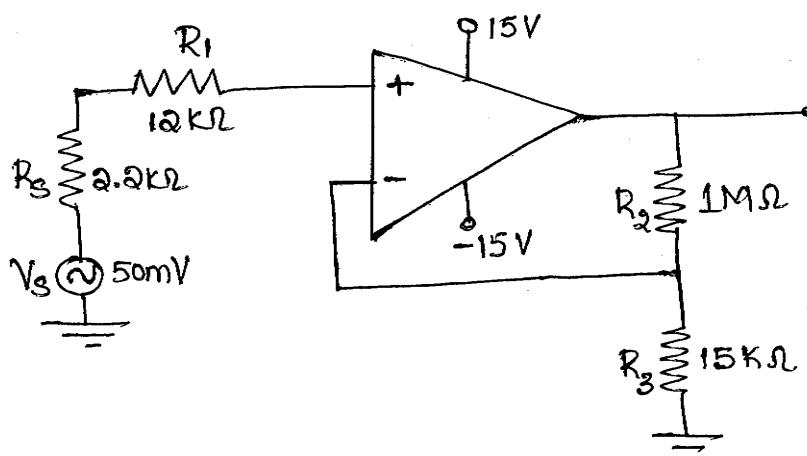
$$Z_{in} = 1.52 \times 10^{12} \Omega$$

* $Z'_{in} = R_1 + Z_{in} = 12k\Omega + 1.52 \times 10^{12} \Omega$

$$Z'_{in} = 1.52 \times 10^{12} \Omega$$

* OIP Impedance : $Z_{out} = \frac{Z_o}{\left(1 + \frac{M}{A_V}\right)} = \frac{75\Omega}{\left(1 + \frac{10^5}{66}\right)}$

$$Z_{out} = 0.05\Omega$$



* A Non-INV amplifier is to amplify a 100mV signal to a level of 3V. Using a 741 op-amp, design a suitable circuit.

[June - 10, 6m]

Given:- $V_i = 100\text{mV}$, $V_o = 3\text{V}$.

for 741 op-amp : $I_B(\text{max}) = 500\text{nA}$.



ARUNKUMAR G M.Tech, Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.

Sol :- * Let $I_2 = 100 \times I_{B(\max)} = 100 \times 500\text{mA} = 50\text{\mu A}$

$$I_2 = 50\text{\mu A}$$

* $R_3 = \frac{V_i}{I_2} = \frac{100\text{mV}}{50\text{\mu A}} = 2\text{k}\Omega$

Use standard resistor value, $R_3 = 1.8\text{k}\Omega$

← (2m)

* Now I_2 level changes i.e.

$$I_2 = \frac{V_i}{R_3} = \frac{100\text{mV}}{1.8\text{k}\Omega} \therefore I_2 = 55.6\text{\mu A}$$

* WKT $A_V = \frac{V_o}{V_i} = \frac{3\text{V}}{100\text{mV}} \approx 30$

* $R_2 + R_3 = \frac{V_o}{I_2}$

$$R_2 = \left(\frac{V_o}{I_2} - R_3 \right) = \left(\frac{3\text{V}}{55.6\text{\mu A}} - 1.8\text{k}\Omega \right)$$

$$R_2 = 52.15\text{k}\Omega$$

Use standard value $R_2 = 47\text{k}\Omega$

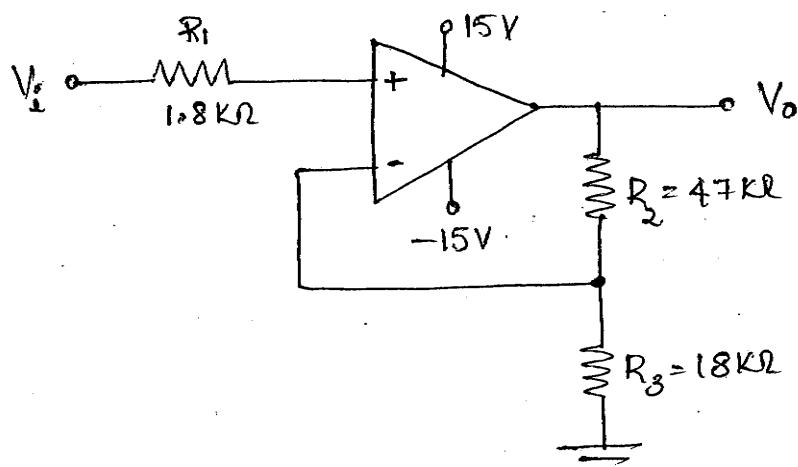
← (2m)

* $R_1 = (R_2 \parallel R_3) = (47\text{k}\Omega \parallel 1.8\text{k}\Omega) \approx 1.73\text{k}\Omega$

Use standard value resistor

$$R_1 = 1.8\text{k}\Omega$$

← (2m)



Direct coupled INV-amplifier :- (for 741 op-amp)

- 1) With a neat ckt diagram, explain direct-coupled INV amplifier.

June - 09, 4m

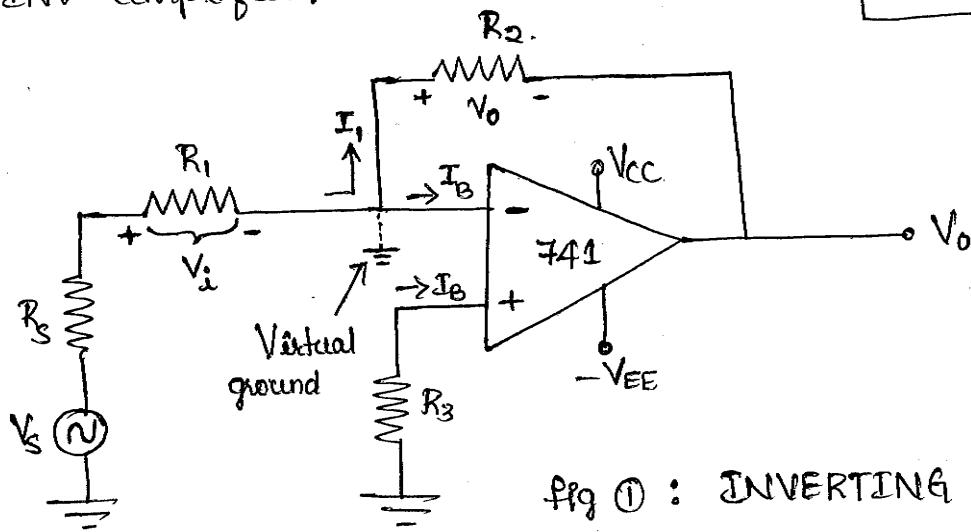


Fig ① : INVERTING amplifier.

- * The gain of the INV-amplifier is given by :

$$A_V = -\frac{R_2}{R_1}$$

Design steps:-

- 1) current I_1 is to be selected much higher than $I_B(\text{max})$ of the op-amp.

$$I_1 = 100 \times I_B(\text{max})$$

$$2) R_1 = \frac{V_i}{I_1}$$

$$3) R_2 = \frac{V_o}{I_1}$$

- 4) When looking out from each diff terminal of op-amp:

$$R_3 = R_1 \parallel R_2$$

And if R_1 is not very much larger than the source resistance, then

$$R_3 \approx (R_1 + R_s) \parallel R_2$$



Direct coupled INV - amplifier (for BIFET (LF 353) op-amp) :-

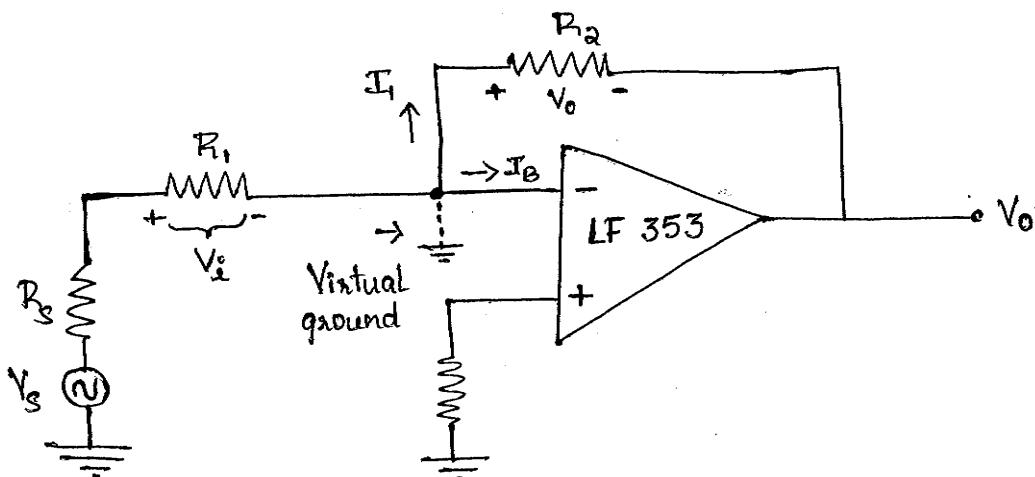


Fig ① : INV - amplifier

Design steps :-

1) For BIFET op-amps select largest value resistor

$$R_2 = 1 \text{ M}\Omega$$

$$2) R_1 = \frac{R_2}{A_V}$$

$$3) R_3 \approx (R_1 \parallel R_2)$$

$$4) A_V = \frac{R_2}{R_1}$$



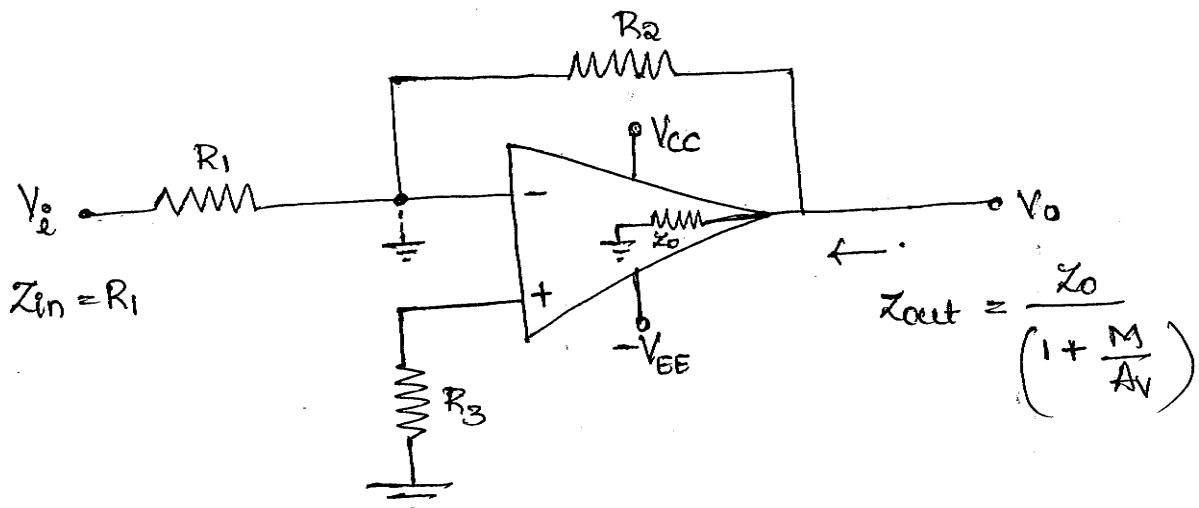
I/p & O/p Impedance of INV-amplifier :-

fig ① : Directly coupled INV-amplifier.

- * The resistor ' R_1 ' is seen with its other end at ground level.

$$\therefore Z_{in} = R_1$$

- * For INV-amplifier

$$B = \frac{R_1}{R_1 + R_2}$$

→ ① &

$$A_V = \frac{R_1 + R_2}{R_1}$$

- * The o/p Impedance of the INV amplifier is given by:-

$$Z_{out} = \frac{Z_0}{1 + MB} \rightarrow ②$$

substituting eq ① in eq ②, we get

$$Z_{out} = \frac{Z_0}{1 + M \left(\frac{R_1}{R_1 + R_2} \right)}$$

$$Z_{out} = \frac{Z_0}{1 + \frac{M}{A_V}}$$



Problems.

1) Design an inverting amplifier using a 741 op-amp. The voltage gain is to be 50 and the op voltage amplitude is to be 2.5V.

Given: $A_v = 50$, $V_o = 2.5V$

For 741 op-amp :

$$I_B(\text{max}) = 500\text{nA}$$

Sol:-

* Let $I_i = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$I_i = 50\mu\text{A}$$

* W.R.T $A_v = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_v} = \frac{2.5V}{50} = 50\text{mV}, \quad V_i = 50\text{mV}$$

* $R_1 = \frac{V_o}{I_i} = \frac{50\text{mV}}{50\mu\text{A}} = 1\text{k}\Omega \quad \therefore R_1 = 1\text{k}\Omega$

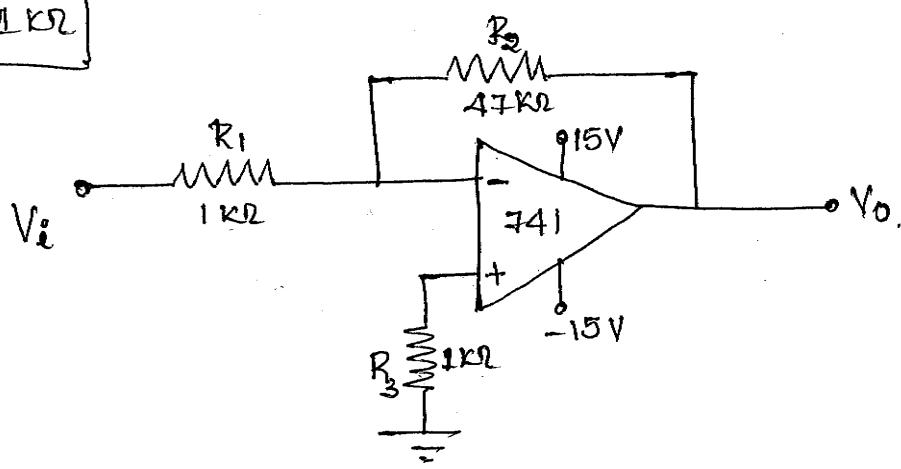
* $R_2 = \frac{V_o}{I_i} = \frac{2.5V}{50\mu\text{A}} = 50\text{k}\Omega$

Use standard value :

$$R_2 = 47\text{k}\Omega$$

* $R_3 = R_1 \parallel R_2 = 1\text{k}\Omega \parallel 47\text{k}\Omega$

$$R_3 \approx 1\text{k}\Omega$$



Q) Design an inverting amplifier using op-amp 741 with a voltage gain of 60 and the o/p voltage required is 3V.

Given :- $A_v = 60$, $V_o = 3V$

for 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

Sol :-

* Let $I_i = 100 \times I_B(\text{max}) = 100 \times 500\text{nA} = \underline{50\mu\text{A}}$

$$I_i = 50\mu\text{A}$$

* WKT $A_v = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_v} = \frac{3V}{60}$$

$$V_i = 50\text{mV}$$

* $R_1 = \frac{V_i}{I_i} = \frac{50\text{mV}}{50\mu\text{A}}$

$$\therefore R_1 = 1\text{k}\Omega$$

* $R_2 = \frac{V_o}{I_i} = \frac{3V}{50\mu\text{A}}$

$$R_2 = 60\text{k}\Omega$$

Use standard value

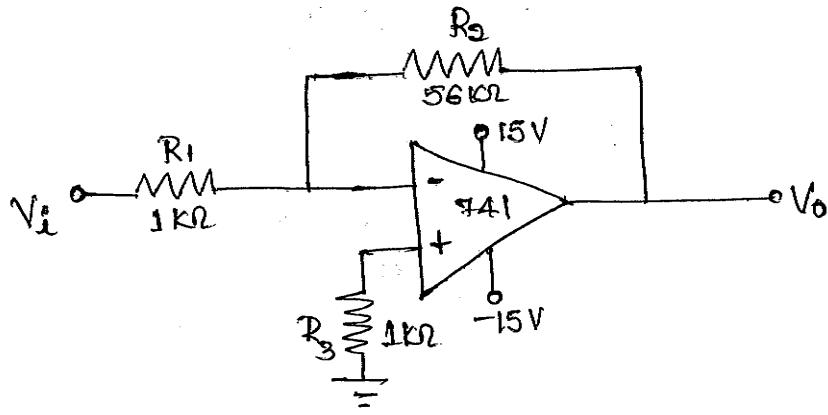
$$R_2 = 56\text{k}\Omega$$

* $R_3 = (R_1 \parallel R_2) = \frac{1\text{k}\Omega \times 56\text{k}\Omega}{1\text{k}\Omega + 56\text{k}\Omega}$

$$R_3 = 983.6\Omega$$

Use standard value

$$R_3 = 1\text{k}\Omega$$



LF 353 BIFET.

1) Design the INVERTING amplifier using a LF 353 BIFET op-amp. The voltage gain is to be 50 and the op voltage amplitude is to be 2.5V.

Given :- $A_V = 50$, $V_o = 2.5V$

Sol :-

* For BIPOLAR op-amps select largest value resistor

$$R_2 = 1M\Omega$$

$$* R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{50}$$

$$R_1 = 20k\Omega$$

Use standard value

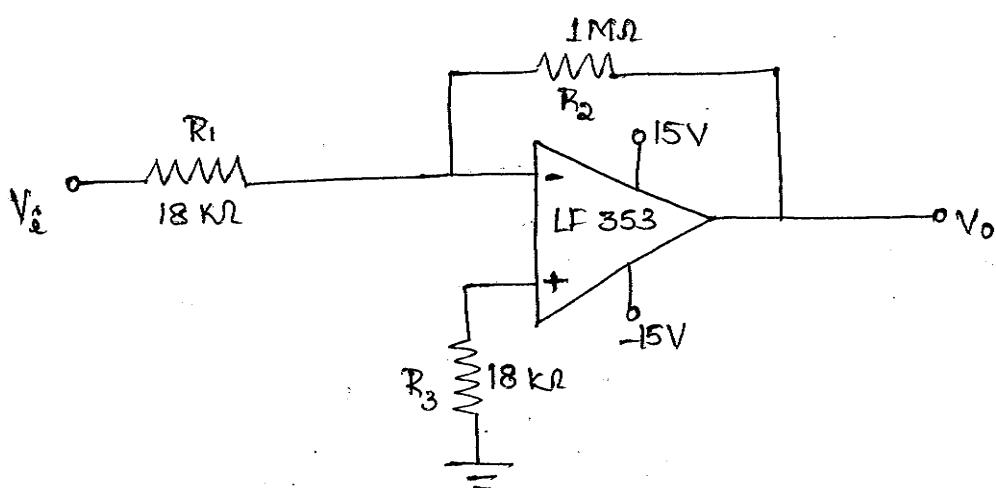
$$R_1 = 18k\Omega$$

$$* R_3 = (R_1 \parallel R_2) = \frac{18k\Omega \times 1M\Omega}{18k\Omega + 1M\Omega}$$

$$R_3 = 17.68k\Omega$$

Use standard value

$$R_3 = 18k\Omega$$



Q) Design the inverting amplifier using a LF 353 BIFET op-amp. The voltage gain is to be 40 and the output voltage amplitude is to be 3V.

Given:- $A_V = 40$, $V_o = 3V$

Sol:-

* select largest value resistor

$$R_2 = 1M\Omega$$

$$* R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{40}$$

$$R_1 = 25k\Omega$$

use standard value

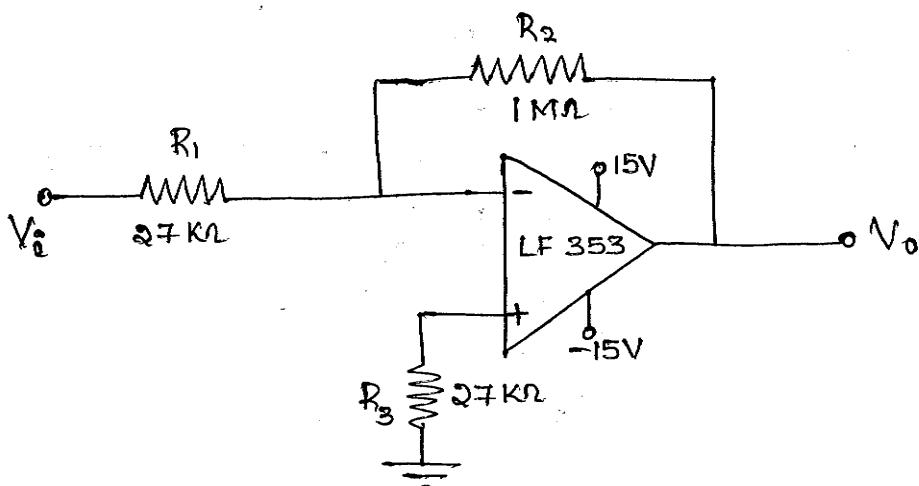
$$R_1 = 27k\Omega$$

$$* R_3 = (R_1 \parallel R_2) = \frac{27k\Omega \times 1M\Omega}{27k\Omega + 1M\Omega}$$

$$R_3 = 26.29k\Omega$$

use standard value

$$R_3 = 27k\Omega$$



3) An inverting amplifier using BIFET LF 353A op-amp is to be employed to amplify a 50mV signal to a level of 3.5 volts. Design the required circuit and determine its IIP and OIP Impedances. Assume $R_g = 1.2\text{ k}\Omega$, $M = 10^5$ and $Z_o = 75\Omega$ for BIFET op-amp.

Given: $V_i = 50\text{mV}$, $V_o = 3.5\text{V}$, $R_g = 1.2\text{ k}\Omega$, $M = 10^5$, $Z_o = 75\Omega$.

Sol:-

* Select largest value resistor: $R_2 = 1\text{ M}\Omega$

$$\text{* WKT } A_v = \frac{V_o}{V_i} = \frac{3.5\text{V}}{50\text{mV}} \quad A_v = 70$$

$$\text{* } R_1 = \frac{R_2}{A_v} = \frac{1\text{ M}\Omega}{70} \quad R_1 = 14.28\text{ k}\Omega$$

Use standard value $R_1 = 15\text{ k}\Omega$.

$$\text{* } R_3 = (R_1 \parallel R_2) = \frac{15\text{ k}\Omega \times 1\text{ M}\Omega}{15\text{ k}\Omega + 1\text{ M}\Omega} \quad R_3 = 14.77\text{ k}\Omega$$

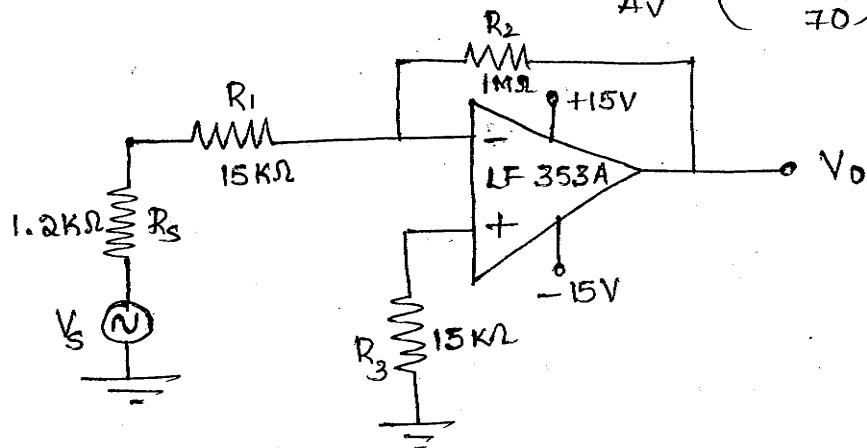
Use standard value $R_3 = 15\text{ k}\Omega$

* The IIP Impedance, $Z_{in} = R_1$

$$Z_{in} = 15\text{ k}\Omega$$

* O/P Impedance:

$$Z_{out} = \frac{Z_o}{1 + \frac{M}{A_v}} = \frac{75\Omega}{1 + \frac{10^5}{70}} = 0.052\Omega$$



SUMMING AMPLIFIERS

INVERTING SUMMING CIRCUIT :-

- * sketch the circuit of a two-I/p inverting summing amplifier. Explain the operation of the circuit & derive the equation for the o/p voltage.

Jcnee - 10, 8M

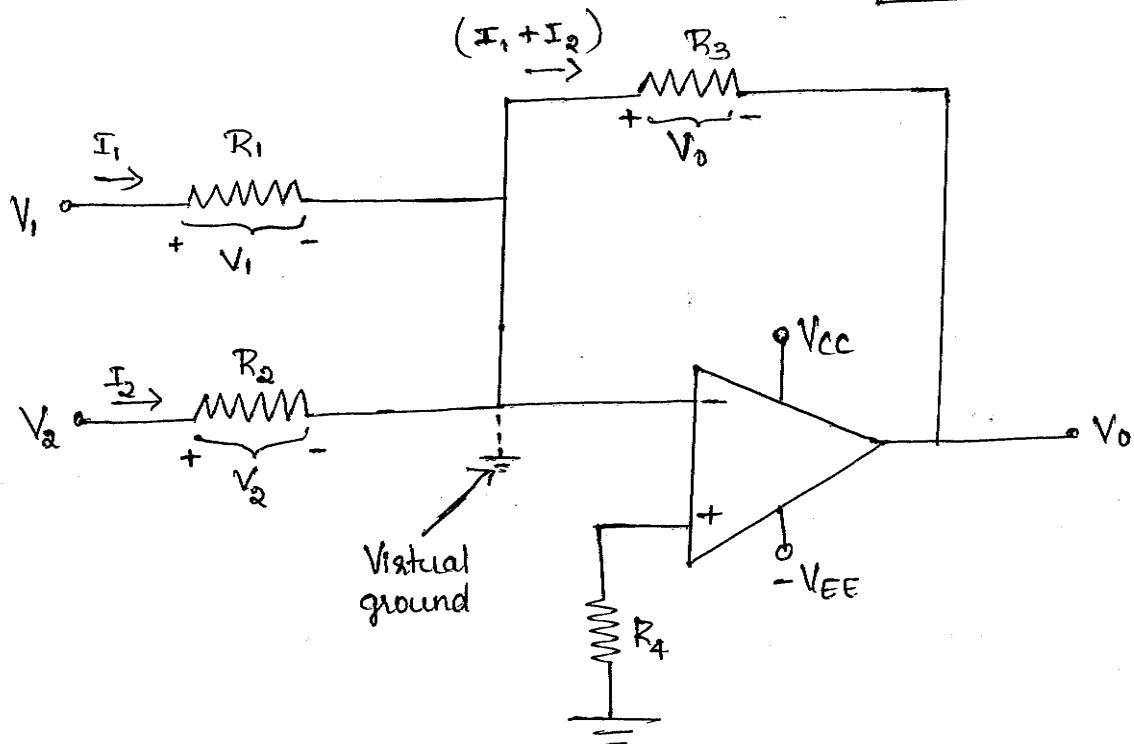


fig ① : op-amp INV summing amplifier with 2 I/p's.

fig ① shows a circuit that amplifies the sum of two or more I/p's. since the inverting terminal behaves as a virtual ground, the currents through the resistors R_1 & R_2 are respectively given by :

$$I_1 = \frac{V_1}{R_1}$$

and.

$$I_2 = \frac{V_2}{R_2}$$

- * These two currents flow through R_3 .

Applying KVL from R_3 to o/p.

$$-(I_1 + I_2) R_3 - V_o = 0.$$

$$V_o = -(I_1 + I_2) R_3 \rightarrow ①$$



Substituting I_1 & I_2 in eq ①, we get

$$V_o = - \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right] R_3$$

$$V_o = - R_3 \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} \right]$$

With $R_1 = R_2$

$$V_o = - R_3 \left[\frac{V_1}{R_1} + \frac{V_2}{R_1} \right]$$

$V_o = - \frac{R_3}{R_1} [V_1 + V_2]$

→ ②

But

$A_V = - \frac{R_3}{R_1}$

$\therefore V_o = A_V [V_1 + V_2]$

→ ③

* If $R_1 = R_2 = R_3$, then $A_V = -1$, then eq ③ becomes

$$V_o = -1 [V_1 + V_2]$$

$V_o = - [V_1 + V_2]$

$R_4 = R_1 \parallel R_2 \parallel R_3$

* Suppose there are three I/P's to a summing circuit as shown in fig ②

* The o/p voltage is given by:

$$V_o = - \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right] R_4$$



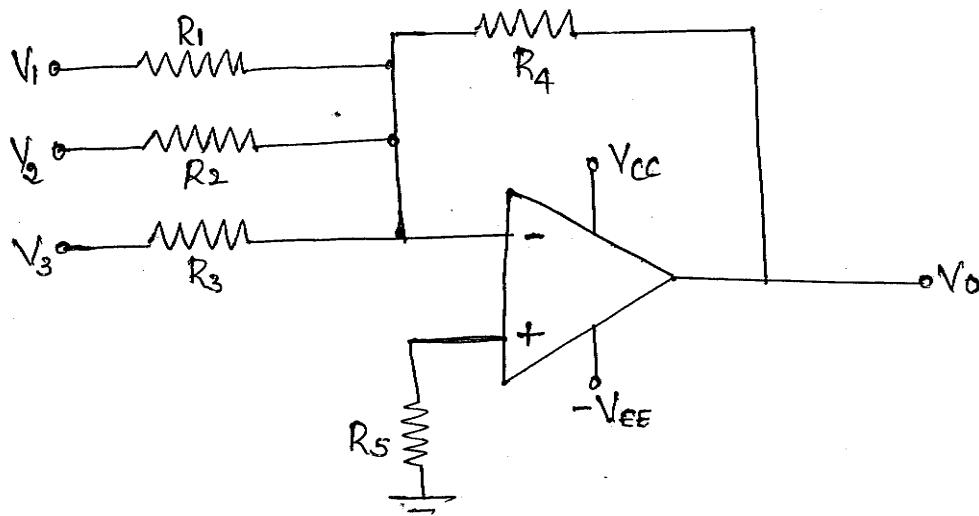


fig ④: INV summing amplifier with 3 I/P's.

Suppose that $R_1 = R_2 = R_3$ then,

$$V_0 = -R_4 \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_1} \right]$$

$$V_0 = -\frac{R_4}{R_1} [V_1 + V_2 + V_3]$$

If $R_4 = \frac{R_1}{3}$, then

$$V_0 = -\frac{R_1}{3R_1} [V_1 + V_2 + V_3]$$

$$V_0 = -\frac{1}{3} [V_1 + V_2 + V_3] \rightarrow ④$$

Equation ④ shows that the o/p voltage is the average value of the three I/P's. Thus, the summing amplifier can be designed to be an averaging circuit.



INV - summing amplifier Design procedure :-

1) $I_L(\text{min}) = 100 \times I_B(\text{max})$

2) $R_1 = \frac{V_s(\text{min})}{I_L(\text{min})}$

3) $R_1 = R_2$

4) for $A_V = -1$, $R_1 = R_3$

5) $R_4 = R_1 \parallel R_2 \parallel R_3$

Problems

1) Design a INV summing amplifier to give the direct sum of two IIP's which each range from 0.1V to 1V. Use a 741 op-amp.

(OR)

1) Two signals which each range from 0.1V to 1V are to be summed. Using a 741 op-amp design a suitable inverting summing circuit

June - 08, 6M

Given : $V_s(\text{min}) = 0.1\text{V}$, $V_s(\text{max}) = 1\text{V}$

For 741 op-amp : $I_B(\text{max}) = 500\text{nA}$.

Sol : * $I_L(\text{min}) = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$I_L(\text{min}) = 50\mu\text{A}$

$\leftarrow [1\text{M}]$



$$* R_1 = \frac{V_s(\text{min})}{I_1(\text{min})} = \frac{0.1V}{50\mu A}$$

$R_1 = 2k\Omega$ Use standard value $R_1 = 1.8k\Omega$ ← (2m)

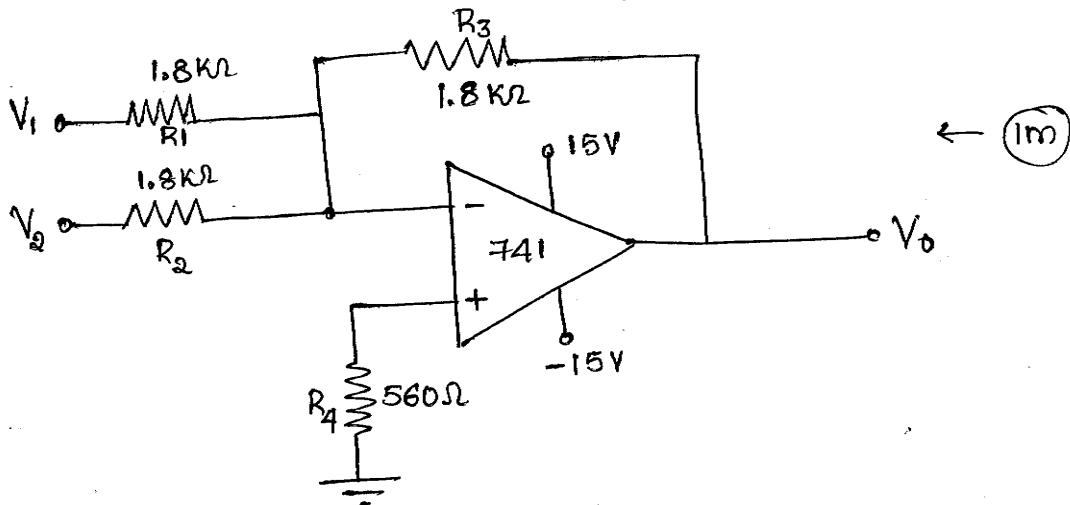
$$* R_1 = R_2 = 1.8k\Omega$$

$$* \text{for } A_V = 1, R_1 = R_3 = 1.8k\Omega$$

$$* R_4 = R_1 \parallel R_2 \parallel R_3 = 1.8k\Omega \parallel 1.8k\Omega \parallel 1.8k\Omega$$

$$R_4 = 600\Omega$$

Use standard value $R_4 \approx 560\Omega$ ← (1m)



2) Three signals each ranging from 0.2V to 0.5V are to be summed. Using a 741 op-amp, design a suitable inverting summer circuit. choose $I_{B(\text{max})} = 500\text{nA}$ for 741 op-amp.

Given :- $V_{s(\text{min})} = 0.2V$, $V_{s(\text{max})} = 0.5V$, $I_{B(\text{max})} = 500\text{nA}$

$$\text{Sol: } * I_1(\text{min}) = 100 \times I_B(\text{max}) \\ = 100 \times 500\text{nA}$$

$$\therefore I_1(\text{min}) = 50 \mu A$$



$$* R_1 = \frac{V_s(\text{min})}{I_1(\text{min})} = \frac{0.5V}{50\text{mA}} \quad R_1 = 4K\Omega$$

Use standard value $R_1 = 3.9K\Omega$

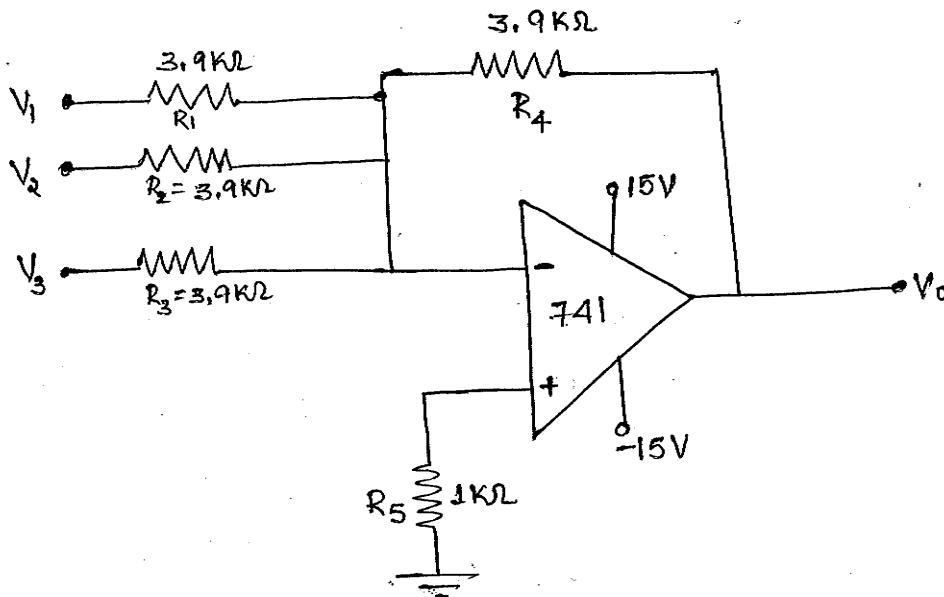
$$* R_1 = R_2 = R_3 = 3.9K\Omega$$

$$* \text{For } A_V = 1, R_4 = R_1 = 3.9K\Omega$$

$$* R_5 = R_1 \parallel R_2 \parallel R_3 \parallel R_4 = 3.9K\Omega \parallel 3.9K\Omega \parallel 3.9K\Omega \parallel 3.9K\Omega$$

$$R_5 = 975\Omega$$

Use standard value $R_5 = 1K\Omega$



3) Design a INV summing amplifier to give the sum of the two I/p's which each range from 0.5V to 1V. Use as 741 op-amp and gain of the circuit as 2.

Given :- $V_s(\text{min}) = 0.5V$, $V_s(\text{max}) = 1V$, $A_V = 2$

For op-amp 741 : $I_B(\text{max}) = 500\text{nA}$



Sol: $I_{I(\min)} = 100 \times I_{B(\max)} = 100 \times 500 \mu A$

$I_{I(\min)} = 50 \mu A$

* $R_1 = \frac{V_s(\min)}{I_{I(\min)}} = \frac{0.5 V}{50 \mu A} \quad R_1 = 10 k\Omega$

* $R_1 = R_2 = 10 k\Omega$

* Given $A_V = 2$.

wkt $|A_V| = \left| \frac{R_3}{R_1} \right|$

$$2 = \frac{R_3}{R_1}$$

$$R_3 = 2R_1 = 2 \times 10 k\Omega$$

$R_3 = 20 k\Omega$

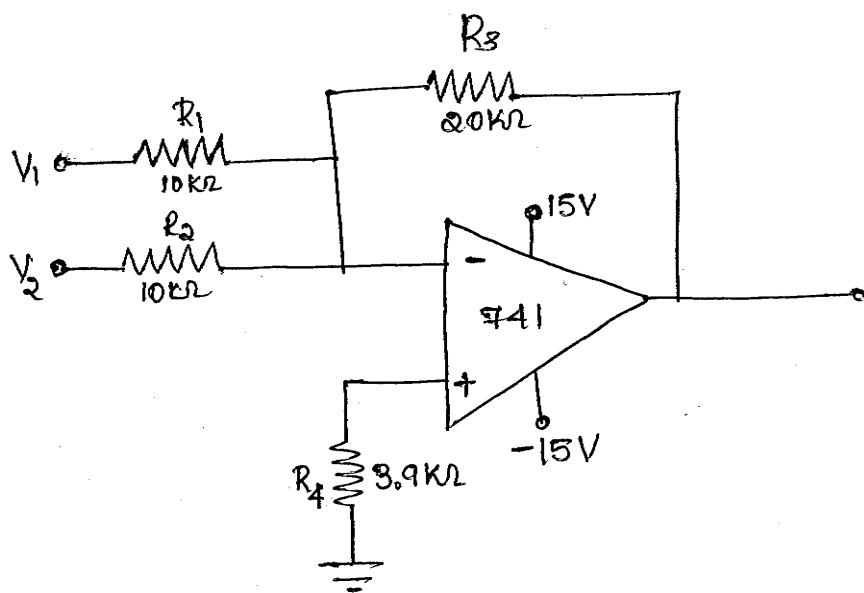
Use standard value: $R_3 = 22 k\Omega$

* $R_4 = R_1 \parallel R_2 \parallel R_3 = 10 k\Omega \parallel 10 k\Omega \parallel 22 k\Omega$

$R_4 = 4.07 k\Omega$

Use standard value

$R_4 = 3.9 k\Omega$



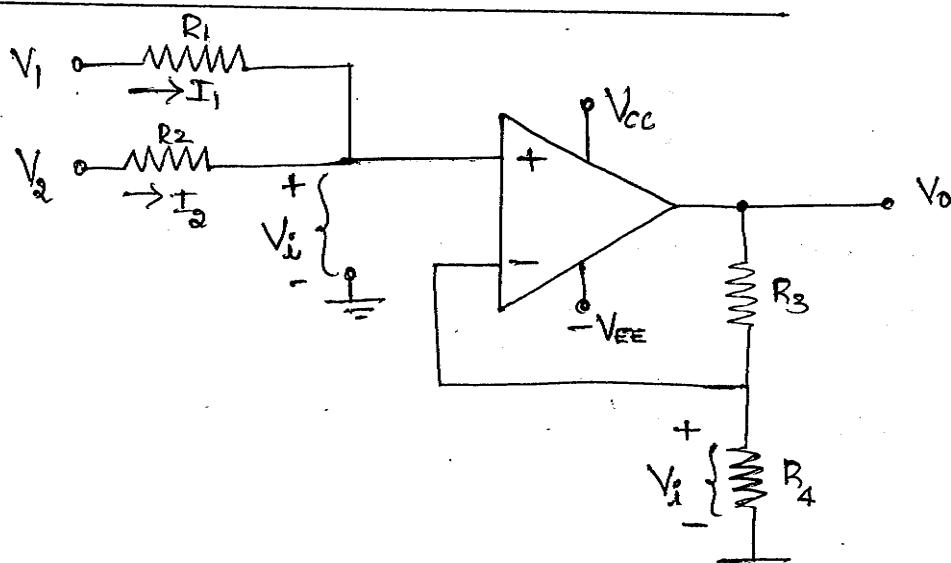
NON - INVERTING SUMMING CKT :-

fig ① : Non - INV summing amplifier with two I/p's.

fig ① shows a Non - INV summing amplifier. The o/p will be a direct sum of +ve I/p signals.

The equation for the o/p voltage can be derived by using Superposition theorem.

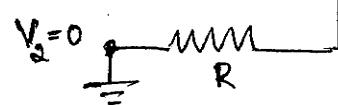
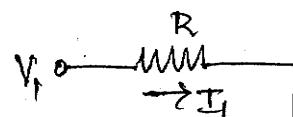
* Let $V_2 = 0$ & $R_1 = R_2 = R$

$$V_{i1} = I_1 R$$

$$= \frac{V_1 R}{R + R}$$

$$= \frac{V_1 R}{2R}$$

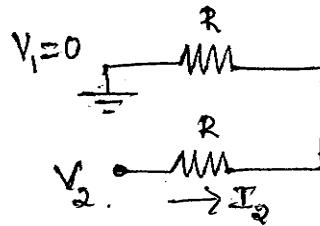
$$\boxed{V_{i1} = \frac{V_1}{2}} \rightarrow ①$$



$$\therefore I_1 = \frac{V_1}{R+R}$$

* Let $V_1 = 0$ & $R_1 = R_2 = R$

$$V_{i2} = I_2 R$$



$$\therefore I_2 = \frac{V_2}{R+R}$$



$$V_{i2} = \frac{V_2 R}{R+R} = \frac{V_2 R}{2R}$$

$$\boxed{V_{i2} = \frac{V_2}{2}} \rightarrow ②$$

* The I/p voltage V_i is given by :

$$\boxed{V_i = V_{i1} + V_{i2}} \rightarrow ③$$

Substituting eq ① & ② in eq ③, we get

$$V_i = \frac{V_1}{2} + \frac{V_2}{2}$$

$$\therefore \boxed{V_i = \frac{V_1 + V_2}{2}}$$

* For Non-INV amplifier, the voltage gain is given by

$$\boxed{A_V = \frac{R_3 + R_4}{R_4}} \rightarrow ④$$

* WKT $A_V = \frac{V_o}{V_i}$

$$\boxed{V_o = A_V V_i} \rightarrow ⑤$$

Substituting eq ③ & ④, we get

$$V_o = \frac{R_3 + R_4}{R_4} \left(\frac{V_1 + V_2}{2} \right)$$

If $R_3 = R_4 = R$.

$$V_o = \frac{R+R}{R} \left(\frac{V_1 + V_2}{2} \right)$$

$$V_o = \frac{2R}{R} \left(\frac{V_1 + V_2}{2} \right)$$

$$(\because V_o = \frac{2R}{2R} (V_1 + V_2))$$

$$\boxed{V_o = (V_1 + V_2)}$$



- * Fig ② shows the Non-INV Summing amplifier with three I/p's.

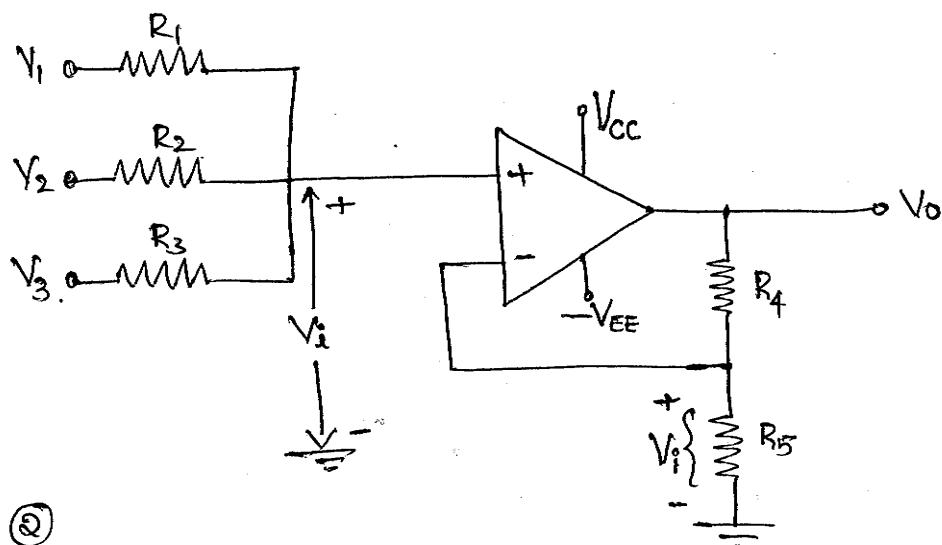


fig ②

- * For the three - I/p Non-INV summing ckt in fig ②, the voltage at the op-amp Non-INV I/p when

$$R_1 = R_2 = R_3 = R$$

$$V_i = \frac{V_1 + V_2 + V_3}{3}$$

$$\text{WKT } V_o = A_v V_i$$

$$V_o = A_v \left(\frac{V_1 + V_2 + V_3}{3} \right)$$

With

$$A_v = 3$$

$$V_o = 3 \left(\frac{V_1 + V_2 + V_3}{3} \right)$$

$$V_o = (V_1 + V_2 + V_3)$$



Difference Amplifier :-

A difference amplifier or differential amplifier, amplifies the difference between the two I/P signals. An IC op-amp is a difference amplifier having INV & Non-INV I/P's. Since the open-loop gain of the op-amp is very large, it has to be used with negative feedback.

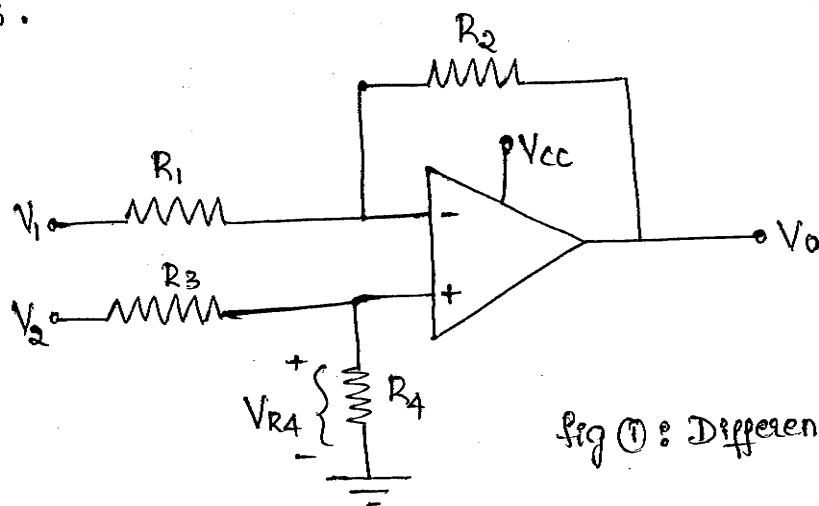


fig ① : Difference amplifier ckt.

Operation :-

Let us use superposition principle to find out the expression for the o/p :

case i :

V_1 acting , $V_2=0V$ (grounded) • let the o/p is V_{01} .

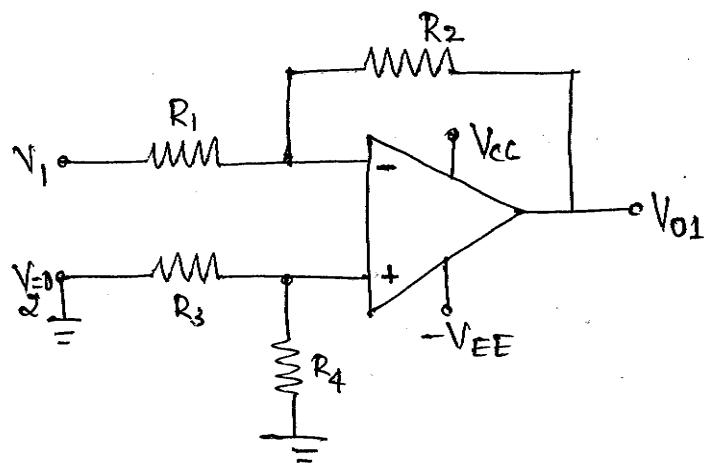


fig ② : V_1 acting & $V_2=0V$

* Now fig ② acts as an INV amplifier

$$\therefore V_{01} = -\frac{R_2}{R_1} V_1 \rightarrow ①$$



case ii: V_2 acting, $V_1 = 0V$ (grounded). Let the o/p is V_{02} .

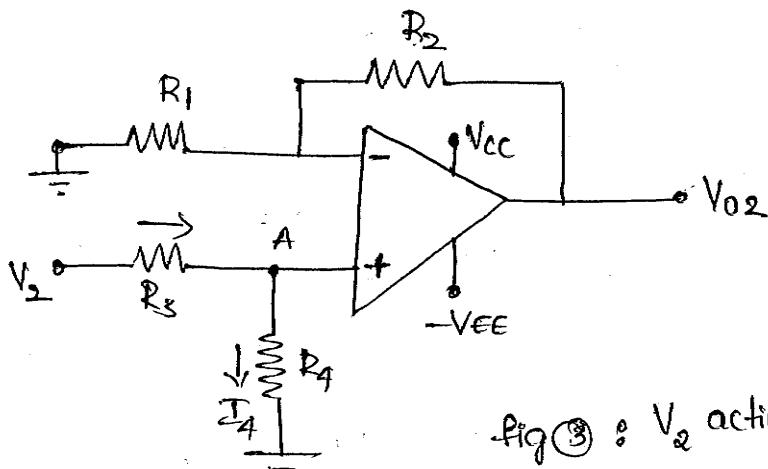


fig ③ : V_2 acting & $V_1 = 0$

- * Now fig ③ : acts as Non-INV amplifier & hence :
- * the o/p voltage is given by :

$$V_{02} = A_V V_A$$

{ \because WKT }

$$A_V = \frac{V_o}{V_A}$$

WKT the gain of the Non-INV amplifier is given by

$$-A_V = \left(1 + \frac{R_2}{R_1} \right)$$

$$V_{02} = \left(1 + \frac{R_2}{R_1} \right) V_A \rightarrow ②$$

from fig ③ the voltage at Node A is given by :

$$V_A = I R_4$$

$$\text{where, } I = \frac{V_2}{R_3 + R_4}$$

$$\therefore V_A = \frac{V_2 R_4}{R_3 + R_4} \rightarrow ③$$

substituting eq ③ in eq ②, we get

$$V_{02} = \left(1 + \frac{R_2}{R_1} \right) \left(\frac{V_2 R_4}{R_3 + R_4} \right) \rightarrow ④$$



With both signals present,

$$\boxed{V_o = V_{o1} + V_{o2}} \rightarrow ⑤$$

Substituting eq ① & ④ in eq ⑤, we get

$$V_o = -\frac{R_2}{R_1} V_1 + \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) V_2$$

Select the resistance as $R_3 = R_1$ and $R_4 = R_2$

$$V_o = -\frac{R_2}{R_1} V_1 + \left(\frac{R_1 + R_2}{R_1}\right) \left(\frac{R_2}{R_1 + R_2}\right) V_2$$

$$V_o = -\frac{R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2 \quad (\because V_o = A_v V_i)$$

$$\text{where } A_v = \frac{R_2}{R_1}$$

$$V_i = V_2 - V_1$$

When $R_1 = R_2$

$$\boxed{V_o = (V_2 - V_1)}$$

Now the o/p is the direct difference of the two I/p voltage.

Continued →

P.T.O



I/p Resistance :-i) Differential I/p resistance :-

The differential I/p resistance is the resistance offered to a signal source which is connected directly across the I/p terminals.

i.e. $R_i(\text{diff}) = R_1 + R_3 + R_4$

ii) Common mode I/p resistance :-

The common mode I/p resistance is the resistance offered to a signal source which is connected b/w both I/p terminals and ground.

i.e. $R_i(\text{cm}) = R_1 \parallel (R_3 + R_4)$

Difference Amplifier \rightarrow FORMULAE

1) For LF 353 op-amp : Select $R_2 = 1\text{M}\Omega$

2) $A_V = \frac{R_2}{R_1}$

3) $R_3 = R_1$

4) $R_4 = R_2$

5) $R_i(\text{diff}) = R_1 + (R_3 + R_4)$

6) $R_i(\text{cm}) = R_1 \parallel (R_3 + R_4)$



PROBLEMS

1) The difference of two IIP signals to be amplified by a factor of 37. Each IIP has an amplitude of approximately 50mV. Using an LF 353 OP-amp, design a suitable circuit and calculate the differential and common mode IIP resistance.

Given: $A_V = 37$, $V_i = 50\text{mV}$

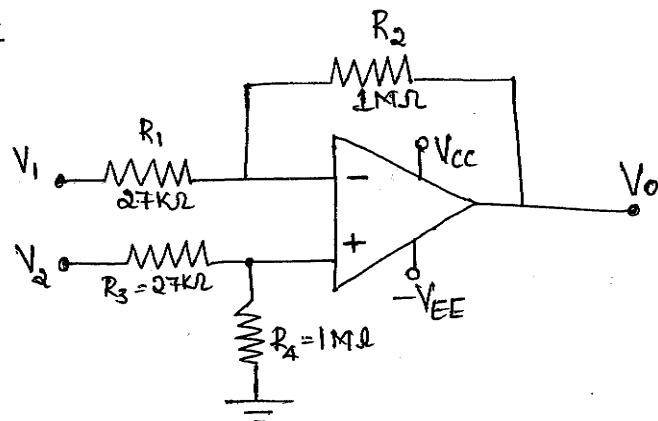
Sol:- For LF 353 op-amp :

* Select largest value resistor $R_2 = 1\text{M}\Omega$

* WKT $A_V = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{A_V} = \frac{1\text{M}\Omega}{37}$$

$R_1 = 27\text{k}\Omega$



* $R_3 = R_1 = 27\text{k}\Omega$

* $R_4 = R_2 = 1\text{M}\Omega$

* $R_{i(\text{diff})} = R_1 + R_3 + R_4$
 $= 27\text{k}\Omega + 27\text{k}\Omega + 1\text{M}\Omega$

$R_{i(\text{diff})} = 1.054\text{M}\Omega$

Use standard value resistor : $R_{i(\text{diff})} = 1\text{k}\Omega$

* $R_{i(\text{cm})} = R_1 \parallel (R_3 + R_4) = 27\text{k}\Omega \parallel (27\text{k}\Omega + 1\text{M}\Omega)$

$R_{i(\text{cm})} = 26.3\text{k}\Omega$



2) The difference of two IIP signals is to be amplified by a factor 40. Each IIP has an amplitude of approximately 40mV. Using a LF353 - OP-amp, design a circuit and calculate the differential and common mode IIP resistance.

Given :- $A_v = 40$, $V_i = 40 \text{ mV}$

Sol :- For LF353 op-amp:

* Select largest value resistor, $R_2 = 1 \text{ M}\Omega$

$$\text{* WKT } A_v = \frac{R_2}{R_1}$$

$$R_1 = \frac{R_2}{A_v} = \frac{1 \text{ M}\Omega}{40}$$

$$R_1 = 25 \text{ k}\Omega$$

* $R_3 = R_1 = 25 \text{ k}\Omega$ Use standard value resistor

$$R_3 = R_1 = 27 \text{ k}\Omega$$

* $R_4 = R_2 = 1 \text{ M}\Omega$

* $R_{i(\text{dif})} = R_1 + R_3 + R_4 = 27 \text{ k}\Omega + 27 \text{ k}\Omega + 1 \text{ M}\Omega$

$$R_{i(\text{dif})} = 1.054 \text{ M}\Omega$$

Use standard value resistor: $R_{i(\text{dif})} = 1 \text{ M}\Omega$

$$\begin{aligned} * R_{i(\text{cm})} &= R_1 \parallel (R_3 + R_4) \\ &= 27 \text{ k}\Omega \parallel (27 \text{ k}\Omega + 1 \text{ M}\Omega) \end{aligned}$$

$$R_{i(\text{cm})} = 26.308 \text{ k}\Omega$$

Use standard value resistor:

$$R_{i(\text{cm})} = 27 \text{ k}\Omega$$



3) Design a difference amplifier with gain 50. Also calculate the values of differential and common mode input resistance.

Given :- $A_V = 50$

Sol :- * select largest value resistor

$$R_2 = 1M\Omega$$

$$* A_V = \frac{R_2}{R_1}$$

$$R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{50}$$

$$R_1 = 20k\Omega$$

$$* R_3 = R_1 = 20k\Omega$$

$$* R_4 = R_2 = 1M\Omega$$

$$* R_i(\text{dif}) = R_1 + R_3 + R_4 = 1.04M\Omega$$

$$* R_i(\text{cm}) = R_1 \parallel (R_3 + R_4)$$

$$= 20k\Omega \parallel (20k\Omega + 1M\Omega)$$

$$R_i(\text{cm}) = 19.615 k\Omega$$



Common Mode Voltages :-

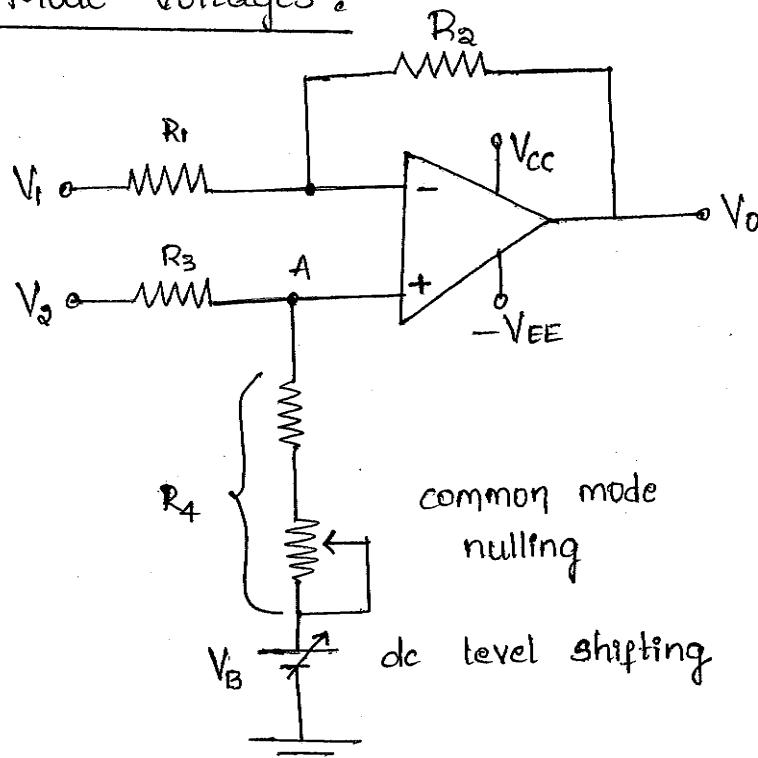


Fig ① : Difference amplifier to nullify common-mode op & op level shifting.

- * Let ' V_c ' is the common voltage gets applied to both the I/p terminals. Hence input 1 becomes $(V_1 + V_c)$ while I/p 2 becomes $(V_2 + V_c)$.
- * The amplified op is the difference b/w the two I/p's i.e. $V_o = (V_2 + V_c) - (V_1 + V_c)$

$$= V_2 + V_c - V_1 - V_c$$

$$\therefore \boxed{V_o = V_2 - V_1}$$
- * The ' V_c ' gets cancelled and has no effect on the op if $\left(\frac{R_4}{R_3} = \frac{R_2}{R_1}\right)$ are equal.



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- * If these ratios are unequal then ' V_c ' at one IIP gets amplified more than that at the other IIP. Hence V_c will not get cancelled & will be present at o/p.
 - * Practically it is impossible to match these ratios perfectly and some common mode voltage is found to be present.
 - * To minimize common mode o/p, the resistor R_4 is selected as the combination of fixed resistor and a smaller variable resistor.
 - * By adjusting the (potentiometer) variable part of ' R_4 ', the ratio R_4/R_3 is made almost equal to R_2/R_1 in order to null the common mode o/p voltage to zero.

O/P Level shifting :-

In fig ① : R_4 is connected to a bias voltage V_B . To understand the effect of V_B , assume that both IIP voltages ($V_1 = V_2 = 0$) are zero.

- * The voltage at the op-amp Non-INV IIP terminal will be

$$V_A = IR_3$$

where

$$I = \frac{V_B}{R_3 + R_4}$$

$$V_A = V_B \cdot \frac{R_3}{R_3 + R_4} \quad \rightarrow ①$$



* The ckt behaves as Non-INV amplifier hence,

$$V_o = V_A \left(1 + \frac{R_2}{R_1} \right) \rightarrow \textcircled{2}$$

Substituting eq \textcircled{1} in eq \textcircled{2}, we get

$$V_o = V_B \left(\frac{R_3}{R_3 + R_4} \right) \cdot \left(1 + \frac{R_2}{R_1} \right)$$

But

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}$$

$$V_o = V_B \left(\frac{R_3}{R_3 + R_4} \right) \left(1 + \frac{R_4}{R_3} \right)$$

$$V_o = V_B \left(\frac{\cancel{R_3}}{\cancel{R_3} + R_4} \right) \left(\frac{R_3 + R_4}{\cancel{R_3}} \right)$$

$$\boxed{V_o = V_B}$$

i.e. there is a shift in the o/p level by an amount equal to the voltage V_B .

∴ By adjusting the voltage ' V_B ', it is possible to get any desired shift in the o/p level.



* Define the following terms as applied to an op-amp and mention their typical values for IC 741:

- i) CMRR
- ii) PSRR
- iii) Slew rate
- iv) Input Impedance

Jan-10, 8M

* Define the following parameters:

- i) Input offset voltage
- ii) CMRR
- iii) Slew rate

Mention their typical values for op-amp 741

June-10, 6M

* CMRR :-

CMRR is defined as the ratio of the open-loop gain 'M' to the Common mode gain ' A_{cm} '.

$$\boxed{CMRR = \frac{M}{A_{cm}}}$$

The CMRR is usually expressed in decibels

$$\boxed{(CMRR)_{dB} = 20 \log_{10} \left(\frac{M}{A_{cm}} \right) dB}$$

For 741 op-amp, typical value of CMRR is 90 dB

* PSRR :-

The PSRR is the ability of the op-amp to reject variations in the power supply voltages



ARUNKUMAR G M.Tech, Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.

$$\text{PSRR} = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$$

If a variation of 1V in V_{cc} & V_{EE} causes the o/p to change by 1V, then PSRR is 1 per volt.

For 741 op-amp, the PSRR is typically 30 mV/V.

* Slew rate :-

The Slew rate 'S' of an op-amp is the maximum rate at which the o/p voltage can change.

When the Slew rate is too slow for the I/P, then o/p will distort.

$$\text{Slew rate} = \frac{\Delta V}{\Delta t}$$

SI

$$S = \left. \frac{dV_o}{dt} \right|_{\text{max}}$$

Typical value for 741 op-amp is 0.5 V/ μ sec.

* O/p Impedance :-

O/p Impedance is the impedance as seen at the o/p terminal w.r.t. to ground.

$$Z_{\text{out}} = \frac{Z_o}{1 + MB}$$

Typical value for 741 op-amp is 75 Ω .



I/p Impedance :-

I/p Impedance of an ideal op-amp is infinite, but it will have a finite value depending on the type of application

$$Z_{in} = Z_i(1 + M\beta)$$

Typical value for 741 op-amp is $0.3 \text{ M}\Omega$

O/p Offset voltage :-

For the o/p voltage to be exactly equal to the I/p, the transistors Q₁ & Q₂ must be perfectly matched.

The o/p voltage can be calculated as

$$V_o = V_i - V_{BE1} + V_{BE2}$$

With $V_{BE1} = V_{BE2}$ and $V_i = 0$

$$\text{o/p } V_o = V_i = 0$$

* Now Suppose that the transistors are not perfectly matched and that $V_{BE1} = 0.7V$ & $V_{BE2} = 0.6V$ with $V_i = 0V$,

$$\text{then o/p } V_o = V_i - V_{BE1} + V_{BE2}$$

$$= 0 - 0.7V + 0.6V$$

$$V_o = -0.1V$$

This unwanted o/p is known as an o/p offset voltage.



I/p offset voltage :-

Now Suppose that the transistors are not perfectly matched & that $V_{BE1} = 0.7V$ while $V_{BE2} = 0.6V$.

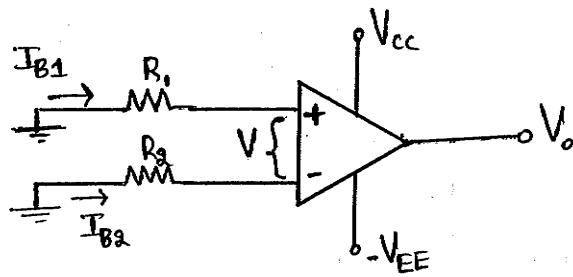
With the I/p $V_i = 0$,

$$\begin{aligned} V_o &= V_i - V_{BE1} + V_{BE2} \\ &= 0 - 0.7V + 0.6V \end{aligned}$$

$$V_o = -0.1V$$

* To Set V_o to ground level, the I/p would hence to be raised to $+0.1V$. This is termed as input offset voltage V_{ios} .

For 741 op-amp, typical value of $V_{ios} = 1mV$ & maximum value of $V_{ios} = 5mV$

* I/p offset current :-

$$V = I_B1 R_1 - I_B2 R_2$$

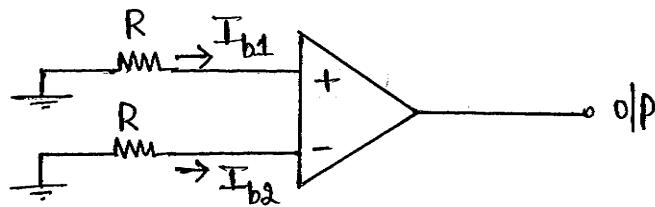
* The algebraic difference between the currents flowing into the two I/p terminals of the op-amp is called I/p offset current & denoted as I_{ios}

$$I_{ios} = |I_{b1} - I_{b2}|$$



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F81 741 op-amp, maximum value of I_{ios} is 200nA

I/p bias Current :-



* The average value of the two currents flowing into the op-amp input terminals is called I/p bias current.

$$I_b = \frac{I_{b1} + I_{b2}}{2}$$

F81 741 op-amp, maximum value of I_b is 500nA

Offset Nulling :-

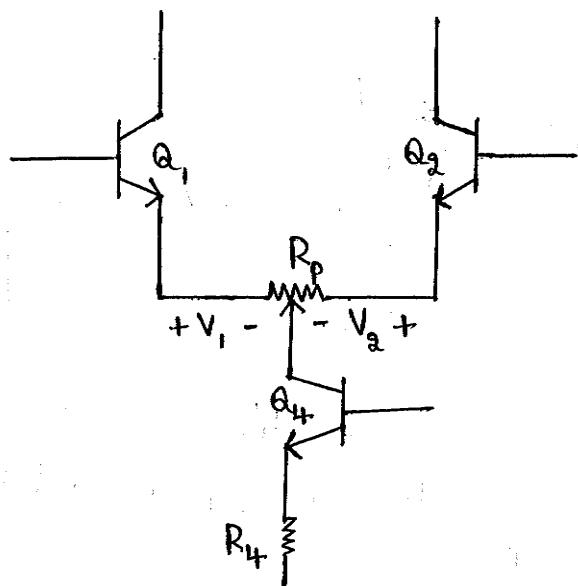


Fig: use of potentiometer for offset Nulling



To minimize the effect of offset voltages and currents, a variable resistance is introduced between the emitters of Q_1 & Q_2 as shown in figure.

The variable resistance R_p is the low resistance potentiometer which alters the voltage drop from base of each transistor to the common moving point of potentiometer. Hence the I_{IP} base current also get altered.

As I_{IP} offset current produces an offset voltage, by adjusting R_p , both I_{IP} offset current as well as input offset voltage can be nullled.

I_{IP} voltage range :-

The maximum positive going & negative going I_{IP} voltage that can be applied to the op-amp so that it functions properly is called its I_{IP} voltage range.

For 741 op-amp, I_{IP} voltage range of $\pm 13\text{V}$ for $\pm 15\text{V}$ Supply.



- * Define CMRR of an op-amp. If a Non-INV Amplifier is designed for a gain of 100 using an op-amp with 95 dB CMRR. calculate the Common mode o/p (V_{ocm}) for a Common mode I/P (V_{icm}) of 2V

Dec-10, 6M

- * CMRR is defined as the ratio of the open-loop gain 'M' to the Common mode gain ' A_{CM} '.

$$\boxed{CMRR = \frac{M}{A_{CM}}}$$

The CMRR is usually expressed in decibels

← 2M

$$\boxed{(CMRR)_{dB} = 20 \log_{10} \left(\frac{M}{A_{CM}} \right) dB}$$

Given: $A_V = 100$, $(CMRR)_{dB} = 95 \text{ dB}$, $V_{icm} = 2V$

WKT

$$\boxed{(CMRR)_{dB} = 20 \log_{10} (CMRR)}$$

$$CMRR = \text{antilog} \left(\frac{95}{20} \right)$$

$$\boxed{CMRR = 56,234} \quad \leftarrow 2M$$

WKT

$$V_{ocm} = \frac{V_{icm}}{CMRR} \cdot A_V = \frac{2V}{56234} \times 100$$

$$\boxed{V_{ocm} = 3.55 \text{ mV}} \quad \leftarrow 2M$$



- * Design a Non-INV amplifier to provide a gain 50 for an I_p of 100mV. Compute its I_p & o/p impedances. Given R_i=2MΩ, R_o=75Ω, I_{Bmax}=500nA, & M=2,00,000 for the op-amp (74H).

Dec-10, 8M

Given :- A_v = 50, V_i = 100mV, I_{Bmax} = 500nA

Sol :-

$$\text{Let } I_2 = 100 \times I_{B(\text{max})}$$

$$= 100 \times 500 \text{nA}$$

$$I_2 = 50 \mu\text{A}$$

$$* R_3 = \frac{V_i}{I_2} = \frac{100 \text{mV}}{50 \mu\text{A}} = 2 \text{k}\Omega \quad \leftarrow 1 \text{M}$$

$$* \text{WKT } A_v = \frac{V_o}{V_i}$$

$$V_o = A_v V_i = 50 \times 100 \text{mV}$$

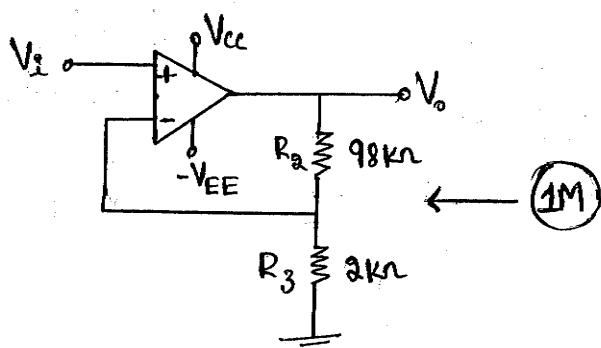
$$V_o = 5 \text{V}$$

$$* R_2 + R_3 = \frac{V_o}{I_2}$$

$$R_2 = \frac{V_o}{I_2} - R_3 = \frac{5 \text{V}}{50 \mu\text{A}} - 2 \text{k}\Omega$$

$$R_2 = 98 \text{k}\Omega$$

↑
1M



* Feedback Factor for Non-INV amplifier is $\beta = \frac{1}{A_v} = \frac{R_3}{R_2 + R_3} = \frac{98k\Omega}{9k\Omega + 98k\Omega}$

$$\boxed{\beta = 0.02}$$

* $Z_{in} = Z_s(1 + M\beta) = 2M\Omega (1 + 200000 \times 0.02)$

$$\boxed{Z_{in} = 8 \times 10^9 \Omega} \leftarrow \textcircled{2M}$$

* $Z_{out} = \frac{Z_o}{(1 + M\beta)} = \frac{75\Omega}{(1 + 200000 \times 0.02)}$

$$\boxed{Z_{out} = 18.75 m\Omega} \leftarrow \textcircled{2M}$$

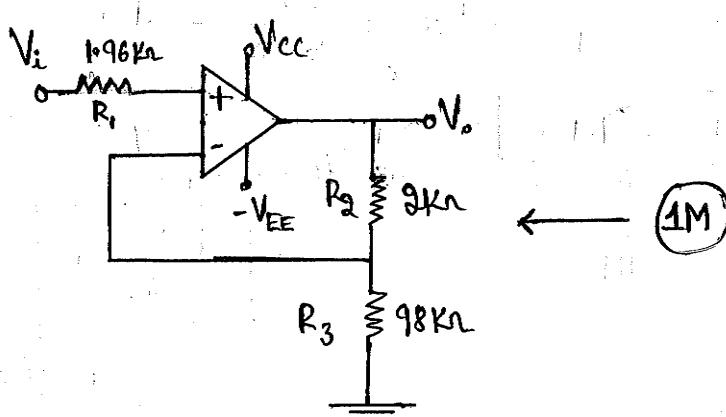
* How do you provide Compensation for the bias current for the amplifier of above question?

Dec - 10, 2M

Sol:- Compensation is done by using R_i ,

$$\text{i.e. } R_i = (R_2 || R_3) = \frac{R_2 R_3}{R_2 + R_3} = \frac{9k\Omega \times 98k\Omega}{9k\Omega + 98k\Omega}$$

$$\boxed{R_i = 1.96 k\Omega} \leftarrow \textcircled{1M}$$



OP-Amps as AC Amplifiers

Introduction :-

- * Op-amp can be used as dc as well as ac amplifiers.

For op-amp ac amplifiers, the coupling capacitors are necessary at the I/p as well as O/p terminals. These capacitors must not be allowed to interrupt the bias current paths to the op-amp I/p terminals.

This sometimes requires additional bias resistors which can affect the circuit I/p Impedance.

- * Since the capacitors have their highest impedances at the lowest signal frequency. All the coupling capacitor values are determined at the lower cut-off frequency ' f_l '.
- * The Impedance of coupling capacitors at f_l is usually one tenth of the resistance in series with them.
- * The f_l is determined using largest capacitor in the circuit and capacitive Impedance is made equal to the series resistance.



Capacitor - coupled voltage follower :-

- * Draw a capacitor coupled voltage follower ckt, and explain functions of the capacitors used. Also explain how these capacitors are to be chosen

June - 05, 8M (E&E)

- * Design a capacitor - coupled voltage follower using IC 741 op-amp. The lower cut-off frequency for the ckt is to be 100Hz and the load resistance is 4.7 k Ω . Draw the ckt & explain the operation.

Jan - 10, 12M

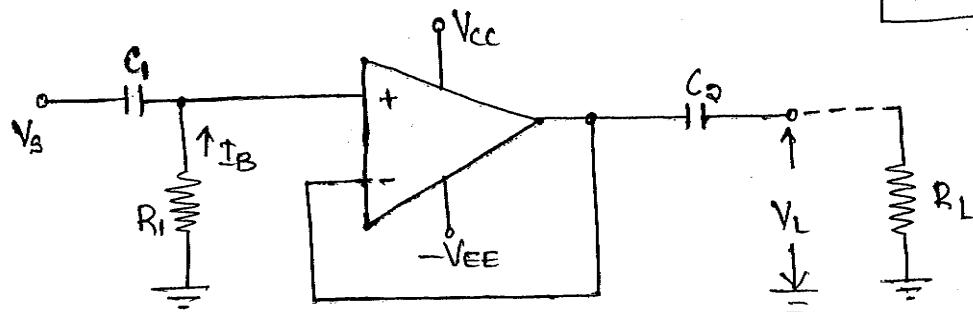
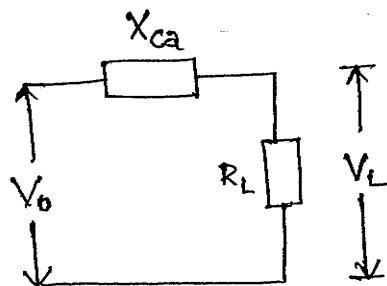
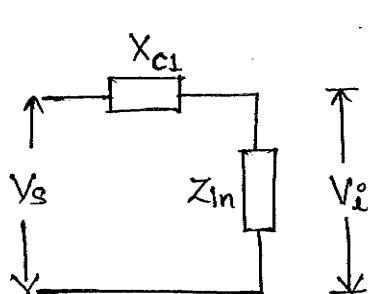


fig @ : capacitor coupled voltage follower ckt



- (b) The signal voltage is divided across X_{C1} & Z_{in}

- (c) The o/p voltage is divided across X_{C2} and R_L

Fig @ : shows a capacitor coupled voltage follower ckt.

- * The Non-INV terminal must be grounded via a resistor 'R_i'. This resistor is required to pass the bias current to the amplifier Non-INV terminal.



- * A resistor equal to ' R_1 ' might be included in series with the inverting terminal to equalize the $I_B R_B$ voltage & thus minimize the op offset voltage.
- * The op capacitor C_2 blocks the small dc offset voltage.

Design :

Design involves calculation of R_1 , C_1 and C_2 .

- * The maximum value of R_1 is determined as

$$R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

- * IIP Impedance of the ckt is

$$Z_{in} = R_1 \parallel Z'_i$$

Where $Z'_i = (1+M_B) Z_i$

Z'_i is the IIP Impedance at the NON-INV terminal & is very much larger than R_1

$$\therefore Z_{in} = R_1$$

- * Load resistor R_L normally has a lower resistance than R_1 .
- * At the lower 3dB frequency ' f_1 ', the impedance of C_1 should be much smaller than Z_{in} .

$$\therefore \text{At } f_1, X_{C1} = \frac{Z_{in}}{10}$$

$$\frac{1}{2\pi f_1 C_1} = \frac{R_1}{10}$$

$$\left\{ \begin{array}{l} Z_{in} = R_1 \& \\ X_{C1} = \frac{1}{2\pi f_1 C_1} \end{array} \right.$$

$$C_1 = \frac{10}{2\pi f_1 R_1}$$



$$\therefore C_1 = \frac{1}{2\pi f_1 (R_L / 10)}$$

from fig ⑥, the load voltage V_L is given by:

$$V_L = I R_L$$

$$\text{where } I = \frac{V_0}{R_L - j X_{C2}}$$

$$V_L = \frac{V_0 R_L}{R_L - j X_{C2}}$$

$$\therefore \text{Magnitude of } V_L = \frac{V_0 R_L}{\sqrt{R_L^2 + X_C^2}}$$

When $X_L = R_L$, then

$$V_L = \frac{V_0 R_L}{\sqrt{R_L^2 + R_L^2}} = \frac{V_0 R_L}{\sqrt{2} R_L} = \frac{V_0 \sqrt{2}}{\sqrt{2} R_L}$$

$$V_L = \frac{V_0}{\sqrt{2}}$$

$$V_L = 0.707 V_0$$

i.e. the ckt low 3 dB frequency f_1 occurs when

$$X_{C2} = R_L$$

$$\therefore X_{C2} = R_L \text{ at } f_1$$

$$\frac{1}{2\pi f_1 C_2} = R_L$$

$$C_2 = \frac{1}{2\pi f_1 R_L}$$



Capacitor - Coupled voltage follower :-

FORMULAE :- FOR #41.

$$1) R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$2) X_{C1} = \frac{R_1}{10} \text{ at } f_1 \text{ i.e. } C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$3) X_{C2} = R_L \text{ at } f_1 \text{ i.e. } C_2 = \frac{1}{2\pi f_1 R_L}$$

$$4) \text{ IIP Impedance, } Z_{in} = R_1$$

FORMULAE

FOR - LF 353 BIFET

1) For LF 353 BIFET op-amp, 1st select maximum resistance.
i.e. $R_1 = R_1(\text{max}) = 1M\Omega$

$$2) X_{C1} = \frac{R_1}{10} \text{ at } f_1 \text{ i.e. } C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$3) X_{C2} = R_L \text{ at } f_1 \text{ i.e. } C_2 = \frac{1}{2\pi f_1 R_L}$$

$$4) \text{ IIP Impedance. } Z_{in} = R_1$$



Problems

1) Design a capacitor coupled voltage follower using 741 op-amp. The lower cut-off frequency for the circuit is to be 50Hz and the load resistance is $R_L = 3.9\text{ k}\Omega$.

Given :- $f_l = 50\text{ Hz}$, $R_L = 3.9\text{ k}\Omega$, Assume $V_{BE} = 0.7\text{ V}$

For 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

Sol :-

$$* R_I(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{ V}}{500\text{nA}}$$

$$R_I(\text{max}) = 140\text{k}\Omega$$

Use standard value resistor

$$R_I(\text{max}) = 120\text{k}\Omega$$

$$* X_{C1} = \frac{R_I}{10} \text{ at } f_l$$

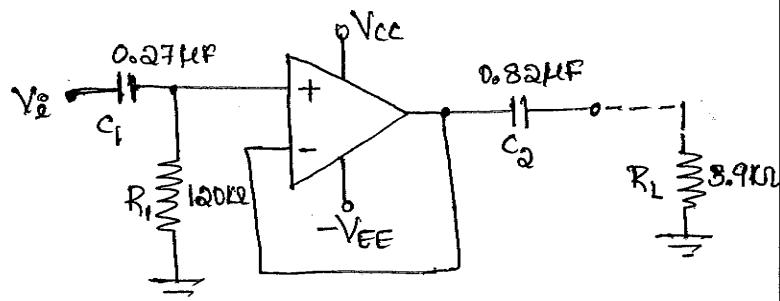
$$C_1 = \frac{1}{2\pi f_l (R_I/10)} = \frac{1}{2\pi \times 50 \times \left(\frac{120\text{k}\Omega}{10}\right)}$$

$$C_1 = 0.27\text{\mu F}$$

$$* X_{C2} = R_L \text{ at } f_l$$

$$C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 50 \times 3.9\text{k}\Omega}$$

$$C_2 = 0.82\text{\mu F}$$



NOTE :-

$$Z_{in} = R_1 = 120\text{k}\Omega$$



2) A 709 op-amp is used in the ckt of a capacitor coupled voltage follower for which $I_B(\text{max}) = 200\text{nA}$. It is desired to have lower cut-off frequency of 30Hz and to supply a load resistance of $5.6\text{k}\Omega$. Design the component values of R_1 , C_1 and C_2 .

Given :- $I_B(\text{max}) = 200\text{nA}$, $f_l = 30\text{Hz}$, $R_L = 5.6\text{k}\Omega$.

Assume $V_{BE} = 0.7\text{V}$.

Sol :-

$$* R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{200\text{nA}} = 350\text{k}\Omega$$

Use standard value resistor

$$R_1(\text{max}) = 330\text{k}\Omega$$

$$* X_{C1} = \frac{R_1}{10} \text{ at } f_l.$$

$$C_1 = \frac{1}{2\pi f_l (R_1/10)} = \frac{1}{2\pi \times 30\text{Hz} \times \left(\frac{330\text{k}\Omega}{10}\right)} = 0.1608\text{nF}$$

choose .

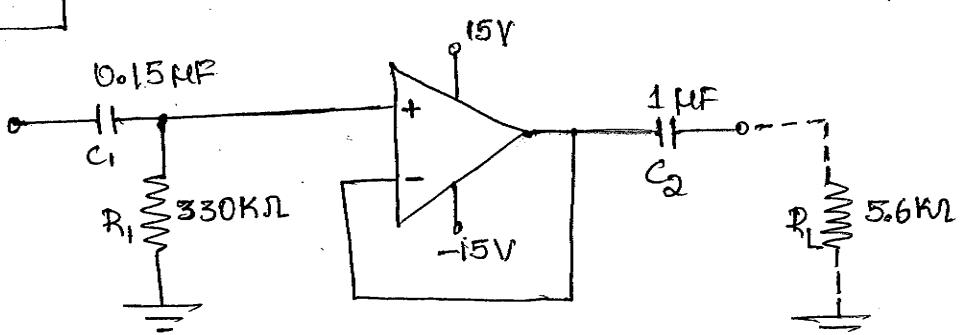
$$C_1 = 0.15\text{nF}$$

$$* X_{C2} = R_L \text{ at } f_l$$

$$C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 30 \times 3.9\text{k}\Omega} = 0.947\text{nF}$$

choose

$$C_2 = 1\text{nF}$$



NOTE :-

$$Z_{in} = R_1 = 330\text{k}\Omega$$



3) Design a capacitor coupled voltage follower using a 741 op-amp. The lower cut-off frequency for the circuit is to be 50Hz & the load resistance is $R_L = 4\text{ k}\Omega$.

Given :- $f = 50\text{ Hz}$, $R_L = 4\text{ k}\Omega$

for 741 op-amp: $I_B(\text{max}) = 500\text{nA}$

Assume $V_{BE} = 0.7\text{V}$.

$$\underline{\text{Sol :-}} * R_{ic(\text{max})} = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}} = 140\text{k}\Omega$$

choose: $R_{ic(\text{max})} = 120\text{k}\Omega$

$$* X_{C1} = \frac{R_1}{10} \text{ at } f_1.$$

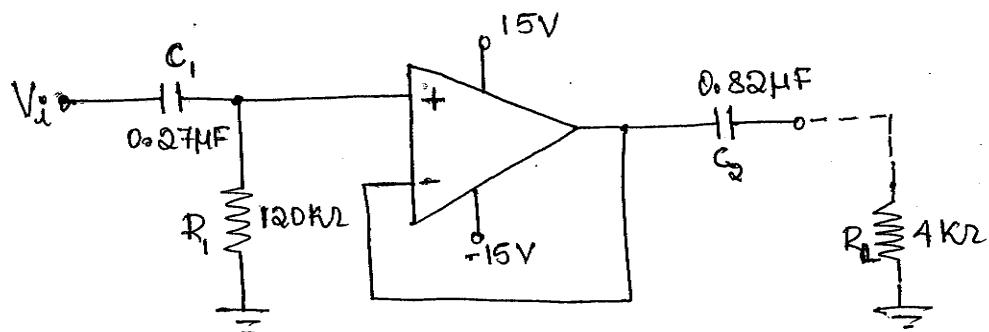
$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 50 \times (120\text{k}\Omega / 10)} = 0.27\text{nF}$$

$$C_1 = 0.27\text{nF}$$

$$* X_{C2} = R_L \text{ at } f_1$$

$$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 4\text{k}\Omega} = 0.79\text{nF}$$

choose $C_2 = 0.82\text{nF}$



NOTE :-

$$Z_{in} = R_1 = 120\text{k}\Omega$$



4) Design a capacitor coupled voltage follower using a 741 op-amp. The lower cut-off frequency of the ckt is to be 115 Hz. The load resistance is 6.8 k Ω

June-07, 6M (EE)

Given :- $f_l = 115 \text{ Hz}$, $R_L = 6.8 \text{ k}\Omega$

for 741 op-amp : $I_{B(\max)} = 500 \text{nA}$

$$\underline{\text{Sol :-}} * R_i(\max) = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7 \text{V}}{500 \text{nA}} = 140 \text{k}\Omega$$

choose. $R_i(\max) = R_i = 120 \text{k}\Omega$ ← (1m)

$$* X_{C1} = \frac{R_i}{10} \text{ at } f_l$$

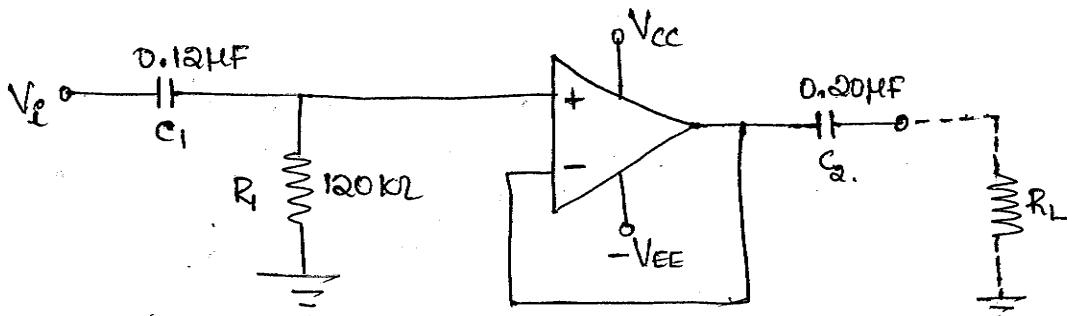
$$C_1 = \frac{1}{2\pi f_l \left(\frac{R_i}{10} \right)} = \frac{1}{2\pi \times 115 \times \left(\frac{120 \text{k}\Omega}{10} \right)} = 0.115 \mu\text{F}$$

choose. $C_1 = 0.12 \mu\text{F}$ ← (2m)

$$* X_{C2} = R_L \text{ at } f_l.$$

$$C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 115 \times 6.8 \text{k}\Omega} = 0.20 \mu\text{F}.$$

$C_2 = 0.20 \mu\text{F}$ ← (2m)



NOTE :-

$$Z_{in} = R_i = 120 \text{k}\Omega$$



Capacitor - Coupled Voltage follower :-LF 353 BIFET op-amp → Problems.

- 1). Design a capacitor - coupled voltage follower using a LF 353 BIFET op-amp. The lower cut-off frequency for the circuit is to be 50 Hz & the load resistance is $R_L = 3.9 \text{ k}\Omega$.

Given :- $R_L = 3.9 \text{ k}\Omega$, $f_l = 50 \text{ Hz}$

Sol :- For LF 353 BIFET

* Select $R_1 = 1 \text{ M}\Omega$

* $X_{C1} = \frac{R_1}{10}$ at f_l

$$C_1 = \frac{1}{2\pi f_l \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 50 \times \left(\frac{1 \text{ M}\Omega}{10} \right)}$$

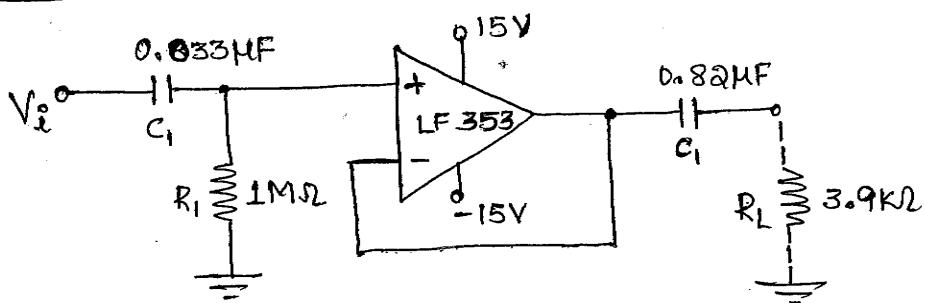
$C_1 = 0.032 \mu\text{F}$

choose : $C_1 = 0.033 \mu\text{F}$

* $X_{C2} = R_L$ at f_l

$$C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 50 \times 3.9 \text{ k}\Omega}$$

$C_2 = 0.82 \mu\text{F}$



Q) A capacitor - coupled voltage follower is to be designed to have a lower cut off frequency of 110 Hz. The load resistance is 6.8 kΩ & op-amp used is LM 353B. Design a suitable ckt.

Given :- $R_L = 6.8 \text{ k}\Omega$, $f_l = 110 \text{ Hz}$.

Sol :- For LM 353B

* select $R_1 = 1 \text{ M}\Omega$

$$* X_{C1} = \frac{R_1}{10} \text{ at } f_l$$

$$C_1 = \frac{1}{2\pi f_l \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 110 \times \left(\frac{1 \text{ M}\Omega}{10} \right)}$$

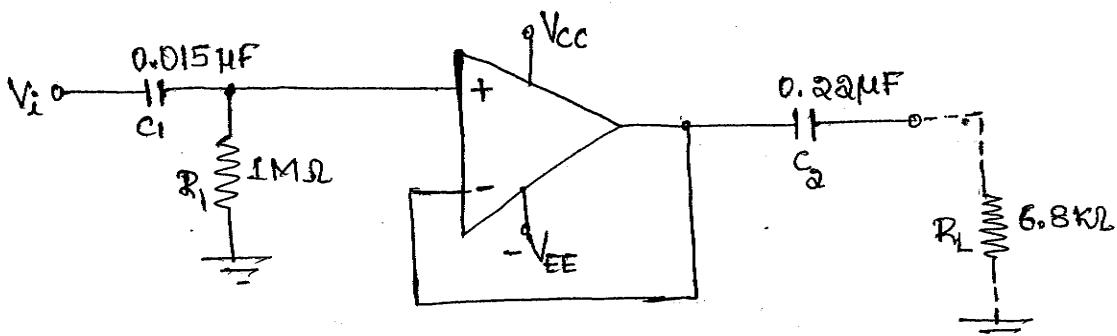
$$C_1 = 0.0144 \mu\text{F}$$

choose $C_1 = 0.015 \mu\text{F}$

$$* X_{C2} = R_L \text{ at } f_l$$

$$C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 110 \times 6.8 \text{ k}\Omega} = 0.213 \mu\text{F}$$

choose $C_2 = 0.22 \mu\text{F}$



NOTE :- $Z_{in} = R_1 = 1 \text{ M}\Omega$.



* Design a capacitor-coupled voltage follower using IC 741 op-amp. The lower cut-off frequency for the ckt. is to be 100Hz and the load resistance is $4.7\text{ k}\Omega$. Draw the ckt & explain the operation.

Jan - 10, 12 M

Sol :-

- i) Draw the ckt of capacitor-coupled voltage follower & explain with design procedure. [6M]
- ii) Given :- $f_1 = 100\text{ Hz}$, $R_L = 4.7\text{ k}\Omega$

Sol :- For 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

$$* R_1(\text{max}) = \frac{0.1\text{ V}_BE}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{ V}}{500\text{nA}} = 140\text{k}\Omega$$

choose

$$R_1 = 120\text{k}\Omega$$

$$* X_{C1} = \frac{R_1}{10} \text{ at } f_1.$$

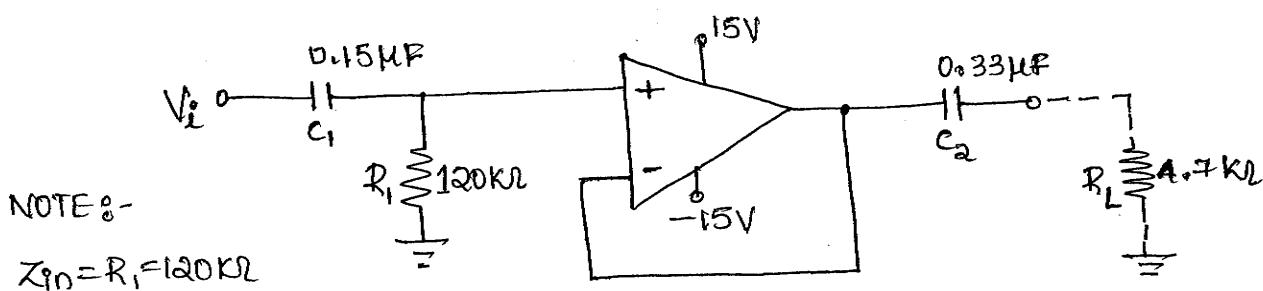
$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 100 \times \left(\frac{120\text{k}\Omega}{10} \right)} = 0.132\text{nF}$$

choose

$$C_1 = 0.15\text{nF}$$

$$* X_{C2} = R_L \text{ at } f_1.$$

$$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 100 \times 4.7\text{k}\Omega} = 0.33\text{nF}$$



* A capacitor coupled voltage follower is to be designed to have a lower cut-off frequency of 120Hz. The load resistance is 8.2k Ω & the op-amp used has a maximum I_{IP} bias current of 600nA. Design a suitable ckt.

Jan-05, 6M(EE)

Given :- $f_l = 120\text{Hz}$, $R_L = 8.2\text{k}\Omega$, $I_{B(\text{max})} = 600\text{nA}$.

Sol :- * $R_{I(\text{max})} = \frac{0.1V_{BE}}{I_{B(\text{max})}} = \frac{0.1 \times 0.7V}{600\text{nA}} = 116.667\text{k}\Omega$

choose $R_{I(\text{max})} = 120\text{k}\Omega$

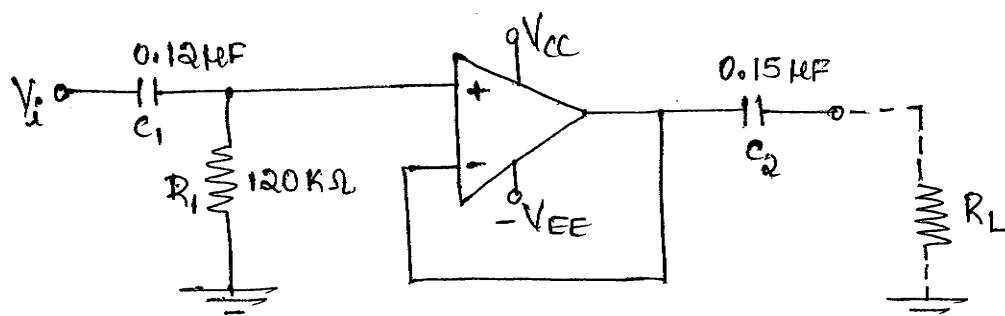
* $C_1 = \frac{1}{2\pi f_l R_I} = \frac{1}{2\pi \times 120 \times \left(\frac{120\text{k}\Omega}{10}\right)} = 0.11\text{nF}$

choose - $C_1 = 0.12\mu\text{F}$

* $C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 120 \times 8.2\text{k}\Omega}$

$C_2 = 0.1617\text{nF}$

choose , $C_2 = 0.15\mu\text{F}$



High Zin capacitor - coupled voltage follower :-

- * Sketch the circuit of a high Zin capacitor coupled voltage follower. Briefly explain its operation & show that the Z_{IP} impedance is very high compared to the capacitor coupled voltage follower.

June - 10, 6M

- * Explain the operation of a high Z_{IP} impedance capacitor - coupled voltage follower, with a neat circuit diagram. Obtain the expression for Z_{IP} Impedance of the circuit.

June - 09, 8M

- * Sketch the ckt of a high Zin capacitor coupled voltage follower. Obtain the expression for Z_{IP} Impedance of the circuit.

Jan - 10, 8 M(EE)

June - 09, 8M(EE)

June - 06, 6M(EE)

Jan - 05, 6M

DEC - 10, 8M

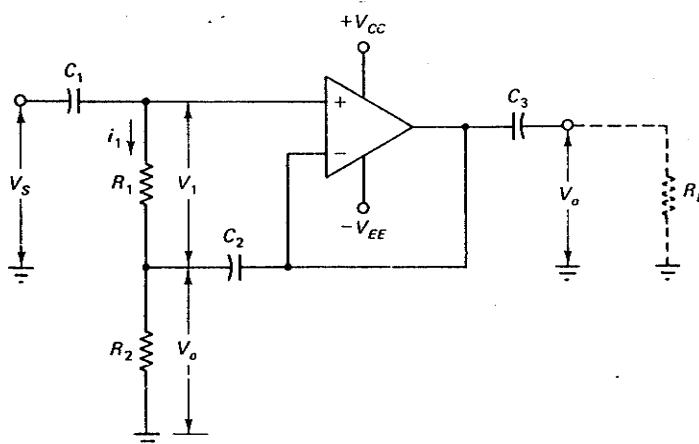


Figure : High input impedance capacitor-coupled voltage follower. Feedback via C_2 to the junction of R_1 and R_2 gives an input impedance of $Z_{in} = (1 + M)R_1$.



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- * The ~~z~~ Z_{IP} Impedance of the capacitor-coupled voltage follower is set by the value of resistor R_1 . This gives a much smaller Z_{IP} Impedance than the direct coupled voltage follower.
 - * Fig ① shows a method by which the Z_{IP} impedance of the capacitor-coupled voltage follower can be substantially increased.
 - * Capacitor C_2 couples the circuit opv voltage to the junction of resistors R_1 & R_2 .
- C_2 behaves as an ac short circuit. so that ' V_o ' is developed across R_2 .

- * Applying KVL from source, R_1 & R_2 ,

$$V_s - V_i - V_o = 0.$$

The voltage across R_1 is V_1 & is given by

$$V_1 = V_s - V_o \rightarrow ①$$

WKT open-loop gain is given by $M = \frac{V_o}{V_1}$

$$V_o = MV_1 \rightarrow ②$$

Sub eq ② in eq ①, we get

$$\underbrace{V_i}_{V_i} = V_s - MV_1$$

$$MV_1 + V_i = V_s.$$

$$V_1(1+M) = V_s$$

$$V_1 = \frac{V_s}{(1+M)} \rightarrow ③$$



* The current i_1 is given by :

$$i_1 = \frac{V_s}{R_1} \rightarrow ④$$

sub eq ③ in eq ④ , we get

$$i_1 = \frac{V_s}{(1+M)R_1} \rightarrow ⑤$$

* IIP resistance

$$Z_{in} = \frac{V_s}{i_1} \rightarrow ⑥$$

sub eq ⑤ in eq ⑥ , we get

$$Z_{in} = \frac{\frac{V_s}{(1+M)R_1}}{\frac{V_s}{R_1}}$$

$$Z_{in} = (1+M)R_1 \rightarrow ⑦$$

since open-loop gain 'M' is very high, this modifies the ckt has very high IIP impedance.

But if stray capacitance b/w the IIP & ground is present , then IIP Impedance reduces.

Design steps :-

$$1) P_{B(max)} = \frac{0.1 V_{BE}}{I_B(max)}$$

2) $R_1(max)$ is split into two equal resistors R_1 & R_2

$$\therefore R_1 = R_2 = \frac{R_1(max)}{2}$$



$$3) \therefore C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10} \right)}$$

$$4) C_1 = C_2$$

$$5) C_3 = \frac{1}{2\pi f_1 R_L}$$

$$6) Z_{in} = (1+M)R_1$$

PROBLEMS

1) Design a high Z_{in} capacitor coupled voltage follower using 741 op-amp having lower cut-off frequency 50Hz & the load resistance is $R_L = 3.9k\Omega$. Also determine the minimum theoretical input impedance of the ckt.

Given :- $f_1 = 50\text{Hz}$, $R_L = 3.9k\Omega$

June -10, 6M (EE)

for op-amp 741 : $I_B(\text{max}) = 500\text{nA}$, Assume $V_{BE} = 0.7\text{V}$

$$M(\text{min}) = 50000$$

Sol:-

$$* R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500 \text{nA}} = 140k\Omega$$

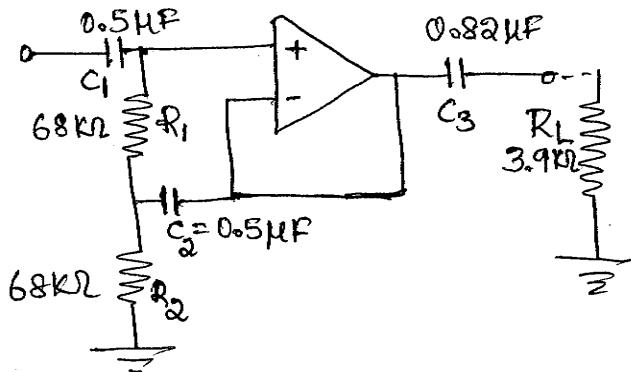
$$* R_1 = R_2 = \frac{R_1(\text{max})}{2} = \frac{140k\Omega}{2} = 70k\Omega \quad \text{choose} \quad R_1 = R_2 = 68k\Omega$$

$$* C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10} \right)} = \frac{1}{2\pi \times 50\text{Hz} \times \left(\frac{68k\Omega}{10} \right)} = 0.5\text{mF}$$

$$* C_3 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 3.9k\Omega} = 0.82\text{mF}$$

$$* Z_{in}(\text{min}) = (1+M(\text{min})) R_1 \\ = (1+50000) 68k\Omega$$

$$Z_{in}(\text{min}) = 3400\text{M}\Omega$$



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2) A capacitor coupled voltage follower using a 709 op-amp is to be designed to have IIP impedance and to have a lower cut-off frequency of 80Hz. The load resistance is 10k Ω . Design the circuit and find minimum theoretical IIP Impedance of the ckt. [Assume M=70,000 & I_{B(max)}=200nA for 709 op-amp].

Given :- f_l=80Hz, R_L=10k Ω

I_{B(max)}=200nA, M=70,000 - Assume : V_{BE}=0.7V.

Sol:- * $R_{i(\max)} = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7V}{200nA} = 350k\Omega$

* $R_1 = R_2 = \frac{R_{i(\max)}}{2} = \frac{350k\Omega}{2} = 175k\Omega$

choose : $R_1 = R_2 = 180k\Omega$

* $C_2 = \frac{1}{2\pi f_l \left(\frac{R_2}{10} \right)} = \frac{1}{2\pi \times 80 \times \left(\frac{180k\Omega}{10} \right)} = 0.11\mu F$

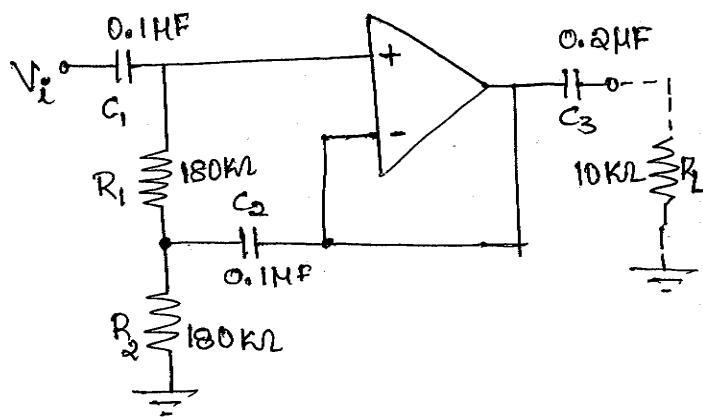
choose $C_2 = 0.1\mu F$.

* $C_1 = C_2 = 0.1\mu F$

* $C_3 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 80 \times 10k\Omega} = 0.198\mu F$

choose $C_3 = 0.2\mu F$.

* $Z_{in.} = (1+M)R_1 =$
 $= (1+70000)180k\Omega$
 $= 1.26 \times 10^6 \Omega$.



3) Design high Zin capacitor coupled voltage follower using an op-amp having lower cut-off frequency of 50Hz and maximum I_{IP} bias current of 500nA. The load resistance is 3.3kΩ if open loop gain of op-amp is 10⁵, find ideal value of I_{IP} impedance of the ckt.

Given :- f_l = 50Hz, I_{B(max)} = 500nA, R_L = 3.3kΩ,
M = 10⁵. Assume V_{BE} = 0.7V.

Sol :-

$$* R_{i(max)} = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7 \text{V}}{500 \text{nA}} = \underline{\underline{140 \text{k}\Omega}}$$

$$* R_1 = R_2 = \frac{R_{i(max)}}{2} = \frac{140 \text{k}\Omega}{2} = \underline{\underline{70 \text{k}\Omega}}$$

choose

$$\boxed{R_1 = R_2 = 68 \text{k}\Omega}$$

$$* C_2 = \frac{1}{2\pi f_l \left(\frac{R_2}{10} \right)} = \frac{1}{2\pi \times 50 \times \left(\frac{68 \text{k}\Omega}{10} \right)} = \underline{\underline{0.468 \text{nF}}}$$

choose

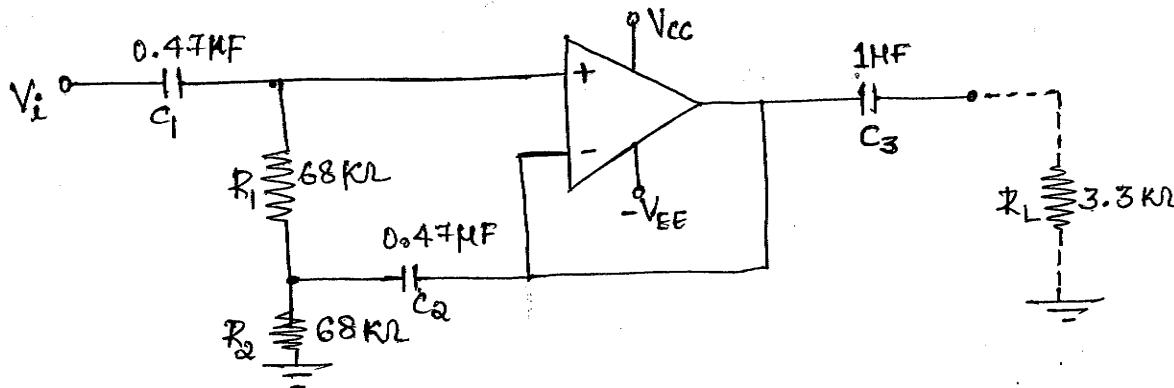
$$\boxed{C_2 = 0.47 \text{nF}}$$

$$* C_1 = C_2 = 0.47 \text{nF}$$

$$* C_3 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 50 \times 3.3 \text{k}\Omega} = \underline{\underline{0.964 \text{nF}}}$$

$$\text{choose } \boxed{C_3 = 1 \text{nF}}$$

$$* Z_{in} = (1+M) R_1 = (1+10^5) \times 68 \text{k}\Omega = \underline{\underline{6800 \text{M}\Omega}}$$



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4) Design Zin capacitor coupled voltage follower using an op-amp having lower cut-off frequency of 50Hz & maximum I_B bias current of 500nA. The load resistance is 3.6kΩ. If the open loop gain is 2×10^5 , find ideal value of Z_{IP} Impedance of the ckt.

June - 10, 8m

Given :- $f_l = 50\text{Hz}$, $I_B(\text{max}) = 500\text{nA}$, $R_L = 3.6\text{k}\Omega$, $M = 2 \times 10^5$

$$\text{Sol :- } R_i(\text{max}) = \frac{0.1 \text{ VBE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}} = 140\text{k}\Omega$$

$$* R_1 = R_2 = \frac{R_{\text{max}}}{2} = \frac{140\text{k}\Omega}{2} = 70\text{k}\Omega \quad \text{choose } R_1 = R_2 = 68\text{k}\Omega \quad \leftarrow (2m)$$

$$* C_2 = \frac{1}{2\pi f_l \left(\frac{R_2}{10} \right)} = \frac{1}{2\pi \times 50 \times \left(\frac{68\text{k}}{10} \right)} = 0.468\text{ }\mu\text{F}$$

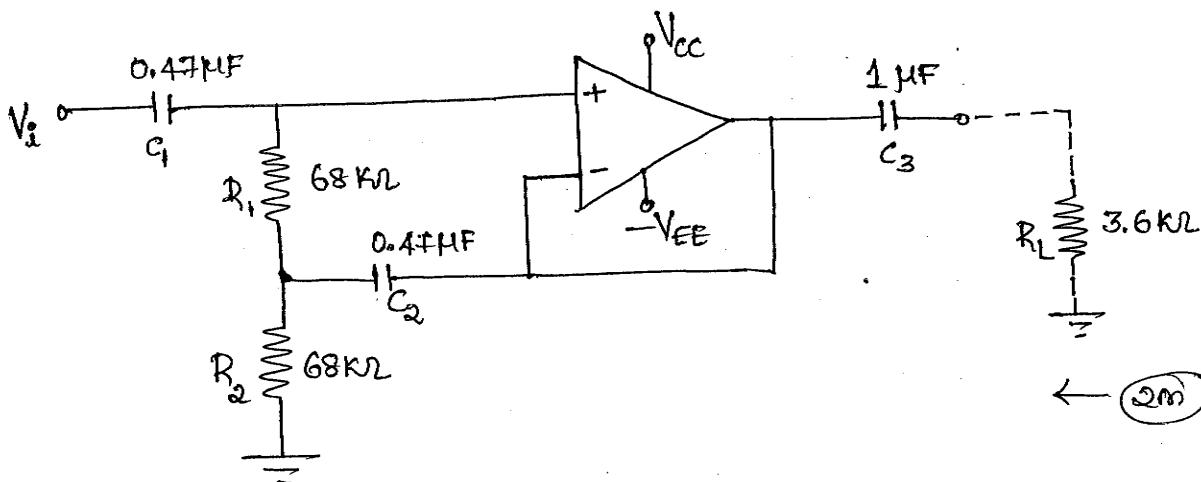
choose $C_2 = 0.47\text{ }\mu\text{F}$

$$* C_1 = C_2 = 0.47\text{ }\mu\text{F} \quad \leftarrow (2m)$$

$$* C_3 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 50 \times 3.6\text{k}\Omega} = 0.884\text{ }\mu\text{F}$$

choose $C_3 = 1\text{ }\mu\text{F}$

$$* Z_{in} = (1+M) R_1 = (1+2 \times 10^5) \times 68\text{k}\Omega = 13600\text{M}\Omega \quad \leftarrow (2m)$$



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Capacitor Coupled NON-INV amplifier :-

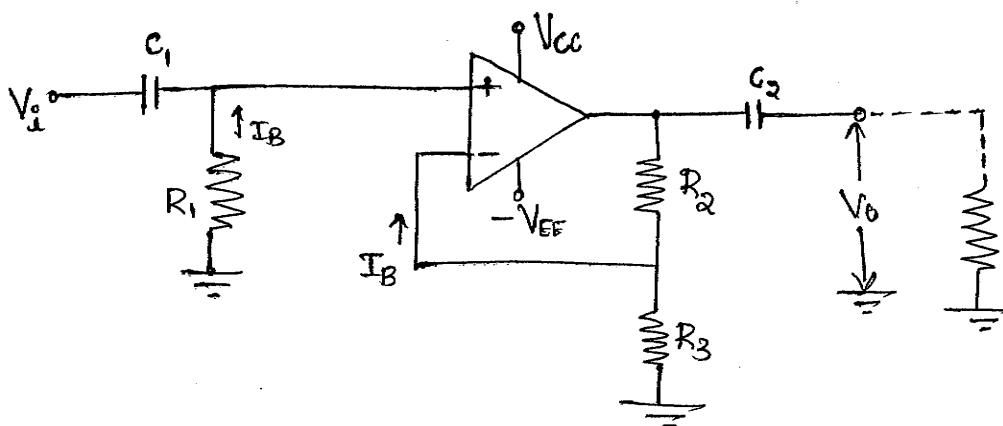


Fig ① : capacitor - coupled Non- INV amplifier.

- * In capacitor - coupled Non-INV amplifier, the Non-INV O/p terminal is grounded via a resistor to provide a path for the O/p bias current.
- * the resistor R_1 may be made equal to $R_2 \parallel R_3$ to compensate for the dc offset voltage at the O/p. since the o/p is also capacitor coupled, it is not of much importance.
- * The Zin impedance is given by $Z_{in} = R_1$

Design steps:-

$$\Rightarrow R_1 = R_{1(\max)} = \frac{0.1 V_{BE}}{I_{B(\max)}}$$

$$2) X_{C1} = \frac{R_1}{10} \text{ at } f_1.$$

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$



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3) $X_{C2} = R_L$ at f_1 .

$$C_2 = \frac{1}{2\pi f_1 R_L}$$

4) $I_2 = 100 I_B(\text{max})$

$$5) R_3 = \frac{V_o}{I_2}$$

$$6) A_V = \frac{V_o}{V_i} \quad \& .$$

$$V_o = A_V V_i$$

$$7) R_2 + R_3 = \frac{V_o}{I_2}$$

[OR]

$$A_V = 1 + \frac{R_2}{R_3}$$

$$R_2 = \frac{V_o}{I_2} - R_3$$

$$\frac{R_2}{R_3} = (A_V - 1)$$

$$R_2 = R_3 (A_V - 1)$$

8) Input impedance

$$Z_{in} = R_1$$



PROBLEMS

1) Using a 741 op-amp, design a capacitor coupled Non-INV amplifier to have a voltage gain of approxima-tely 66. The signal amplitude is to be 15mV. The load resistor is $2.2\text{ k}\Omega$ and the lower cut-off frequency is to be 120Hz. Make the necessary modifications to give the highest I_{IP} impedance & determine the required capacitor values.

Given :- $A_v = 66$, $R_L = 2.2\text{ k}\Omega$, $f = 120\text{ Hz}$, $V_i = 15\text{ mV}$.

for 741 OP-amp : $I_{B(\max)} = 500\text{nA}$

Assume $V_{BE} = 0.7\text{V}$

Sol :-

$$\Rightarrow R_{I(\max)} = \frac{0.1V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7\text{V}}{500 \times 10^{-9}} = 140\text{k}\Omega$$

choose $R_I = R_{I(\max)} = 120\text{k}\Omega$

$$2) C_1 = \frac{1}{2\pi f_1 \left(\frac{R_I}{10} \right)} = \frac{1}{2\pi \times 120 \times \left(\frac{120\text{k}\Omega}{10} \right)} = 0.11\text{HF}$$

choose $C_1 = 0.12\mu\text{F}$

$$3) C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 120 \times 2.2\text{k}\Omega} = 0.6\text{HF}$$

choose $C_2 = 0.68\mu\text{F}$

$$4) I_2 = 100 \times I_{B(\max)} = 100 \times 500\text{nA} = 50\mu\text{A}$$

$$5) R_3 = \frac{V_o}{I_2} = \frac{15\text{mV}}{50\mu\text{A}} = 300\Omega \quad \text{choose } R_3 = 270\Omega$$



Now, I_2 becomes. $I_2 = \frac{V_i}{R_3} = \frac{15\text{mV}}{270\Omega}$

$$I_2 = 55.6\mu\text{A}$$

6) WKT $V_o = A_v V_i = 66 \times 15\text{mV}$

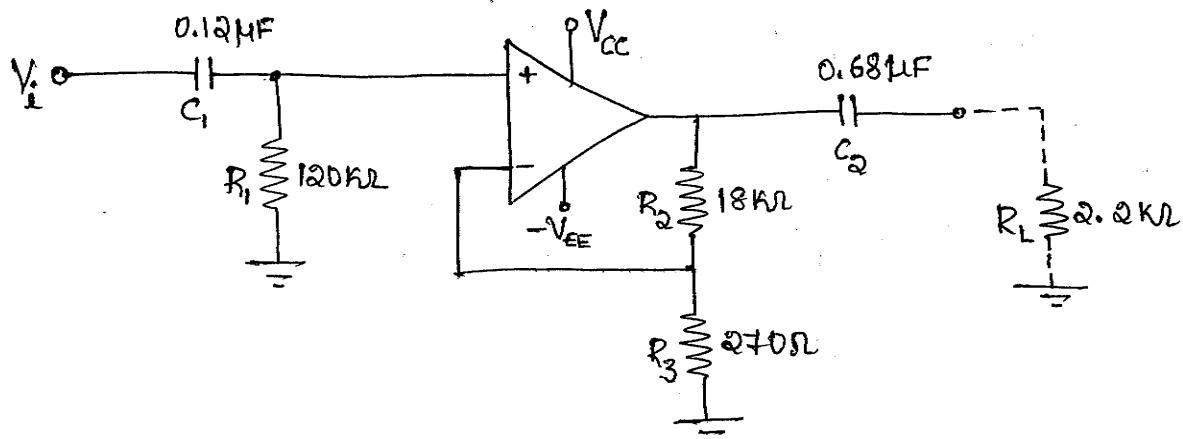
$$V_o = 990\text{mV}$$

7) $R_2 = \left(\frac{V_o}{I_2} - R_3 \right) = \left(\frac{990\text{mV}}{50\mu\text{A}} - 270\Omega \right)$

$$R_2 = 17.53\text{k}\Omega$$

choose

$$R_2 = 18\text{k}\Omega$$



Q) A capacitor - coupled Non-INV amplifier is to be used with $A_V = 120$ and $V_L = 4.2$ Volts. The load resistance is $8.2\text{ k}\Omega$ and the lower cut-off frequency is to be 60Hz . Design a suitable circuit using 715 op-amp for which $I_B(\text{max}) = 1.5\mu\text{A}$.

Given :- $A_V = 120$, $V_L = V_o = 4.2\text{V}$, $R_L = 8.2\text{ k}\Omega$, $f_l = 60\text{Hz}$,
 $I_B(\text{max}) = 1.5\mu\text{A}$.

Sol :-

$$1) R_{1(\text{max})} = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{1.5 \mu\text{A}} = 46.67\text{ k}\Omega$$

choose. $R_1 = R_{1(\text{max})} = 47\text{ k}\Omega$

$$2) C_1 = \frac{1}{2\pi f_l \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 60 \times 4.7\text{k}\Omega} = 0.564\text{ nF}$$

choose. $C_1 = 0.56\text{ nF}$

$$3) C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 60 \times 8.2 \times 10^3} = 0.323\text{ nF}$$

choose. $C_2 = 0.33\text{ nF}$

$$4) I_2 = 100 \times I_B(\text{max}) = 100 \times 1.5\mu\text{A} = 0.15\text{mA}$$

$$5) R_3 = \frac{V_i}{I_2}$$

$$\text{WKT } A_V = \frac{V_o}{V_i} \Rightarrow V_i = \frac{V_o}{A_V} = \frac{4.2\text{V}}{120} = 35\text{mV}$$

$$R_3 = \frac{35\text{mV}}{0.15\text{mA}} = 233.33\Omega$$

choose $R_3 = 230\Omega$



Now I_2 becomes

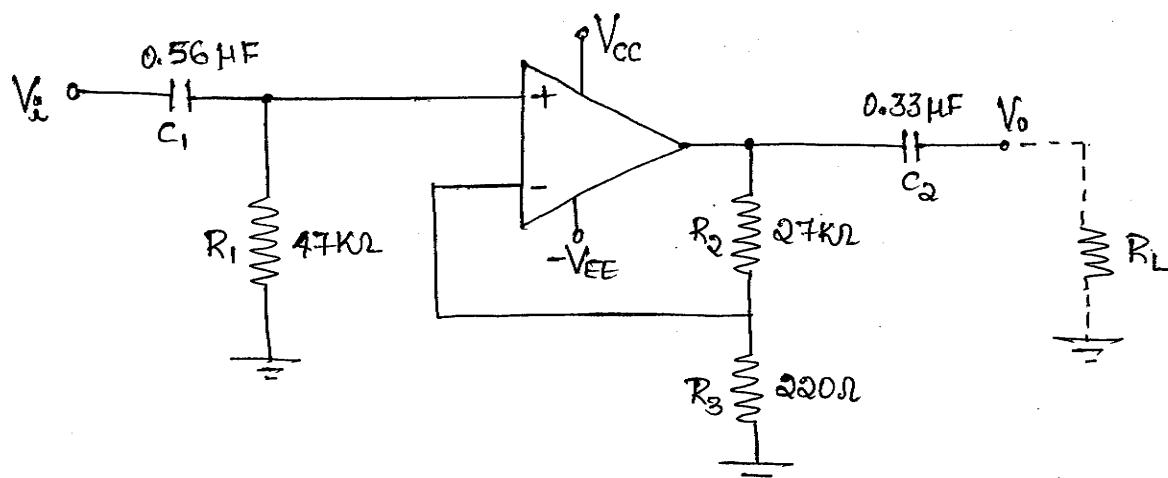
$$I_2 = \frac{V_i}{R_3} = \frac{35\text{mV}}{220\Omega} = \underline{\underline{0.159\text{mA}}}$$

6) $R_2 = \left(\frac{V_o}{I_2} - R_3 \right) = \left(\frac{4.2\text{V}}{0.159\text{mA}} - 220\Omega \right)$

$$R_2 = 26.19\text{k}\Omega$$

choose

$$R_2 = 27\text{k}\Omega$$



3) Design a capacitor coupled Non-INV amplifier having Voltage gain of about 75 and the source voltage is 10mV. We following data for the op-amp used.

For op-amp used : $I_B(\text{max}) = 500\text{nA}$, lower - cutoff freq = 100Hz, the load resistance is $3.3\text{k}\Omega$.

Given :- $A_V = 75$, $V_i = 10\text{mV}$, $I_B(\text{max}) = 500\text{nA}$, $f_l = 100\text{Hz}$, $R_L = 3.3\text{k}\Omega$.

Sol :-

$$1) R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}} = 140\text{k}\Omega$$

choose.

$$R_1 = R_1(\text{max}) = 120\text{k}\Omega$$

2)

$$C_1 = \frac{1}{2\pi f_l \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 100 \times \left(\frac{120\text{k}\Omega}{10} \right)} = 0.132\mu\text{F}$$

choose.

$$C_1 = 0.15\mu\text{F}$$

3)

$$C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 100 \times 3.3\text{k}\Omega} = 0.482\mu\text{F}$$

choose.

$$C_2 = 0.5\mu\text{F}$$

4)

$$I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$$

$$I_2 = 50\text{\textmu A}$$

5)

$$R_3 = \frac{V_i}{I_2} = \frac{10\text{mV}}{50\text{\textmu A}} = 200\Omega$$

$$R_3 = 200\Omega$$



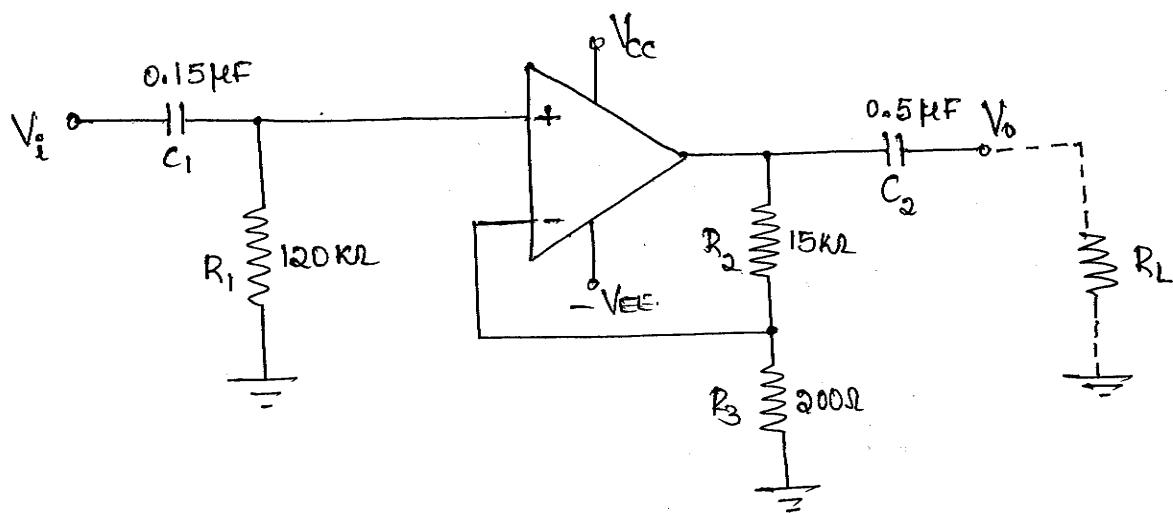
$$6) R_2 = \left(\frac{V_o}{I_2} - R_3 \right)$$

$$= \left(\frac{750 \text{ mV}}{50 \mu\text{A}} - 200\Omega \right)$$

$$V_o = A_v \times V_i = 75 \times 10 \text{ mV} = 750 \text{ mV.}$$

$$R_2 = 14.8 \text{ k}\Omega$$

choose $R_2 = 15 \text{ k}\Omega$



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A) A capacitor coupled Non-INV amplifier using op-amp is to have $A_v = 100$ and $V_o = 5V$. The load resistance is $10\text{ k}\Omega$ and the lower cut-off frequency is to be 100 Hz . Design a suitable ckt.

June-08, 8M

Given :- $A_v = 100$, $V_o = 5V$, $R_L = 10\text{ k}\Omega$, $f_l = 100\text{ Hz}$.

For 741 op-amp : $I_B(\text{max}) = 500\text{nA}$.

Sol:-

$$* R_I(\text{max}) = \frac{0.1 \text{ VBE}}{I_B(\text{max})} = \frac{0.1 \times 0.7V}{500\text{nA}} = \underline{\underline{140\text{ k}\Omega}}$$

choose. $R_I = 120\text{ k}\Omega$

$$* C_1 = \frac{1}{2\pi f_l \left(\frac{R_I}{10} \right)} = \frac{1}{2\pi (100\text{Hz}) \times \left(\frac{120\text{ k}\Omega}{10} \right)} = 0.132\text{ }\mu\text{F}$$

choose. $C_1 = 0.15\text{ }\mu\text{F}$

$$* C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 100 \times 10\text{ k}\Omega} = 0.159\text{ }\mu\text{F}$$

choose $C_2 = 0.15\text{ }\mu\text{F}$

$$* I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA} = \underline{\underline{50\text{ }\mu\text{A}}}$$

$$* R_3 = \frac{V_i}{I_2}$$

$$\text{WKT } A_v = \frac{V_o}{V_i}$$

$$V_i = \frac{V_o}{A_v} = \frac{5V}{100} = \underline{\underline{50\text{ mV}}}$$



$$* R_3 = \frac{50mV}{50\mu A} = \underline{\underline{1k\Omega}}$$

$$* R_2 = \left(\frac{V_o}{I_2} - R_3 \right) = \left(\frac{5V}{50\mu A} - 1k\Omega \right)$$

$$R_2 = 99k\Omega$$

OR

$$A_V = 1 + \frac{R_2}{R_3}$$

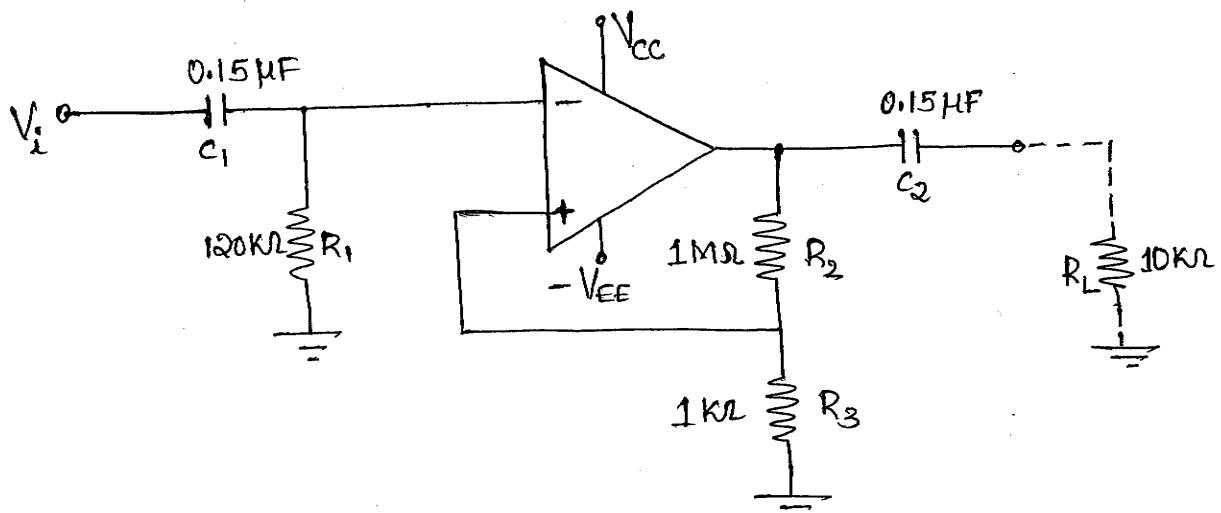
$$\frac{R_2}{R_3} = (A_V - 1)$$

$$R_2 = R_3(A_V - 1)$$

$$= 1k\Omega (100 - 1)$$

$$R_2 = 99k\Omega$$

choose . $R_2 = 1M\Omega$



5) A Non-INV amplifier as in fig ① has the following components $R_1 = 33\text{ k}\Omega$, $R_2 = 150\text{ k}\Omega$, $R_3 = 1.5\text{ k}\Omega$, $R_L = 4.7\text{ k}\Omega$, $C_1 = 0.39\mu\text{F}$, $C_2 = 0.27\mu\text{F}$. Determine the ckt voltage gain, Z_{in} impedance, and lower cut off freq.

[Jan -10, 6M(EE)]

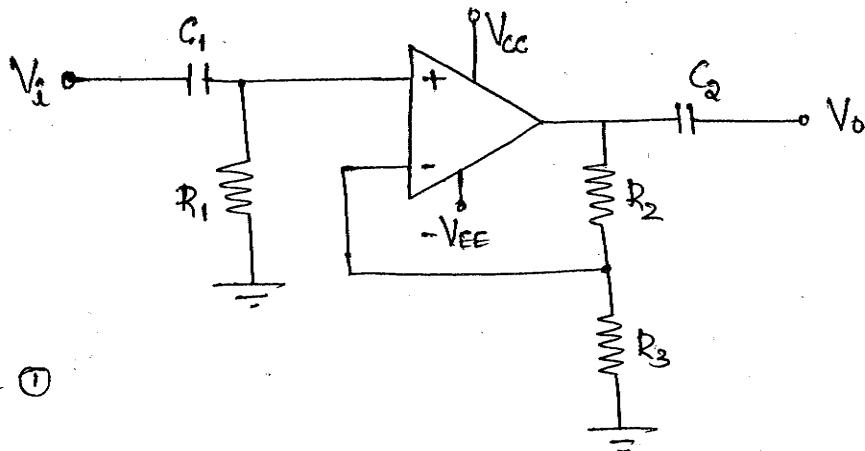


fig ①

Sol :-

i) $A_V = 1 + \frac{R_2}{R_3} = 1 + \frac{150\text{ k}\Omega}{1.5\text{ k}\Omega} =$

ii) $Z_{in} = R_1 = 33\text{ k}\Omega$

iii) WKT $C_2 = \frac{1}{2\pi f_1 R_L}$

$$f_1 = \frac{1}{2\pi R_L C_2} = \frac{1}{2\pi \times 4.7\text{ k}\Omega \times 0.27\mu\text{F}}$$

$f_1 = 125.41\text{ Hz}$



High Zin capacitor - coupled Non-INV amplifier :-

1) With a neat ckt diagram, explain the operation of a high IIP Impedance capacitor coupled Non-INV amplifier. Develop the expression for IIP Impedance of the ckt.

June - 08, 8m (EE)

June - 07, 8m (EE)

June - 10, 8M (EE)

Jan - 06, 6m (EE)

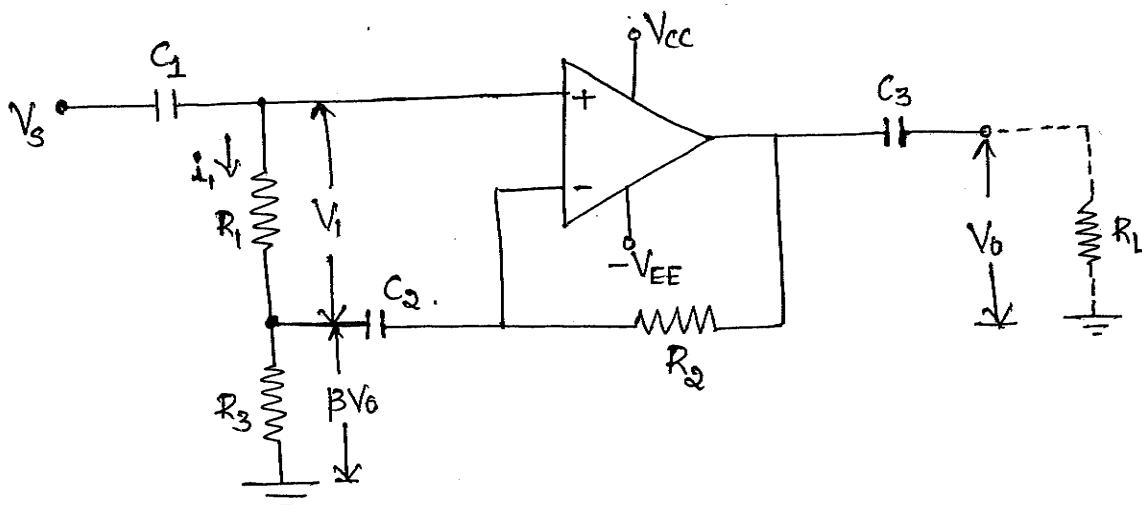


fig ① : High IIP Impedance capacitor - coupled Non-INV amplifier.

- * The - IIP Impedance of Non-INV amplifier can be improved by using capacitor C_2 . The voltage is fed back from the o/p to the - IIP via R_2 , C_2 and R_3 .
- ∴ The feedback factor 'B' is given by

$$B = \frac{R_3}{R_2 + R_3}$$

Applying KVL from V_s , R_1 & R_3 , we get :-

$$V_s - V_i - B V_o = 0$$



$$V_1 = V_s - \beta V_o \rightarrow ①$$

WKT

$$M = \frac{V_o}{V_1}$$

FIB factor

$$\beta = \frac{V_{R3}}{V_o}$$

$$V_{R3} = \beta V_o.$$

$$V_o = M V_1 \rightarrow ②$$

Sub. eq ⑤ in eq ①, we get

$$V_1 = V_s - \beta M V_1$$

$$V_1 + \beta M V_1 = V_s$$

$$V_1 [1 + \beta M] = V_s$$

$$V_1 = \frac{V_s}{(1 + \beta M)} \rightarrow ③$$

* The current $i_1 = \frac{V_1}{R_1}$

$$i_1 = \frac{V_s}{(1 + \beta M) R_1} \rightarrow ④$$

* IIP Impedance is given by:

$$Z_{in} = \frac{V_s}{i_1} \rightarrow ⑤$$

Sub eq ④ in eq ⑤ we get

$$Z_{in} = \frac{V_s}{\frac{V_s}{(1 + \beta M) R_1}}$$

$$\therefore Z_{in} = (1 + \beta M) R_1$$



Design steps :-

1) $R_1 + R_3 = R_1(\text{max})$.

$$R_1 + R_3 = R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

2) $R_1 + R_3 = R_2$

3) $R_1 \approx R_2$

4) $A_V = 1 + \frac{R_2}{R_3} \quad \therefore R_3 = \frac{R_2}{A_V - 1}$

5) $R_1 + R_3 = R_1(\text{max})$

$$R_1 = R_1(\text{max}) - R_3$$

6) $X_{C2} = \frac{R_2}{10} \text{ at } f_1$

$$C_2 = \frac{1}{2\pi f_1 R_3}$$

7) choose $C_1 = 1000 \text{ pF}$ (to be much larger than stray capacitance)

8) $X_{C3} = R_L \text{ at } f_1$

$$C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10} \right)}$$

9) I/P Impedance. $Z_{in} = (1 + M\beta) R_1$



High Z_{in} capacitor coupled Non-INV amplifier :-

Design steps for LF 353 BIFET op-amp:

1) For a BIFET OP-AMP

Select : $R_2 = 1M\Omega$

2) W.R.T. $A_V = \frac{V_o}{V_i}$

$$A_V = \frac{R_2 + R_3}{R_3}$$

$$A_V = 1 + \frac{R_2}{R_3}$$

3) W.R.T $A_V = 1 + \frac{R_2}{R_3}$

$$\frac{R_2}{R_3} = A_V - 1$$

$$R_3 = \frac{R_2}{A_V - 1}$$

4) $R_1 = R_2 - R_3$

5) $X_{C2} = R_3 \text{ at } f_1 , C_2 = \frac{1}{2\pi f_1 R_3}$

6) $X_{C3} = \frac{R_L}{10} \text{ at } f_1 , C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10} \right)}$

7) Select $C_1 = 1000 \text{ pF}$ (To be much larger than stray capacitance).



PROBLEMS

1). Design a high zlp impedance capacitor-coupled Non-INV amplifier using T41 op-amp to have a gain of $A_V = 140$ and $f_l = 120 \text{ Hz}$. The zlp signal is 40mV and the load resistance varies from $1.8 \text{ k}\Omega$ to $20 \text{ k}\Omega$. Assume $I_{B(\max)} = 500 \text{ nA}$.

Given :-

$$A_V = 140, f_l = 120 \text{ Hz}, R_L = 1.8 \text{ k}\Omega \text{ to } 20 \text{ k}\Omega,$$

$$I_{B(\max)} = 500 \text{ nA}, V_z = 40 \text{ mV}.$$

Sol: -

$$* R_1 + R_3 = R_1(\max) = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7V}{500 \text{ nA}} = \underline{140 \text{ k}\Omega}$$

choose \$R_1(\max) = 150 \text{ k}\Omega\$

$$* R_1 + R_3 \approx R_2 = R_1(\max) = 150 \text{ k}\Omega$$

$$* R_3 = \frac{R_2}{A_V - 1} = \frac{150 \text{ k}\Omega}{140 - 1} = \underline{1.08 \text{ k}\Omega}$$

choose \$R_3 = 1 \text{ k}\Omega\$

$$* \text{WKT} \quad R_1 + R_3 = R_1(\max)$$

$$R_1 = R_1(\max) - R_3$$

$$= 150 \text{ k}\Omega - 1 \text{ k}\Omega$$

$$R_1 = 149 \text{ k}\Omega$$

choose \$R_1 = 150 \text{ k}\Omega\$



* $R_1 \approx R_2 = 150 \text{ k}\Omega$

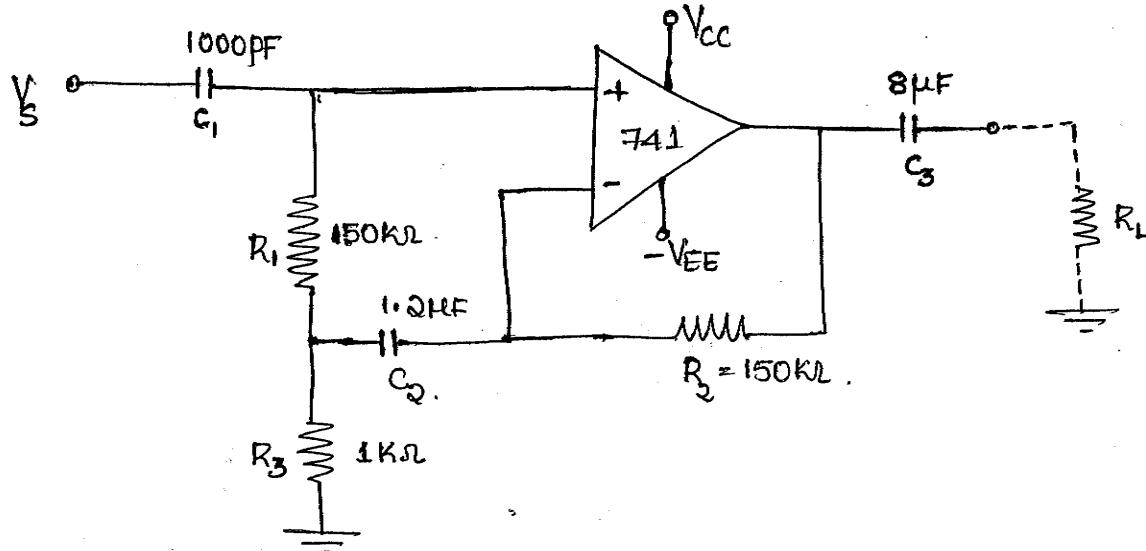
* $C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi \times 120 \times 1\text{ k}\Omega} = 1.33 \mu\text{F}$

choose. $C_2 = 1.2 \mu\text{F}$

* $C_1 = 1000 \text{ pF}$

* $C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)} = \frac{1}{2\pi \times 120 \times \left(\frac{1.8 \times 10^3}{10}\right)} = 7.36 \mu\text{F}$

choose. $C_3 = 8 \mu\text{F}$



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BIFET — LF 353 OP-amp.

1) Using a LF 353 BIFET op-amp, design a high Z_{in} capacitor-coupled Non-INV amplifier to have a low cut-off frequency of 200 Hz. The I/p & O/P voltages are to be 15 mV and 3V respectively, and the minimum load resistance is $12\text{ k}\Omega$.

Given :- $f_l = 200\text{ Hz}$, $V_i = 15\text{ mV}$, $V_o = 3\text{ V}$, $R_L = 12\text{ k}\Omega$

Sol :- $A_V = \frac{V_o}{V_i} = \frac{3\text{ V}}{15\text{ mV}} = 200$

* For BIFET op-amp, select $R_2 = 1\text{ M}\Omega$

* $R_3 = \frac{R_2}{A_V - 1} = \frac{1\text{ M}\Omega}{200 - 1} = 5\text{ k}\Omega$. choose $R_3 = 4.7\text{ k}\Omega$

* $R_1 = R_2 - R_3 = 1\text{ M}\Omega - 4.7\text{ k}\Omega = 995.3\text{ k}\Omega$, choose $R_1 = 1\text{ M}\Omega$

* $C_2 = \frac{1}{2\pi f_l R_3} = \frac{1}{2\pi \times 200 \times 4.7\text{ k}\Omega} = 0.17\text{ nF}$

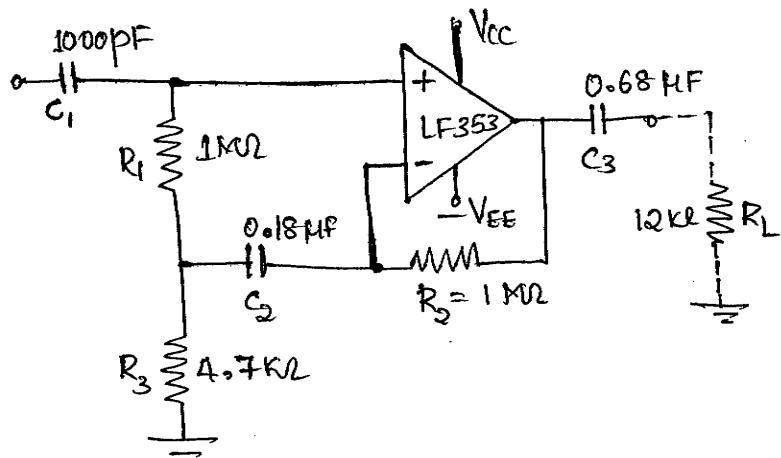
choose $C_2 = 0.18\text{ }\mu\text{F}$

* choose $C_1 = 1000\text{ pF}$

* $C_3 = \frac{1}{2\pi f_l \left(\frac{R_L}{10} \right)}$
 $= \frac{1}{2\pi \times 200 \times \left(\frac{12\text{ k}\Omega}{10} \right)}$
 $= 0.66\text{ nF}$

choose

$C_3 = 0.68\text{ }\mu\text{F}$



Q) A capacitor coupled Non-INV amplifier is to be designed to have high Z_{LP} Impedance with a gain of 40dB. If the open loop gain of op-amp is 2×10^5 and Z_{LP} Impedance $1.5 \times 10^6 \Omega$, calculate the various ckt elements. The required cut-off frequency is 100Hz. The load resistance is $2.2 \text{ k}\Omega$ and Z_{LP} parasitic capacitance 15 pF . Also calculate the Z_{LP} impedance.

Jan -09, 8M

Given :-

$$A_V = 40 \text{ dB}, M = 2 \times 10^5, R_L = 2.2 \text{ k}\Omega$$

$$Z_L = 1.5 \times 10^6 \Omega, f_c = 100 \text{ Hz}, C_{ld} = 15 \text{ pF}$$

For op-amp 741 : I_{B(max)} = 500nA

Sol:- Gain is given in dB. Convert it to normal gain.

$$(A_V)_{\text{dB}} = 20 \log_{10} (A_V)$$

$$A_V = \log_{10}^{-1} \left(\frac{A_V(\text{dB})}{20} \right)$$

$$A_V = 100$$

* $R_1 + R_3 = R_2$ &

$$R_1 + R_3 = R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7V}{500 \text{ nA}}$$

$$R_1(\text{max}) = 140 \text{ k}\Omega$$

choose $R_1(\text{max}) = 150 \text{ k}\Omega$

* $R_1 + R_3 \approx R_2 = R_1(\text{max}) = 150 \text{ k}\Omega \therefore R_2 = 150 \text{ k}\Omega$

* $R_3 = \frac{R_2}{A_V - 1} = \frac{150 \text{ k}\Omega}{100 - 1} = 1.5 \text{ k}\Omega$

$$R_3 = 1.5 \text{ k}\Omega$$



* WKT $R_1 + R_3 = R_1(\text{max})$

$$R_1 = R_1(\text{max}) - R_3 = 150 \text{ k}\Omega - 1.5 \text{ k}\Omega.$$

$$R_1 = 148.5 \text{ k}\Omega$$

choose

$$R_1 = 150 \text{ k}\Omega$$

* i.e.

$$R_1 \approx R_2 = 150 \text{ k}\Omega$$

$$* C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi \times 100 \times 1.5 \text{ k}\Omega} = 1.06 \mu\text{F}; \text{ choose } C_2 = 1 \mu\text{F}$$

$$* C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10} \right)} = \frac{1}{2\pi \times 100 \times \left(\frac{0.2 \text{ k}\Omega}{10} \right)} = 7.2 \mu\text{F}; \text{ choose } C_3 = 6.8 \mu\text{F}$$

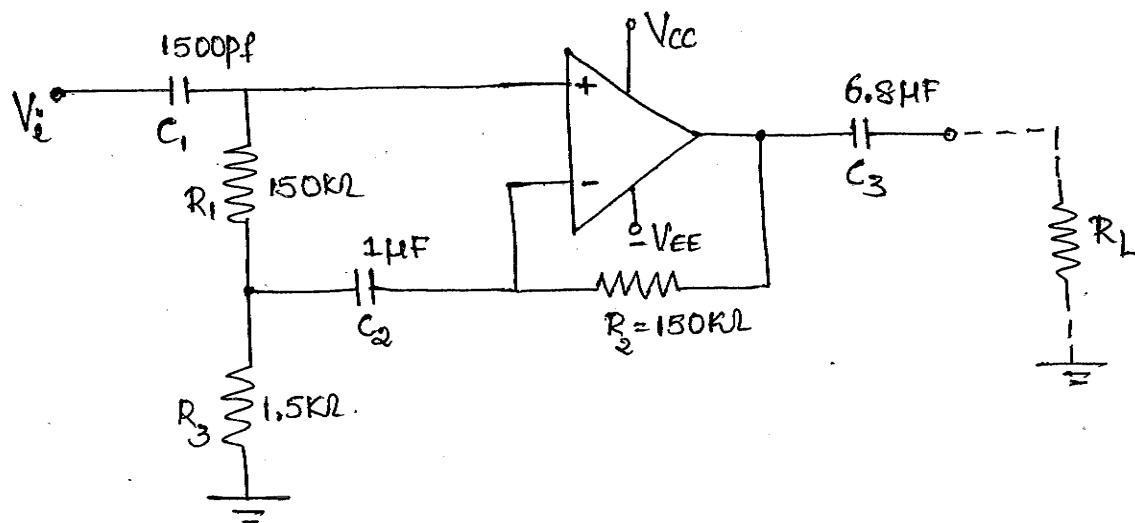
$$* C_1 \gg C_{ld}, \text{ let } C_1 = 100 \times C_{ld} = 100 \times 15 \text{ pF}, C_1 = 1500 \text{ pF}$$

$$* \beta = \frac{R_3}{R_2 + R_3}$$

$$\beta = \frac{1.5 \text{ k}\Omega}{150 \text{ k}\Omega + 1.5 \text{ k}\Omega} = 0.09 \rightarrow \beta \approx 0.01$$

$$* Z_{in} = (1 + M_B) Z_i = (1 + 2 \times 10^5 \times 0.01) 1.5 \times 10^6 \Omega$$

$$Z_{in} = 3 \times 10^9 \Omega$$



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3) A high IIP Impedance capacitor coupled Non-INV amplifier is to be designed to have $A_V = 120$ and $f_L = 100\text{Hz}$. The IIP signal is 50mV & the load resistance ranges from $2.7\text{k}\Omega$ to $27\text{k}\Omega$. Design a suitable ckt using a 741 op-amp.

[Jan-08, 8M(EE)]

Given :- $A_V = 120$, $f_L = 100\text{Hz}$, $V_i = 50\text{mV}$,

$R_L = 2.7\text{k}\Omega$ to $27\text{k}\Omega$ i.e Take $\boxed{R_L = 2.7\text{k}\Omega}$

For op-amp 741: $I_B(\text{max}) = 500\text{nA}$

Sol :-

$$* R_{1(\text{max})} = \frac{0.1 V_{BE}}{I_{B(\text{max})}} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}} = 140\text{k}\Omega$$

choose $\boxed{R_{1(\text{max})} = 150\text{k}\Omega}$

$$* (R_1 + R_3) \parallel R_2 = R_{1(\text{max})} = 150\text{k}\Omega \quad \therefore \boxed{R_2 = 150\text{k}\Omega}$$

$$* R_3 = \frac{R_2}{A_V - 1} = \frac{150\text{k}\Omega}{120 - 1} = 1.26\text{k}\Omega$$

choose $\boxed{R_3 = 1.2\text{k}\Omega}$

$$* \text{WKT } R_1 + R_3 = R_{1(\text{max})}$$

$$R_1 = R_{1(\text{max})} - R_3 = 150\text{k}\Omega - 1.2\text{k}\Omega$$

$\boxed{R_1 = 148.8\text{k}\Omega}$

choose

$\boxed{R_1 = 150\text{k}\Omega}$

i.e

$\boxed{R_1 \approx R_2}$

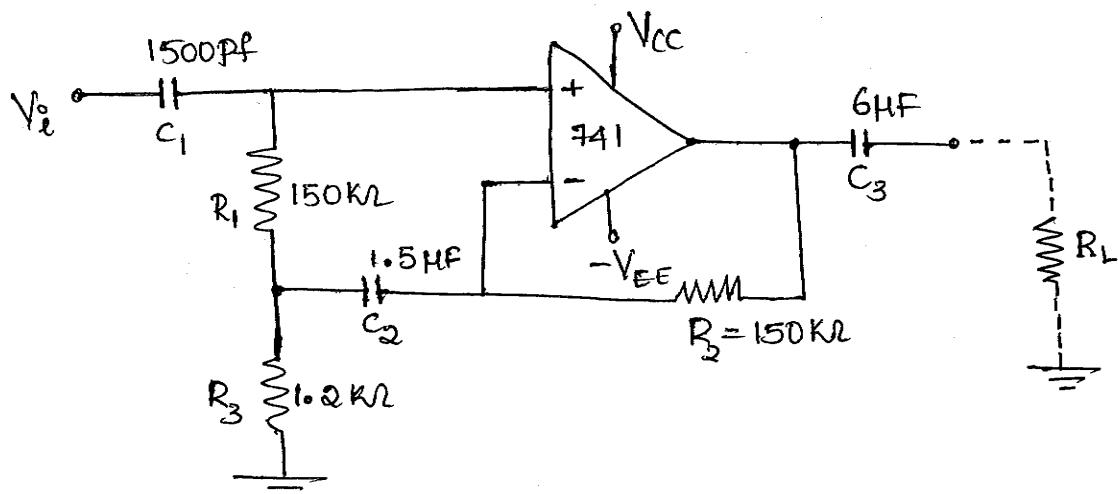
$$* C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi \times 100 \times 1.2\text{k}\Omega} = \underline{\underline{1.32\text{HF}}}$$

choose

$\boxed{C_2 = 1.5\mu\text{F}}$



* Select $C_1 = 1500 \text{ pF}$



- 4) Using a 741 op-amp, design a high Z_{in} Non-INV amplifier to operate with a +36V power supply. The load resistance is $12 \text{ k}\Omega$. The lower cut-off frequency is to be 150Hz & the voltage gain is to be 7.

Given :- $R_L = 12 \text{ k}\Omega$, $f_l = 150 \text{ Hz}$, $A_v = 7$.

For op-amp 741 : $I_B(\text{max}) = 500 \text{ nA}$

SOL :-

$$* R_1(\text{max}) = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7 \text{ V}}{500 \text{ nA}} = 140 \text{ k}\Omega$$

Choose

$$R_1(\text{max}) = 150 \text{ k}\Omega$$

$$* R_1 + R_3 \approx R_2 = R_1(\text{max}) = 150 \text{ k}\Omega$$

$$R_2 = 150 \text{ k}\Omega$$



$$\text{* } R_3 = \frac{R_2}{A_V - 1}$$

$$= \frac{150\text{ k}\Omega}{7-1} = 25\text{ k}\Omega, \text{ choose } R_3 = 27\text{ k}\Omega$$

$$\text{* WKT } R_1 + R_3 = R_{i(\max)}$$

$$R_1 = R_{i(\max)} - R_3 = 150\text{ k}\Omega - 27\text{ k}\Omega$$

$$R_1 = 123\text{ k}\Omega \quad \text{choose } R_1 = 120\text{ k}\Omega$$

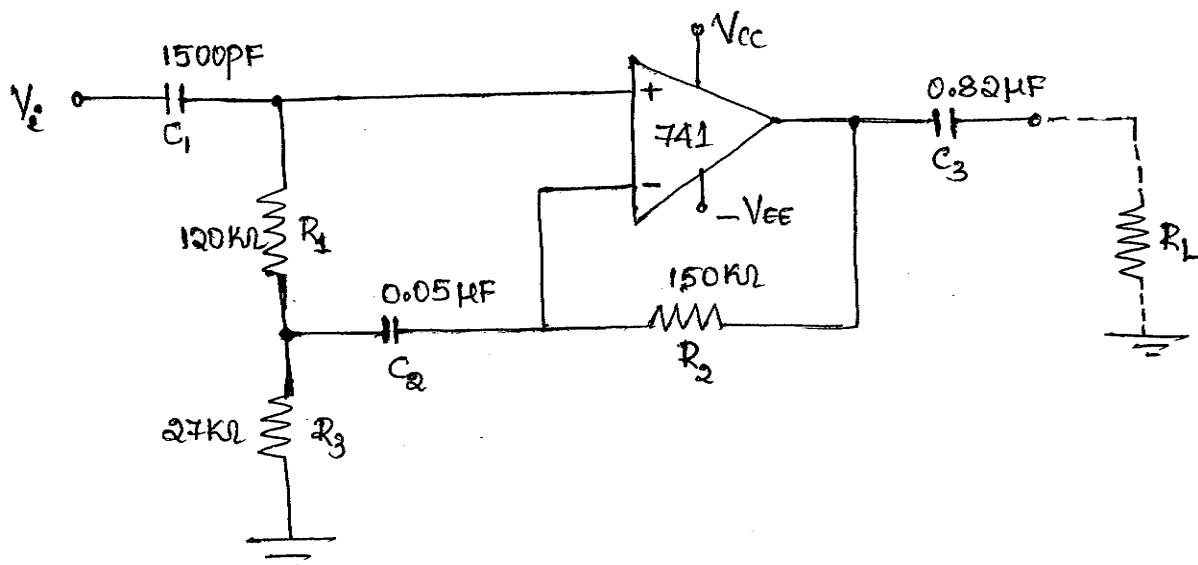
$$\text{* } C_2 = \frac{1}{2\pi f_i R_3} = \frac{1}{2\pi \times 150 \times 27\text{ k}\Omega} = 0.039\text{ }\mu\text{F}$$

$$\text{choose, } C_2 = 0.05\text{ }\mu\text{F}$$

$$\text{* } C_3 = \frac{1}{2\pi f_i \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 150 \times \left(\frac{12\text{ k}\Omega}{10} \right)} = 0.884\text{ }\mu\text{F}$$

$$\text{choose, } C_3 = 0.82\text{ }\mu\text{F}$$

$$\text{* Choose } C_1 = 1500\text{ pF}$$





ARUNKUMAR G M.Tech, *Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.*

Capacitor - Coupled INVERTING Amplifier :-

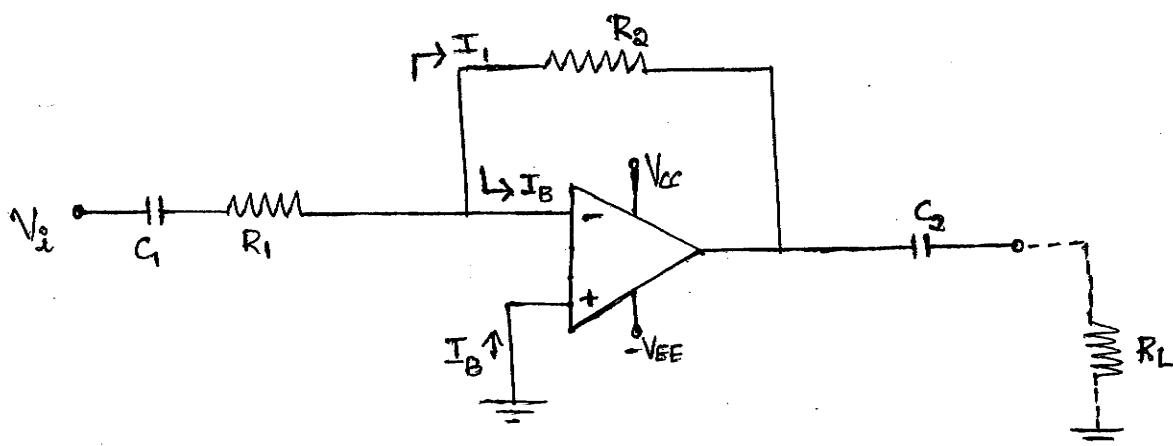


Fig ① : Capacitor - coupled INV - amplifier.

- * In capacitor coupled INV amplifier, the bias current to the op-amp. INV terminal flows via R_2 , so coupling capacitor C_1 does not interrupt the IIP bias current.
- * No resistor is included in series with the NON-INV IIP terminal because of a small dc offset is unimportant with a capacitor coupled op.
- * The IIP impedance $Z_{in} = R_1$

Design steps :-

1) Let $I_I = 100 \times I_B(\text{max})$.

$$2) R_1 = \frac{V_i}{I_I}$$

$$3) R_2 = \frac{V_o}{I_I}$$

$$4) X_{C1} = \frac{R_1}{10} \text{ at } f_1$$

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$5) X_{C2} = R_L \text{ at } f_1$$

$$C_2 = \frac{1}{2\pi f_1 R_L}$$



PROBLEMS.

1) A capacitor - coupled INV amplifier has the following components : $R_1 = 2.7\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$, $R_L = 1.5\text{ k}\Omega$, $C_1 = 3.9\text{ }\mu\text{F}$, $C_2 = 0.68\text{ }\mu\text{F}$. Determine the ckt voltage gain, lower cut-off frequency and impedance of C_1 at f_1 . Draw the ckt & insert the given values.

June - 08, 6M(EE)

Given :- $R_1 = 2.7\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$, $R_L = 1.5\text{ k}\Omega$, $C_1 = 3.9\text{ }\mu\text{F}$, $C_2 = 0.68\text{ }\mu\text{F}$.

SOL :- * Voltage gain :

$$A_V = -\frac{R_2}{R_1} = -\frac{100\text{ k}\Omega}{2.7\text{ k}\Omega} = -37$$

$$|A_V| = 37$$

* $C_2 = \frac{1}{2\pi f_1 R_L}$

$$f_1 = \frac{1}{2\pi R_L C_2} = \frac{1}{2\pi \times 1.5\text{ k}\Omega \times 0.68\text{ }\mu\text{F}}$$

$$f_1 = 156.03\text{ Hz}$$

$$X_{C1} = \frac{1}{2\pi f_1 C_1} = \frac{1}{2\pi \times 156.03 \times 3.9\text{ }\mu\text{F}}$$

$$X_{C1} = 261.54\text{ }\Omega$$

NOTE :-

IIP Impedance .

$$Z_{in} = R_1 = 2.7\text{ k}\Omega$$



Q) A capacitor coupled INV amplifier use the following components : $R_1 = 3.9\text{ k}\Omega$, $R_2 = 120\text{ k}\Omega$, $R_L = 0.2\text{ k}\Omega$, $C_1 = 4.7\text{ }\mu\text{F}$, $C_2 = 0.82\text{ }\mu\text{F}$. Find the

- i) ckt voltage gain (ii) I/P Impedance
- iii) lower cut-off freq. f_1 (iv) Impedance of C_1 at f_1 .

Sol :-

$$\text{i)} |A_{v1}| = \frac{R_2}{R_1} = \frac{120\text{ k}\Omega}{3.9\text{ k}\Omega}$$

$$|A_{v1}| = 30.77$$

$$\text{ii)} Z_{in} = R_1 = 3.9\text{ k}\Omega$$

$$\text{iii)} f_1 = \frac{1}{2\pi C_1 \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 4.7\text{ }\mu\text{F} \times \left(\frac{3.9\text{ k}\Omega}{10} \right)}$$

$$f_1 = 86\text{ Hz}$$

$$\text{iv)} X_{C1} = \frac{1}{2\pi f_1 C_1} = \frac{1}{2\pi \times 86 \times 4.7\text{ }\mu\text{F}}$$

$$X_{C1} = 393.75\Omega$$

Design for BIFET op-amp :-

1) Select $R_2 = 1\text{ M}\Omega$ for BIFET op-amp.

2) WKT $|A_{v1}| = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{|A_{v1}|}$$

$$3) C_1 = \frac{1}{2\pi f_1 (R_1/10)}$$

$$4) C_2 = \frac{1}{2\pi f_1 R_L}$$



1) A capacitor coupled INV amplifier is to be designed using BIFET op-amp, having gain $A_v = -180$ & lower dB frequency $f_l = 75\text{ Hz}$. The IIP signal available is 40 mV & the load resistance $R_L = 1.8\text{ k}\Omega$. Design the circuit.

Given :- $|A_v| \approx 180$, $f_l = 75\text{ Hz}$, $R_L = 1.8\text{ k}\Omega$, $V_i = 40\text{ mV}$

Sol :- for BIFET op-amp.

* choose $R_2 = 1\text{ M}\Omega$

* $|A_v| = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{|A_v|} = \frac{1\text{ M}\Omega}{180} = 5.55\text{ k}\Omega,$$

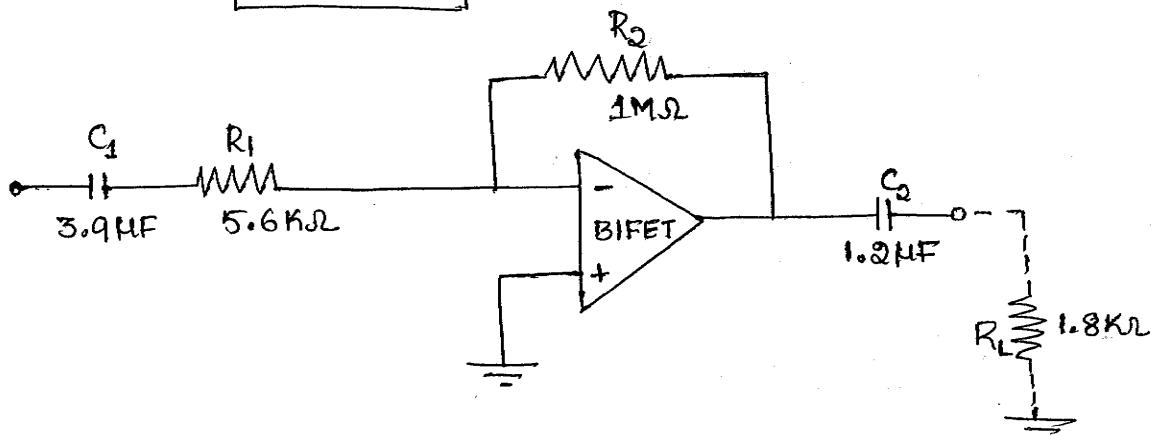
choose $R_1 = 5.6\text{ k}\Omega$

* $C_1 = \frac{1}{2\pi f_l \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 75 \times \left(\frac{5.6\text{ k}\Omega}{10} \right)} = 3.99\text{ nF}$

choose $C_1 = 3.9\text{ nF}$

* $C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 75 \times (1.8 \times 10^3)} = 1.18\text{ nF}$

choose $C_2 = 1.2\text{ nF}$



- * Design capacitor coupled INV amplifier using op-amp 741 to have voltage gain of 100. Assume signal voltage of 10mV and load of $4.7\text{ k}\Omega$.

Given: $A_V = 100$, $V_i = 10\text{ mV}$, $R_L = 4.7\text{ k}\Omega$

Sol :- For op-amp 741 : $I_{OC(\max)} = 500\text{nA}$

* Let $I_I = 100 \times I_{OC(\max)} = 100 \times 500\text{nA}$

$$I_I = 50\mu\text{A}$$

* $R_1 = \frac{V_i}{I_I} = \frac{10\text{ mV}}{50\mu\text{A}} = 200\Omega$

NKT $A_V = \frac{R_2}{R_1}$

$$R_2 = A_V R_1 = 100 \times 200\Omega$$

$$R_2 = 20\text{k}\Omega$$

* $C_1 = \frac{1}{2\pi f_l \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 120 \times \left(\frac{200}{10} \right)} = 66.31\text{ HF}$

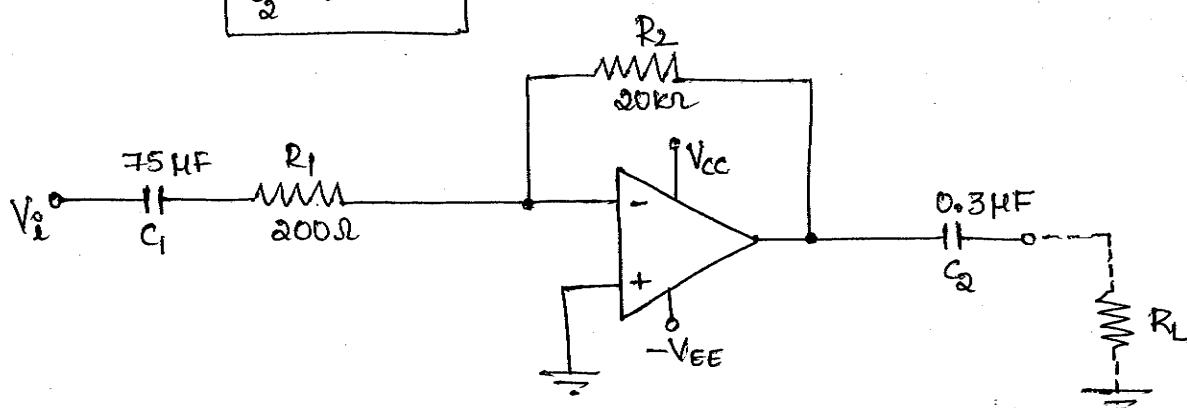
choose

$$C_1 = 75\text{ HF}$$

* $C_2 = \frac{1}{2\pi f_l R_L} = \frac{1}{2\pi \times 120 \times 4.7 \times 10^3} = 0.2821\text{ HF}$

choose.

$$C_2 = 0.3\text{ HF}$$



Setting the upper cut-off frequency :-

- * Briefly discuss the upper cut-off frequency of an op-amp ckt. show how the cut-off frequency can be set for inverting and Non-INV amplifiers.

Jan-08, 8m(EE)

June-09, 6M

- * How upper cut-off frequency is decided in an op-amp & when is it necessary?

Jan-09, 6M

- * Explain how the upper cut-off frequency can be set for inverting & Non-INV amplifiers.

June-10, 6M

- * Briefly discuss the upper cut-off frequency of an op-amp ckt & show how the cut-off frequency can be set for INV amplifier.

Jan-10, 6M(EE)

 \Rightarrow

- * The highest signal frequency that can be processed by an op-amp ckt depends on the op-amp selected (for eg 741, LF353 etc).

are

for example : If very low frequency signals to be amplified, as there would be interference from high frequency noise voltages, since these also get amplified.

- * If these high frequency noise voltages are to be eliminated, there must be a provision for their effective attenuation.

This can be achieved by setting the upper cut-off frequency just above the highest desired signal frequency.



This is done by connecting a feedback capacitor C_f from the op-amp output to its INV terminal as shown in fig ④ & ⑤ below.

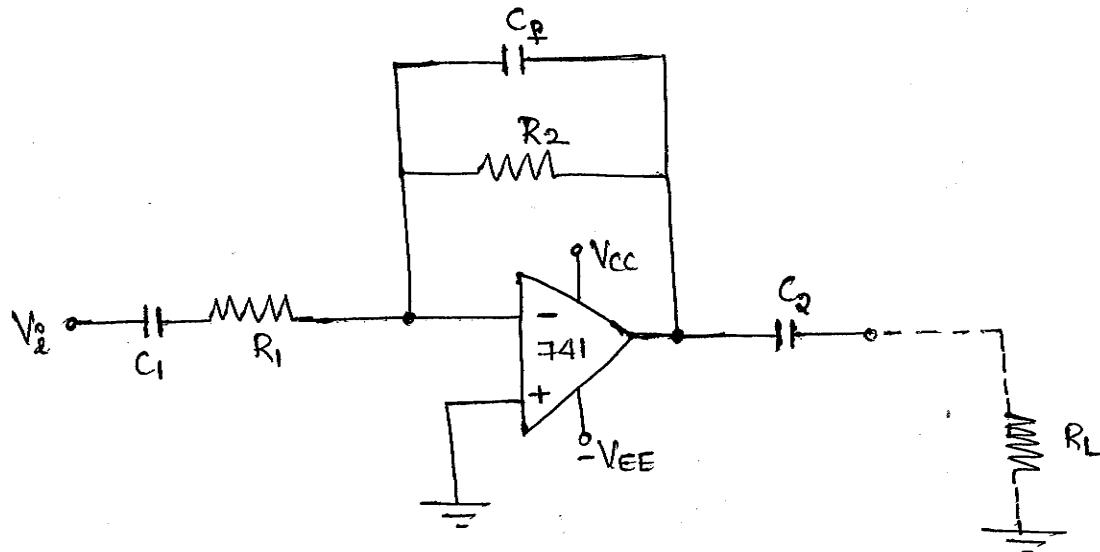


fig ④ : INV amplifier with feedback capacitor C_f to set the upper cut-off frequency.

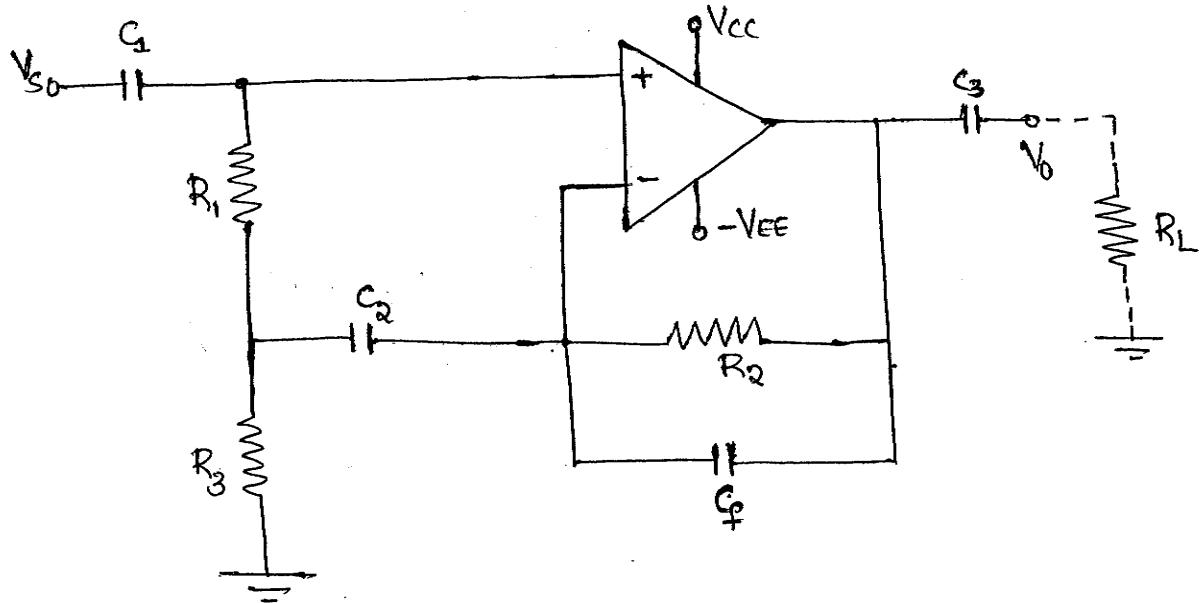


fig ⑤ : Non-INV amplifier with feedback capacitor C_f to set the upper cut-off frequency.



* For INV amplifier, the voltage gain is.

$$A_V = \frac{R_2 \parallel X_{Cf}}{R_1}$$

$$\left\{ \left(A_V = \frac{R_2}{R_1} \right) \right.$$

$$A_V = \frac{R_2 \cdot X_{Cf}}{R_1 (R_2 + X_{Cf})} \curvearrowright$$

In fig @ C_f is in parallel with R_2
So again becomes.

$$A_V = \frac{1}{R_1 \left[\frac{R_2}{R_2 X_{Cf}} + \frac{X_{Cf}}{R_2 X_{Cf}} \right]}$$

$$\left(\frac{R_2 \parallel X_{Cf}}{R_1} \right)$$

$$A_V = \frac{1}{R_1 \left[\frac{1}{X_{Cf}} + \frac{1}{R_2} \right]}$$

Magnitude of A_V i.e.

$$A_V = \frac{1}{R_1 \sqrt{\left(\frac{1}{X_{Cf}}\right)^2 + \left(\frac{1}{R_2}\right)^2}}$$

When $X_{Cf} = R_2$

$$A_V = \frac{1}{R_1 \sqrt{\left(\frac{1}{R_2}\right)^2 + \left(\frac{1}{R_2}\right)^2}}$$

$$= \frac{1}{R_1 \sqrt{2 \left(\frac{1}{R_2}\right)^2}}$$

$$= \frac{1}{\frac{R_1}{R_2} \sqrt{2}}$$

$$A_V = \frac{1}{\sqrt{2}} \left(\frac{R_2}{R_1} \right) \rightarrow ①$$



The equation ① indicates that the gain is 3dB down the normal voltage gain.

Thus upper cut-off frequency f_2 (or f_H) for the cct can be set to the desired frequency f_2 by making,

$$\boxed{X_{CP} = R_2} \quad \text{at } f_2.$$

{ ∵ Normal Vtg.
gain is

$$A_V = \frac{R_2}{R_1}$$

This analysis is applicable to Non-INV amplifier also (fig ⑥).

Capacitor coupled INV amplifier

Design steps :-

1) $I_I = 100 \times I_B(\text{max})$

2) $R_I = \frac{V_i}{I_I}$

3) $A_V = \frac{R_2}{R_I}$

$$\boxed{R_2 = A_V R_I}$$

4) $C_1 = \frac{1}{2\pi f_L (R_I/10)}$ Where $f_L = f_1$ = lower freq.

5) $C_2 = \frac{1}{2\pi f_H (R_L)}$ Where $f_H = f_2$ = Higher frequency.



PROBLEMS

1) The INV - amplifier is to be capacitor - coupled and to have a signal frequency range of 10Hz to 1KHz. If the load resistance is 250Ω , calculate the required capacitor value. The voltage gain is to be 50 & the o/p v_o amplitude is to be 0.5V.

Given - $f_1 = 10\text{Hz}$, $f_2 = 1\text{KHz}$, $R_L = 250\Omega$, $A_v = 50$ & $V_o = 0.5\text{V}$.

SOL :-

For op-amp 741 : $I_{B(\max)} = 500\text{nA}$

$$* I_i = 100 \times I_{B(\max)} = 100 \times 500\text{nA} , \boxed{I_i = 50\text{nA}}$$

$$* A_v = \frac{V_o}{V_i} \Rightarrow V_i = \frac{V_o}{A_v} = \frac{0.5\text{V}}{50} , \boxed{V_i = 50\text{mV}}$$

$$* R_i = \frac{V_i}{I_i} = \frac{50\text{mV}}{50\text{nA}} , \boxed{R_i = 1\text{k}\Omega}$$

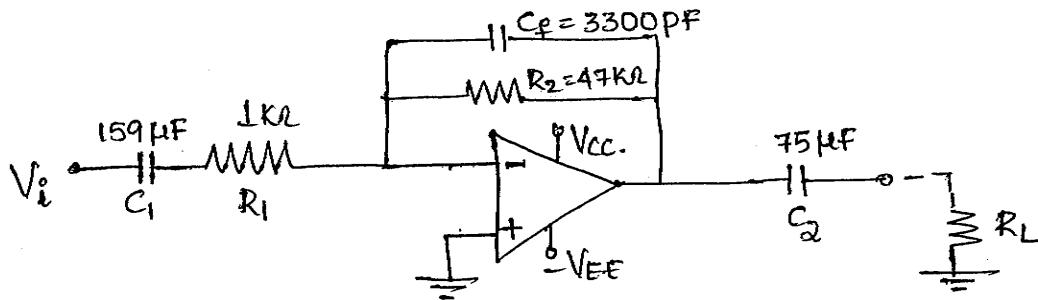
$$* \text{WKT } A_v = \frac{R_2}{R_1} \Rightarrow R_2 = A_v R_1 = 50 \times 1\text{k}\Omega = \boxed{50\text{k}\Omega}$$

choose, $\boxed{R_2 = 47\text{k}\Omega}$

$$* C_1 = \frac{1}{2\pi f_1 (R_1/10)} = \frac{1}{2\pi \times 10 \times (1\text{k}\Omega/10)} = \boxed{159\text{nF}}$$

$$* C_2 = \frac{1}{2\pi f_2 R_L} = \frac{1}{2\pi \times 10 \times 250\Omega} = \boxed{64\text{nF}}, \text{ choose } \boxed{C_2 = 75\text{nF}}$$

$$* C_f = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 1\text{kHz} \times 47\text{k}\Omega} = 3386\text{pF}, \text{ choose } \boxed{C_f = 3300\text{pF}}$$



Q) Design a capacitor coupled INV-amp using MA-741 op-amp, with following specifications : voltage gain = 50, o/p voltage amplitude = 0.5V. The frequency range is 40Hz to 2KHz and load resistance = 250Ω.

June - 09, 6M(EE)

Given :- $A_V = 50$, $V_o = 0.5V$, $f_1 = 40\text{Hz}$, $f_2 = 2\text{KHz}$, $R_L = 250\Omega$

Sol :- For op-amp 741 : $I_B(\text{max}) = 500\text{nA}$

* $I_I = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$I_I = 50 \mu\text{A}$

* WKT $A_V = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_V} = \frac{0.5V}{50}$$

$V_i = 50\text{mV}$

* $R_I = \frac{V_i}{I_I} = \frac{50\text{mV}}{50\text{nA}}$

$R_I = 1\text{k}\Omega$

* WKT $A_V = \frac{R_2}{R_1}$

$$R_2 = A_V R_1 = 50 \times 1\text{k}\Omega = 50\text{k}\Omega$$

choose. $R_2 = 47\text{k}\Omega$

* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 40 \times \left(\frac{1\text{k}\Omega}{10} \right)} = 39.78\text{nF}$

choose. $C_1 = 39\text{nF}$



$$* C_2 = \frac{1}{2\pi f_p R_L}$$

$$\approx \frac{1}{2\pi \times 40 \times 250\Omega}$$

$$C_2 = 15.91 \mu F$$

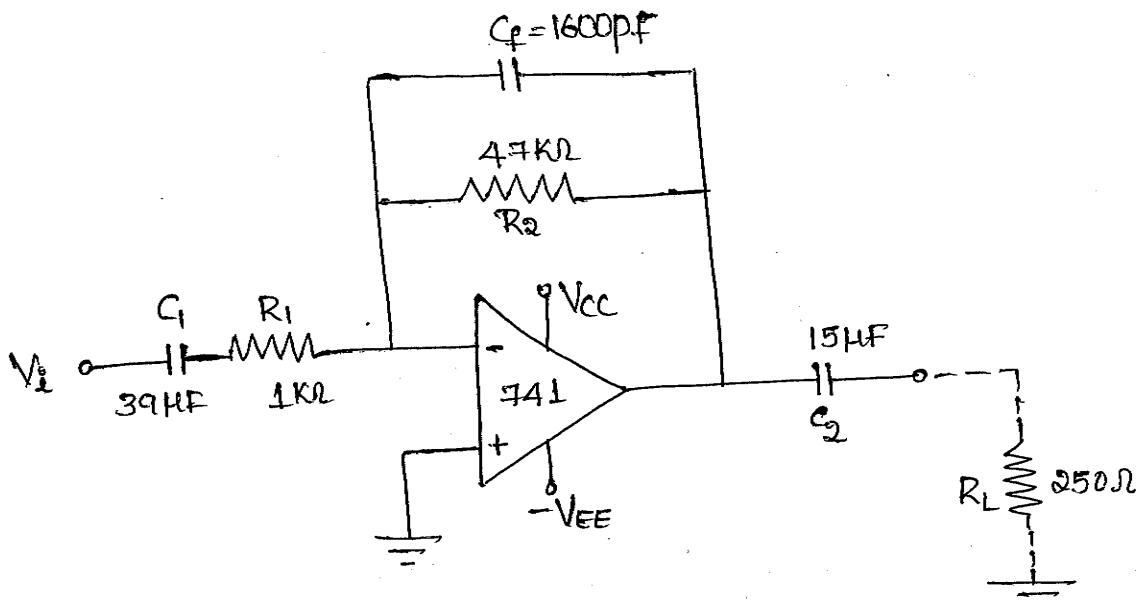
choose $C_2 = 15 \mu F$

$$* C_f = \frac{1}{2\pi f_2 R_2}$$

$$\approx \frac{1}{2\pi \times 2 \text{kHz} \times 47 \text{k}\Omega}$$

$$C_f = 1693.13 \text{ pF}$$

choose $C_f = 1600 \text{ pF}$



3) Design a capacitor coupled INV-amplifier using 741 with a gain of 50 & the o/p amplitude is 2.5 Volts. The signal frequency range is 10Hz to 1KHz. The load resistance is 250Ω .

June - 06, 8M(EE)

Given - $A_V = 50$, $V_o = 2.5V$, $R_L = 250\Omega$
 $f_1 = 10\text{ Hz}$, $f_2 = 1\text{ KHz}$.

Sol: - For 741 op-amp : $I_{B(\max)} = 500\text{nA}$

* Let $I_i = 100 \times I_{B(\max)} = 100 \times 500\text{nA}$

$$I_i = 50\mu\text{A}$$

* WKT $A_V = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_V} = \frac{2.5V}{50}$$

$$V_i = 50\text{mV}$$

* $R_1 = \frac{V_i}{I_i} = \frac{500\text{mV}}{50\mu\text{A}}$

$$R_1 = 1\text{ k}\Omega$$

* WKT $A_V = \frac{R_2}{R_1}$

$$R_2 = A_V R_1 = 50 \times 1\text{k}\Omega$$

$$R_2 = 50\text{k}\Omega$$



$$* C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 10 \times \left(\frac{1k\Omega}{10} \right)} = 159 \text{ HF}$$

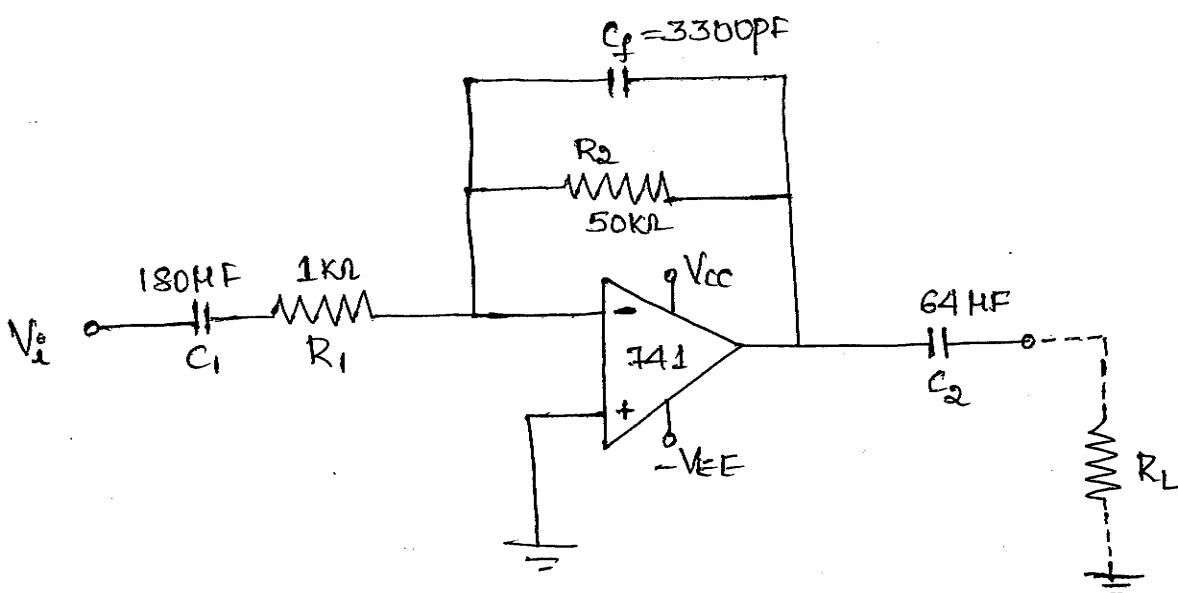
choose $C_1 = 180 \mu\text{F}$

$$* C_2 = \frac{1}{2\pi f_2 R_L} = \frac{1}{2\pi \times 10 \times 250\Omega} = 64 \text{ HF}$$

choose $C_2 = 75 \text{ HF}$

$$* C_f = \frac{1}{2\pi f_3 R_2} = \frac{1}{2\pi \times 1 \times 10^3 \times 50 \text{ k}\Omega} = 3386 \text{ pF}$$

choose $C_f = 3300 \text{ pF}$



A) Design the INV amplifier to operate in a frequency range of 25Hz to 2KHz. The load resistance is 470Ω . The required voltage gain is 100 while signal voltage is 10mV. Use op-amp 741.

Given: $f_1 = 25\text{Hz}$, $f_2 = 2\text{KHz}$, $R_L = 470\Omega$, $A_V = 100$.
 $V_i = 10\text{ mV}$.

Sol:- for op-amp 741, $I_B(\text{max}) = 500\text{nA}$

* Let $I_I = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$I_I = 50\mu\text{A}$$

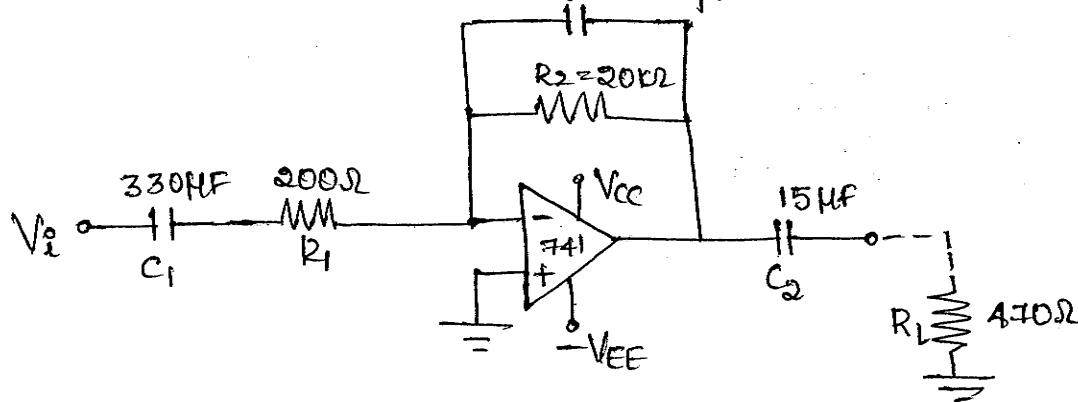
* $R_1 = \frac{V_i}{I_I} = \frac{10\text{mV}}{50\mu\text{A}}$, $R_1 = 200\Omega$

* WKT $R_2 = A_V R_1 = 100 \times 200\Omega = 20\text{k}\Omega$, $R_2 = 20\text{k}\Omega$

* $C_1 = \frac{1}{2\pi f_1 (R_1 / 10)} = \frac{1}{2\pi \times 25 \times (\frac{200}{10})} = 318.309\text{ nF}$
choose, $C_1 = 330\mu\text{F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 25 \times 470} = 13.545\text{ nF}$
choose, $C_2 = 15\mu\text{F}$

* $C_3 = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 2\text{kHz} \times 20\text{k}\Omega} = 3978.87\text{ pF}$
choose, $C_3 = 3900\text{pF}$



ARUNKUMAR G M.Tech, Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.

5) Design a capacitor coupled INV amplifier using a 741 op-amp to have a voltage gain of -75, output voltage amplitude of 3V and a signal frequency range of 20Hz to 12KHz. The load resistance is 470Ω and $I_B(\text{max}) = 500\text{nA}$.

Given :- $A_V = 75$, $V_o = 3V$, $f_1 = 20\text{Hz}$, $f_2 = 12\text{KHz}$, $I_B(\text{max}) = 500\text{nA}$, $R_L = 470\Omega$.

Sol :-

* let $I_i = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$I_i = 50\mu\text{A}$$

* W.R.T $A_V = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_V} = \frac{3V}{75}$$

$$V_i = 40\text{mV}$$

* $R_i = \frac{V_i}{I_i} = \frac{40\text{mV}}{50\mu\text{A}} = 800\Omega$

choose. $R_1 = 820\Omega$

* $R_2 = A_V \times R_1 = 75 \times 820\Omega = 61.5\text{k}\Omega$

choose. $R_2 = 68\text{k}\Omega$



$$* C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 20 \times \left(\frac{820\Omega}{10} \right)} = 97.05 \mu F$$

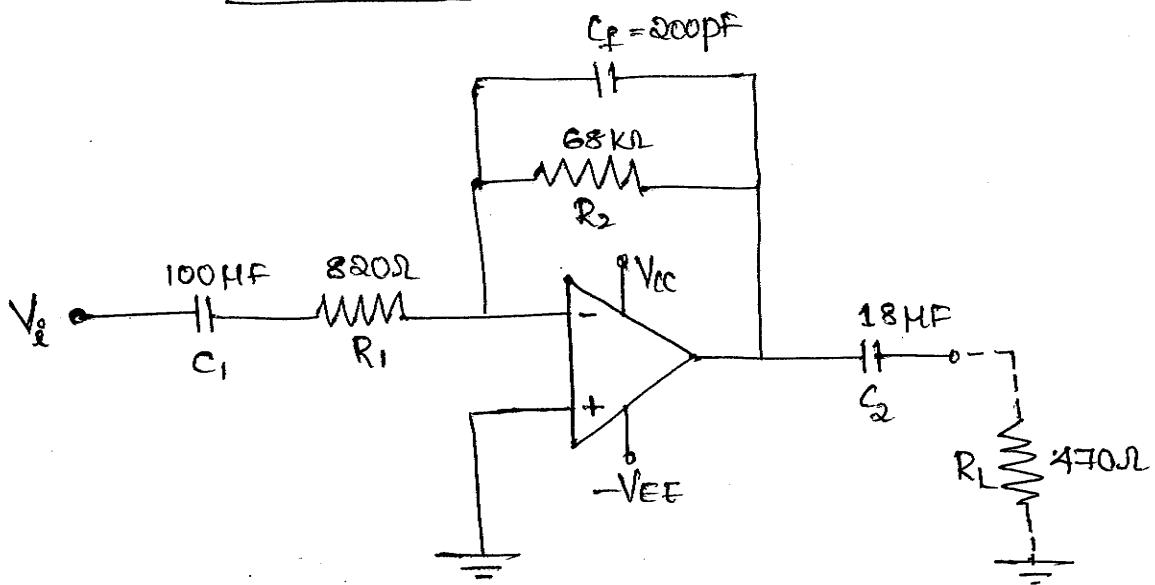
choose $C_1 = 100 \mu F$

$$* C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 20 \times 470\Omega} = 16.93 \mu F$$

choose $C_2 = 18 \mu F$

$$* C_f = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 12 \times 10^3 \times 68 \times 10^3} = 195 \text{ pf}$$

choose $C_f = 200 \text{ pF}$



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ARUNKUMAR G M.Tech, *Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.*

- * Design a C-Coupled INV amplifier for a pass-band gain of 100, $f_1 = 120\text{ Hz}$ & $f_2 = 5\text{ kHz}$. Assume $R_L = 2\text{k}\Omega$ and use the LF353 BIFET op-amp.

Dec - 10, 8M

Given :- $A_V = 100$, $f_1 = 120\text{Hz}$, $f_2 = 5\text{kHz}$, $R_L = 2\text{k}\Omega$

Sol :-

For BIFET op-amp

* Choose $R_2 = 1\text{M}\Omega$ ← (1M)

* WKT $A_V = \frac{R_2}{R_1}$

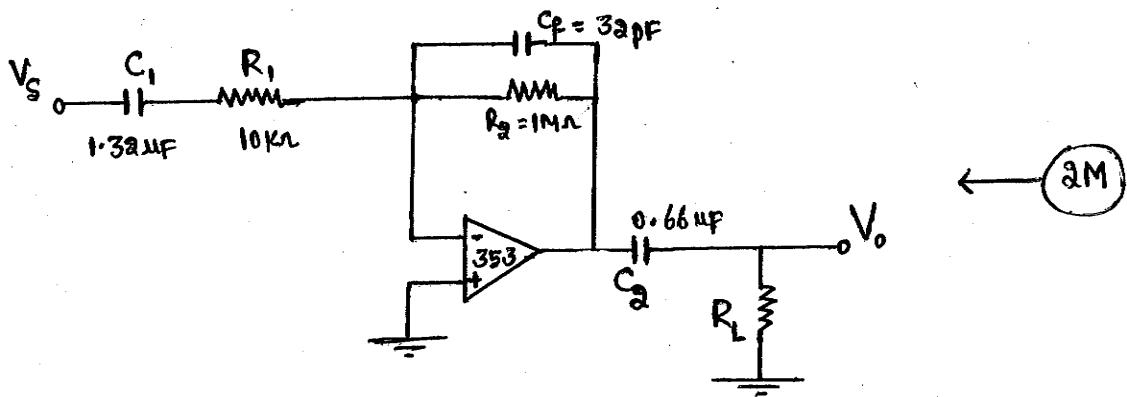
$$R_1 = \frac{R_2}{A_V} = \frac{1\text{M}\Omega}{100}$$

∴ $R_1 = 10\text{k}\Omega$ ← (1M)

* $C_1 = \frac{1}{2\pi f_1 (R_1/10)} = \frac{1}{2\pi \times 120 \times \left(\frac{10\text{k}\Omega}{10}\right)} = 1.32\text{nF} \leftarrow (1M\right)$

* $C_2 = \frac{1}{2\pi f_1 R_2} = \frac{1}{2\pi \times 120 \times 1\text{M}\Omega} = 0.66\text{nF} \leftarrow (1M\right)$

* $C_F = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 5\text{kHz} \times 1\text{M}\Omega} = 32\text{pF} \leftarrow (2M\right)$





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Capacitor - Coupled difference amplifier :-.

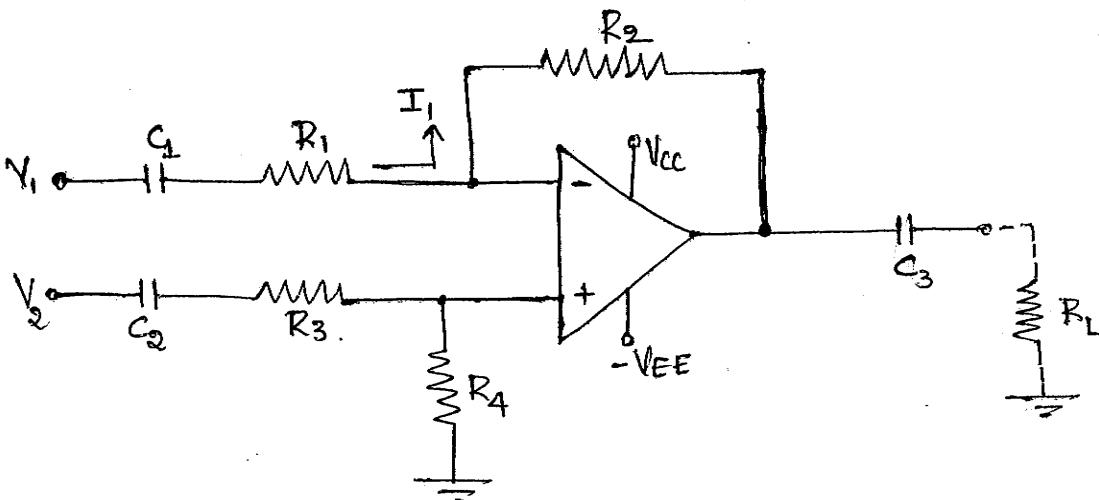


fig ① : capacitor - coupled difference amplifier.

fig ① shows a capacitor - coupled difference amplifier. this ckt amplifies the difference between two signals applied at the Non-INV and INV terminals of the op-amp.

* The o/p voltage is given by,

$$V_o = (V_2 - V_1)$$

Design steps :-

1) Let $I_1 = 100 \times I_B(\text{max})$

2) $R_1 = \frac{V_1}{I_1}$

3) $R_3 = R_1$

4) $R_2 = \frac{V_o}{I_1}$

5) $R_4 = R_2$

6) $X_{C1} = \frac{R_1}{10} \text{ at } R_1 ,$

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$



7) $X_{C_2} = (R_3 + R_4) / 10 \text{ at } f_1.$

$$C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10} \right)}$$

8) $X_{C_3} = R_L \text{ at } f_1.$

$$C_3 = \frac{1}{2\pi f_1 R_L}$$

9) $V_o = A_v (V_2 - V_1)$

Where, $A_v = \frac{R_2}{R_4}$



Design steps for LF 353 BIFET op-amp :-

1) Select $R_o = 1M\Omega$

2) WKT. $A_v = \frac{R_2}{R_1}$

$$\boxed{R_1 = \frac{R_2}{A_v}}$$

3) $R_3 = R_1$

4) $R_4 = R_2$

5) $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$

6) $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10} \right)}$

7) $C_3 = \frac{1}{2\pi f_1 R_L}$

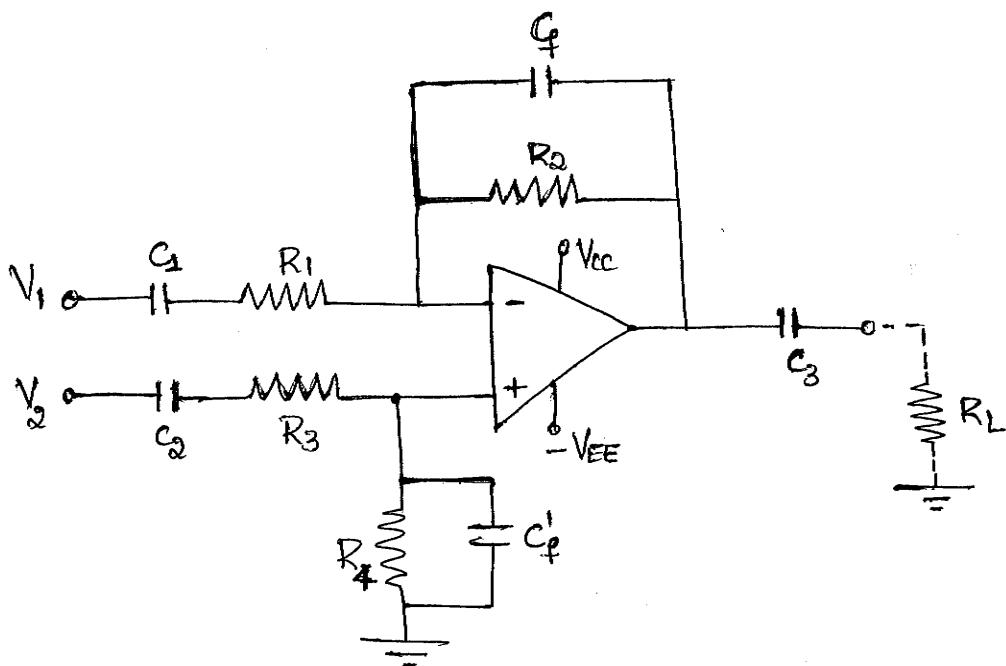
8) $A_v = \frac{R_2}{R_1}$

$V_o = A_v V_i$

$$\boxed{V_o = A_v (V_2 - V_1)}$$



Setting upper cut-off frequency for Difference amplifier :-



Design steps :-

i) For 741 op-amp :

$$1) \text{ Let } I_1 = 100 \times I_B(\text{max})$$

$$2) R_1 = \frac{V_1}{I_1}$$

$$3) R_3 = R_1$$

$$4) R_2 = \frac{V_o}{I_1}$$

$$5) R_4 = R_2.$$

$$6) C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$7) C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10} \right)}$$

$$8) C_3 = \frac{1}{2\pi f_1 R_L}$$

$$9) C_4' = \frac{1}{2\pi f_2 R_2}$$

$$10) C_4' = \frac{1}{2\pi f_2 R_4}$$

$$11) V_o = A_v V_i$$

$$\text{where } A_v = \frac{R_2}{R_1}$$

$$V_i = (V_2 - V_1)$$

$$V_o = \frac{R_2}{R_1} (V_2 - V_1)$$



ii) For BIFET LF 353 op-amp :-

1) select $R_2 = 1 \text{ M}\Omega$

2) $R_4 = R_2$

3) WKT $A_V = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{A_V}$$

4) $R_3 = R_1$

5) $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$

6) $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10} \right)}$

7) $C_3 = \frac{1}{2\pi f_1 R_L}$

8) $A_V = \frac{R_2}{R_1}$

$V_o = A_V V_i$

$$V_o = A_V (V_2 - V_1)$$



1) A difference amplifier has following components
 $R_1 = R_3 = 6.8 \text{ k}\Omega$, $R_2 = R_4 = 68 \text{ k}\Omega$, $C_1 = 2.2 \mu\text{F}$, $C_2 = 0.2 \mu\text{F}$ &
 o/p capacitor $C_3 = 1 \mu\text{F}$. Determine the ckt lower
 cut-off frequency and maximum differential z/p voltage
 that can be applied if the o/p is not to exceed 5 Volts.

Given :- $V_o = 5 \text{ V}$

June - 09, 6M

June - 06, 6M

Sol :-

$$* X_{C1} = \frac{R_1}{10}$$

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$C_1 = \frac{10}{2\pi f_1 R_1}$$

$$f_1 = \frac{10}{2\pi C_1 R_1} = \frac{10}{2\pi \times 2.2 \mu\text{F} \times 6.8 \text{ k}\Omega}$$

$$f_1 = 106 \text{ Hz}$$

NOTE :-

Differential z/p

$$V_d = V_2 - V_1$$

$$* A_V = \frac{R_2}{R_1} = \frac{68 \text{ k}\Omega}{6.8 \text{ k}\Omega}$$

$$A_V = 10$$

$$* A_V = \frac{V_o}{V_d} = \frac{V_o}{V_d}$$

$$V_d = \frac{V_o}{A_V} = \frac{5 \text{ V}}{10}$$

$$V_d = 0.5 \text{ V}$$

\leftarrow Differential z/p voltage.



Use of a single - polarity supply :-

Voltage follower :-

June - 08, 6M(EE)

i) capacitor coupled voltage follower using single polarity supply :-

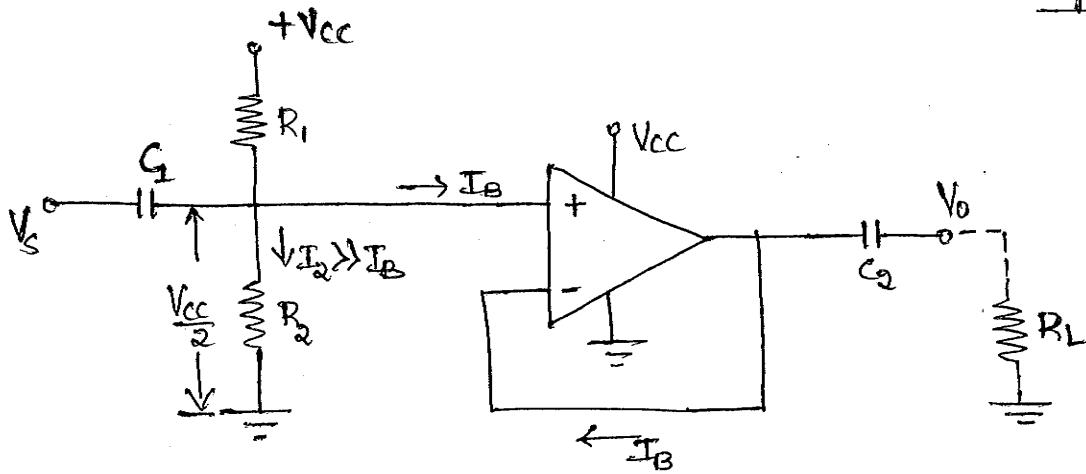


fig @ : capacitor - coupled voltage follower using a single - polarity supply.

* The capacitors block the dc bias voltages at the I/p & the o/p. If the op-amp data sheet lists the minimum supply voltage as $\pm 9V$, then a minimum of 18V should be used in a single polarity supply.

* The potential divider R_1 & R_2 sets the bias. Voltage at the Non-INV I/p terminal as $V_{CC}/2$ i.e. the dc o/p voltage & the INV input are also at $\frac{V_{CC}}{2}$. (\because Voltage follower).

* I/p Impedance is

$$Z_{in} = (R_1 \parallel R_2)$$



Design steps :-

1) Let $I_1 = 100 \times I_B(\text{max})$

2) $R_1 = R_2 = \frac{V_{CC}}{2I_1}$

3) $Z_{in} = (R_1 \parallel R_2)$

4) $X_{C1} = \frac{(R_1 \parallel R_2)}{10} \text{ at } f_1$

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1 \parallel R_2}{10} \right)}$$

5) $X_{C2} = R_L \text{ at } f_1$

$$C_2 = \frac{1}{2\pi f_1 R_L}$$



Non - INVERTING Amplifier :-

- i) Capacitor - coupled Non-INV amplifier using a single polarity supply :-

Jan -08, 8m (EE)
Jan -05, 8m (EE)

DEC - 10, 4M

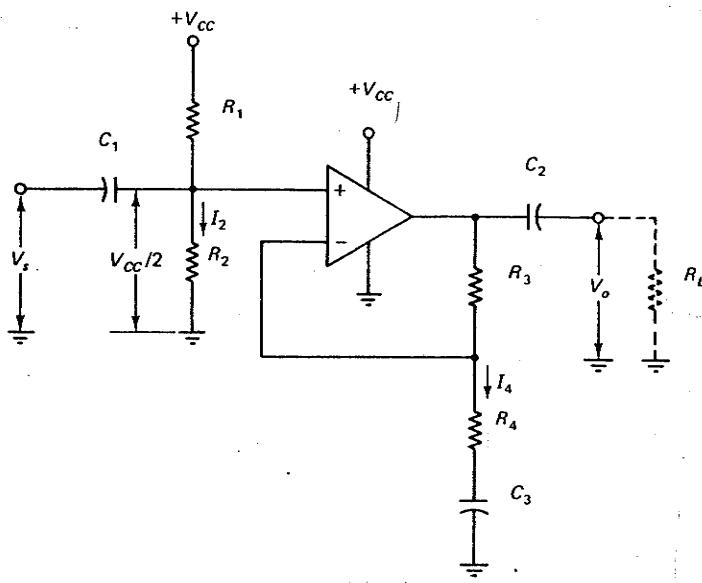


fig @ : Capacitor coupled Non-INV amplifier using a single polarity supply.

- * fig shows the ckt of a capacitor - coupled Non-INV amplifier using a single - polarity supply.

Two resistors R_1 & R_2 form the voltage divider ckt setting the bias voltage at $V_{cc}/2$.

The bottom of resistor R_4 is grounded through a capacitor 'c' as shown in fig. @.

If this capacitor is not used, then the dc Voltage developed across $R_4 = V_{cc}/2$ will be amplified by the gain A_v , resulting in an o/p. $V_o = A_v \times V_{cc}/2$. This large voltage saturates the o/p to a level equal to. $(V_{cc} - 1)$ Volts.



Design steps :-

1) Let $I_2 = 100 \times I_B(\text{max})$

2) Let $I_4 = 100 \times I_B(\text{max})$

3) $R_1 = R_2 = \frac{V_{CC}/2}{I_2}$

4) WKT $A_v = \frac{V_o}{V_i}$

$$V_i = A_v \cdot V_o$$

5) $R_4 = \frac{V_i}{I_4}$

6) $R_3 + R_4 = \frac{V_o}{I_4}$

Then Calculate R_3

7) $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1 || R_2}{10} \right)}$

8) $C_2 = \frac{1}{2\pi f_2 \frac{R_L}{10}}$

9) $C_3 = \frac{1}{2\pi f_1 R_4}$



Q) High Z_{in} Impedance capacitors coupled NON-INVERTING amplifier using single polarity supply:-

June - 10 M (EE)

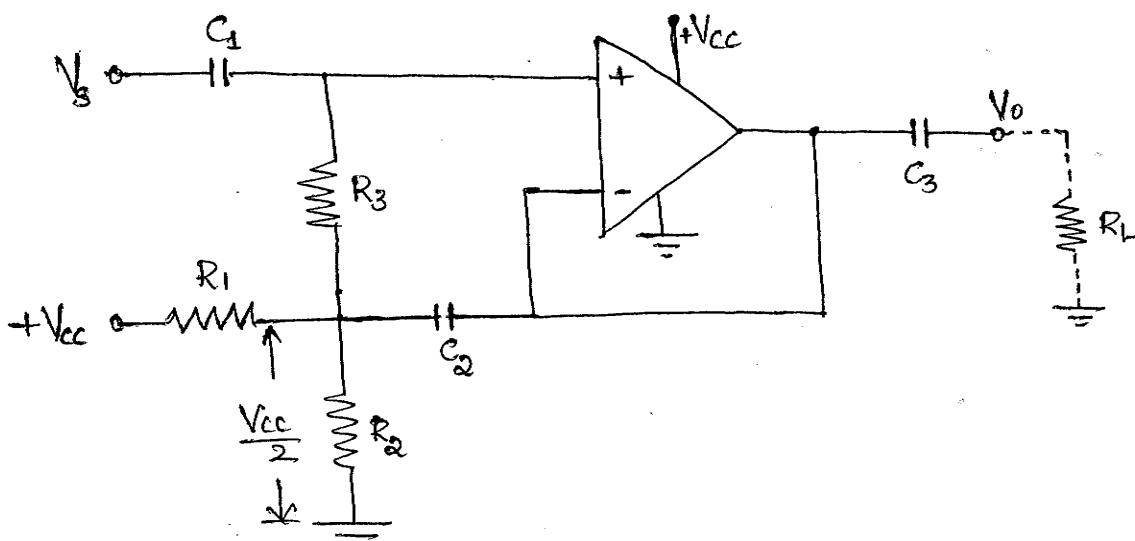


Fig (b) : High Z_{in} Impedance capacitor-coupled voltage follower using a single-polarity supply.

Fig (b) shows a high Z_{in} Impedance voltage follower using a single polarity supply.

- * Two resistors R₁ & R₂ form the voltage divider circuit setting the bias voltage at V_{cc}/2. The resistor 'R₃' is included to increase the Z_{in} impedance by providing feedback through the capacitor 'C₂'.

- * The Z_{in} impedance is given by

$$Z_{in} = (1 + M) R_3$$



* $X_{C2} = \frac{(R_1 \parallel R_2)}{10}$ at f_1

$$C_2 = \frac{1}{2\pi f_1 \left(\frac{R_1 \parallel R_2}{10} \right)}$$

* $X_{C4} = \frac{R_3}{10}$ at f_1

$$C_4 = \frac{1}{2\pi f_1 \left(\frac{R_3}{10} \right)}$$



PROBLEM

- 1) A capacitor-coupled Non-INN amplifier is to have a +24 supply, a voltage gain of 100, an O/P amplitude of 5V, a lower cut-off frequency of 75Hz, and a minimum load resistance of 5.6k Ω . Using a 741 op-amp design a suitable ckt

June-05, 12M

Given :- $V_{CC} = +24V$, $A_V = 100$, $V_o = 5V$, $f_l = 75\text{Hz}$, $R_L = 5.6\text{k}\Omega$
for 741 op-amp $I_B(\text{max}) = 500\text{nA}$

Sol :-

* Let $I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$
 $I_2 = 50\mu\text{A}$

* Let $I_4 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$
 $I_4 = 50\mu\text{A}$

* $R_1 = R_2 = \frac{V_{CC}/2}{I_2} = \frac{24/12}{50\mu\text{A}} = 240\text{k}\Omega$

choose $R_1 = R_2 = 220\text{k}\Omega$

* $V_i = \frac{V_o}{A_V} = \frac{5\text{V}}{100}$

$V_i = 50\text{mV}$

* $R_4 = \frac{V_i}{I_4} = \frac{50\text{mV}}{50\mu\text{A}}$

$R_4 = 1\text{k}\Omega$



$$* R_3 + R_4 = \frac{V_o}{I_4} = \frac{5V}{50\mu A}$$

$$R_3 + R_4 = 100 k\Omega$$

$$R_3 = 100 k\Omega - R_4$$

$$\therefore = 100 k\Omega - 1 k\Omega$$

$$R_3 = 99 k\Omega$$

choose $R_3 = 100 k\Omega$

$$* C_1 = \frac{1}{2\pi f_1 (R_1 || R_2 / 10)} = \frac{1}{2\pi \times 75 \times \left(\frac{220 k\Omega || 220 k\Omega}{10} \right)}$$

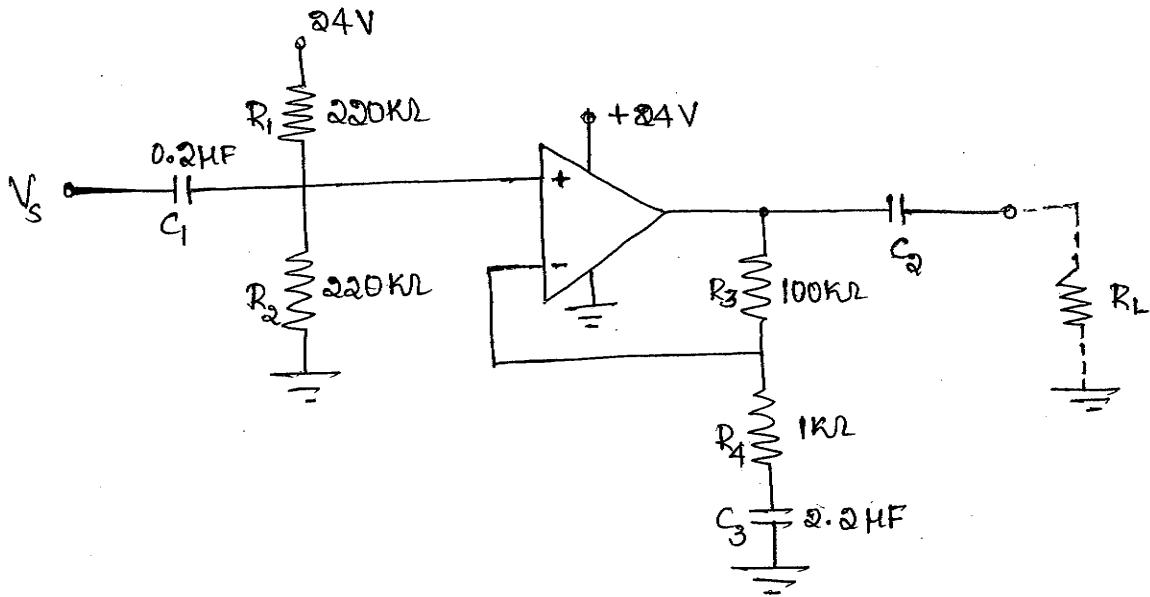
$$C_1 = 0.2 \mu F$$

$$* C_2 = \frac{1}{2\pi f_2 (R_L / 10)} = \frac{1}{2\pi \times 75 \times \left(\frac{5.6 k\Omega}{10} \right)} = 3.8 \mu F$$

choose: $C_2 = 3.9 \mu F$

$$* C_3 = \frac{1}{2\pi f_3 R_4} = \frac{1}{2\pi \times 75 \times 1 k\Omega} = 2.12 \mu F$$

choose $C_3 = 2.2 \mu F$



Capacitor - coupled INV amplifier using a single polarity supply:-

- * Draw the ckt diagram of a capacitor coupled INV amplifier using a single polarity supply and briefly explain.

Jan-10, 8M

June-08, 6M

- * Sketch the ckt of a capacitor coupled INV amplifier using a single polarity power supply. Briefly explain its operation.

Jan-09, 6M (EE)

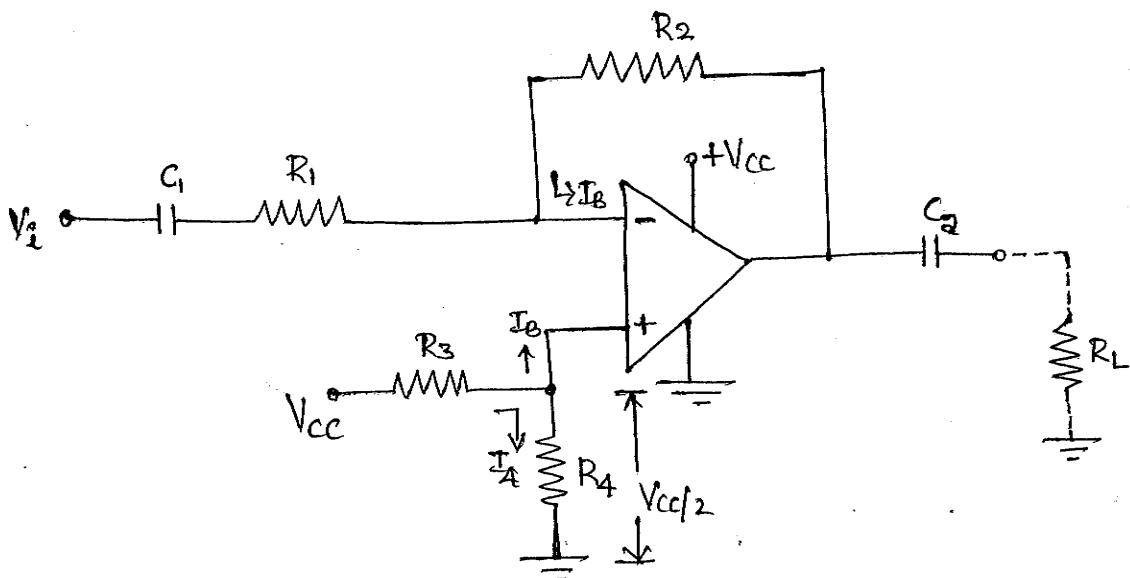


fig ①: capacitor - coupled INV - amplifier using a single - polarity supply.

fig ① shows the ckt of capacitor - coupled INV amplifier using a single polarity supply.

Two resistors R_3 & R_4 form the voltage divider ckt setting the bias voltage to $V_{cc}/2$ at the Non-INN terminal. This makes the INV I/p & o/p voltage equal to $V_{cc}/2$.



* IIP Impedance $Z_{in} = R_1$

Design steps :-

* Let $I_i = I_4 = 100 \times I_B(\text{max})$.

$$* R_1 = \frac{V_i}{I_i}$$

$$* \text{WKT } A_V = \frac{V_o}{V_i}$$

$$\boxed{V_o = A_V V_i}$$

$$* R_2 = \frac{V_o}{I_1}$$

$$* \text{WKT } A_V = \frac{R_2}{R_1}$$

$$\boxed{R_2 = A_V R_1}$$

$$* R_3 = R_4 = \frac{V_{cc}/2}{I_4}$$

$$* C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$* C_2 = \frac{1}{2\pi f_1 R_2}$$



1) Design a capacitor-coupled INV amplifier to operate with a +20V supply. The minimum IIP signal level is 50mV, the voltage gain is to be 68, the load resistance is 500Ω , and the lower cut-off frequency is to be 200Hz. Use 741 op-amp.

June-09, 6M
Jan-09, 6M(EE)

Given:- $V_{cc} = +20V$, $V_i = 50mV$, $A_v = 68$

$$R_L = 500\Omega, f_l = 200\text{Hz}$$

For op-amp 741 : $I_B(\text{max}) = 500\text{nA}$

Sol :-

* Let $I_I = I_A = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$I_I = I_A = 50\mu\text{A}$

* $R_1 = \frac{V_i}{I_I} = \frac{50\text{mV}}{50\mu\text{A}}$

$R_1 = 1\text{k}\Omega$

* WKT $A_v = \frac{V_o}{V_i}$

$$V_o = A_v V_i = 68 \times 50\text{mV}$$

$V_o = 3.4\text{V}$

* $R_2 = \frac{V_o}{I_I} = \frac{3.4\text{V}}{50\mu\text{A}}$

(OR) $R_2 = A_v \times R_1$
 $= 68 \times 1\text{k}\Omega$

$R_2 = 68\text{k}\Omega$

$R_2 = 68\text{k}\Omega$



$$* R_3 = R_4 = \frac{V_{CC}/2}{I_4} = \frac{20/2}{50 \mu A} = 200 \text{ k}\Omega$$

choose R₃ = R₄ = 180 kΩ ← (1m)

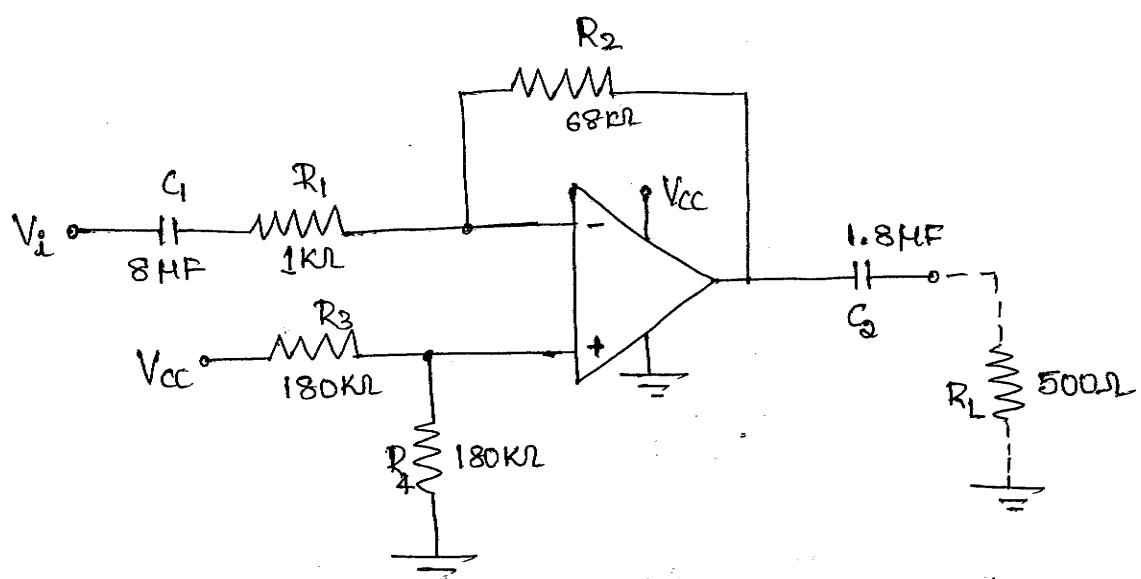
$$* C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)}$$

$$= \frac{1}{2\pi \times 200 \times \left(\frac{1 \text{ k}\Omega}{10} \right)}$$

C₁ = 7.95 μF , choose C₁ = 8 μF ← (1m)

$$* C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 200 \times 500} = 1.59 \mu F$$

choose C₂ = 1.8 μF ← (1m)



2) Design a capacitor coupled INV amplifier to operate with a single +24V supply. The minimum input signal level is 40mV, the voltage gain is -47, the load resistance is 680Ω & the lower 3dB frequency is 150 Hz. Using a 741 op-amp for which $I_B(\text{max}) = 500\text{nA}$.

Given :-

$$V_{cc} = 24V, V_i = 40\text{mV}, A_v = 47, R_L = 680\Omega,$$

$$f_l = 150\text{Hz}, I_B(\text{max}) = 500\text{nA}.$$

Sol :-

$$\star \text{ Let } I_t = I_4 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$$

$$I_t = I_4 = 50\mu\text{A}$$

$$\star R_1 = \frac{V_i}{I_t} = \frac{40\text{mV}}{50\mu\text{A}} = 800\Omega$$

$$\text{choose } R_1 = 820\Omega$$

$$\star V_o = A_v V_i = 47 \times 40\text{mV}$$

$$V_o = 1.88V$$

$$\star R_2 = \frac{V_o}{I_t} = \frac{1.88V}{50\mu\text{A}} = 37.6\text{k}\Omega \quad \boxed{\text{OR}} \quad R_2 = A_v R_1 \\ = 47 \times 820\Omega$$

$$\text{choose } R_2 = 39\text{k}\Omega$$

$$R_2 = 38.5\text{k}\Omega$$

$$\star R_3 = R_4 = \frac{V_{cc}/2}{I_4} = \frac{24/2}{50\mu\text{A}} = 240\text{k}\Omega$$

choose

$$R_3 = R_4 = 220\text{k}\Omega$$



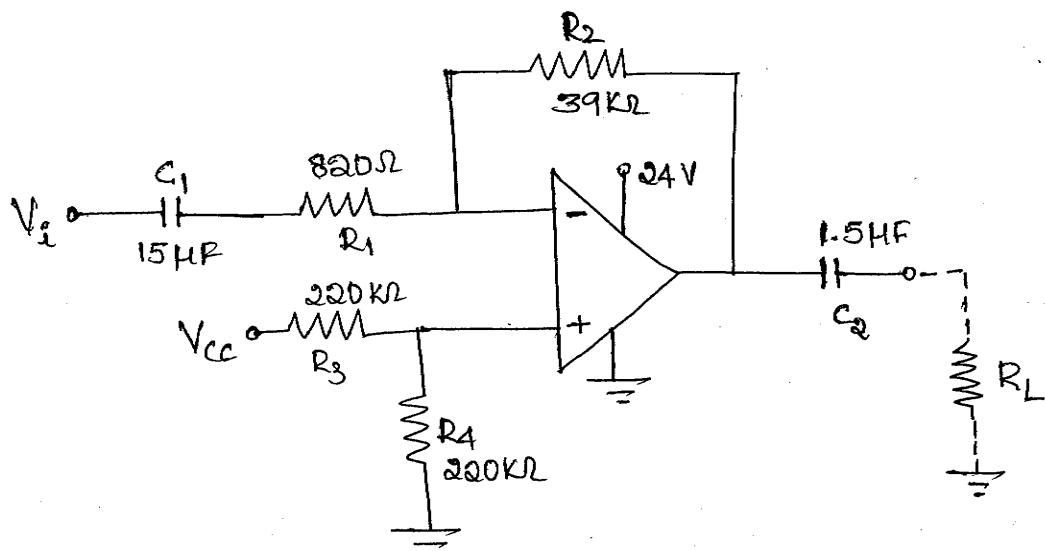
$$* C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10} \right)} = \frac{1}{2\pi \times 150 \times \left(\frac{820\Omega}{10} \right)} = 12.93 \mu F$$

choose $C_1 = 15 \mu F$

$$* C_2 = \frac{1}{2\pi f_1 R_L}$$

$$= \frac{1}{2\pi \times 150 \times 680\Omega} = 1.56 \mu F$$

choose $C_2 = 1.5 \mu F$



* Derive the condition under which an NON-INV amplifier can be used as a voltage follower. What will be the Input Impedance?

Jan-09, 6M

SOL :-

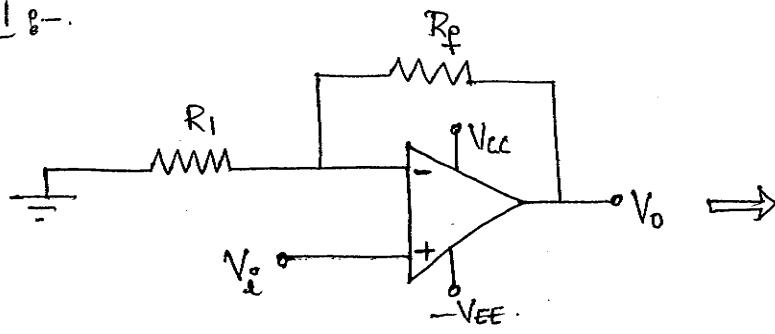


fig ① Non-INV amplifier.

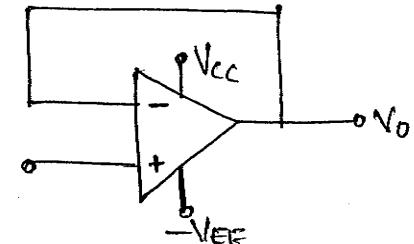


fig ② : Voltage follower.

Case i :-

WKT the gain of the Non-INV amplifier is given by

$$A_V = 1 + \frac{R_f}{R_1} \rightarrow ①$$

In eq ①, If $R_1 \rightarrow \infty$ & $R_f = 0$, then eq ① becomes

$$A_V = 1 + 0$$

$$\boxed{A_V = 1}$$

WKT. $A_V = \frac{V_o}{V_i}$

$$\therefore A_V = \frac{V_o}{V_i} = 1$$

$$\boxed{V_o = V_i}$$

Now the ckt behave as voltage follower.



Case ii' >

WKT for Non-INV amplifier

$$A_V = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_i} \rightarrow \textcircled{2}$$

If $R_i \gg R_f$, then $\frac{R_f}{R_i} \ll 1$ & eq $\textcircled{2}$ becomes

$$A_V = \frac{V_o}{V_i} \approx 1$$

$$\therefore V_o \approx V_i$$

Now ckt behaves as voltage follower.

* I/P Impedance of Non-INV amp is

$$Z_{in} = (1 + M\beta) Z_i$$

The I/P Impedance of voltage follower is

$$Z_{in} = R_i$$



Chapter-3

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Op-Amps Frequency Response and Compensation

Introduction :-

op-amp introduces phase-shift when ac signal is applied to its I_P. When frequency of ac signal increases, the phase shift introduced by op-amp also increases.

At some particular frequency the total phase shift can be upto 360°.

When the loop voltage gain “ $M_P \geq 1$ ” and the total phase shift from I_P to O_P through op-amp & from O_P to I_P through feedback path, approaches 360°, then the op-amp circuit becomes unstable and breaks into oscillation.

To avoid instability, compensation capacitors and resistors are used either to reduce voltage gain or to minimize the phase shift.

* The upper cut-off frequency of an op-amp ckt depends upon the particular op-amp employed (741 or LF353 etc) and upon the compensating components (R & C).

* The frequency response is also limited by the op-amp slew rate.



NOTE :-

Loop voltage gain :-

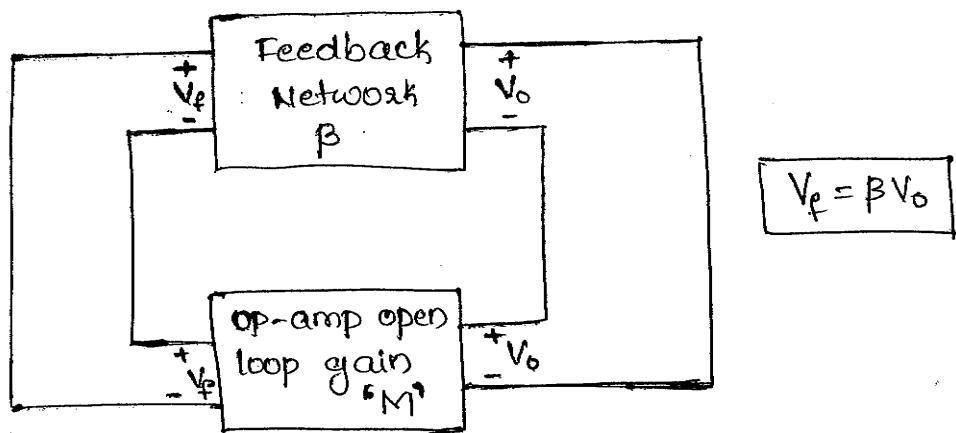
Loop voltage gain of the op-amp is defined as the product of the voltage gain 'M' & the feedback factor 'B' i.e., "MB".

op-amp circuit stability :-

* Discuss the op-amp ckt stability and show how feedback in an INVERTING amplifier can produce instability. Explain the conditions necessary for oscillations to occur in an op-amp ckt.

Jan -10, 8 M

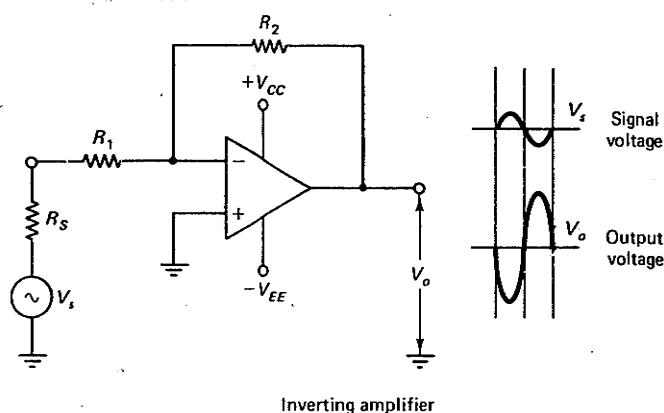
⇒ * Due to the presence of feedback network, op-amp circuits are bound to become unstable and break into oscillations.



* When loop gain ie $MB=1$, & total phase shift around the loop is 360° , then op-amp become unstable & break into oscillation. To prevent this, frequency compensation ckt's are used.



INVERTING Amplifier :-



Inverting amplifier

Fig ① : INV amplifier

- * In INVERTING amplifier IP signal ' V_s ' is amplified by a factor $\frac{R_2}{R_1}$ and phase shifted by 180° .

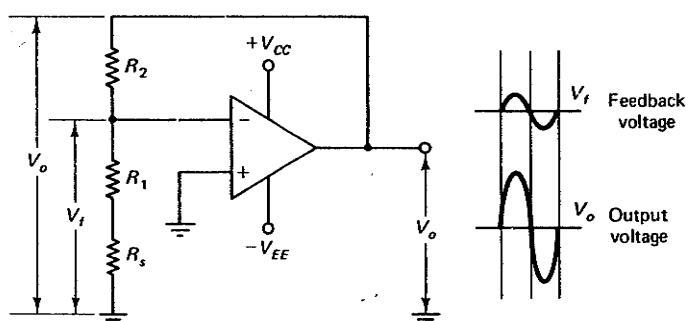


Fig ② Inverting amplifier oscillating

P.T.O



- * The circuit of fig ① can be redrawn with input voltage V_s grounded and is shown in fig ②.

The o/p voltage ' V_o ' is divided by the feedback network to produce feedback voltage ' V_f '. This feedback voltage V_f is amplified by open loop gain M of the op-amp to produce an o/p voltage ' V_o ' which in turn generates the feedback voltage ' V_f '.

$$\therefore \text{O/p voltage } V_o = M V_f \quad (\because \text{I/P is } 'V_f')$$

- * The feedback voltage V_f is given by

$$V_f = I R_1$$

$$\text{where } I = \frac{V_o}{R_1 + R_2}$$

$$V_f = \frac{R_1}{R_1 + R_2} \cdot V_o$$

$$V_f = \beta V_o$$

Where $\beta = \frac{R_1}{R_1 + R_2}$ & is called feedback factor.

(Neglecting signal source resistance R_s).

- * If βV_o is exactly equal to V_f in both magnitude and phase, the circuit is supplying its own ac I/p and a state of continuous oscillation exists.



- * The conditions necessary for oscillations to occur in an op-amp ckt are:
 - 1) The loop gain should be equal to or greater than one. i.e $M\beta=1$
 - 2) The phase shift around the loop should be equal to 360° .

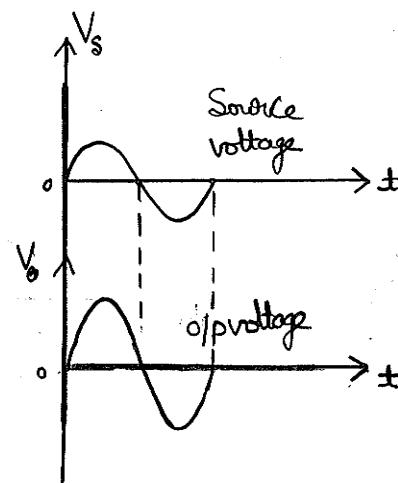
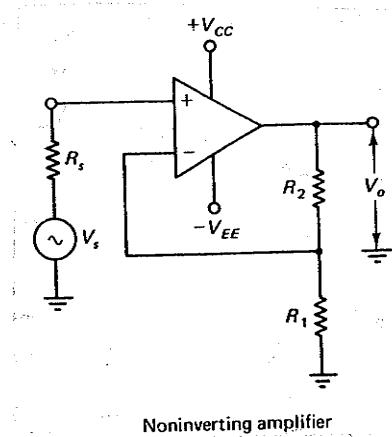
The above two conditions are known as "Barkhausen Criteria".



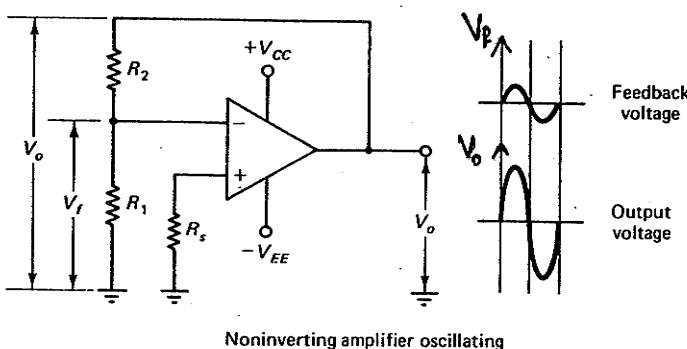
NON-INVERTING Op-amp :-

- * show how feedback in an Non-INV amplifier ckt can produce instability.

[June -07, 6M(EE)]



- * In Non-INV amplifier I/p Signal ' V_s ' is amplified by a Factor $(1 + \frac{R_2}{R_1})$ without any phase-shift.



P.T.O



- * The ckt of fig ① can be redrawn with IIP voltage ' V_s ' grounded and is shown in fig ②.
- * The o/p voltage ' V_o ' is divided by the feedback network to produce feedback voltage ' V_f '. This feedback voltage V_f is amplified by open-loop gain 'M' of the op-amp to produce an o/p voltage ' V_o ' which inturn generates the feedback voltage ' V_f '.
 \therefore o/p voltage
$$V_o = M V_f \quad (\because \text{IIP is } V_f)$$

- * The feedback voltage V_f is given by

$$V_f = IR_1$$

Where $I = \frac{V_o}{R_1 + R_2}$

$$V_f = \frac{R_1}{R_1 + R_2} V_o$$

$$V_f = \beta V_o$$

Where $\beta = \frac{R_1}{R_1 + R_2}$ & is called feedback factor.

- * If βV_o is exactly equal to V_f in both magnitude & phase, the circuit is supplying its own ac IIP and a state of continuous oscillation exists.



Frequency and phase response :-

i) frequency & phase response of single-stage amplifier.

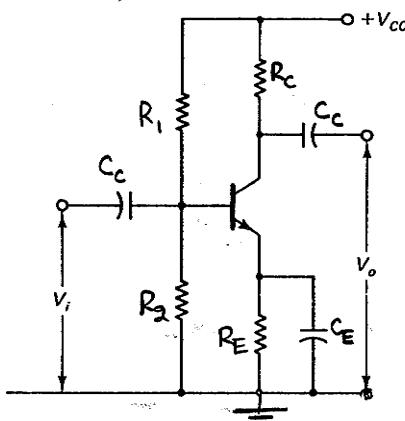


Fig 1: (a) Single-stage transistor amplifier

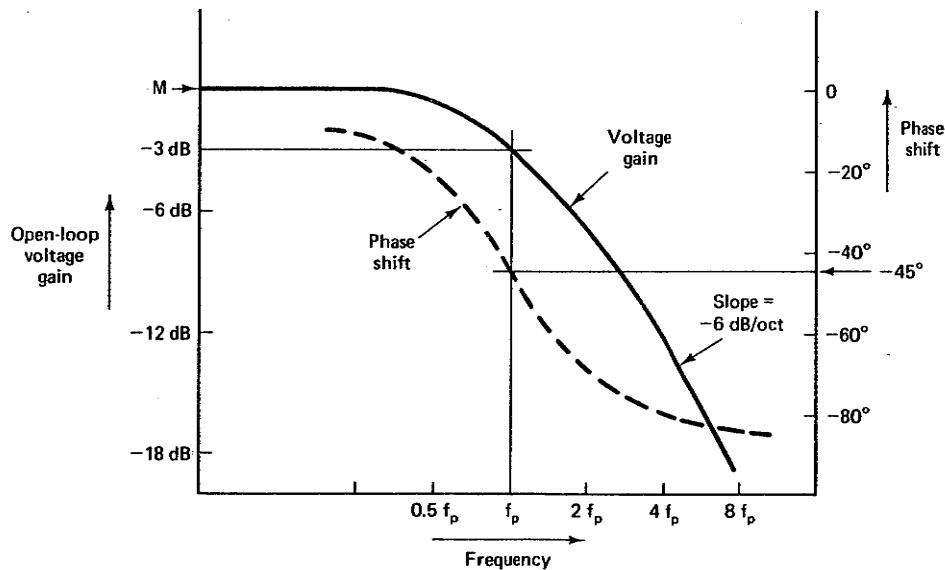


Fig 1: (b) High frequency ends of gain/frequency and phase/frequency responses

P.T.O



* fig 1 (a) shows a single-stage transistor amplifier circuit while fig 1 (b) shows the high frequency end of the gain/ frequency and phase/ frequency response of the circuit.

* The voltage gain of a single-stage amplifier starts to fall off at some high frequency. This may be due to junction capacitance of transistor and stray capacitance in the circuit.

* The frequency is plotted to a logarithmic base. The voltage gain falls off at a rate of 6dB. for each doubling of frequency (i.e -6dB per octave).

This can also be stated as -20dB/decade i.e for each ten times increase in frequency.

* The pole frequency ' f_p ' is the frequency at which the voltage gain reduces to -3dB from the mid-band gain.

Fig 1 (b) also shows the graph of phase shift versus frequency. At pole frequency ' f_p ' phase lag increases from 0° to -45° .

As the frequency increases, the phase lag continues to increase to a maximum of -90° .



ii) Frequency & phase response of op-amp :-

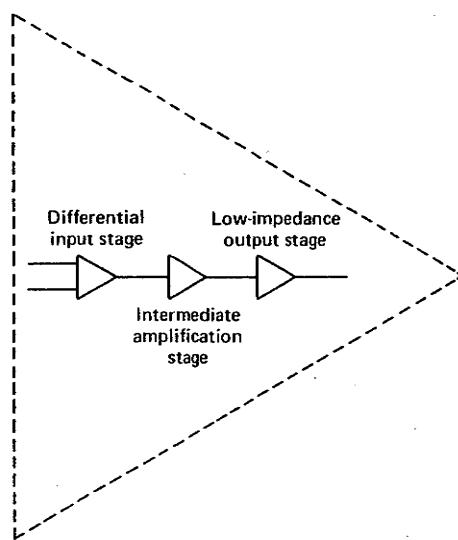


Fig 1

An operational amplifier has three stages of amplification

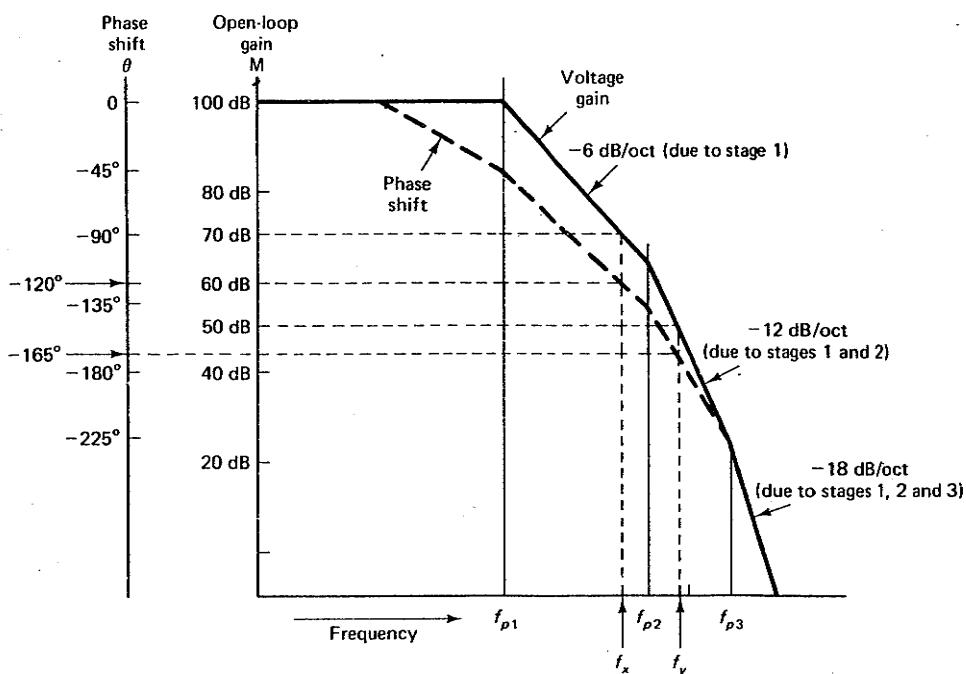


Fig 2

Straight-line approximation of op-amp open-loop gain/frequency and phase/frequency responses

P.T.O



Fig ① shows the internal block diagram of op-amp.

It has three stages of amplification.

Stage 1 :— Differential amplifier stage.

Stage 2 :— Intermediate amplification stage.

Stage 3 :— Low impedance op stage.

- * The f_{p1} , f_{p2} and f_{p3} are the pole frequencies of these three stages and are such that $f_{p3} > f_{p2} > f_{p1}$

A straight line approximation of the gain / frequency response graph for a typical op-amp is shown in fig ②. This graph is also known as Bode plot.

- * From fig ②, we observe that the overall voltage gain 'M' decreases (fall off) at 6dB/octave or -20dB/decade - from f_{p1} when only the gain of stage 1 is decreasing.

- * From f_{p2} , stage 2 gain is decreasing at 6dB/octave, so the total fall rate is 12dB/octave or -40dB/decade.

- * Finally, when the frequency reaches f_{p3} , the gain of stage-3 is decreasing at 6dB/octave so that the overall fall off 'M' due to all 3 stages is 18dB/octave or -60dB/decade.

- * The phase-shift of each stage is also added together to give the total phase shift for the op-amp.



* At f_{p1} , the stage -1 phase shift is -45° while the phase shift from stage -2 & stage 3 is negligibly small, so the total phase shift is -45° .

* At f_{p2} , stage -2 adds another -45° .

At this point the stage -1 phase shift is at its maximum of -90° :

∴ The total phase shift at f_{p2} is

$$\theta = -45^\circ - 90^\circ$$

$\theta = -135^\circ$

$$\left. \begin{array}{l} \therefore \text{Stage-1} \rightarrow 90^\circ \\ \text{Stage-2} \rightarrow -45^\circ \end{array} \right\}$$

* When the frequency is f_{p3} ,

stage -1 phase shift $\rightarrow -90^\circ$

stage -2 phase shift $\rightarrow -90^\circ$

stage -3 phase shift $\rightarrow -45^\circ$

$$\therefore \theta = -90^\circ - 90^\circ - 45^\circ$$

$\theta = -225^\circ$

This open-loop phase shift is additional to the -180° phase shift that normally occurs from the op-amp INV. I/P terminal to the O/P.



Phase Margin :-

- * WKT oscillations occur in an op-amp ckt when the loop gain $M_B \geq 1$ and the loop phase shift is -360° .

In fact, the phase shift does not have to be exactly -360° for oscillation to occur.

For eg :- If $M_B \geq 1$ & loop phase shift is -330° . makes the ckt unstable. To avoid oscillations the total loop phase shift must not be greater than -315° when $M_B = 1$

- * The difference between 360° and the actual phase shift at $M_B=1$ is referred to as the phase Margin.

To have stability

$$\text{Minimum phase margin} = 360^\circ - 315^\circ = 45^\circ$$

- * What is the need of stability check in an op-amp from the frequency response. Show how stability of an op-amp can be analyzed. When do you say an op-amp is stable?

Jan - 09, 8M





High gain Amplifier stability :

OR.

stability of high gain Amplifier :-

- * Explain why an op-amp with a higher closed loop gain is more likely to be stable.
- WKT, the overall voltage gain of an amplifier with negative feedback is

$$A_V = \frac{1}{B}$$

$$\boxed{B = \frac{1}{A_V}} \rightarrow \textcircled{1}$$

- * The loop gain = $M_B \rightarrow \textcircled{2}$

Substituting eq $\textcircled{1}$ in $\textcircled{2}$, we get

$$\boxed{M_B = \frac{M}{A_V}}$$

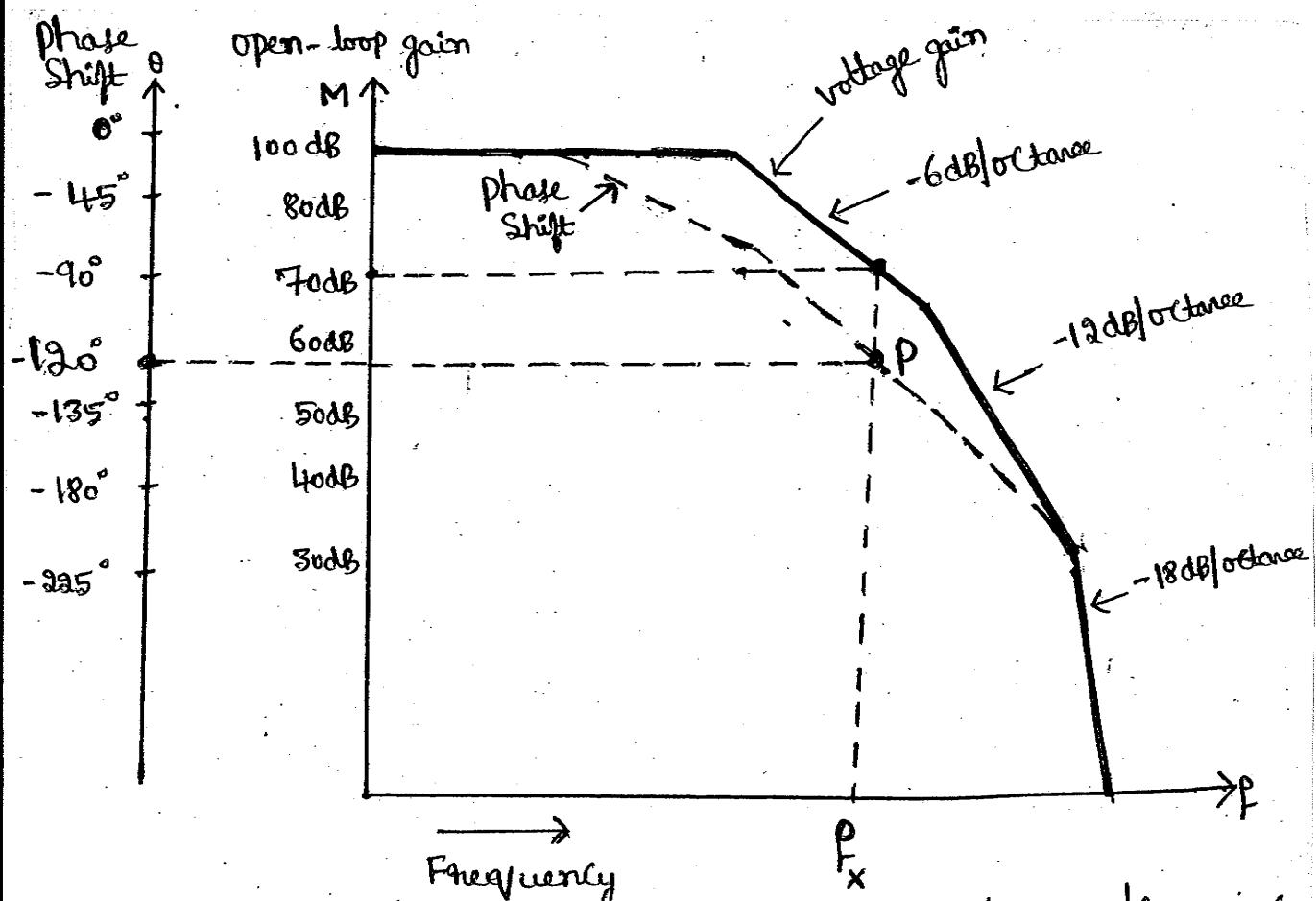


Fig ①: Straight-line approximation of op-amp open-loop gain/frequency and phase/frequency responses

* Suppose an INVERTING op-amp with a frequency response as in fig ① is used with feedback to produce an amplifier with a closed loop gain of 70dB.

A horizontal line drawn on the frequency response graph at $A_V = 70 \text{ dB}$ intersects the open-loop gain / frequency graph at frequency f_x .

At this point $M = 70 \text{ dB}$.

$$\therefore \text{Loop gain } M_B = \frac{M}{A_V} = \frac{70 \text{ dB}}{70 \text{ dB}}$$

$$M_B = 1$$

\therefore At frequency ' f_x ', the first condition of the ckt to become unstable is satisfied.

Now, let us calculate the loop phase shift at frequency ' f_x '. The vertical line at frequency f_x cuts the phase characteristics at point 'p'. A horizontal line drawn at p corresponds to -120° phase shift i.e.

$$\theta = -120^\circ$$

* The phase shift $\phi = -180^\circ + \theta = -180^\circ - 120^\circ$

$$\phi = -300^\circ$$

* The phase margin $= 360^\circ - \phi = 360^\circ - 300^\circ$

$$\therefore \text{phase margin} = 60^\circ$$



- * With $A_V = 40 \text{ dB}$, at $M_B = 1$, the phase margin is 60° .

Since the minimum phase margin for stability is 45° . \therefore The ckt is unlikely to oscillate & remains stable even though $M_B = 1$.

- * For frequencies lower than f_x , the loop gain ' $M_B > 1$ ' but the phase shift will be less than -120° and the ckt will not break into oscillations.

- * For frequencies greater than f_x , the loop gain ' $M_B < 1$ '. The total phase shift may be between -330° to -360° , but $M_B < 1$. Thus the ckt will not break into oscillations at higher frequencies.

- * With the help of frequency and phase response curve of a typical op-amp, discuss the concept of Circuit Stability for high gain and low gain amplifiers

Dec - 10, 12M





stability of lower gain amplifiers :-

- * Explain why an op-amp with a lower closed loop gain is more likely to be unstable.

Jan - 05, 6M(EE)



- * WKT, the overall voltage gain of an amplifier with negative feedback is

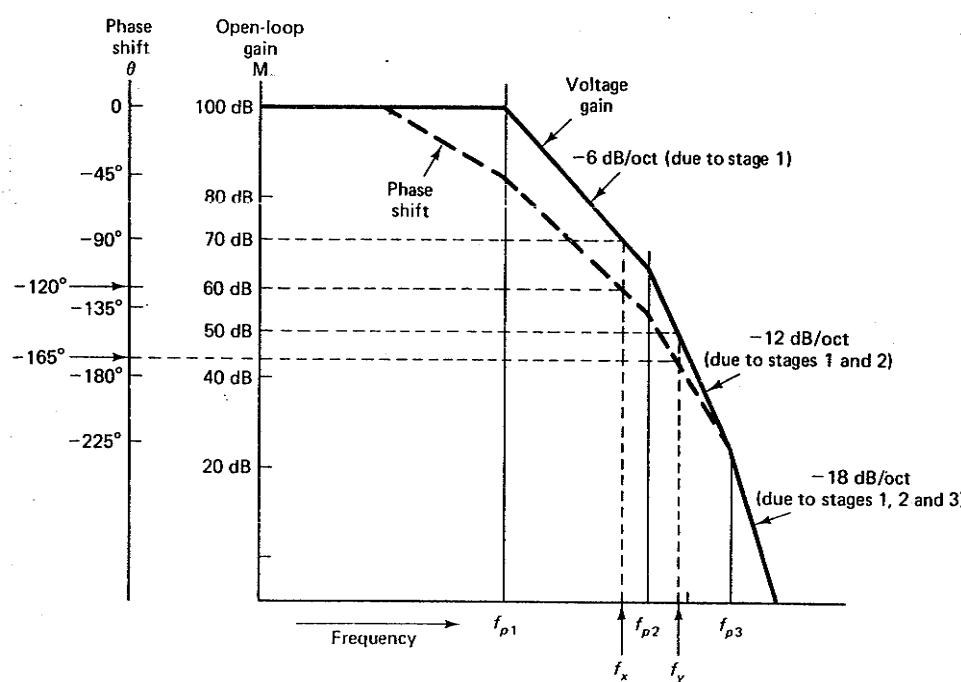
$$A_V = \frac{1}{B}$$

$$B = \frac{1}{A_V} \rightarrow ①$$

- * The loop gain = $M_B \rightarrow ②$

substituting eq ① in eq ② we get

$$M_B = \frac{M}{A_V}$$



Straight-line approximation of op-amp open-loop gain/frequency and phase/frequency responses



* Suppose an INVERTING op-amp with a frequency response as shown in fig ① is used with feedback to produce an amplifier with a closed loop gain of 50 dB.

* A horizontal line drawn on the frequency response graph at $A_v = 50 \text{ dB}$ intersects the open loop gain / freq. graph at frequency f_y .

At this point $M = 50 \text{ dB}$

$$\therefore \text{Loop gain} = M_B = \frac{M}{A_v} = \frac{50 \text{ dB}}{50 \text{ dB}}$$

$$M_B = 1$$

\therefore At frequency ' f_y ', the first condition of the ckt to become unstable is satisfied.

* Now let us calculate the loop phase shift at frequency ' f_y '. The vertical line at frequency f_y cuts the phase characteristic at point 'P'.

A horizontal line drawn at P corresponds to -165° phase shift i.e. $\Theta = -165^\circ$

* The phase shift introduced by the INV amplifier is -180° .

$$\therefore \text{The total phase shift } \phi = -180^\circ + \Theta \\ = -180^\circ - 165^\circ$$

$$\phi = -345^\circ$$



* The phase margin = $360^\circ - \phi$
 $\approx 360^\circ - 345^\circ$

∴ [phase margin = 15°]

- * With $A_V = 50$ dB, at $M_B = 1$, the phase margin is 15° which is less than the minimum phase margin of 45° .

As both the conditions are satisfied, the ckt break into oscillations.

- * With $A_V = 70$ dB, there is less feedback and the circuit is stable.

Whereas at $A_V = 50$ dB, there is more feedback and the circuit breaks into oscillations.



Frequency Compensating Methods :-

- * What is frequency compensation? Mention different types of frequency compensation.

In order to stabilize op-amp circuit, frequency compensating networks are used.

These networks are R-C networks connected into the op-amp circuit.

The different frequency compensating networks are :-

- 1) phase lag compensation.
- 2) phase lead compensation
- 3) Miller effect compensation
- 4) Feed forward compensation.

* phase - Lag compensation :-

- * With a neat sketch, explain the working of a lag compensation network. Show how it affects the frequency response of an op-amp.

June - 10, 8M

June - 10, 6M(EE)

Jan - 06, 6M(EE)

- * Draw the ckt of a lag compensation network. Explain its operation & show how it affects the frequency response of an op-amp.

June - 08, 6M

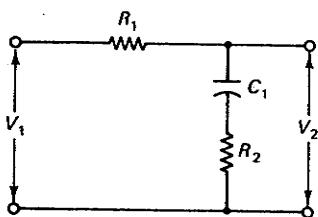


- * What is frequency compensation? Explain phase lag or phase lead compensation method.

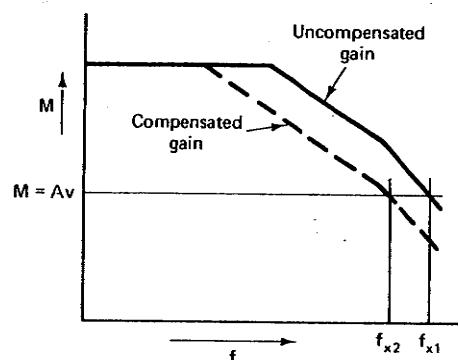
Jan -10, 8M(EE)

- * Explain the frequency compensating methods adopted to stabilize the op-amp ckt.

June -06, 6M(EE)



(a) Lag compensation network



(b) Effect of lag compensation on gain/frequency response

Fig ①

Fig 1 (a) shows a phase-lag compensation network consisting of two resistors and a capacitor.

- * At lower frequencies, $X_{C1} \gg R_2$ then voltage V_2 lags V_1 . A phase lag of -90° might be introduced.
- * At higher frequencies, $X_{C1} \ll R_2$ & the network becomes pure resistive network and no phase lag occurs. But at higher frequencies the phase lag network introduces only attenuation as shown in fig 1 (b).



- * The components of the phase lag network (R_1, R_2 & C_1) are calculated to introduce additional phase lag at lower frequencies. At higher frequencies there is only attenuation without any additional phase lag.
- * The effect of phase-lag network attenuation is to shift the frequency from f_{x_1} to a lower frequency f_{x_2} at which $M_B=1$

Since $f_{x_2} < f_{x_1}$, the phase shift introduced by op-amp at f_{x_2} will be less than at f_{x_1} . Due to this, the phase margin increases and the ckt is unlikely to break into oscillations.

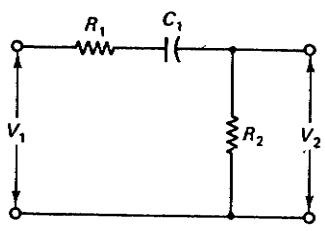
Thus the phase lag network is used to attenuate the loop gain, so that $M_B=1$ occurs at frequencies where the amplifier phase shift is too small to cause oscillations.



phase - lead compensation :-

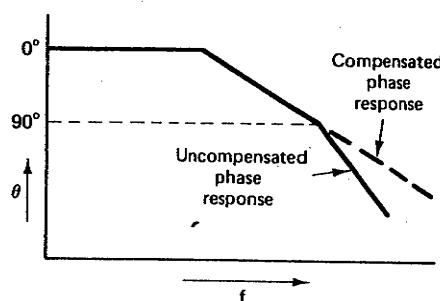
* Explain the Frequency Compensation technique, using a phase - lead network

Dec-10, 4M



a. Lead compensation network

Fig ①



b. Effect of lead compensation on phase/frequency response

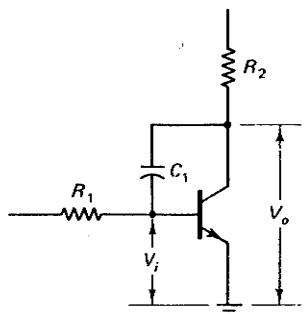
* In fig 1 @ , the RC network introduces a phase lead.

When $X_{C1} \gg R_1$, V_2 leads by V_1 . The phase lead network is used to introduce a phase lead.

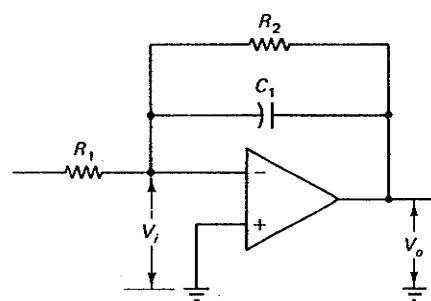
The phase lead network cancels some of the unwanted phase lag introduced by op-amp internal circuitry. This increases the phase margin at $M_B=1$. & improves the circuit stability.



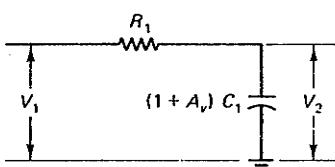
Miller - Effect compensation :-



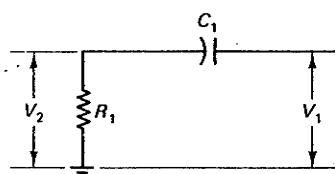
(a) Single-stage transistor amplifier with capacitor between input and output



(b) Op-amp inverting amplifier with capacitor between input and output



(c) R_1 and $(1 + A_v) C_1$ in (a) above constitutes a lag network for signal voltages



(d) R_1 and C_1 in (b) above constitutes a lead network for feedback voltages

Fig ①

• consider a common-emitter transistor amplifier stage with a capacitor connected between its collector and base terminal as shown in fig 1@.

* When an input voltage V_i is applied, V_i is amplified and phase inversion occurs. The o/p voltage is given by

$$V_o = -A_v V_i \rightarrow ①$$



* When the base voltage goes up by V_i and the collector voltage goes down by $A_v V_i$, the voltage change across capacitor C_1 is.

$$\Delta V_{C1} = V_i - V_o \rightarrow ②$$

{ Applying KVL from V_i, V_c & V_o

$$V_i - \Delta V_{C1} - V_o = 0.$$

$$\Delta V_{C1} = V_i - V_o$$

Sub eq ① in eq ② we get

$$\Delta V_{C1} = V_i - (-A_v V_i)$$

$$\Delta V_{C1} = V_i + A_v V_i$$

$$\Delta V_{C1} = V_i [1 + A_v]$$

∴ The charge supplied to the capacitor is

$$Q = C_1 \times \Delta V_{C1}$$

$$= C_1 \times V_i [1 + A_v]$$

$$Q = C_1 [1 + A_v] V_i$$

∴ When the base voltage increases by V_i , then at the o/p, the capacitance appears to have been amplified by an amount $(1 + A_v)$. This effect of capacitance amplification is called as "Miller effect".

* A capacitor and resistor connected in the same way as C_1 and R_1 in fig 1@ are used for the frequency compensation inside the 741 op-amp. This circuit behaves as a phase-lag network as shown in fig 1@.

* The advantage here is that the capacitance is amplified by the Miller effect, so very small capacitance is used inside the 741 op-amp.



* In fig 1 (b) the combination of C_1 and R_1 behaves as a phase lead network within the feedback loop. Thus C_1 and R_1 introduce a phase lead to cancel some of the phase lag in the loop.

Feed forward compensation :-

In feedforward compensation a capacitor is connected b/w the IIP & op terminals of the high-gain stage of the op-amp.

At high frequencies the high gain op-amp stage introduces large amount of phase shift to the IIP signal.

The capacitor connected across op-amp compensates this phase to some extent thereby reducing the large phase shift.



Upper cut-off frequency of an op-amp :-

- * Show that the upper cut-off frequency of an op-amp ckt occurs when the open-loop gain equals the closed-loop gain.

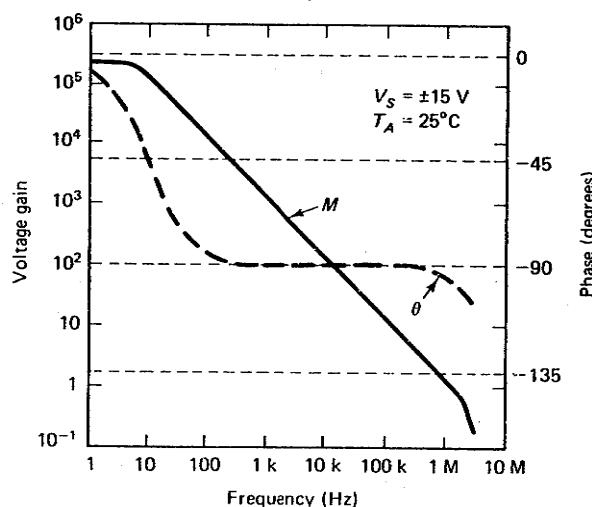


Figure ① Open-loop gain/frequency and phase/frequency responses for a 741 operational amplifier. The phase shift remains approximately -90° for much of the frequency range.

- * The upper cut-off frequency ' f_2 ' is the frequency at which the closed loop gain falls to $\frac{V_{fb}}{V_{in}}$ below the normal mid-frequency gain.
- * The voltage gain of an amplifier with negative feedback is given by :

$$A_V = \frac{M}{1 + MB} \rightarrow ①$$

WKT the phase shift of the op-amp increases with increase in signal frequency.

Then eq ① becomes,

$$A_V \approx \frac{M/\theta}{1 + (M/\theta B)} \rightarrow ②$$



from fig ① it is clear that the phase shift for the 741 remains at -90° for much of the frequency range during which the gain is falling by 20dB per decade.

Substituting -90° for θ in the eq ②

$$A_V \approx \frac{M \cancel{-90^\circ}}{1 + (M \cancel{-90^\circ} \beta)}$$

$$A_V = \frac{-jM}{1 - jM\beta}$$

$$|A_V| = \frac{M}{\sqrt{1^2 + (M\beta)^2}} \rightarrow ③$$

When $M = A_V = \frac{1}{\beta}$, then eq ③ becomes

$$|A_V| = \frac{A_V}{\sqrt{1^2 + \left(\frac{1}{\beta} \cdot \beta\right)^2}} = \frac{A_V}{\sqrt{1^2 + 1^2}}$$

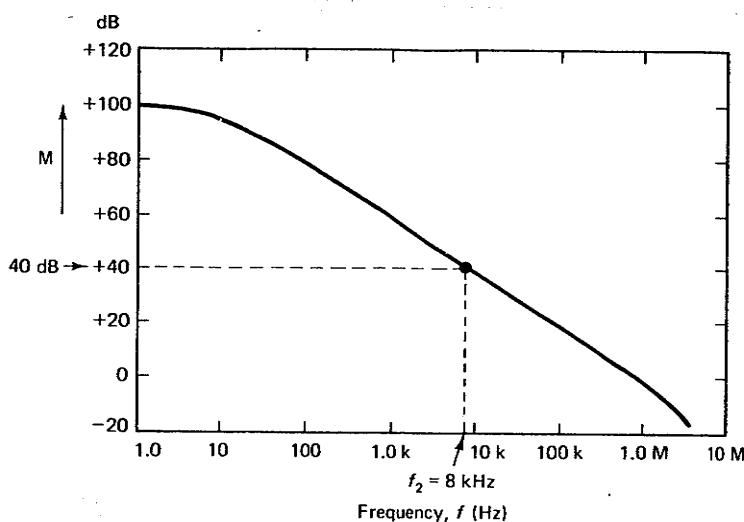
$$|A_V| = \frac{A_V}{\sqrt{2}}$$

$$\therefore |A_V|_{dB} = (A_V \cdot -3) dB$$

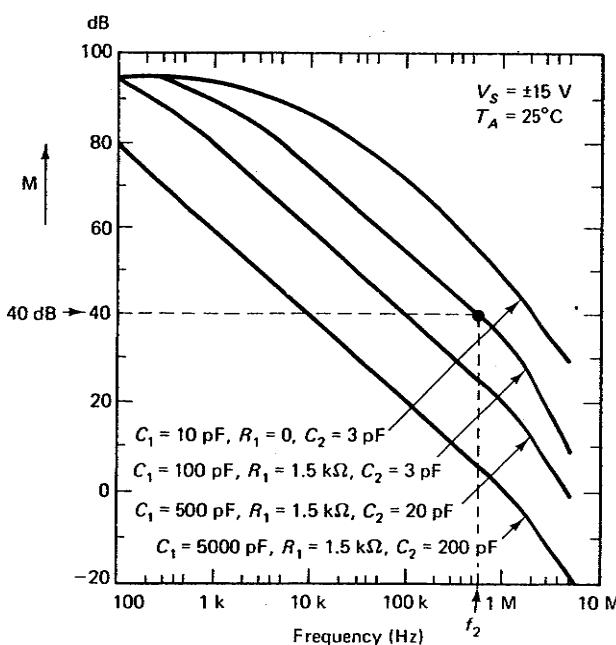
\therefore The upper cut-off frequency f_o occurs at $M = A_V$.



- Q) Determine the typical upper cut-off frequency for a Non - INV amplifier with $A_v = 100$, @ when a 741 op-amp is used and ⑥ when a 709 is employed.



(a) Gain/frequency response for 741 operational amplifier



(b) Gain/frequency response for 709 operational amplifier using recommended compensation

Figure Q Gain/frequency responses for 741 and 709 operational amplifiers. The upper cutoff frequency for any op-amp circuit is found by drawing a horizontal line at $M \approx A_v$.



Sol :- $A_V = 100$

$$(A_V)_{dB} = 20 \log_{10}(100)$$

$$(A_V)_{dB} = 40 \text{ dB}$$

∴ Upper cut off frequency f_2 occurs at

$$(A_V)_{dB} = 40 \text{ dB}$$

- a) In fig ①, draw a horizontal line at $M = 40 \text{ dB}$. From the intersection of the line & the open-loop frequency response, $f_2 \approx 8 \text{ kHz}$

- b) For the 709, refer to fig ②, draw a horizontal line at $M = 40 \text{ dB}$. The intersection of the $M = 40 \text{ dB}$ line and the frequency response curve.

$$f_2 = 600 \text{ kHz}$$

Gain - Bandwidth product :- (GBW)

The gain - bandwidth product of an op-amp is the product of closed loop gain ' A_V ' and the cut-off frequency for the gain.

i.e. Gain - bandwidth product = $A_V f_2$



* calculate the gain-bandwidth product.

- i) For $A_V = 80 \text{ dB}$, $f_2 = 80 \text{ Hz}$
- ii) For $A_V = 60 \text{ dB}$, $f_2 = 800 \text{ Hz}$
- iii) For $A_V = 1$, $f_u = 800 \text{ kHz}$

Sol :- i) for $A_V = 80 \text{ dB}$, $f_2 = 80 \text{ Hz}$

$$(A_V)_{\text{dB}} = 20 \log_{10} (A_V)$$

$$A_V = \log_{10}^{-1} \left(\frac{80}{20} \right)$$

$$A_V = 10000$$

$$\text{GBW} = A_V f_2 = 10000 \times 80$$

$$\boxed{\text{GBW} = 800000}$$

ii) for $A_V = 60 \text{ dB}$, $f_2 = 800 \text{ Hz}$

$$A_V = \log_{10}^{-1} \left(\frac{60}{20} \right)$$

$$A_V = 1000$$

$$\text{GBW} = A_V f_2 = 1000 \times 800 \text{ Hz}$$

$$\boxed{\text{GBW} = 800000}$$

iii) for $A_V = 1$ & $f_2 = f_u = 800 \text{ kHz}$

$$\text{GBW} = A_V f_u = 1 \times 800 \times 10^3$$

$$\boxed{\text{GBW} = 800000}$$



Unity - gain frequency (f_u) :-

The frequency at which $A_v=1$ is called unit gain frequency denoted as ' f_u '.

Unity - gain bandwidth :-

$$f_u = A_v f_2$$

The gain bandwidth corresponding to f_u is also called unity gain bandwidth.

$$f_2 = \frac{f_u}{A_v}$$

- * Determine the gain-bandwidth product, estimate the upper cut-off frequencies for the 741 op-amp with $A_v=100$.

Given :- $A_v = 100$.

For 741 op-amp unity gain frequency $f_u = 800\text{ KHz}$
i.e. $A_v = 1$ at $f_u = 800\text{ KHz}$.

Sol : WKT $f_u = A_v f_2$

$$f_2 = \frac{f_u}{A_v} = \frac{800\text{ KHz}}{100}$$

$$f_2 = 8\text{ KHz}$$



Using the gain-bandwidth product, estimate the upper cut-off frequencies for a Non-INV amplifier with $A_v = 100$ ① When a 741 op-amp is used and.

Given :- $A_v = 100$

Sol :-

① For 741 op-amp : $f_u = 800 \text{ kHz}$

$$\text{WKT} \quad f_2 = \frac{f_u}{A_v} = \frac{800 \text{ kHz}}{100}$$

$$f_2 = 8 \text{ kHz}$$

* Determine the upper cut-off frequency for ② a voltage follower ckt using a 741 op-amp and ③ a unity gain INV amplifier using a 741 op-amp.

Sol :-

② In voltage follower gain $A_v = 1$

for 741 op-amp : $f_u = 800 \text{ kHz}$

$$\text{WKT} \quad f_u = f_2 \cdot A_v$$

$$f_2 = \frac{f_u}{A_v} = \frac{800 \text{ kHz}}{1}$$

$$f_2 = 800 \text{ kHz}$$

③ for unity gain INV amplifier

$$R_1 = R_2$$

WKT the gain is given by

$$A_v = \frac{R_1 + R_2}{R_1} = \frac{R_1 + R_1}{R_1} = \frac{2R_1}{R}$$

$$A_v = 2$$



$f_{o2} = 41 \text{ op-amp } f_u = 800 \text{ kHz.}$

$$f_2 = \frac{f_u}{A_V} = \frac{800 \text{ kHz}}{2}$$

$f_2 = 400 \text{ kHz}$

NOTE :-

The calculation of upper cut-off frequency holds good only for small signals with o/p voltage being less than $\pm 1V$.



Slew Rate Effects :-

Define slew rate of an op-amp. Show how the slew rate of an op-amp can produce distortion in a sinusoidal op waveform. Also explain how the slew rate can limit the amplitude of the distortion free sine wave op for a given op-amp cut-off frequency.

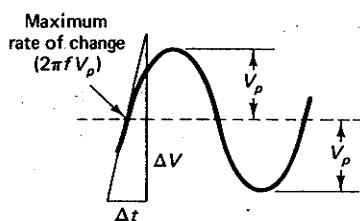
June - 10, 6M (EE)

Sol :-

Slew rate : The slew rate 's' of an op-amp is the maximum rate at which the op voltage can change.

$$\text{i.e. } S = \frac{dV_o}{dt} \Big|_{\text{max.}}$$

- * For large signals, the upper cut-off frequency will be much lower than the small signal circuits. This is due to the op-amp slew rate.



(a) Sine wave maximum rate of change

P.T.O



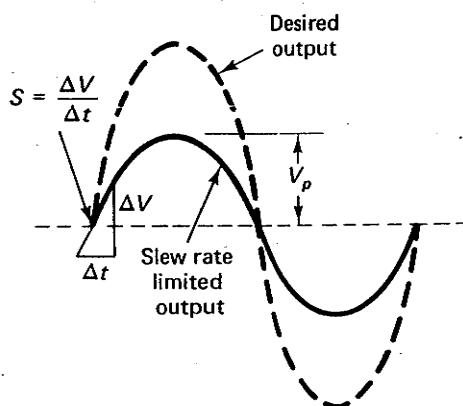
Fig 1 (b) shows a sinusoidal op-amp voltage waveform from an op-amp. It is observed that the fastest rate of change of voltage occurs when the waveform crosses zero.

At this point, maximum rate of change is given by:

$$\text{Maximum rate of change} = 2\pi f V_p \text{ volt/sec}$$

Where $f \rightarrow$ frequency of the signal &

$V_p \rightarrow$ peak amplitude of the signal.



(b) Sine wave output amplitude can be limited by the op-amp slew rate

Fig 1 (b) shows the distorted waveform that occurs when the slew rate is too slow for the op-amp amplitude & frequency.

- * For a distortion-free op-amp, the op-amp slew rate 'S' must be equal to, or greater than, the maximum rate of change of the waveform.

$$\therefore S = 2\pi f V_p$$

- * The slew rate-limited frequency for a given op-amp amplitude is.

$$f_s = \frac{S}{2\pi V_p}$$



* The slew rate-limited o/p amplitude for a given cut-off frequency ' f_s ' is

$$V_p = \frac{s}{2\pi f_s}$$

1) ① calculate the slew-rate-limited cut off frequency for a voltage follower ckt using a 741 op-amp if the peak of sine wave o/p is to be 5V.

⑤ determine the maximum peak value of the sinusoidal o/p voltage that will allow the 741 voltage follower ckt to operate at the 800kHz unity gain cut off frequency.

⑥ calculate the maximum peak value of sine wave o/p voltage that can be produced by the amplifier for op-amp 741 having upper cut-off frequency 8kHz.

Sol :-

① Given $V_p = 5V$, $f_s = ?$

for 741 op-amp : $s = 0.5 V/\mu s$

NOTE:-

$$s = 0.5 V/\mu s$$

$$\text{i.e. } s = \frac{0.5 V}{1 \times 10^6}$$

$$\text{WKT } f_s = \frac{s}{2\pi V_p} = \frac{0.5 V / \mu s}{2\pi \times 5V} = \frac{0.5 V}{2\pi \times 5V \times 10^6}$$

$$f_s = 15.9 \text{ kHz}$$

② $f_s = 800 \text{ kHz}$, $V_p = ?$

for 741 op-amp : $s = 0.5 V/\mu s$



$$\text{WKT} \quad V_p = \frac{s}{2\pi f_2} = \frac{0.5 \text{ V / ms}}{2\pi \times 800 \text{ kHz}} = \frac{0.5 \text{ V}}{2\pi \times 800 \text{ kHz} \times 10^6}$$

$$V_p = 99 \text{ mV}$$

① Given : $f_2 = 8 \text{ kHz}$

for 741 op-amp : $f_2 = 8 \text{ kHz}$ & $s = 0.5 \text{ V / ms}$.

$$\text{WKT} \quad V_p = \frac{s}{2\pi f_2} = \frac{0.5 \text{ V / ms}}{2\pi \times 8 \text{ kHz}} = \frac{0.5 \text{ V}}{2\pi \times 8 \text{ kHz} \times 10^6}$$

$$V_p = 9.9 \text{ V}$$

2) Determine

- i) The slew-rate limited cut-off frequency for a voltage follower ckt using a LM 353 op-amp if the peak of sine wave op is to be 6.5 Volt.
- ii) The maximum peak value of the sinusoidal op voltage that will allow the LM 353-A . voltage follower circuit to operate at the 4MHz unity-gain cut-off frequency.
- iii). The maximum peak value of sinewave op voltage that can be produced by the amplifier having $f_2 = 250 \text{ kHz}$. Assume slew rate = 13V / ms.

Soln-

i) Given : $V_p = 6.5 \text{ V}$, $s = 13 \text{ V / ms}$.

$$\text{WKT} \quad f_s = \frac{s}{2\pi V_p} = \frac{13 \text{ V}}{2\pi \times 6.5 \times 10^6}$$

$$\therefore f_s = 318.31 \text{ kHz}$$



ii) Given :

Unity gain cutoff frequency i.e. $f_Q = 4 \text{ kHz}$

$$\text{WKT} \quad V_p = \frac{S}{2\pi f_Q} = \frac{13 \text{ V}}{2\pi \times 4 \text{ kHz} \times 10^6}$$

$$\therefore V_p = 0.52 \text{ V}$$

iii) Given : $f_Q = 250 \text{ kHz}$.

$$\text{WKT} \quad V_p = \frac{S}{2\pi f_Q} = \frac{13}{2\pi \times 250 \text{ kHz} \times 10^6}$$

$$\therefore V_p = 8.28 \text{ Volts.}$$

3) Define the Slew rate and determine the Slew rate limited cut-off frequency for a 741 based voltage follower. The peak Sinewave o/p should be 10V. Given; Slew rate of 741 is 0.5 V/sec.

Dec - 10, 4M

The Slew rate 'S' of an op-amp is the maximum rate at which the o/p voltage can change.

$$S = \left. \frac{dV_o}{dt} \right|_{\text{max}} \quad \leftarrow \quad 1 \text{M}$$

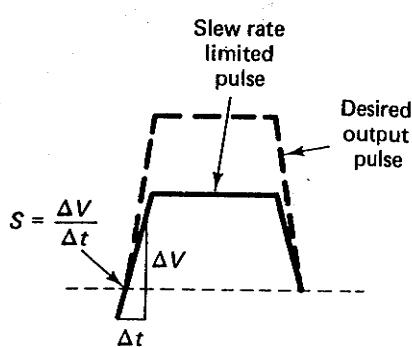
Given :- $S = 0.5 \text{ V/sec.}, V_p = 10 \text{ V.}$

$$f_s = \frac{S}{2\pi V_p} = \frac{0.5 \text{ V/sec.}}{2\pi \times 10}$$

$$f_s = 7.95 \text{ kHz} \quad \leftarrow \quad 3 \text{M}$$



Slew rate effect on o/p pulse rise time & amplitude :-



A pulse output waveform can be limited by the op-amp slew rate

Cut-off frequency limited rise time :-

When a pulse-type signal is to be amplified the o/p rise time is related to the circuit cut-off frequency. The equation for cut-off frequency limited rise time is

$$t_{\alpha}(f_2) = \frac{0.35}{f_2}$$

Slew rate limited rise time :-

When a pulse waveform is distorted by the op-amp slew rate, the o/p rise time and the amplitude are directly related to the slew rate & is given by :

$$t_{\alpha}(s) = \frac{V_p}{S}$$



- * @ calculate the cut-off frequency - limited rise time for a voltage follower ckt using a 741 op-amp. Also determine the slew rate - limited rise time if the opamp amplitude is to be 5V.
- ⑥ Determine the maximum undistorted pulse opamp amplitude for the 741 voltage follower if the opamp rise time is not to exceed 1μs.
- ⑦ calculate the minimum opamp rise time & the maximum pulse amplitude at that rise time for a 741 amplifier with an upper cutoff frequency of 100 kHz.

Sol :-

- a) For 741 op-amp : i) Upper cut-off frequency $f_2 = 800 \text{ kHz}$
ii) $s = 0.5 \mu\text{s/V}$.

Given : $V_p = 5 \text{ V}$, $t_{\alpha}(f_2) = ?$, $t_{\alpha(s)} = ?$

$$\text{WKT. } t_{\alpha}(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800 \text{ kHz}}$$

$$t_{\alpha}(f_2) = 0.4 \mu\text{s}$$

$$t_{\alpha(s)} = \frac{V_p}{s} = \frac{5 \text{ V}}{0.5 \text{ V}/\mu\text{s}}$$

$$t_{\alpha(s)} = 10 \mu\text{s}$$

- b) Given : $V_p = ?$, $t_{\alpha(s)} = 1 \mu\text{s}$, $s = 0.5 \text{ V}/\mu\text{s}$.

$$V_p = t_{\alpha(s)} \cdot s = 1 \mu\text{s} \times 0.5 \text{ V}/\mu\text{s}$$

$$V_p = 0.5 \text{ V}$$



② Given : $f_2 = 100 \text{ kHz}$

$$\text{WKT} \quad t_R(f_2) = \frac{0.35}{f_2} = \frac{0.35}{100 \text{ kHz}}$$

$$t_R(f_2) = 3.5 \mu\text{s}$$

$$\text{WKT. } V_p = t_R(s) \cdot S = 3.5 \mu\text{s} \times 0.5 \text{ V}/\mu\text{s}$$

$$V_p = 1.75 \text{ V}$$

- * calculate the cut-off frequency limited slew rate time for a voltage follower ckt using a 741 op-amp. Also determine the slew rate limited slew time if the off amplitude is 4V.

Given : For 741 op-amp : $f_2 = 800 \text{ kHz}$, $S = 0.5 \text{ V}/\mu\text{s}$

$$V_p = 4 \text{ V}$$

- * cut off frequency limited slew time

$$t_R(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800 \text{ kHz}}$$

$$t_R(f_2) = 0.4 \mu\text{s}$$

- * slew rate limited slew time.

$$t_R(s) = \frac{V_p}{S} = \frac{4}{0.5 \text{ V}/\mu\text{s}}$$

$$t_R(s) = 8 \mu\text{s}$$



* calculate the slew rate - limited cut off frequency for a voltage follower ckt using a 741 op-amp, if the peak of Sinewave op is to be 6V. Determine the maximum peak value of the sinusoidal op voltage that will allow the 741 voltage follower circuit to operate at 800kHz. Unity gain cut-off frequency.

Given : $S = 0.5 \text{ V}/\mu\text{s}$

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* Slew rate - limited cut-off frequency :-

$$\text{WKT} \quad f_s = \frac{S}{2\pi V_p} = \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 6\text{V}} = \frac{0.5 \text{ V}}{2\pi \times 6\text{V} \times 10^{-6}}$$

$$f_s = 13.26 \text{ kHz}$$

← (2M)

* Maximum peak value :-

$$V_p = \frac{S}{2\pi f_2} = \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 800 \text{ kHz}} = \frac{0.5 \text{ V}}{2\pi \times 800 \text{ kHz} \times 10^{-6}}$$

$$V_p = 99 \text{ mV}$$

← (2M)



* Determine the upper cut off frequency & the maximum distortion-free o/p amplitude for a voltage follower :

- i) When a 741 op-amp is used and
- ii) When an LF353 op-amp is used.

For 741 : $f_2 = 800 \text{ kHz}$, $S = 0.5 \text{ V/msec}$.

For LF353 : $f_2 = 5 \text{ MHz}$, $S = 13 \text{ V/msec}$.

June -08, 6M

SOL :-

for 741 op-amp :

$$\times t_d(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800 \text{ kHz}}$$

$$t_d(f_2) = 0.44 \text{ msec} \quad \leftarrow \boxed{1\frac{1}{2} \text{ M}}$$

$$\times V_p = t_d(f_2) \times S = 0.44 \cancel{\text{msec}} \times 0.5 \text{ V/msec}$$

$$V_p = 220 \text{ mV} \quad \leftarrow \boxed{1\frac{1}{2} \text{ M}}$$

for LF353 op-amp :

$$\times t_d(f_2) = \frac{0.35}{f_2} = \frac{0.35}{5 \text{ MHz}}$$

$$t_d(f_2) = 70 \text{ ns} \quad \leftarrow \boxed{1\frac{1}{2} \text{ M}}$$

$$\begin{aligned} \times V_p = t_d(f_2) \times S &= 70 \text{ ns} \times 13 \text{ V/msec.} \\ &\approx 70 \times 10^{-9} \times \frac{13 \text{ V}}{10^6} \end{aligned}$$

$$V_p = 910 \text{ mV} \quad \leftarrow \boxed{1\frac{1}{2} \text{ M}}$$



* An op-amp has a unity cross-over frequency of 1MHz. calculate the upper cut off frequency in the following cases :-

- i) INV amplifier with $A_{vc} = 100 \text{ dB}$.
- ii) Non-INV amplifier with $A_{vc} = 50 \text{ dB}$
- iii) Voltage follower :
show these on the frequency response plot if $A_v = 120 \text{ dB}$.

Jan - 09, 4M

Given : $f_u = 1 \text{ MHz}$

Sol :-

- i) INV amplifier : $A_{vc} = 100 \text{ dB}$

$$(A_{vc})_{\text{dB}} = 20 \log_{10} (A_{vc})$$

$$A_{vc} = \log_{10} \left(\frac{100 \text{ dB}}{20} \right)$$

$$A_{vc} = 100000.$$

WKT $f_2 = \frac{f_u}{A_{vc}} = \frac{1 \text{ MHz}}{100000}$

$$f_2 = 10 \text{ Hz} \quad \leftarrow 1 \text{ M}$$

- ii) Non-INV amplifier : $A_{vc} = 50 \text{ dB}$.

$$A_{vc} = \log_{10} \left(\frac{50 \text{ dB}}{20} \right)$$

$$A_{vc} = 316.227$$



WKT $f_2 = \frac{f_u}{A_v} = \frac{1\text{MHz}}{316.22}$

$$f_2 = 3.162 \text{ kHz} \quad \leftarrow 1\text{M}$$

ii) Voltage follower :-

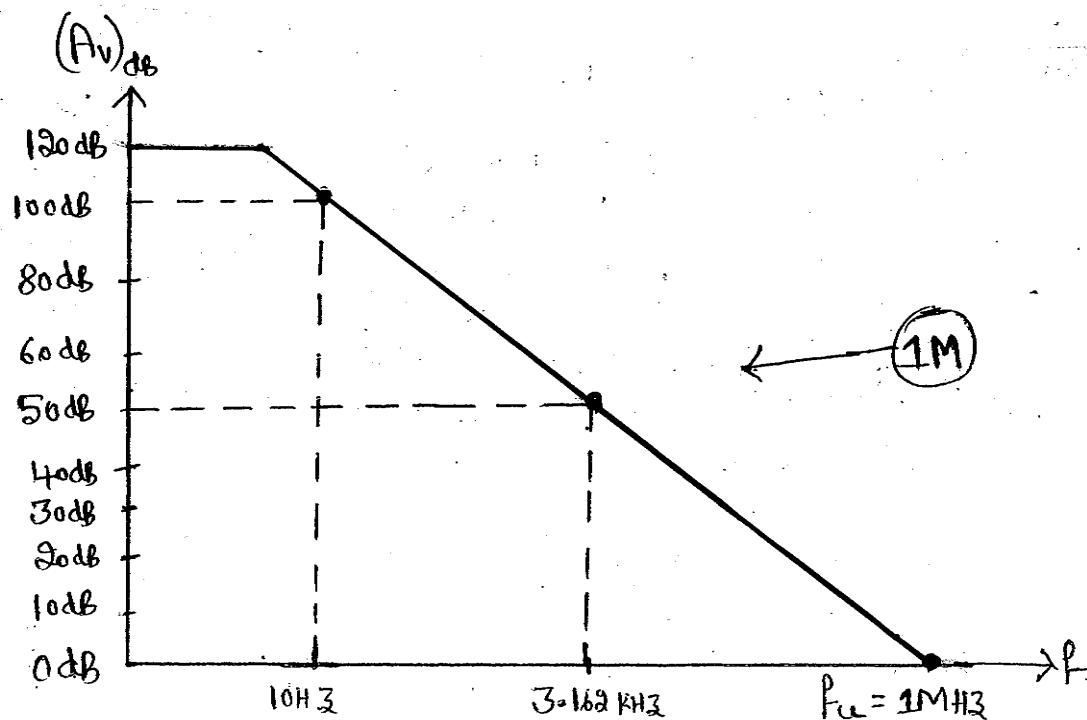
for voltage follower $A_v = 1$

$$(A_v)_{\text{dB}} = 20 \log_{10}(1)$$

$$(A_v)_{\text{dB}} = 0$$

WKT $f_2 = \frac{f_u}{A_v} = \frac{1\text{MHz}}{1}$

$$f_2 = 1\text{MHz} \quad \leftarrow 1\text{M}$$



* i) calculate the slew rate limited cut off frequency for a voltage follower circuit using a 741 op-amp if the peak of sinewave o/p is to be 5V.

← Model paper - I , 4M

ii) determine the maximum peak value of the sinusoidal o/p voltage that will allow the 741 voltage follower ckt to operate at 800 kHz. unity gain cutoff frequency.

Model paper - II , 6M

Given :- $V_p = 5V$

i) For 741 op-amp : $S = 0.5 \text{ V/ \mu sec}$, $f_2 = 800 \text{ kHz}$

$$* \text{ WKT } t_{\alpha}(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800 \text{ kHz}}$$

$$t_{\alpha}(f_2) = 0.4375 \text{ \mu sec}$$

$$* t_{\alpha}(s) = \frac{V_p}{S} = \frac{5V}{0.5V/\mu \text{sec}}$$

$$t_{\alpha}(s) = 10 \mu \text{sec}$$

ii) $f_2 = 800 \text{ kHz}$.

$$t_{\alpha}(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800 \text{ kHz}}$$

$$t_{\alpha}(f_2) = 0.4375 \text{ \mu sec}$$

$$V_p = t_{\alpha}(s) \times S = t_{\alpha}(f_2) \times S = 0.4375 \mu \text{sec} \times \frac{0.5V}{\mu \text{sec}}$$

$$V_p = 0.218V$$



* Determine

- i) the slew rate limited cutoff frequency for a voltage follower ckt using a LM353A op-amp if the peak of sine wave op is to be 6.5 Volts.
- ii) the maximum peak value of the sinusoidal op. voltage that will allow the LM353-A voltage follower ckt to operate at the 4MHz Unity-gain cutoff freq.
- iii) the maximum peak value of sine wave op voltage that can be produced by the amplifier having $f_2 = 250\text{kHz}$. Assume slew rate = 13V/μs.

Sol:-

i) Given: $s = 13\text{V}/\mu\text{s}$, $V_p = 6.5\text{V}$, $f_S = ?$

$$f_S = \frac{s}{2\pi V_p} = \frac{13\text{V}/\mu\text{s}}{2\pi \times 6.5\text{V}} = \frac{13\text{V}}{2\pi \times 6.5\text{V} \times 10^6}$$

$$f_S = 318.31\text{kHz}$$

ii) Given: $s = 13\text{V}/\mu\text{s}$, unity gain frequency. $f_2 = 4\text{MHz}$

$$V_p = \frac{s}{2\pi f_2} = \frac{13\text{V}/\mu\text{s}}{2\pi \times 4 \times 10^6} = \frac{13\text{V}}{2\pi \times 4 \times 10^6 \times 10^6}$$

$$V_p = 0.52\text{V}$$

iii) Given: $f_2 = 250\text{kHz}$, $s = 13\text{V}/\mu\text{s}$.

$$V_p = \frac{s}{2\pi f_2} = \frac{13\text{V}/\mu\text{s}}{2\pi \times 250\text{kHz}} = \frac{13\text{V}}{2\pi \times 250\text{kHz} \times 10^6}$$

$$V_p = 8.28\text{ Volts}$$



* calculate :

- i) the cutoff frequency limited rise time for a voltage follower using LM 353A op-amp. Also find the slew rate - limited rise time if the opamp amplitude is to be 6.5 Volts.
- ii) the maximum undistorted pulse opamp amplitude for LM 353A voltage follower if the opamp rise time is not to exceed 0.8 μsec.
- iii) the minimum opamp rise time & the maximum pulse amplitude at that rise time for a LM 353A amplifier with an upper cutoff frequency of 400 kHz.

[Assume $f_u = 4\text{MHz}$ and $s = 13\text{V}/\mu\text{sec}$ for LM 353A op-amp].

Given:

i) $V_p = 6.5\text{V}$, $f_u = 4\text{MHz}$, $s = 13\text{V}/\mu\text{sec}$.

$$t_R(f_2) = \frac{0.35}{f_2} = \frac{0.35}{4 \times 10^6} = 87.5\text{nsec}$$

$t_R(f_2) = 87.5\text{nsec}$

$$t_R(s) = \frac{V_p}{s} = \frac{6.5\text{V}}{13\text{V}/\mu\text{sec}}$$

$t_R(s) = 0.5\mu\text{sec}$

ii) $V_p = t_R(s) \cdot s = (0.8 \times 10^{-6})(13\text{V}/\mu\text{sec}) = \frac{0.8 \times 10^{-6} \times 13\text{V}}{10^6}$

$V_p = 10.4\text{V}$

iii) Given :- $f_2 = 400\text{kHz}$.

$$t_R(f_2) = \frac{0.35}{f_2} = \frac{0.35}{400 \times 10^3}$$



$$t_{\alpha}(f_2) = 0.875 \mu s$$

$$V_p = t_{\alpha}(f_2) S = 0.875 \mu s \times 13V / \mu s$$

$$\geq 0.875 \mu s \times \frac{13V}{10^6}$$

$$V_p = 11.375 \text{ Volts}$$

* calculate the minimum rise time and maximum undistorted op-p pulse amplitude at that rise time for an amplifier with closed loop gain 50, using a 741 op-amp.

[Jan -08, 4M (EE)]

[Jan -05, 6M (EE)]

Given : $A_v = 50$.

for 741 op-amp : $f_u = 800 \text{ KHz}$.

Sol : $f_2 = \frac{f_u}{A_v} = \frac{800 \text{ KHz}}{50}$

$$f_2 = 16 \text{ KHz}$$

* $t_{\alpha}(f_2) = \frac{0.35}{f_2} = \frac{0.35}{16 \text{ KHz}}$

$$t_{\alpha}(f_2) = 21.875 \mu \text{sec}$$

* $V_p = S \times t_{\alpha}(f_2) = \frac{0.5V}{\mu s} \times 21.875 \mu \text{sec}$

$$V_p = 10.9375 \text{ V}$$



* calculate the slew rate limited cut-off frequency for a voltage follower circuit using 741 op-amp. The peak value of the sinewave op is to be 5V. The slew rate of op-amp is $0.5 \text{ V}/\mu\text{s}$. Determine the maximum peak value of the sinusoidal op voltage that will allow the voltage follower circuit to operate at 500kHz unity gain cutoff frequency.

June -07, 6M(EE)

Given :- $S = 0.5 \text{ V}/\mu\text{s}$, $V_p = 5\text{V}$.

$$\text{i)} \quad t_{\alpha}(s) = \frac{V_p}{S} = \frac{5\text{V}}{0.5 \text{ V}/\mu\text{s}}$$

$t_{\alpha}(s) = 10 \mu\text{s.}$

ii) $f_2 = 500 \text{ kHz.}$

$$t_{\alpha}(f_2) = \frac{0.35}{f_2} = \frac{0.35}{500 \text{ kHz.}}$$

$t_{\alpha}(f_2) = 0.7 \mu\text{sec}$

* $V_p = t_{\alpha}(f_2) S = 0.7 \mu\text{sec} \times 0.5 \text{ V}/\mu\text{sec.}$

$V_p = 0.35 \text{ V}$



* A 741 with a slew rate of $0.5 \text{ V}/\mu\text{s}$ is used as a voltage follower.

i) Calculate the slew rate limited cutoff frequency if the sine wave op is 5 Volts.

ii). If the ckt is to operate with a unity gain cutoff frequency of 800 kHz, calculate the maximum peak value of the sinusoidal op voltage.

iii). If the upper cutoff frequency is 8 kHz, calculate the maximum. value of the peak op voltage.

June - 06, 6M (EE)

Sol :-

i) Given : $S = 0.5 \text{ V}/\mu\text{s}$, $V_p = 5 \text{ V}$

$$f_s = \frac{S}{2\pi V_p} = \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 5 \text{ V}} = \frac{0.5 \text{ V}}{2\pi \times 5 \times 10^6}$$

$$f_s = 15.915 \text{ kHz}$$

ii) $f_2 = f_3 = 800 \text{ kHz}$.

$$V_p = \frac{S}{2\pi f_s} = \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 800 \text{ kHz}} = \frac{0.5 \text{ V}}{2\pi \times 800 \text{ kHz} \times 10^6}$$

$$V_p = 99.47 \text{ mV.}$$

iii) $f_2 = f_3 = 8 \text{ kHz}$.

$$V_p = \frac{S}{2\pi f_s} = \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 8 \text{ kHz}} = \frac{0.5 \text{ V}}{2\pi \times 8 \text{ kHz} \times 10^6}$$

$$V_p = 9.947 \text{ V}$$



- * Determine the upper cut-off frequency for
- a voltage follower using a 741 op-amp and
 - a unity gain inverting amplifier using a 741 op-amp
unity gain frequency for 741 op-amp is 800 kHz.

Sol: Given: $f_u = 800 \text{ kHz}$

- i) For voltage follower

$$A_V = 1$$

$$f_2 = \frac{f_u}{A_V} = \frac{800 \text{ kHz}}{1}$$

$$f_2 = 800 \text{ kHz}$$

- ii) For Non-INV amplifier gain

$$A_V = 1 + \frac{R_2}{R_1}$$

For unity gain INV amplifier $R_f = R_s$

$$A_V = 1 + \frac{R_1}{R_f}$$

$$A_V = 2$$

$$f_2 = \frac{f_u}{A_V} = \frac{800 \text{ kHz}}{2}$$

$$f_2 = 400 \text{ kHz}$$



* A square wave of amplitude 500 mV is to be amplified to 3V amplitude (both peak to peak). The specified rise time should be 4 μ sec. or less. Can 741 be used?

[Given SR for 741 = 0.5 V/ μ sec]

Given :- $S = 0.5 \text{ V}/\mu\text{sec}$, $V_i = 500 \text{ mV}$, $V_p(\text{P-P}) = 3 \text{ V}$
 $t_R = 4 \mu\text{sec}$.

Sol: Peak off $V_p = \frac{3 \text{ V}}{2}$

$$V_p = 1.5 \text{ V}$$

Slew rate : $S = \frac{\Delta V_o}{t} = \frac{1.5 \text{ V} - (-1.5 \text{ V})}{4 \mu\text{sec}}$

$$S = 0.7 \text{ V}/\mu\text{sec}$$

The op-amp 741 has slew rate of 0.5 V/ μ sec

* For the given parameter : $S = 0.75 \text{ V}/\mu\text{sec}$.

Hence 741 cannot be used.



* Determine the upper cutoff frequency and maximum distortion free op amp amplitude for a voltage follower when a 741 op-amp is used.

June - 10, 4M

Given:

For 741 op-amp : $f_2 = 800 \text{ kHz}$ & $S = 0.5 \text{ V}/\mu\text{s}$.

for voltage follower : $A_V \approx 1$

Sol :-

$$* t_{\alpha}(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800 \text{ kHz}}$$

$$t_{\alpha}(f_2) = 0.44 \mu\text{sec} \quad \leftarrow \quad \text{(Qm)}$$

$$* V_p = t_{\alpha}(f_2) \times S = 0.44 \mu\text{sec} \times 0.5 \text{ V}/\mu\text{sec}$$

$$V_p = 220 \text{ mV} \quad \leftarrow \quad \text{(Qm)}$$



Zin MOD compensation :-

- * Sketch and explain a circuit to show the Zin mod method of frequency compensation. State the application of the circuit. Jan -10, 8M

- * With a neat circuit diagram, explain Zin mod method of frequency compensation. Write the equation for the feedback factor Jan-09, 6M(EE) June-09, 8M

- * Explain how bandwidth increase by using Zin mod compensation. Jan-09, 8M

In order to increase the bandwidth of an op-amp ckt, input impedance modification 'Zin MOD' technique of frequency compensation is used.

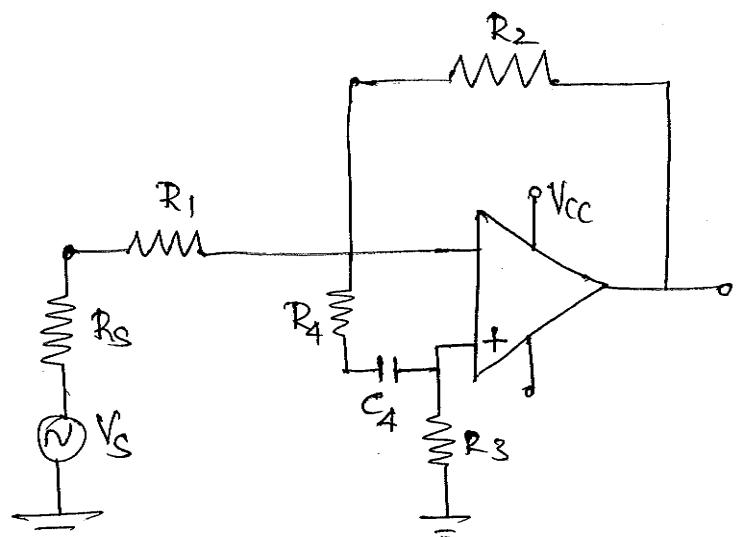


fig ①: R_4 & C_4 are used at the op-amp input to alter the ckt loop gain.

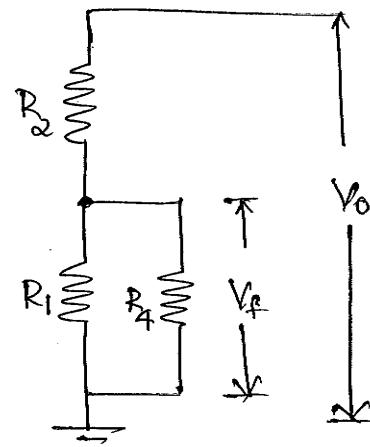


fig ② Neglecting R_3 & R_4 , the feedback N/W is changed by Zin MOD.



* Fig @ shows INV amplifier ckt in which R_4 & C_4 are connected across the op-amp I/O terminals.

The capacitor C_4 acts as a open ckt to dc & parallel (coupled) ac signal.

The impedance of C_4 i.e X_{C4} is selected much smaller than the resistance of R_4 at the frequency at which $M_P = 1$ ($X_{C4} \ll R_4$).

* At oscillation frequency of the ckt, R_4 appears in parallel ($C_4 \rightarrow$ acts as short ckt) with R_1 to give feedback N/W as shown in fig ⑥.

For simplicity, R_3 is assumed to be a short ckt and R_S is taken to be much smaller than R_1 (i.e. $R_S \ll R_1$).

* Without R_4 & C_4 in the ckt, the feedback factor is

$$\boxed{\beta = \frac{R_1}{R_1 + R_2}}$$

* with R_4 in the ckt, the feedback factor becomes

$$\boxed{\beta' = \frac{R_1 || R_4}{(R_1 || R_4) + R_2}} \quad \therefore (R_1 || R_4)$$

Thus the voltage feedback from the o/p to the I/O is attenuated by the presence of R_4 .

* for the ckt stability, the op-amp gain is now.

$$\frac{1}{\beta'} = \frac{(R_1 || R_4) + R_2}{R_1 || R_4}$$



- * The voltage gain of INV amplifier remains

$$A_V = \frac{R_2}{R_1}$$

- * Without the use of R_4 & C_4 , the gain of the amplifier will be $A_V = \frac{1}{\beta}$. with the use of R_4 & C_4 $\beta' < \beta$. so that $\frac{1}{\beta'}$ is more.

The compensating components are actually selected according to higher gain. This increases the bandwidth.

- * Due to presence of R_4 & C_4 . Input impedance of op-amp is modified hence the method is called Z_{in} mod compensation.
- * The Z_{in} Impedance is very high and is given by

$$Z_{in} = (1 + MB) (Z_{in} \parallel R_4)$$



Q) List the precautions that should be observed for op-amp circuit stability. Briefly explain each.

June -08, 8M

Jan -10, 4M

June -10, 8M

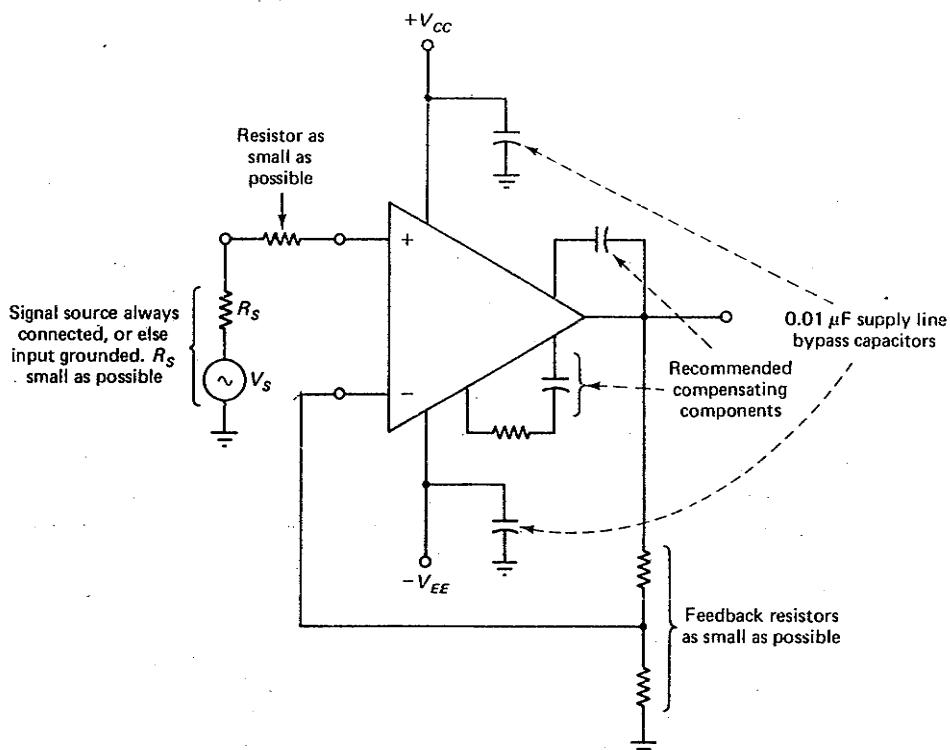


Figure For operational amplifier circuit stability, use the manufacturer's recommended compensating components, keep all resistor values to a minimum, connect $0.01 \mu F$ capacitors to bypass the supply lines to ground, and always have the signal source connected.

The following list of precautions should be observed for op-amp ckt stability:

- 1) For the low frequency applications, use an internally compensated op-amp like the 741.
- 2) When using an op-amp that must be compensated, use the manufacturer's recommended value & methods where possible use over-compensation.



3) Keep all component leads as short as possible, and take care with component placement.

Resistors connected to the op-amp I/p terminals should have the body of the resistor placed close to the I/p terminals.

4) Use 0.01 μ F high frequency capacitors to bypass the supply terminals (V_{cc} & $-V_{ee}$) to ground. Connect these capacitors close to the IC terminals.

5) Always connect signal source to the ckt or ground the ckt I/p (i.e. Do not keep source open ckted).

6) Do not connect oscilloscopes or other instruments at the op-amp input terminals (INV or Non-IN V I/p).

7) If a circuit is unstable after all of the above precautions have been observed, reduce the value of all circuit resistors. Also reduce the signal source resistance if possible.

If necessary, try compensating for stray capacitance or load capacitance.

8) For increasing circuit bandwidth, use Zin mod compensation.



Non-Linear circuit Applications

Crossing detectors :-

- * What is zero crossing detector.

Whenever op-amp is operated in the open-loop mode & everytime an input signal crosses zero, the op-amp will change its state either from $+V_{sat}$ to $-V_{sat}$ or Vice-versa.

Zero-crossing detectors are of two types:

- 1) Non-INV zero-crossing detector.
- 2) INV - zero-crossing detector.

Non-INV Zero-crossing detector :-

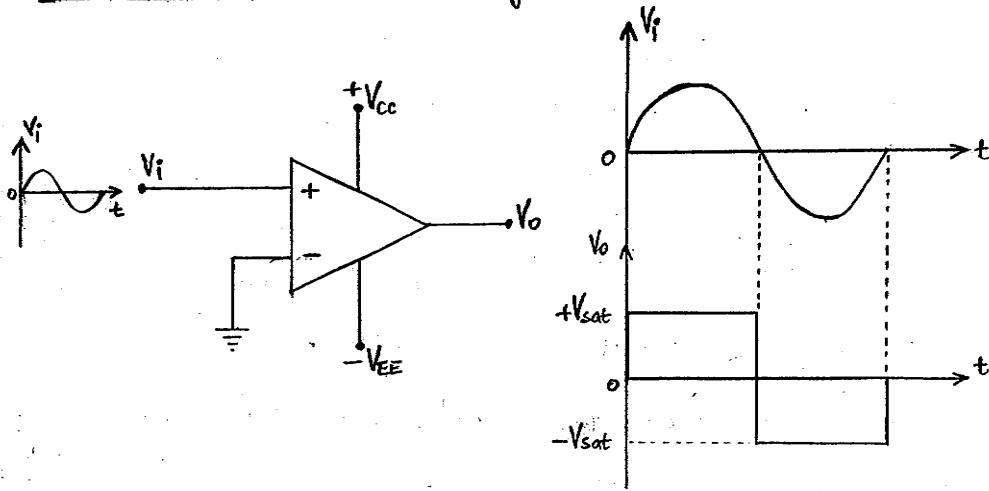


fig @ : Non-INV zero-crossing detector ckt.

- * The input voltage is applied to the NON-INV terminal & INV terminal is grounded.



When the input signal is positive, the o/p of the op-amp will be at $+V_{sat}$. When the input signal is negative, the o/p of the op-amp immediately switches to $-V_{sat}$.

thus when the input signal crosses the zero level, the o/p voltage switches from one saturation level to another i.e $+V_{sat}$ to $-V_{sat}$. so this ckt is called NON-INV zero crossing detector.

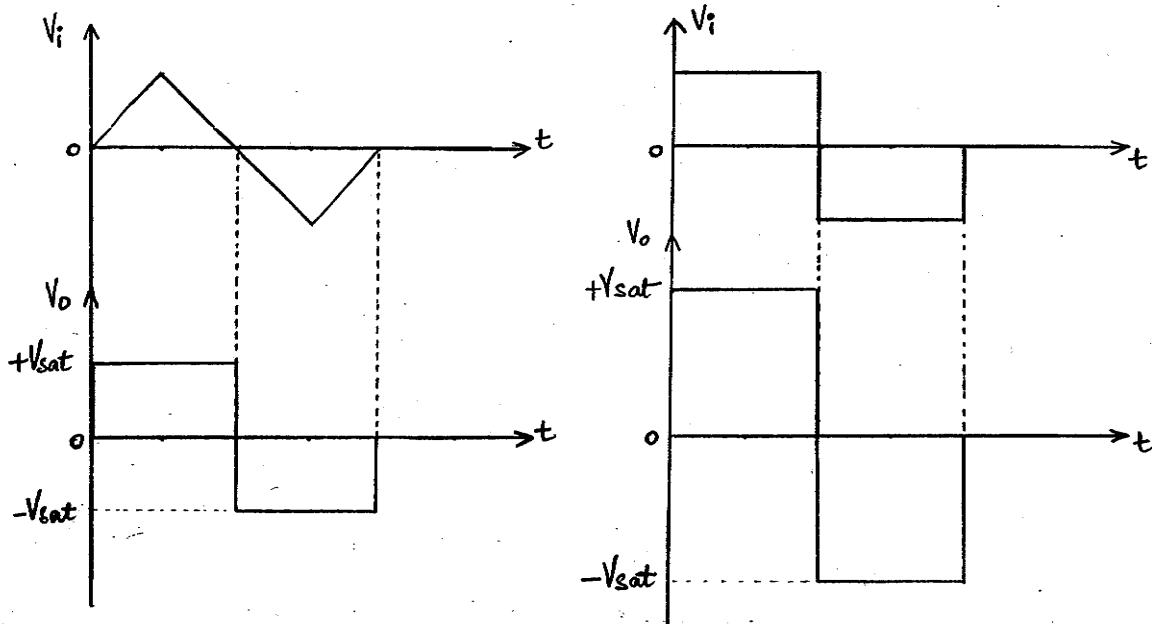
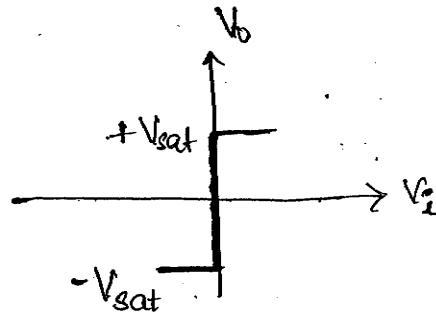


fig ⑤ I/O waveforms.

fig ⑤ show the o/p. waveforms that result for various I/P to a zero-crossing detector.

Regardless of the I/P wave shape, the o/p is always a rectangular waveform.

Transfer characteristic :-



INV Zero crossing detector :-

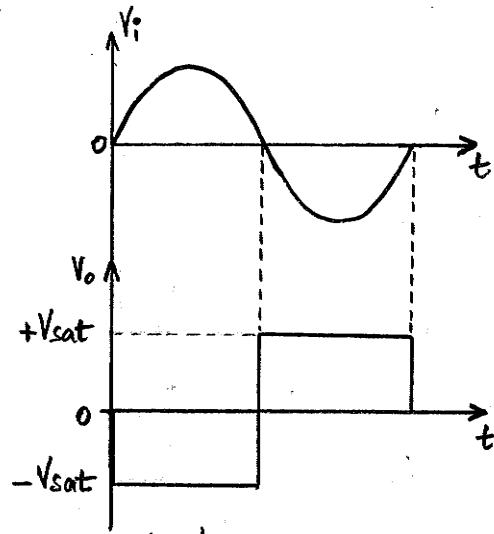
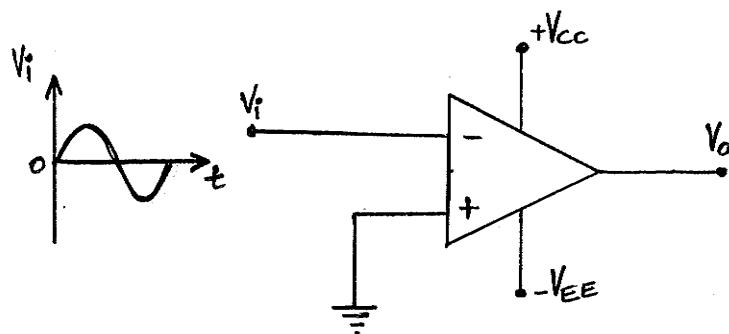
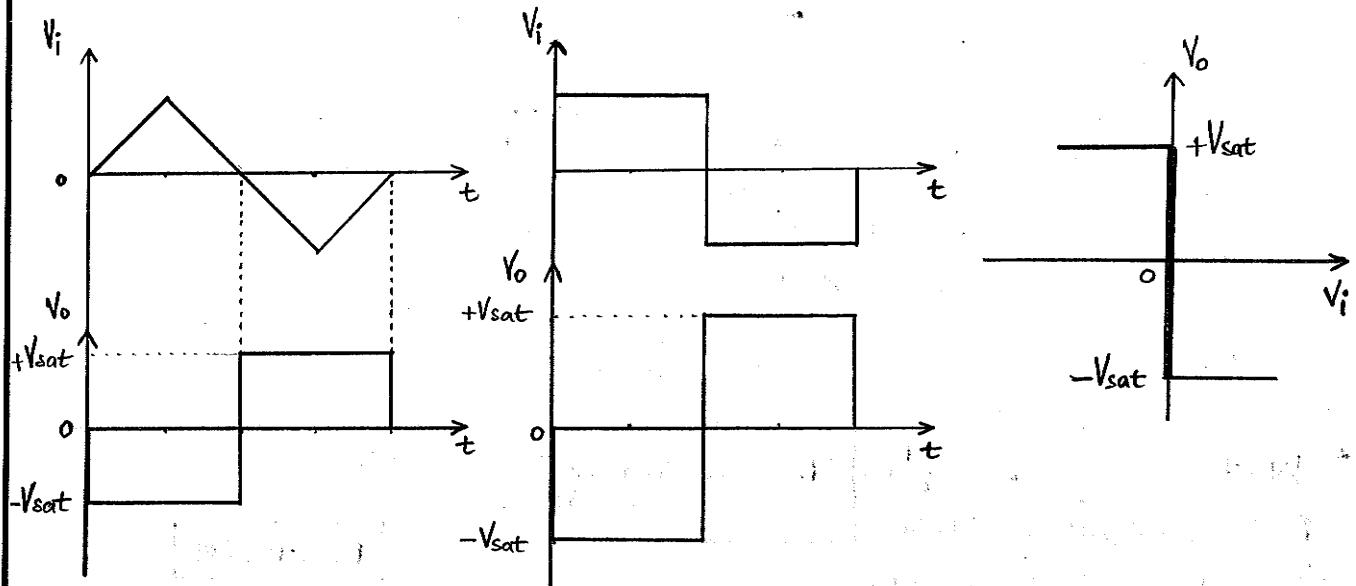


fig ① : INV zero-crossing detector

When the input signal is positive, the o/p of the op-amp will be at -Vsat. When the o/p signal is negative, the o/p of the op-amp immediately switches to +Vsat.

Thus when the input signal crosses the zero level, the o/p voltage switches from one saturation level to another i.e +Vsat to -Vsat. So this ckt is called INV - zero crossing detector. Sometimes termed as inverter.



Voltage - level detector : (Non-INV)

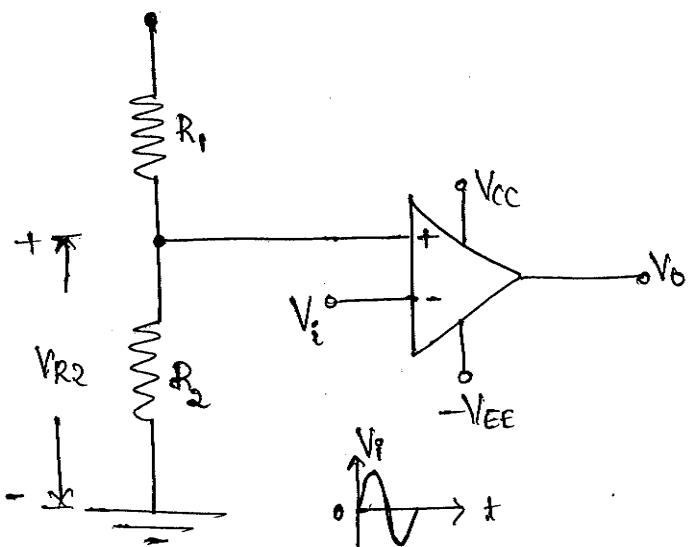


fig ① : voltage - level detector.

* Instead of biasing the Non-INV terminal to ground level it can be connected to a positive or negative dc voltage level as shown in fig ①. Here the op-amp changes each time input crosses the reference voltage. Thus this ckt is called a voltage level detector.

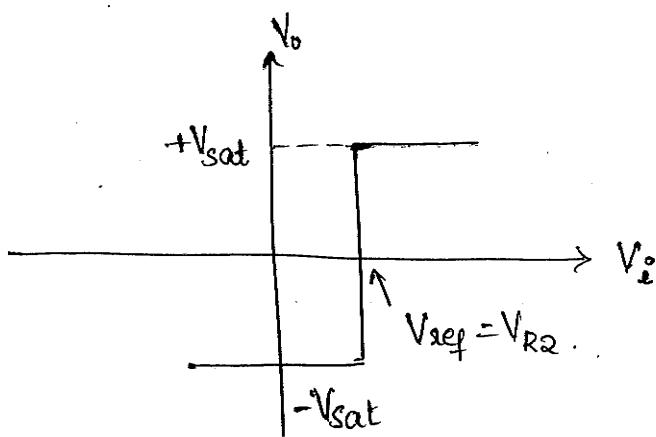


fig ② : Transfer characteristics.

* With waveforms, explain the working of :

- i) Zero-Crossing detector
- ii) voltage - level detector

Dec-10, 6M



Capacitor - Coupled crossing detector :-

* Explain working of capacitor coupled zero crossing detector, show waveforms at various points.

Jan-06, 6M(EE)

June-06, 6M(EE)

Jan-08, 88 M(EE)

June-09, 7M(EE)

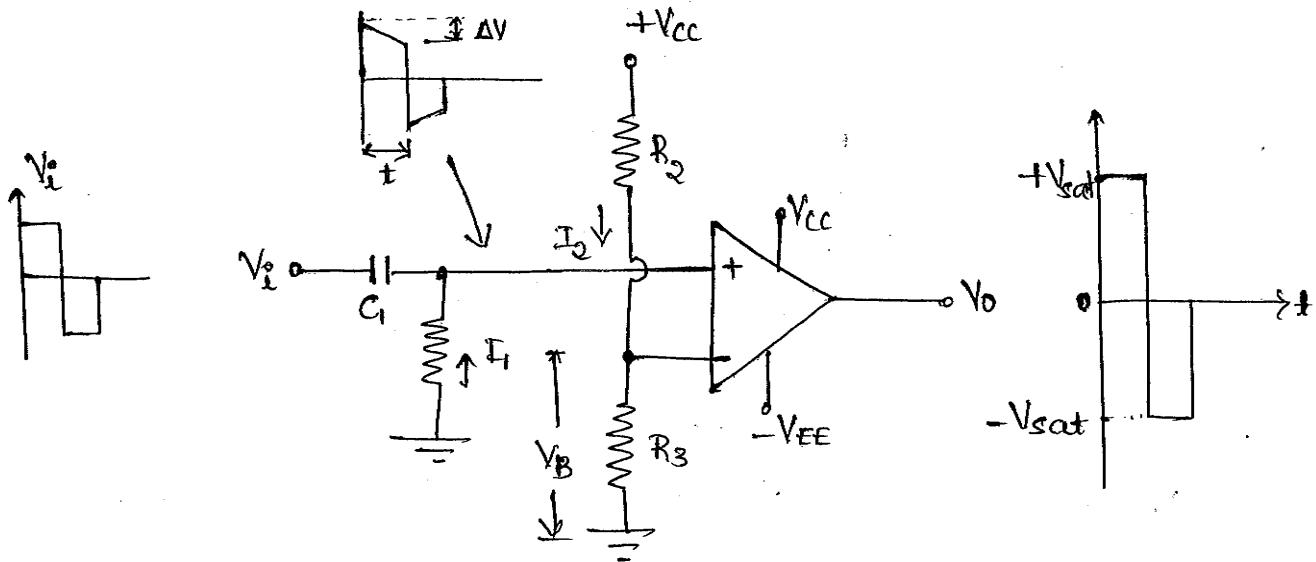


fig @ Capacitor coupled crossing detector.

fig @ shows capacitor coupled crossing detector with Non- INV terminal connected to ground via resistor R_1 to provide a dc bias current path to the op-amp.

The INV terminal connected to a potential divider ckt. Due to this INV terminal is held at a small +ve voltage (V_B). This ensures that the o/p is held at $-V_{sat}$, when no input signal is present.

* When capacitor -coupled signal (V_i) drives the Non - INV o/p terminal above V_B , the o/p switches to $+V_{sat}$ and when input is less than V_B (i.e. $V_i < V_B$) the o/p falls back to $-V_{sat}$.



- * The resistance R_1 is designed as

$$R_{1(\text{max})} = R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

- * The current I_2 is chosen to be about 100 times $I_{B(\text{max})}$

$$\therefore I_2 = 100 \times I_{B(\text{max})}$$

- * The voltage V_B across R_3 is given by:

$$V_B = I_2 R_3$$

$$R_3 = \frac{V_B}{I_2}$$

$$V_B = V_{R3} = 0.1 V$$

V_B is usually chosen to be about 0.1V.

- * Applying KVL from V_{CC} , R_2 & R_3 , we get

$$V_{CC} - I_2 R_2 - I_2 R_3 = 0.$$

$$V_{CC} - V_{R2} - V_B = 0.$$

$$V_{CC} = I_2 [R_2 + R_3]$$

$$V_{R2} = V_{CC} - V_B$$

$$R_2 + R_3 = \frac{V_{CC}}{I_2}$$

NOTE

$$V_B = V_{R3}$$

$$R_2 = \frac{V_{CC}}{I_2} - R_3$$

$$V_{R2} = V_{CC} - V_{R3}$$

$$\therefore R_2 = \frac{V_{R2}}{I_2}$$

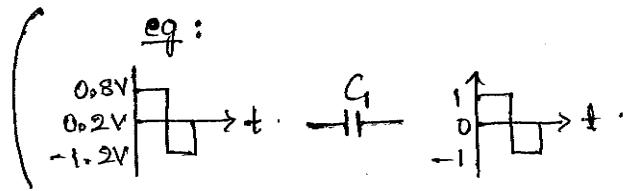
- * At lower frequency, X_{C1} should be much smaller than R_1 i.e

$$X_{C1} = \frac{R_1}{20}$$

$$\therefore C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{20} \right)}$$



- * The input voltage to capacitor 'C' may not be symmetrical above or below ground level, but it is always symmetrical on the op-amp side of C_1 .



- * When square wave is applied as an input to a capacitor-coupled detector, the waveform at the op-amp input terminal can develop considerable tilt as shown in fig ①.

- * The I_{IP} current is calculated as :

$$I_1 = \frac{V_i}{R_1}$$

(Note,
 $I_1 = \frac{V_i(\text{peak})}{R_1}$)

Assuming I_1 constant,

$$C_1 = \frac{I_1 t}{\Delta V}$$

where,

$$t = \frac{1}{2f}$$

$$\therefore T = t + t$$

$$T = 2t$$

$$t = \frac{T}{2}$$

$$t = \frac{1}{2f}$$

FORMULAEDesign steps :-

$$1) R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$2) \text{let } I_2 = 100 \times I_B(\text{max})$$

$$3) \text{Assume } V_B = V_{R3} = 0.1V$$

$$4) V_{R2} = V_{CC} - V_B$$

$$5) R_2 = \frac{V_{R2}}{I_2}$$

$$6) R_3 = \frac{V_{R3}}{I_2}$$

$$7) V_i(\text{peak}) = \frac{V_i(p-p)}{2}$$

$$8) I_1 = \frac{V_i}{R_1}$$

$$9) \text{Assume } \Delta V = 1V$$

$$10) t = \frac{T}{2} = \frac{1}{2f}$$

$$11) C_1 = \frac{I_1 t}{\Delta V}$$

formulae to find the slew rate.

$$1) \Delta V_0 = +V_{sat} - (-V_{sat})$$

$$\text{WKT } +V_{sat} = (V_{CC} - 1)$$

$$-V_{sat} = (-V_{EE} + 1)$$

$$2) \Delta t = 0.1 \times t$$

$$3) X_{C1} = \frac{R_1}{20}$$

$$4) f(\text{min}) = \frac{1}{2\pi X_{C1} C_1}$$

$$5) S_{\text{min}} = \frac{\Delta V_0}{\Delta t}$$



Problems.

1) A capacitor-coupled zero-crossing detector is to handle a 1kHz square wave input with a peak-to-peak amplitude of 6V. Design a suitable circuit, using a 741 op-amp with a $\pm 12V$ supply.

Given :- $f = 1\text{kHz}$, $V_{(p-p)} = 6\text{V}$, $V_{cc} = 12\text{V}$.

Sol :- For op-amp 741 : $I_B(\text{max}) = 500\text{nA}$

-Assuming i) $\Delta V = 1\text{V}$,

$$\text{ii)} \quad V_B = V_{R3} = 0.1\text{V}$$

$$\text{iii)} \quad V_{BE} = 0.7\text{V}$$

$$* \quad R_1 = \frac{0.1V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}} = 140\text{k}\Omega$$

use

$$R_1 = 120\text{k}\Omega$$

$$* \quad \text{let } I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$$

$$I_2 = 50\text{\textmu A}$$

$$* \quad V_{R2} = V_{cc} - V_B = 12\text{V} - 0.1\text{V}$$

$$V_{R2} = 11.9\text{V}$$

$$* \quad R_2 = \frac{V_{R2}}{I_2} = \frac{11.9\text{V}}{50\text{\textmu A}} = 238\text{k}\Omega$$

Use standard value :

$$R_2 = 220\text{k}\Omega$$



NOW $I_2 = \frac{V_{R2}}{R_2} = \frac{11.9V}{220k\Omega}$

$$I_2 = 54.1 \mu A$$

* $R_3 = \frac{V_{R3}}{I_2} = \frac{0.1V}{54.1 \mu A} = 1.85 k\Omega$

Use $R_3 = 1.8 k\Omega$

* $V_i(\text{peak}) = \frac{V_i(p-p)}{2} = \frac{6V}{2}$

$$V_i(\text{peak}) = 3V$$

* $I_1 = \frac{V_i}{R_1} = \frac{3V}{120k\Omega}$

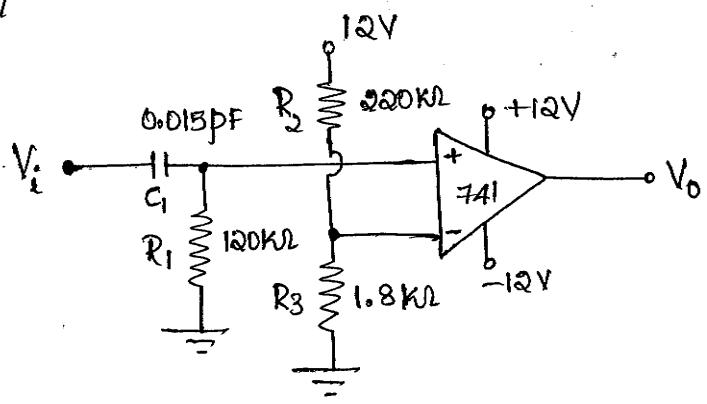
$$I_1 = 25 \mu A$$

* $t = \frac{1}{2f} = \frac{1}{2 \times 1 \text{kHz}}$

$$t = 500 \mu s$$

* $C_1 = \frac{I_1 t}{AV} = \frac{25 \mu A \times 500 \mu s}{1V} = 0.0125 \mu F$

Use $C_1 = 0.015 \mu F$



2) For the circuit designed in problem 1, estimate the minimum op-amp slew rate to give a reasonably undistorted op. Also, calculate the lowest sine wave input frequency that can be applied without the phase shift error exceeding 3° .

Given: from problem 1

$$V_{CC} = 12V, -V_{EE} = -12V, t = 500 \mu\text{sec}, R_1 = 120 \text{ k}\Omega$$

Sol:- $A V_o = +V_{sat} - (-V_{sat})$

$$+V_{sat} = V_{CC} - 1V = 12V - 1V$$

$$+V_{sat} = 11V$$

$$-V_{sat} = (-V_{EE} + 1V) = -12V + 1V.$$

$$-V_{sat} = -11V$$

$$\Delta V_o = 11V - (-11V)$$

$$\therefore \Delta V_o = 22V$$

* $\Delta t = 0.1 \times t = 0.1 \times 500 \mu\text{sec}$

$$\Delta t = 50 \mu\text{sec}$$

* $S_{min} = \frac{\Delta V_o}{\Delta t} = \frac{22V}{50 \mu\text{sec}} = 0.44V/\mu\text{sec}$

* $X_{C1} = \frac{R_1}{20} = \frac{120 \text{ k}\Omega}{20}$

$$X_{C1} = 6 \text{ k}\Omega$$

* $f_{(min)} = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6 \text{ k}\Omega \times 0.015 \mu\text{F}} = \underline{\underline{1.8 \text{ kHz}}}$



3) A capacitor-coupled zero crossing detector is to handle a 2KHz square wave with a peak-to-peak amplitude of 10V. Design a ckt using a 741 op-amp with a $\pm 15V$ supply. Estimate the minimum op-amp slew rate to give a reasonably undistorted op. Also, calculate the lowest sine wave input frequency that can be applied without the phase shift error exceeding 3° .

Given: $V_B = 0.1V$, $I_{B(\max)} = 500\text{nA}$

June -09, 8m

$f = 2\text{KHz}$, $V_{(P-P)} = 10V$, $V_{CC} = 15V$, $-V_{EE} = -15V$

Sol : Assuming

$$\begin{aligned}\Delta V &= 1V \\ V_B &= V_{R3} = 0.1V \\ V_{BE} &= 0.7V\end{aligned}$$

* $R_1 = \frac{0.1V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7V}{500\text{nA}} = \underline{\underline{140\text{k}\Omega}}$

Use $R_1 = 120\text{k}\Omega$ ← Im

* Let $\frac{I_2}{2} = 100 \times I_{B(\max)} = 100 \times 500\text{nA}$

$$\frac{I_2}{2} = 50\mu\text{A}$$

* $V_{R2} = V_{CC} - V_B = 15 - 0.1V$

$$V_{R2} = 14.9V$$

* $R_2 = \frac{V_{R2}}{\frac{I_2}{2}} = \frac{14.9V}{50\mu\text{A}} = 298\text{k}\Omega$

Use $R_2 = 270\text{k}\Omega$



* Now $I_2 = \frac{V_{R2}}{R_2} = \frac{14.9V}{2K\Omega}$

$$\boxed{I_2 = 65.18 \mu A}$$

* $R_3 = \frac{V_{R3}}{I_2} = \frac{0.1V}{50 \mu A} = 2K\Omega$

use $\boxed{R_3 = 1.8 K\Omega} \leftarrow \textcircled{1M}$

* $V_i(\text{peak}) = \frac{V_i(p-p)}{2} = \frac{10V}{2}$

$$\boxed{V_i(\text{peak}) = 5V}$$

* $I_1 = \frac{V_i}{R_1} = \frac{5V}{1.8 K\Omega}$

$$\boxed{I_1 = 41.6 \mu A}$$

* $t = \frac{1}{2f} = \frac{1}{2 \times 2 \text{kHz}}$

$$\boxed{t = 250 \mu \text{sec}}$$

* $C_1 = \frac{I_1 t}{AV} = \frac{41.6 \mu A \times 250 \mu s}{1V} = \underline{\underline{0.0104 \mu \text{sec}}}$

use $\boxed{C = 0.01 \mu F} \leftarrow \textcircled{1M}$

* $AV = +V_{sat} - (-V_{sat})$

$+V_{sat} = (V_{CC} + I) = (15V - 1V) = \underline{\underline{14V}}$

$-V_{sat} = (-V_{EE} + I) = (-15V + 1V) = \underline{\underline{-14V}}$



$$\therefore \Delta V_0 = 14 - (-14V)$$

$$\boxed{\Delta V_0 = 28V} \quad \leftarrow \quad \text{1M}$$

$$* \quad t = \frac{1}{2f} = \frac{1}{2 \times 2 \times 10^3}$$

$$\boxed{t = 250 \mu\text{sec}}$$

$$* \quad \Delta t = 0.1 \times t = 0.1 \times 250 \mu\text{sec}$$

$$\boxed{\Delta t = 25 \mu\text{sec}}$$

$$* \quad X_{C1} = \frac{R_1}{20} = \frac{120 \text{ k}\Omega}{20}$$

$$\boxed{X_{C1} = 6 \text{ k}\Omega}$$

$$* \quad S(\text{min}) = \frac{\Delta V_0}{\Delta t} = \frac{28V}{25 \mu\text{sec.}}$$

$$\boxed{S(\text{min}) = 1.12V/\mu\text{sec}} \quad \leftarrow \quad \text{1M}$$

$$* \quad f(\text{min}) = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6 \text{ k}\Omega \times 0.01 \mu\text{F}}$$

$$\boxed{f(\text{min}) = 2.65 \text{ kHz}} \quad \leftarrow \quad \text{1M}$$



A) A capacitor coupled zero detector is to handle a 1KHz square wave with a peak to peak amplitude of 6V. Design a suitable circuit using a 741 op-amp with a $\pm 12V$ supply. Estimate the minimum op-amp slew rate to give a reasonably undistorted output. Also calculate the lowest sine wave input frequency that can be applied without the phase shift error exceeding 3° .

Jan-09, 8M(EE)

Given :-

$$f = 1\text{ KHz}, V_{(p-p)} = 6\text{V}, +V_{CC} = 12\text{V}, -V_{EE} = -12\text{V}$$

Sol :- Assuming :

$$\begin{aligned} V_{BE} &= 0.7\text{V} \\ V_B &= V_{R3} = 0.1\text{V} \\ \Delta V &= 1\text{V} \end{aligned}$$

for 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

$$* R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}} = \underline{\underline{140\text{k}\Omega}}$$

choose. $R_1 = 120\text{k}\Omega$

$$* \text{ Let } \frac{I}{2} = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$$

$$\underline{\underline{I_2 = 50\mu\text{A}}}$$

$$* V_{R2} = V_{CC} - V_B = 12\text{V} - 0.1\text{V}$$

$$\underline{\underline{V_{R2} = 11.9\text{V}}}$$

$$* R_2 = \frac{V_{R2}}{I_2} = \frac{11.9\text{V}}{50\mu\text{A}} = \underline{\underline{238\text{k}\Omega}}$$

choose,

$$\underline{\underline{R_2 = 270\text{k}\Omega}}$$



* Now $I_2 = \frac{V_{R2}}{I_2} = \frac{11.9V}{270k\Omega}$

$$\boxed{I_2 = 54.1 \mu A}$$

* $R_3 = \frac{V_{E3}}{I_2} = \frac{0.1V}{54.1 \mu A} = 1.85 k\Omega$

choose $\boxed{R_3 = 1.8 k\Omega}$

* $V_i(\text{peak}) = \frac{V_i(p-p)}{2} = \frac{6V}{2}$

$$\boxed{V_i(\text{peak}) = 3V}$$

* $I_1 = \frac{V_i(p)}{R_1} = \frac{3V}{120k\Omega}$

$$\boxed{I_1 = 25 \mu A}$$

* $t = \frac{1}{2f} = \frac{1}{2 \times 1 \text{kHz}}$

$$\boxed{t = 50.0 \mu \text{sec}}$$

* $C_1 = \frac{I_1 t}{\Delta V} = \frac{25 \mu A \times 500 \mu \text{sec}}{1V} = 0.0125 \mu F$

choose $\boxed{C_1 = 0.015 \mu F}$

* $\Delta V_o = +V_{sat} - (-V_{sat}) = [V_{cc} - 1] - [-V_{EE} + 1]$

$$\Delta V_o = (12 - 1) - (-12 + 1)$$

$$\boxed{\Delta V_o = 22V}$$



* $\Delta t = 0.1 \times t = 0.1 \times 500 \mu\text{sec}$

$\Delta t = 50 \mu\text{sec}$

* $S_{\min} = \frac{\Delta V_o}{\Delta t} = \frac{22V}{50 \mu\text{sec}}$

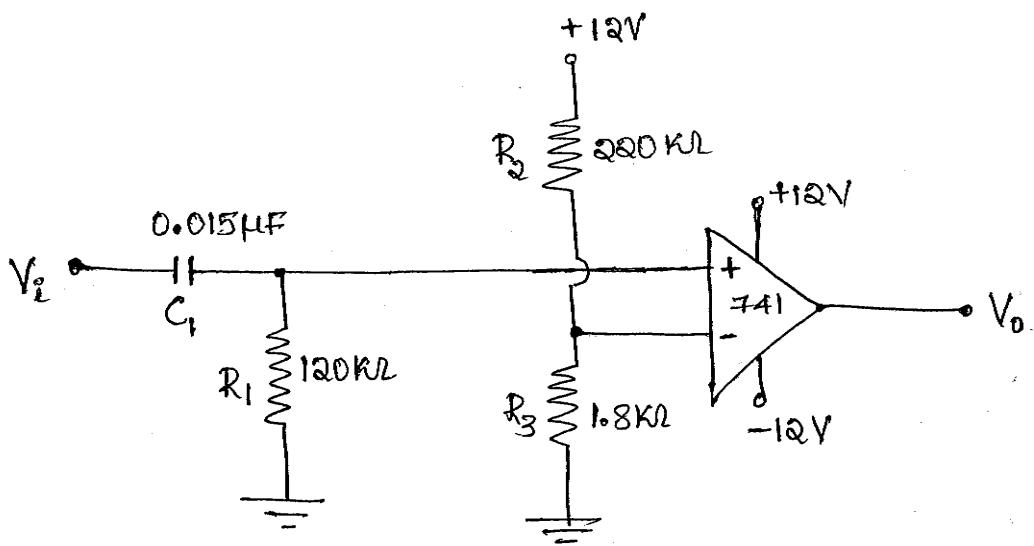
$S_{\min} = 0.44 \text{ V}/\mu\text{sec}$

* $X_{C1} = \frac{R_1}{20} = \frac{120 \text{ k}\Omega}{20}$

$X_{C1} = 6 \text{ k}\Omega$

* $f_{(\min)} = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6 \text{ k}\Omega \times 0.015 \mu\text{F}}$

$f_{(\min)} = 1.8 \text{ kHz}$



5) A capacitor coupled zero crossing detector is to provide an op voltage of approximately $\pm 15V$, when a 5 kHz , $\pm 3V$ square wave input is applied. Design a suitable ckt to use a bipolar op-amp. Tilt at the Non-INV terminal ΔV is to be $0.75V$.

June-07, 6M(EE)

Given :- $V_{CC} = +15V$, $-V_{EE} = -15V$, $f = 5\text{ kHz}$,
 $V_i = 3V$, $\Delta V = 0.75V$.

Sol :- Assuming :

$$\begin{aligned} V_{BE} &= 0.7V \\ V_B &= V_{E3} = 0.1V \end{aligned}$$

For 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

* $R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7V}{500\text{nA}} = 140\text{k}\Omega$

choose, $R_1 = 120\text{k}\Omega$

* Let $\frac{I}{2} = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$\frac{I}{2} = 50\mu\text{A}$$

* $V_{R2} = V_{CC} - V_B = 15V - 0.1V$

$$V_{R2} = 14.9V$$

* $R_2 = \frac{V_{R2}}{\frac{I}{2}} = \frac{14.9V}{50\mu\text{A}} = 298\text{k}\Omega$

choose $R_2 = 270\text{k}\Omega$

Now. $\frac{I}{2} = \frac{V_{R2}}{R_2} = \frac{14.9V}{270\text{k}\Omega}$. $\therefore \frac{I}{2} = 55.18\mu\text{A}$



$$* R_3 = \frac{V_{o3}}{I_2} = \frac{0.1V}{55.18\text{mA}} = 1.812\text{k}\Omega$$

choose $R_3 = 1.8\text{k}\Omega$

$$* I_1 = \frac{V_{i(p)}}{R_1} = \frac{3V}{120\text{k}\Omega}$$

$I_1 = 25\mu\text{sec}$

$$* t = \frac{1}{2f} = \frac{1}{2 \times 5\text{kHz}}$$

$t = 100\mu\text{sec}$

$$* C_1 = \frac{I_1 t}{\Delta V} = \frac{25\mu\text{sec} \times 100\mu\text{sec}}{0.75V}$$

$C_1 = 3333.33\text{pF}$

choose $C_1 = 3300\text{pF}$

$$* \Delta V_0 = +V_{sat} - (-V_{sat})$$

$$+V_{sat} = (V_{cc} - 1V) = (15V - 1V) = 14V$$

$$-V_{sat} = (-V_{EE} + 1V) = (-15 + 1V) = -14V$$

$$\Delta V_0 = 14V - (-14V)$$

$\Delta V_0 = 28V$

$$* \Delta t = 0.1 \times t = 0.1 \times 100\mu\text{sec}$$

$\Delta t = 10\mu\text{sec}$

$$* S_{min} = \frac{\Delta V_0}{\Delta t} = \frac{28V}{10\mu\text{sec}}$$

$S_{min} = 2.8V/\mu\text{sec}$

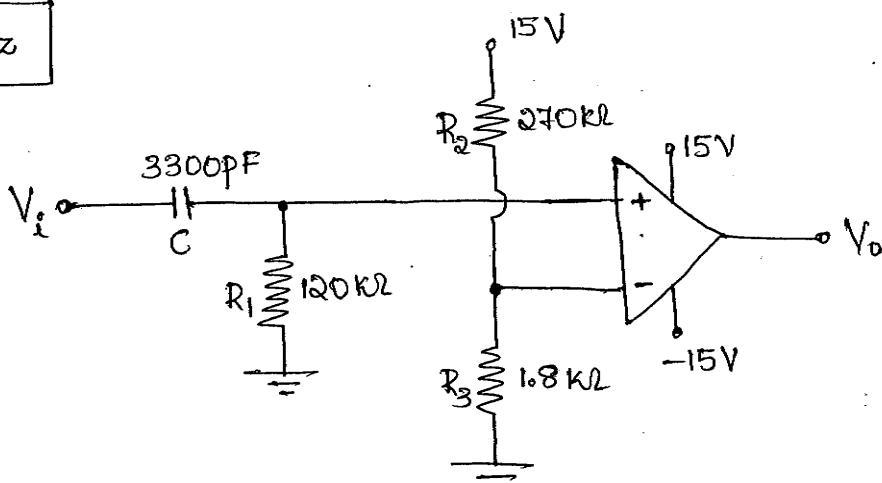


$$* X_{C1} = \frac{R_1}{2\pi} = \frac{120\text{ k}\Omega}{2\pi}$$

$$X_{C1} = 6\text{ k}\Omega$$

$$f_{\min} = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6\text{ k}\Omega \times 3300\text{ pF}}$$

$$f_{\min} = 8.038\text{ kHz}$$



b) A capacitor coupled zero crossing detector is to provide an opv voltage of approximately $\pm 17\text{ V}$, when a 3 kHz , $\pm 2\text{ V}$ square wave ifp is applied. Design a suitable ckt to use a bipolar op-amp.

[Jan - 08, 6M (EE)]

Given: $+V_{CC} = 17\text{ V}$, $-V_{EE} = -17\text{ V}$, $f = 3\text{ kHz}$, $V_{i(p)} = 2\text{ V}$.

Sol: Assuming

- i) $\Delta V = 1$
- ii) $V_B = V_{Q3} = 0.1\text{ V}$
- iii) $V_{BE} = 0.7\text{ V}$

For 741 op-amp : $I_{B(\max)} = 500\text{nA}$

$$* R_1 = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7\text{ V}}{500\text{nA}} = 140\text{ k}\Omega \quad \text{choose } R_1 = 120\text{ k}\Omega$$



* Let $\frac{I_2}{2} = 100 \times I_B(\text{max}) = 100 \times 500 \text{nA}$

$$\boxed{\frac{I_2}{2} = 50 \text{mA}}$$

* $V_{R2} = V_{CC} - V_B = 17V - 0.1V$

$$\boxed{V_{R2} = 16.9V}$$

* $R_2 = \frac{V_{R2}}{\frac{I_2}{2}} = \frac{16.9V}{50 \text{mA}} = 338 \text{k}\Omega$, choose $\boxed{R_2 = 330 \text{k}\Omega}$

* Now $\frac{I_2}{2} = \frac{V_{R2}}{R_2} = \frac{16.9V}{330 \text{k}\Omega}$. $\boxed{\frac{I_2}{2} = 51.212 \text{mA}}$

* $R_3 = \frac{V_{R3}}{\frac{I_2}{2}} = \frac{0.1V}{51.212 \text{mA}} = \underline{1.952 \text{k}\Omega}$

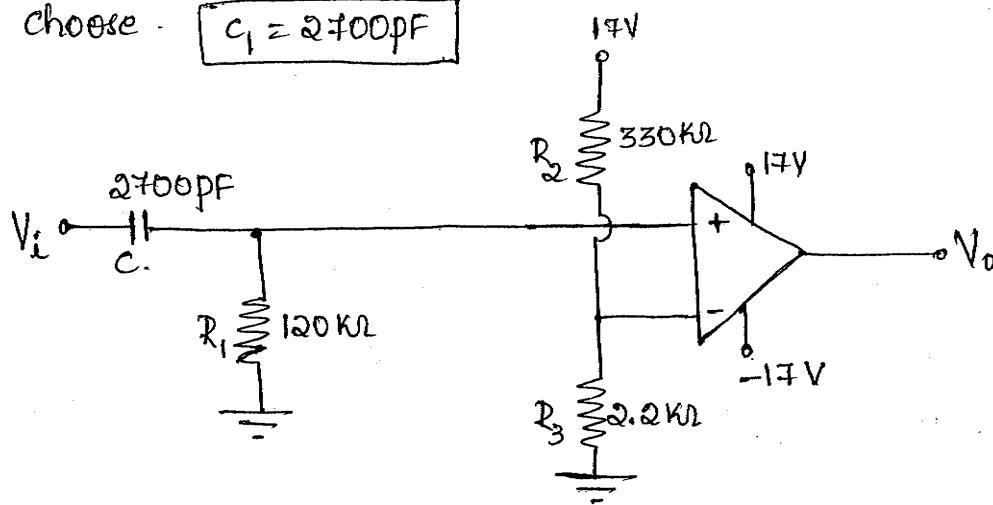
choose $\boxed{R_3 = 2.2 \text{k}\Omega}$

* $I_1 = \frac{V_i(p)}{R_1} = \frac{2V}{120 \text{k}\Omega}$, $\boxed{I_1 = 16.66 \text{mA}}$

* $t = \frac{1}{2f} = \frac{1}{2 \times 3 \text{kHz}}$, $\boxed{t = 166.66 \mu\text{sec}}$

* $C_1 = \frac{I_1 t}{AV} = \frac{16.66 \text{mA} \times 166.66 \mu\text{sec}}{1V} = 2776.55 \text{pF}$

choose - $\boxed{C_1 = 2700 \text{pF}}$



INVERTING SCHMITT TRIGGER CIRCUIT :-

- 1) With a neat circuit diagram and waveforms, explain the operation of INV schmitt trigger.

June -09, 6 M

June-10, 6M(EE)

Jan-09, 6M(EE)

June-08, 6M(EE)

Jan-05, 6 M(EE)

- 2) Explain the operation of an INV schmitt trigger circuit with different UTP & LTP voltages, with the help of a suitable ckt. Discuss the design procedure for components used. Also indicate the input/output characteristics for the INV schmitt trigger circuit.

Jan-10, 10M

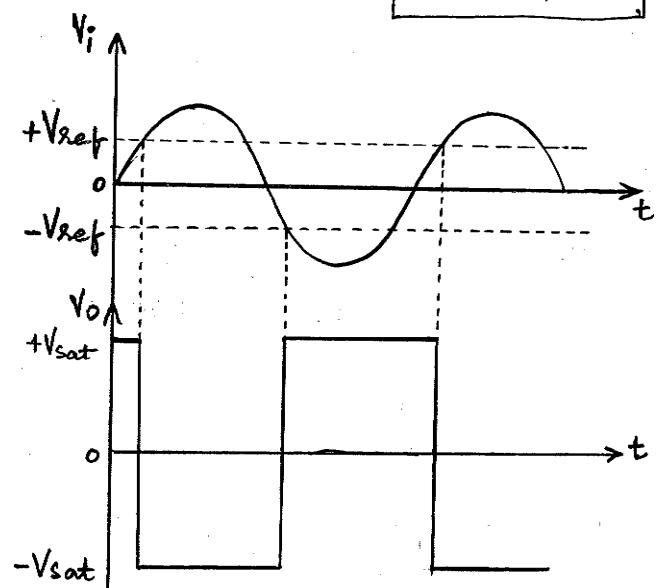
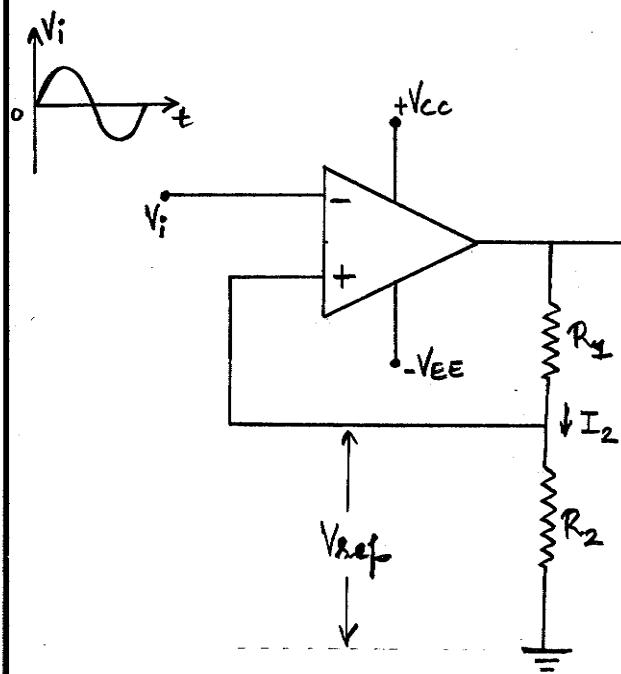


fig 1 @ shows an INV schmitt trigger circuit.

- * The input is applied to the inverting terminal of the schmitt trigger circuit. The feedback signal is given to the Non-INV terminal. This ensure +ve feedback.



- * The voltage at the Non-INV input is

$$V_{ref} = I_2 R_2$$

Where $I_2 = \frac{V_o}{R_1 + R_2}$

$$\therefore V_{ref} = \frac{V_o R_2}{R_1 + R_2}$$

- * When the o/p voltage V_o is at $+V_{sat}$, then V_{ref} will be a positive voltage & voltage at Non-INV terminal will also be positive ($+V_{ref}$).

i.e. $V_{ref} = \frac{V_o R_2}{R_1 + R_2}$ $(\because \text{Now } V_o = +V_{sat})$

$$+V_{ref} = \frac{+V_{sat} R_2}{R_1 + R_2} \quad (+ve \text{ saturation})$$

- * When $V_i > +V_{ref}$, then the voltage at INV terminal becomes greater than ($+V_{ref}$) Non INV terminal & the o/p will switch from $+V_{sat}$ to $-V_{sat}$.

i.e. $V_{ref} = \frac{V_o R_2}{R_1 + R_2}$ $(\because \text{Now } V_o = -V_{sat})$

$$\therefore -V_{ref} = \frac{-V_{sat} R_2}{R_1 + R_2} \quad (-ve \text{ saturation})$$

- * In fig 1 ⑤, the voltage at point $+V_{ref}$ on the waveform at which o/p shifts from $+V_{sat}$ to $-V_{sat}$ is called "upper Triggering point" (UTP).



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Similarly, the voltage at point $-V_{ref}$ on the waveform at which o/p shifts from $-V_{sat}$ to $+V_{sat}$ is called "Lower Triggering point" (LTP).

Thus the o/p of a schmitt trigger is always a square wave or rectangular wave.

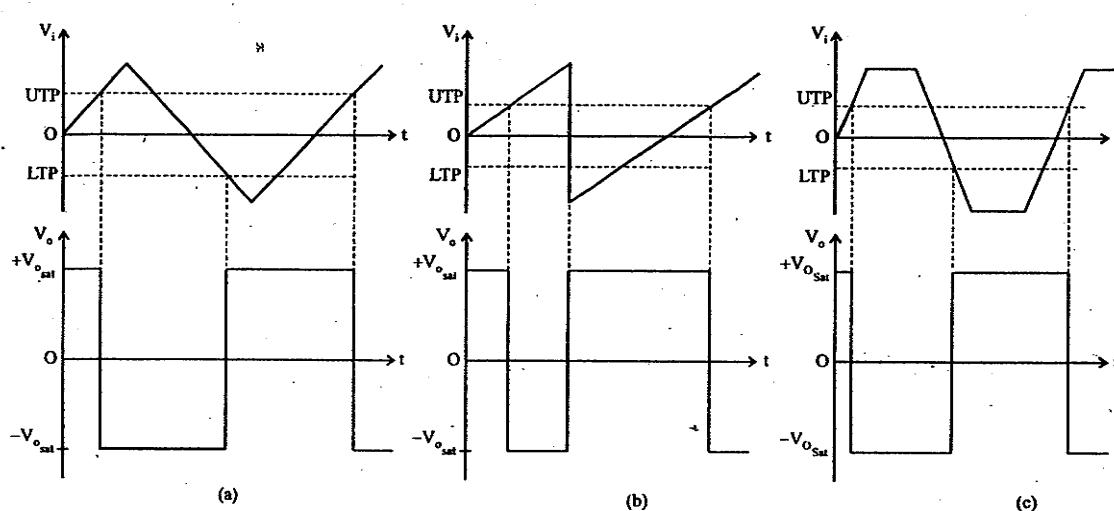


Fig. : (a) Triangular input waveform producing square wave
 (b) Saw tooth input waveform producing square wave
 (c) Trapezoidal input waveform producing square wave

Input / output characteristics or Transfer characteristics :-

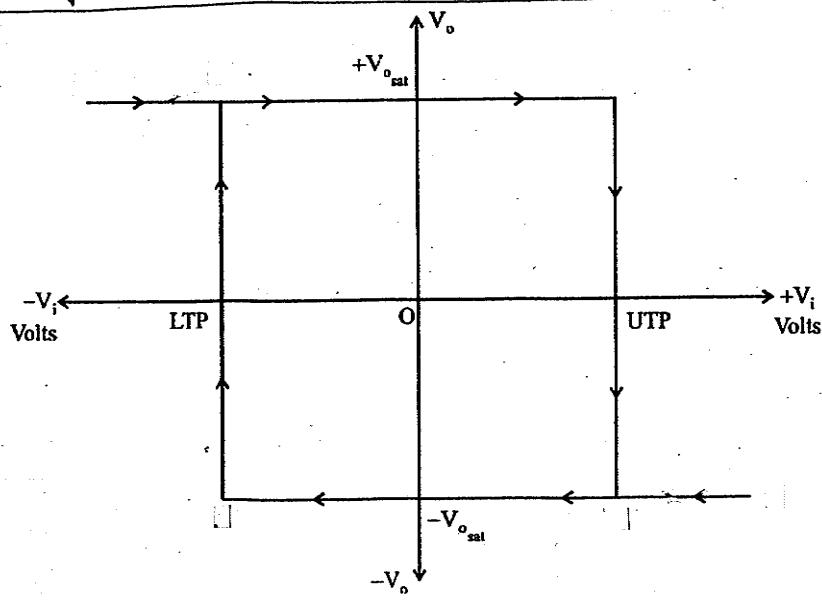


Fig. : Input/output characteristics (transfer characteristics) of Schmitt trigger



- * When $V_i = 0V$, the o/p will be at $+V_{sat}$. When $V_i = UTP$ the o/p switches from $+V_{sat}$ to $-V_{sat}$.
When $V_i < LTP$, the o/p will be at $-V_{sat}$. When $V_i = LTP$, the o/p switches from $-V_{sat}$ to $+V_{sat}$.
- * The voltage difference between the upper and lower triggering points is referred to as hysteresis.

∴
$$V_H = UTP - LTP$$

Schmitt trigger circuit design :-

- * The current I_2 flowing through the resistors R_1 & R_2 is chosen to be 100 times $I_B(\text{max})$.
i.e.
$$I_2 = 100 I_B(\text{max})$$
- * $R_2 = \frac{\text{triggering voltage}}{I_2}$
- * $R_1 = \frac{V_o - \text{triggering voltage}}{I_2}$

NOTE : WKT. $V_{ref} = I_2 R_2$

$$\therefore R_2 = \frac{V_{ref}}{I_2}$$

- * Applying KVL from o/p V_o , R_1 & R_2 , we get

$$V_o - I_2 R_1 - V_{ref} = 0.$$

$$V_o - V_{ref} = I_2 R_1.$$

$$\therefore R_1 = \frac{V_o - V_{ref}}{I_2}$$



FORMULAE :-

for equal UTP & LTP i.e., $UTP = LTP$

- 1) Let $I_2 = 100 \times I_B(\text{max})$
- 2) $UTP = V_{R2}$
- 3) $R_2 = \frac{V_{R2}}{I_2}$
- 4) Applying KVL from V_o , R_1 & R_2

$$V_o - I_2 R_1 - I_2 R_2 = 0$$

$$V_o - I_2 R_1 - V_{R2} = 0.$$

$$I_2 R_1 = V_o - V_{R2}$$

$$R_1 = \frac{V_o - V_{R2}}{I_2}$$

$$V_o = +V_{sat}$$

$$R_1 = \frac{V_{sat} - V_{R2}}{I_2}$$



1) Using a 741 op-amp with a supply of $\pm 12V$, design an INV-Schmitt triggering circuit to have trigger points of $\pm 2V$.

Given :- $V_{cc} = +12V$, $V_{sat} = 12V$, $U_{TP} = L_{TP} = 2V$.

Sol :- for 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

* Let $\frac{I}{2} = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$\boxed{\frac{I}{2} = 50\mu\text{A}}$$

* $V_{R2} = U_{TP} = 2V$

* $R_2 = \frac{V_{R2}}{\frac{I}{2}} = \frac{2V}{50\mu\text{A}} = 40\text{k}\Omega$

choose $\boxed{R_2 = 39\text{k}\Omega}$

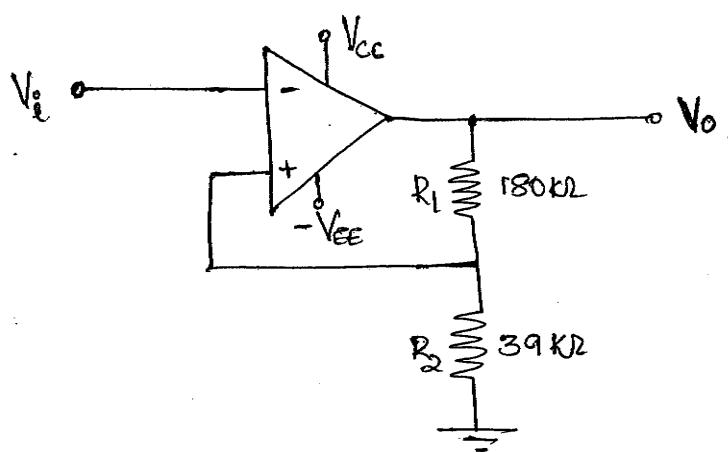
Now, $\frac{I}{2} = \frac{V_{R2}}{R_2} = \frac{2V}{39\text{k}\Omega}$

$$\boxed{\frac{I}{2} = 51.3\mu\text{A}}$$

* $R_1 = \frac{V_{sat} - V_{R2}}{\frac{I}{2}} = \frac{12 - 2}{51.3\mu\text{A}} = 175\Omega$

choose

$$\boxed{R_1 = 180\Omega}$$



Q) Using a bipolar op-amp, design an INV schmitt trigger ckt to trigger at ± 0.8 volt and to produce an o/p of approximately ± 11 V.

Given: $\pm V_{sat} = \pm 11$ V, $U_{TP} = L_{TP} = \pm 0.8$ V

For 741 op-amp $I_E(\text{max}) = 500\text{nA}$

Sol:-

* Let $I_2 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$I_2 = 50\mu\text{A}$$

* $V_{R2} = U_{TP} = 0.8$ V

* $R_2 = \frac{V_{R2}}{I_2} = \frac{0.8\text{ V}}{50\mu\text{A}} = 16\text{ k}\Omega$

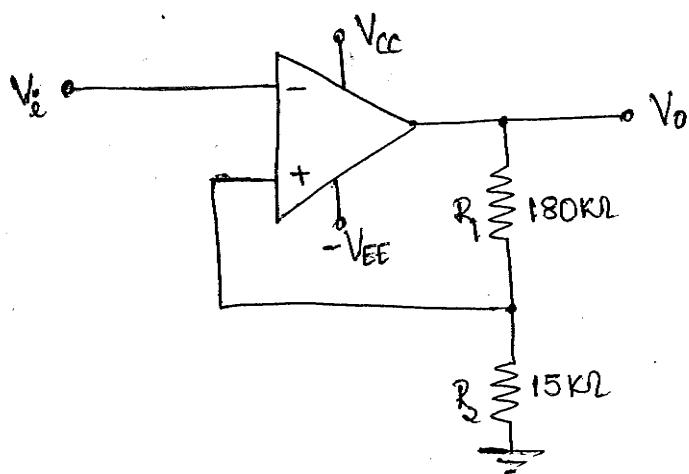
choose $R_2 = 15\text{ k}\Omega$

* Now $I_2 = \frac{V_{R2}}{15\text{ k}\Omega}$

$$I_2 = 53.33\mu\text{A}$$

* $R_1 = \frac{V_{sat} - V_{R2}}{I_2} = \frac{11 - 0.8\text{ V}}{53.33\mu\text{A}} = 191.25\text{ k}\Omega$

choose $R_1 = 180\text{k}\Omega$



ARUNKUMAR G M.Tech, Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.

Adjusting the Trigger points (UTP & LTP) :-

i) Schmitt Trigger with LTP = 0 :-

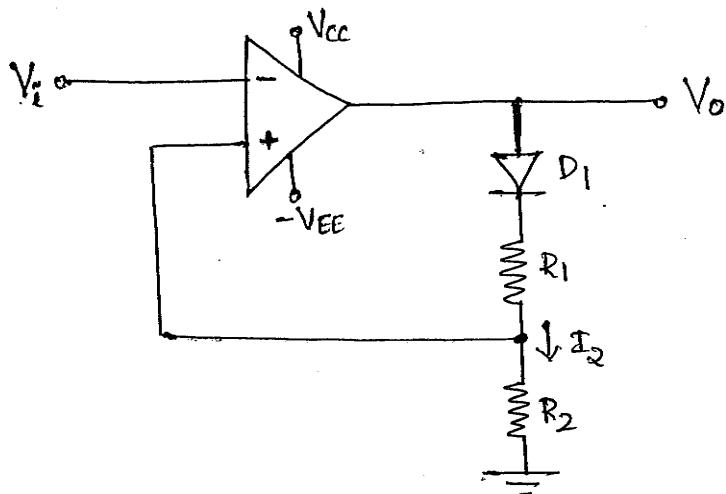


Fig ① : Schmitt trigger ckt with LTP = 0

- * Fig ① shows the ckt with +ve UTP & zero LTP.
This can be achieved by using a diode in series with R_1 .
When the o/p is at $+V_{sat}$, the diode D_1 is forward biased and UTP will be equal to the voltage drop across the resistor R_2 (i.e. $V_{ref} = UTP$).

$$UTP = IR_2$$

$$UTP = \frac{V_{sat} \cdot R_2}{R_1 + R_2}$$

$$\left(\text{where } \beta = \frac{R_2}{R_1 + R_2} \right)$$

- * When the o/p is at $-V_{sat}$, the diode D_1 is reverse biased and only a very small current (I_B) flows through R_2 & the Non-INV terminal is held at $\approx 0V$. thus $LTP = 0$.
- * When the input voltage is reduced below ground level, the o/p will go to $+V_{sat}$.



- * The diode D_1 must be selected to have a maximum reverse voltage (PIV) greater than the circuit supply voltage.
- * The maximum reverse recovery time ' t_{rr} ' should be much smaller than the minimum pulse width of the input signal i.e.

$$t_{rr} \leq \frac{\text{minimum pulse width}}{10}$$

ii) INV - SCHMITT trigger having different LTP & UTP :-

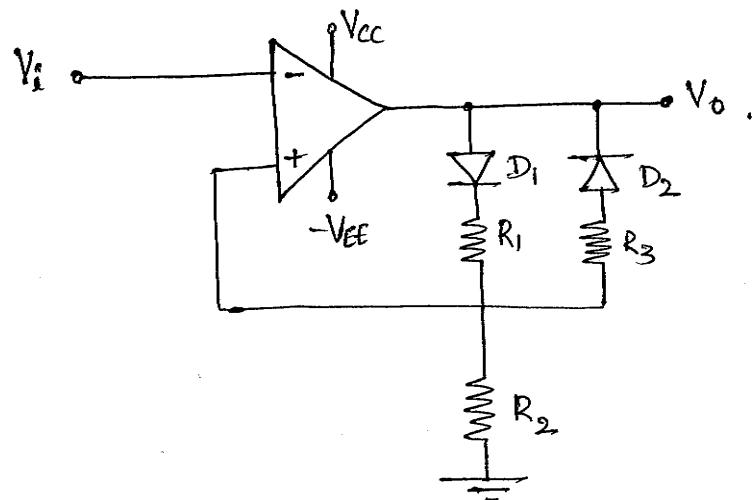


fig ①: schmitt trigger circuit with different LTP&UTP.

- * The schmitt trigger ckt shown in fig ① uses two diodes D_1 & D_2 and three resistors R_1 , R_2 & R_3 to get different LTP & UTP voltage.

Case i: When $V_o = +V_{sat}$, the diode D_1 is forward biased and D_2 is reverse biased. The UTP is given by.

$$\text{UTP} = V_{R_2} = \frac{R_2}{R_1 + R_2} [|V_o| - V_F]$$



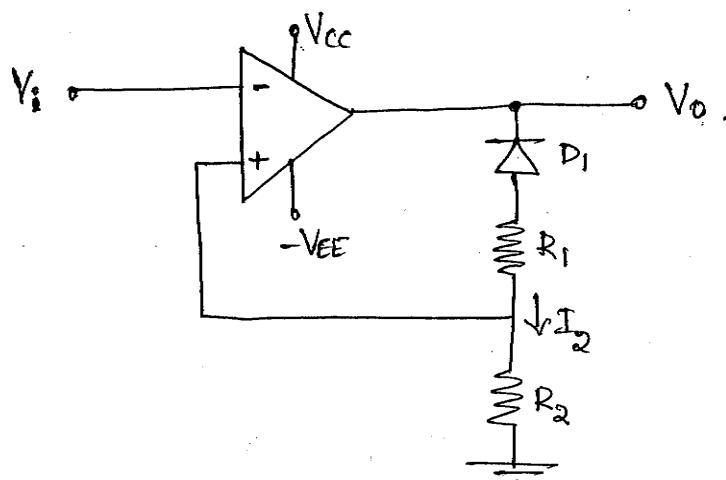
Case ii : When $V_o = -V_{sat}$, the diode D_1 is reverse biased and D_2 is forward biased. The LTP is given by.

$$LTP = V_{R2} = \frac{R_2}{R_3 + R_2} [|V_o| - V_F]$$

Where V_F is the voltage drop across D_1 & D_2 .

- * Different values of R_1 & R_2 gives different UTP & LTP voltages.

NOTE :- Schmitt trigger with $UTP = 0$:-



UNEQUAL 'UTP' & LTP :-

FORMULAE

Let $I_Q = 500 \mu A$

$$\Rightarrow R_2 = \frac{V_{R2}}{I_Q}$$

$V_{R2} = UTP$

$R_2 = \frac{UTP}{I_Q}$

2) $V_{sat} = (V_{cc} - 1V)$

3) $-V_{sat} = (-V_{EE} + 1V)$

4) Assume $V_F = 0.7V$

5) $UTP = \frac{R_2}{R_1 + R_2} (|V_{sat}| - V_F)$

Determine R_1 .

6) $LTP = \frac{R_2}{R_3 + R_2} (|V_{sat}| - V_F)$

Determine R_3 .



FORMULAE FOR LTP = 0 & UTP = +Ve Schmitt trigger.

1) Let $I_2 = 500 \mu A$

$$2) R_2 = \frac{V_{R2}}{I_2}$$

Here $V_{R2} = UTP$.

$$R_2 = \frac{UTP}{I_2}$$

$$3) R_1 = \frac{V_{R1}}{I_2}$$

Applying KVL to o/p ckt

$$V_{sat} - V_F - I_2 R_1 - V_{R2} \rightarrow 0$$

$$I_2 R_1 = V_{sat} - V_F - V_{R2}$$

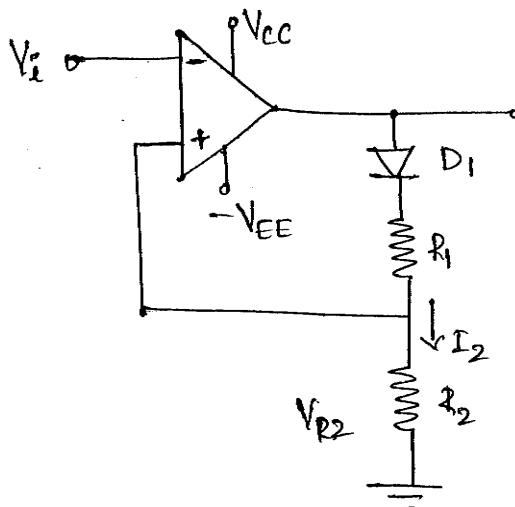
$$R_1 = \frac{V_{sat} - V_F - V_{R2}}{I_2}$$

where

$$+ V_{sat} = (V_{cc} - 1V)$$

$$V_{R2} = UTP$$

$$R_1 = \frac{[V_{cc} - 1] - V_F - UTP}{I_2}$$



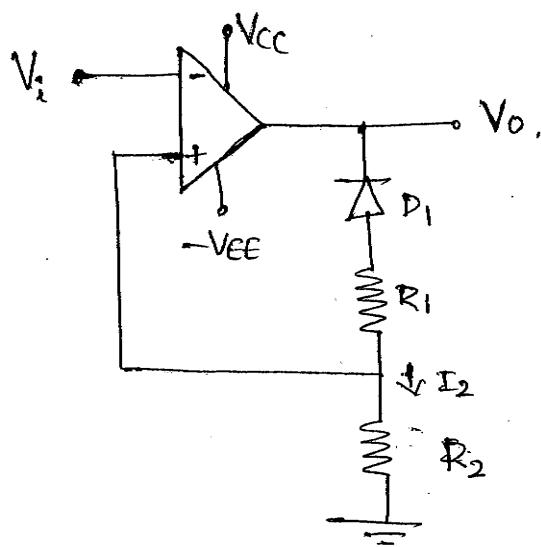
Formula for UTP = 0 & LTP = +Ve Schmitt trigger.

1) Let $I_2 = 500 \mu A$

2) $R_2 = \frac{V_{R2}}{I_2}$

Here $V_{R2} = \text{LTP}$

3)
$$R_2 = \frac{\text{LTP}}{I_2}$$



3) $R_1 = \frac{V_{R1}}{I_2}$

Applying KVL to o/p ckt

$$V_{sat} - V_F - I_2 R_1 - V_{R2} = 0$$

$$V_{sat} - V_F - V_{R2} = I_2 R_1$$

$$R_1 = \frac{V_{sat} - V_F - V_{R2}}{I_2}$$

$V_{sat} = V_{cc} - 1V$
 $V_{R2} = \text{LTP}$

$\therefore R_1 = \frac{[V_{cc} - 1V] - V_F - \text{LTP}}{I_2}$



1) An INV schmitt trigger ckt is to have UTP = 0V & LTP = 1V. Design a suitable ckt using a bipolar op-amp and $\pm 15V$ supply.

June -08, 7*1

Given: UTP = 0V, |LTP| = 1V, $V_{CC} = 15V$, $-V_{EE} = -15V$.

Sol: Assume $V_F = 0.7V$

* Let $I_2 = 500 \mu A$ ← (1M)

* $R_2 = \frac{V_{R2}}{I_2}$

$V_{R2} = LTP$

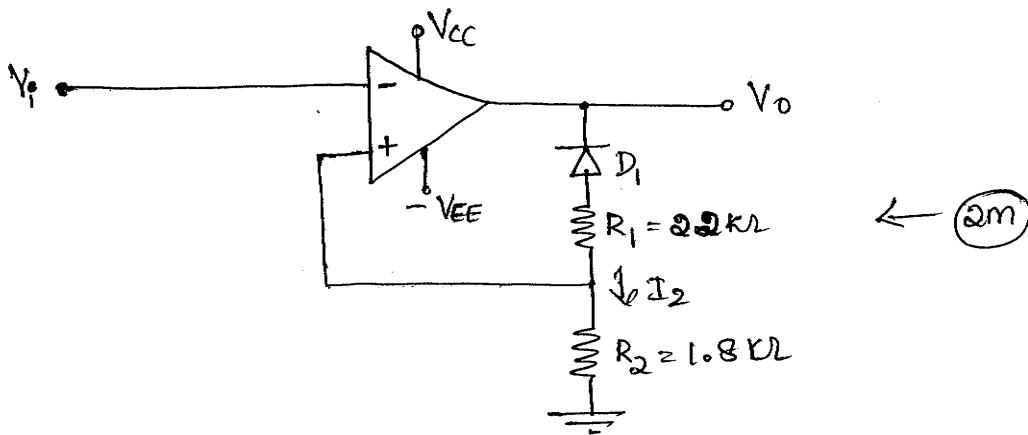
$$R_2 = \frac{|LTP|}{I_2} = \frac{1V}{500 \mu A} = \frac{2k\Omega}{}, \text{ choose } R_2 = 1.8 k\Omega \leftarrow (1M)$$

* Now I_2 becomes $I_2 = \frac{V_{R2}}{R_2} = \frac{1V}{1.8 k\Omega}$

$I_2 = 555.5 \mu A$ ← (1M)

* $R_1 = \frac{|-V_{EE}| + 1}{I_2} = \frac{|-15| + 1}{555.5 \mu A} = \frac{16V}{555.5 \mu A}$

$R_1 = 29.14 k\Omega$ ← (2M) choose $R_1 = 22 k\Omega$



2) An INV schmitt trigger ckt is to have $U_{TP} = 0.4$ & $|LTP| = 2.5V$. Design a suitable ckt using a bipolar op-amp & a $\pm 18V$ supply.

June - 10, 8M

Given :- $U_{TP} = 0V$, $|LTP| = 2.5V$, $V_{cc} = 18V$
 $-V_{EE} = -18V$. Assume $V_F = 0.7V$

Sol :- * Let $I_2 = 500\mu A$

$$* R_2 = \frac{V_{P2}}{I_2} = \frac{|LTP|}{2} = \frac{2.5V}{500\mu A} = 5k\Omega$$

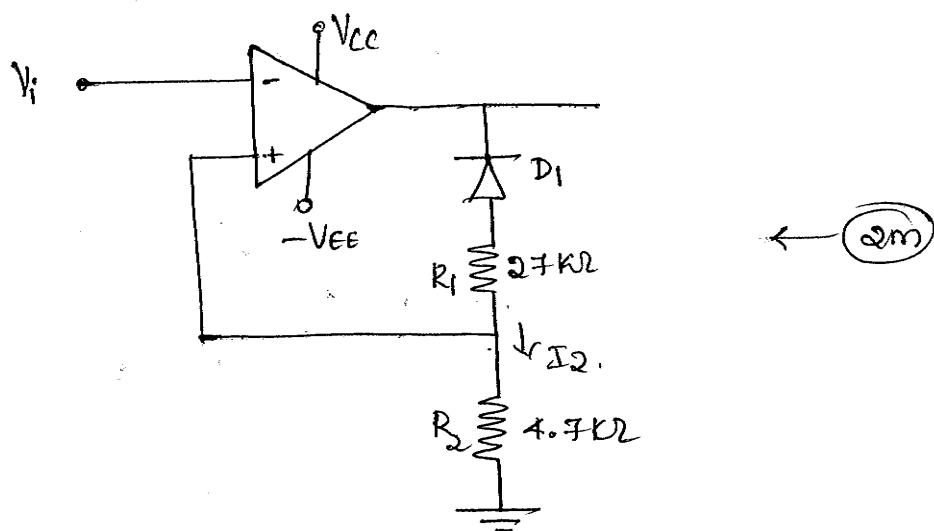
choose $R_2 = 4.7k\Omega$ ← (3m)

$$* \text{Now } I_2 \text{ becomes } I_2 = \frac{V_{P2}}{R_2} = \frac{2.5V}{4.7k\Omega}$$

$$I_2 = 532\mu A$$

$$* R_1 = \frac{|-V_{EE}| + V_F - |LTP|}{I_2} = \frac{17 - 0.7 - 2.5V}{532\mu A} = 25.9k\Omega$$

choose $R_1 = 27k\Omega$ ← (3m)



3) An INV Schmitt trigger ckt is to have UTP = 0.5 V & LTP = 0. Design a suitable ckt using a bipolar and a $\pm 18V$ supply.

Given: UTP = 0.5 V, LTP = 0 V, $V_{CC} = 18V$.

Assume $V_F = 0.7V$.

Sol :-

$$\text{* Let } I_2 = 500 \mu\text{A}$$

$$V_{RQ} = UTP = 0.5V$$

$$\text{* } R_2 = \frac{V_{R2}}{I_2} = \frac{UTP}{I_2} = \frac{0.5V}{500 \mu\text{A}} = 5k\Omega$$

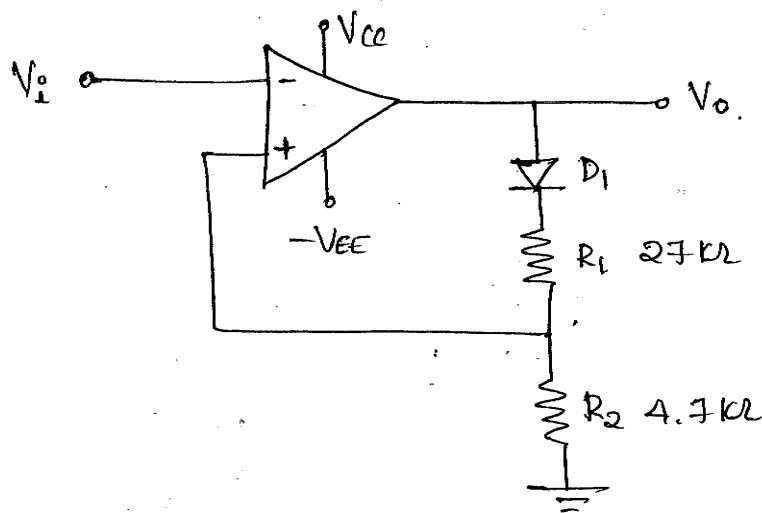
$$\text{choose } R_2 = 4.7k\Omega, \text{ Now } I_2 = \frac{V_{R2}}{R_2} = \frac{0.5V}{4.7k\Omega}$$

$$I_2 = 532 \mu\text{A}$$

$$\text{* } R_1 = \frac{(V_{CC} - 1) - V_F - V_{R2}}{I_2}$$

$$= \frac{17 - 0.7V - 0.5V}{532 \mu\text{A}} = 25.9k\Omega$$

$$\text{choose } R_1 = 27k\Omega$$



4) An INV schmitt trigger ckt is to have UTP = 1V & LTP = 0V. Design a suitable ckt using a bipolar op-amp & $\pm 15V$ supply.

Given :- UTP = 1V, LTP = 0V, V_{cc} = 15V

Sol :- Assume V_F = 0.7V

* Let $I_2 = 500 \mu A$

* $V_{R2} = UTP = 1V$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{1V}{500 \mu A} = 2k\Omega$

choose $R_2 = 1.8 k\Omega$

* Now I_2 becomes $I_2 = \frac{V_{R2}}{R_2} = \frac{1V}{1.8V}$

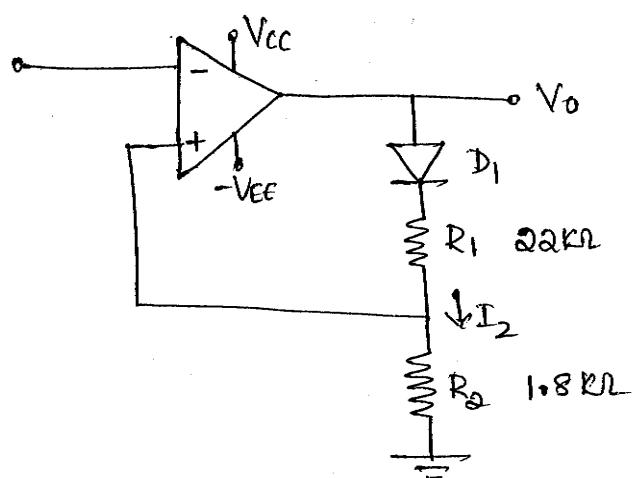
$I_2 = 555.5 \mu A$

* $R_1 = \frac{(V_{cc} - 1) - V_F - V_{R2}}{I_2} = \frac{14 - 0.7V - 1V}{555.5 \mu A}$

$R_1 = 22.14 k\Omega$

choose

$R_1 = 22 k\Omega$



1) Using a bipolar op-amp with ± 18 volts supply, design an inverting schmitt trigger circuit to have $UTP = 1.5V$ & $LTP = -3V$.

Given :- $V_{CC} = 18V$, $-V_{EE} = -18V$, $UTP = 1.5V$, $|LTP| = 3V$.

Assume $V_F = 0.7V$.

Sol: $V_{R2} = UTP = 1.5V$.

$$+V_{sat} = (V_{CC} - 1) = 17V$$

$$-V_{sat} = -V_{EE} + 1 = -18 + 1.$$

$$-V_{sat} = -17V$$

* Let $I_2 = 500\mu A$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{1.5V}{500\mu A} = 3k\Omega$

choose. $R_2 = 2.7k\Omega$

$$UTP = \frac{R_2 (+V_{sat} - V_F)}{R_1 + R_2}$$

$$1.5V = \frac{2.7k\Omega (17V - 0.7V)}{R_1 + 2.7k\Omega}$$

$$1.5R_1 + 4.05 \times 10^3 = 2.7k\Omega (16.3V)$$

$$1.5R_1 = 44.01 \times 10^3 - 4.05 \times 10^3$$

$$R_1 = \frac{39.96 \times 10^3}{1.5} = 26.64k\Omega$$

choose $R_1 = 27k\Omega$



$$* |LTP| = \frac{R_2 (1 - V_{sat}) - V_F}{R_2 + R_3}$$

$$3 = \frac{2.7k\Omega}{2.7k + R_3} (17 - 0.7V)$$

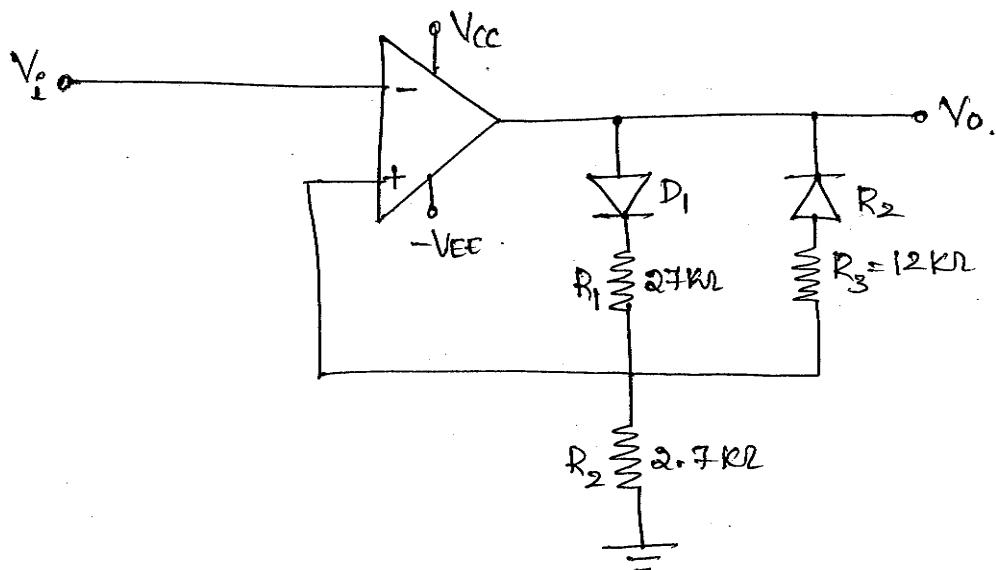
$$3R_3 + 8.1 \times 10^3 = 2.7k\Omega (16.3V)$$

$$3R_3 = 44.01 \times 10^3 - 8.1 \times 10^3$$

$$R_3 = \frac{35.91 \times 10^3}{3} = 11.97k\Omega$$

choose.

$$R_3 = 12k\Omega$$



Astable Multivibrator :- (Free running Multivibrator)

- 1) Sketch the ckt of an op-amp astable multivibrator, show the voltage waveforms at various points in the ckt and explain its operation.

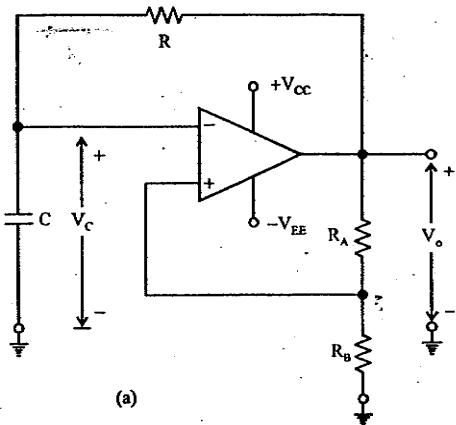
Dec - 10, 6M

Jan - 09, 6M (EE)

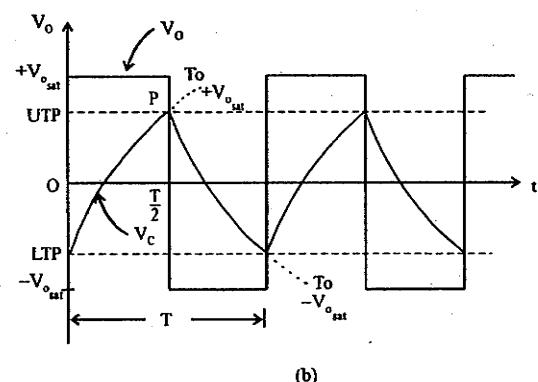
Jan - 10, 6M (EE)

June - 08, 5m (EE)

Jan - 08, 8M (EE)



(a)



(b) Output voltage and capacitor voltage waveforms

Fig. 6.31 : (a) Astable multivibrator circuit,

* Astable multivibrator is also called as free-running multivibrator (\because it has no ILP). The op voltage continuously switches between high & low levels without any ILP. It has no stable state.

* The op-amp resistors R₁ and R₂ constitutes an INV schmitt trigger circuit. The ILP voltage to the schmitt trigger circuit is the voltage across the capacitor C.



Operation :

Let the capacitor voltage be initially zero i.e. $V_c = 0$ and let $V_o = +V_{sat}$. Due to positive feedback, the potential at point B in fig ① is given by

$$V_B = \frac{R_2}{R_1 + R_2} V_{sat} = UTP$$

- * The capacitor 'c' charges exponentially with a time constant equal to RC with a polarity '+' on top. When the capacitor voltage V_c just crosses the UTP voltage, the o/p V_o rapidly changes from $+V_{sat}$ to $-V_{sat}$. Now o/p voltage $V_o = -V_{sat}$. The voltage at point B is given by :

$$V_B = \frac{R_2}{R_1 + R_2} -V_{sat} = LTP$$

$$V_c = -V_{sat}$$

- * Now the capacitor discharges to zero & starts charging in the reverse direction due to o/p V_o being at $-V_{sat}$. The capacitor voltage increases negatively towards $-V_{sat}$. When V_c just crosses LTP voltage, the o/p V_o rapidly changes from $-V_{sat}$ to $+V_{sat}$ thus producing a symmetrical square wave o/p V_o as shown in fig ②.



Design :-

- * The minimum current flowing through R is chosen to be 100 times the op-amp input bias current $I_B(\text{max})$.

$$I_1 = 100 \times I_B(\text{max})$$

- * The resistor R is then calculated as :

$$R = \frac{|V_o| - UTP}{I_1}$$

- * The capacitance C_1 is

$$C = \frac{I_1 \times t}{\Delta V}$$

Where $t = T/2$ &

$$\Delta V = UTP - LTP$$

$$C = \frac{I_1 \times T/2}{(UTP - LTP)}$$

- * For BIFET op-amp, the capacitor C_1 is first chosen to be much greater than stray capacitance.

- * Explain the operation of an op-amp based astable multivibrator. use relevant waveforms.

Dec-10, 6M



- * Explain working of an op-amp based multivibrator. Show that $T = 2RC \ln \frac{(1+\beta)}{(1-\beta)}$ where β is feedback ratio.

June-05, 8M(EE)

1st Explain Astable multivibrator

- * The charging of capacitor is exponential & the capacitor voltage at any instant is given by:

$$V_{C1} = V_f + (V_i - V_f) e^{-t/\tau} \rightarrow ①$$

Where $\tau = RC$ time constant of charging.

V_f = final value of capacitor voltage.

$\therefore V_f = +V_{sat}$ in the interval $0 < t < T/2$

V_i = initial value of the capacitor voltage

$$\therefore V_i = -\frac{R_2}{R_1 + R_2} V_{sat}$$

(where $\beta = \frac{R_2}{R_1 + R_2}$)

$$V_i = -\beta V_{sat}$$

Now eq ① becomes.

$$V_{C1} = +V_{sat} + [-\beta V_{sat} - V_{sat}] e^{-\frac{t}{RC}}$$

$$= +V_{sat} + [-V_{sat}(1+\beta)] e^{-\frac{t}{RC}}$$

$$V_{C1} = +V_{sat} [1 - (1+\beta) e^{-t/RC}] \rightarrow ②$$



At $t = T/2$, $V_c = +\beta V_{sat}$

Now eq ② becomes

$$\beta V_{sat} = V_{sat} \left[1 - (1+\beta) e^{-\frac{T}{2RC}} \right]$$

$$\beta = 1 - (1+\beta) e^{-\frac{T}{2RC}}$$

$$(1+\beta) e^{-\frac{T}{2RC}} = 1-\beta.$$

$$e^{-\frac{T}{2RC}} = \frac{(1-\beta)}{(1+\beta)}$$

Taking natural log on both sides of eq ③, we get,

$$-\frac{T}{2RC} = \ln \frac{(1-\beta)}{(1+\beta)}$$

$$T = -2RC \ln \left(\frac{1-\beta}{1+\beta} \right)$$

$$T = +2RC \ln \left(\frac{1+\beta}{1-\beta} \right) \rightarrow ④$$



- * For a astable multivibrator, show that frequency of o/p waveform is $f = \frac{1}{2RC}$ for a symmetric opp square wave. Show the ckt.

June - 09, EEE (C)

Sol:

- * The charging of capacitor is exponential & the capacitor voltage at any instant is given by:

$$V_C = V_f + (V_i - V_f) e^{-t/\tau} \rightarrow ①$$

Where $\tau = RC$ time constant of charging.

V_f = final value of capacitor voltage.

$\therefore V_f = +V_{sat}$ in the interval $0 < t < T/2$

V_i = initial value of the capacitor voltage

$$\therefore V_i = -\frac{R_2}{R_1 + R_2} V_{sat}$$

(where $\beta = \frac{R_2}{R_1 + R_2}$)

$$V_i = -\beta V_{sat}$$

Now eq ① becomes.

$$V_{C1} = +V_{sat} + [-\beta V_{sat} - V_{sat}] e^{-\frac{t}{R_1 C_1}}$$

$$= +V_{sat} + [-V_{sat}(1+\beta)] e^{-\frac{t}{R_1 C_1}}$$

$$V_{C1} = +V_{sat} [1 - (1+\beta) e^{-\frac{t}{R_1 C_1}}] \rightarrow ②$$

$$\text{At } t = T/2, V_c = +\beta V_{sat}$$

Now eq ② becomes



$$\beta V_{sat} = V_{sat} \left[1 - (1+\beta) e^{-\frac{T}{2RC}} \right]$$

$$\beta = 1 - (1+\beta) e^{-\frac{T}{2RC}}$$

$$(1+\beta) e^{-\frac{T}{2RC}} = 1-\beta$$

$$e^{-\frac{T}{2RC}} = \frac{(1-\beta)}{(1+\beta)} \rightarrow \textcircled{3}$$

Taking natural log on both sides of eq \textcircled{3}, we get,

$$-\frac{T}{2RC} = \ln \frac{(1-\beta)}{(1+\beta)}$$

$$T = -2RC \ln \left(\frac{1-\beta}{1+\beta} \right)$$

$$T = +2RC \ln \left(\frac{1+\beta}{1-\beta} \right) \rightarrow \textcircled{4}$$

Now if $\beta = 0.47$ in eq \textcircled{4}, then

$$T = 2RC \ln \left(\frac{1+0.47}{1-0.47} \right)$$

$$T = 2RC \ln (2.77)$$

$$T = 2RC(1)$$

$$T = 2RC$$

$$P = \frac{1}{2RC}$$

WKT

$$P = \frac{1}{T}$$



ARUNKUMAR G M.Tech, *Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.*



FORMULAE :-Astable Multivibrator

1) Let $I_1 = 100 \times I_B(\text{max})$.

2) $R_2 = \frac{V_{D2}}{I_1}$

3) $R_1 = \frac{V_{sat} - V_{D2}}{I_1}$

4) $R = \frac{V_{sat} - UTP}{I_1}$

5) $C = \frac{I_1 \times t}{\Delta V}$

Where $t = T/2$

$$\Delta V = UTP - LTP$$

6) $f = \frac{1}{2RC}$

7) $T = 2RC \ln \left(\frac{1+B}{1-B} \right)$

Where $B = \frac{R_2}{R_1 + R_2}$

8) $T = T_{ON} + T_{OFF}$

$$f = \frac{1}{T}$$



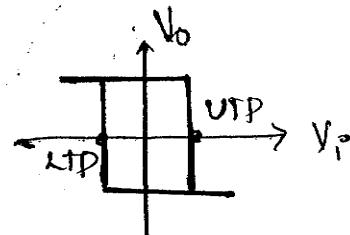
1) Design an Astable multivibrator that can produce an op with $t_{ON} = t_{OFF} = 1\text{ msec}$. The op-amp is driven with a $\pm 15\text{V}$ supply. Draw waveforms across capacitor, feedback and output. The hysteresis should not exceed 0.1V .

Jan-09, 6M

Given :- $V_H = 0.1\text{V}$

$$\text{UTP} - \text{LTP} = 0.1\text{V}$$

$$\text{If } \text{UTP} = \text{LTP} = \frac{0.1\text{V}}{2} = 0.05\text{V}$$



$$t_{ON} = t_{OFF} = 1\text{ msec}$$

$$V_{cc} = 15\text{V}, -V_{EE} = -15\text{V}$$

$$V_{sat} = (V_{cc} - 1) = 15\text{V} - 1\text{V} = 14\text{V}$$

Sol :- For 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

$$V_{R2} = \text{UTP} = 0.05\text{V}$$

* Let $I_1 = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$I_1 = 50\text{mA}$$

$$* R_2 = \frac{V_{R2}}{I_1} = \frac{\text{UTP}}{50\text{mA}} = \frac{0.05\text{V}}{50\text{mA}}$$

$$R_2 = 1\text{k}\Omega$$

$$* R_1 = \frac{V_{sat} - V_{R2}}{I_1} = \frac{14\text{V} - 0.05\text{V}}{50\text{mA}} = 279\text{k}\Omega$$

choose

$$R_1 = 270\text{k}\Omega$$



$$* R = \frac{V_{sat} - UTP}{I} = \frac{14V - 0.05V}{50\mu A} = \underline{\underline{279k\Omega}}$$

choose R = 270k\Omega

$$* C = \frac{I_1 \times t}{\Delta V}$$

$$t = T/2$$

$$T = t_{ON} + t_{OFF} = 1\text{msec} + 1\text{msec} = 2\text{msec}$$

$$t = \frac{T}{2} = \frac{2\text{msec}}{2}$$

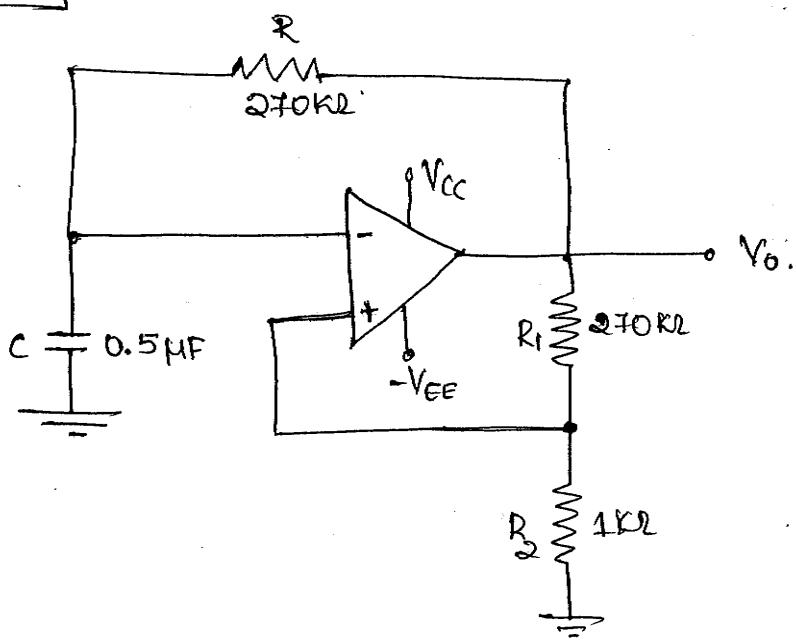
$$* t = 1\text{msec}$$

$$* \Delta V = UTP - LTP = 0.05V - (-0.05V)$$

$$\Delta V = 0.1V$$

$$C = \frac{50\mu A \times 1\text{msec}}{0.1V}$$

$$C = 0.5\mu F$$



2) An op-amp astable multivibrator circuit is to have a 4 KHz. output with an amplitude of ± 14 Volts using a ± 15 V supply. Using a bipolar op-amp, design a suitable ckt.

Given :- $f = 4 \text{ KHz}$, $\pm V_{\text{sat}} = \pm 14 \text{ V}$

Sol :- Assuming $UTP = |LTP| = 0.5 \text{ V}$

for 741 op-amp $I_B(\text{max}) = 500 \text{nA}$

$$* V_{R2} = UTP = 0.5 \text{ V}$$

$$\Delta V = UTP - LTP = 0.5 \text{ V} - (-0.5 \text{ V})$$

$$\boxed{\Delta V = 1 \text{ V}}$$

$$* T = \frac{1}{f} = \frac{1}{4 \text{ KHz}} = \underline{250 \mu\text{sec}}$$

$$t = \frac{T}{2} = \frac{250 \mu\text{sec}}{2}$$

$$\boxed{t = 125 \mu\text{sec}}$$

$$* \text{Let } I_I = 100 \times 500 \text{nA}$$

$$\boxed{I_I = 50 \mu\text{A}}$$

$$* R_2 = \frac{V_{R2}}{I_I} = \frac{UTP}{50 \mu\text{A}} = \frac{0.5 \text{ V}}{50 \mu\text{A}} = 10 \text{ k}\Omega$$

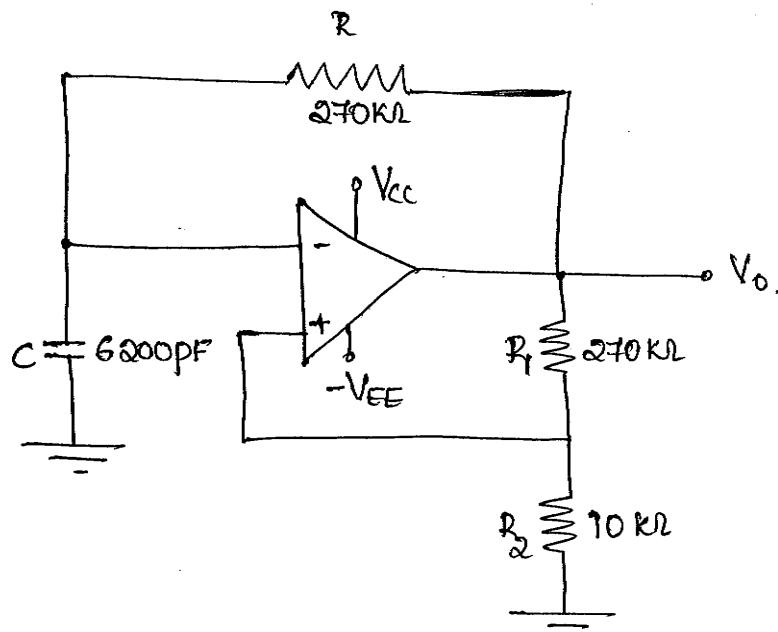
$$\boxed{R_2 = 10 \text{ k}\Omega}$$

$$* R = R_I = \frac{V_{\text{sat}} - V_{R2}}{I_I} = \frac{14 \text{ V} - 0.5 \text{ V}}{50 \mu\text{A}} = \underline{270 \text{ k}\Omega}$$



$$* C_2 = \frac{I_1 \times t}{\Delta V} = \frac{50 \mu A \times 125 \mu sec}{1V} = 6250 \text{ pF}$$

choose. $C = 6200 \text{ pF}$



Design of Astable multivibrator using BIFET Op-amp:

1) Select UTP & LTP $\ll V_o$.

$$\text{Let } |UTP| = |LTP| \approx 0.5 \text{ V}$$

2) $V_{cc} = (V_o + 1 \text{ V})$

3) For BIFET select $R_1 = 1 \text{ M}\Omega$

4) $I_2 = \frac{|V_o| - UTP}{R_1}$

5) $R_2 = \frac{V_{R2}}{I_2}$

6) Let $C = 0.1 \text{ nF}$

7) $t = \frac{1}{2f}$

8) $C = \frac{I_1 t}{\Delta V}$

$$I_1 = \frac{C \cdot \Delta V}{t}$$

Where $\Delta V = (UTP - LTP)$

9) $R = \frac{V_o - UTP}{I_1}$



1) Using a BIFET op-amp, design an astable multivibrator to have a $\pm 9V$ output with a frequency of 1kHz.

Given : $V_o = \pm 9V$, $f = 1\text{kHz}$

Sol :

* select UTP & LTP $\ll V_o$.

$$\text{Let } |UTP| = |LTP| = 0.5V.$$

$$\text{Let } R_1 = 1M\Omega$$

$$* I_2 = \frac{|V_o| - UTP}{R_1} = \frac{9V - 0.5V}{1M\Omega}$$

$$I_2 = 8.5\text{ mA}$$

$$* R_2 = \frac{V_{R2}}{I_2} = \frac{UTP}{I_2} = \frac{0.5V}{8.5\text{ mA}} = 59k\Omega$$

$$\text{choose } R_2 = 56k\Omega$$

$$* \text{let } C = 0.1\text{ nF}$$

$$* t = \frac{1}{2f} = \frac{1}{2 \times 1\text{kHz}}$$

$$t = 500\mu\text{sec}$$

$$\Delta V = UTP - (-LTP) = 0.5V - (-0.5V)$$

$$\Delta V = 1V$$

$$* I_1 = \frac{C \Delta V}{t} = \frac{0.1\text{ nF} \times 1V}{500\mu\text{sec}} = \underline{\underline{200\mu\text{A}}}$$

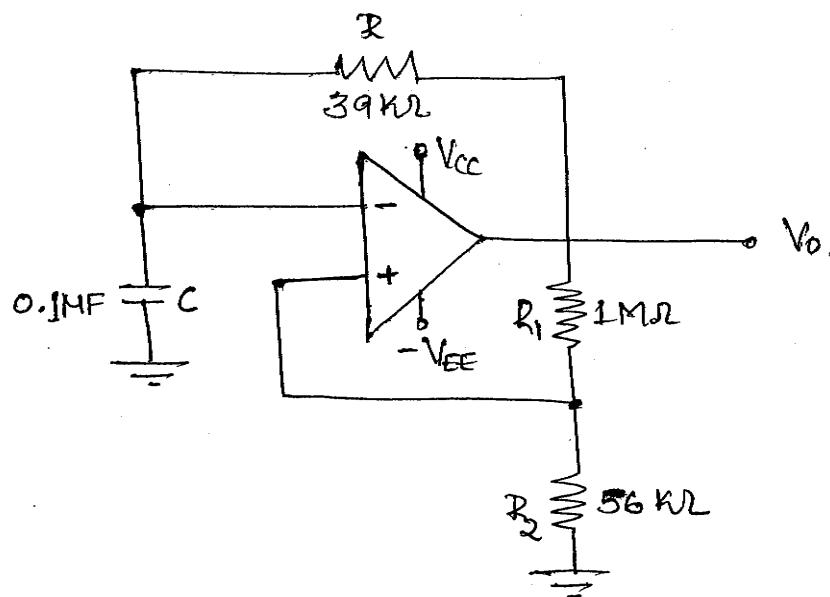


$$* R = \frac{V_o - UTP}{I_i}$$

$$= \frac{9V - 0.5V}{200\mu A}$$

$$R = \underline{42.5 k\Omega}$$

choose. R = 39 k\Omega



Monostable Multivibrator :-

1) Draw the ckt of an op-amp monostable multivibrator & explain its operation

June - 08, 7M

2) With a neat ckt diagram & waveforms derive an expression for pulse width of monostable multivibrator using op-amp.

Model - 1, 8M

June - 10, 10 M(EE)

June - 09, 7M(EE)

June - 07, 8 M(EE)

Jan - 05, 8 M(EE)

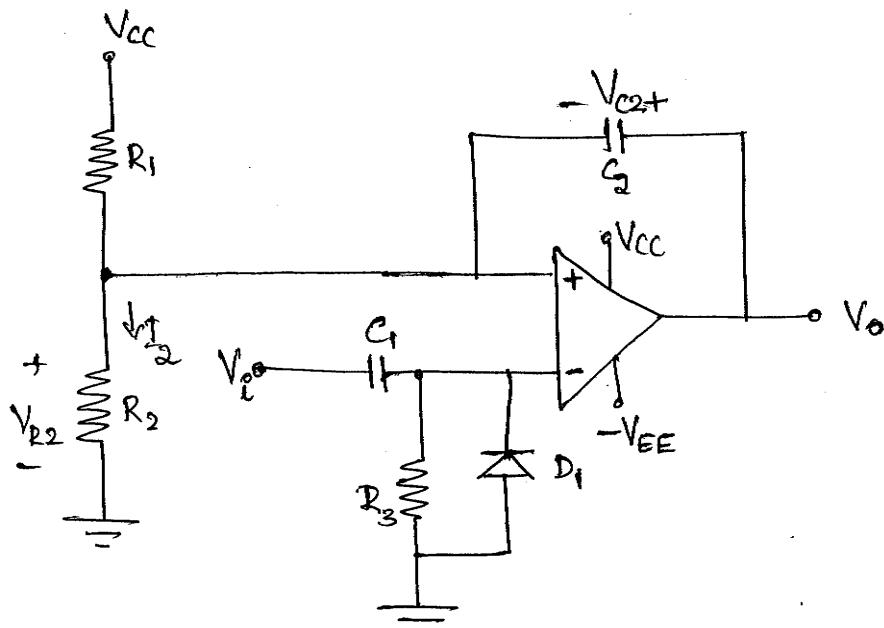


Fig
Bell \rightarrow 230

fig ① : Monostable multivibrator and ckt waveforms.

- * A monostable multivibrator has only one stable off state. In this stable state, the opv voltage may be high or low, and it remains in this state until the multivibrator is triggered.

Operation :-

Before the application of trigger pulse, the INV input terminal of op-amp is grounded through resistor R_3 . The Non-INV terminal is connected to voltage divider ckt of R_1 & R_2 connected to $+V_{CC}$.



- * the voltage V_{R2} across R_2 at Non-INV terminal is higher than INV terminal voltage & the o/p voltage is held at $+V_{sat}$ and capacitor C_2 is charged with the polarity shown in fig ①.
- * The I/p positive trigger pulse is now applied to the differentiating circuit of R_3 & C_1 to produce positive and negative spikes at the op-amp INV terminal as shown in fig 1.
- * The negative spike is clipped at $-0.7V$ by diode D_1 , so that it has no effect on the circuit.

The +ve spike rises the voltage at the INV I/p terminal beyond that at the Non-INV terminal and op-amp o/p switches to $-V_{sat}$.

- * The spikes has a relatively short time duration, so the INV I/p terminal quickly returns to the zero voltage level.

When o/p goes to $-V_{sat}$, the Non-INV I/p terminal voltage is held at a -ve potential of

$$V_f = -V_{sat} - V_{C2}$$

- * Now capacitor C_2 discharges via R_1 and R_2 thus gradually raising the Non-INV I/p terminal toward ground level. When the Non-INV terminal voltage goes slightly above ground, the op-amp o/p immediately switches back to $+V_{sat}$. & the ckt is returned to its original state.



- * The ckt produces a negative going o/p pulse each time it is triggered. The pulse width (PW) of the o/p depends on C_1 , V_{R2} & the resistance of R_1 & R_2 .

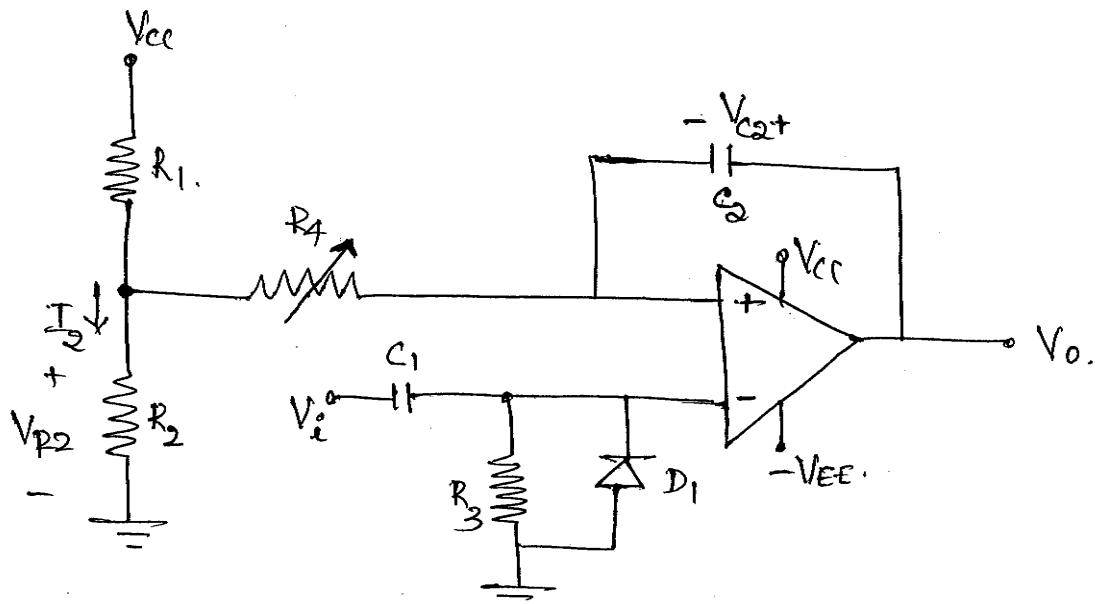


fig ② Modification to provide pulse-width adjustment.

- * To control the pulse width (PW) a resistor R_4 can be included in the ckt as shown in fig ②.

The total resistance in series with the capacitor is now $(R_4 + R_1 \parallel R_2)$. Usually, R_4 is selected to be much larger than $(R_1 \parallel R_2)$. So that the capacitor charge/discharge resistance is effectively R_4 .

- * By adjusting R_4 , the charge/discharge time can be altered thus controlling the o/p pulse width.

Design:-

- 1) Let $I_Q = 100 \times I_B(\text{max})$
- 2) The voltage V_{R2} is chosen to be in the range 0.5 to 1 Volts.



$$R_2 = \frac{V_{R2}}{I_2}$$

3) Determine R_1 .

Applying KVL from V_{CC} , R_1 & R_2

$$V_{CC} - I_2 R_1 - I_2 R_2 = 0.$$

$$V_{CC} - I_2 R_2 - V_{R2} = 0$$

$$I_2 R_2 = V_{CC} - V_{R2}$$

$$R_2 = \frac{V_{CC} - V_{R2}}{I_2}$$

4). To design the differentiator ckt, the time constant $R_3 C_1$ is assumed to be 10% of input pulse width 't' to generate suitable spikes from the pulses.

$$R_3 C_1 = 10\% \text{ of } t$$

$$R_3 C_1 = 0.1 t$$

$$C_1 = \frac{0.1 t}{R_3}$$

Q. C_1 might be first selected much larger than stray capacitance then R_3 can be calculated from below equation. i.e.

$$R_3 = \frac{0.1 t}{C_1}$$

* $R_3 = \frac{0.1 V_{BE}}{I_B(\text{max})}$



- * The capacitance C_2 is given by.

$$C_2 = \frac{PW}{(R_1 \parallel R_2) \ln [(E - E_0)/(E - e_c)]}$$

where
 $PW \rightarrow$ desired off pulse width
 $E \rightarrow$ capacitor charging voltage &
 $E_0 \rightarrow$ initial capacitor voltage before triggering

- * $E = V_{R2} + V_{sat}$
- * $E_0 = V_{R2} - V_{sat}$
- * The final capacitor voltage e_c is

$e_c = V_{sat}$



1) Design a monostable multivibrator circuit to have an off pulse width of 1sec when triggered by a 2V, 100 usec input pulse. Use a 741 op-amp with a $\pm 12V$ supply.

Given: $V_{cc} = 12V$, $PWL = 1\text{ msec}$

$$V_{sat} = (V_{cc} - 1V) = (12V - 1V)$$

$$\boxed{V_{sat} = 11V} \quad \text{by} \quad \boxed{-V_{sat} = -11V}$$

$$V_i = 2V, t = 100\text{ usec.}$$

Sol: - For 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

* Let $\boxed{V_{R2} = 0.5V}$

* Let $\frac{I_2}{2} = 100 \times I_B(\text{max}) = 100 \times 500\text{nA}$

$$\boxed{I_2 = 50\mu A}$$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{0.5V}{50\mu A}$

$$\boxed{R_2 = 10k\Omega}$$

* $R_1 = \frac{V_{cc} - V_{R2}}{\frac{I_2}{2}} = \frac{12V - 0.5V}{50\mu A} = 230k\Omega$

choose, $\boxed{R_1 = 220k\Omega}$

* $E = V_{R2} + V_{sat} = 0.5V + 11V$

$$\boxed{E = 11.5V}$$

* $E_0 = V_{R2} - V_{sat} = 0.5V - 11V$

$$\boxed{E_0 = -10.5V}$$



* $e_c = V_{sat}$

$e_c = 11V$

* $C_Q = \frac{P_W}{(R_1 || R_2) \ln \left[\frac{(E - E_0)}{(E - e_c)} \right]} = \frac{1 \text{ m sec}}{(220k || 10k) \ln \left[\frac{11.5V - (-10.5V)}{11.5V - 11V} \right]}$

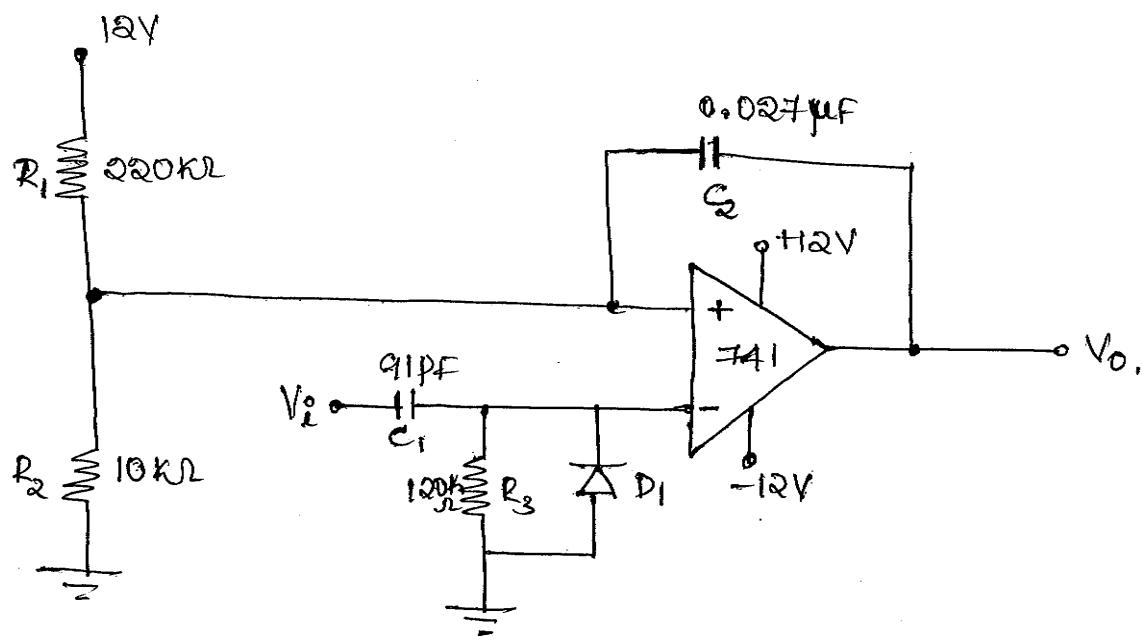
$C_Q = 0.027 \mu F$

* $R_3(\max) = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7V}{500 \text{ nA}} = 140k\Omega$

choose $R_3(\max) = 120k\Omega$

* $C_1 = \frac{0.1 t}{R_3} = \frac{0.1 \times 100 \mu \text{sec}}{120k\Omega} = 83 \mu \text{F}$

choose $C_1 = 91 \mu \text{F}$





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Filters :

Filters are circuits that pass only a desired band of frequencies & attenuates the undesired band of frequencies.

The filters are classified as :

- 1) Low pass filter.
- 2) High pass filter.
- 3) Band pass filter and
- 4) Band elimination or band reject or Band stop filter.

Filters can be of passive or active type.

Passive filters use only passive components such as resistors, capacitors & inductors.

Active filters use transistor or op-amps together with passive components. Active filters are further defined in terms of rate at which off fall off at the edge of the frequency range.

* If the fall off rate is 20dB/decade, the filters are called as first order filters.

If the fall off rate is 40dB/ decade, the filters are called as Second order filters.

If the fall off rate is 60dB/ decade, the filters are called as third order filters.



Advantages of active filters over passive filters :-

1) What are the advantages of active filters over passive filters?

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- 1) Because of high input impedance & low off impedance of op-amp, the active filter does not cause loading of the source or load.
- 2) Active filters are more economical because of absence of inductors. (Inductors are bulky, costly & dissipate more power).
- 3) Due to availability of modern ICs, a variety of cheaper op-amps are available.
- 4) The op-amp gain can be easily controlled in the closed loop fashion, hence active filter input signal is not attenuated.
- 5) The active filter is easier to tune or adjust to any frequency compared to passive filters.
- 6) Active filter has excellent isolation between source and load.



First order Low pass Active filter :-

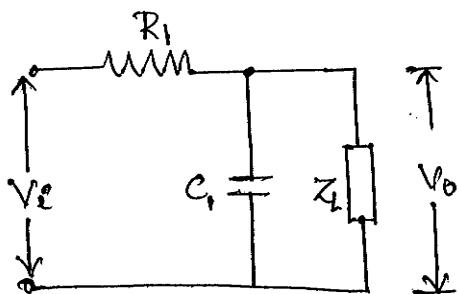


fig @ : passive low-pass filter.

A passive low pass filter ckt consisting of a resistor & a capacitor is shown in fig @. The filter load ' Z_L ' is connected in parallel with a capacitor C_1 . Unless $Z_L \gg X_{C1}$, the load is likely to affect the filter performance.

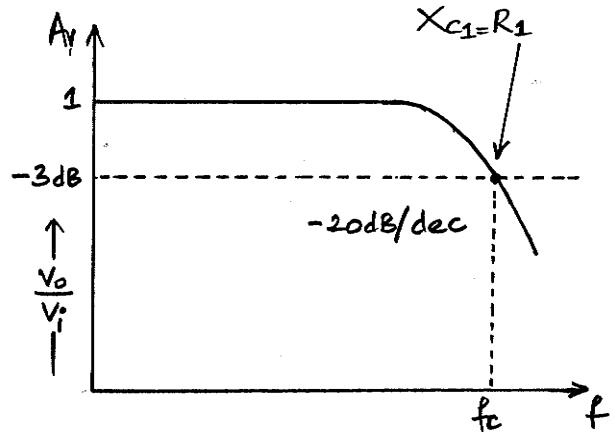
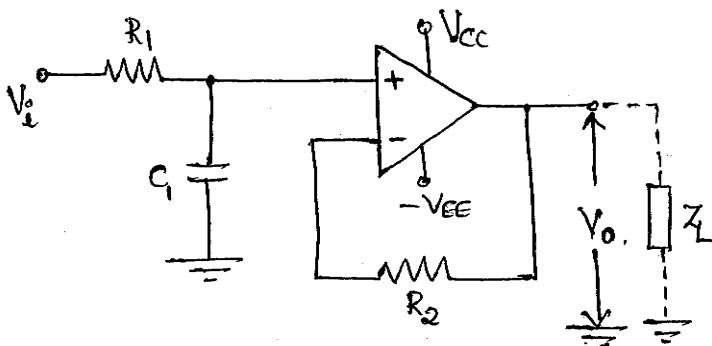


fig @ : Active low-pass filter.

* Connecting a voltage follower to ckt of fig @ eliminates the load problem and converts the circuit into an active filter.

* The o/p voltage V_o of the active filter is given by : from fig @.

$$V_o = I \times (-jX_{C1})$$

$$= \frac{V_i}{R_1 - jX_{C1}} \cdot -jX_{C1}$$



$$\text{Taking magnitude, } V_o = V_i \cdot \frac{\sqrt{x_{C1}^2}}{\sqrt{R_1^2 + X_{C1}^2}} = V_i \cdot \frac{X_{C1}}{\sqrt{R_1^2 + X_{C1}^2}}$$

$$\boxed{\frac{V_o}{V_i} = \frac{X_{C1}}{\sqrt{R_1^2 + X_{C1}^2}}} \rightarrow \textcircled{1}$$

- * At low frequencies, $X_{C1} \gg R_1$, so eq \textcircled{1} gives the gain as approximately $\underline{1}$.
- * At higher frequencies, $X_{C1} \approx R_1$, the gain decreases.
- The frequency at which the o/p voltage is down by 3dB from its pass frequency is defined as cut-off frequency 'f_c' of the filter.
- * In fig \textcircled{1}, f_c is the frequency at which $X_{C1} = R_1$

Now eq \textcircled{1} becomes

$$\boxed{A_V = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}}}$$

$$\left\{ \begin{aligned} \because \frac{V_o}{V_i} &= \frac{X_{C1}}{\sqrt{R_1^2 + X_{C1}^2}} = \frac{X_{C1}}{\sqrt{X_{C1}^2 + X_{C1}^2}} \\ &= \frac{X_{C1}}{\sqrt{2} X_{C1}^2} = \frac{X_{C1}}{X_{C1} \sqrt{2}}. \end{aligned} \right.$$

$$\left. \frac{V_o}{V_i} = \frac{1}{\sqrt{2}}. \right\}$$

- * At frequencies higher than f_c, the gain of the ckt falls off at a rate of 20dB/decade i.e. a fall of 20 dB each time the frequency is increased by a factor of 10.



Design steps :-

$$1) R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$2) R_1 = R_2$$

$$3) X_{C1} = R_1 \text{ at } f_c.$$

$$\frac{1}{2\pi f_c C_1} = R_1.$$

$$C_1 = \frac{1}{2\pi f_c R_1}$$

1st order active low pass active filter :-FORMULAE :-

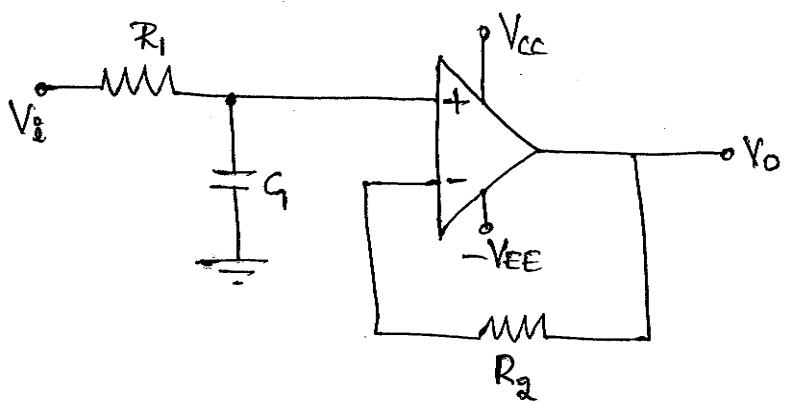
$$1) R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$2) R_1 = R_2$$

$$3) X_{C1} = R_1 \text{ at } f_c.$$

$$\frac{1}{2\pi f_c C_1} = R_1.$$

$$C_1 = \frac{1}{2\pi f_c R_1}$$



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↳ Using a 741 op-amp, design a first-order active low pass filter to have a cut off frequency of 1KHz.

Given: $f_c = 1\text{ KHz}$.

Sol :- For op-amp 741 : $I_B(\text{max}) = 500\text{nA}$

Assume $V_{BE} = 0.7\text{ V}$

$$* R_1 = \frac{0.1V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{ V}}{500\text{nA}}$$

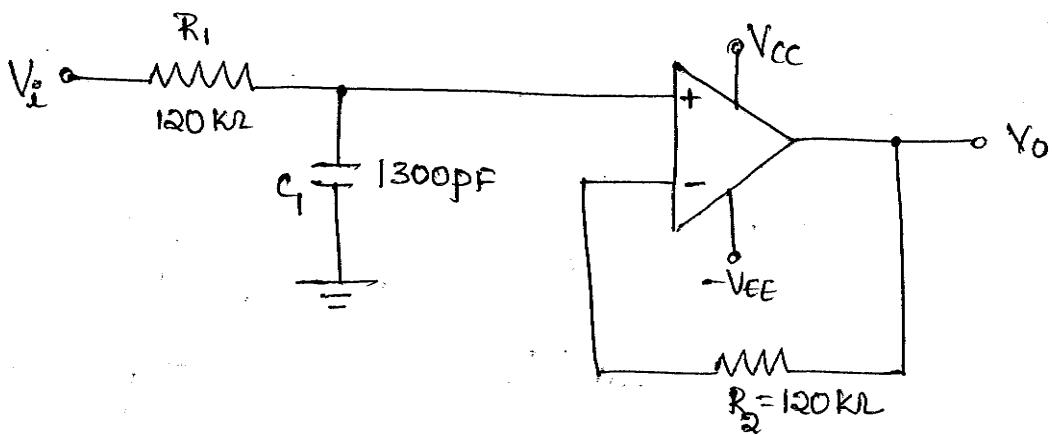
$$R_1 = 140\text{ k}\Omega$$

choose $R_1 = 120\text{ k}\Omega$

$$* R_2 = R_1 = 120\text{ k}\Omega$$

$$* C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 1\text{ KHz} \times 120\text{ k}\Omega} = 1326\text{ pF}$$

choose $C_1 = 1300\text{ pF}$



Q) Design a first order active low pass filter using 715 op-amp having a cut-off frequency of 4KHz.
 $[I_{B(\max)} = 1.5 \mu A \text{ for 715 op-amp}]$.

Given: $f_c = 4\text{KHz}$, $I_{B(\max)} = 1.5 \mu A$

Assume : $V_{BE} = 0.7\text{V}$

Sol :-

$$* R_1 = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7\text{V}}{1.5 \mu A} = 46.67\text{ k}\Omega$$

choose

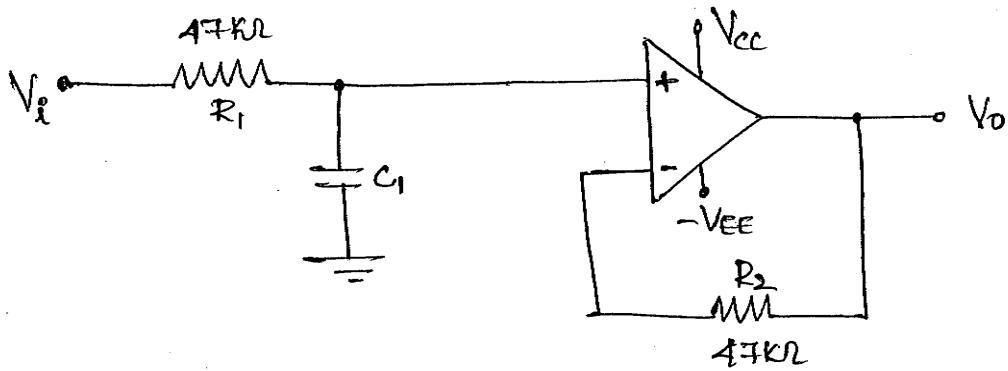
$$R_1 = 47\text{ k}\Omega$$

$$* R_2 = R_1 = 47\text{ k}\Omega$$

$$* C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 4\text{KHz} \times 47\text{ k}\Omega} = 846.57\text{ pF.}$$

choose.

$$C_1 = 820\text{ pF}$$



Second order Low-pass active filter :-

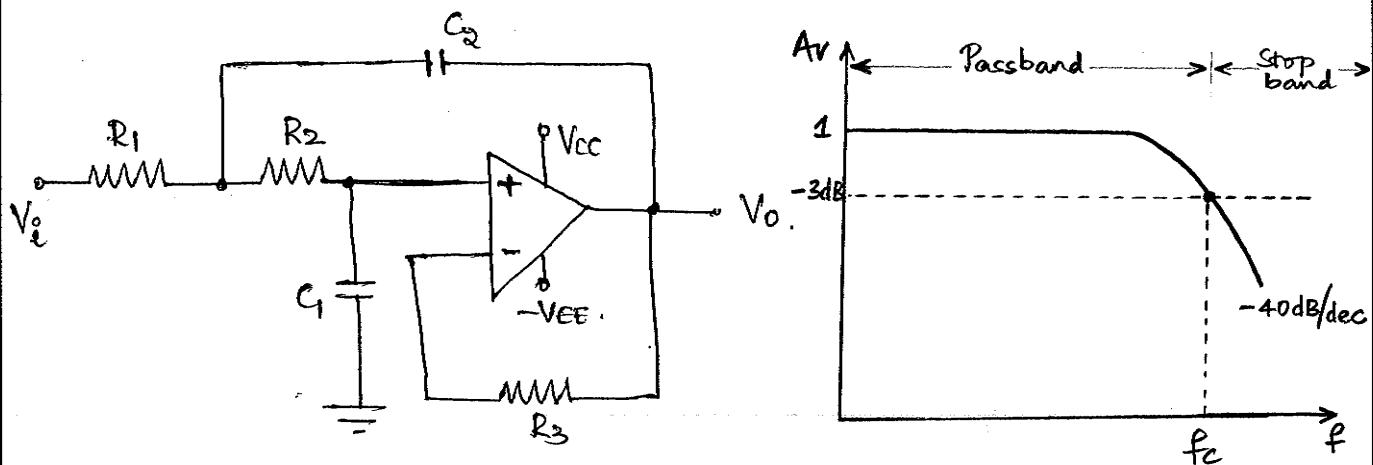


Fig @: Second order LPF ckt.

- * In first-order low pass filter after cutoff freq the voltage gain decreases at the rate of \$20\text{dB/decade}\$.
- { * In second-order low pass filter, after cut-off frequency, the voltage gain decreases at the rate of \$40\text{ dB/decade}\$. }
- * Fig @ shows a second order low pass filter, which has a frequency response that falls off at the rate of \$40\text{ dB}\$ per decade above the upper cut-off frequency.
- * This steeper roll-off rate is achieved by using the \$C_1 R_2\$ together with feedback from the op-amp via capacitor \$C_2\$ to the junction of \$R_1\$ and \$R_2\$.
- * At low frequencies, \$X_{C1}\$ & \$X_{C2}\$ are much larger than \$R_1\$ & \$R_2\$ and they have no effect on the ckt. So, the op-amp voltage is equal to the I/p giving a Voltage gain of 1 (\$\because A_v = \frac{V_o}{V_i}\$).



* At high frequencies, the effect of C_1 & R_2 causes the op-amp to fall off at a rate of 20dB per decade as the frequency increases.

* The R_2 & C_1 introduce a phase lag.

The C_2 combined with R_1 & R_2 introduces a phase lead.

The result of these phase differences is that the feedback via C_2 produces a further fall off of 20dB per decade.

This second order low pass filter produces a fall-off rate of 40dB per decade.

Design steps :-

$$1) R_1 + R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$2) R_1 = R_2$$

$$3) X_{C1} = \sqrt{2} R_2 \text{ at } f_c$$

$$\frac{1}{2\pi f_c C_1} = \sqrt{2} R_2$$

$$C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2}$$

$$4) R_3 = R_1 + R_2$$

$$5) C_2 = 2C_1$$



Second order low pass active filter :-FORMULAE

$$1) R_1 + R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})} \quad \text{usually } R_1 = R_2.$$

$$2) X_{C1} = \sqrt{2} R_2 \text{ at } f_c$$

$$\frac{1}{2\pi f_C C_1} = \sqrt{2} R_2$$

$$C_1 = \frac{1}{2\pi f_C \sqrt{2} R_2}$$

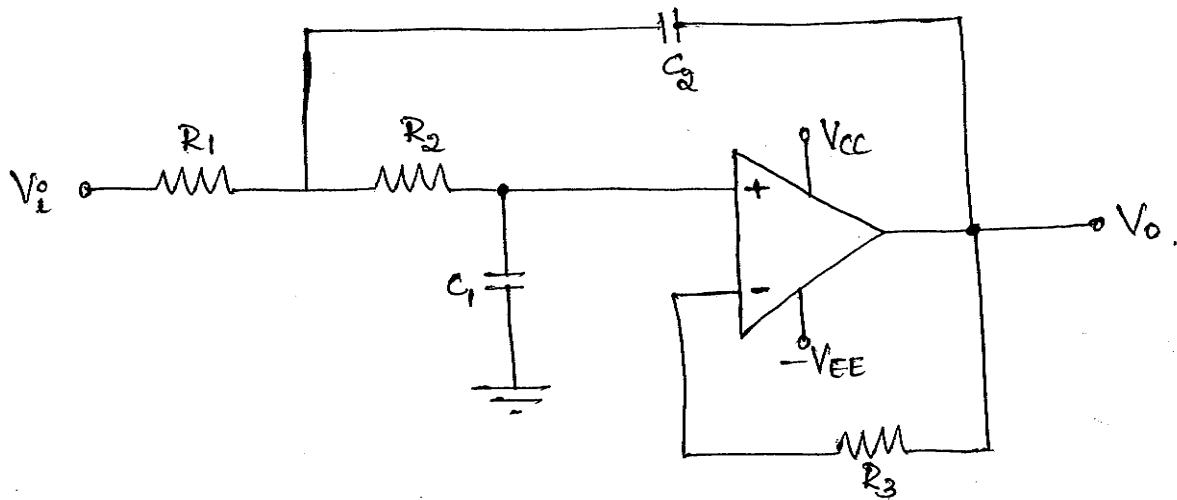
$$3) R_3 = R_1 + R_2$$

$$4) C_2 = 2C_1$$

NOTE :- The resistance R_1 satisfies the equation.

$$R_1 = \sqrt{2} X_{C2}$$

$$R_1 = \frac{\sqrt{2}}{2\pi f_C C_2}$$



PROBLEMS 8

1) Design a second order low pass filter circuit to have a cut-off frequency of 1kHz.

Given: $f_c = 1\text{kHz}$, assuming $V_{BE} = 0.7\text{V}$

Sol: for 741 op-amp : $I_B(\text{max}) = 500\text{nA}$.

$$* R_1 + R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}}$$

$$R_1 + R_2 = 140\text{k}\Omega, \quad R_1 = R_2 = \frac{140\text{k}\Omega}{2}$$

If $R_1 = R_2 = 70\text{k}\Omega$, choose std value

$$R_1 = R_2 = 68\text{k}\Omega$$

$$* R_3 = R_1 + R_2 = 68\text{k}\Omega + 68\text{k}\Omega$$

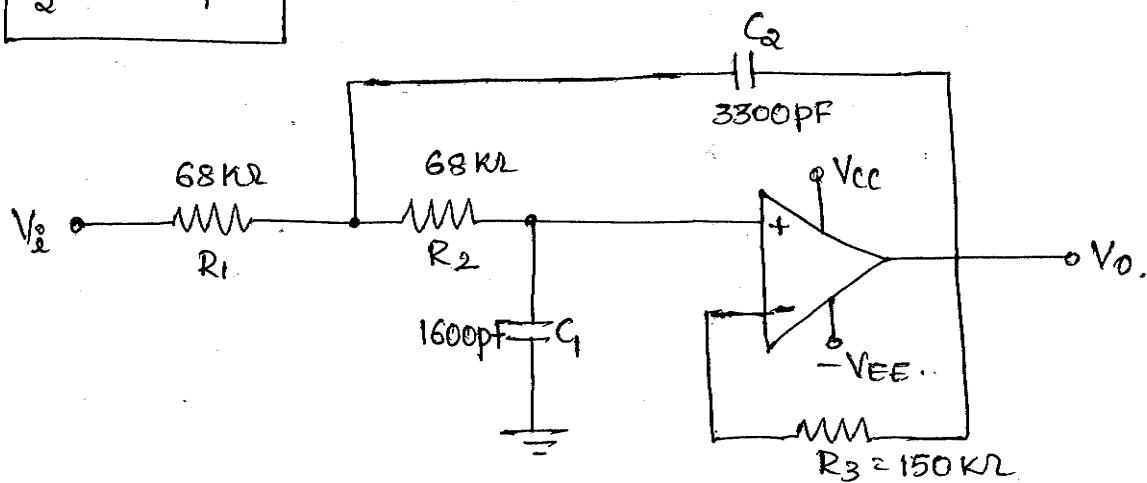
$$R_3 = 136\text{k}\Omega, \quad \text{choose } R_3 = 150\text{k}\Omega$$

$$* C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 1\text{kHz} \times \sqrt{2} \times 68\text{k}\Omega} = 1655\text{pF}$$

choose, $C_1 = 1600\text{pF}$

$$* C_2 = 2C_1 = 2 \times 1600\text{pF} = 3200\text{pF}$$

use $C_2 = 3300\text{pF}$



Q2) Design a Second order low pass Active filter having a cut-off frequency of 2.5 kHz. Use 709 op-amp.

Given :- $f_c = 2.5 \text{ kHz}$

For op-amp 709 : $I_B(\text{max}) = 200 \text{nA}$

Sol :-

$$* R_1 + R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \text{V} \times 0.7 \text{V}}{200 \text{nA}} = \underline{350 \text{k}\Omega}$$

$$R_1 = R_2 = \frac{350 \text{k}\Omega}{2} = 175 \text{k}\Omega$$

choose std value of $R_1 = R_2 = 180 \text{k}\Omega$

$$* R_3 = R_1 + R_2 = 180 \text{k}\Omega + 180 \text{k}\Omega = 360 \text{k}\Omega$$

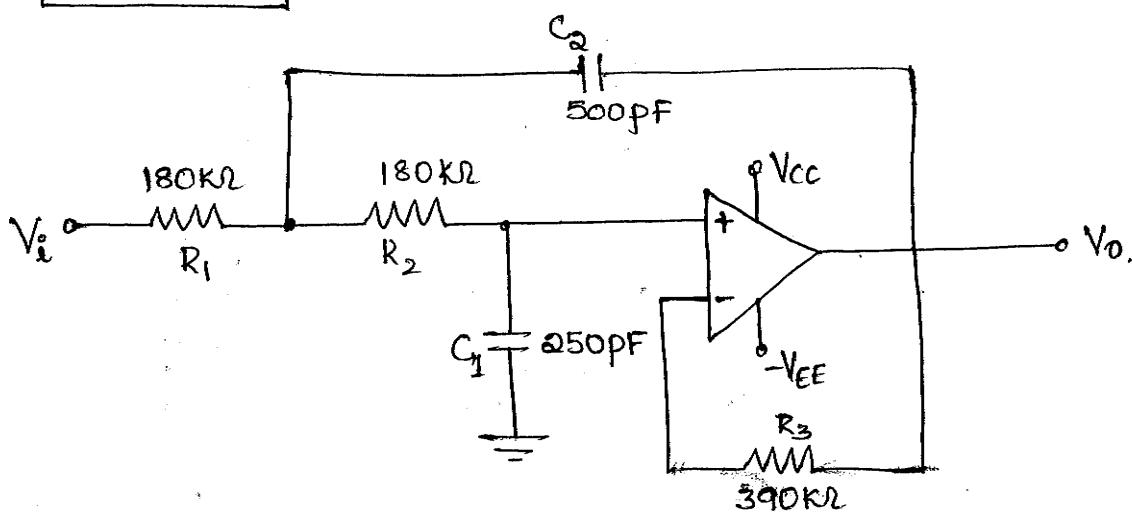
choose std value of $R_3 = 390 \text{k}\Omega$

$$* G = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 2.5 \text{kHz} \times \sqrt{2} \times 180 \text{k}\Omega}$$

$$C_1 = 250 \text{pF}$$

$$* C_2 = 2G = 2 \times 250 \text{pF}$$

$$C_2 = 500 \text{pF}$$



3) Using a 741 op-amp, design a second order low pass filter to have a cut-off frequency of 5 kHz.

Given: $f_C = 5 \text{ kHz}$

Jan - 09, 6M(EE)

Sol: For 741 op-amp: $I_B(\text{max}) = 500 \text{nA}$

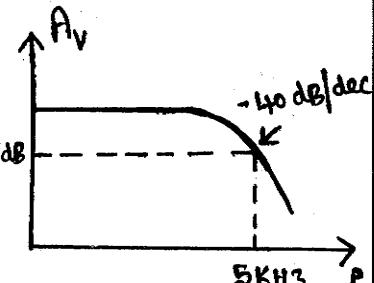
Dec - 10, 8M

Assume $V_{BE} = 0.7 \text{ V}$.

$$* R_1 + R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7 \text{ V}}{500 \text{nA}} = 140 \text{k}\Omega - 3 \text{dB}$$

$$R_1 = R_2 = \frac{140 \text{k}\Omega}{2} = 70 \text{k}\Omega$$

Use std value $R_1 = R_2 = 68 \text{k}\Omega$ ← (2m)



$$* R_3 = R_1 + R_2 = 68 \text{k}\Omega + 68 \text{k}\Omega = 136 \text{k}\Omega$$

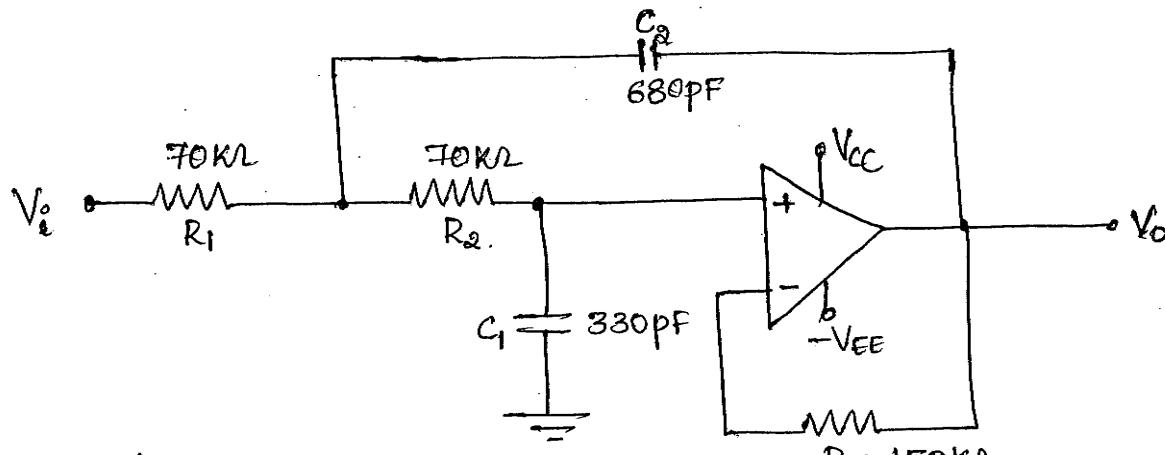
Use std value $R_3 = 150 \text{k}\Omega$ ← (1m)

$$* C_1 = \frac{1}{2\pi f_C \sqrt{2} R_2} = \frac{1}{2\pi \times 5 \text{kHz} \times \sqrt{2} \times 68 \text{k}\Omega} = 330.9 \text{ pF}$$

Use std value, $C_1 = 330 \text{ pF}$ ← (1 1/2 m)

$$* C_2 = 2C_1 = 2 \times 330 \text{ pF} = 660 \text{ pF}$$

Use std value $C_2 = 680 \text{ pF}$ ← (1 1/2 m)



Comment:- In 2nd order LPF after cut-off

frequency, the voltage gain decreases at the rate of 40 dB/decade.

* At cut-off freq., v/o gain drops by 3 dB from its maximum gain.



A) Design a second order low pass filter ckt to have a cutoff frequency of 2kHz. Draw the ckt & indicate the frequency response of the filter.

Jan-10, 10M

Given: $f_c = 2\text{kHz}$

SOL: For 741 op-amp: $I_B(\text{max}) = 500\text{nA}$

Assume: $V_{BE} = 0.7\text{V}$.

$$* R_1 + R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7\text{V}}{500\text{nA}} = 140\text{k}\Omega$$

$$R_1 = R_2 = \frac{140\text{k}\Omega}{2} = 70\text{k}\Omega$$

Use std value $R_1 = R_2 = 68\text{k}\Omega \leftarrow 9\text{m}$

$$* R_3 = R_1 + R_2 = 68\text{k}\Omega + 68\text{k}\Omega = 136\text{k}\Omega$$

Use std value $R_3 = 150\text{k}\Omega \leftarrow 1\text{m}$

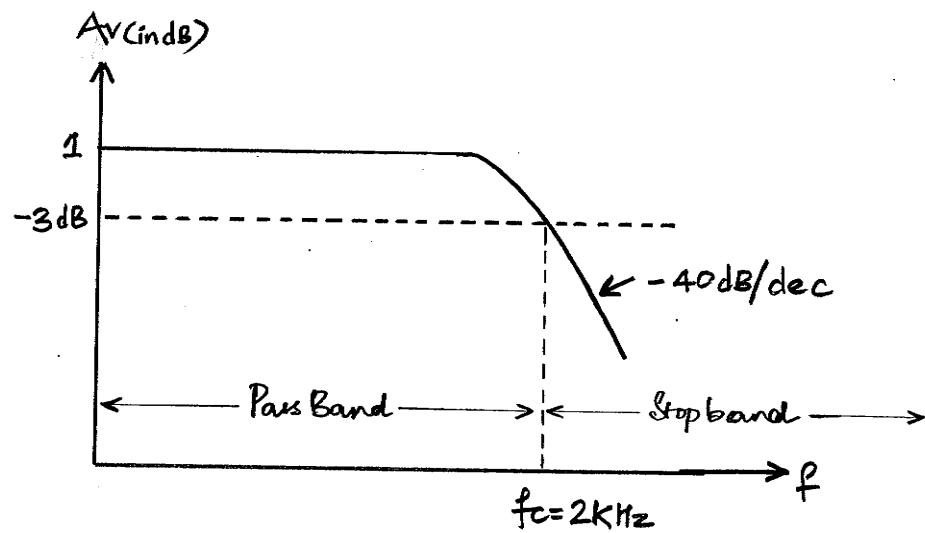
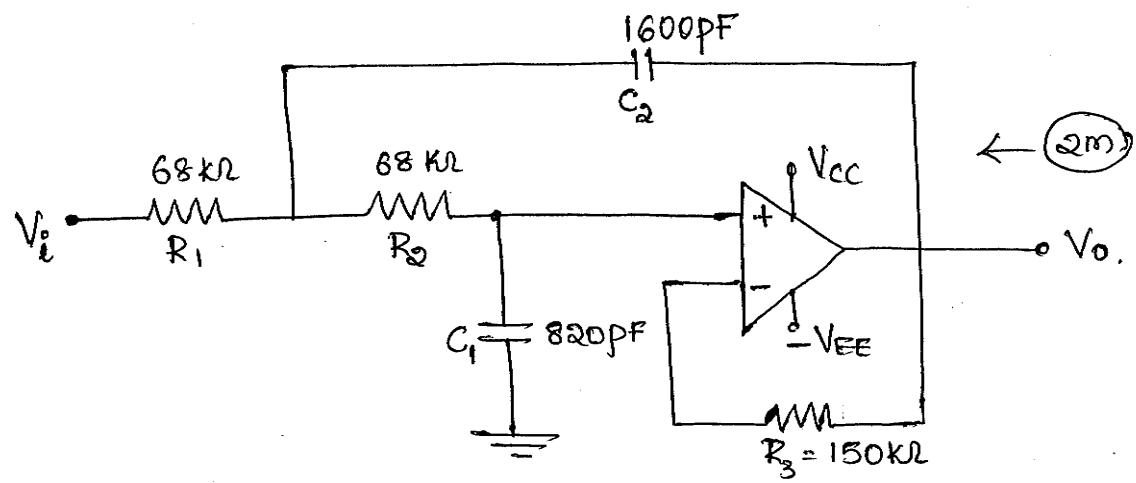
$$* C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 2\text{kHz} \times 68\text{k}\Omega \times \sqrt{2}} = 827.4\text{pF}$$

Use std value $C_1 = 820\text{pF} \leftarrow 1\frac{1}{2}\text{m}$

$$* C_2 = 2C_1 = 2 \times 820\text{pF} = 1640\text{pF}$$

Use std value $C_2 = 1600\text{pF} \leftarrow 1\frac{1}{2}\text{m}$





3) Design a 2nd order LPF using 741 for a cut-off frequency of 5kHz. Draw its frequency response & comment on the same.

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First order High pass Active filter :-

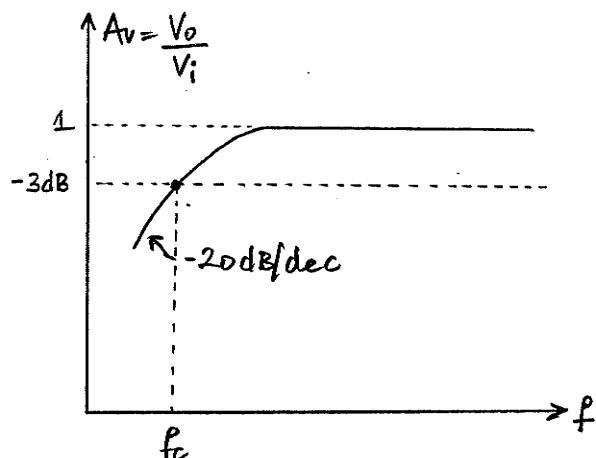
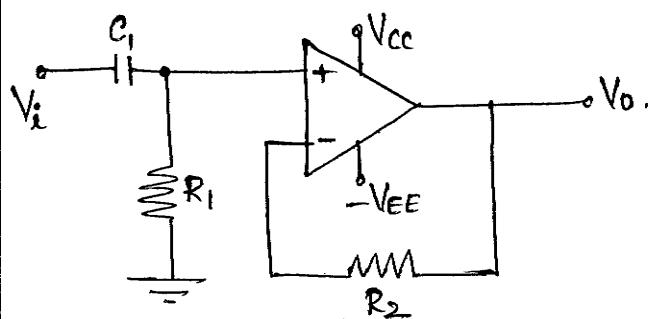


fig @ Active high pass filter.

- * The first order high pass filter can be obtained by interchanging the elements R_1 & C_1 in a first order low pass filter circuit.

In fig @, the voltage follower isolates the load from R_1 & C_1 .

- * At high frequencies, X_{C1} is very much smaller than R_1 & voltage gain V_o/V_i is almost equal to 1 or 0 dB.

- * When the frequency decreases to a value such that $X_{C1} = R_1$, the voltage gain drops by 3dB. As the frequency decreases further, the voltage gain rolls off at 20 dB per decade.

Design steps :

$$\text{1)} R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})} \quad \Leftrightarrow \quad R_2 = R_1.$$

$$\text{2)} X_{C1} = R_1 \text{ at } f_c.$$

$$\frac{1}{2\pi f_c C_1} = R_1 \quad \Leftrightarrow$$

$$C_1 = \frac{1}{2\pi f_c R_1}$$



FORMULAE :- 1st order HPF.

$$1) R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$2) R_2 = R_1$$

$$3) C_1 = \frac{1}{2\pi f_C R_1}$$

FOR BIFET op-amp.

FORMULAE :-

NOTE :- LM 108 has very low input bias current, it should be treated as BIFET op-amp.

1) Select C_1 , very much larger than stray capacitance.

i.e. $C_1 = 1000 \text{ pF}$

$$2) R_1 = \frac{1}{2\pi f_C C_1}$$

$$3) R_2 = R_1$$

4) For LM 108 op-amp, the unity gain frequency

$$f_u = 1 \text{ MHz}$$

i.e. $f_2 = \frac{f_u}{A_v} = 1 \text{ MHz}$



4) Design a first order active high-pass filter for a cut-off frequencies of 4.5 kHz. Use 741 op-amp.

Given :- $f_c = 4.5 \text{ kHz}$

for 741 op-amp : $I_B(\text{max}) = 500\text{nA}$

Assume : $V_{BE} = 0.7 \text{ V}$

Sol :-

$$* R_1 = \frac{0.1 V_{BE}}{I_B(\text{max})} = \frac{0.1 \times 0.7 \text{ V}}{500\text{nA}} = 140 \text{ k}\Omega$$

Use std value

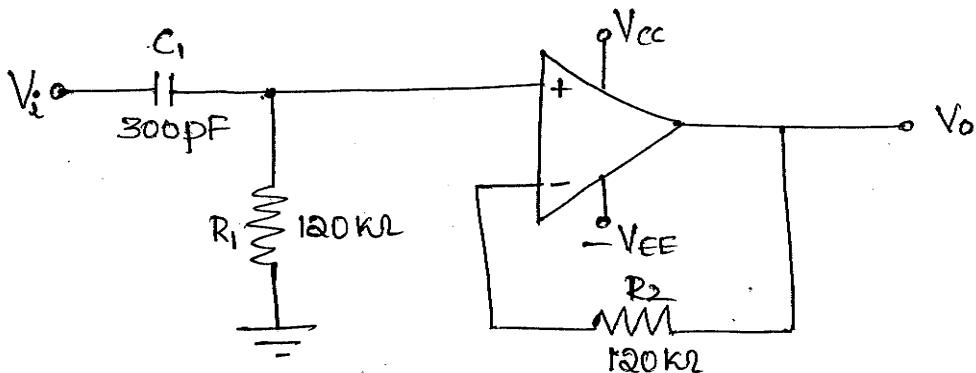
$$R_1 = 120 \text{ k}\Omega$$

*

$$R_2 = R_f = 120 \text{ k}\Omega$$

$$* C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 4.5 \text{ kHz} \times 120 \text{ k}\Omega} = 295 \text{ pF}$$

Use std value : $C_1 = 300 \text{ pF}$



2) Design a first order high pass active filter ckt to have a cut-off frequency of 5 kHz. Use an LM 108 op-amp & estimate the highest frequency that can be passed.

Given: $f_c = 5 \text{ kHz}$.

Sol:

The LM 108 op-amp has very low input bias current, it should be treated as BIFET op-amp.

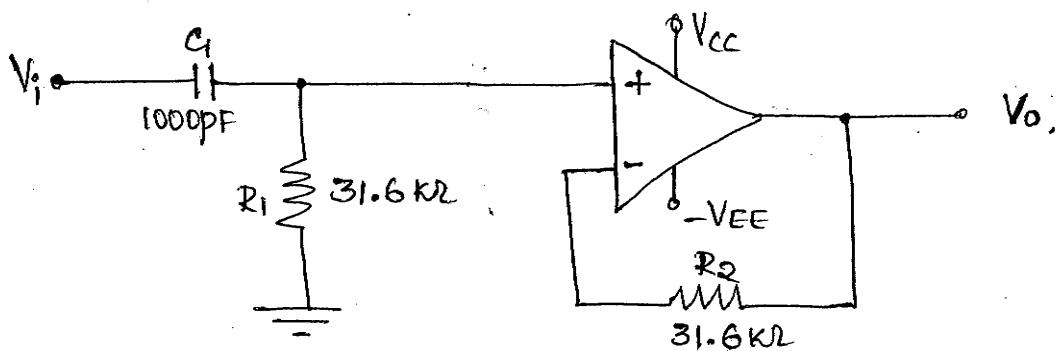
* Select C_1 very much larger than stray capacitance.

$$\therefore C_1 = 1000 \text{ pF}$$

$$* R_1 = \frac{1}{2\pi f_c C_1} = \frac{1}{2\pi \times 5 \text{ kHz} \times 1000 \text{ pF}} = 31.8 \text{ k}\Omega$$

$$* \text{ Use std value } R_1 = 31.6 \text{ k}\Omega \pm 1\%.$$

$$* R_2 = R_1 = 31.6 \text{ k}\Omega$$



Second order High pass active filter :-.

- * Sketch the ckt of a second order active high pass filter, explain its working.

June - 10, 8M

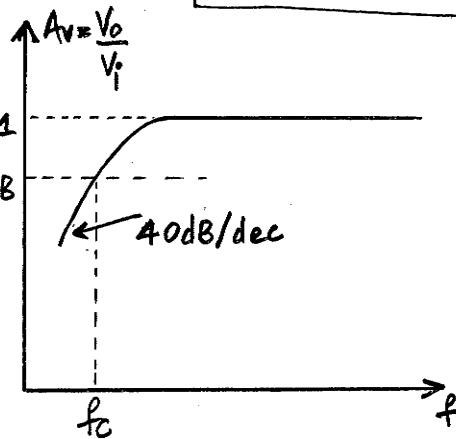
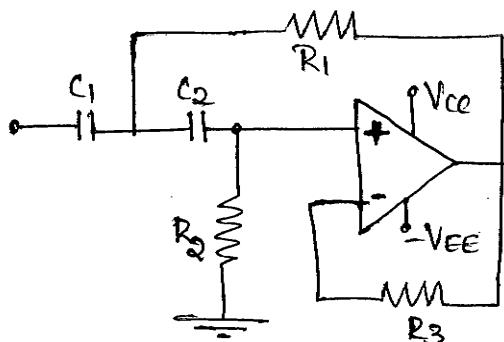


fig @: Second order high pass filter.

- * The second order high pass filter ckt is similar to the second order low-pass filter ckt, except that the resistor and capacitor positions are interchanged.

- * At higher frequencies, X_{C1} & X_{C2} are much smaller than R_1 & R_2 , consequently, C_1 , C_2 , R_1 & R_2 have no significant effect on the ckt.

The o/p voltage is then equal to the I/p, giving a Voltage gain of 1.

- * At low frequencies, the effect of C_2 & R_2 causes the o/p to fall off at a rate of 20dB per decade. A phase lead is produced by C_2 & R_2 & a phase lag is generated by R_1 combined with C_1 & C_2 . So, feedback via R_1 produces a further roll-off of 20dB per decade.

Thus the total roll-off rate is 40dB per decade.



Design steps 8 -

$$\text{1)} R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$\text{2)} R_2 = \sqrt{2} \times C_2 \text{ at } f_C$$

$$R_2 = \sqrt{2} \cdot \frac{1}{2\pi f_C C_2}$$

$$C_2 = \frac{\sqrt{2}}{2\pi f_C R_2} = \frac{1}{2\pi f_C \left(\frac{R_2}{\sqrt{2}} \right)}$$

$$\text{3)} C_1 = C_2$$

$$\text{4)} R_1 = \frac{R_2}{2}$$

$$\text{5)} R_3 = R_2$$

6) The impedance X_{C1} satisfies the equation.

$$X_{C1} = \sqrt{2} R_1 \text{ at } f_C$$

$$\text{i.e. } C_1 = \frac{1}{2\pi f_C \left(\frac{R_1}{\sqrt{2}} \right)}$$



2nd Order HPF :-FORMULAE :

$$1) R_2 = \frac{0.1 V_{BE}}{I_B(\text{max})}$$

$$2) C_2 = \frac{\sqrt{2}}{2\pi f_c R_2} = \frac{1}{2\pi f_c \left(\frac{R_2}{\sqrt{2}} \right)}$$

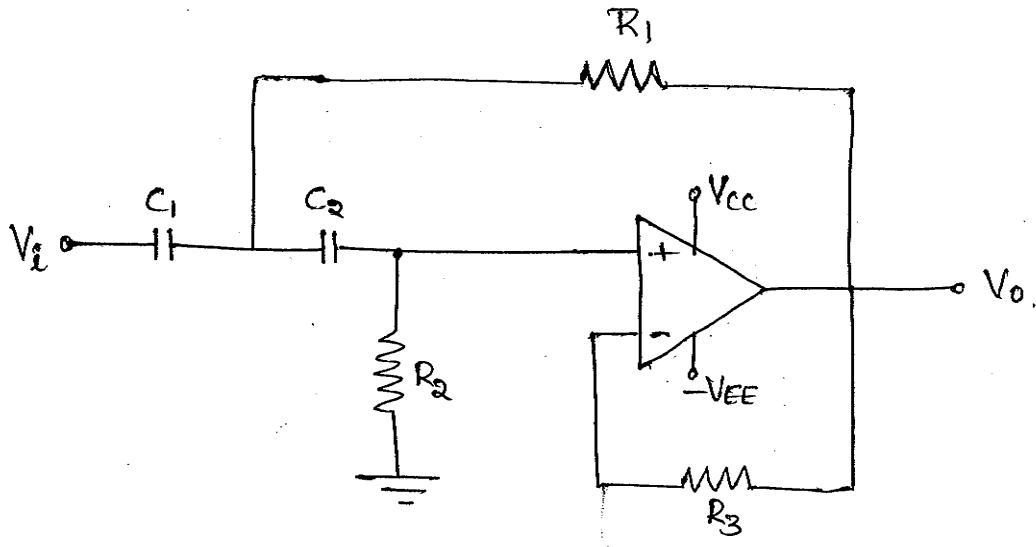
$$3) C_1 = C_2$$

$$4) R_1 = \frac{R_2}{2}$$

$$5) R_3 = R_2.$$

NOTE :- The impedance X_{C1} satisfies the equation.

$$X_{C1} = \sqrt{2} R_1$$



1) Design a second order high pass active filter to have a cutoff frequency of 12 kHz. Use a 715 op-amp and estimate the highest signal frequency that will be passed.

Given :- $f_c = 12 \text{ kHz}$

Sol : for 715 op-amp : $I_{B(\max)} = 1.5 \mu\text{A}$

$$* R_2 = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \text{ V} \times 0.7 \text{ V}}{1.5 \mu\text{A}} = 46.66 \text{ k}\Omega$$

Use std value $R_2 = 47 \text{ k}\Omega$

$$* R_1 = \frac{R_2}{2} = \frac{47 \text{ k}\Omega}{2} = 23.5 \text{ k}\Omega$$

Use std value $R_1 = 22 \text{ k}\Omega$

$$* R_3 = R_2 = 47 \text{ k}\Omega$$

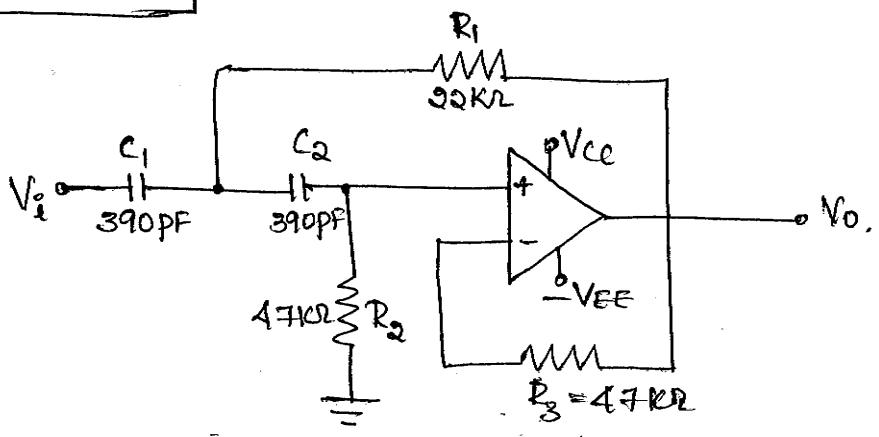
$$* C_2 = \frac{1}{2\pi f_c \left(\frac{R_2}{\sqrt{2}} \right)} = \frac{1}{2\pi \times 12 \text{ kHz} \times \left(\frac{47 \text{ k}\Omega}{\sqrt{2}} \right)} = 398 \text{ pF}$$

Use std value $C_2 = 390 \text{ pF}$

$$* C_1 = C_2 = 390 \text{ pF}$$

* From 715 data sheet, the op-amp unity gain cut-off frequency is $f_u = 11 \text{ MHz}$

$$f_2 = \frac{f_{ue}}{Av} = 11 \text{ MHz}$$



Q) Using op-amp, design a second order high pass filter to have a cut off frequency of 7KHz.

June-08, 6M

Given :- $f_c = 7\text{KHz}$

Sol:- for 741 op-amp : $I_{B(\max)} = 500\text{nA}$

Assume : $V_{BE} = 0.7\text{V}$

$$* R_2 = \frac{0.1 V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7\text{V}}{500 \text{nA}} = 140\text{k}\Omega$$

Use std value, $R_2 = 120\text{k}\Omega$

$$* R_1 = \frac{R_2}{2} = \frac{120\text{k}\Omega}{2} = 60\text{k}\Omega$$

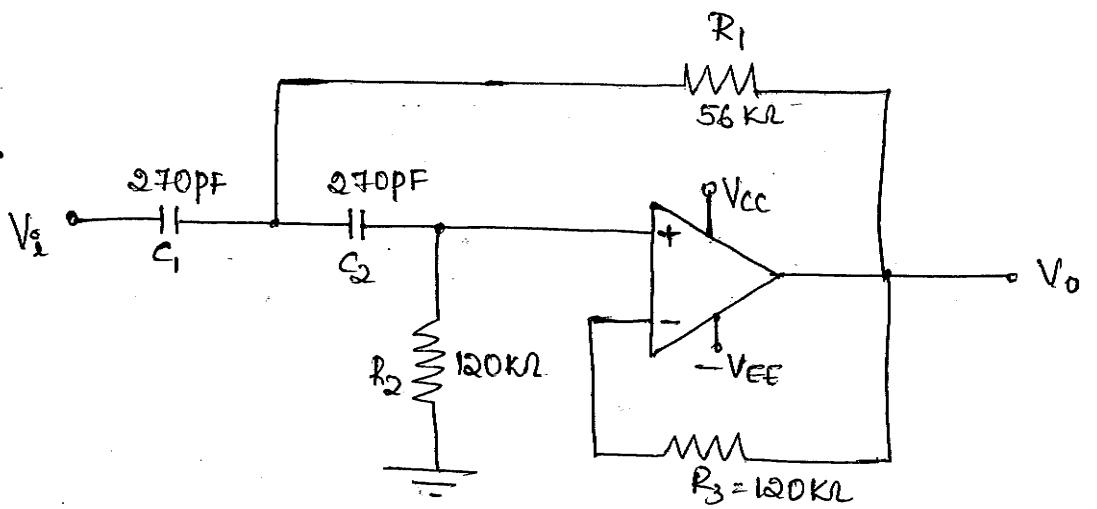
Use std value $R_1 = 56\text{k}\Omega$

$$* R_3 = R_2 = 120\text{k}\Omega$$

$$* C_2 = \frac{1}{2\pi f_c \left(\frac{R_2}{\sqrt{2}} \right)} = \frac{1}{2\pi \times 7\text{KHz} \times \left(\frac{120\text{k}\Omega}{\sqrt{2}} \right)}$$

$$* C_2 = 267.9\text{pF} \quad \text{Use std value } C_2 = 270\text{pF}$$

$$* C_1 = C_2 = 270\text{pF}$$



3) Using a 741 op-amp, design a second order high-pass filter to have a cut-off frequency of 15 kHz.

Given :- $f_c = 15 \text{ kHz}$

June - 09, 6M

Sol :- For 741 op-amp : $I_B(\max) = 500 \text{ mA}$

Assume : $V_{BE} = 0.7 \text{ V}$

$$* R_2 = \frac{0.1 V_{BE}}{I_B(\max)} = \frac{0.1 \times 0.7 \text{ V}}{500 \text{ mA}} = 140 \text{ k}\Omega$$

Use std value

$$R_2 = 120 \text{ k}\Omega \quad \leftarrow 1\text{M}$$

$$* R_1 = \frac{R_2}{2} = \frac{120 \text{ k}\Omega}{2} = 60 \text{ k}\Omega$$

Use std value

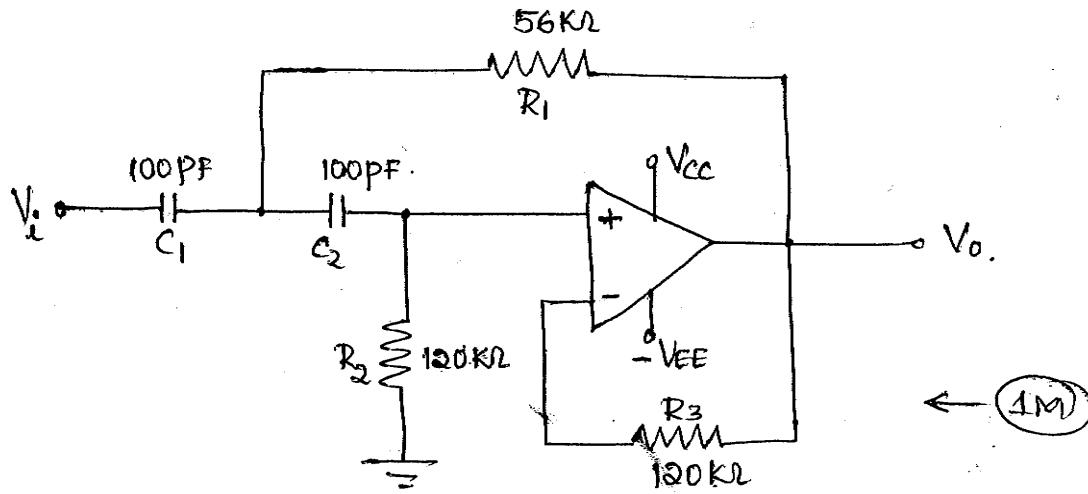
$$R_1 = 56 \text{ k}\Omega$$

$$* R_3 = R_2 = 120 \text{ k}\Omega \quad \leftarrow 1\text{M}$$

$$* C_2 = \frac{1}{2\pi f_c \frac{R_2}{\sqrt{2}}} = \frac{1}{2\pi \times 15 \text{ kHz} \times \left(\frac{120 \text{ k}\Omega}{\sqrt{2}} \right)}$$

$$C_2 = 125 \text{ pF} \quad \leftarrow 1\text{M} \quad \text{choose } C_2 = 100 \text{ pF}$$

$$* C_1 = C_2 = 100 \text{ pF} \quad \leftarrow 1\text{M}$$



Chapter-7

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Voltage Regulators

A voltage regulator is an electronic CKT that provides a constant dc o/p voltage independent of the [change in] the load current, temperature and ac line voltage variations.

Voltage regulators are classified as

- 1) Series regulator
- 2) Switching regulator

Series op-amp regulator :-

Show how op-amp can be used as series regulator

model paper 1 - 6M

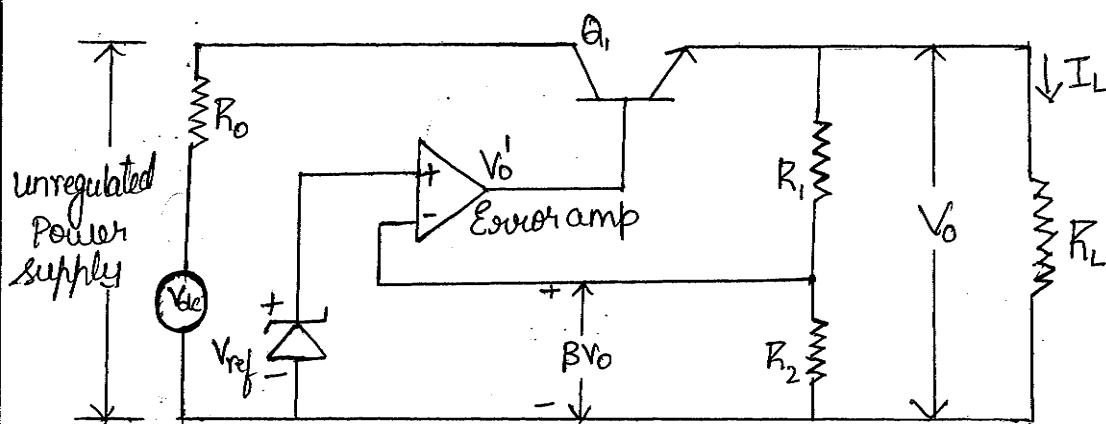


fig ① A regulated power supply



* A voltage regulator is an electronic ckt that provides a constant dc o/p voltage independent of the [change in] the load current, temperature & ac line voltage variations

fig ① shows a regulated power supply. The Ckt consists of four major components.

- 1) Reference voltage V_{ref} [Zener diode]
- 2) Error amplifier [Difference amplifier]
- 3) Series pass transistor [Q_1]
- 4) Feedback network [R_1 & R_2]

* The power transistor Q_1 is in series with the unregulated dc voltage ' V_{in} ' and the regulated o/p voltage ' V_o '. Any variation in o/p voltage is absorbed by this transistor.

* The transistor Q_2 connected as an emitter follower and therefore provide sufficient current gain to drive the load.

The o/p voltage is sampled by potential divider R_1 and R_2 [feedback N/w] and fed back to the INV input terminal of the op-amp error amplifier

* The sampled voltage is compared with the reference voltage V_{ref} . The o/p V_o of the error amplifier drives the series transistor Q_1 .



When the o/p voltage tends to increase, then the feedback voltage $\underline{V_f}$ also increases.

where

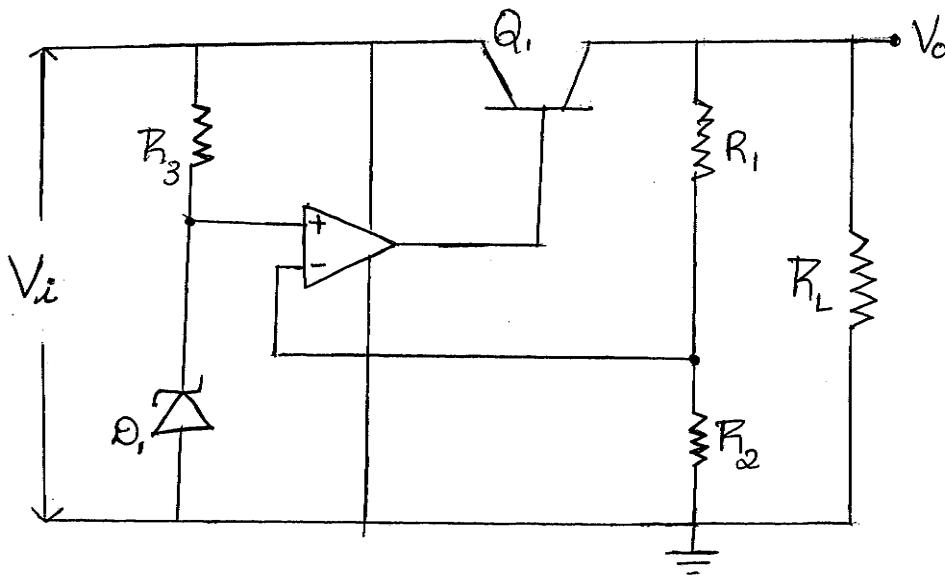
$$\boxed{\beta = \frac{R_2}{R_1 + R_2}}$$

* The voltage at INV input terminal of op-amp increases and as a result the o/p voltage V_o' of the op-amp decreases. Since Q acts as emitter follower, the o/p voltage V_o which follows V_o' , thus the V_o also reduces.

Thus o/p voltage V_o remains constant.





Problem :-Series Pass regulator :-Formulae :-

$$I_2 = 50 \mu A$$

$$1) V_{S(\min)} = V_o + 3V$$

$$2) R_3 = \frac{V_o - V_z}{I_z(\max)}$$

$$3) R_1 = \frac{V_o - V_z}{I_2}$$

$$4) R_2 = \frac{V_z}{I_2}$$

$$V_{CE} = 0.7V$$



Design a series pass regulator to give an o/p of 9 volts to a minimum and load resistance of $36\ \Omega$ for a two-in-one radio. The input dc coming from a rectifier filter varies between 9 volts to 15 volts. The op-amp available has a bias current of 12 nA and requires $V_{S\min} = \pm 7\text{ V}$ & $V_{S\max} = \pm 18\text{ V}$. The available zener diode is of 4.7 V with $I_z\max = 20\text{ mA}$. Specify the ratings required of series pass element and constant current short circuit protection transistor.

Jan - 09, 8M



Given :- $V_0 = 9V$, $V_Z = 4.7V$, $I_B = 12\text{nA}$,

$I_{Z(\text{max})} = 20\text{mA}$, $V_{S(\text{min})} = \pm 7V$, $V_{S(\text{max})} = \pm 18V$

Sol:

Choosing $I_2 = 50\text{mA}$

$$* R_3 = \frac{V_0 - V_Z}{I_{Z(\text{max})}} = \frac{9V - 4.7V}{20\text{mA}} = 430\Omega \quad [\text{ans}]$$

$$* \text{choose } R_3 = 1000\Omega$$

$$R_1 = \frac{V_0 - V_Z}{I_2} = \frac{9 - 4.7V}{50\text{mA}} = 86K\Omega$$

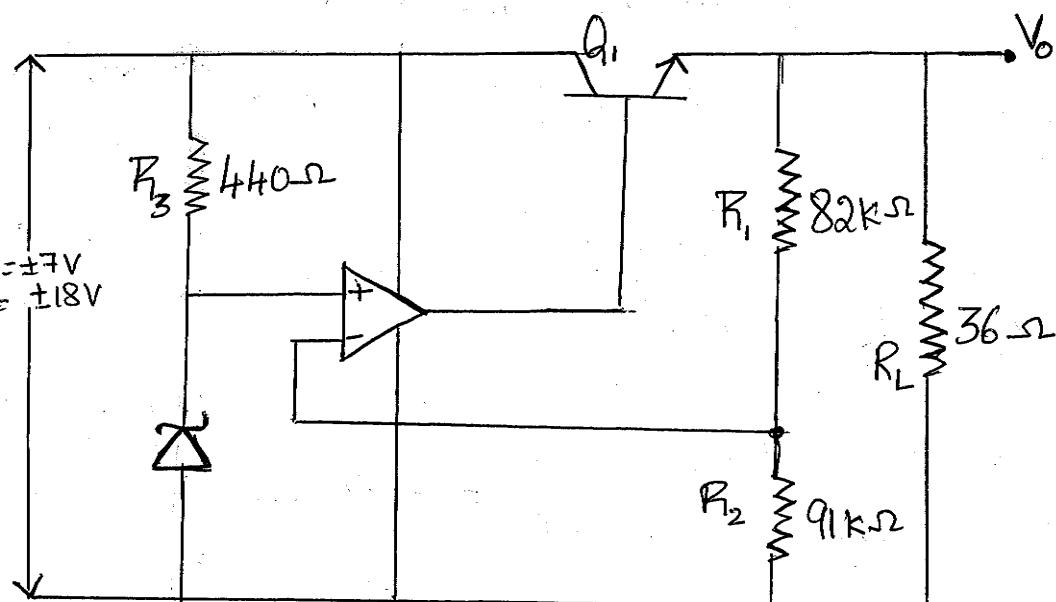
$$\text{choose } R_1 = 82K\Omega$$

$$* R_2 = \frac{V_Z}{I_2} = \frac{4.7}{50\text{mA}} = 94K\Omega$$

$$\text{choose } R_2 = 91K\Omega$$

$$* V_{CE} = 0.7V$$





IC Voltage Regulators :-

* IC voltage regulator replaces discrete component CKts op-amp regulator with IC, which gives low cost, high reliability, reduction in size & excellent performance.

- Eg: i) 78XX | 79XX Fixed voltage series regulators
 ii) 723 general purpose regulators.

Fixed Voltage Series Regulator:

Briefly explain the standard representation/configuration of 78XX regulators.

Jan-2011, 6M

* 78XX series are three terminal positive fixed voltage regulators. In 78XX, the last two numbers 'XX' indicate the op voltage.

7805 → +5V	}	← 2M
7806 → +6V		
7808 → +8V		
7812 → +12V		
7815 → +15V		
7818 → +18V		
7824 → +24V		



* 79XX series are three terminals negative fixed voltage regulators. In 78XX, the last two numbers 'XX' indicate the o/p voltage.

In 79XX series two extra voltage options of -2V and -5.2V available.

These regulators are available in two types of package:

- 1) metal package
- 2) Plastic package

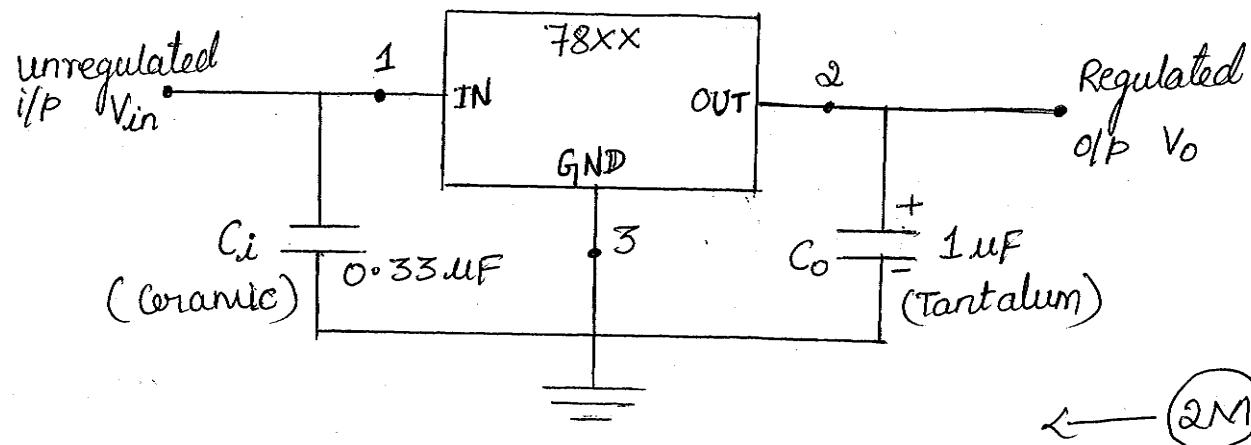
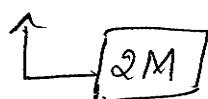


fig shows the standard representation of IC voltage regulator.

* A capacitor C_i is usually connected between input and ground terminal to cancel the inductive effect due to long leads.

* The o/p capacitor C_o improves the transient response.



Characteristics of IC regulators:

- * List and briefly explain the characteristics of three terminal IC regulators. What are the limitations of these regulators?

June-08, FM

There are four characteristics of three terminal IC regulators:

1) V_o : [Regulated o/p voltage]

The regulated o/p voltage is fixed at a value as specified by the manufacturer.

There are various models available with different o/p voltages.

Eg: 78XX series has o/p voltage at 5, 6, 8, 12, 15, 18V etc

2) $|V_{in}| \geq |V_o| + 2 \text{ volts}$:

The unregulated input voltage must be at least 2V more than the regulated o/p voltage.

for example, if $V_o = 5V$, then $V_{in} = 7V$

3) Maximum o/p current ($I_{o(max)}$):

The load current may vary from '0' to rated maximum o/p current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum o/p current.



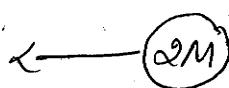
4) Thermal shutdown:

The IC has a built-in temperature sensor which turns off the IC when it becomes too hot. The O/p current will drop and remains there until the IC has cooled significantly.



Limitations:

1) No short ckt protection



2) O/p voltage is fixed

Advantages of IC voltage Regulators:

1) Easy to use

2) Simplifies power supply design

3) Low cost

4) Conveniently used for local regulations.

5) Over-current protection

6) Thermal overload protection.



Important Performance Parameter:

- * Explain the important parameters listed in the data sheet of 78XX.
- * Define and explain the following terms, used in a voltage regulator.
 - i) Line regulation ii) Load regulation

Jan - 09, 4M

- * Explain the terms line regulation, load regulation and ripple rejection for a dc voltage regulator

June - 09, 6M

The important performance parameters of a 3-terminal IC regulators are:

- 1) Line / Input Regulation
- 2) Load regulation
- 3) Ripple Rejection

1) Line regulation:

It is defined as the percentage change in the o/p voltage for a change in the input voltage. It is usually expressed in millivolt or as a percentage of the o/p voltage.

Typical value of line regulation from the data sheet of 7805 is 3mV.



2) Load Regulation :

It is defined as the change in output voltage for a change in load current and is also expressed in millivolts or as percentage of V_o .

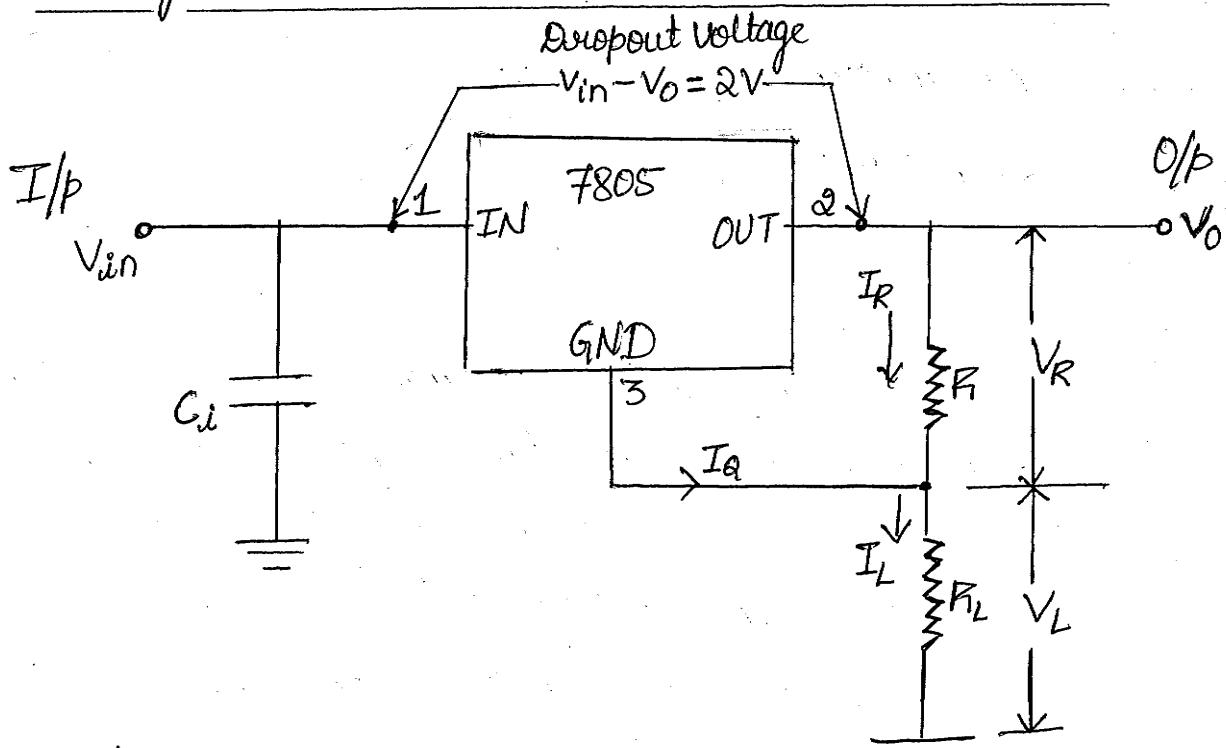
For 7805 regulator, the load regulation is 15mV for a load current variation for 5mA to 1.5 amps.

3) Ripple rejection :

The IC regulator not only keeps the O/p voltage constant but also reduces the amount of ripple voltage [in O/p]. It is usually expressed in dB.

For 7805, it is 78dB.

IC Regulator used as a current source :-



fig(i): IC 7805 as a current source



The three terminal fixed voltage regulator can be used as a current source as shown in fig①. From the CKT it is clear that,

$$I_L = I_R + I_Q \rightarrow ①$$

where I_Q is the quiescent current.

For 7805, $I_Q = 4.2 \text{ mA}$

* The I_R is given by

$$I_R = \frac{V_R}{R} \rightarrow ②$$

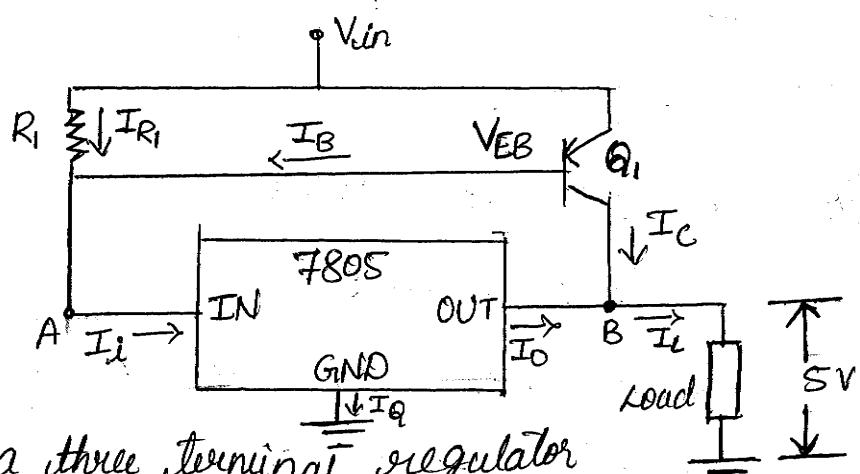
Sub eqn ② in eqn ①, we get

$$I_L = \frac{V_R}{R} + I_Q \rightarrow ③$$

In eqn ③, V_R, I_Q are constant, R can be selected to provide a sufficient current.

Thus 78XX can be used as current source.

Boosting IC regulator o/p current:



fig②: Boosting a three terminal regulator



It is possible to boost the output current of a three terminal regulator simply by connecting an external pass transistor in parallel with the regulator as shown in fig ①.

Operation:

- * For low load currents, the voltage drop across R_i is insufficient [i.e; $V_{BE} < 0.7V$] to turn ON transistor Q_1 & the regulator itself is able to supply the load current.
- * However when I_L increases, the voltage drop across R_i increases. When this voltage drop [*i.e* $V_{BE} = 0.7V$] the transistor Q_1 turns ON & transistor Q_2 supplies the extra current needed to drive low resistance load.
- * Applying KCL at node B, we get

$$I_C + I_O - \overbrace{I_L}^{\curvearrowright} = 0$$

$$\boxed{I_L = I_O + I_C} \rightarrow ①$$

$$(WKT \quad I_C = \beta I_B)$$

- * For regulator (for 7805)

$$\boxed{I_i = I_Q + I_O} \rightarrow ②$$

Since I_Q is very small, we can neglect it

$$\therefore \boxed{I_i = I_O} \rightarrow ③$$



* Applying KCL at node A, we get

$$I_{R_1} + I_B - I_i = 0$$

$$I_B = I_i - I_{R_1} \rightarrow \textcircled{4}$$

WKT $I_{R_1} = \frac{V_{EB(ON)}}{R_1}$

Sub eqn $\textcircled{3}$ & I_{R_1} value in eqn $\textcircled{4}$, we get

$$I_B = I_0 - \frac{V_{EB(ON)}}{R_1}$$

WKT

$$I_C = \beta I_B$$

Sub I_B value, we get

$$I_C = \beta \left[I_0 - \frac{V_{ON}}{R_1} \right]$$

$$I_C = \beta I_0 - \beta \frac{V_{EB(ON)}}{R_1} \rightarrow \textcircled{5}$$

Sub eq $\textcircled{5}$ in eqn $\textcircled{1}$, we get

$$I_L = I_0 + \beta I_0 - \beta \frac{V_{EB(ON)}}{R_1}$$

$$I_L = I_0 (1 + \beta) - \frac{\beta V_{EB(ON)}}{R_1}$$





Boosting IC regulator O/p current Problems:

FORMULAE :

i) When Q_1 is OFF [i.e; when $V_{BE} < 0.7V$]

$$1) I_L = I_{R_1}$$

$$2) I_L = \frac{V_o}{R_L}$$

$$3) V_{EB} = I_{R_1} \times R_1$$

$$\boxed{V_{EB} = I_L \times R_1}$$

$$4) I_O = I_L = I_i$$

ii) when Q_1 is ON [i.e; when $V_{EB} > 0.7V$]

$$1) I_L = I_{R_1}$$

$$2) I_L = \frac{V_o}{R_L}$$

$$3) V_{EB} = I_L R_1$$

$$4) I_L = I_0(1+\beta) - \beta \frac{V_{EB(ON)}}{R_1}$$

$$I_0(1+\beta) = I_L + \beta \frac{V_{EB(ON)}}{R_1}$$

$$\boxed{I_0 = \frac{I_L + \beta \frac{V_{EB(ON)}}{R_1}}{(1+\beta)}}$$

$$5) \text{W.K.T. } I_L = I_0 + I_C$$

$$\boxed{I_C = I_L - I_0}$$



Design of Current Source:

FORMULAE:

1) V_R = Voltage b/w pin 2 & 3

Eg: For 7805, $V_R = 5V$

For 7806, $V_R = 6V$

$$2) I_L = \frac{V_R}{R} + I_Q$$

$$\frac{V_R}{R} = I_L - I_Q$$

$$\therefore R = \frac{V_R}{I_L - I_Q}$$

NOTE: For 7805, $I_Q = 4.2 \text{ mA}$



Q) Using 7805, design a current source to deliver 0.2A current to a 22Ω , 10W load. Take quiescent current as 4.2mA.

Given:- $I_L = 0.2 \text{ A}$, $R_L = 22\Omega$

June - 10, 6M

For 7805 : $V_o = V_R = 5V$ &

$$I_Q = 4.2 \text{ mA}$$

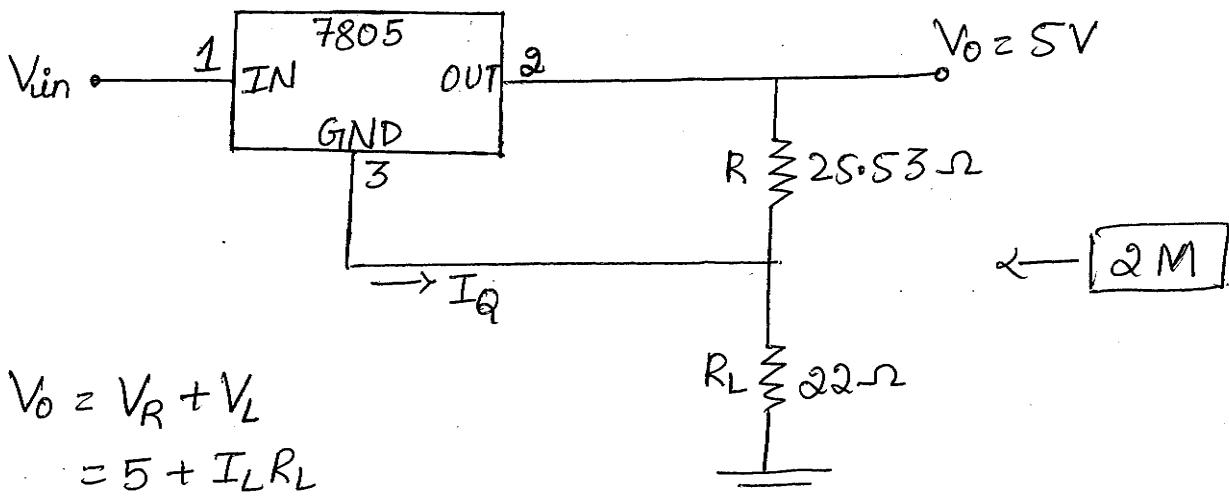
Sol:

$$I_L = \frac{V_R}{R} + I_Q$$

$$R = \frac{V_R}{I_L - I_Q} = \frac{5V}{0.2A - 4.2 \text{ mA}}$$

$$R = 25.53\Omega$$

← 2M



$$V_o = V_R + V_L$$

$$= 5 + I_L R_L$$

$$= 5 + 0.2 \times 22\Omega$$

$$V_o = 9.4V$$

← 2M



2. For the current booster circuit using 7805, calculate the O/p current coming from 7805 & I_C coming from transistor Q_1 for loads 100Ω , 5Ω , 1Ω . Assume $V_{BE(ON)} = 1V$, $\beta = 15$, $R_i = 7\Omega$

Given:- $V_{EB(ON)} = 1V$, $\beta = 15$, $R_i = 7\Omega$

For 7805 : $V_o = 5V$

- Load : i) $R_L = 100\Omega$
 ii) $R_L = 5\Omega$
 iii) $R_L = 1\Omega$

Sol :-

$$\text{i) } R_L = 100\Omega$$

$$* I_L = \frac{V_o}{R_L} = \frac{5V}{100\Omega}$$

$$I_L = 50mA$$

$$V_{EB} = I_L \times R_i = 50mA \times 7\Omega$$

$$V_{EB} = 0.35V$$

since $V_{EB} < 0.7V$. Hence Q_1 is OFF

so $I_O = I_L = I_i = 50mA$



ii) $R_L = 5\Omega$

$$* I_L = \frac{V_o}{R_L} = \frac{5V}{5\Omega}$$

$I_L = 1A$

$$* V_{EB} = I_L R_1 = 1 \times 7\Omega$$

$V_{EB} = 7V$

since $V_{EB} > 0.7V$

$\therefore Q_1$ is ON

Now

$$I_L = (1 + \beta) I_0 - \beta \frac{V_{EB(ON)}}{R_1}$$

$$\frac{I_0 + \beta \frac{V_{EB(ON)}}{R_1}}{(1 + \beta)} = 1 + 15 \times \frac{1V}{7}$$

$I_0 = 196mA$

$$* I_C = I_L - I_0 = 1A - 196mA$$

$I_C = 804mA$



III) $R_L = 1\Omega$

$$* I_L = \frac{V_0}{R_L} = \frac{5V}{1\Omega}$$

$I_L = 5A$

$$* V_{EB} = I_L R_i = 5A \times 7\Omega$$

$V_{EB} = 35V$

since $V_{EB} > 0.7V$

\therefore

Q_1 is ON

$$* I_o = \frac{I_L + \beta \frac{V_{EB(ON)}}{R_i}}{1+\beta} = \frac{5A + 15 \times \frac{1V}{7V}}{(1+15)}$$

$I_o = 446mA$

$$* I_c = I_L - I_o = 5A - 446mA$$

$I_c = 4.55A$



Fixed Regulator used as adjustable Regulator:

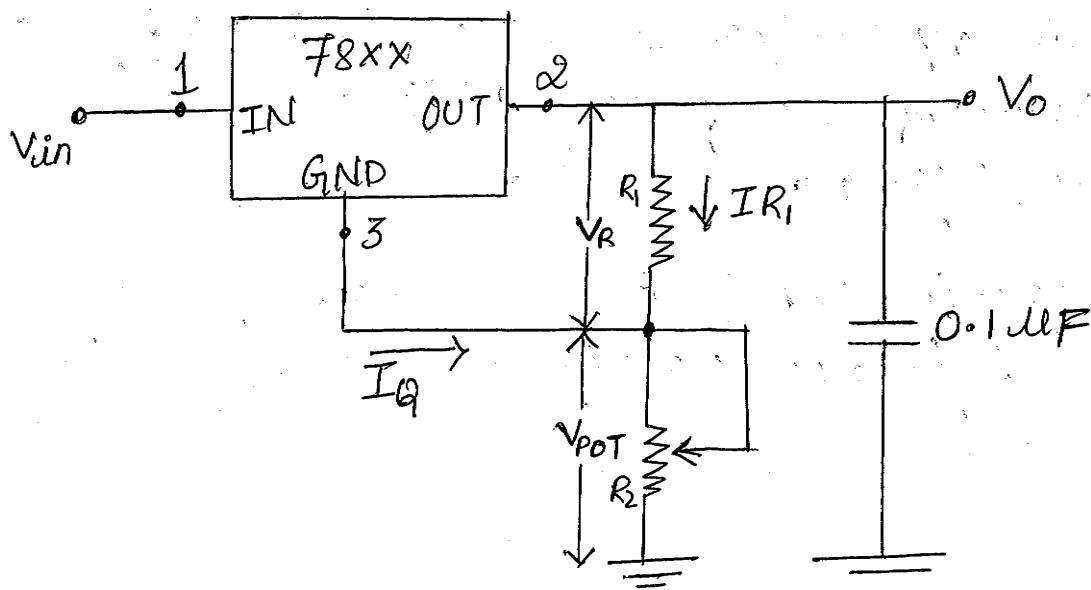


fig ① : Adjustable Regulator

* Fixed Regulator can be made use as a variable regulated voltage regulator. The ckt is shown in fig ①

The o/p vltg of the ckt is

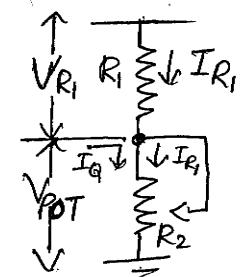
$$V_o = V_R + V_{POT}$$

$$V_o = V_R + (I_Q + I_{R1}) R_2$$

$$V_o = V_R + I_Q R_2 + \underline{I_{R1} R_2}$$

$$V_o = \underline{V_R} + I_Q R_2 + \frac{V_R}{R_1} R_2$$

$$V_o = V_R \left(1 + \frac{R_2}{R_1}\right) + I_Q R_2 \rightarrow ①$$



$$V_{POT} = [I_Q + I_{R1}] R_2$$

&

$$V_R = I_{R1} \times R_1$$

$$I_{R1} = \frac{V_R}{R_1}$$

where V_R is the regulated voltage difference b/w the OUT and GND terminals.



* The effect of I_Q is minimized by choosing R_2 as small as possible (i.e; neglecting $I_Q R_2$)

The minimum o/p voltage of the adjustable regulator is the value of the fixed voltage available from the regulator.

Hence neglecting $I_Q R_2$, it is possible to get an adjustable regulated voltage of any value.

NOTE :

- * The LM117, 217, 317 +ve regulators and LM137, 237, 337 -ve regulators are used for obtaining adjustable o/p voltages.
- * The o/p voltage can be adjusted from 1.2V to 40V & current upto 1.5A.



FORMULAE:

$$1) R_1 = \frac{V_R}{I_{R_1}}$$

$$2) R_2 = \frac{V_{POT}}{(I_Q + I_{R_1})}$$

$$3) V_o = V_R \left[1 + \frac{R_2}{R_1} \right]$$

$$4) \text{WKT in general } V_o = V_R + V_{POT}$$

$V_{POT} = V_o - V_R$

NOTE:- For 7805, $I_Q = 4.2 \text{ mA}$

Assume: $I_{R_1} = 25 \text{ mA}$



1) Specify suitable component values to get $V_o = 7.5V$ using a 7805 regulator.

Given: $V_o = 7.5V$

For 7805, o/p V_{tg} is 5V i.e; $V_R = 5V$ &

$$I_Q = 4.2 \text{ mA}$$

Assume: $I_{R_1} = 25 \text{ mA}$

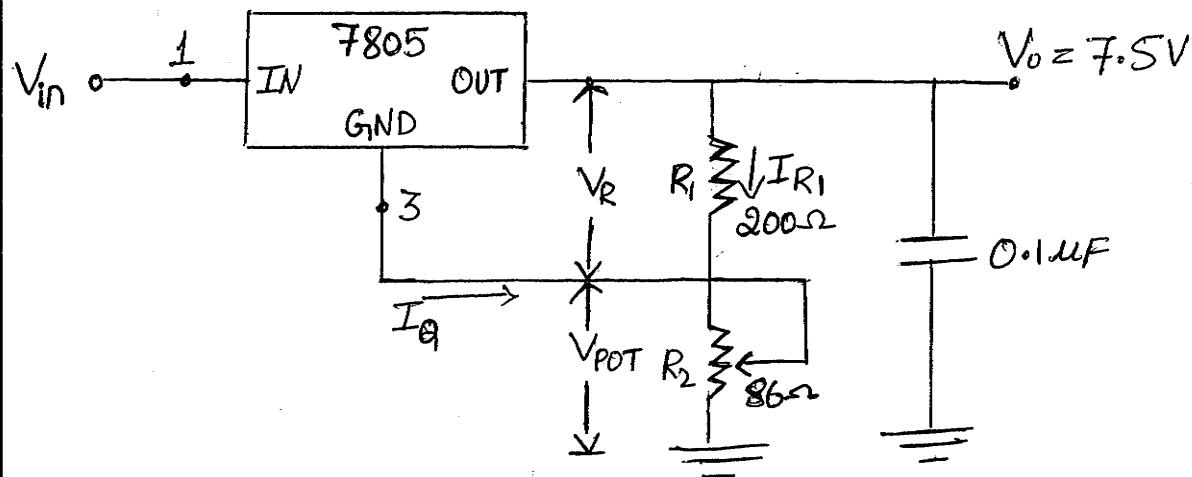
Sol: $V_{POT} = V_o - V_R = 7.5V - 5V$

$$V_{POT} = 2.5V$$

* $R_1 = \frac{V_R}{I_{R_1}} = \frac{5V}{25 \text{ mA}} = 200\Omega$

* $R_2 = \frac{V_{POT}}{(I_Q + I_{R_1})} = \frac{2.5V}{(4.2 \text{ mA} + 25 \text{ mA})} = 85.6\Omega$

choose $R_2 = 86\Omega$



2) Design a 7805 regulator to get the o/p $V_o = 6.5V$

Given: $V_o = 6.5V$

For 7805, o/p vfg is 5V i.e, $V_R = 5V$ &

$$I_Q = 4.2 \text{ mA}$$

Assume: $I_{R_1} = 25 \text{ mA}$

Sol: $V_{POT} = V_o - V_R = 6.5V - 5V$

$$V_{POT} = 1.5V$$

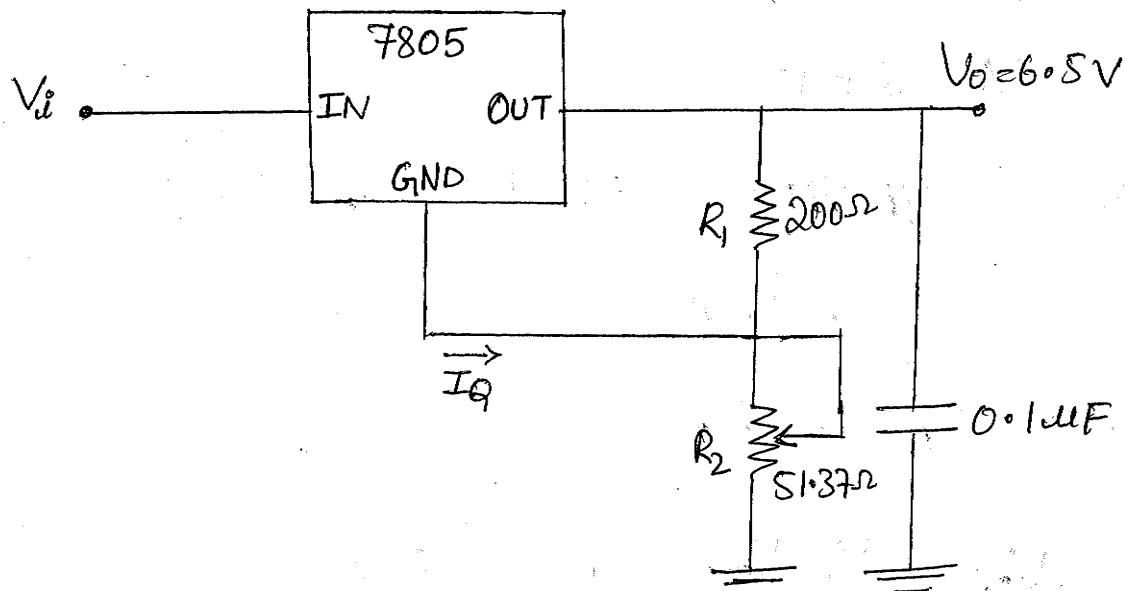
$$* R_1 = \frac{V_R}{I_{R_1}} = \frac{5V}{25 \text{ mA}}$$

$$R_1 = 200\Omega$$

$$* R_2 = \frac{V_{POT}}{I_Q + I_{R_1}} = \frac{1.5V}{(4.2 \text{ mA} + 25 \text{ mA})}$$

$$R_2 = 51.37\Omega$$





Dual Voltage Supply:

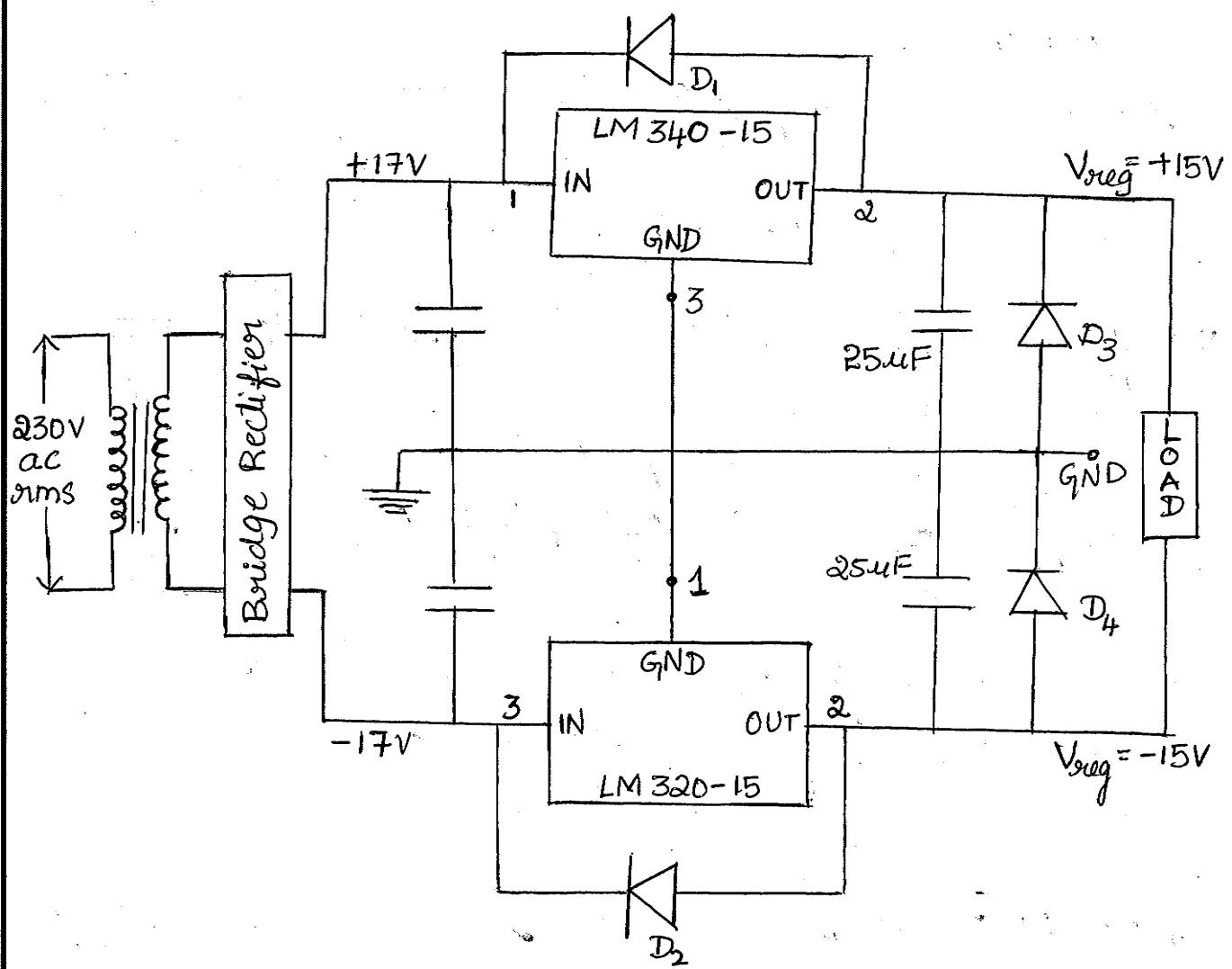


fig ①: Dual voltage $\pm 15V$ supply

* Three terminal fixed voltage regulators can be used to provide dual power supply required for op-amp.

The CKT shows a bipolar $\pm 15V$ supply provided by two fixed voltage regulators LM340-15 & LM-320-15.

The LM340-15 is a $+15V$ regulator & LM320-15 is a $-15V$ regulator



The pin configuration of LM340 & LM320 is different

* The diodes D_1 & D_2 in the CKT protect the regulator against short circuit occurring at its input terminals.

Diodes D_3 & D_4 provide protection against the situation when both the regulators may not turn ON simultaneously.

* If there is a load between two op's, the faster one will reverse the polarity of other & causes it to latch up unless it is properly clamped and this clamping is done by the diodes.

* Once the regulator starts operating properly, diodes are reverse biased & have no effect on circuit.

NOTE: LM325H is a dual tracking $\pm 15V$ supply & is available in a IC [10-pin]

Demerits of 3-terminal IC regulators:

The three terminal IC regulators have the following limitation [drawback or demerits]

- 1) No short circuit protection
- 2) Output voltage is fixed [either $+ve$ or $-ve$]



F23 General purpose regulator :

* Draw and explain the functional diagram of 723 IC

or

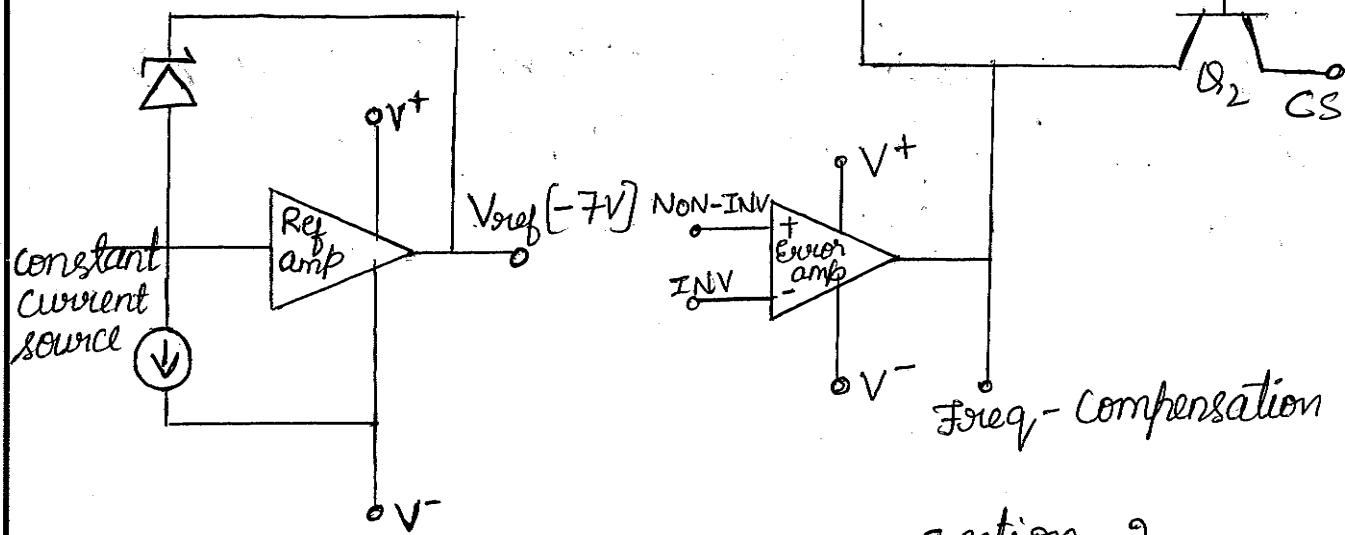
Model paper-1, 8M

* Draw the functional diagram of 723 regulator and explain it.

* IC 723 is a general purpose regulator, which can be adjusted over a wide range of both +ve & -ve regulated o/p voltage.

* IC 723 has a limitation that it has no inbuilt thermal protection. It also has no short circuit limits

* The functional diagram of IC 723 is as shown below:



Section - 1

section - 2

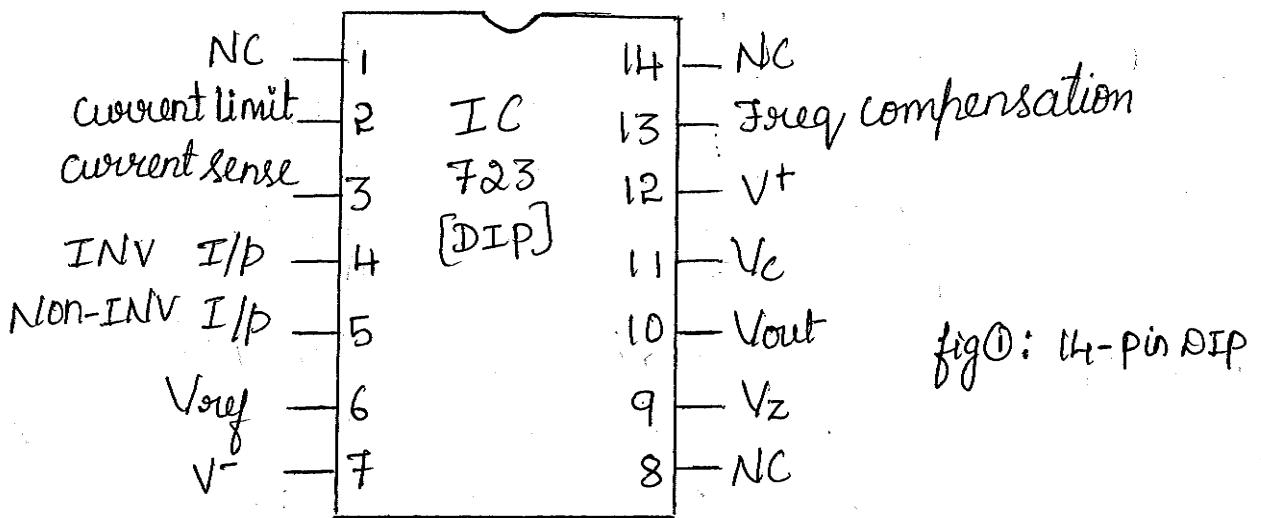
* IC 723 has two sections. The section 1 has zener diode, a constant current source & reference amplifier produces a fixed voltage of 7V at V_{ref} terminal.



- * The constant current source forces the zener to operate at fixed point so that the zener o/p's a fixed voltage.
- * The section - 2 consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2 .
The error amplifier compares a sample of the o/p voltage applied at the INV terminal with that of reference voltage (V_{ref}) applied at the Non-INV terminal.
- * The error signal controls the conduction of Q_1 . These two sections are internally not connected but are available as 723 IC regulator.

IC-723 Pin diagram:

- * 723 IC regulator is available in a 14-pin Dual-in-line package & 10 pin metal-can package as shown below:



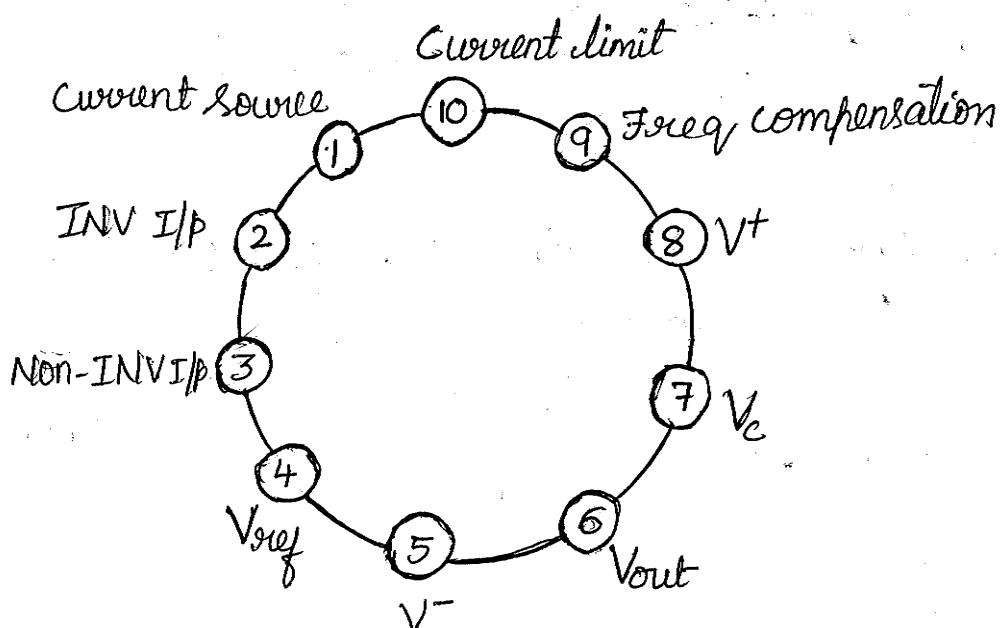


fig ②: 10 - pin metal - can package

Low voltage regulator using 723 IC :-

1. Explain the application of IC 723 as basic low voltage regulator.

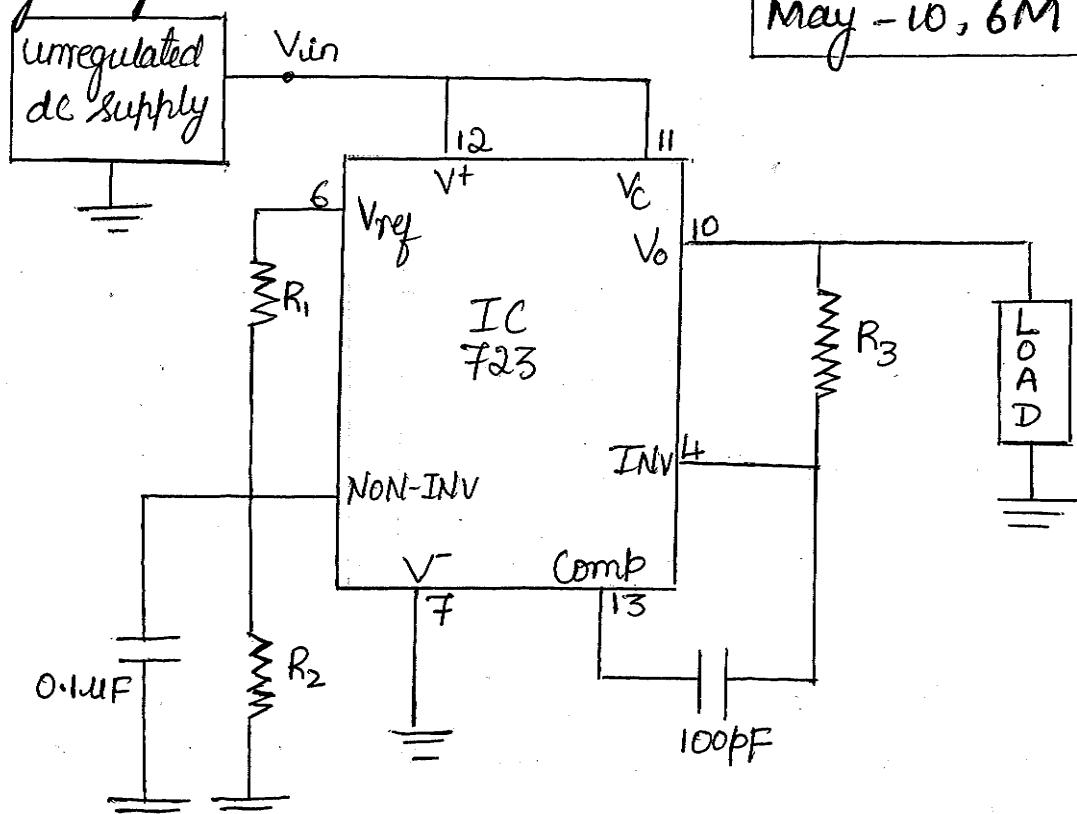


fig ③: A low voltage regulator using IC 723



A simple positive low voltage [2V to 7V] regulator can be made using 723 as shown in fig ①

- * The voltage at the Non-INV terminal of the error amplifier due to R_1 & R_2 is

$$V_{NI} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

$$\therefore V_{NI} = IXR_2$$

$$V_{NI} = \frac{V_{ref}}{R_1 + R_2} \cdot R_2$$

- * The difference b/w the voltage at NON-INV terminal and o/p voltage V_o (directly fed back) at INV terminal are the I/P's to the error amplifier.

- * The o/p of the error amplifier drives the pass transistor Q_1 . Since Q_1 is operating as emitter follower

$$V_o = V_{ref} \cdot \frac{R_2}{R_1 + R_2}$$

- * If o/p voltage becomes low i.e voltage at INV terminal goes down, this makes the o/p of the error amplifier to be more positive, thereby increasing the conduction of pass transistor Q_1 , & thus o/p voltage across load increases.

Thus initial drop in voltage is compensated. Similarly any increase in load voltage or change in i/p voltage gets regulated.



* The reference voltage is typically 7.15V, so o/p voltage is

$$V_o = 7.15 \cdot \frac{R_2}{R_1 + R_2}$$

So o/p voltage will be always less than 7.15V.
Thus fig ② is used as low voltage regulator.

FORMULAE

- 1) $V_o = V_{ref} \cdot \frac{R_2}{R_1 + R_2}$
- 2) From above equation determine R_2 by assuming R_1 or vice versa.
- 3) $R_3 = R_1 || R_2$

NOTE: $V_{ref} = 7V$





Q) Design a voltage regulator using IC 723 to get a voltage o/p of 3V.

Given: $V_o = 3V$

$$\text{WKT } V_{\text{ref}} = 7V$$

Sol'n: WKT

$$V_o = V_{\text{ref}} \frac{R_2}{R_1 + R_2}$$

$$3 = 7 \frac{R_2}{R_1 + R_2}$$

$$3R_1 + 3R_2 = 7R_2$$

$$4R_2 = 3R_1$$

$$R_2 = \frac{3}{4} R_1$$

Assume $R_1 = 10k\Omega$

$$R_2 = \frac{3}{4} \times 10k\Omega$$

$$R_2 = 7.5k\Omega$$

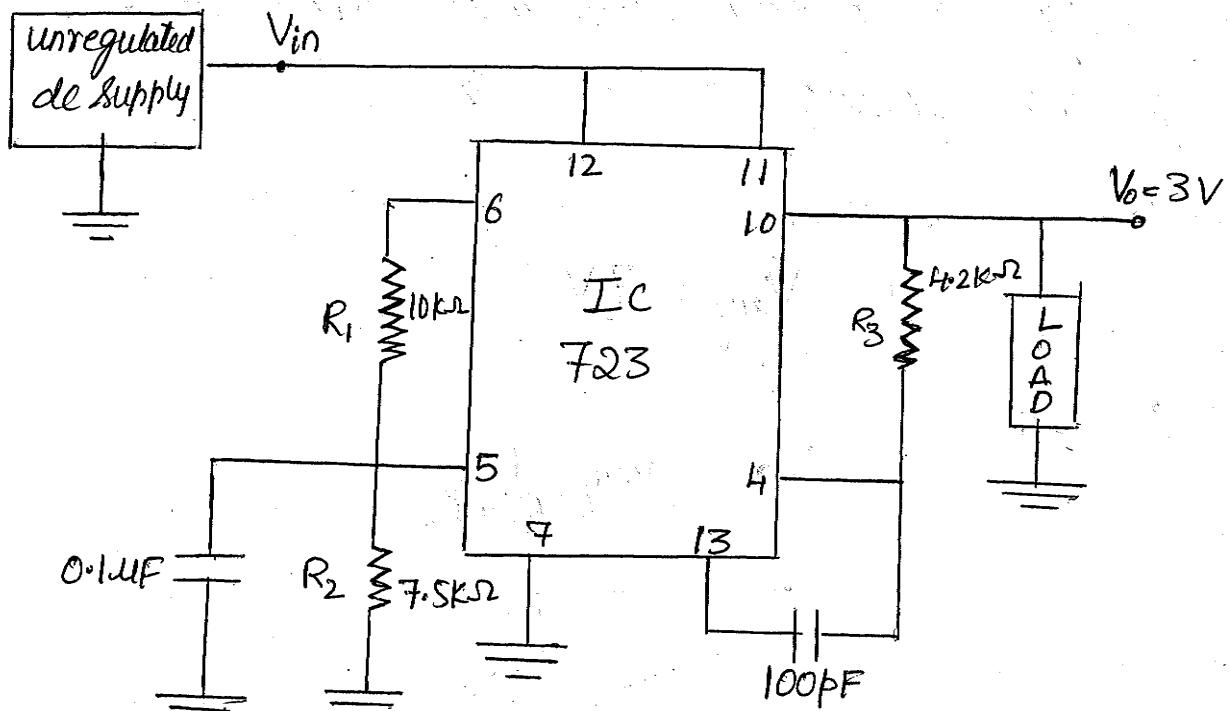
$$* R_3 = R_1 || R_2$$

$$= \frac{R_1 \times R_2}{R_1 + R_2}$$

$$= \frac{10k\Omega \times 7.5k\Omega}{10k\Omega + 7.5k\Omega}$$

$$R_3 = 4.2k\Omega$$





2) Design a voltage regulator using IC 723 to get a voltage o/p of 5V.

[Jan-10, 8M]

Given: $V_0 = 5V$

WKT $V_{ref} = 7V$

Sol:

$$V_0 = V_{ref} \cdot \frac{R_2}{R_1 + R_2}$$

$$5 = 7 \cdot \frac{R_2}{R_1 + R_2}$$

$$5R_1 + 5R_2 = 7R_2$$

$$5R_1 = 7R_2 - 5R_2$$

$$5R_1 = 2R_2$$

$$R_2 = \frac{5}{2} R_1$$



$$R_2 = 0.5 R_1$$

Assume $R_1 = 10\text{ k}\Omega$

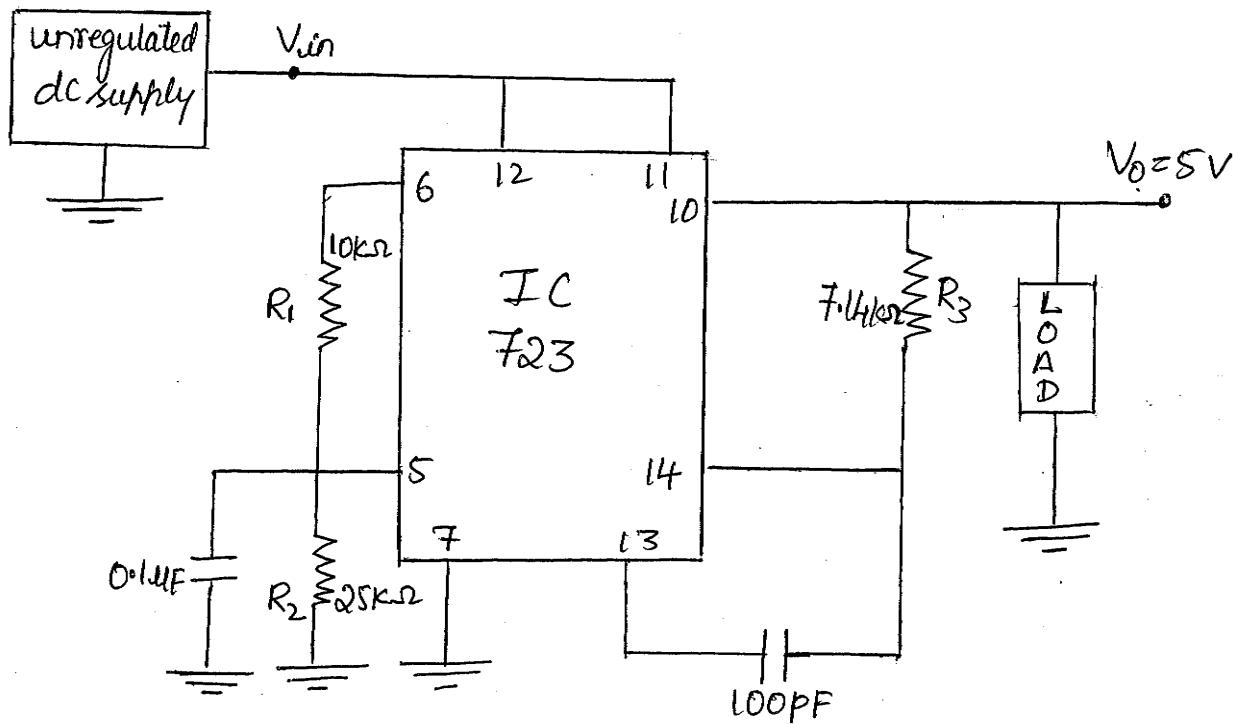
$$R_2 = 0.5 \times 10\text{ k}\Omega$$

$$R_2 = 25\text{ k}\Omega$$

* $R_3 = R_1 || R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$

$$R_3 = \frac{10\text{ k}\Omega \times 25\text{ k}\Omega}{10\text{ k}\Omega + 25\text{ k}\Omega}$$

$$R_3 = 7.14\text{ k}\Omega$$





ARUNKUMAR G M.Tech, *Lecturer in E&CE Dept. S.T.J.I.T, Ranebennur.* 42

IC 723 as High voltage Regulator : [V_o>7V]

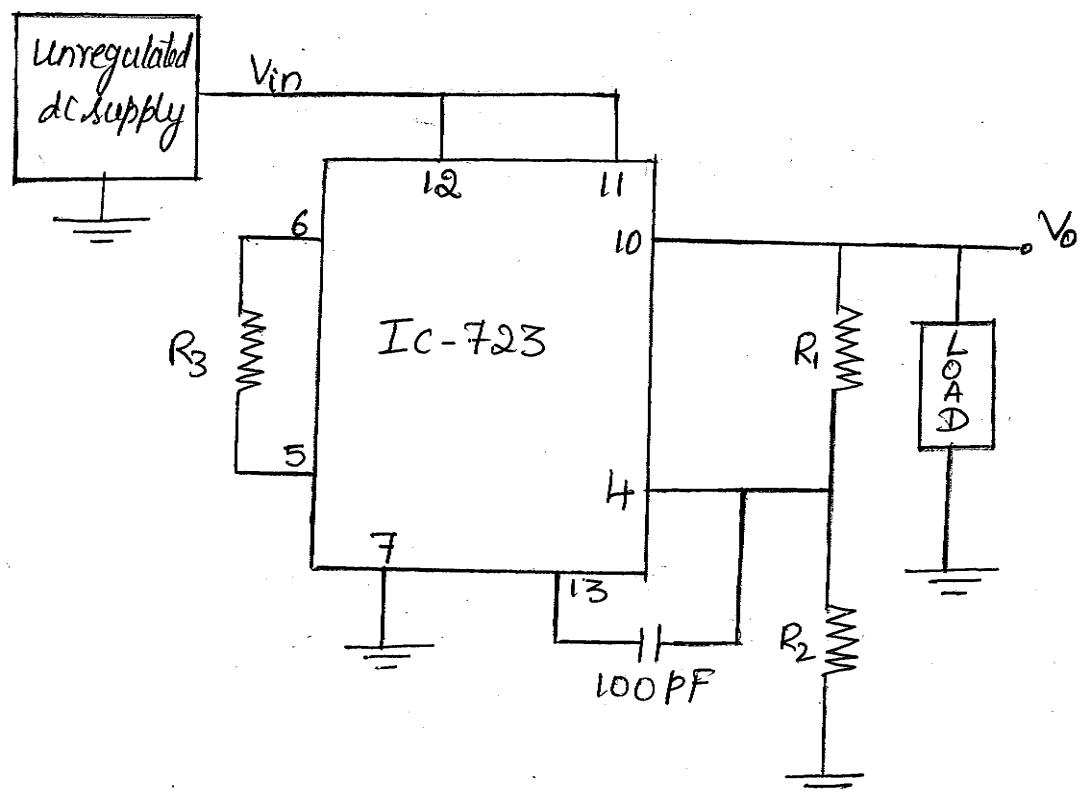


fig @ : Basic high voltage 723 regulator

Fig @ show the basic high voltage 723 voltage to get O/P voltage greater than 7V.

* The Non-INV terminal is directly connected to V_{out} through R_3 . Hence voltage at Non-INV terminal is

$$V_{NI} = V_{ref} = 7.15V$$

* The error amplifier acts as Non-INV amplifier with a voltage gain of

$$A_V = 1 + \frac{R_1}{R_2}$$



* The o/p voltage of the ckt is

$$V_o = 7.15 \left(1 + \frac{R_1}{R_2} \right)$$

thus regulated o/p voltage is greater than 7.15V

FORMULAE

- 1) $V_o = 7 \left(1 + \frac{R_1}{R_2} \right)$
- 2) From above equation determine R_2 by assuming R_1 or vice-versa.
- 3) $R_3 = R_1 R_2$

Note : $V_{ref} = 7V$



1) Design a high voltage 723 regulator so as to get an o/p voltage of 25V.

June-08, 7M

Given: $V_o = 25V$

Assume $V_{ref} = 7V$

Sol: WKT

$$V_o = V_{ref} \left(1 + \frac{R_1}{R_2} \right) \quad \leftarrow \boxed{1M}$$

$$25V = 7V \left(1 + \frac{R_1}{R_2} \right)$$

$$\frac{25V}{7V} = 1 + \frac{R_1}{R_2}$$

$$3.57 = 1 + \frac{R_1}{R_2}$$

$$\frac{R_1}{R_2} = 2.57$$

$$R_1 = 2.57 R_2 \quad \leftarrow \boxed{1M}$$

Assume $R_2 = 10K\Omega$

$$R_1 = 2.57 \times 10K\Omega$$

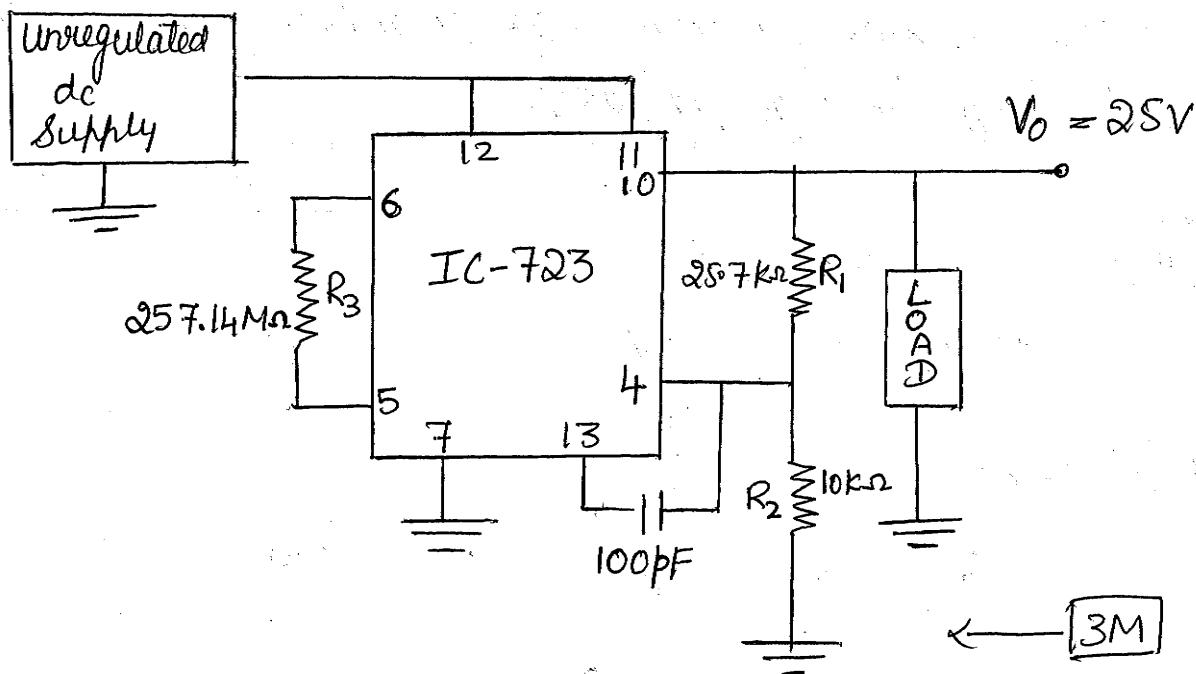
$$R_1 = 25.7 K\Omega \quad \leftarrow \boxed{1M}$$

* $R_3 = R_1 R_2$

$$= 25.7 K\Omega \times 10 K\Omega$$

$$R_3 = 257.14 M\Omega \quad \leftarrow \boxed{1M}$$





2) Design a high voltage regulator to get a o/p voltage of 28 volts.

Given: $V_o = 28V$

$$\text{WKT } V_{ref} = 7V$$

Sol: WKT $V_o = V_{ref} \left(1 + \frac{R_1}{R_2}\right)$

$$28V = 7V \left(1 + \frac{R_1}{R_2}\right)$$

$$\frac{28}{7} = 1 + \frac{R_1}{R_2}$$

$$H = 1 + \frac{R_1}{R_2}$$

$$\frac{R_1}{R_2} = H - 1$$

$$R = 3R_2$$

assume $R_2 = 1K\Omega$

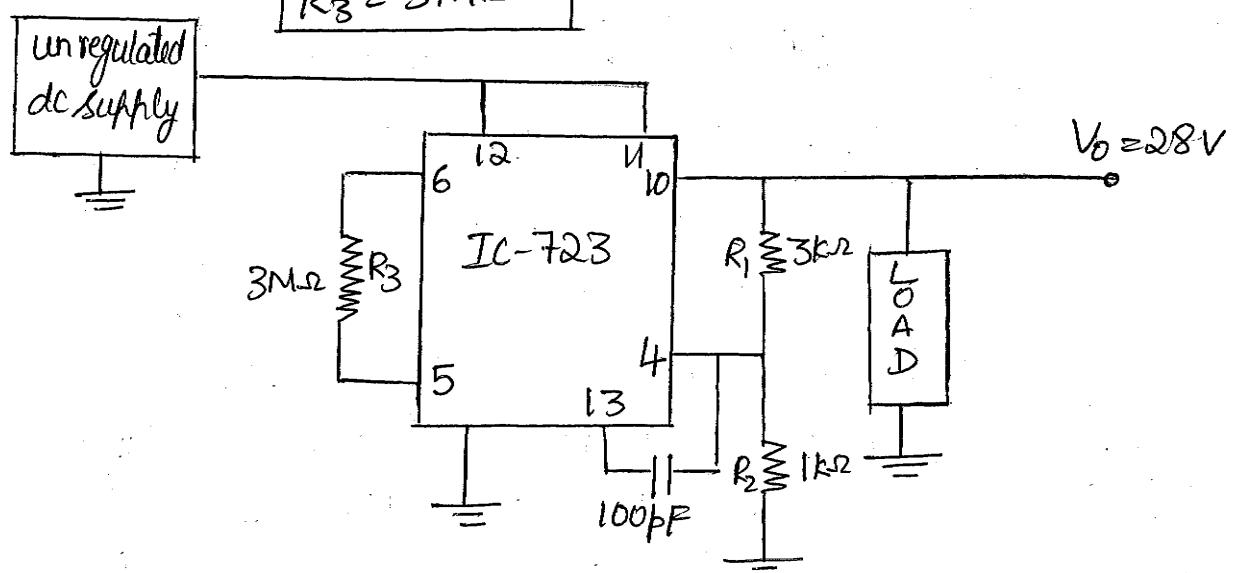


$$R_1 = 3 \times 1k\Omega$$

$$R_1 = 3k\Omega$$

$$* R_3 = R_1 R_2 = 1k\Omega \times 3k\Omega$$

$$R_3 = 3M\Omega$$



3) Design a 723 based voltage regulator to provide constant $V_o = 20V$ and $I_{o \max} = 250mA$

Given $V_{in-unreg} = 30V \pm 10\%$

[Jan 2011, 6 M]

Given:- $V_o = 20V$ $I_{o \max} = 250mA$

$$V_{in-unreg} = 30V \pm 10\%$$

Sol: WKT $V_o = 7.15 \left(1 + \frac{R_1}{R_2}\right)$ ← [IM]

$$\frac{20V}{7.15V} = 1 + \frac{R_1}{R_2}$$

$$2.797 - 1 = \frac{R_1}{R_2}$$

$$R_1 = 1.797 R_2$$

Assume $R_2 = 10k\Omega$ ← [IM]



$$R_1 = 1.797 \times 10k\Omega$$

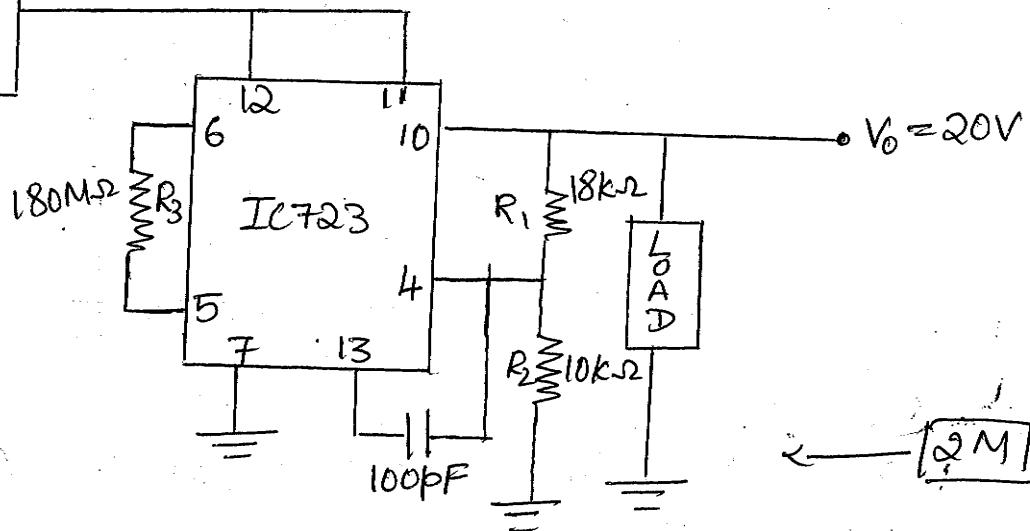
$$R_1 = 17.97 k\Omega$$

Choose $R_1 = 18 k\Omega \leftarrow [IM]$

* $R_3 = R_1 R_2 = 18 k\Omega \times 10 k\Omega$

$$R_3 = 180 M\Omega \leftarrow [IM]$$

Unregulated
dc
supply



NOTE:

$$\text{Given } I_{O\max} = 250 \text{ mA}$$

$$\& V_{BE} = 0.7V$$

$$V_{CE\max} = V_{in(\max)} - V_o = 33V - 20V$$

$$V_{CE\max} = 13V$$

* $R_{SC} = \frac{V_{BE}}{I_{O\max}} = \frac{0.7V}{250 \text{ mA}}$

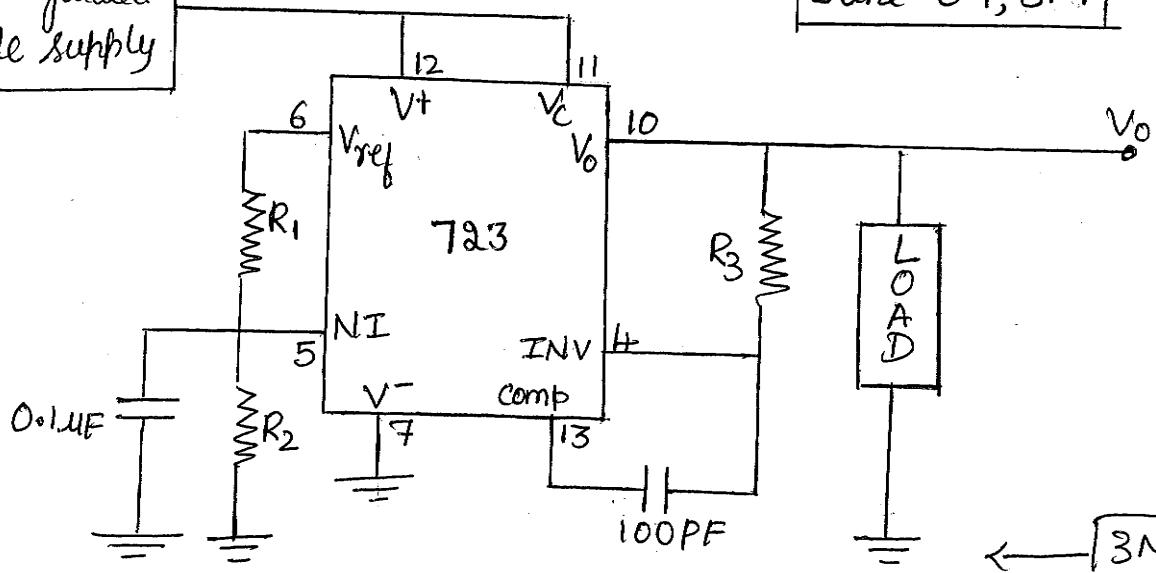
$$R_{SC} = 2.8\Omega$$



* With a neat schematic diagram, explain the salient features of a 723 regulator.

Unregulated
dc supply

June-09, 8M



3M

The salient features of a 723 regulators are ← [5M]

- 1) It works as voltage regulator at o/p voltage ranging from 2V to 37V at currents upto 150mA
- 2) Input and output short-circuit protection is provided.
- 3) It has good line and load regulation
- 4) Low temperature drift and high ripple rejection
- 5) Low standby current drain
- 6) Small size, lower cost.
- 7) It can be used at load currents greater than 150mA with external pass transistor.



Current Limit Protection:-

- * Explain the working of a series voltage regulator, with current limit protection.

Jan-2011, 8M

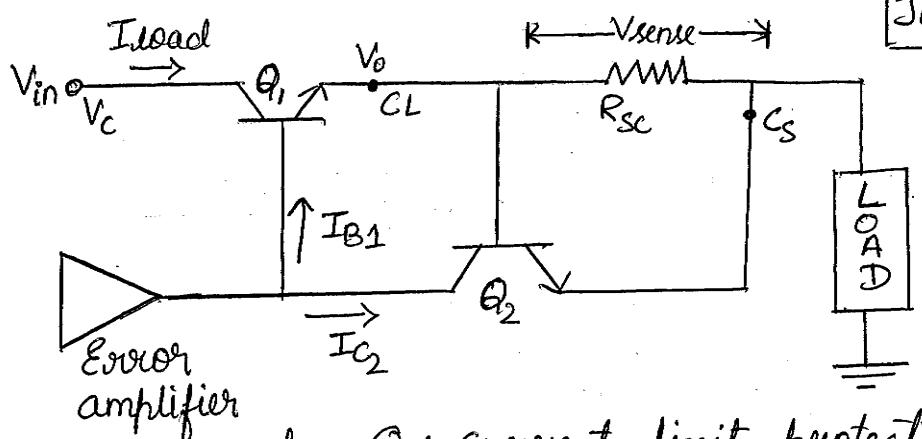


fig @ : current limit protection ckt

→ 3M

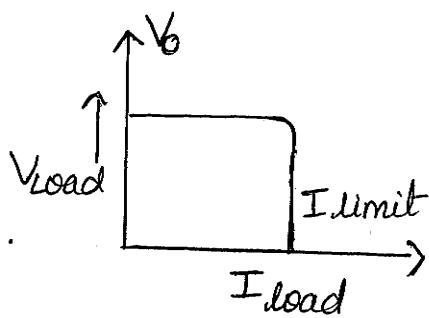


fig ⑥ : characteristic curve for a current limited regulator

- * The low and high voltage regulators using 723 IC have no short circuit protection. If the IC tries to drive very large current at constant o/p voltage then the IC gets hotter and may burn out.
- * The IC is therefore, provided with a current limit facility. The ability of the regulator to prevent the load current from increasing beyond certain limit is called "current limiting" & is denoted by I_limit.
- * The o/p voltage remains constant for load current below I_limit. As the current approaches to the limit,



the o/p voltage drops to zero, as shown in fig (b), thus protecting the regulator from high current.

- * The current limit I_{limit} is set by connecting an external resistor R_{sc} between the terminals CL and CS terminals as shown in fig (a). The CL terminal is also connected to the o/p terminal V_o and CS terminal to the load.
- * The load current produces a small voltage drop V_{sense} across R_{sc} , when $V_{\text{sense}} \approx 0.5V$, the transistor ' Q_2 ' begins to turn ON [since - $V_{\text{sense}} = V_{B2E}$]

Now current I_C starts flowing into the collector of Q_2 and the base current to Q_1 reduces. As a result, the emitter current of Q_1 also decreases i.e; load current is decreased.

So any increase in the load current will get nullified (& vice-versa)

* WKT $V_{\text{sense}} = V_{B2E} = 0.5V$

$$I_{\text{limit}} = \frac{V_{\text{sense}}}{R_{\text{sc}}}$$

$$R_{\text{sc}} = \frac{V_{\text{sense}}}{I_{\text{limit}}}$$

Explanation $\leftarrow [5M]$



i) Design a current limit circuit for a 723 regulator to limit the current of 60mA

Given: $I_{sc} = 60\text{mA}$

WKT

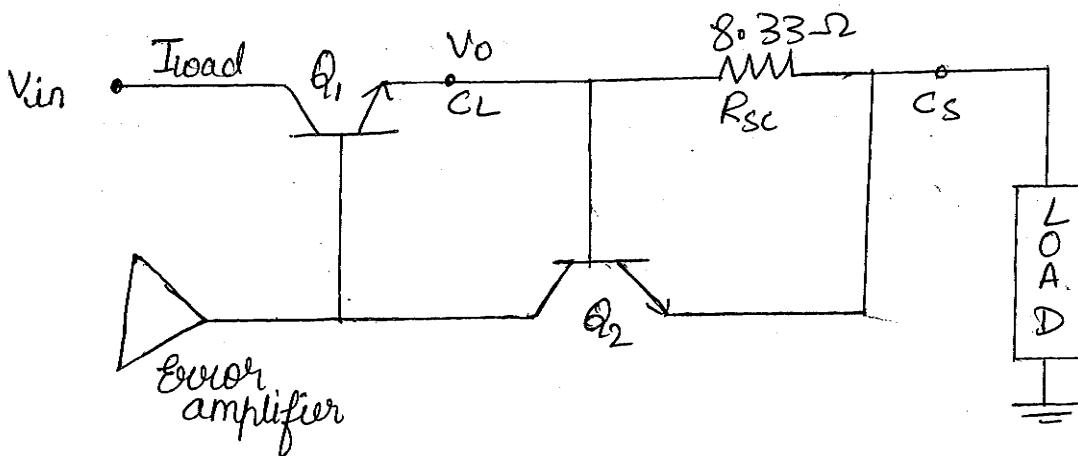
$$V_{sense} = 0.5\text{V}$$

Sol:

WKT

$$R_{sc} = \frac{V_{sense}}{I_{limit}} = \frac{0.5\text{V}}{60\text{mA}}$$

$$R_{sc} = 8.33\Omega$$



Current fold back:

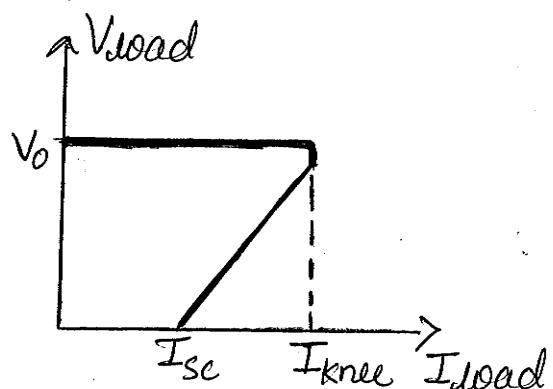
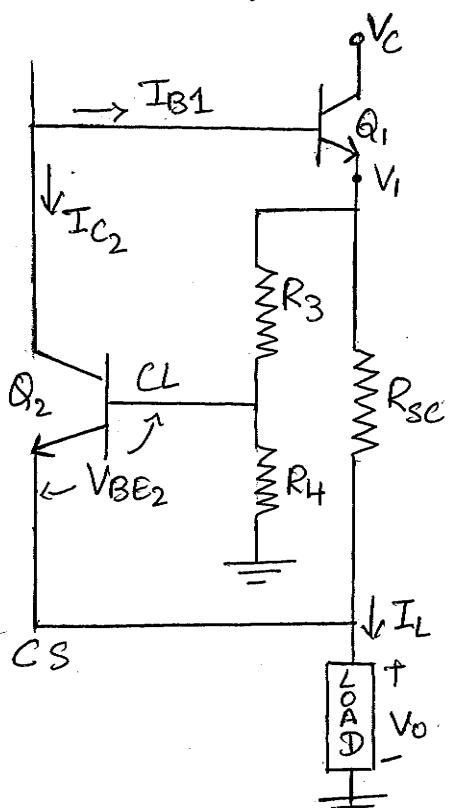


fig ⑥ : current fold back
characteristic curve

fig ⑤ current foldback

- * If the load is short circuited, the voltage V_0 becomes zero and a large current flows through the regulator. To protect the regulator, current foldback method is used.
- * Fig ⑥ shows the current foldback characteristic curve. When load goes on increasing, the o/p voltage V_0 is held constant till a value I_{knee} . Once the load current tries to increase beyond this, the current fold-back ckt decreases both o/p voltage and o/p current.
- * Fig ⑤ shows the current foldback ckt. The voltage at base of Q_2 is divided by $R_3 - R_4$ network. Q_2 conducts only when $V_{BE2} = 0.5V$ i.e; the voltage drops across R_{sc} .



- * As Q_2 conducts, I_{C2} flows more and thereby decreasing I_{B1} . Thus Q_1 turns off and I_L decreases. This decreases V_i , thus voltage at base of Q_2 also drops i.e; $\frac{VR_4}{R_4 + R_3}$
- * This process continues till $V_o = 0V$ & V_i is equal to $0.5V$.

Current Boosting in 723 IC :-

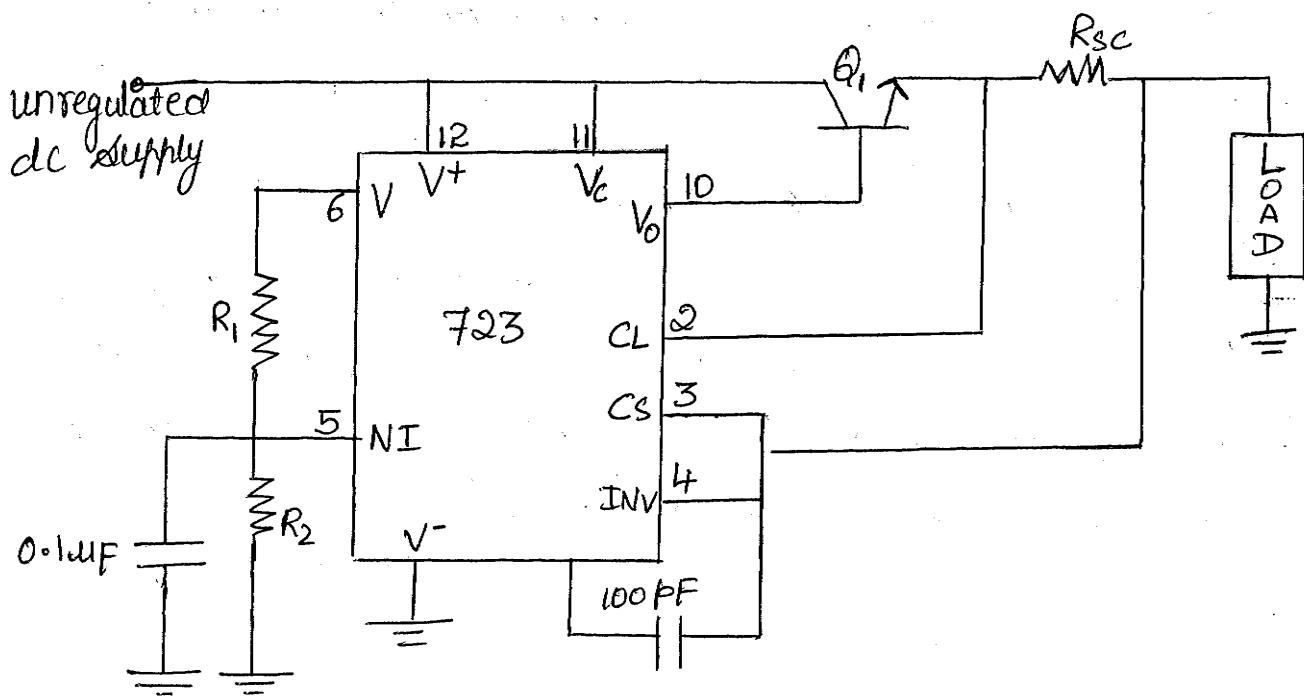


fig @ : current boosted low voltage regulator

- * The maximum current that 723 IC regulator can provide is 140mA. For many applications this current is not sufficient.



It is possible to boost the current level by adding a boost transistor Q_1 to the voltage regulator as shown in fig @.

- * The unregulated dc supply V_{IN} supplies the collector current to Q_1 . The o/p current from pin-10 is connected to the base of pass transistor Q_1 . This base current gets multiplied by β of pass transistor Q_1 .

$$\therefore I_L = \beta \times I_{O(723)}$$

NOTE:

- * β varies from 15 to 50
- * $I_{O(723)} = 140 \text{ mA}$



Limitation of Linear voltage Regulators :

- 1) The required input step down transformer is bulky and expensive.
- 2) Due to low line frequency (50 Hz), large values of filter capacitors are required.
- 3) The efficiency is very low.
- 4) I/p must be greater than the o/p voltage.
- 5) As large is the difference b/w i/p & o/p voltage, more is the power dissipation in the series pass transistor.
- 6) For higher i/p voltages, efficiency decreases.
- 7) The need for dual supply is not economical & flexible to achieve with the help of linear regulators.



Switching Regulator or Switch mode power Supplies

1) Explain the principle of operation of a switching regulator. Discuss its advantages & disadvantages.

Jan - 10, 8M

2) Explain the principle of switch mode power supplies. Enumerate their advantages and disadvantages.

June - 10, 8M

3) What is the principle of switch-mode power supplies? Discuss their advantages and disadvantages.

June - 08, 6M

June - 09, 6M

* In switching regulator, the pass transistor is used as a "controlled switch" and is operated at either cut off or saturated state. Hence power transmitted across the transistor is in discrete pulses (i.e; rrr)

* When transistor is in cut-off region, there is no current & dissipates no power.



- * When transistor is in saturation region, a negligible voltage drop appears across it & thus power dissipation is very less. Hence power transmitted increases and also the efficiency (70% to 90%)
- * Switching regulator uses concept of pulse width modulation to control the average value of o/p voltage. If the duty cycle varied as shown in fig①, the average value of the voltage changes w.r.t duty cycle.

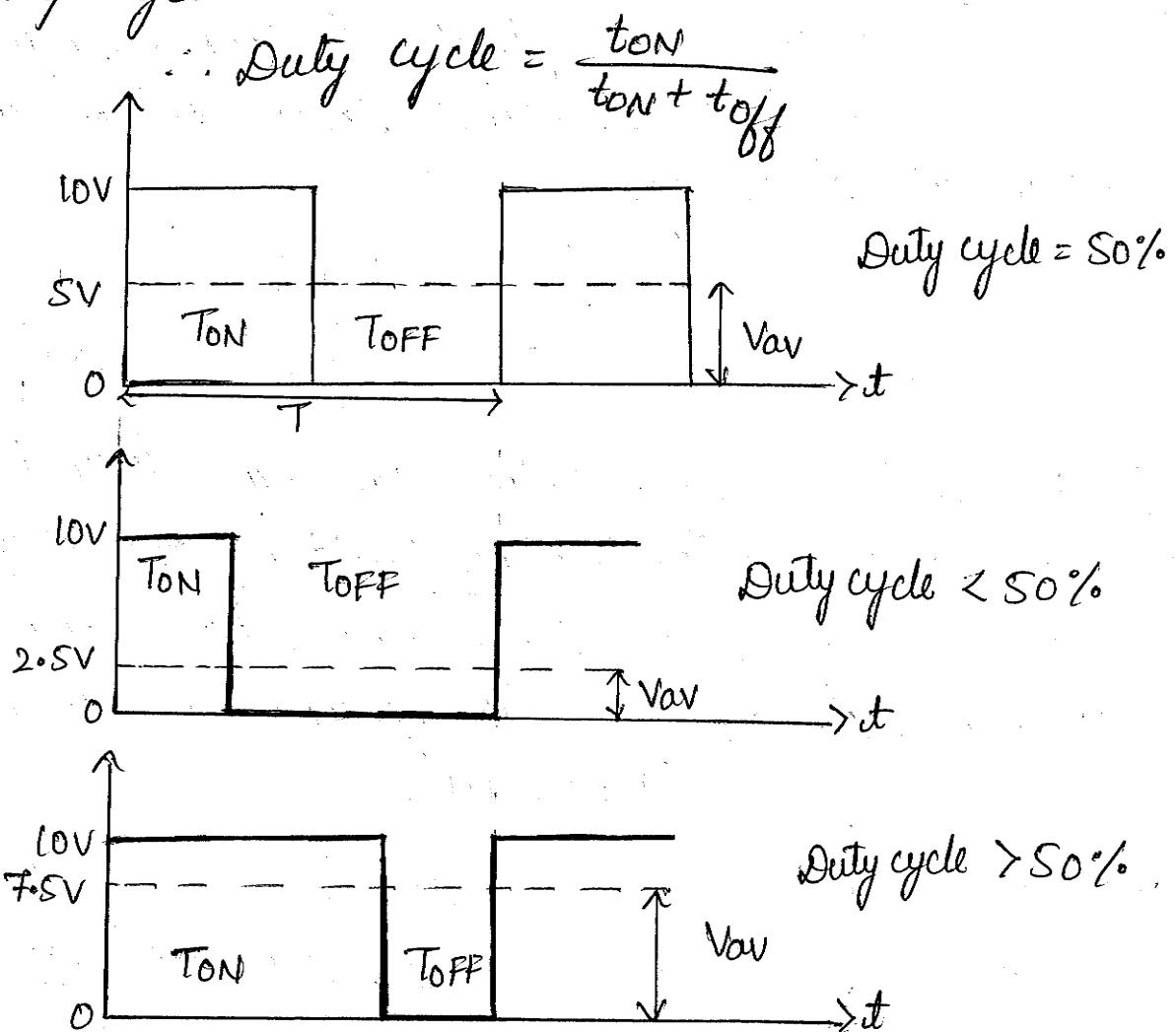


fig ①: Pulse width modulation and average value



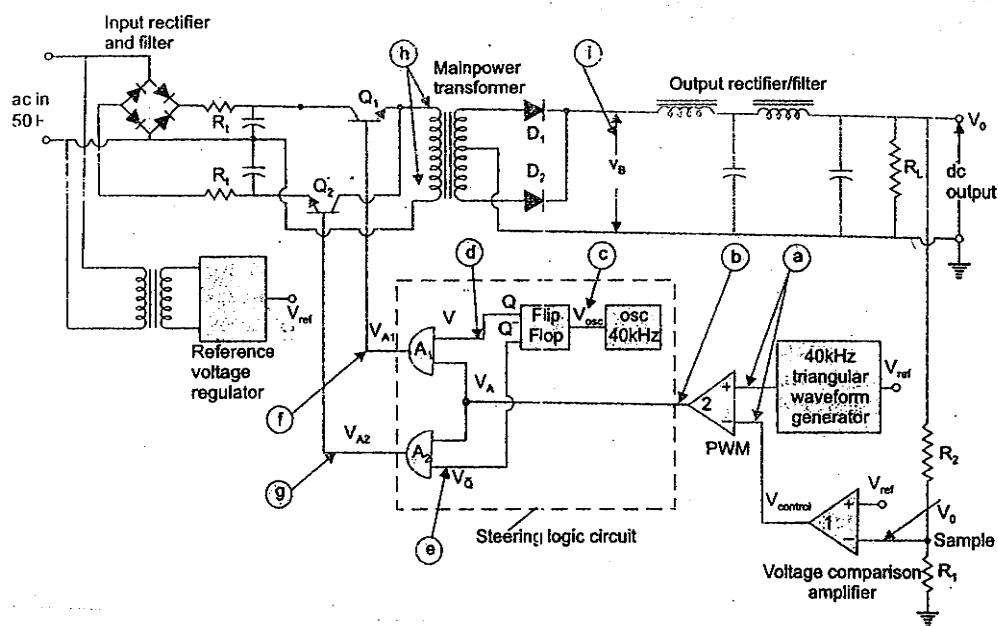


Fig ① shows a switching power supply

- * The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The thermistor R_t limits the high initial capacitor charge current.
- * Transistors Q & Q₂ are alternatively switched OFF & ON at 20KHz. These transistors are either fully on or cut-off, so they dissipate very little power.
- * The transistors Q₁ & Q₂ drives the primary of the main transformer. The secondary is



Centre tapped & full wave rectification is achieved by diodes D_1 & D_2 . This unidirectional square wave is next filtered through a two stage LC filter to produce o/p voltage V_o .

- * The regulation of V_o is achieved by the feedback ckt consisting of a pulse width modulation & steering logic ckt.

The fraction of the o/p i.e; $\frac{R_2}{R_1+R_2} V_o$ is feedback to the INV input of the comparator 1 & is compared with a fixed reference voltage V_{ref} in comparator 1.

- * The o/p of comparator 1 is called $V_{control}$ & is applied to the (-) input terminal of comparator 2 & a triangular waveform of frequency 40KHz is applied at the (+) input terminal.

(It may be noted that a high frequency triangular waveform is being used to reduce the ripple)

- * The comparator 2 functions as a pulse width modulator & its o/p is a square wave V_A of period 'T'

The duty cycle of the square wave is $\frac{T_{ON}}{T_{ON} + T_{OFF}}$
and varies with $V_{control}$ which in turn varies with



the variation of o/p V_o

- * The o/p V_A drives a steering logic ckt shown in dashed blocks.

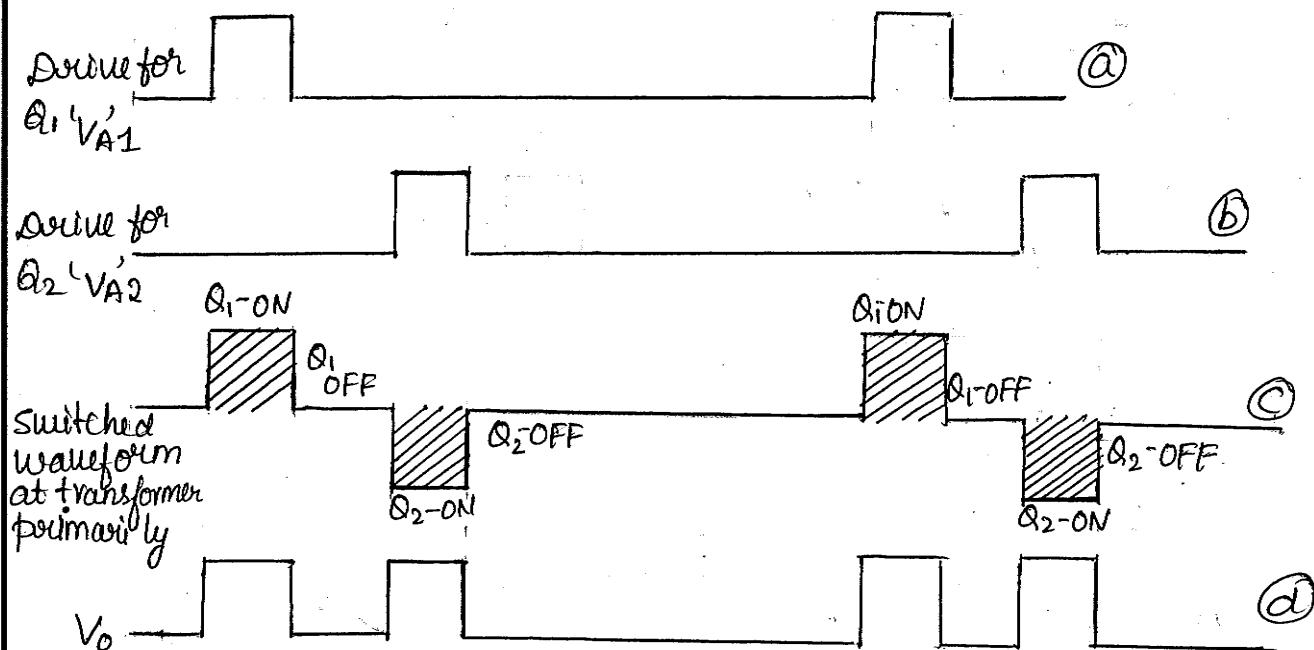


fig ③ : switching power supply waveform

- * The o/p V_{A1} & V_{A2} of AND gates A₁ & A₂ are shown in fig ③ - ④ & ⑥.

These waveforms are applied at the base of transistor Q₁ & Q₂. Depending upon whether Q₁ or Q₂ is ON, the waveform at the i/p of the transformer will be a square wave as shown in fig ④.

The rectified o/p V_B is shown in fig ⑤

- * By using switch [transistor] with low losses and a filter with high quality factor, the conversion efficiency can easily exceed 90%.



* If there is a rise in dc o/p voltage V_o , the voltage control $V_{control}$ of the comparator 1 also rises. Now time period T_1 decreases. This in turn decreases the pulse width of the waveform during the main power transformer.

Reduction in pulse width lowers the average value of the dc o/p voltage V_o . Thus the initial rise in the dc o/p voltage V_o has been nullified.

Advantages:

- 1) Efficiency is high [70% to 90%]
- 2) Decrease in size and cost.
- 3) The high operating frequency used for the switching transistor allows the use of smaller transformer.
- 4) The power dissipation of pass transistor is very small.
- 5) Small o/p filters.



Disadvantages:

- 1) Design is complex.
- 2) Ripple voltage is higher compared to linear regulator.
- 3) The response to load variations is not fast as compared to linear regulators.
- 4) Electromagnetic & radio frequency interference occurs.
- 5) A switch mode power supply requires external components like inductors & transformers.



Comparison of Linear regulators & Switching regulators :-

Sl No	Linear regulator	Switching regulator (SMPS)
1)	Efficiency is low	Efficiency is high
2)	cost is low	cost is high
3)	Design is simple	Design is complex
4)	Ripples are less at O/p.	Ripples are more at the o/p
5)	Power handling capacity is low	Power handling capacity is high
6)	NO switching losses	switching losses are high
7)	Response to load variation is fast	Response to load variation is slow.
8)	weight is high	It is light in weight.
9)	Due to low line frequency large filter capacitors are required.	high switching frequency allows small values of choke & capacitor
10)	Power transmitted across a transistor is in linear fashion	Power transmitted across a transistor is in the form of discrete pulse.
11)	series pass transistor does not act as a switch	series pass transistor acts as a switch.



Chapter-8

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Other Linear IC Applications555 Timer :

- * The IC 555 timer is one of the most versatile linear IC used for generating accurate time delay or oscillation.
- * IC 555 timer is available in two packages
 - i] 8-Pin Circular style &
 - ii] 8-Pin DIP type.

Features of IC 555 timer :

- ▷ It operates on +5V to +18V.
- ▷ It has adjustable duty cycle.
- ▷ High temperature stability.
- ▷ High current output. [200mA Sink @ Source]
- ▷ Low cost.
- ▷ Operated in two modes :
 - i) Monostable Multivibrator mode and
 - ii) Astable or free running mode.

Applications of 555 timer :

- ▷ Monostable and Astable multivibrator.
- ▷ Oscillator
- ▷ Ramp and square wave generator.
- ▷ Pulse generator.
- ▷ Burglar alarm.



- ⇒ Traffic Light Control and
- ⇒ Voltage Monitor etc.

Functional Diagram or Block Diagram of 555 timer:

- * Draw and Explain the functional diagram of 555 timer.

June-10, 6M

- * Explain the functional diagram of IC 555 with a neat sketch

Jan-10, 10M

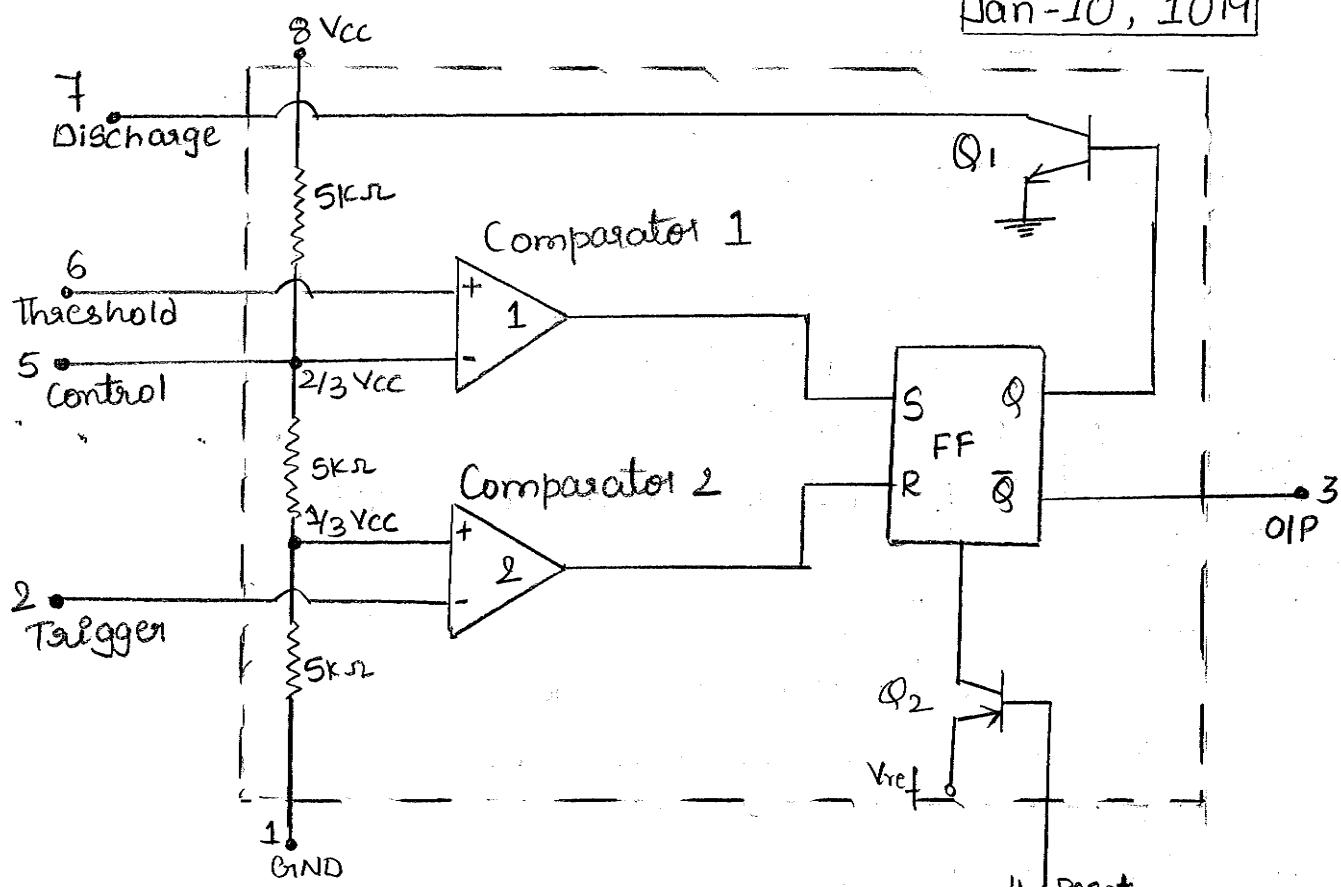


fig ① : Functional diagram of 555 timer.

fig ① Shows the functional diagram for 555 IC timer. It consists of two op-amp voltage comparators, resistive voltage divider network, SR Flip-Flop and a discharging transistor.



Pin 1 : Ground :-

All the voltages are measured with respect to this terminal.

Pin 2 : Trigger :-

Due to Voltage divider network, the voltage of Non-INN terminal of Comparator 2 is fixed at $V_{cc}/3$. The INV I/P of Comparator 2 which is compared with $V_{cc}/3$. When the trigger I/P is slightly less than $V_{cc}/3$ the Comparator 2 O/P goes high. This O/P is given to reset I/P of R-S flip-flop. Thus $Q=0$ & $\bar{Q}=1$. [\bar{Q} is connected to O/P].
 \therefore O/P of the timer is high.

Pin 3 : Output :-

* The \bar{Q} of the flip-flop goes to pin 3 which is the O/P. The load can be connected in two ways:
 i] Between Pin 3 and ground is called Normally-off load.
 ii] Between Pin 3 and Vcc is called Normally-ON load.

Pin 4 : RESET :-

The 555 timer can be reset by applying a negative pulse to this pin.

This pin is connected to Vcc to avoid false triggering when the timer is not in use.

Pin 5 : Control Voltage :-

An external voltage applied to this terminal changes the threshold as well as the triggering voltage ($2/3 V_{cc}$)



By applying a voltage on this pin, the pulse width [duty cycle] of the o/p waveform can be varied.

Pin 6 : Threshold :-

This is a Non-INN I/p of Comparator 1. The Voltage at this pin Compare with the $\frac{2}{3} V_{cc}$ at the INV terminal of Comparator 1.

When the Voltage at this pin is greater than threshold Voltage $\frac{2}{3} V_{cc}$, the o/p of the Comparator 1 goes high, The flip-flop then resets switching the o/p to the timer to become low.

Pin 7 : Discharge :-

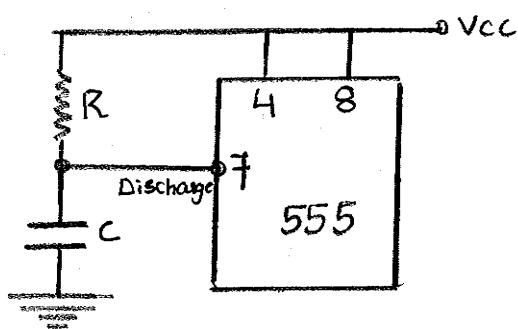
This pin is connected to the Collector of the discharge transistor Q_1 .

When the O/P is high [i.e. $\bar{Q}=1 \Rightarrow Q=0$], transistor Q_1 is OFF and acts as open ckt to the external Capacitor.illy, When the O/P is low [i.e $\bar{Q}=0 \Rightarrow Q=1$], Q_1 is ON & acts as a short ckt, Shorting out the external capacitor 'C' to ground.

Pin 8 : +Vcc :-

The IC 555 Timer Can work with an Supply Voltage between +15v to +18V.

Note :



Monostable Multivibrator Using IC-555 :

Jan-09, 5m

* 555 timer as monostable

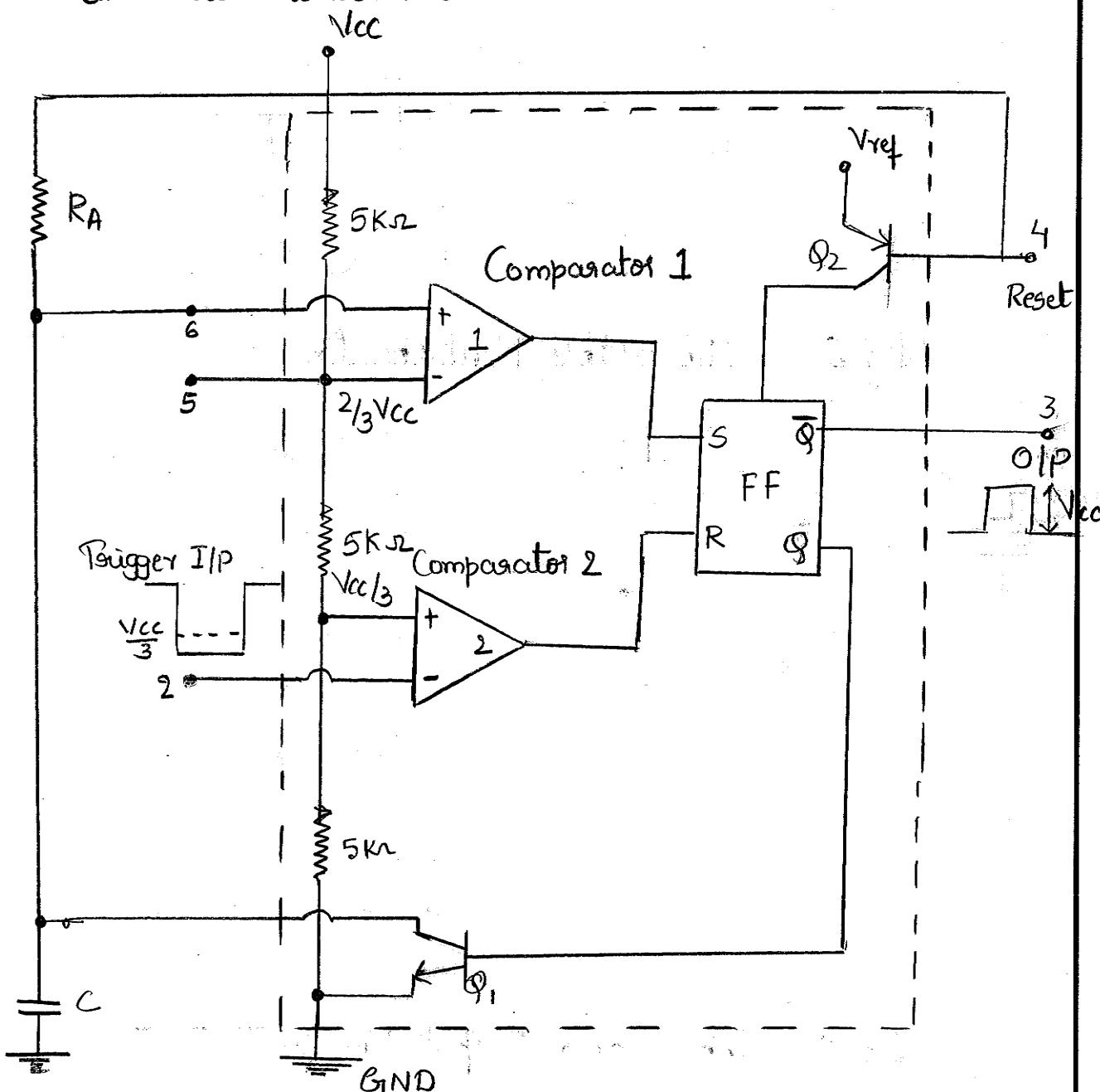
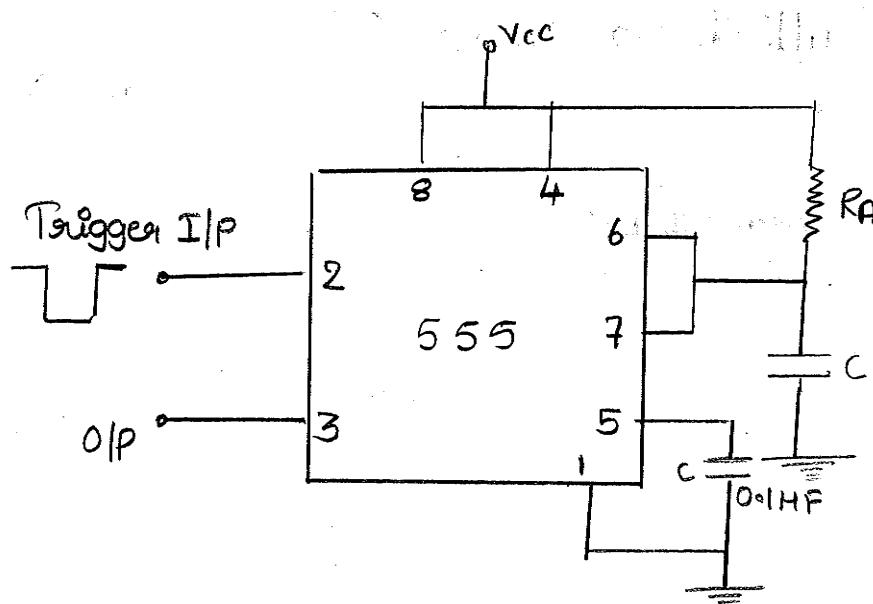
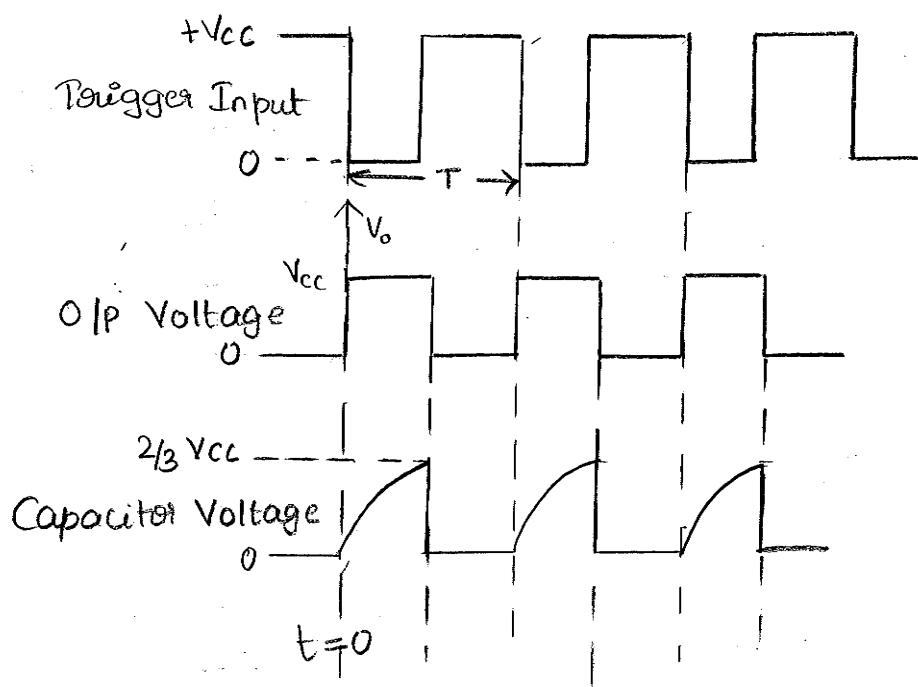


fig ① : 555 timer in Monostable operation with functional diagram.





fig③ : Monostable Multivibrator



fig③ : Input and Output Waveforms.

* Assume that the O/P of the 555 timer is initially low i.e. the circuit is in a stable state, transistor Q₁ is ON and Capacitor 'C' is shorted to ground.



By the application of -ve trigger pulse to pin-2, transistor Q_1 is Turn-OFF, Which releases the short ckt across the capacitor 'C' & drives the o/p to high. [i.e. $Q=0$ & $\bar{Q}=1$].

Now the capacitor 'C' starts charging towards V_{cc} through R_A . When the voltage across the capacitor 'C' equals $2/3 V_{cc}$, the Comparator 1 o/p goes to high, which inturn drives [to] the o/p to low state [i.e. $Q=1$ & $\bar{Q}=0$].

* Now Transistor Q_1 is ON [$\because Q=1$] & hence Capacitor 'C' discharges through the transistor Q_1 .

The o/p of the monostable multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats.

So a rectangular wave is produced at the o/p. The pulse width of this rectangular pulse is controlled by the charging time of capacitor & Resistor.

Thus $R_A C$ Controls the pulse width.



Derivation of Pulse width :-

The voltage across capacitor increases exponentially and is given by :

$$V_C = V_{CC} \left[1 - e^{-t/R_{AC}} \right] \rightarrow ①$$

$$\text{at } t = T, V_C = \frac{2}{3} V_{CC}$$

Now eq ① becomes

$$\frac{2}{3} V_{CC} = V_{CC} \left[1 - e^{-T/R_{AC}} \right]$$

$$\frac{2}{3} = 1 - e^{-T/R_{AC}}$$

$$\frac{2}{3} - 1 = - e^{-T/R_{AC}}$$

$$\frac{2-3}{3} = - e^{-T/R_{AC}}$$

$$+\frac{1}{3} = + e^{-T/R_{AC}}$$

$$e^{-T/R_{AC}} = \frac{1}{3}$$



$$e^{-\frac{T}{RAC}} = \frac{1}{3}$$

$$-\frac{T}{RAC} = \ln\left[\frac{1}{3}\right]$$

$$+\frac{T}{RAC} = +1.0996$$

$$T = 1.0996 RAC$$

$$\therefore T \approx 1.1 RAC \rightarrow ②$$

Eq ② indicates that the OLP Voltages waveform depends on the values of $R_A + C$ and it is independent of V_{cc} .





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Problems :

1] Design a monostable multivibrator using 555 timer to obtain a pulse width of 10msec

Jan-10, 6M

Sol3 Given, $T = 10\text{ msec}$

$$\text{WKT, } T = 1.1 R_{AC} C$$

$$R_{AC} = \frac{T}{1.1}$$

$$R_{AC} = \frac{10\text{ msec}}{1.1}$$

$$R_{AC} = 9.09\text{ msec}$$

← [2M]

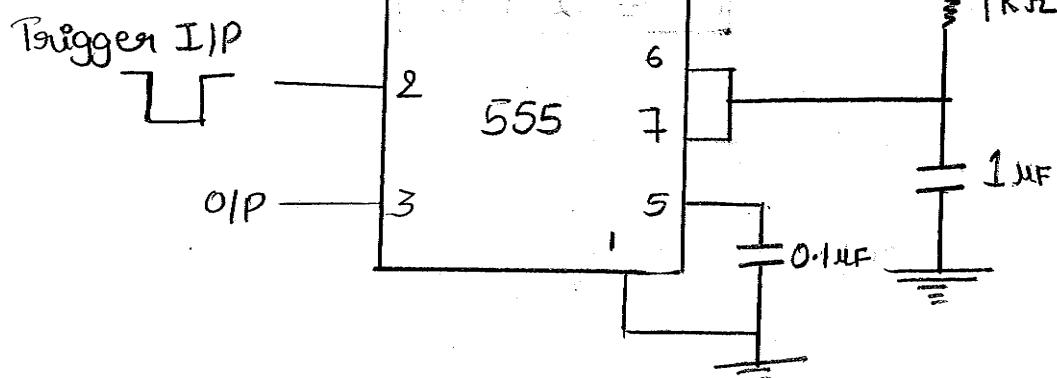
Assume $C = 1\text{ uF}$

← [1M]

$$R_A = \frac{9.09\text{ msec}}{1\text{ uF}} = 9.09\text{ k}\Omega$$

∴ $R_A = 9.9\text{ k}\Omega$

← [2M]



2] In the monostable multivibrator, the component values are $R_A = 5.6\text{ k}\Omega$, $C = 0.068\text{ HF}$. Find the pulse width T .

Sols $\text{WKT, } T = 1.1 R_A C$

$$= 1.1 \times 5.6\text{ k}\Omega \times 0.068\text{ HF}$$

$$T = 0.42\text{ msec}$$

3] In the monostable multivibrator, $R = 100\text{ k}\Omega$ & the time delay $T = 100\text{ msec}$. Calculate the value of C . Verify the value of C obtained.

Sols $\text{WKT, } T = 1.1 R_A C$

$$T = 1.1 \times 100\text{ k}\Omega \times C$$

$$\frac{100\text{ msec}}{1.1 \times 100\text{ k}\Omega} = C$$

$$C = 0.9\text{ HF}$$



Astable Multivibrator :-

* 555 timer as astable multivibrator.

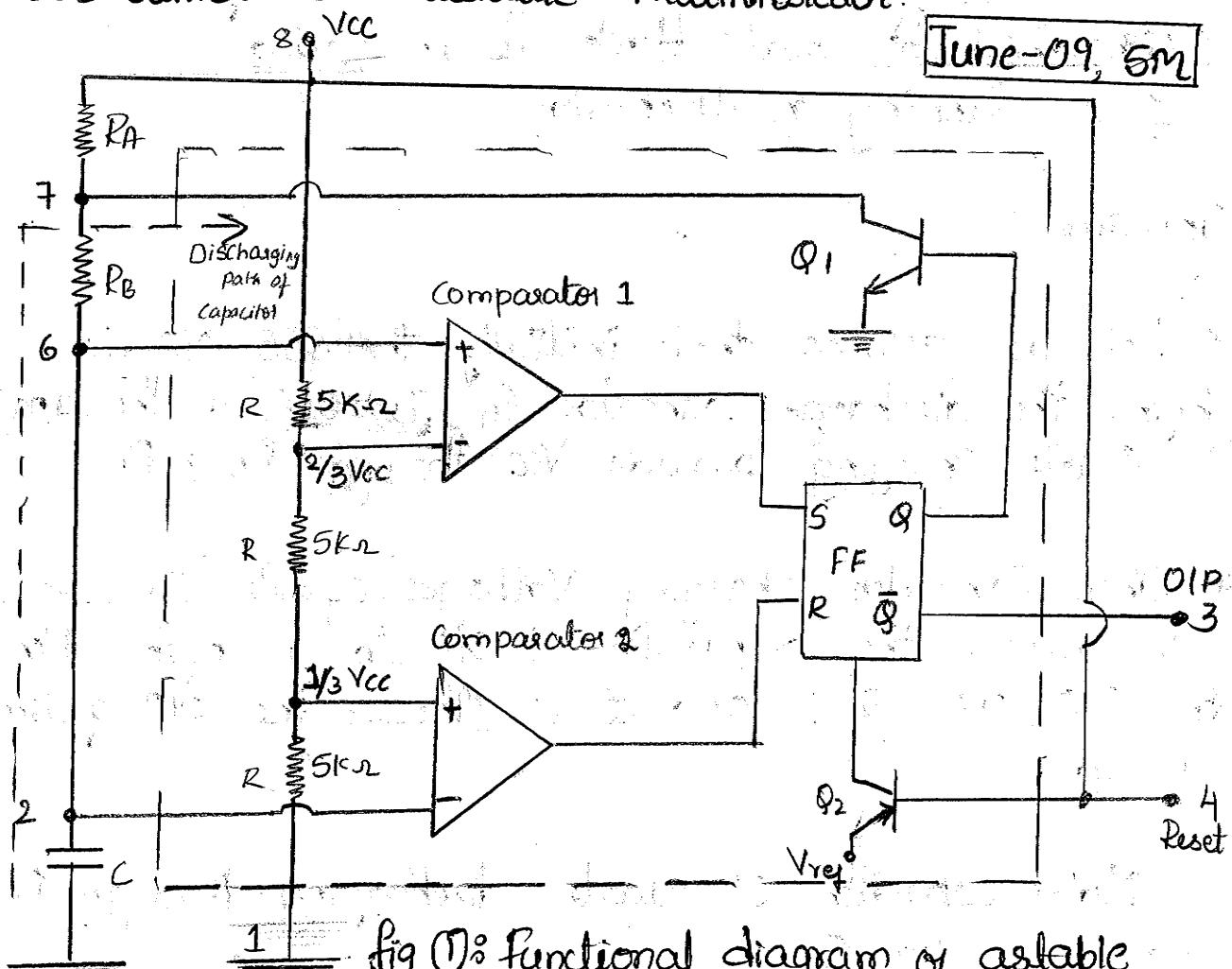


fig ①: functional diagram of astable multivibrator using 555 timer.

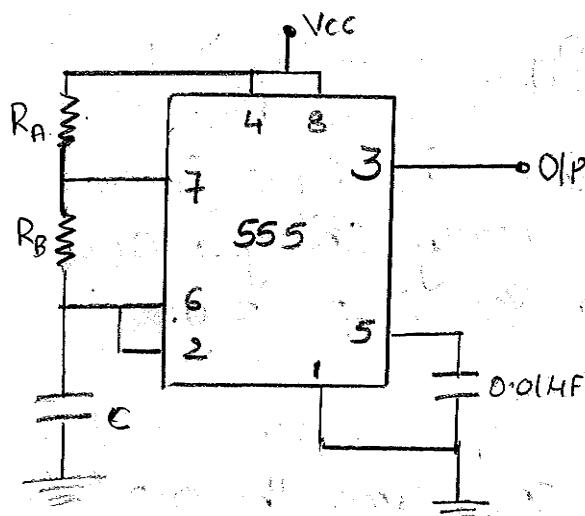


fig ②: Astable Multivibrator Using 555 timer

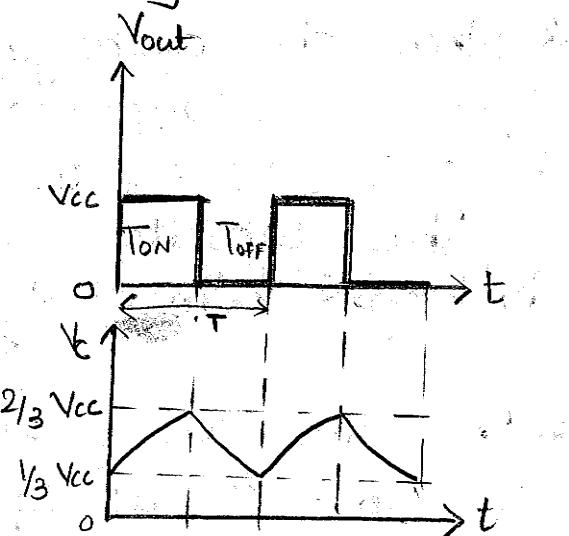


fig ③ ④: O/P waveforms



* An Astable multivibrator is a rectangular wave generating Circuit. This Ckt does not require an external trigger to change the state of the O/P [either high or low]. Hence it is called free running multivibrator.

Operation :

* Let us assume that initially the 555 O/P is high, the discharge transistor Q_1 is OFF & the capacitor 'C' starts charging towards V_{cc} through R_A & R_B .

* When Capacitor charging Voltage equals to $\frac{2}{3} V_{cc}$, it causes the Comparator 1 O/P to go high. Hence the FlF O/P $Q=1$ and $\bar{Q}=0$. Thus, the O/P of timer is low.

Now capacitor 'C' starts discharging through R_B and transistor Q_1 .

* When the discharging Voltage across the capacitor 'C' equals $\frac{V_{cc}}{3}$, Comparator 2 O/P goes to high and hence it resets the FlF. Then the cycle repeats.

Thus Capacitor is periodically charged and discharged between $\frac{2}{3} V_{cc}$ to $\frac{V_{cc}}{3}$ respectively.

* The time during which the Capacitor charges from $\frac{V_{cc}}{3}$ to $\frac{2}{3} V_{cc}$ is equal to the time the O/P is high.



By The time during which the capacitor discharges from $\frac{2V_{cc}}{3}$ to $\frac{V_{cc}}{3}$ is equal to the time the opamp is low.

* The charging time for the capacitor is given by

$$T_c = 0.693 [R_A + R_B] C$$

* The discharging time for the capacitor is given by

$$T_d = 0.693 R_B C$$

* The time for one cycle is

$$T = T_c + T_d = 0.693 [R_A + R_B] C + 0.693 R_B C$$

$$T = 0.693 R_A C + 0.693 R_B C + 0.693 R_B C$$

$$T = 0.693 [R_A + 2R_B] C$$

* Duty Cycle $\% D = \frac{T_c}{T} \times 100$

$$\% D = \frac{0.693 [R_A + R_B] C}{0.693 [R_A + 2R_B] C} \times 100$$

$$\% D = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$



* Frequency of oscillation is given by,

$$f = \frac{1}{T}$$

$$f = \frac{1}{T} = \frac{1}{0.693[R_A+2R_B]C}$$

$$f = \frac{1}{0.693} \times \frac{1}{C(R_A+2R_B)}$$

$$f = \frac{1.44}{C[R_A+2R_B]}$$

$$\therefore f = \frac{1.44}{[R_A+2R_B]C} H_3$$



* Derive an expression for charging and discharging time for Astable Multivibrator. [T_c or T_{on} & T_d or T_{off}]

→ The expression for capacitor charging is given by

$$V_C = V_{CC} \left[1 - e^{-t/RC} \right] \rightarrow ①$$

Eq. ① is valid only if the initial voltage on the capacitor is zero.

→ If there is a some initial voltage present then the charging equation gets modified as follows:

$$V_C = V_F + (V_i - V_F) e^{-t/RC} \rightarrow ②$$

Where, $V_F \rightarrow$ Final Voltage

$V_i \rightarrow$ Initial Voltage

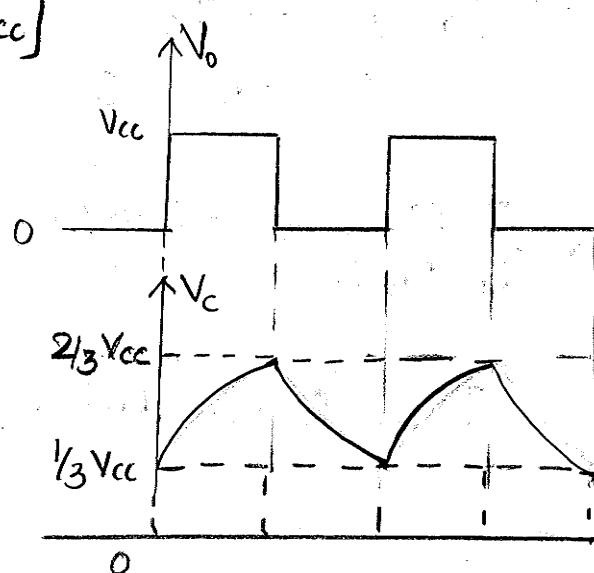
T_{on} or T_c :- $[V_C = \frac{2}{3} V_{CC}]$

During charging period,

At, $t = T_c$,

$V_i = \frac{V_{CC}}{3}$, $V_F = V_{CC}$,

$R = R_A + R_B$



Now Eq ② becomes,

$$\frac{2}{3} V_{cc} = V_{cc} + \left[\frac{V_{cc}}{3} - V_{cc} \right] e^{-T_c / (R_A + R_B) C}$$

$$\frac{2}{3} V_{cc} - V_{cc} = \left[\frac{V_{cc} - 2V_{cc}}{3} \right] e^{-T_c / (R_A + R_B) C}$$

$$\frac{2V_{cc} - 2V_{cc}}{3} = \left[-\frac{2V_{cc}}{3} \right] e^{-T_c / (R_A + R_B) C}$$

$$+\frac{V_{cc}}{\cancel{3}} = +\frac{2V_{cc}}{\cancel{3}} e^{-T_c / (R_A + R_B) C}$$

$$\frac{1}{2} = e^{-T_c / (R_A + R_B) C}$$

$$0.5 = e^{-T_c / (R_A + R_B) C}$$

$$\ln(0.5) = -\frac{T_c}{(R_A + R_B) C}$$

$$+\frac{T_c}{(R_A + R_B) C} = +0.693$$

$$T_c = 0.693 [R_A + R_B] C$$



T_{OFF} or T_d :

The capacitor discharges from $\frac{2V_{cc}}{3}$ to $\frac{V_{cc}}{3}$

∴ At $t = T_d$, $V_i = \frac{2V_{cc}}{3}$, $V_F = 0$, $R = R_B$

Now eq. ② becomes,

$$\frac{V_{cc}}{3} = 0 + \left[\frac{2V_{cc}}{3} - 0 \right] e^{-T_d/R_B C}$$

$$\frac{V_{cc}}{3} = \frac{2V_{cc}}{3} e^{-T_d/R_B C}$$

$$\frac{1}{2} = e^{-T_d/R_B C}$$

$$e^{-T_d/R_B C} = 0.5$$

$$-\frac{T_d}{R_B C} = \ln(0.5)$$

$$+\frac{T_d}{R_B C} = +0.693$$

$T_d = 0.693 R_B C$

→ Total time period is given by

$$T = T_c + T_d$$



$$T = 0.693 [R_A + R_B] C + 0.693 R_B C$$

$$\therefore T = 0.693 [R_A + 2R_B] C$$

* The frequency of oscillation is given by

$$f = \frac{1}{T} = \frac{1}{0.693 [R_A + 2R_B] C}$$

$$f = \frac{1.44}{[R_A + 2R_B] C} \text{ Hz}$$

→ Duty Cycle :

$$\% D = \frac{T_C}{T} \times 100$$

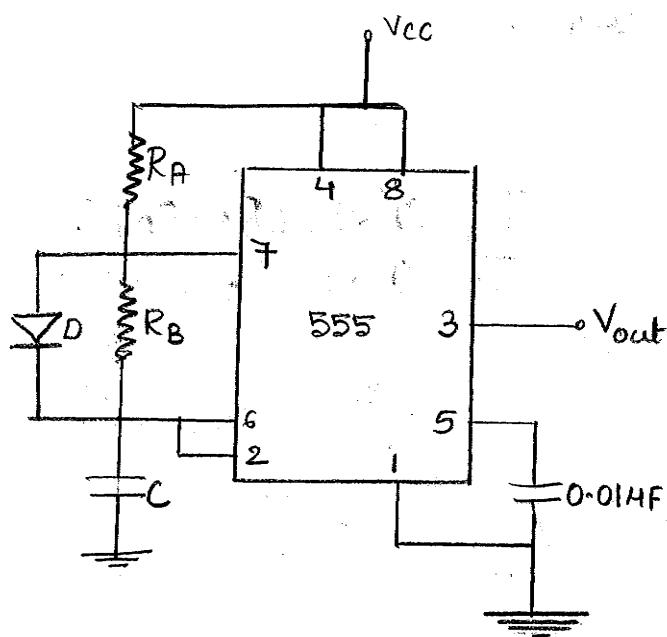
$$= \frac{0.693 [R_A + R_B] C}{0.693 [R_A + 2R_B] C} \times 100$$

$$\% D = \frac{[R_A + R_B]}{[R_A + 2R_B]} \times 100$$

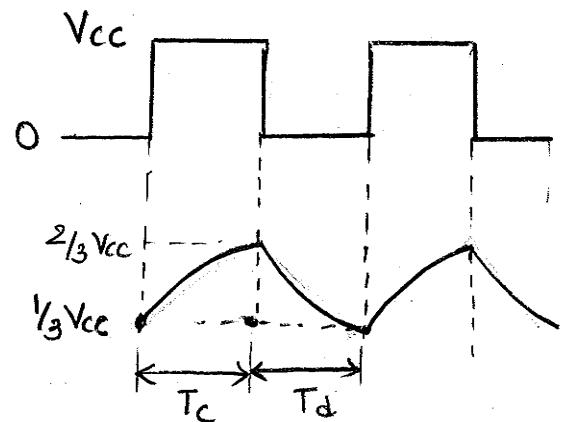


Astable Multivibrator to generate Square wave.

[Duty Cycle = 50.1%]



Fig①: Square wave generator



Fig②: Square wave.

* To get exactly 50.1% duty cycle i.e. square wave op it is necessary to modify the astable timer ckt.

In modified astable ckt, the capacitor 'C' charges through R_A and diode D & discharges through R_B .

\therefore

$$T_c = 0.693 R_A C$$

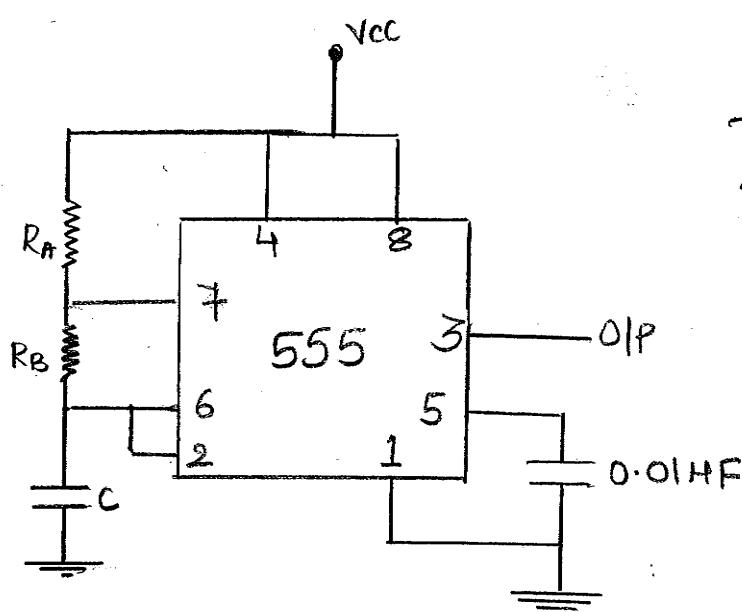
&

$$T_d = 0.693 R_B C$$



NOTE :

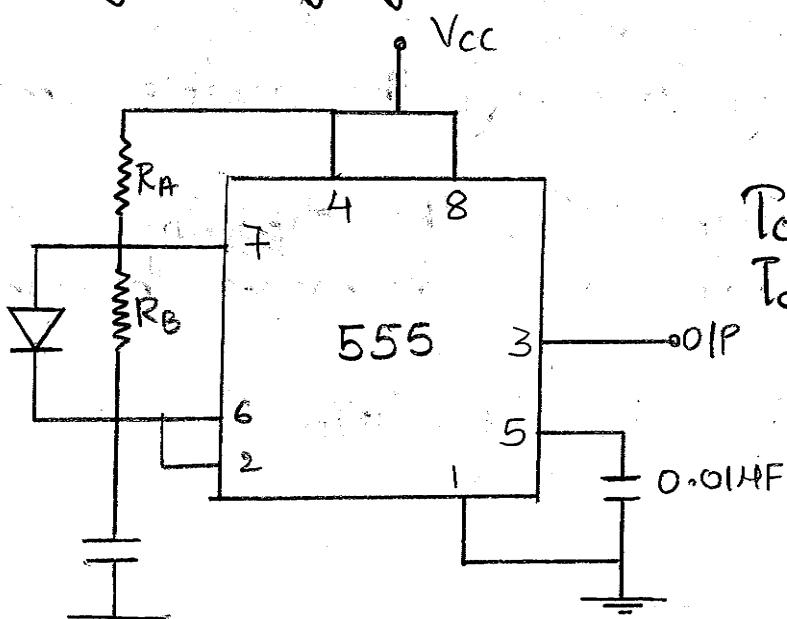
1] To get Duty Cycle ' $D > 50\%$ '.



$$T_c = 0.693 [R_A + R_B] C$$

$$T_d = 0.693 R_B C$$

2] To get Duty Cycle ' $D \leq 50\%$ '.



$$T_c = 0.693 R_A C$$

$$T_d = 0.693 R_B C$$



Problems :

i] For the astable multivibrator, $R_A = 4.7\text{ k}\Omega$, $R_B = 1\text{ k}\Omega$ and $C = 1\text{ }\mu\text{F}$. Determine

- i] The positive pulse width ' T_c '
- ii] The negative pulse width ' T_d '
- iii] Free-running frequency ' f '
- iv] Duty cycle

Sol:

$$\begin{aligned} i] \quad T_c &= 0.693 [R_A + R_B] C \\ &= 0.693 [4.7\text{ k} + 1\text{ k}] \times 14 \\ T_c &= 3.933\text{ msec} \end{aligned}$$

$$\begin{aligned} ii] \quad T_d &= 0.693 R_B C \\ &= 0.693 \times 1\text{ k} \times 1 \times 10^{-6} \end{aligned}$$

$$T_d = 0.69\text{ msec}$$

$$iii] \quad f = \frac{1}{T}$$

$$T = T_c + T_d = 3.933\text{ msec} + 0.69\text{ msec} = 4.623\text{ msec}$$

$$f = \frac{1}{4.623\text{ msec}}$$

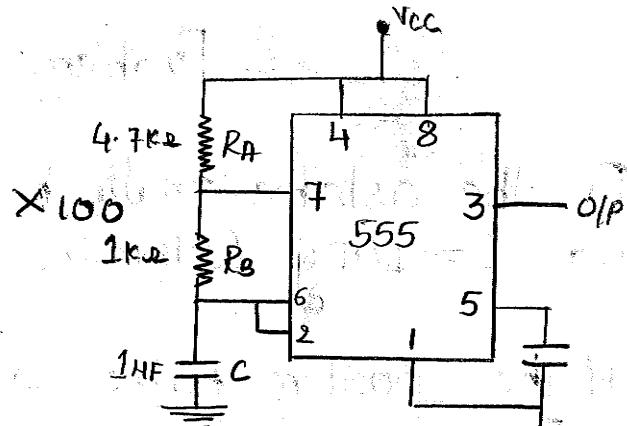
$$f = 216.31\text{ Hz}$$



$$\text{IV] Duty Cycle} = \frac{T_c}{T} \times 100 \cdot \%$$

$$= \frac{3.983 \times 10^{-3}}{4.623 \times 10^{-3}} \times 100$$

$$\boxed{\text{Duty Cycle} = 85.07\%}$$



2] Design an Astable multivibrator Using 555 Timer to generate an O/P waveform of 2kHz with a duty cycle of 50%.

Sol → Given,

$$D = 50\%, f = 2\text{Hz} \times 10^3 = 2\text{kHz}$$

$$T = \frac{1}{f} = \frac{1}{2\text{kHz}}$$

$$\boxed{T = 0.5\text{msec}}$$

WKT, In 50% duty cycle $T_{on} = T_{off}$ i.e. $T_c = T_d$

$$* T_c = 0.693 R_A C$$

Assuming

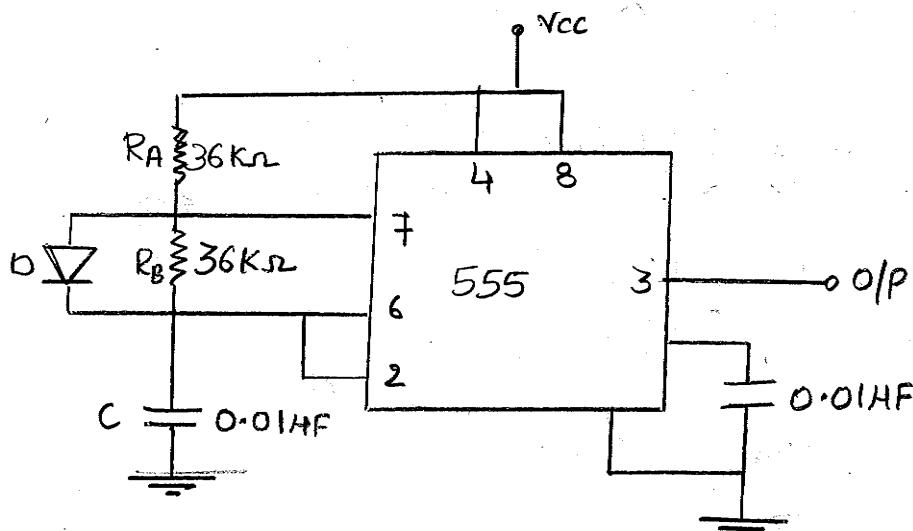
$$\boxed{C = 0.01\text{nF}}$$

$$R_A = \frac{T_c}{0.693 C} = \frac{0.5\text{msec}}{0.693 \times 0.01 \times 10^{-9}}$$



$$R_A = 36 \cdot 07 \text{ k}\Omega$$

$$\therefore R_A = R_B = 36 \cdot 07 \text{ k}\Omega$$



3] Design a 555 astable multivibrator to operate at 5kHz with a duty cycle of 40%.

$$\text{Sol} \Rightarrow f = 5 \text{ kHz},$$

$$D = 0.4$$

$$T = \frac{1}{f} = \frac{1}{5 \text{ kHz}} = 0.2 \text{ msec}$$

$$D = \frac{T_c}{T}$$

$$T_c = D \times T$$

$$T_c = 0.4 \times 0.2 \text{ msec}$$

$$T_c = 0.08 \text{ msec}$$



$$\text{WKT}, \quad T = T_c + T_d$$

$$T_d = T - T_c = 0.2 \text{ msec} - 0.08 \text{ msec}$$

$$T_d = 0.12 \text{ msec}$$

$$\text{WKT}, \quad T_c = 0.693 R_A C$$

$$R_A = \frac{I_c}{0.693 C}$$

Assume

$$C = 0.01 \mu F$$

$$R_A = \frac{0.08 \times 10^{-3}}{0.693 \times 0.01 \mu F}$$

$$R_A = 11.54 \text{ k}\Omega$$

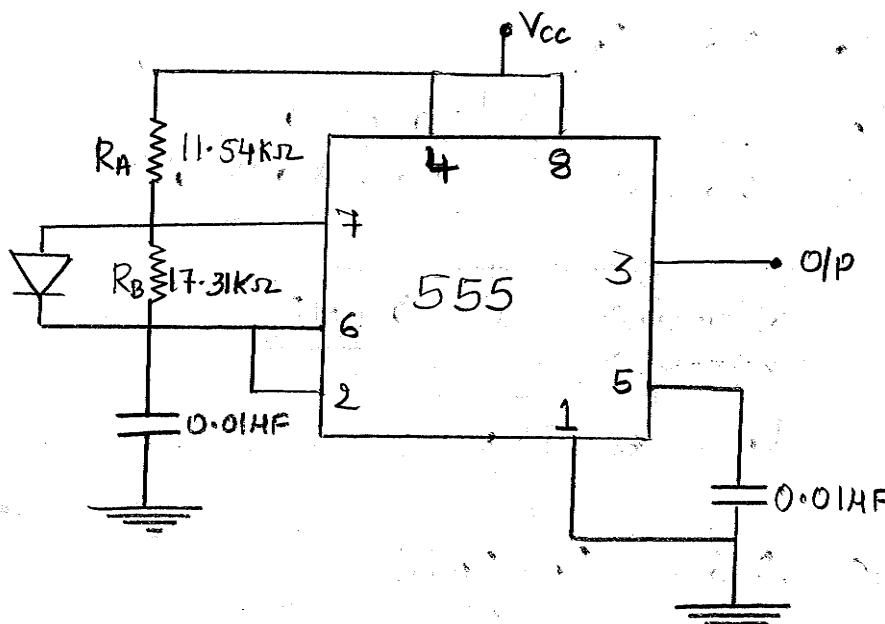
$$\text{WKT}, \quad T_d = 0.693 R_B C$$

$$R_B = \frac{T_d}{0.693 C}$$

$$= \frac{0.12 \times 10^{-3}}{0.693 \times 0.01 \times 10^{-6}}$$

$$R_B = 17.31 \text{ k}\Omega$$





4] Design a 555 astable multivibrator for an O/p frequency of 1kHz & duty cycle 60.1.

Soln,

$$f = 1\text{kHz}, \quad D = 0.6$$

$$* T = \frac{1}{f} = \frac{1}{1\text{kHz}} = 1\text{msec}$$

$$* D = \frac{T_c}{T}$$

$$0.6 = \frac{T_c}{1\text{msec}}$$

$T_c = 0.6 \times 1\text{msec} = 0.6\text{msec}$

$* \text{WKT, } T = T_c + T_d$

$T_d = T - T_c = 1\text{msec} - 0.6\text{msec}$

$T_d = 0.4\text{msec}$



* WKT, $T_d = 0.693 R_B C$

$$R_B = \frac{T_d}{0.693 C} = \frac{0.4 \times 10^{-3}}{0.693 \times 0.1 \times 10^{-6}}$$

Assuming $C = 0.1 \text{ nF}$

$$R_B = 5.77 \text{ k}\Omega$$

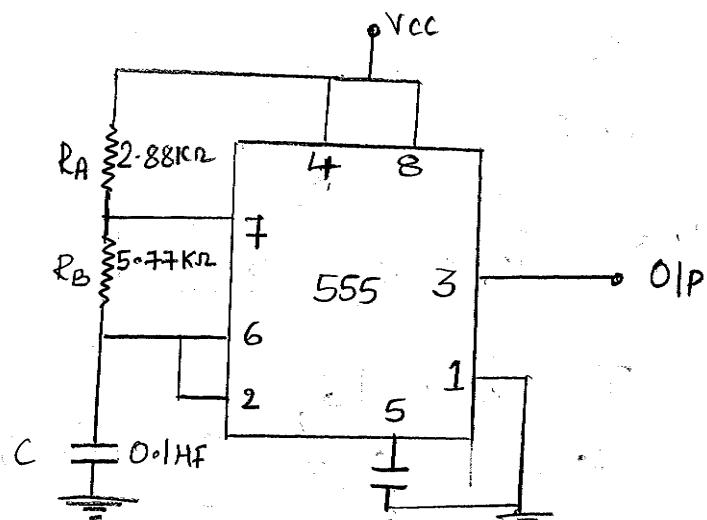
* WKT, $T_C = 0.693 [R_A + R_B] C$

$$R_A + R_B = \frac{T_C}{0.693 C}$$

$$R_A = \frac{T_C}{0.693 C} - R_B$$

$$R_A = \frac{0.6 \times 10^{-3}}{0.693 \times 0.1 \times 10^{-6}} - 5.77 \times 10^3$$

$$R_A = 2.88 \text{ k}\Omega$$



5] A 555 Stable multivibrator has $R_A = 2.2k\Omega$ and $R_B = 6.8k\Omega$ and $C = 0.01\text{HF}$
 Calculate, i] t_{high} ii] t_{low} iii] free-running frequency
 and iv] Duty Cycle.

Draw the connection diagram.

June-08, 7M

Sols

i] t_{high}

$$T_C = 0.693 [R_A + R_B] C = 0.693 [2.2k\Omega + 6.8k\Omega] 0.01\text{HF}$$

$$T_C = 0.062 \text{ msec}$$

← (1m)

ii] t_{low}

$$T_D = 0.693 R_B C = 0.693 \times 6.8k\Omega \times 0.01\text{HF}$$

$$T_D = 0.047 \text{ msec}$$

← (1m)

iii] free-running frequency

$$T = T_C + T_D = 0.062 \times 10^{-3} + 0.047 \times 10^{-3}$$

$$T = 0.109 \text{ msec}$$

$$f = \frac{1}{T} = \frac{1}{0.109 \text{ m}} = 9.14 \text{ kHz}$$

$$f = 9.14 \text{ kHz}$$

← (2M)



(Q1)

$$f = \frac{1.14}{(R_A + 2R_B)C} = \frac{1.14}{(2.2k + 2 \times 6.8k) \times 0.01\mu F}$$

$$\boxed{f = 9.44 kHz} \quad \leftarrow (2M)$$

iv] Duty Cycle

$$D = \frac{T_C}{T}$$

$$(Q1) \quad D = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

$$= \frac{0.062 \text{ msec}}{0.109 \text{ msec}}$$

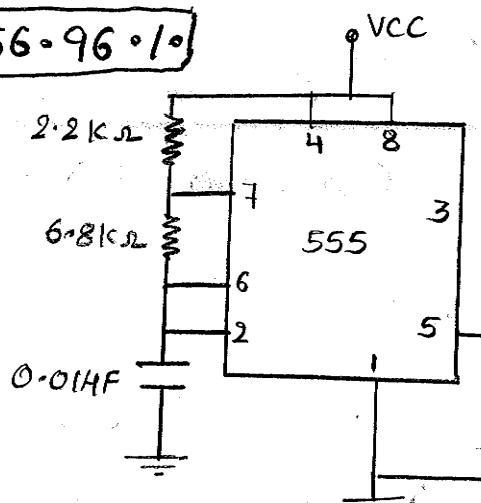
$$D = \frac{(2.2k + 6.8k)}{(2.2k + 2 \times 6.8k)} \times 100$$

$$D = 0.56$$

$$\boxed{1-D = 56.1}$$

$$\boxed{1-D = 56.1} \quad \leftarrow (2M)$$

$$\boxed{1-D = 56.96 \cdot 10}$$



Schnitt Trigger :

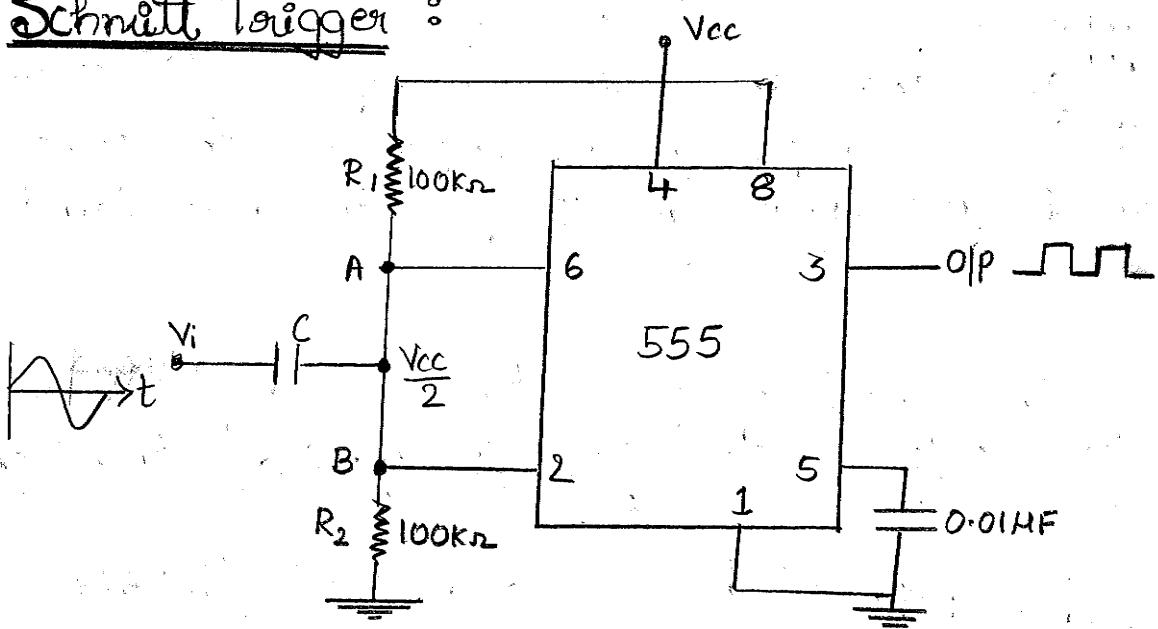


fig ① : 555 timer Connected as Schnitt trigger (ckt)

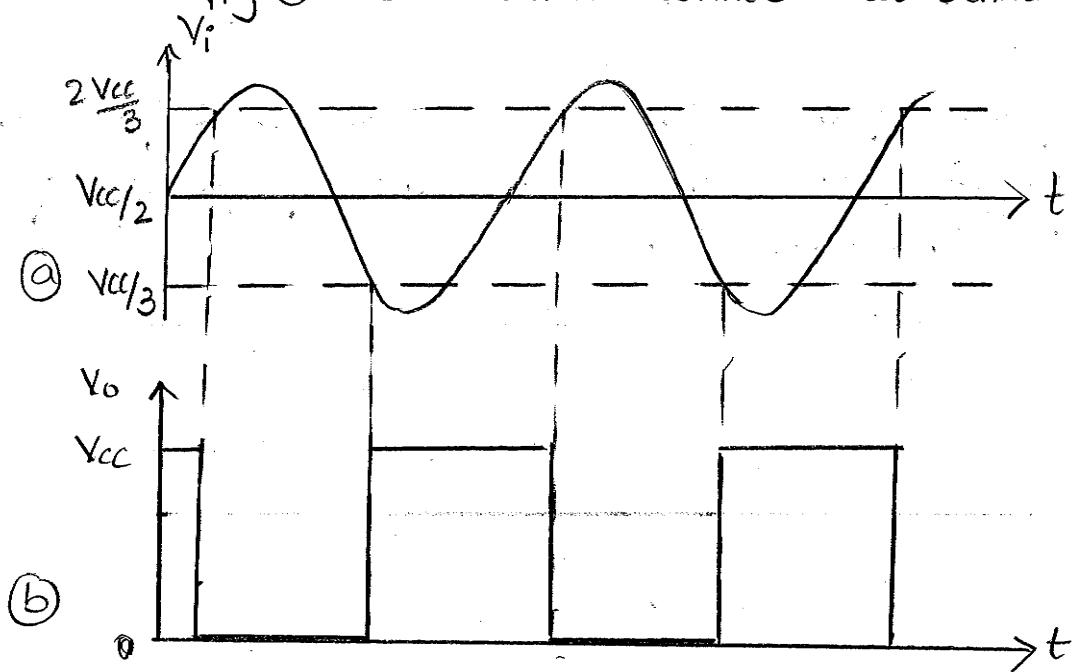


fig ② : (a) Input Voltage Waveform, (b) Output Voltage Waveform.

Fig ① shows a schnitt trigger circuit using a 555 timer. Here the two internal comparators are tied together [Pin 2 & 6] and externally biased at $V_{CC}/2$ through R_1 and R_2 .



- * The upper Comparator will Set when the voltage at point A goes above the bias value of $\frac{V_{cc}}{2}$ to $\frac{2}{3} V_{cc}$. and the lower Comparator will Set when the voltage at point B goes down to $\frac{V_{cc}}{3}$ from the bias value of $\frac{V_{cc}}{2}$.
- * If a Sine wave of ~~peak to peak~~ amplitude greater than $\frac{V_{cc}}{6}$ [$\because \frac{V_{cc}}{6} = \frac{2V_{cc}}{3} - \frac{V_{cc}}{2}$] is applied, then the internal flip-flop will be Set and reset alternately thus producing a square wave at the o/p pin 3.
- * The frequency of the square wave obtained from the Schmitt trigger is same as the frequency of the I/P Sinusoidal Signal.
i.e. I/P Signal Frequency = o/p Signal Frequency.



Phase Locked Loop [PLL] :

* Phase locked loop as automatic frequency controller.

Jan-09, 5M

* Write Explanatory note on PLL

Jan-10, 5M

* With the block diagram, explain the operation of phase locked loop:

Jan-09, 6M [EE]

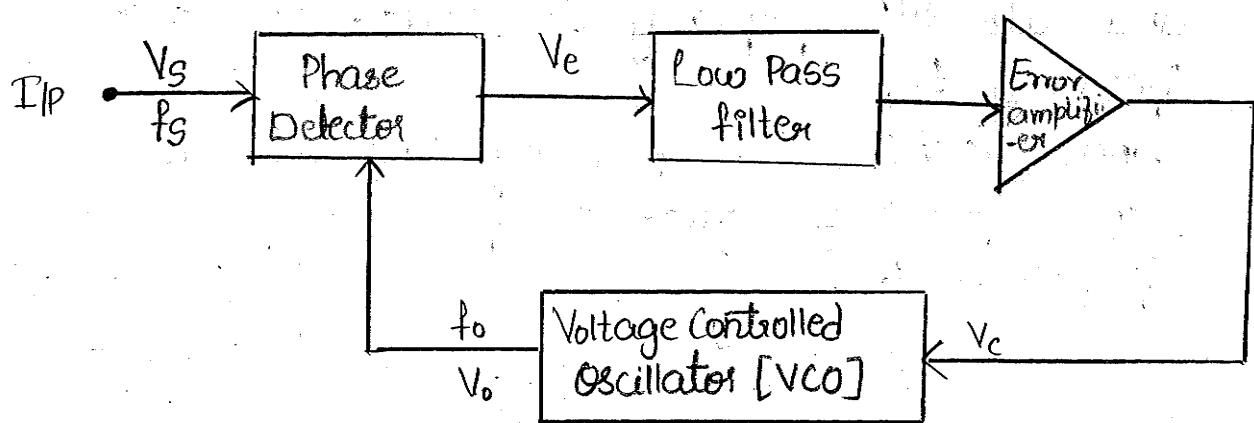


Fig ① : Block diagram of PLL

Fig ① Shows the block diagram of PLL.

PLL is a feedback system consists of :

- 1] Phase detector
- 2] Low-Pass filter
- 3] Error amplifier
- 4] Voltage Controlled Oscillator [VCO]



* The VCO is a free running multivibrator which operates at a frequency ' f_0 ' [determined by an external timing resistor & an external capacitor] called free running frequency.

*

* A VCO is an oscillator Ckt in which the O/P frequency ' f_0 ' can be controlled by an externally applied voltage. The VCO provides the linear relationship between the applied voltage and the oscillator frequency. The applied voltage is called control voltage ' V_c '.

{ When $V_c = 0$, VCO is in free-running mode and its O/P frequency is called as center frequency ' f_0 '.

When $V_c \neq 0$, VCO frequency will shift to some other frequency called ' f ' from a free running frequency ' f_0 '. }

* Let an input signal of amplitude ' V_s ' & frequency ' f_s ' be applied to the PLL. The phase detector compares the phase and frequency of the incoming signal to that of the O/P ' V_o ' of the VCO.

* If there is a difference in either the frequency or in phase or in both, then phase detector generates an error voltage V_e .

The phase detector produces the sum [$f_s + f_o$] and differences [$f_s - f_o$] components at its O/P. The high



frequency Component ($f_s + f_o$) is removed by the low pass filter and the difference frequency Component is amplified and then applied as Control Voltage ' V_c ' at VCO.

- * The Signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s & f_o . As soon as this happens, then PLL is said to be in Capture range.
- * The VCO Continues to change frequency till its OIP frequency becomes equal to the Input Signal frequency. The Ckt is said to be locked.

Once the PLL is locked, the OIP frequency of VCO i.e. f_o is identical to f_s except for a finite phase difference ϕ .

- * After achieving locking, the PLL then tracks the frequency changes in the input signal.

Thus, a PLL goes through three stages :

- i] free running ii] Capture and iii] Locked or tracking



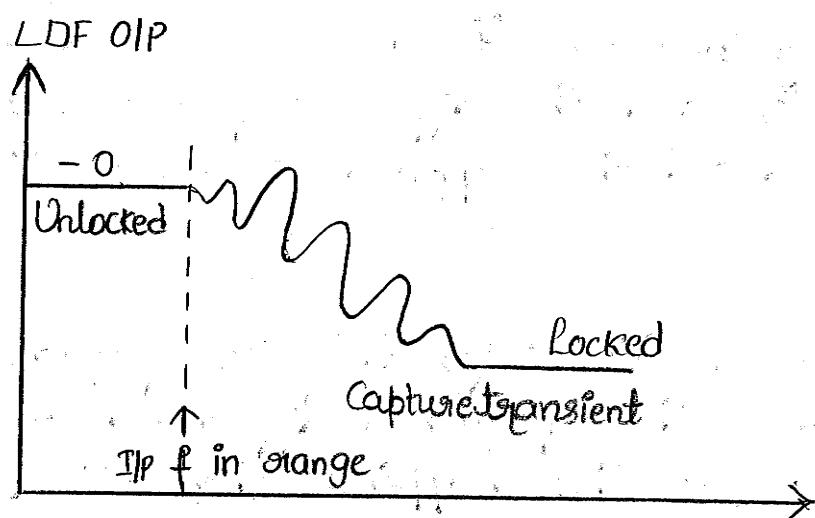


fig ② : The Capture transient.

Figure ② Shows the Capture transient. As capture starts, a small sine wave appears. This is due to the frequency difference between the VCO and the IIP Signal.

Each successive cycle causes the VCO frequency to move closer to the IIP Signal frequency.



Important definitions related to PLL :-

* Explain the following for a PLL

- i] Lock-in range ii] Capture range
- iii] Pull-in time

June-08, 6M

* Define lock-in range and capture range with reference to PLL.

Jan-11, 2M

i] Lock-in Range (①) Tracking range :-

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range ① Tracking range.

The lock range is usually expressed as a percentage of f_0 (VCO frequency).

ii] Capture range :-

The range of frequencies over which the PLL can acquire lock with an IIP signal is called the capture range.

Capture range is also expressed as a percentage of f_0 .



iii] Pull-in time :-

The total time taken by the PLL to establish lock is called Pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.



Voltage Controlled Oscillator [VCO] :-

* 566 Voltage Controlled Oscillator

June-09, 5M

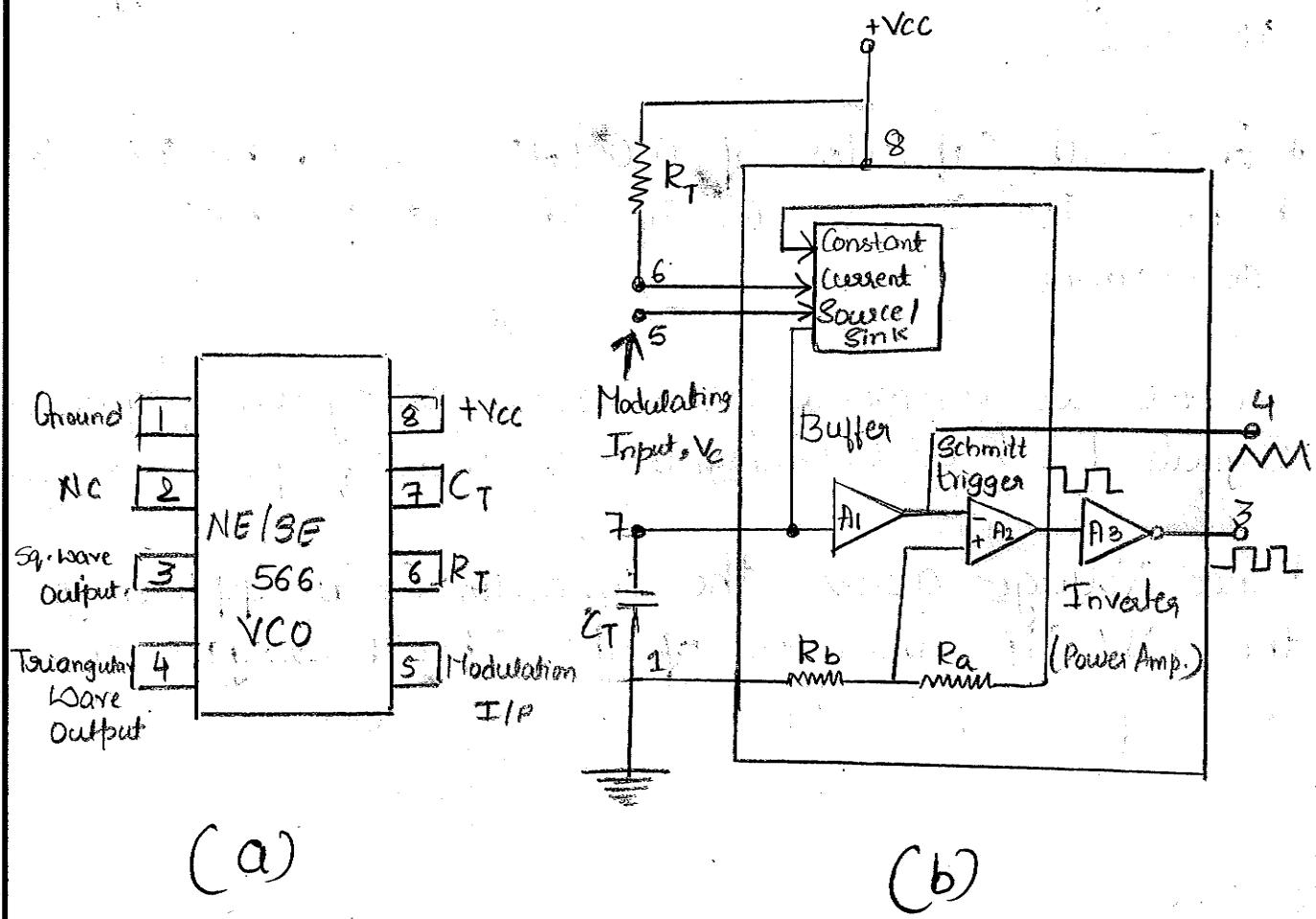


fig 1 : Voltage Controlled Oscillator.

- Pin Configuration.
- Block Diagram.

VCO is available in the IC form manufactured by Signetics with brand name NE136 566.

* In fig 1 (b), a timing capacitor C_T is linearly charged (a) discharged by a Constant Current Source/Sink.

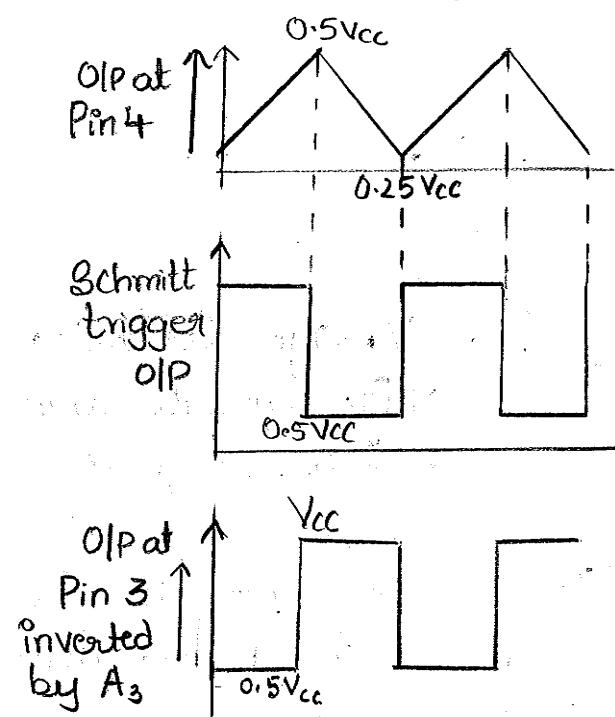
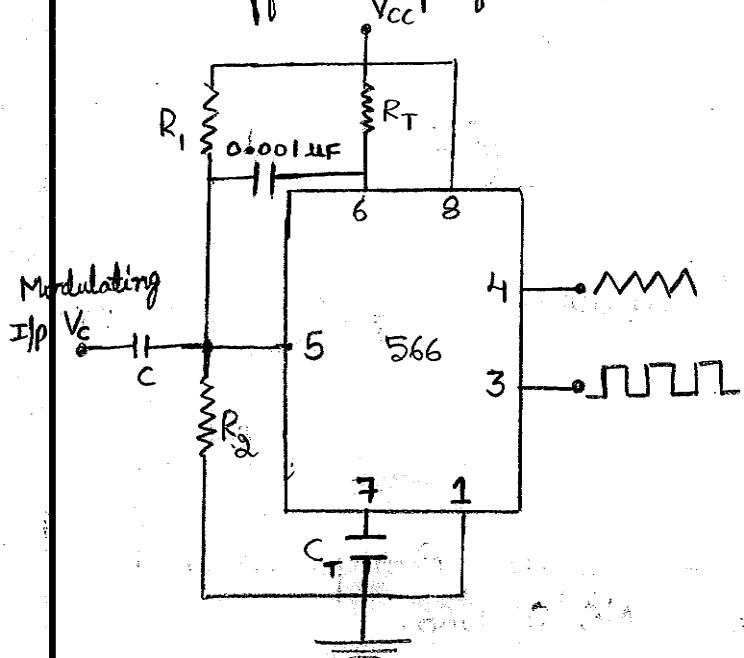


The amount of current can be controlled by changing the voltage V_C applied at the modulating input (Pin 5) or by changing the timer resistor R_T external to IC chip. The voltage at Pin 6 is held at the same voltage as Pin 5.

* A small capacitor of 0.001 μF should be connected between Pin 5 and 6 to eliminate possible oscillations.

A VCO is commonly used in converting low frequency signals [such as EEGs] into an audio frequency range.

* The voltage across the capacitor C_T is applied to the INV IIP terminal of the Schmitt trigger A_2 via buffer amplifier A_1 .



Fig(2): (a) Typical Connection diagram, (b) OLP Waveform



* The OIP Voltage Swing of the Schmitt trigger is designed to V_{cc} and $0.5V_{cc}$. If $R_a = R_b$, the voltages at the Non-INV terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$.

In fig 2 (b), When the voltage on the capacitor C_T exceeds $0.5V_{cc}$ during charging, the OIP of the Schmitt trigger goes Low [i.e $0.5V_{cc}$]. The capacitor now discharges and when it is at $0.25V_{cc}$, the OIP of Schmitt trigger goes High (V_{cc}).

* The Capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at Pin 4.

* The square wave OIP of the Schmitt trigger is inverted by inverter A_3 and is available at Pin 3.

* The OIP frequency of the VCO is given by :

$$f_o = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}} \rightarrow ①$$

The OIP frequency of the VCO can be changed either by,

i] R_T ii] C_T iii] V_c .

* With no modulating input signal, if the Voltage at Pin 5 is biased at $\frac{7}{8}V_{cc}$, Eq ① gives the VCO



OLP frequency as ,

$$f_0 = \frac{2(V_{CC} - 7/8 V_{CC})}{C_T R_T V_{CC}} = \frac{2 \left(\frac{8V_{CC} - 7V_{CC}}{8} \right)}{C_T R_T V_{CC}}$$

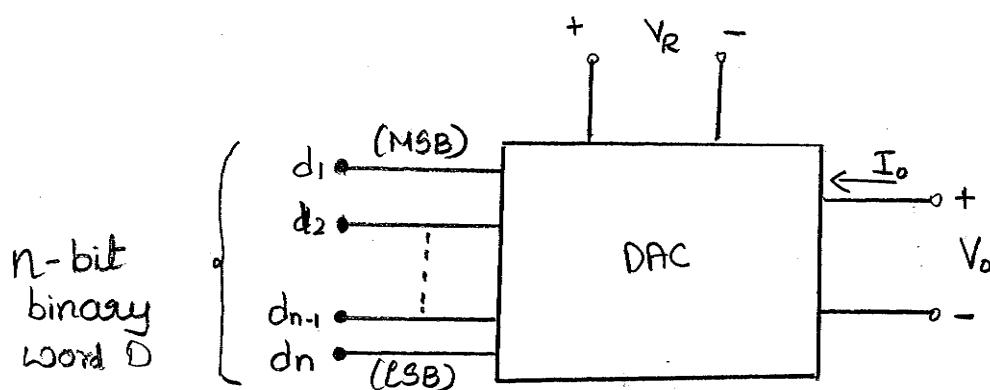
$$f_0 = \frac{2V_{CC}}{8 C_T R_T V_{CC}}$$

$$f_0 = \frac{1}{4 C_T R_T}$$

$f_0 = \frac{0.25}{R_T C_T}$



Basic DAC Techniques :



fig① : Schematic of a DAC

* The input to the DAC is a n -bit binary word D whose digits are d_1, d_2, d_3, d_4 [i.e. $D = d_1, d_2, \dots, d_n$] and is combined with a reference Voltage V_r to give an analog O/P Signal.

The O/P of a DAC can be either a Voltage or Current. The analog O/P voltage is expressed as :

$$V_o = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \dots + d_n 2^{-n})$$

Where, K = Scaling factor usually adjusted to unity

V_{FS} = full scale O/P Voltage

d_1 = Most Significant bit [MSB] with a weight of $V_{FS}/2$

d_n = Least Significant bit [LSB] with a weight of $V_{FS}/2^n$



Weighted Resistor DAC (Q1) Binary Weighted Resistor DACs -

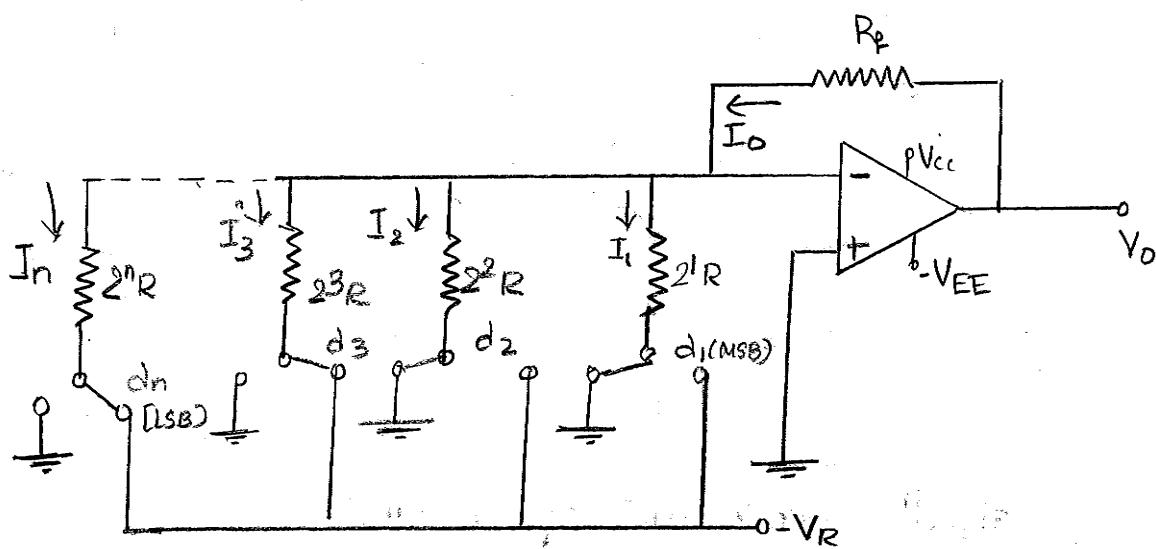


fig : A Simple weighted resistor DAC

- * The DAC Uses an summing Op-amp with a binary weighted resistor $2^1 R, 2^2 R, 2^3 R, \dots, 2^n R$ as shown in fig @
- * It has n-electronic switches d_1, d_2, \dots, d_n Controlled by the binary $1/p$ word. These switches are Single pole double throw [SPDT] type.
- * If the binary input to a particular switch is 1, it connects the resistance to the reference Voltage (-ve).
- * If the input bit is 0, the switch connects the resistor to the ground.

From fig @, the o/p Current I_o for an ideal Op-amp can be written as

$$I_o = I_1 + I_2 + I_3 + \dots + I_n$$



$$I_0 = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3 + \dots + \frac{V_R}{2^n R} d_n$$

Where $d_1, d_2, d_3, \dots, d_n$ may be either 0 or 1 depending on the binary input word.

$$I_0 = \frac{V_R}{R} [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}] \rightarrow ①$$

* The OIP Voltage

$$V_o = I_0 R_f \rightarrow ②$$

Sub Eq ① in Eq ②

$$V_o = V_R \left[\frac{R_f}{R} \right] [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$

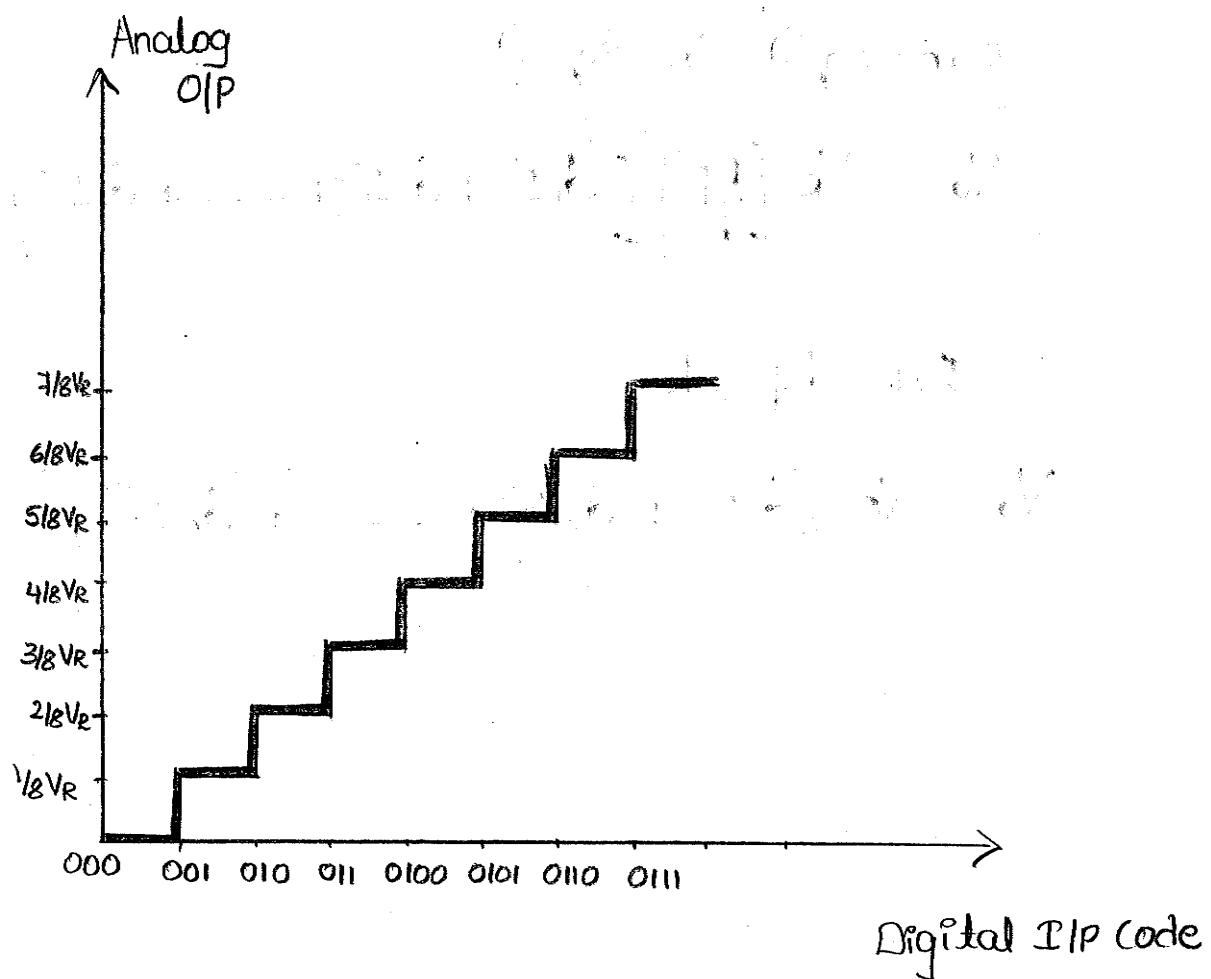
Let $R_f = R$

$$V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}]$$



Eg: for 3-bit DAC

Digital I/P			Analog O/P
d_1	d_2	d_3	V_o
0	0	0	0
0	0	1	$1/8 V_R$
0	1	0	$2/8 V_R$
0	1	1	$3/8 V_R$
1	0	0	$4/8 V_R$
1	0	1	$5/8 V_R$
1	1	0	$6/8 V_R$
1	1	1	$7/8 V_R$



Digital I/P Code



* Briefly explain the working of a 4-bit binary weighted resistor DAC.

Jan-11, 6M

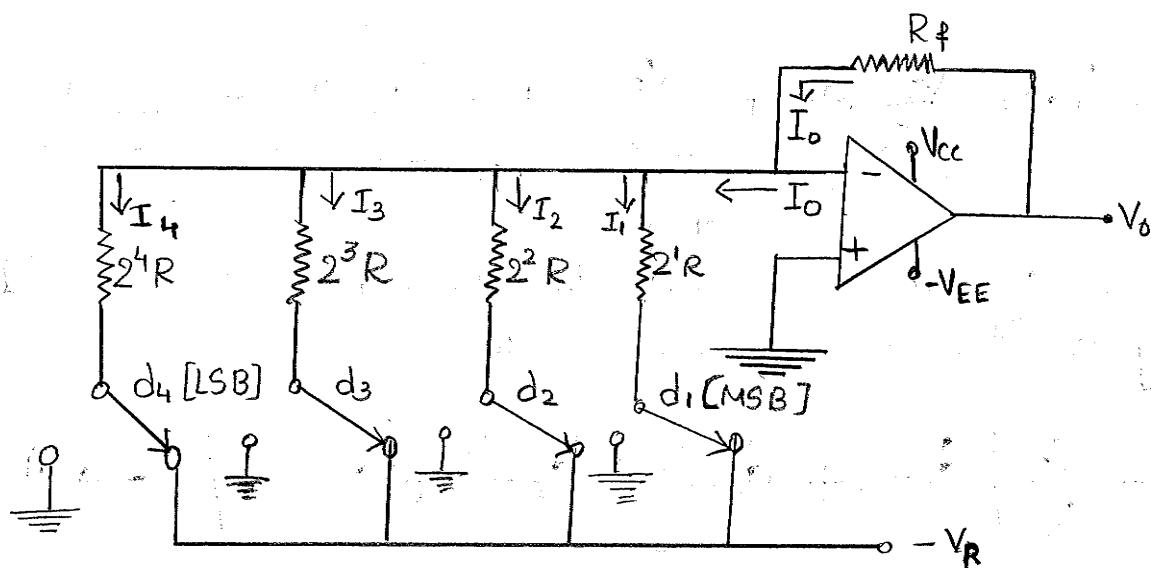


fig @

→ The DAC uses an summing op-amp with a binary weighted resistor $2^4 R$, $2^3 R$, $2^2 R$ & $2^1 R$ as shown in fig @.

→ It has 4 electronic switches d_1 , d_2 , d_3 & d_4 controlled by the binary TLP word. These switches are Single pole double throw [SPDT] type.

→ If the binary input to a particular switch is 1 it connects the resistance to the reference voltage ($-V_R$)

If the input bit is 0, the switch connects the resistor to the ground.



From fig @, the OIP current I_o for an [ideal] ideal op-amp can be written as

$$I_o = I_1 + I_2 + I_3 + I_4$$

$$I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3 + \frac{V_R}{2^4 R} d_4$$

Where d_1, d_2, d_3 and d_4 may be either 0 @ 1 depending on the binary input word.

$$I_o = \frac{V_R}{R} \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} \right] \rightarrow ①$$

→ The OIP voltage

$$V_o = I_o R_f \rightarrow ②$$

Sub eq ① in eq ② , we get

$$V_o = \frac{V_R}{R} R_f \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} \right]$$

Let $R_f = R$.

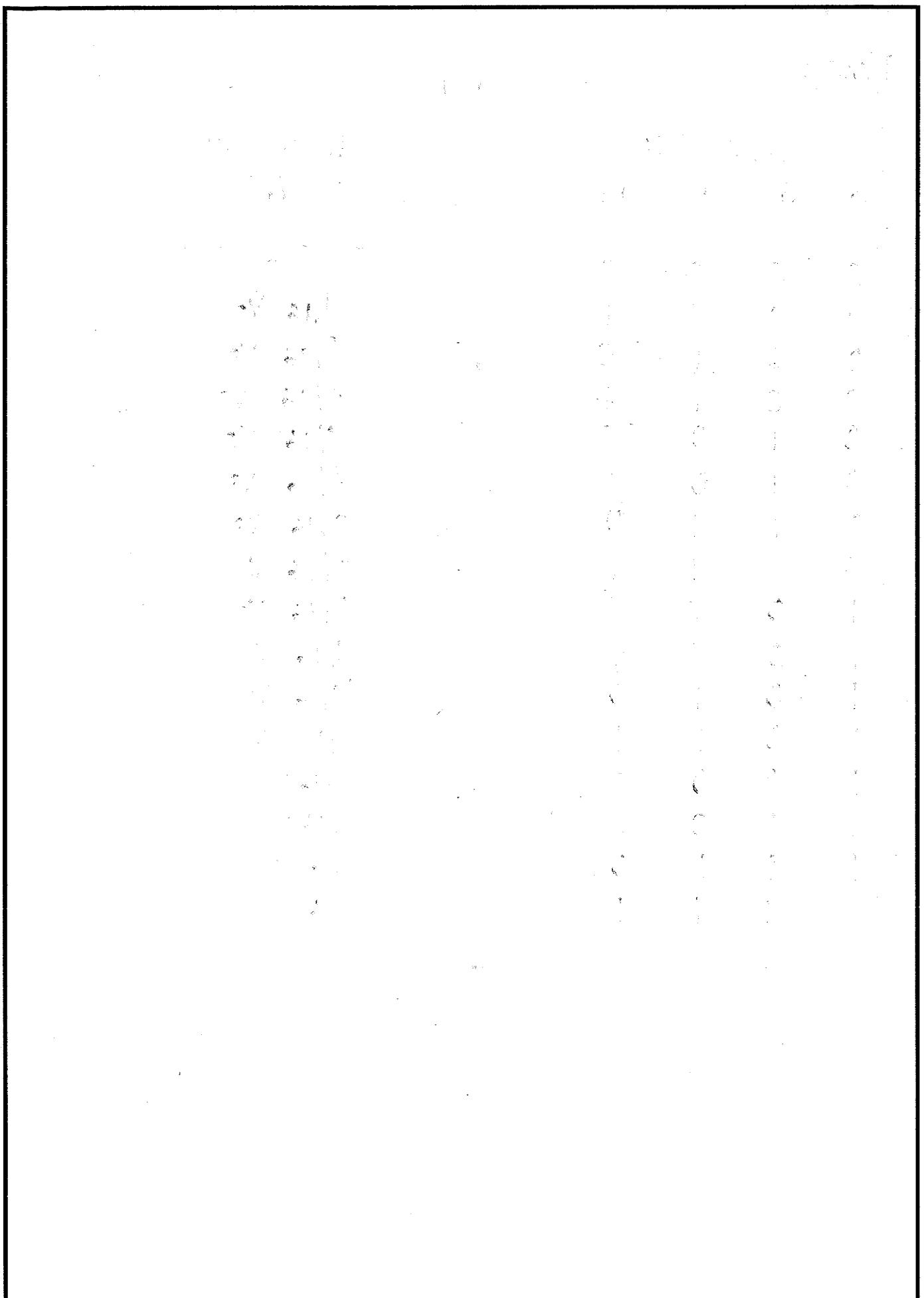
$$V_o = V_R \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} \right] \leftarrow ③$$



Note :

Digital IIP				Analog OIP
d_1	d_2	d_3	d_4	V_o
0	0	0	0	0
0	0	0	1	$1/16$ VR
0	0	1	0	$2/16$ VR
0	0	1	1	$3/16$ VR
0	1	0	0	$4/16$ VR
0	1	0	1	$5/16$ VR
0	1	1	0	$6/16$ VR
0	1	1	1	$7/16$ VR
1	0	0	0	$8/16$ VR
1	0	0	1	$9/16$ VR
1	0	1	0	$10/16$ VR
1	0	1	1	$11/16$ VR
1	1	0	0	$12/16$ VR
1	1	0	1	$13/16$ VR
1	1	1	0	$14/16$ VR
1	1	1	1	$15/16$ VR

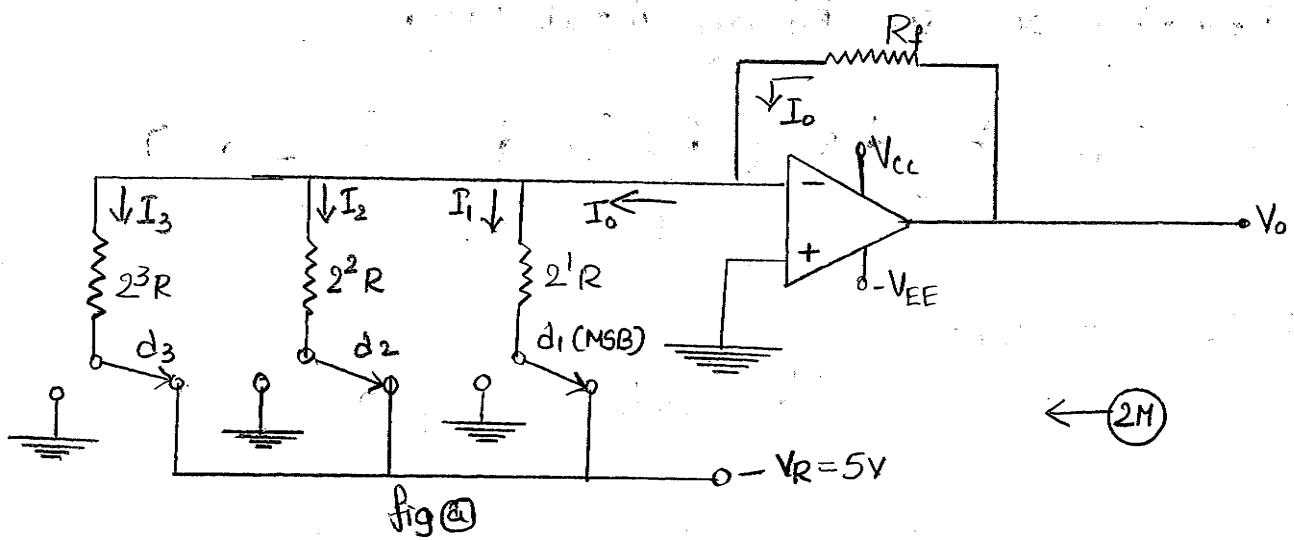




* 8-bit DAC with $V_{out(max)} = 5 \text{ volts}$.

Jan-09, 5m

Explain about 3-bit DAC and Substitute $V_R=5V$.



* The DAC uses an summing op-amp with a binary weighted resistor $2^1 R$, $2^2 R$ & $2^3 R$ as shown in fig @.

* It has 3 electronic switches d_1 , d_2 & d_3 controlled by the binary IIP word. These switches are single pole double throw [Spot] type.

* If the binary input to a particular switch is 1, it connects the resistance to the reference Voltage ($-V_R$).

* If the binary input bit is 0, the Switch connects the resistor to the ground.

From fig @, the O/P Current I_o for an ideal op-amp can be written as,

$$I_o = I_1 + I_2 + I_3$$



$$I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3$$

Where d_1 , d_2 & d_3 may be either 0 or 1 depending on the binary input word.

$$I_o = \frac{V_R}{R} [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}] \rightarrow ①$$

* The OP Voltage,

$$V_o = I_o R_f \rightarrow ②$$

Sub Eq ① in Eq ②, we get

$$V_o = V_R \left(\frac{R_f}{R} \right) [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$$

$$\text{Let } R_f = R$$

$$V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$$

← ②m



R-2R Ladder DAC :

* With a sketch, explain the Working of R-2R ladder DAC.

June-10, 8m

* R-2R ladder DAC

June-09, 5m

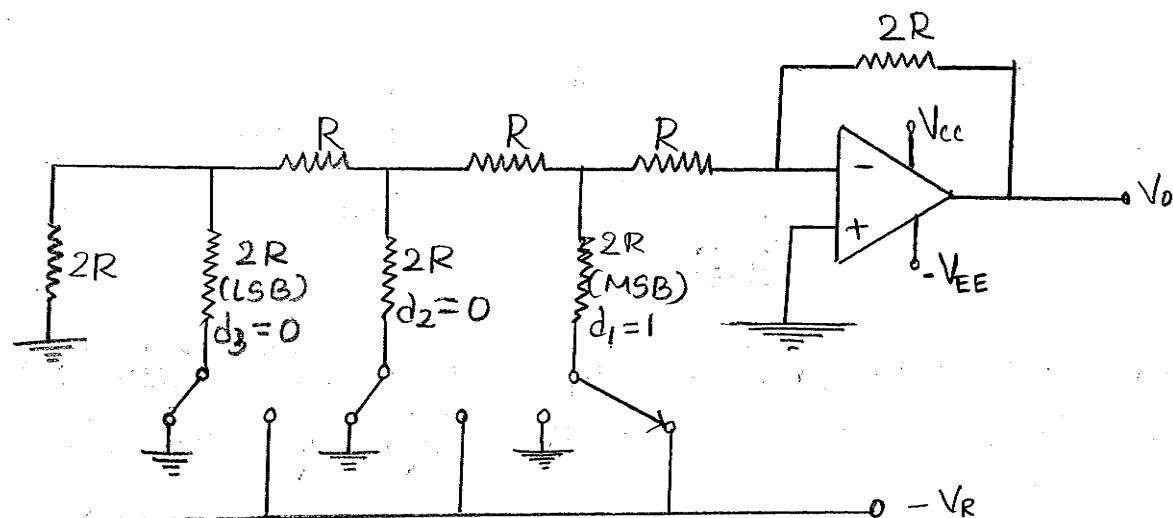


fig @ : R-2R ladder DAC

* R-2R ladder DAC uses only two values of resistor and hence it is easy to fabricate all resistors on a chip [IC].

The typical value of R ranges from $2.25\text{ k}\Omega$ to $10\text{ k}\Omega$.

* The resistors [R-2R] are so arranged as to form a ladder network as shown in fig @.

For simplicity, Consider a 3-bit DAC as shown in fig @. Let the digital input be a 3-bit binary word given as $D = 100$.



$$\therefore d_1 = 1, d_2 = 0 \text{ and } d_3 = 0$$

The switch positions are as shown in fig⑥ and the circuit is redrawn below.

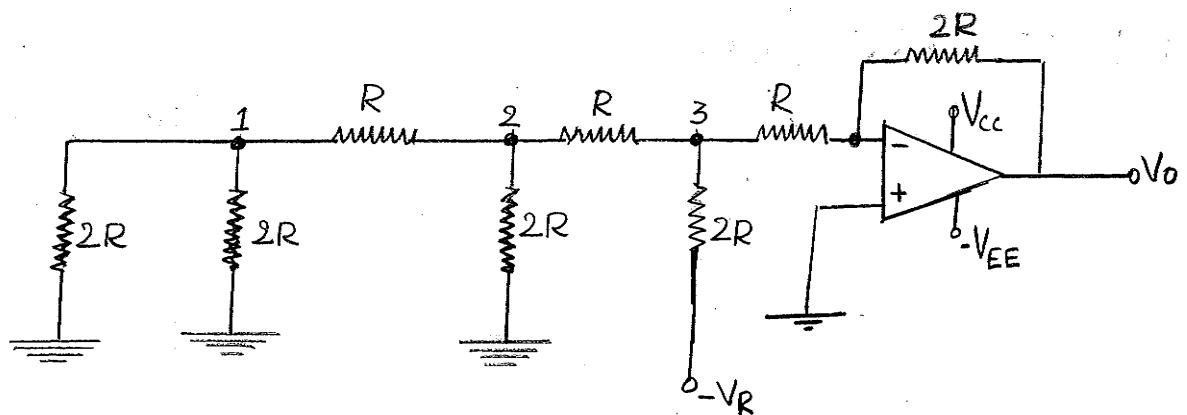
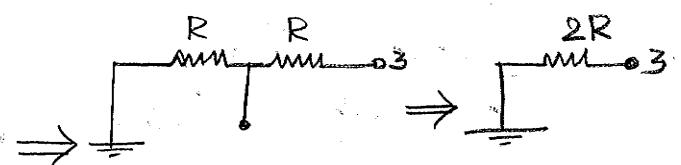
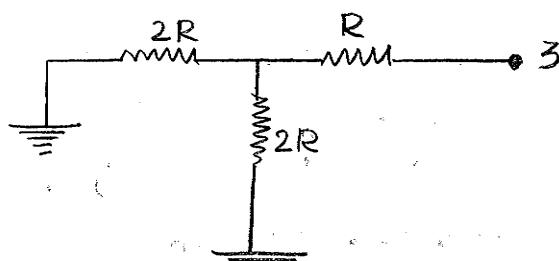
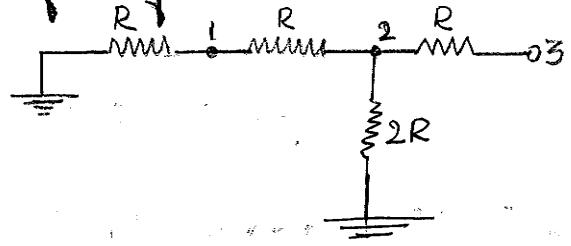
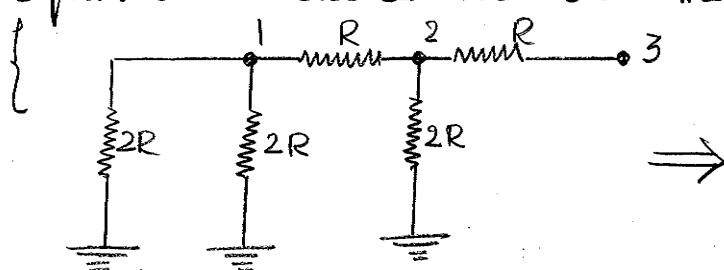


fig ⑥

* To calculate Voltage at node 3(V_3), Calculate the equivalent resistance to the left of node 3.



i.e., i] $2R \parallel 2R = R$

ii] $R + R = 2R$

iii] $2R \parallel 2R = R$

iv] $R + R = 2R$



∴ Equivalent resistance to the left of node 3 is $2R$.

The modified ckt is as shown in fig C.

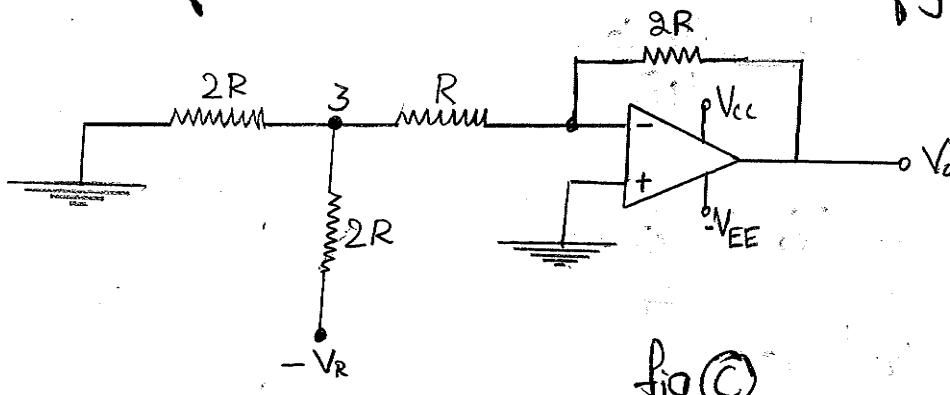


fig C

* The Voltage at node 3 is given by

$$V_3 = IR$$

$$= \frac{-V_R R}{2R+2R}$$

$$= \frac{-V_R R}{4R}$$

$$= -\frac{V_R}{4}$$

$$\boxed{V_3 = -\frac{V_R}{4}}$$

* Fig C is redrawn as below.

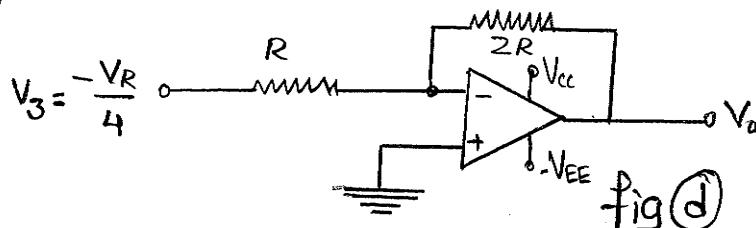


fig D

* Fig D is INV amplifier and its O/P Voltage is given by



$$V_o = - \left(\frac{2R}{R} \right) \left(\frac{-V_R}{4} \right) \quad \left\{ \therefore V_o = - \left(\frac{R_f}{R_i} \right) V_i \right\}$$

$$V_o = \frac{2RV_R}{4R}$$

$$\boxed{V_o = \frac{V_R}{2}}$$

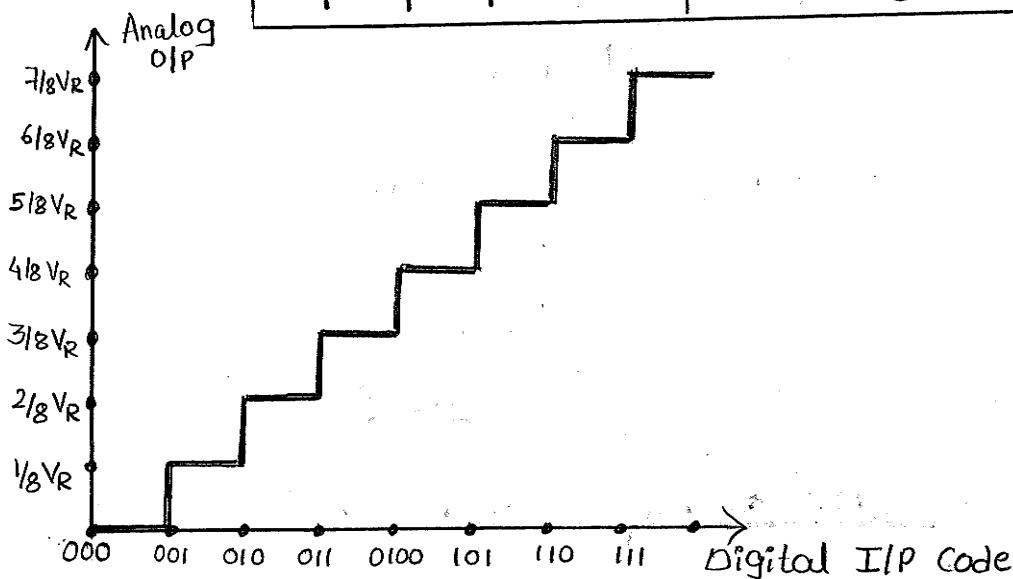
Since, $V_R = V_{FS}$

$$\therefore \boxed{V_o = \frac{V_{FS}}{2}}$$

$[V_{FS} = \text{full scale OIP } V_{tg}]$

* In general,

Digital I/P			Analog O/P V_o
d_1	d_2	d_3	
0	0	0	0
0	0	1	$\frac{1}{8}V_R$
0	1	0	$\frac{2}{8}V_R$
0	1	1	$\frac{3}{8}V_R$
1	0	0	$\frac{4}{8}V_R$
1	0	1	$\frac{5}{8}V_R$
1	1	0	$\frac{6}{8}V_R$
1	1	1	$\frac{7}{8}V_R$



Performance parameters of DAC :

The various performance parameters of DAC are :

1) Resolution

2) Accuracy

3) Monotonicity

4) Conversion time

5) Settling time

6) Stability

1) Resolution :

Resolution is defined in two ways :

i] Resolution is the number of different analog O/P values that can be ~~performed~~ provided by a DAC for an n-bit DAC.

$$\boxed{\text{Resolution} = 2^n}$$

ii] Resolution is also defined as the ratio of a change in O/P voltage resulting from a change of 1LSB at the digital inputs.

$$\boxed{\text{Resolution} = \frac{V_{OFS}}{2^n - 1}}$$

2) Accuracy :

It is a comparison of actual O/P Voltage with expected O/P. It is expressed in percentage.

Ideally, the accuracy of DAC should be at



Wort, $\pm \frac{1}{2}$ of its LSB.

$$\text{Accuracy} = \frac{V_{OFS}}{(2^n-1)^2}$$

3] Monotonicity :

A converter is said to have good monotonicity if it does not miss any step backward when stepped through its entire range by a counter.

4] Conversion time :

It is a time required for conversion of analog signal into its digital equivalent or vice versa. It is also called settling time.

5] Settling time :

This is the time required for the OIP of the DAC to settle to within $\pm \frac{1}{2}$ LSB of the final value for a given digital IIP [i.e zero to full scale.]

6] Stability :

The performance of converter changes with temperature, age and power supply variation. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.



FORMULAE

* Resolution of DAC

$$\text{i)} \text{Resolution} = 2^n$$

Where n is the number of bits in DAC

$$\text{ii)} \text{Resolution} = \frac{V_{OFS}}{2^n - 1} \times V_{LSB}$$

Where V_{OFS} = Full Scale OIP Voltage.

* OIP Voltage V_o = Resolution $\times D$

For ex:

$$D = (1000)_2 = 8$$

$$D = (0100)_2 = 4$$

* $V_{OFS} = \text{Step Size} \times (2^n - 1)$

Where n is the no. of bits in DAC

* For 8-bit DAC

$$* \text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

$$* \text{MSB} = \frac{1}{2^1} = \frac{1}{2}$$

* For 4-bit DAC

$$\text{LSB} = \frac{\text{Voltage range}}{2^4} = \frac{\text{Voltage range}}{16}$$



$$\text{MSB} = \frac{\text{Voltage Range}}{2^1} = \frac{\text{Voltage Range}}{2}$$

* Full Scale OLP = [Full Scale Voltage - LSB]

* For n-bit DAC, OLP Voltage is given by

$$V_o = V_R \left[d_1 \cdot \frac{1}{2^1} + d_2 \cdot \frac{1}{2^2} + d_3 \cdot \frac{1}{2^3} + \dots + d_n \cdot \frac{1}{2^n} \right]$$



Problems

i) What O/P voltage would be produced by a D/A converter whose O/P range is 0 to 10V and whose input binary number is

- i) 10 [for a 2-bit DAC]
- ii) 0110 [for a 4-bit DAC]
- iii) 10111100 [for a 8-bit DAC]

$$\text{Sol} \Rightarrow V_R = 10V$$

i) $(10)_2$

$$V_o = V_R [d_1 2^{-1} + d_2 2^{-2}]$$

$$= 10 [1 \times 2^{-1} + 0 \times 2^{-2}]$$

$$V_o = 5V$$

ii) 0110

$$V_o = 10 [0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4}]$$

$$V_o = 3.75V$$

iii) 10111100

$$V_o = 10 [1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 1 \times 2^{-5} + 1 \times 2^{-6} + 0 \times 2^{-7} + 0 \times 2^{-8}]$$

$$V_o = 7.34V$$



2) Calculate the values of the LSB, MSB and full scale OIP for an 8-bit DAC for the 0 to 10V range.

Sol:

* LSB for 10V range.

$$LSB = \frac{10V}{2^8}$$

$$\boxed{LSB = 39mV}$$

* MSB for 10V range

$$MSB = \frac{10V}{2^1}$$

$$\boxed{MSB = 5V}$$

* Full Scale OIP = [Full Scale Voltage - LSB]
 $= [10V - 39mV]$

$$\boxed{\text{Full Scale OIP} = 9.961V}$$

3) An 8-bit DAC has an OIP Voltage range of 0-255V. Define its resolution in two ways.

Sol:

i] Resolution = $2^n = 2^8 = 256$

ii] Resolution = $\frac{V_{OFS}}{2^n - 1} = \frac{2.55}{2^8 - 1}$



$$\text{Resolution} = \frac{2.55}{2^8 - 1}$$

$$\boxed{\text{Resolution} = 10\text{mV/LSB}}$$

4) The digital IP for a 4-bit DAC is 0110. Calculate its final OP voltage. Given, $V_{OFS} = 15\text{V}$.

Sol3 Resolution = $\frac{V_{OFS}}{2^n - 1} = \frac{15\text{V}}{2^4 - 1}$

$$\boxed{\text{Resolution} = 1\text{V/LSB}}$$

* $V_o = \text{Resolution} \times D$

$$D = (0110)_2 = [0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0]$$

$$\boxed{D = 6}$$

$$V_o = 1\text{V/LSB} \times 6$$

$$\boxed{V_o = 6\text{V}}$$

5) An 8-bit DAC has resolution of 20mV/LSB . Find V_{OFS} and V_o if the input is $(10000000)_2$

Sol3 Resolution = $\frac{V_{OFS}}{2^n - 1}$



$$20mV = \frac{V_{OFS}}{2^8 - 1}$$

$$V_{OFS} = 5.1 V$$

$$D = (10000000)_2 = 128$$

$$V_o = \text{Resolution} \times D = 20mV \times 128$$

$$V_o = 2.56 V$$

6) Find out stepsize and analog OIP for 4-bit R-2R ladder DAC when IIP is 1000 and 1111.
Assume $V_{ref} = +5V$

$$\text{Sol} \Rightarrow \text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{5V}{2^4 - 1}$$

$$\text{Resolution} = 0.33 V/\text{LSB}$$

$$* \text{ For } D = (1000)_2 = 8$$

$$\text{OIP } V_o = \text{Resolution} \times D = 0.33 \times 8$$

$$V_o = 2.6667 V$$

$$* \text{ For } D = (1111)_2 = 15$$

$$\text{OIP } V_o = \text{Resolution} \times D = 0.33 \times 15$$

$$V_o = 5V$$



7) A 12-bit DAC has a stepsize of 8mV. Determine the full scale OIP Voltage. Also find the OIP Voltage for the IIP of 010101101101

Sols

Given, $n = 12$

Step Size = 8mV

$$* V_{OFS} = \text{Step Size} \times (2^n - 1)$$

$$= 8\text{mV} \times (2^{12} - 1)$$

$$\boxed{V_{OFS} = 32.76 \text{ V}}$$

$$\{ D = (010101101101)_2 = (1389)_{10}$$

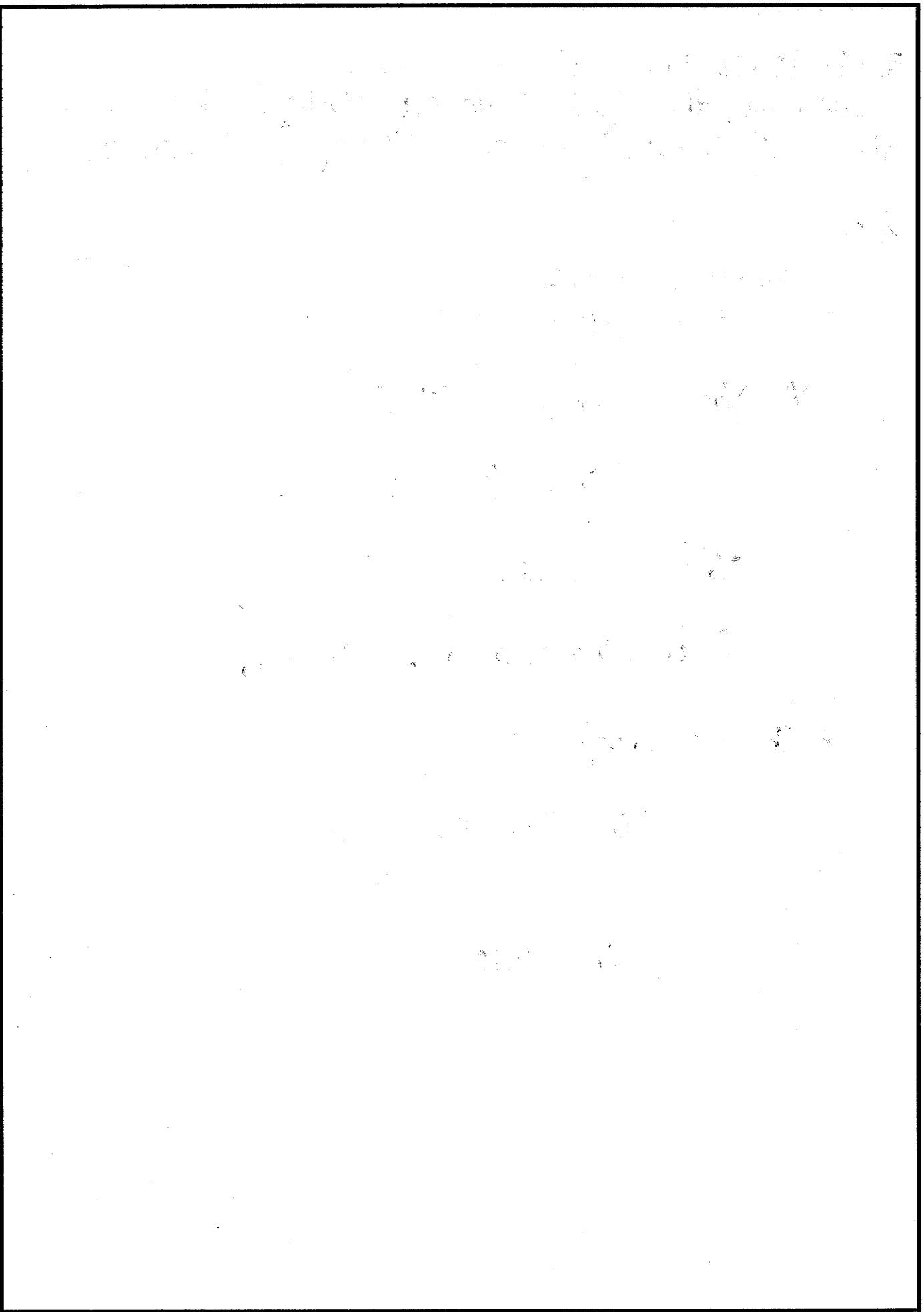
* The OIP Voltage,

$$V_o = \text{Resolution} \times D$$

$$= 8\text{mV} \times 1389$$

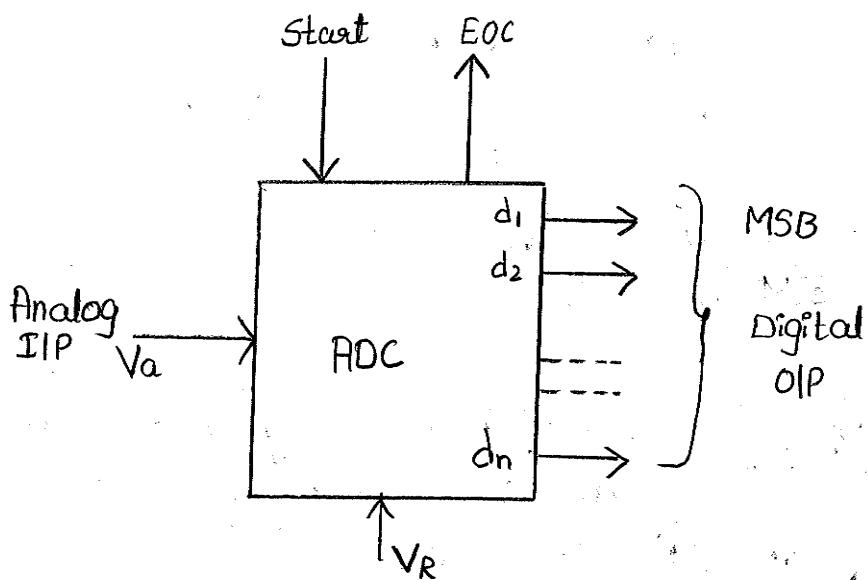
$$\boxed{V_o = 11.112 \text{ V}}$$





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Analog to digital Converters [ADC] :



fig① : Functional diagram of ADC.

Fig① Shows the block schematic of ADC. It accepts an analog input Voltage V_a and produces an o/p binary word d_1, d_2, \dots, d_n so that,

$$D = d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \dots + d_n 2^{-n}$$

Where d_1 is the most significant bit [MSB] and d_n is the least significant bit [LSB].

- * An ADC has two additional control lines :
- i] The START input to tell the ADC when to start the conversion and
- ii] The EOC [end of conversion] o/p announces when the conversion is complete.



Classification of ADC's :

* ADC's are classified broadly into two groups according to their conversion technique.

- 1) Direct type ADC's &
- 2) Integrating type ADC's.

* Direct type ADC's Compare a given analog signal with the internally generated equivalent signal. Some of the direct type ADC's are :

- 1] Flash type Converter
- 2] Parallel Comparator ADC.
- 2] Counter type Converter.
- 3] Tracking or servo converter.
- 4] Successive approximation type converter etc.

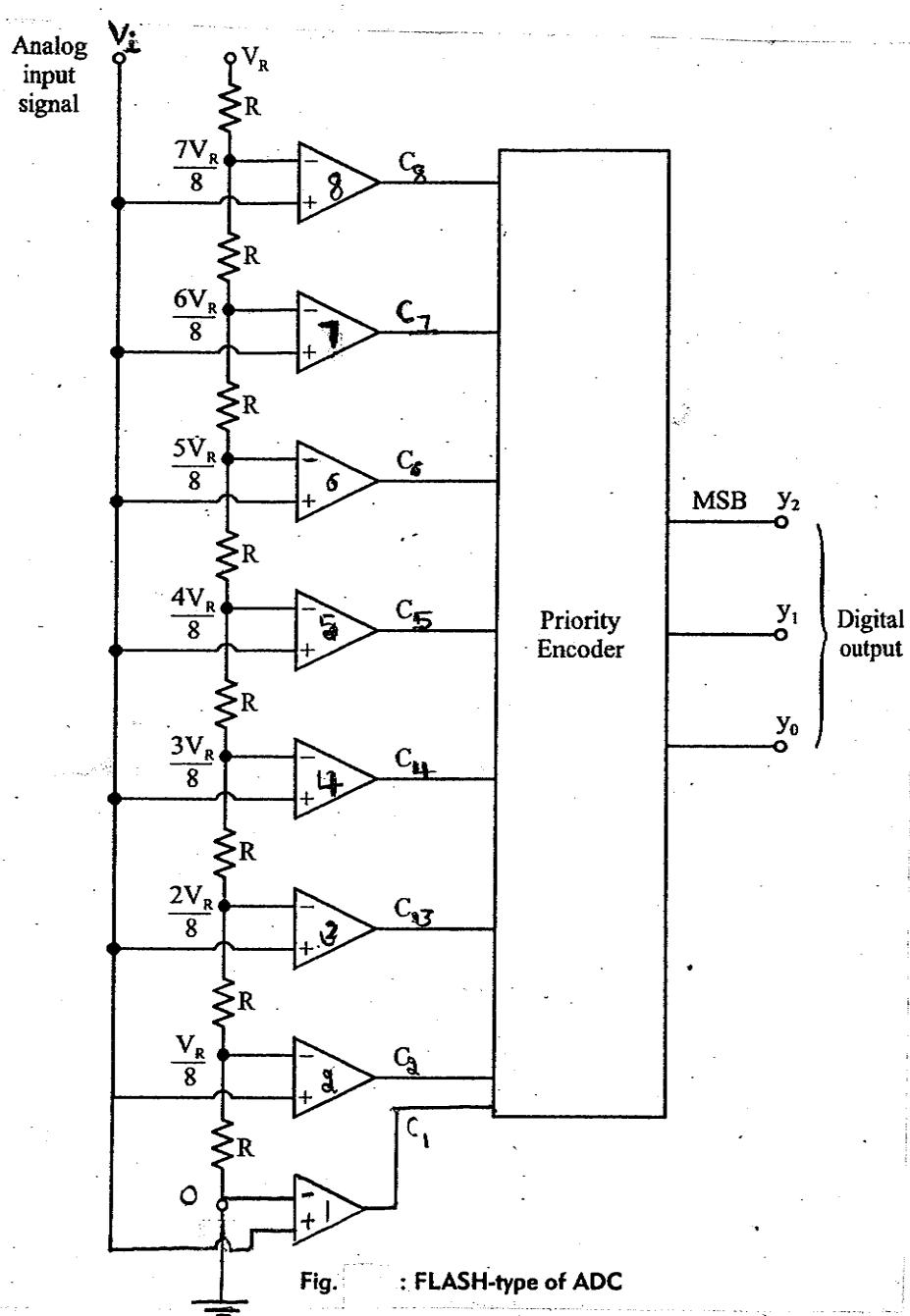
* Integrating type ADC's, the analog input signal is first converted into a linear function of frequency of time, and this is subsequently converted into a digital code.

The two most widely used integrating type converters are :

- 1) Charge balancing ADC
- 2) Dual Slope ADC.



Flash ADC or parallel Comparator ADC:



Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

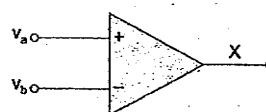


Fig. (b) Comparator and its truth table



Table | Digital output data according to analog input

Input voltage V_i	Outputs of comparators								Digital outputs		
	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	y_2	y_1	y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

→ Fig shows a 3-bit A/D Converter. The Ckt consists of a resistive divider network, 8 op-amp Comparator and a 8-line to 3-line encoder [3-bit priority encoder].

- * The analog input ' V_i ' & the INV Σp terminals are connected to various levels of the reference voltage V_R produced by the resistive divider network as shown in figure. The reference voltage V_R is equal to the full scale input Signal voltage.
- * All resistors are of equal magnitude, the voltage levels at the nodes are equally divided between the reference voltage V_R and the ground.



- * The main purpose of building the circuit in the fashion shown in figure is to compare the I/p analog circuit V_i with each of the node voltages.
- * The comparators give o/p of 1 or 0 depending upon whether the I/p Signal level is greater or less than the reference voltage level.
 - i.e. if $V_i > V_d$, then o/p $X = 1$
 - $V_i < V_d$, then o/p $X = 0$
 - $V_i = V_d$, then o/p $X = \text{previous value}$
- * The number of Comparators required for n-bit resolution is 2^n & Quantization error is $\pm \frac{1}{2} \text{ LSB}$.
- * The maximum frequency for a Sinusoidal I/p voltage to be digitized within an accuracy of $\pm \frac{1}{2} \text{ LSB}$ is

$$f_{\max} = \frac{1}{2\pi T_c 2^n}$$

Where

$T_c \rightarrow$ Conversion time &

$n \rightarrow$ number of bits.

Advantages :-

➢ Conversion is very fast (High Speed)

Disadvantages :-

➢ It requires a large number of Comparators i.e. number of Comparators required almost doubles for each added bit.
 ➢ Expensive



* If the conversion time of a 8-bit flash ADC is 10 μsec,
Find the maximum frequency of a Sinusoidal voltage that
can be digitized.

Given :-

$$n=8 \text{ and } T_c = 10 \mu\text{sec}$$

Sol :-

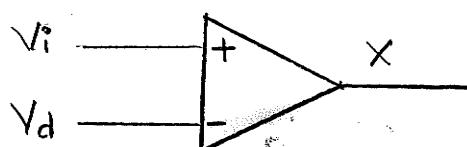
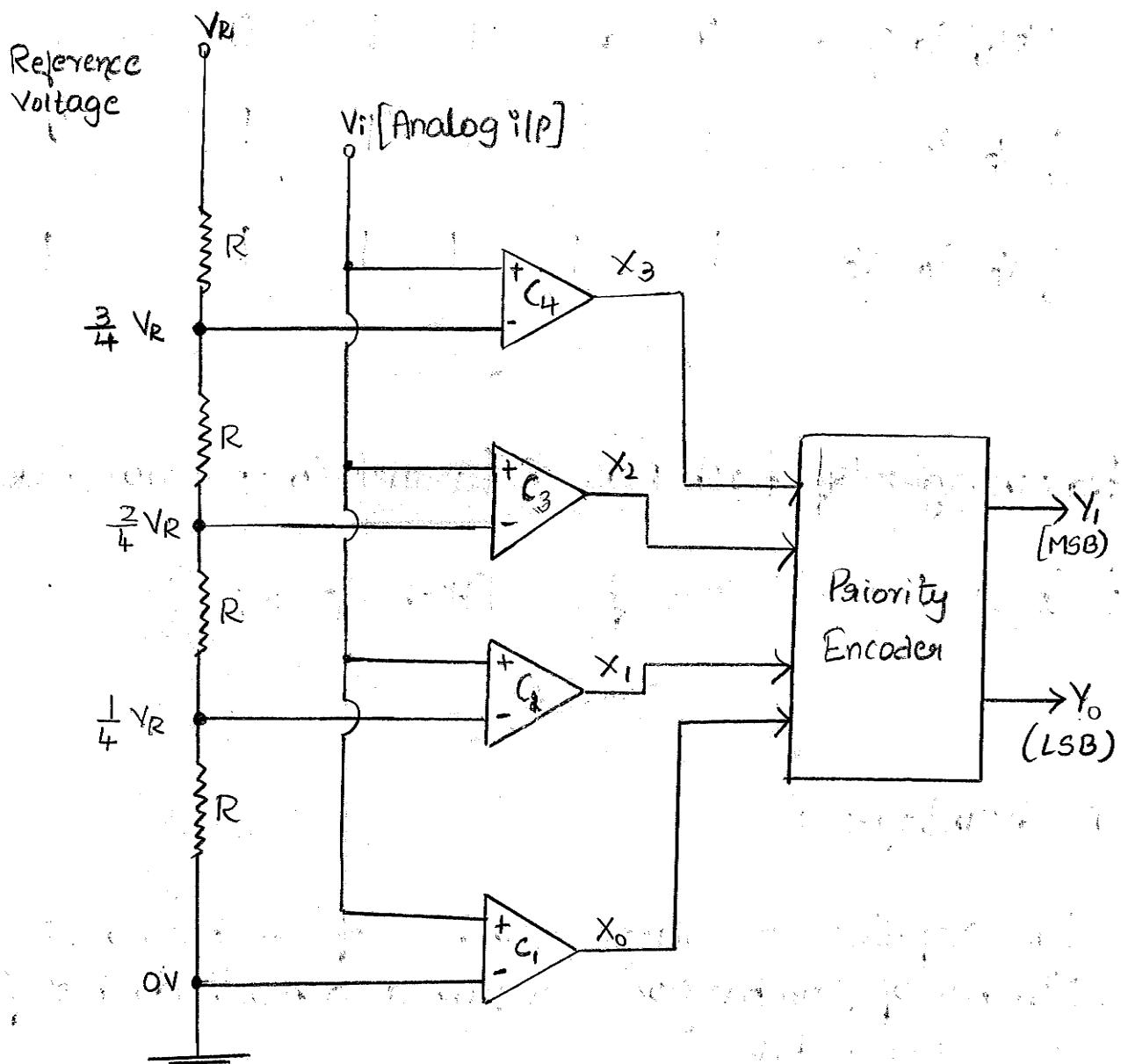
$$\text{WKT } f_{\max} = \frac{1}{2\pi T_c 2^n} = \frac{1}{2\pi \times (10 \times 10^{-6}) \times 2^8}$$

$$f_{\max} = 62.17 \text{ Hz}$$



* Design a 2-bit Flash ADC

Sol3 Number of Comparators = $2^n = 2^2 = 4$
Where $n=2$



I/P Voltage	O/P Logic 'X'
$V_i > V_d$	$X = 1$
$V_i < V_d$	$X = 0$
$V_i = V_d$	Previous Value



Analog Input Voltage (V _i)	O/P of Comparators				Digital O/P's	
	X ₃	X ₂	X ₁	X ₀	Y ₁	Y ₀
0 to V _R /4	0	0	0	1	0	0
V _R /4 to $\frac{2}{4}$ V _R	0	0	1	1	0	1
$\frac{2}{4}$ V _R to $\frac{3}{4}$ V _R	0	1	1	1	1	0
$\frac{3}{4}$ V _R to V _R	1	1	1	1	1	1

Advantages of flash ADC @ Parallel Comparator ADC:

1) Conversion is very fast [High Speed]

Disadvantages :

1) It requires a large number of comparators i.e.- Number of comparators required almost doubles for each added bit.

Ex : 1) For 3-bit ADC

No. of comparators is $2^n = 2^3 = 8$

2) For 4-bit ADC

No. of comparators is $2^n = 2^4 = 16$

2) Expensive.



Successive approximation ADC :

- * Explain the operation of a successive approximation ADC using a simplified block diagram. Jan-11, 6m

- * 4-bit ADC with $V_{in(max)} = 2$ Volts. Jan-09, 5m
[Explain any one ADC.]

- * What is the main disadvantage of Flash ADC? With the help of a neat diagram explain the operation of a successive approximation type ADC. June-08, 7m

- * A/D Converters. Jan-10, 5m

Sol:

Explain Disadvantage of Flash type ADC ← 1m

- A Successive Approximation A to D Converter is based on a very efficient code searching strategy called binary search.
- The searching process is very fast, a n-bit conversion being completed in only n-clock periods.

P.T.O



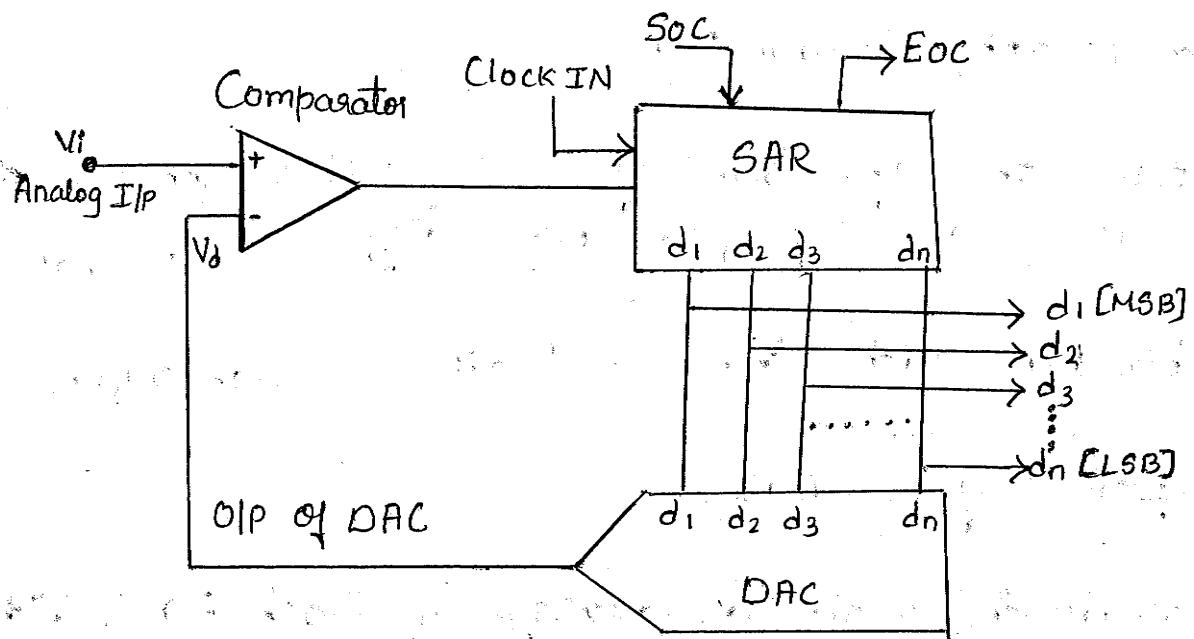


fig ①: Block diagram of Successive approximation ADC Converter

Fig ① Shows the block diagram of Successive approximation ADC.

It consists of

- DAC
- Comparator &
- Successive Approximation Register (SAR)

→ The external clock IIP sets the internal timing parameters. The SOC Signal Starts the process of Conversion and the activated EOC Signal announces the end of Conversion process.

Operation :

The SOC Signal initiates the process of signal search. The SAR sets the MSB $d_1 = 1$, as soon as the START Signal arrives, and all other bits are set to 0, of the converter is a 8-bit converter, the



initial setting would be 10000000.

The OIP VA of the DAC for this trial code is compared with the analog IIP Vi. If the analog IIP Vi is greater than the DAC OIP VA [i.e., $V_i > V_A$], it implies that the trial code 10000000 is less than the correct digital representation of Vi. The MSB d7 is left at 1 and the next lower significant bit is set at 1, and the process is repeated.

- On the other hand, if the IIP Vi is less than the DAC OIP VA, it implies that the trial code 10000000 is greater than the correct digital representation of Vi. In such an event, the MSB is set to '0' and the next lower significant bit is set to '1', and the process is repeated. [i.e. 01000000]
- The above process of comparison is repeated for all subsequent bits, one at a time, until all bit positions have been tested.
- The Comparator changes the state whenever the DAC OIP crosses Vi, and this activates the EOC command.

P.T.O



Correct digital Representation	SAR OIP VA at different Stages	Comparator OIP
10110010	10000000	1
	11000000	0
	10100000	1
	10110000	1
	10111000	0
	10110100	0
	10110010	1
	10110011	0

→ Comparator OIP after Comparing all 8-bits = 10110010 = Digital representation of analog IIP.

In practice, however, an additional pulse is needed to load the OIP register and reinitialize the Ckt.

→ The time required for one conversion from analog to digital depends on both the clock period 'T' and the number of bits 'n'.

$$T_c = T(n+1)$$

Where T_c denotes the conversion time.



* Dual Slope DAC (a) Integrator type DAC :

June-09, 5M

→ The dual Slope DAC is an integrator type A to D converter. Its accuracy is quite high, even though the speed of operation is quite low.

{ In dual Slope DAC, the analog input voltage and a reference voltage are both converted into time periods by means of an integrator, and are then measured by means of a counter.

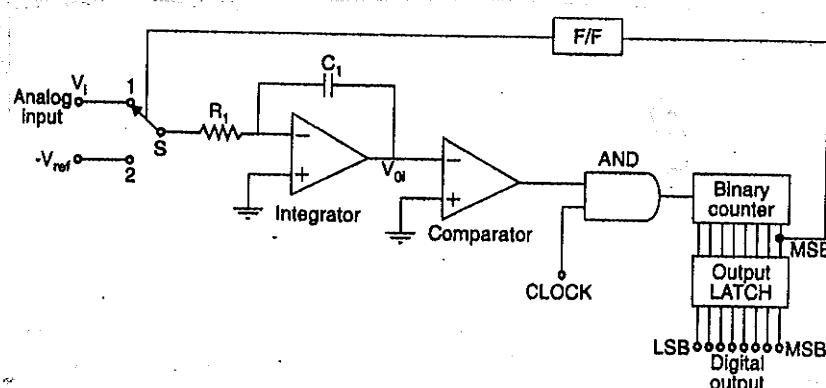


Fig 1(a)

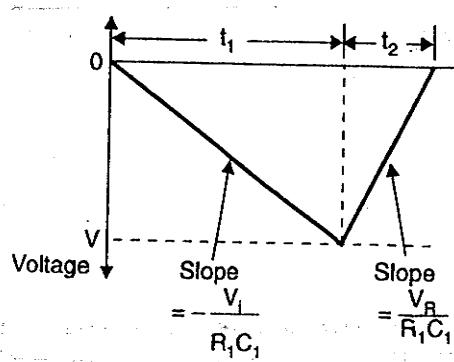


Fig 1(b)

Fig ① @ Shows the block diagram of Dual Slope DAC.



→ The integrator is a amp generator. There is a switch arrangement 'S' by which the integrator input can be switched between the analog input Voltage V_i and a negative reference Voltage $-V_{ref}$. The switch is controlled by the MSB of the binary Counter.

→ When the MSB is a logic 0, the Switch closes on terminal 1 at which the input Voltage is applied.

→ When the MSB is a logic 1, the Switch closes on terminal 2 at which the input Voltage is applied.

→ Operation:

→ Let the Switch close on terminal 1 at $t=0$. The analog input Voltage V_i gets applied at the INV terminal of the integrator.

The Integrator O/P Voltage is given as

$$V_{oi} = \frac{-i}{R_i C_i} \int_0^{t_i} V_i dt = -\frac{1}{RC} V_i \int_0^{t_i} 1 \cdot dt$$

$$\boxed{V_{oi} = -\frac{V_i t_i}{R_i C_i}}$$

→ The integrator O/P Voltage is applied to the Comparator. The Comparator O/P goes high. It enables the AND gate and the clock pulses reach the Counter.

→ At the end of 2^n clock periods, the MSB of the



Counter goes high. This causes the O/P of the flip-flop to go high with the result that the analog switch 'S' Switches from position 1 to position 2, and connects the reference Voltage to the integrator INV terminal.

Simultaneously the binary counter gets reset. The negative reference voltage $-V_R$ which now forms the I/P to the integrator makes the O/P of the integrator increases as a positive linear ramp.

When it reaches Zero level, the comparator O/P goes low, and this disables the AND gates, and the result of it is the clock pulses cease to reach the counter.

The Counter stops at a count corresponding a time interval t_2 .

→ Charge Voltage = Discharge Voltage.

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$t_2 = \frac{V_i}{V_R} t_1$$

In above equation V_R & t_1 are fixed. Hence

$$t_2 \propto V_i$$

i.e. t_2 is directly proportional to the analog input voltage and hence is a measure of it. The O/P



of the counter is also proportional to the analog I/P.

$$\therefore \text{Digital O/P of the Counter} = [\text{Counts/sec}] \times \frac{V_i}{V_R}$$

Advantages:

- 1) It possesses a high degree of accuracy.
- 2) It is cheap and reliable.
- 3] Its performance is not adversely affected by change of temperature.



Problems :

- 1) The reference voltage for a dual slope ADC is 100mV of $t_1 = 50\text{ms}$, find t_2 if the input voltage is 150mV.

Sol 2) Given,

$$V_R = 100\text{mV}$$

$$t_1 = 50\text{msec}$$

$$V_i = 150\text{mV}$$

$$t_2 = ?$$

$$\text{W.K.T, } t_2 = t_1 \cdot \frac{V_i}{V_R}$$

$$= \frac{50\text{msec} \times 150\text{mV}}{100\text{mV}}$$

$$t_2 = 75\text{msec}$$

- 2) For a dual slope ADC, $V_R = 100\text{mV}$, $t_1 = 50\text{msec}$ and the clock frequency is 12KHz. Find the digital output for an input voltage of 200mV.

Sol 3) Given, $V_R = 100\text{mV}$, $V_i = 200\text{mV}$, $t_1 = 50\text{msec}$

Given clock frequency = 12KHz

$$= 12000 \text{ counts/sec}$$



$$\text{WKT, Digital O/P} = (\text{Counter/sec}) \cdot \frac{t_i V_i}{V_R}$$

$$= \frac{12000 \times 50 \times 10^{-3} \times 200 \times 10^3}{100 \text{mV}}$$

$$\boxed{\text{Digital O/P} = 1200 \text{ Counts.}}$$

3) An 8-bit ADC O/P's all 1's when $V_i = 2.55 \text{V}$, find its,

- Resolution in mV/LSB and
- Digital O/P when $V_i = 1.28 \text{V}$

June-10, 6m

$$\text{Soln, i] Resolution} = 2^n = 2^8 = 256$$

$$\text{Resolution} = \frac{V_{ops}}{2^n - 1} = \frac{2.55 \text{V}}{2^8 - 1}$$

$$\boxed{\text{Resolution} = 10 \text{mV/LSB}}$$

← 3m

$$\text{ii] Digital O/P} = \frac{1.28 \text{V}}{10 \text{mV/LSB}}$$

$$\boxed{\text{Digital O/P} = 128 \text{ LSB}}$$

Digital O/P Code = Binary Equivalent of LSB = 128LSB

$$= \underline{\underline{10000000}}$$

← 3m

