Logic States:-

→ Binary login (0, 1)

→ three valued logic (0, 1, x) x = undefined

→ (Tenary logic)

→ Four valued logic (0, 1, x, z)

x - floating node without conducting path to V_{DD} (or) GND

z - high impedance

Truth Table

Eg: AND gate

A \ i/p →	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

→ outputs

Truth:- OR gate

AB	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

Not - gate

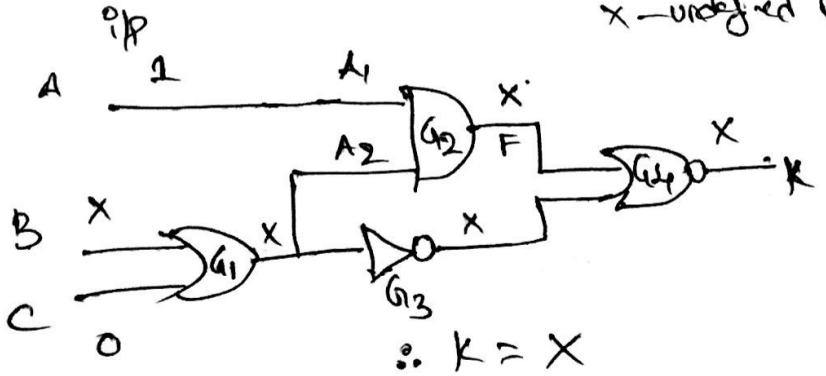
i/p →	0	1	X	Z
	1	0	X	

Note:-

More States ; More Accuracy ; More CPU time.

(a) Ternary logic simulation

X - undefined (0/1) → (not accurate.)



∴ K = X

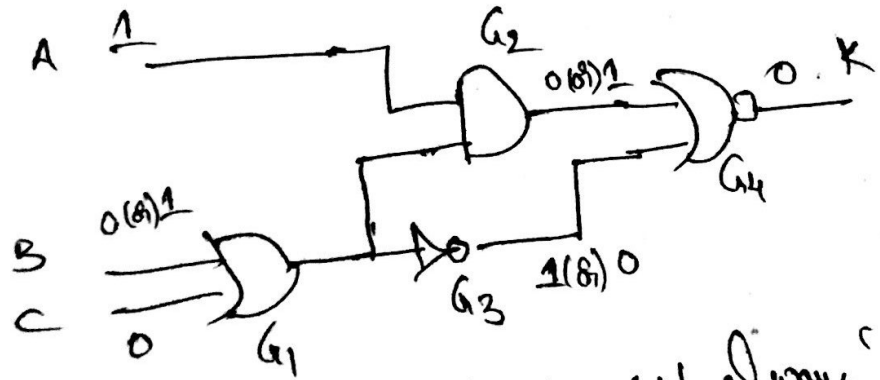
ABC - Primary i/p's (PI)

A_1, A_2 - Gate i/p for G_2

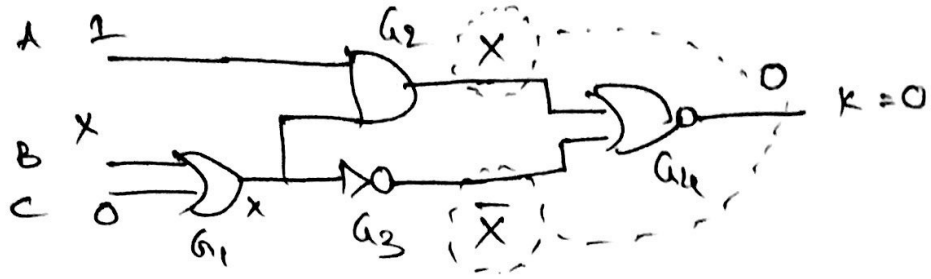
K - Primary o/p (PO)

F - Gate o/p for G_2

(b). Enumerate all possible case (B=0 & 1) ∴ K=0

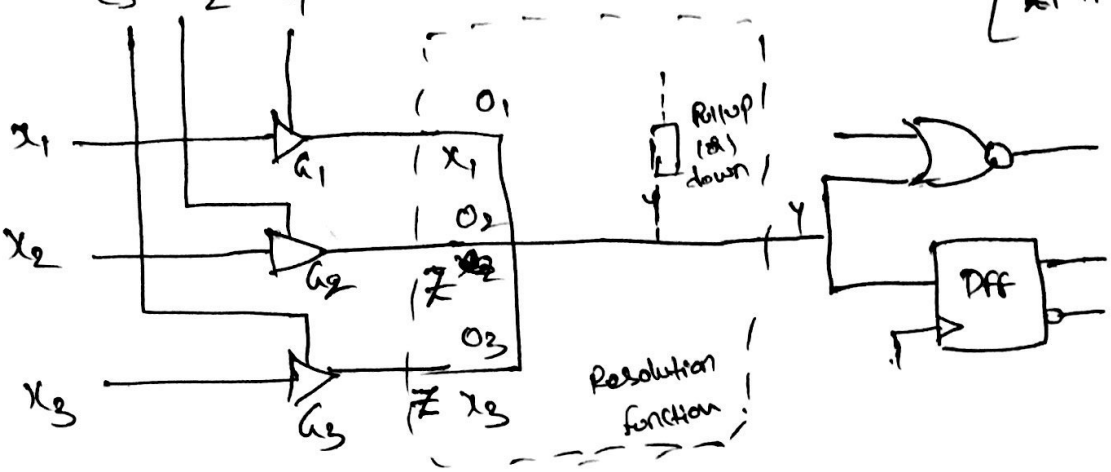


the o/p is said always '0' this is case of fanout case.



High Impedance state - Z

$O_i = \begin{cases} x_i \text{ if } e_i = 1 \\ Z \text{ if } e_i = 0 \end{cases}$



Tristate bus driver.

Eg: $e_3 = 0$; $e_2 = 1$; $e_1 = 1$ from above ckt what is o/p $Y = ?$

$\therefore Y = X$ (undefined)

Input Scanning :-

→ is to check gate one by one

→ Determines gate output by numbers of C (Controlling value) ; i - (inversion value) ; X - (undefined).

→ Controlling value (c) :-
C = i/p value that decide gate o/p

→ inversion (i) :-
i = 1 gate o/p is inverted w.r.t gate i/p
i = 0 ; otherwise

Testing other conditions determined :
AND i/p → 0
OR i/p → 1

	C	i
AND	0	0
OR	1	0
NAND	0	1
NOR	1	1