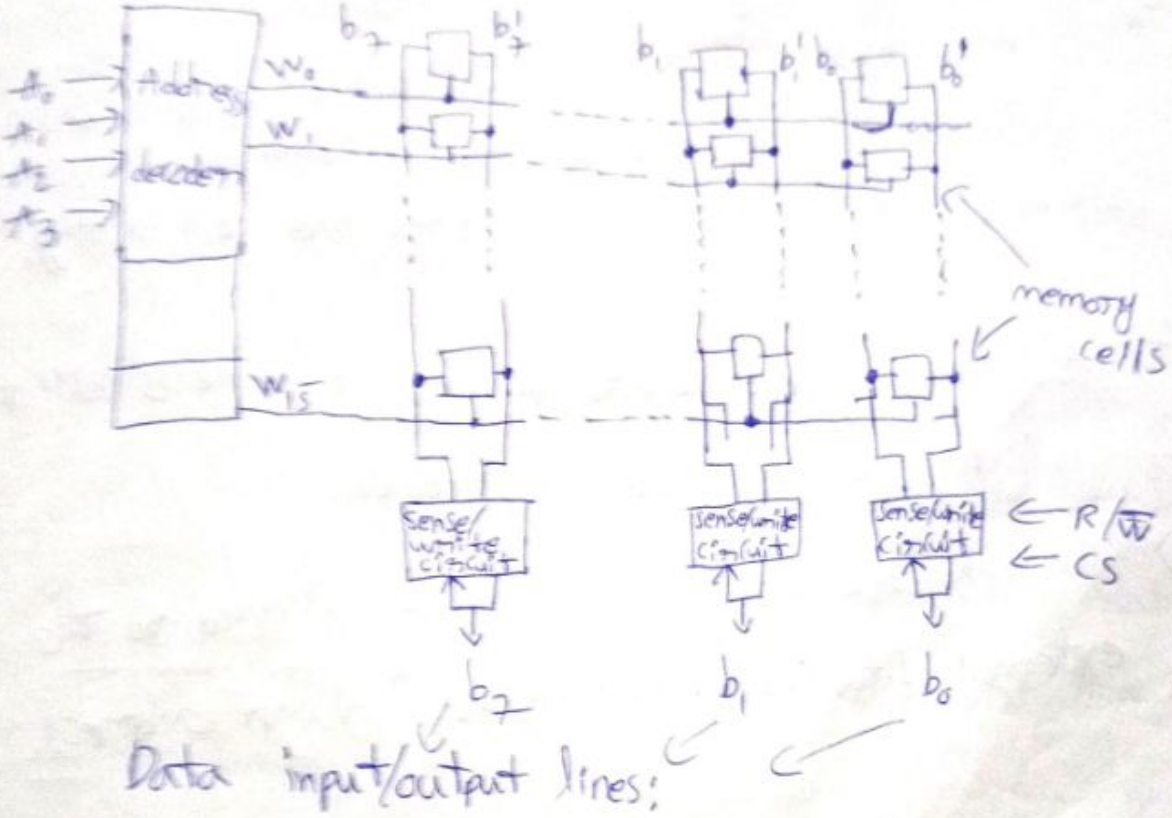
System I/O Controllers SATA Ethernet

Internal organization of memory chips:-

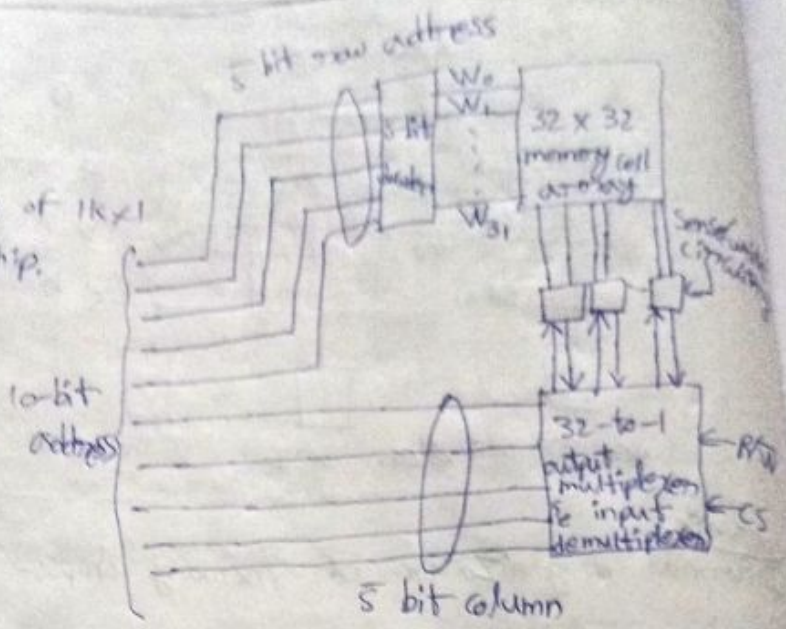


organization of bit cells in a memory chip.

word line - An array of rows of memory cells in random access

memory is used with bitline to generate the address of

=) Semiconductor RAM memories-5



→ Organization of 1k x 1 memory chip.

→ 10 bit address → 5 bits from row addresses
→ 5 bits from column

for the cell array.

→ A row address selects a row of 32 cells, all of which are accessed in parallel.

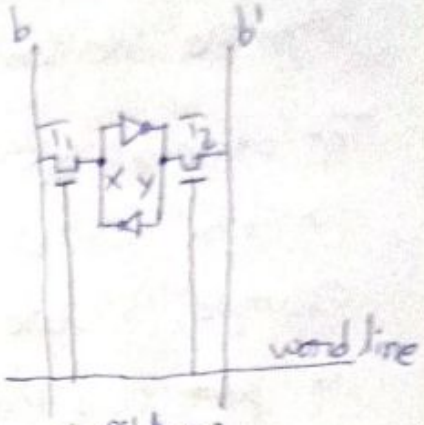
→ But, only one of these cells is connected to the external data line, based on the column address.

UNIT - IV The memory System

=) Semiconductor RAM memories -

Static memories (SRAM)

=) Read operation



Assume cell is in State 1.

to read keep word line to 1.

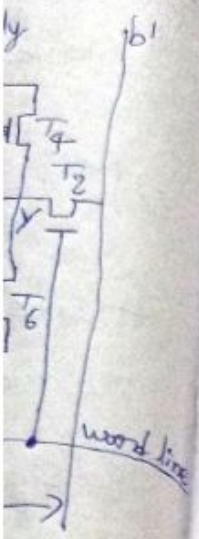
so signal on bit line b is high & the signal on bit line b' is low.

↑ Static RAM Cell.

=) write operation

During a write operation, the sense/write circuit drives bit lines b & b'.

It places the appropriate value on bit line b & it's complement on b' & activates the word line. This forces the cell into the corresponding state, which the cell retains when the word line is deactivated.



→ During a read/write, the wordline goes high & the transistor connects the capacitor to the bitline. whatever value is on bitline gets stored/ retrieved from the capacitor.

⇒ Dynamic RAM:-

→ Stores bit data in capacitor.

→ Capacitor leaks, unless it refreshed periodically.

→ Due to refresh requirement, It is dynamic memory

→ data lost when power off.

Advantages over SRAM / Structural Simplicity, 1 Transistor, 1 capacitor

→ slower than RAM, cheaper & smaller in size.

⇒ Asynchronous DRAM:-

Classic DRAM — Asynchronous interface,

→ Responds as quickly as possible to changes in control inputs.

→ Stores in capacitor for only 10ms.

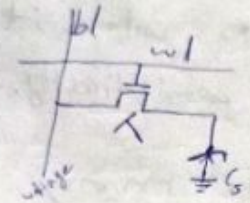
→ If Storing for long time, periodically refresh it.

sense Amplifier to find voltage in capa
1. Activates word line → Turns on Transis
2. Voltage on bit line → through Transistor
→ Info stored as in dynamic memory
cell in form of a charge on a capacitor & contents must be periodically refreshed by restoring the capacitor charge to it's full value.

charge stor
capacitor.

Read oper
2 Steps
Refresh sens
cell

Value = 1 { if V > Th value capaci
A full voltage through Bitline to store in capacitor.



Value = 0 { if V < Th value
zero, voltage ↓ down through the Bit line.

=) Read only memory:-

Different types of non volatile memories have been developed. ↓ no data (memory) loss when power off.

→ ROM, PROM, EPROM, EEPROM.

ROM → → Read only memory. This type of memory is non-volatile. The information is stored permanently in such memories during manufacture. → can't modify data.

PROM → programmability is achieved by inserting a fuse at point P in the diagram. Before, it is programmed, the memory contains all os.

- A ROM stores such instructions that are required to start a computer.

Bit line

EEPROM

from

info

Conte

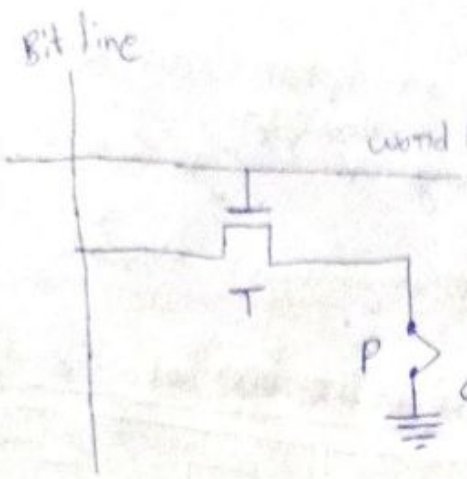
UH

Can

el

EPRO

m

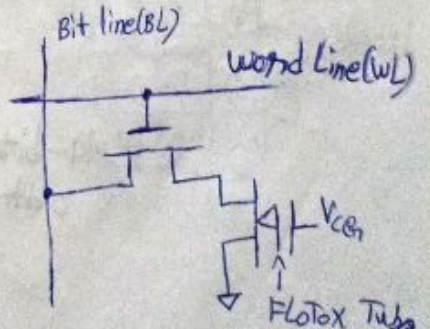


Flash cards
Flash memory

A Rom cell.

EEPROM:- Electrically Erasable programmable read only memory

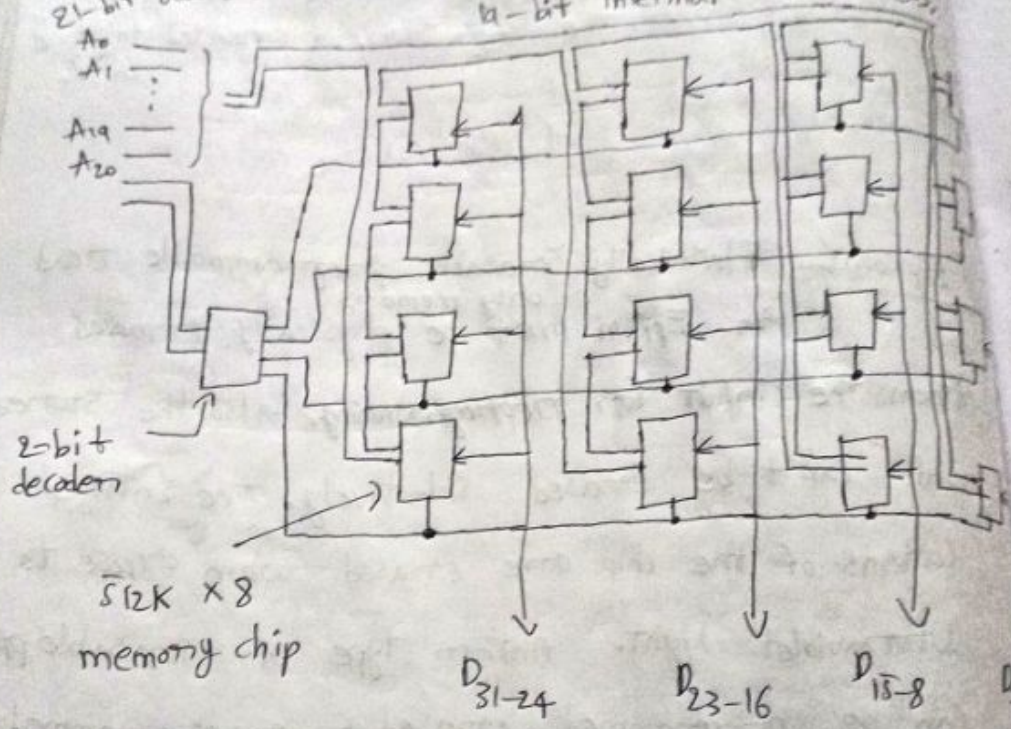
An EPROM must be physically removed from the circuit for reprogramming. Also, the stored info can't be erased selectively. The entire contents of the chip are erased when expose to Ultraviolet light. Another type of erasable PROM can be programmed, erased, & reprogrammed electrically. Such a chip is called an electrically erasable PROM / EEPROM.

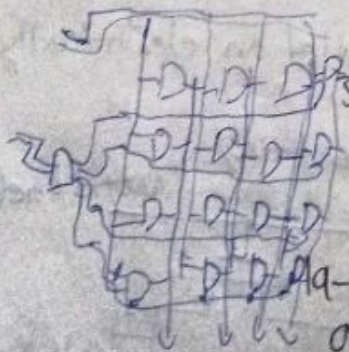


EPROM:-

An EPROM, (or) erasable programmable read-only memory, is a type of programmable read-only memory (PROM) chip that retains it's data when it's power supply is switched off.

once programmed, an Eprom can be erased by exposing it to strong ultraviolet light source (such as UV from a mercury-vapour lamp).





⇒ Structure of larger memories

organization of a 2M × 32 memory module using 512K × 8 static memory chips.

⇒ Flash memory

Storage device

memory to

Computing dev

Video.

⇒ Flash mem

Storage d

Can Keep

Power is

reprog

EEPRO

⇒ Synch

ope

=) Flash memory card -

A flash memory card is a small storage device that uses non-volatile semiconductor memory to store data on portable/remote computing devices. It includes text, pictures, audio & video.

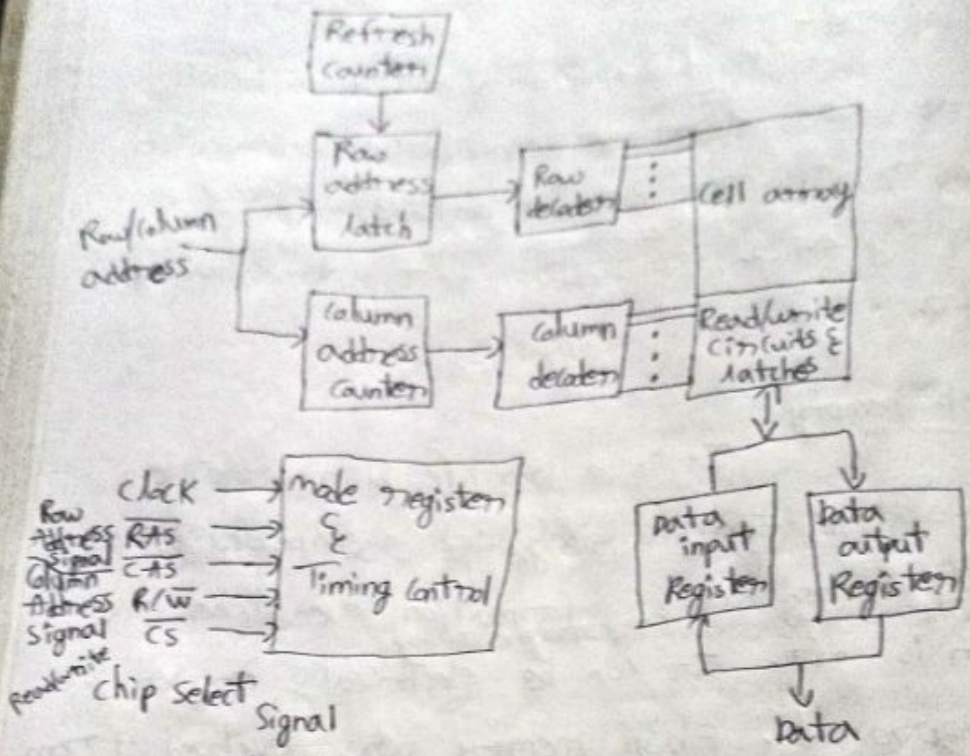
=) Flash memory -

It is a long-life & non-volatile storage chip that is widely used in embedded systems. It can keep stored data & information even when the power is off. It can be electrically erased & reprogrammed. Flash memory was developed from EEPROM (electronically erasable programmable read only memory).

=) Synchronous Dynamic Random Access memory :-

operations of SDRAM are controlled by a clock signal.

Ref

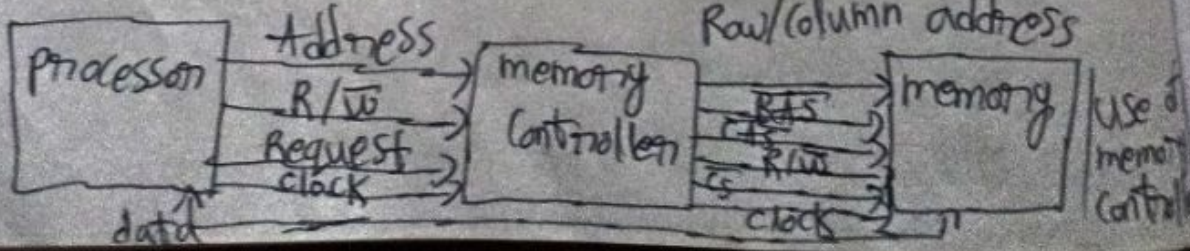


The factors / Speed & Efficiency of data transfer are affected by

- memory Latency → amount of time takes to transfer a word/data to/from the mem

Memory bandwidth → no. of bits/bytes that can be transferred in 1 second. used to measure how much time is needed to transfer an entire block of data.

Bandwidth = Data Transferred * width of data
Rate



⇒ Cache memory :-

→ Locality of Reference :-

- The references to memory at any given time interval tend to be confined within a localized areas.
- The area contains a set of Info & the membership changes gradually as time goes by.

→ Temporal Locality :-

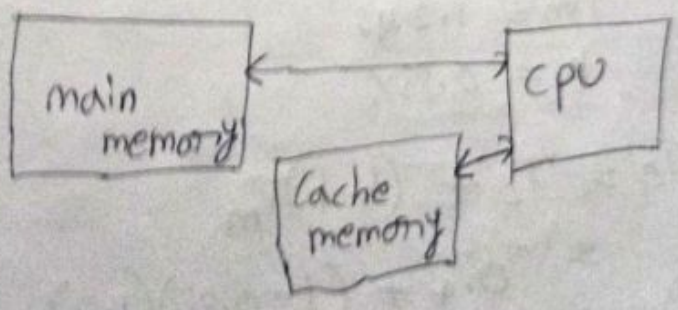
- The Info which will be used in near future, is likely to be in use already

→ Spatial Locality :-

If a word is accessed, adjacent words are likely accessed soon.

⇒ Cache :-

- The Property of Locality of Reference makes the Cache memory Systems work.
- Cache is a fast small capacity memory that should hold those Info which are most likely to be accessed.



⇒ performance of cache :-

memory Access

- All the memory accesses are directed

first to cache.

- If word in cache; Access cache to provide it to CPU.
- If word is not in cache; Bring a block(consecutive) including that word to replace a block now in cache.

→ How can we know if word that is needed is in cache?
→ If new replaces old blocks, which one should we choose?

⇒ Performance of cache memory System:-

Hit Ratio – % of memory accesses satisfied by cache memory system.

Te – Effective memory access time in cache memory system.

Tc – cache access time

Tm – main memory access time.

$$Te = Tc + (1-h)Tm$$

Ex:-

$Tc = 0.4\,\mu s$

$Tm = 1.2\,\mu s$

$h = 0.85\%$

$$Te = Tc + (1-h)Tm$$
$$= 0.4 + (1-0.85)(1.2)$$
$$= 0.4 + (0.15)(1.2)$$
$$= 0.4 + 0.18 \Rightarrow 0.58\,\mu s$$

Associative mapping:-

→ mapping function – Specification of correspondence b/w main memory blocks & cache blocks.

a) Any block location in cache can store any block in memory → most flexible.

b) mapping Table is implemented in an associative memory → Fast, very Expensive.

c) mapping Table → stores both addresses & the content of the memory word.

address (15 bits)

Argument register

← Address →	← Data →
01000	3450
02777	6710
22235	1234

Content Addressed memory

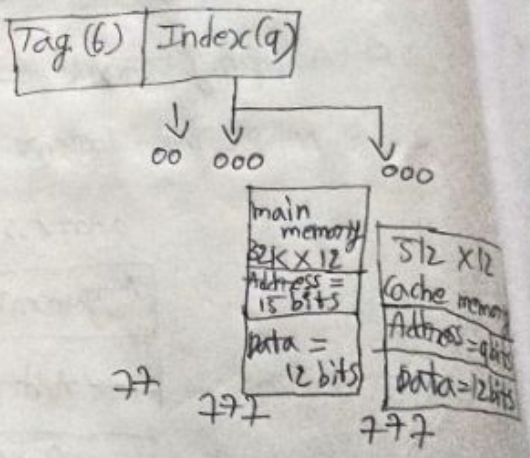
=> Direct mapping:-

a) Each memory block has only one place to load in cache.

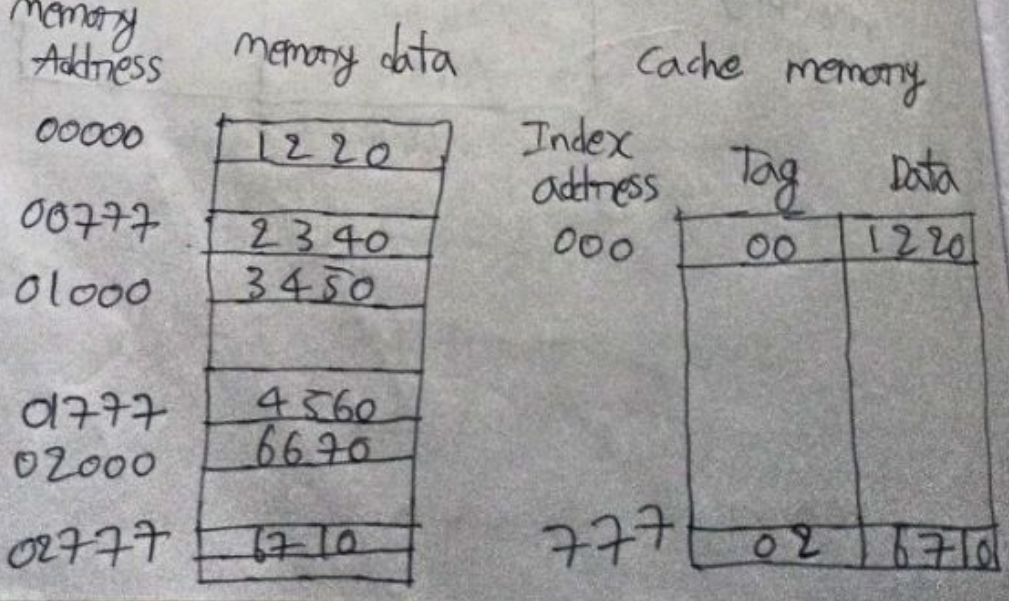
b) mapping table is made of RAM, instead of CAM.

c) n-bit memory address consists of 2 parts; K bits of index field & n-k bits of tag field

Addressing Relationships



Direct mapping cache organization:-

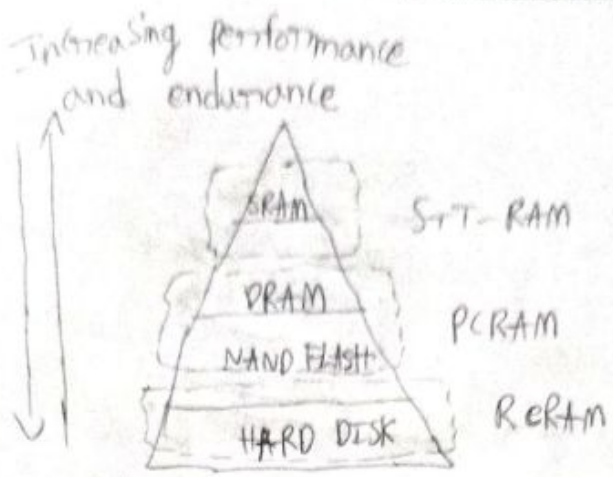


Increasing and e...

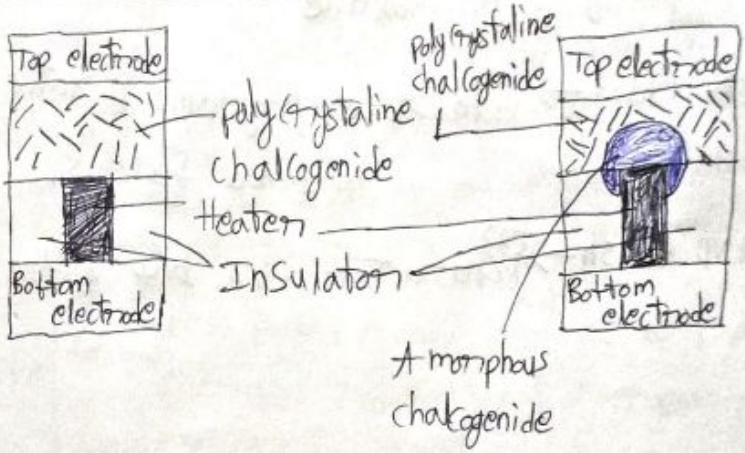
Decreasing cost ... increasing

=> non-vol...

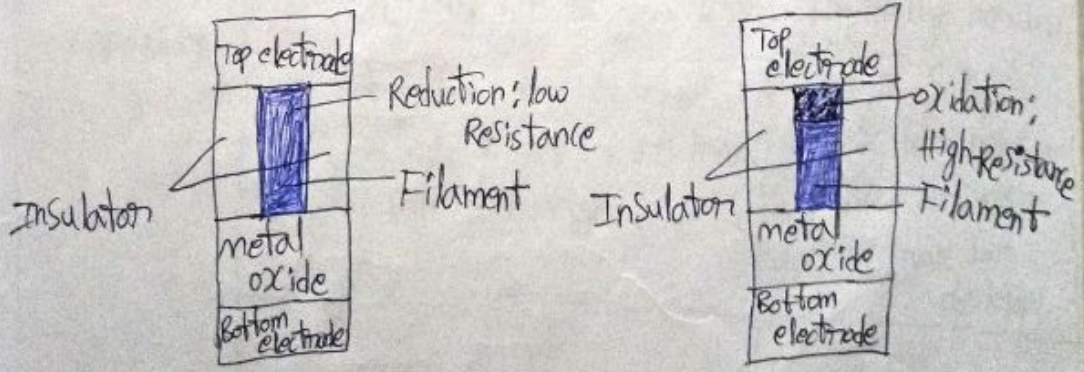
Insul...



=) Non-volatile RAM Technologies:-

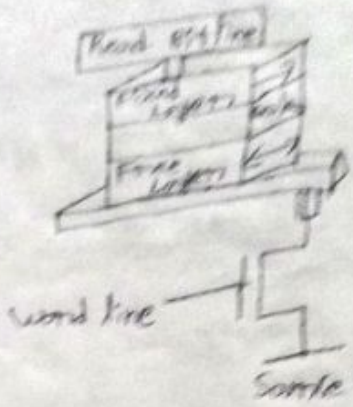


PCRAM



ReRAM

STT RAM



Flash memory → non-volatile

NOR flash → to store programs & static app data, Embedded Systems.

NAND flash → has characteristics b/w DRAM & hard disk.

=) Solid state drives:-

→ It refers to electronic circuitry built with semiconductors.

→ It replace hard disk drives (HDDs).

→ Both as Internal & External secondary memory.

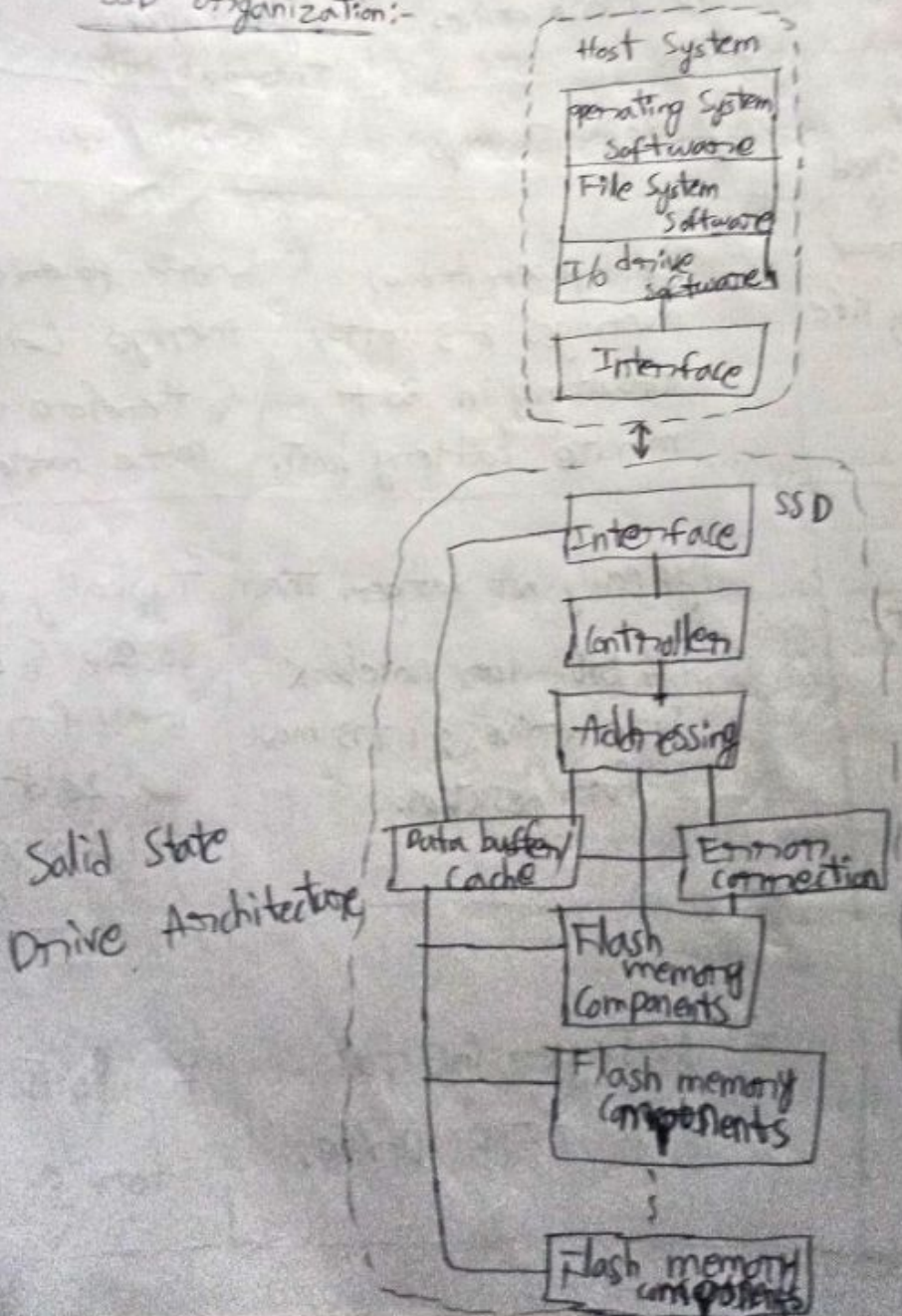
=) SSD compare to HDD:-

	NAND Flash drives	Seagate Laptop Internal HDD
File copy/ write speed	200–550 mbps	50–120 mbps
Power draw/ battery life	Less power draw, averages 2–3 watts, resulting in 30+ minute battery boost.	more power draw, Averages 6–7 watts, & therefore uses more battery.
Storage capacity	Typically not larger than 512 GB for notebook size drives; 1 TB max for desktops.	Typically around 500GB & 2TB max for notebook size drives; 4TB max for desktops.
Cost	≈ $0.50 per GB for a 1-TB Drive.	≈ $0.15 per GB for a 4-TB drive.

=> Advantages:-

- -> High-performance I/O operations/second
- -> Durability
- -> Longer life span
- -> Lower power consumption
- -> Quieter & cooler running capabilities.
- -> Lower access times & latency rates.

=> SSD organization:-



Solid State Drive Architecture

write through protocol, cache blocks updated, write back / copy back protocol.

early approach → to reduce processor waiting time.

⇒ set-associative mapping

write through:-

→ Simplest & most commonly used procedure is to update main memory & every memory write operation.

→ cache memory being updated in parallel, if it contains the word at the specified address, i.e. write through address.

→ Advantage:- main memory always contain the same data as the cache.

→ This characteristic is important in systems with the direct memory access, transfers.

→ It ensures Data residing in main memory are valid at all times so that an I/o device communicating through DMA would receive the most recent updated data.

⇒ write-back/ copy-back:-

→ The 2nd procedure is called the write-back method.

→ In this method, only the cache location is updated during a write operation.

→ It's location is marked by a flag so, that later when

the word is removed from the cache is copied into main memory.

→ Reason? — from the write back method
During the time a word resides in the cache, it may be updated several times.

→ As long as, the word remains in the cache, it doesn't matter whether the copy in main memory is out of date, since requests from the word are filled from the cache.

→ It is only — when word is displaced from cache, an accurate copy need be rewritten into main memory.

⇒ Set-associative mapping:-

→ Cache divided into no. of sets.

→ Set Consists → no. of blocks.

→ main memory block maps to a Specific cache Set based on eq. $S = i \bmod S$,

S - sets in cache (no.)
i - main memory block (no.)
s - Specific cache set to which block i maps.

→ An incoming block maps to any block in the assigned cache set.

→ Therefore All Address issued by the processor is divided into 3 distinct fields.

→ These are
→ Tag, Set
→ Set field
→ Tag fie
→ word
→ Ad
addr
Leng
S =
→
→

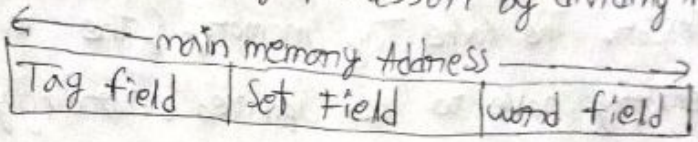
→ These are Tag, Set & word fields.

→ Set field- Used to identify the specific cache set that ideally should hold the targeted block.

→ Tag field- Identifies the targeted block with in the determined set (there).

→ word field- Identifies the Element within the block that is requested by the processor.

→ According to this technique, mmu interprets the address issued by processor by dividing into 3 fields.



Set-associative-mapped address fields

Length in bits,

a) word field = $\log_2 B$

b) Set field = $\log_2 S$

c) Tag field = $\log_2 \left(\frac{N}{S}\right)$

N - main memory size

S - no. of sets in cache

B - size of the Block in words.

$S = N = B_S$ / N - no. of cache Blocks

B_S - no. of the Blocks/set.

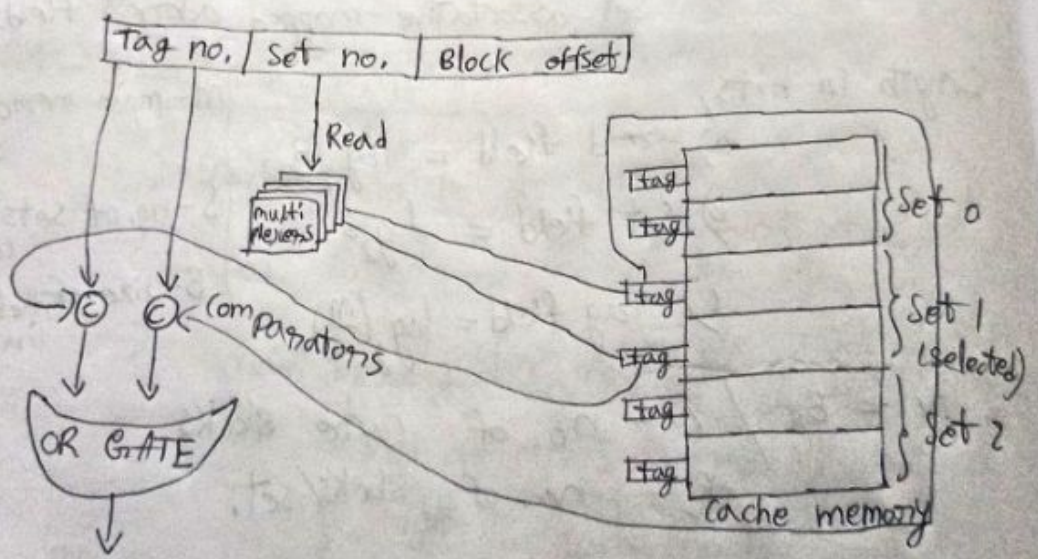
→ use Set field to determine the specified set.

→ Use Tag field to find a match with any of the blocks in the determined set. A match in Tag memory indicates that specified set determined

in Step 1, is holding targeted block, that is i.e. a cache

→ Array of words contained in hit cache block, the requested word is selected using a selector with the help of the word field.

→ If in Step 2, no match is found, then this indicates cache miss. ∴, Therefore the required block has to be brought from main memory, deposited in the specified set first, & the Targeted element is made available to the processor. The cache Tag memory & the cache block memory have to be updated accordingly.



2-way set Associative mapping