UNIT-III Micro programmed Control and Input-output organisation

Control memory

Address Sequencing -

micro Instruction, micro program, micro operations, control words

Interpreting of the control Address register

micro programmed control unit, micro Instructions, micro program

unconditional branch (or) conditional branch depending on Status bit conditions.

main memory → users → programs → machine Instructions & data → memory

Computer on - First load initial address into control address register with this we can execute instruction fetch routine

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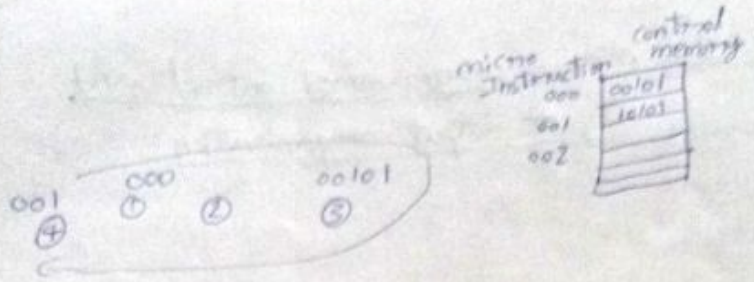


I/o interface:-

Internal storage — CPU memory
&
External devices — I/o-phera-pheral

1. (peripherals)
P→electro magnetic & Electro mechanical :-

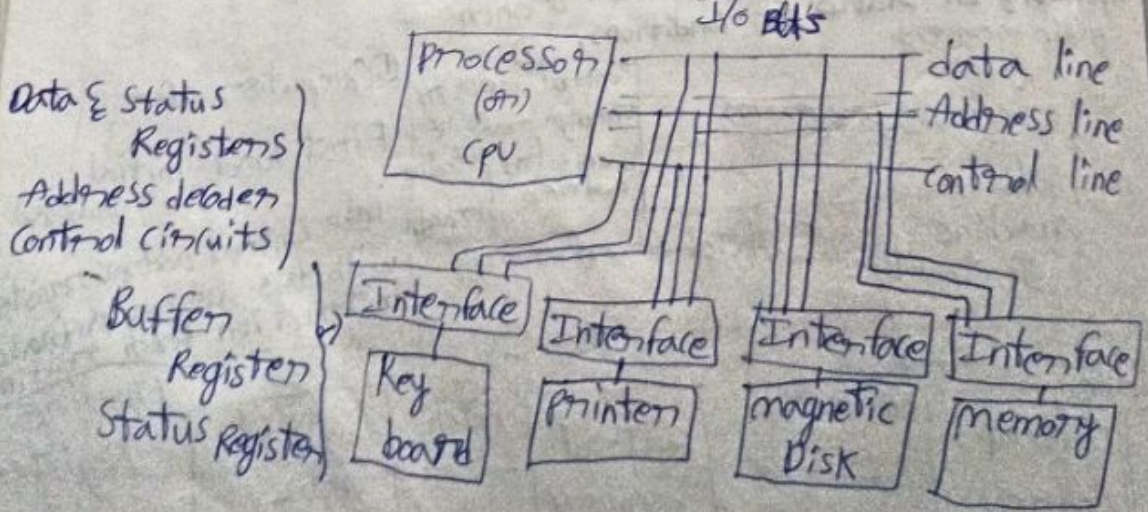
↓ CPU

(Conversion of signals)
CPU & memory

2. Data transfer rate of peripheral devices
Slower & CPU is fastern

3. Interface unit
↓ CPU & Input/output

⇒ I/o Bus and Interface module.



I/o Commands

memory B

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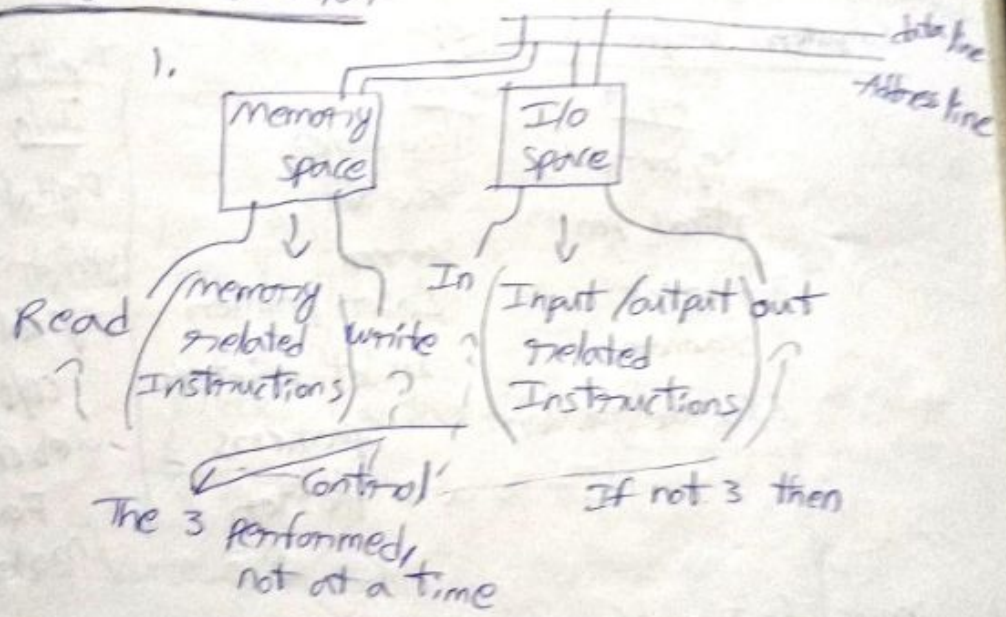
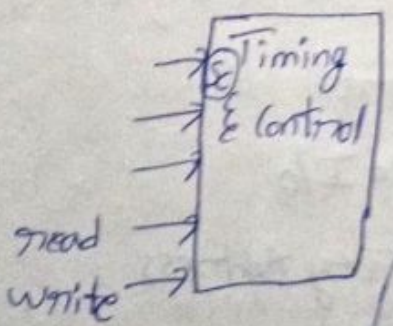
I/O Commands:-

a) Status command - To check the status of the devices.
b) Control command - To perform read & write operations.
c) Data input command - To give data to buffer Register.
d) Data output command - To take the data from buffer Register.

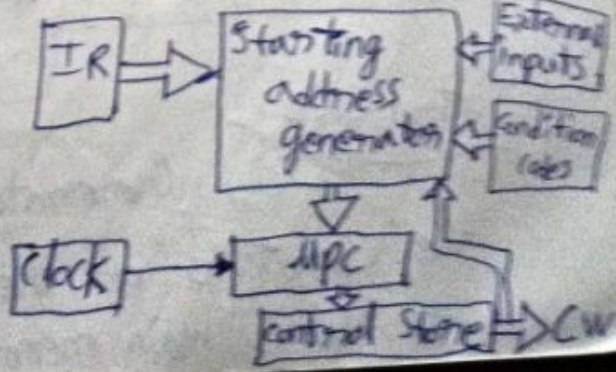
Memory Bus V/s I/O:-

1.





Basic organization of a micro programmed control unit.



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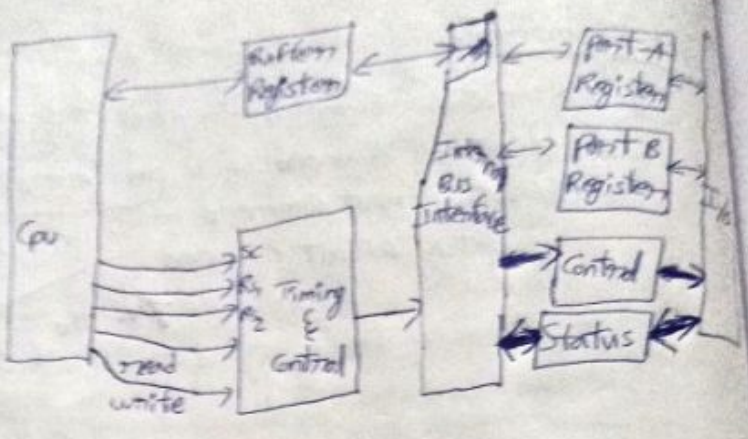


Computer peripheral device;-

input	output	I/O
Keyboard	head phones	Digital Camera
optical pen	head set	pen drive
Joy Stick	Screen	Digital Camera
Scanners	Laser printers	CD/DVD
Bar code reader	inkjet printers	web cam
	Speakers	Fax
	plotter	modem

Modes of Transfer;-

Programmed I/O

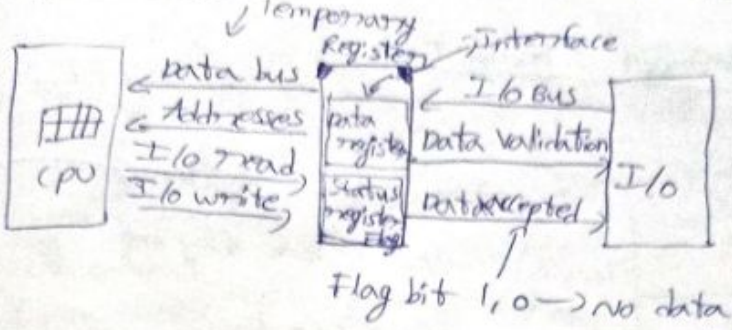
Interrupt initiated I/O

DMA → Data memory Address

Control unit;- Generates timing & control signals for the operations of the Computer. Control unit Comm with ALU & main memory. It controls transmission bw

processor memory & various peripherals.

=> programmed I/O:-



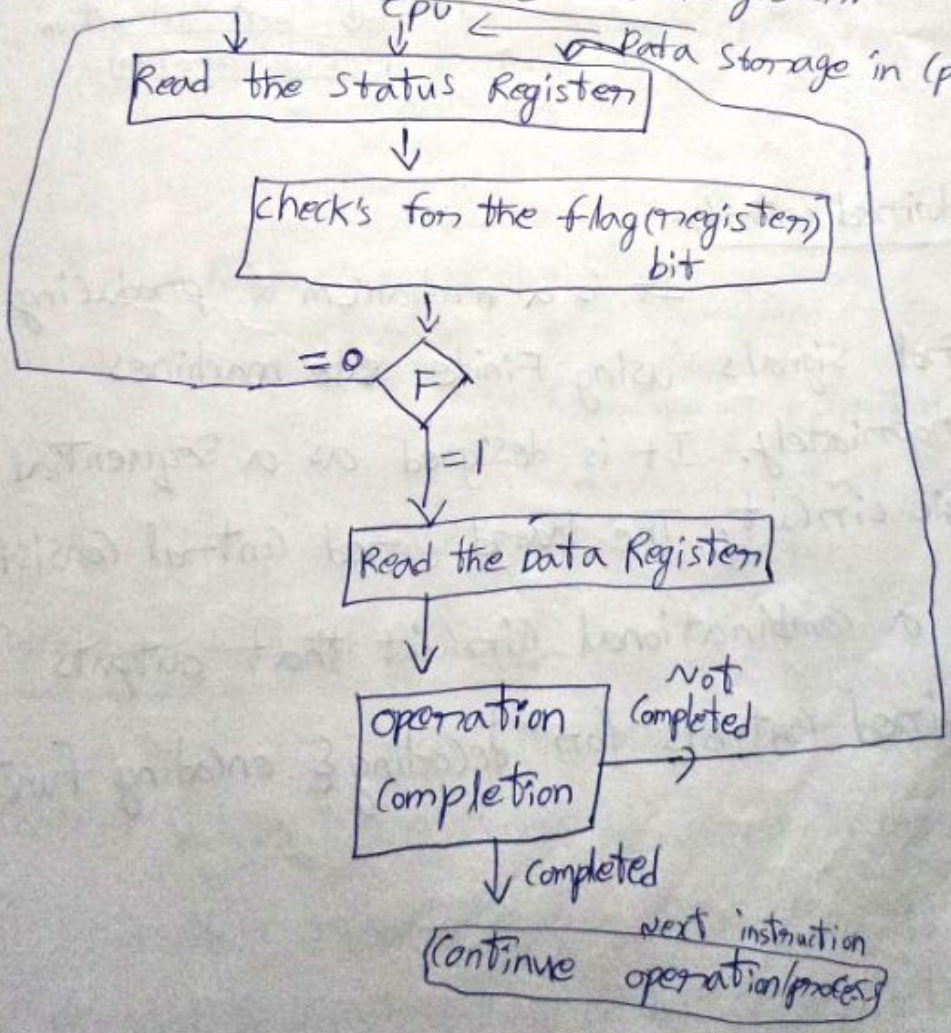
Sequence of bytes

each byte by 3 steps can be Transfered.

→ Read the status register

→ Check the Flag bit

→ Read the Data register.



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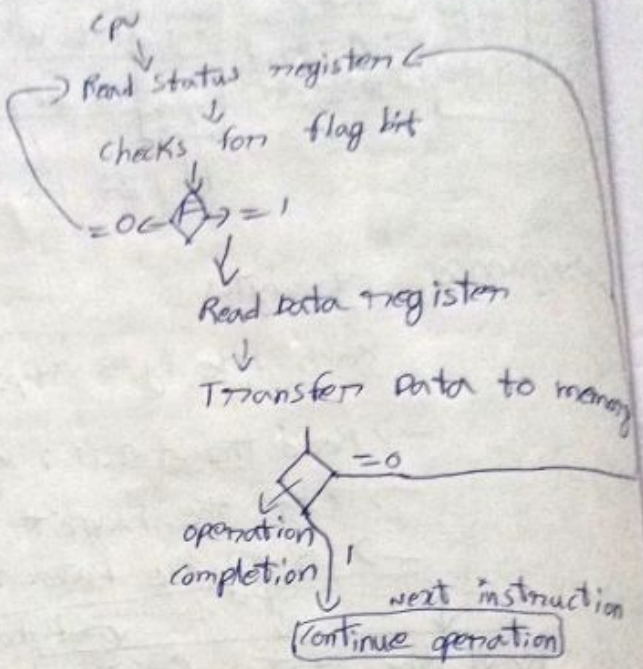
=> Interrupt initiate I/O:-



Handwired Control:-

It is a mechanism of producing control signals using Finite state machines appropriately. It is designed as a sequential logic circuit. The hard wired control consists of a combinational circuit that outputs desired controls for decoding & encoding functions

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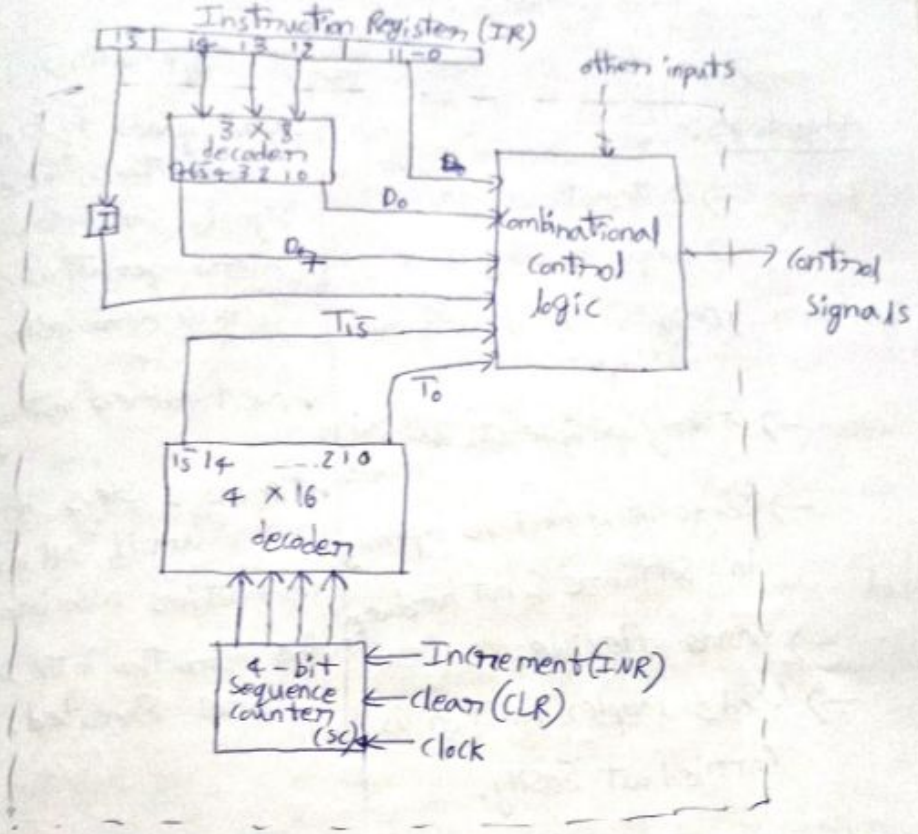

Routine → group of micro instructions.

Mapping → Transformation of instruction code bits to an address in control memory where the routine is located.

Microprogrammed Control:-

A control unit whose binary control values are saved as words in memory. A controller results in the instructions to be implemented by constructing a definite collection of signals at each system clock beat. when the bit is set,

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the control signal is active.

Instruction
↓↓↓
operations

Advantages:-

→ Systematic design,

→ Simple to debug & design.

→ Design of control unit much Simpler.

→ orderly and systematic design process

→ Used to control functions implemented in Software & not hardware.

→ more flexible.

→ Used to complex function is carried out Easily.

• Ram Signals to Exe... instructions, These Signals can control micro operations ... with a micro instruc...

• Next address instruct... gen...

• previous 2 steps done until all micro instructions associated w... the instruction in the set are Executed.

Dis advantages:-

→ Adaptability is obtained at more cost.

→ Slower than hardwired control unit.

=) modes of Transfer:-

CPU
↓
Read
Interrupt / CPU
↓
CPU

Interrupted initiated I/O:-

Interrupt Routine service
IRS
I/O

priority
=) TO ... I...
Software →
Hardware →
d...
Ise
Checks if
d gene...
pri...
=) Dis advant...
→ Time
=) Daisy cha...
This
dev...
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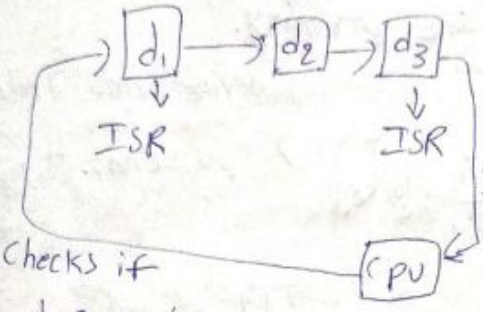
priority Interrupt

=) To overcome Interrupt approaches;-

Software → Polling

Hardware → Daisy chain
→ parallel chain



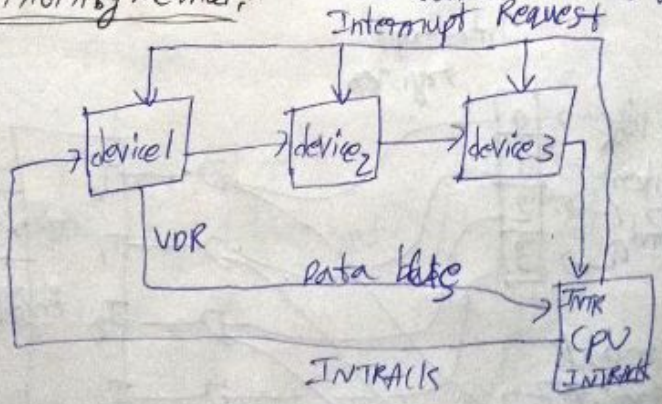
CPU checks every device based on priority

priority :- $d_1 > d_2 > d_3$

=) Dis advantages:-
→ Time Consuming

=) Daisy chain in priority method:-

VAD - Address of Service routine which services that device.



This method includes a serial connection of all devices that request an interrupt. The device with the highest priority is located in the first position followed by lower-priority devices up to the device

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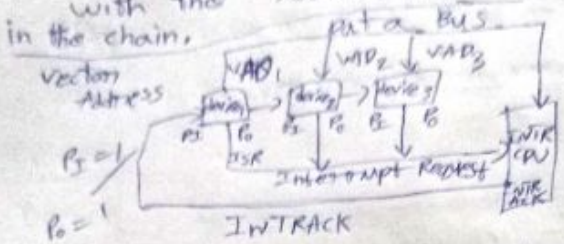
with the lowest priority which is situated
in the chain.



Priority:-
device 1 > device 2
> device 3

Interrupt Acknowledgement

=) Farthen the device, Lower the priority.

$P_I = 1$, VAD

$P_I = 0$, acknowledgement blocked (Not interrupt)

$P_0 = 1$, next device

$P_0 = 0$, ISR

$P_I = 0$ & $P_0 = 1$, next device

$P_I = 1$ & $P_0 = 0$, Consumes acknowledgement

→ device sends INTR to

→ CPU sends INTRACK to dev

→ If $P_I = 1$, generates

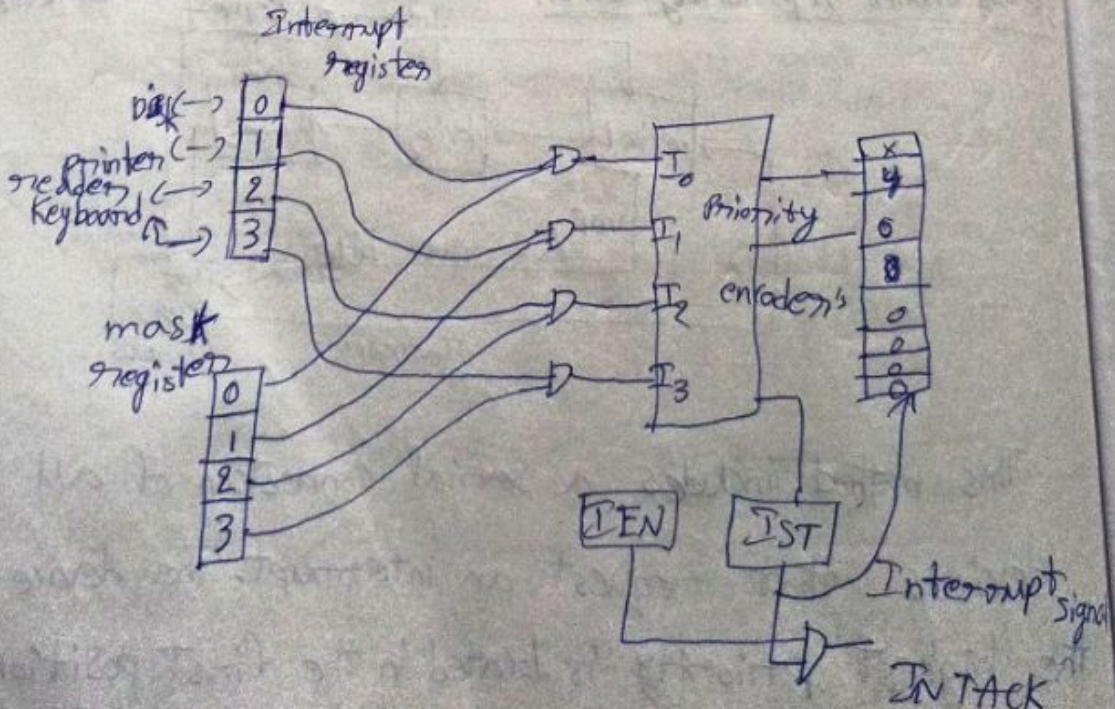
If $P_I = 0$, through

→ If $P_0 = 1$, Sends to next device.

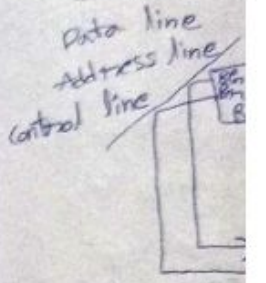
If $P_0 = 0$, ISR.

device puts interrupt vector address into data bus of CPU.

=) parallel priority Interrupt chain



=) Direct mem



=) PCI E

PCI E

Transactio
Laye

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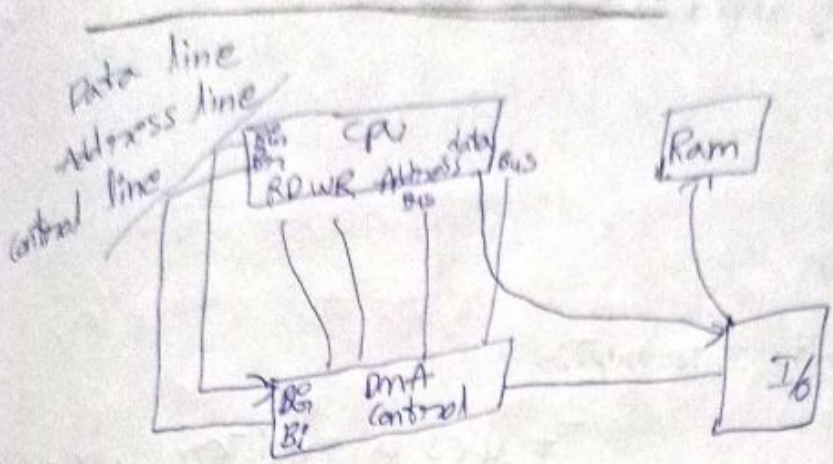
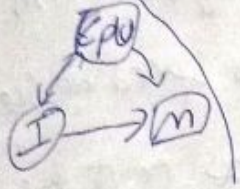
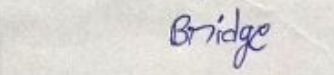
=) Direct memory Access control:-



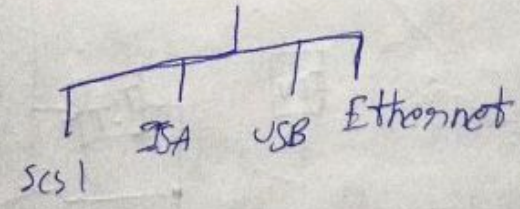
word count = 10 decrements every cycle

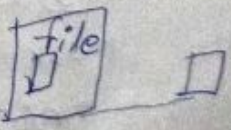


=) PCI Express:-

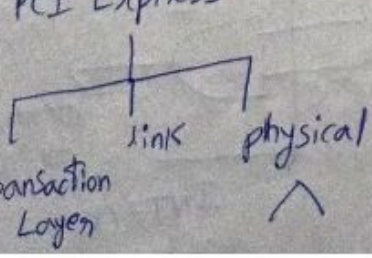


Bridge





PCI - good Architecture



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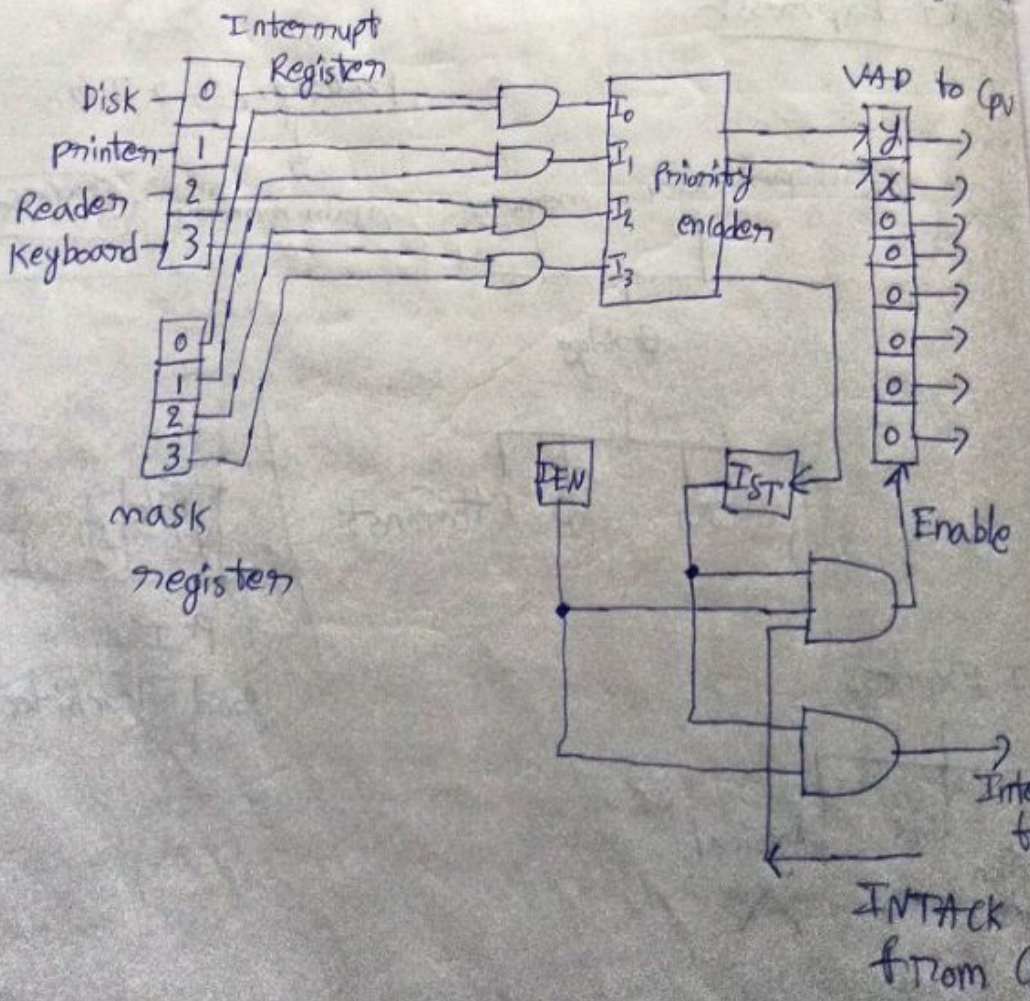
Polling – It involves testing a status flag repeatedly until a character is received, as dis...

Interrupt

Memory

⇒ Parallel priority Interrupt:-

It uses a register whose bits are set separately by the interrupt signal from each device. magnetic disk with its high speed device, given the highest priority, printer has next priority, followed by a character reader and a keyboard.



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priority - According to position of bits, in the register.

mask register - Controls the status of each interrupt request.

Programmed to disable Low-priority interrupts while a higher-priority device is being serviced.

By program register, we can set/reset any bit in the mask register.

Bits in interrupt register = Bits in mask register.

→ AND gate for Interrupt & mask bit to produce four inputs to a priority encoder.

→ Interrupt recognized if corresponding mask bit is set to 1 by the program, priority encoder generates 2 bits of VAD, transferred to CPU.

→ Another output from encoder sets interrupt status in flip-flop IST when an interrupt that's not masked occurs. Interrupt enable flip-flop IEN can be Set/cleared by the program to provide an overall control over the interrupt System.

→ outputs of IEN, IST provides a common interrupt signal for CPU.

→ Interrupt acknowledgement signal from CPU enables

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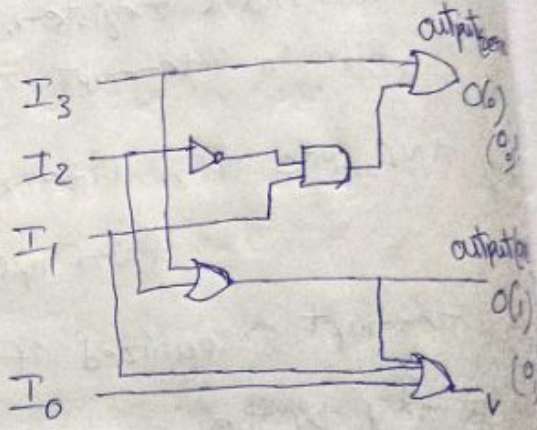
the bus buffers in the output registers & VAD is placed into the data bus.

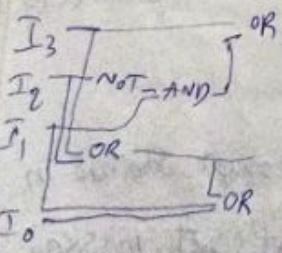
=) **priority encoder:-**

It is a circuit/Algorithm that compresses multiple binary inputs into a smaller number of outputs. They used to control interrupt requests by acting on highest priority interrupt.

4 to 2 priority encoder

I_3	I_2	I_1	I_0	O_1	O_0	V
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

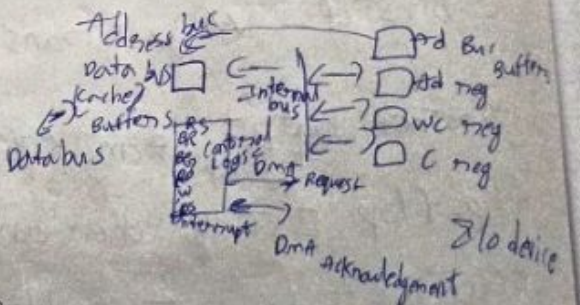




AND

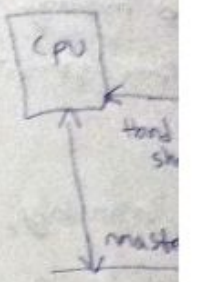
NOT

OR



=) **Direct memory access:-**

It is a feature of Computer Systems that allow certain hardware Subsystems to access main System memory (Random-access memory) independently of CPU. DMA can also be used for memory to memory coping/moving of data within memory.



CPU using
read/write
with DMA
other
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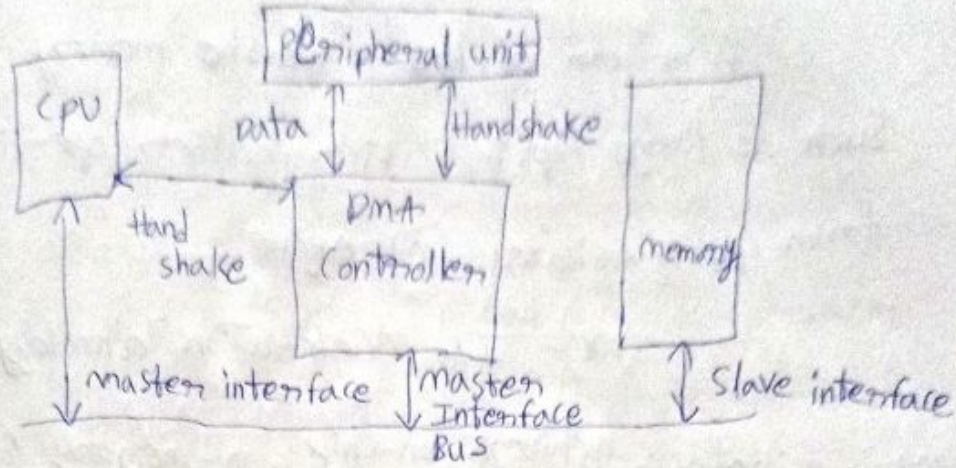

CPU using programmed I/O, it is fully occupied of read/write operation, & can't do other work.

with DMA, CPU initiates the transfer, then it do other operations while transfer is in progress, & finally receives an interrupt from DMA controller, when the operation is done. Useful at any time, CPU can't keep up with rate of data transfer, when CPU needs to perform work while waiting for a relatively slow I/o data transfer. many H/w Systems use DMA, including disk drive controllers, Sound cards. Used for intra-chip data transfer in multi-core processors. Computers with DMA can transfer data to & from devices with much less CPU overhead, than computers w/o DMA channels.

A processing Element inside a multi-core processor can transfer data to & from it's local memory without occuping it's processor time, allowing computation & data transfer

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to proceed in parallel.

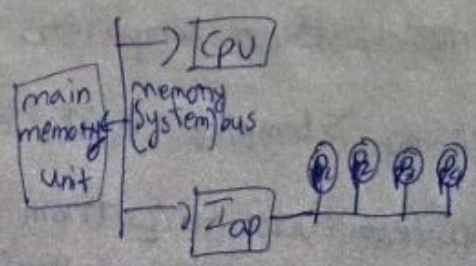
DMA can offload expensive memory operations such as large copies / scatter-gather operations, from CPU to dedicated DMA engine.

Ex:- I/O Acceleration Technology,

DMA is of interest in network-on-chip & in-memory computing architectures.

=> Input-output processor:-

Iop is like a CPU that handles the details of I/O operations. More equipped with facilities than those are available in typical DMA controllers. Iop can fetch & execute it's instructions that are specifically designed to characterize I/O transfers. In addition to I/O related tasks it can do other processing tasks like Arithmetic, logic, branching & code translation. main memory unit takes the pivotal role. It communicates with processor by means of DMA.



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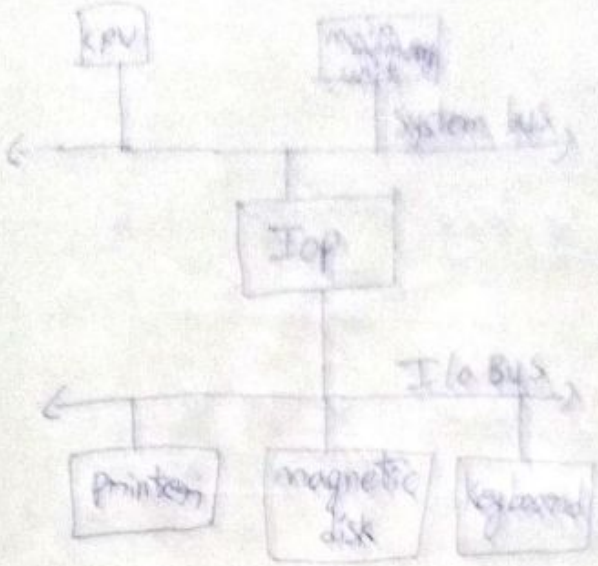

→ Input devices can directly access to main memory w/o intervention by processor in I/o processor based systems.

→ used to address problems that arises in

→ Iop is a specialised processor which loads & store data into memory along with execution of I/o instructions & acts as an interface between System & devices.

Comm'ds → processor to memory

processor to I/

⇒ PCI Express:-

Peripheral Component Interconnect is a local Computer bus for attaching hardware devices in a Computer & is part of the PCI local Bus Standard.

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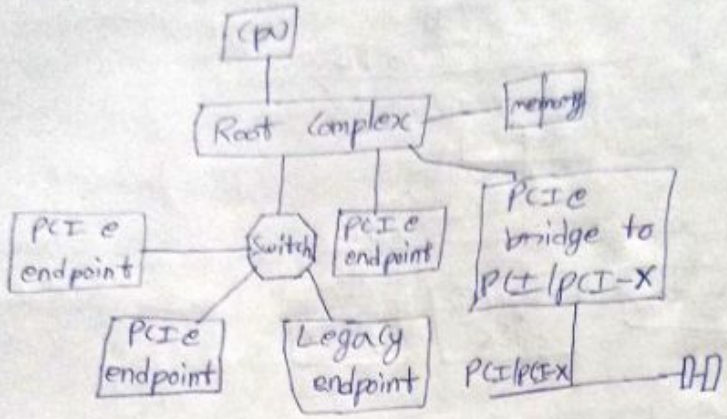

To install ethernet & remote cards.

Advantages:-

→ Interface a greatest of 5 components to PCI & you'll be able more supplant each of them by settled gadgets on the ~~brother~~ hand.

→ Diff. PCIs on Same computer.

→ PCI improve speed of exchanges from 33MHz to 133MHz, with transfer rate of 1gb/sec.

→ PCI can handle gadgets employing a greatest of 5 volts & pins utilized can exchange more that one flag through one stick.

Dis advantages:- → PCI Graphics Card can't get to System mem

→ PCI don't Support pipeline.

PCI
Physical & Logical architectu

PCI physical archi

Super

INT-IV
Internal

A_0 → Add
A_1 →
A_2 → dec
A_3 →

word