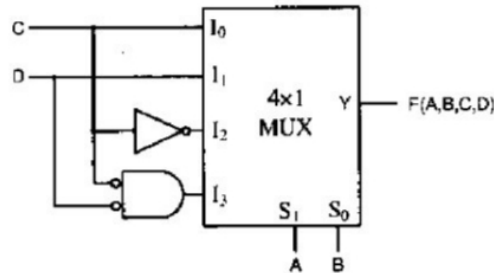


## Question

Q.39 The Boolean function realized by the logic circuit shown is



(A)  $F = \sum m(0, 1, 3, 5, 9, 10, 14)$   
(C)  $F = \sum m(1, 2, 4, 5, 11, 14, 15)$

(B)  $F = \sum m(2, 3, 5, 7, 8, 12, 13)$   
(D)  $F = \sum m(2, 3, 5, 7, 8, 9, 12)$

# Implementation of 4x1 Multiplexer using Verilog and Vaman Board

## Hardware Implementation Report

### Q.1 FPGA Experiment

#### Objective

To design, simulate, and physically implement a 4x1 multiplexer using Verilog HDL on a Vaman FPGA development board. The output of the multiplexer is observed using LEDs.

#### Hardware Required

- Vaman FPGA Board
- LEDs
- Resistors (220  $\Omega$ )
- Jumper Wires
- Breadboard
- sevensegment

## Theory

A multiplexer (MUX) is a combinational circuit that selects one of several input signals and forwards the selected input to a single output line. A 4x1 multiplexer has 4 input lines, 2 selection lines, and 1 output line.

The truth table for a 4x1 MUX is as follows:

Select Lines (S1 S0)	Selected Input	Output (Y)
00	I0	I0
01	I1	I1
10	I2	I2
11	I3	I3

## Verilog Code

```
\begin{lstlisting}[style=verilog, caption={4x1 Multiplexer Verilog Code}]
module mux_7seg(
    input A, B, C, D,          // Input switches
    output reg [6:0] seg
);

    wire F;
    wire I0, I1, I2, I3;

    // MUX input lines
    assign I0 = C;
    assign I1 = D;
    assign I2 = (~C) | D;
    assign I3 = 1'b0;

    // 4x1 MUX logic
    assign F = (~A & ~B & I0) |
               (~A & B & I1) |
               ( A & ~B & I2) |
               ( A & B & I3);

    // Display logic
    always @(*) begin
        case (F)
            1'b0: seg = 7'b0000001; // display '0'
            1'b1: seg = 7'b1001111; // display '1'
            default: seg = 7'b1111111; // off
        endcase
    end
endmodule
\end{lstlisting}
```

## PCF File (Pin Constraint File)

```
1 set_io a 3
2 set_io b 64
3 set_io c 62
4 set_io d 63
5 set_io e 61
6 set_io f 59
7 set_io g 57
8
9
10 set_io Z 56
11 set_io Y 23
12 set_io X 33
13 set_io W 27
```

Listing 1: .pcf File for Vaman Board Pin Mapping

## Procedure

1. Write the Verilog code for a 4x1 multiplexer in seven segment.
2. Create a new project in the Vaman IDE or through command line using Yosys and nextpnr.
3. Add the Verilog file and PCF file to the project.
4. Synthesize and implement the design.
5. Generate the bitstream or binary (.bin) file.
6. Upload the bitstream to the Vaman board.
7. Connect LEDs and switches to observe the multiplexer output.

## Output and Observation

When the select lines are changed, the output LED glows corresponding to the selected input line as per the truth table.

## Conclusion

The 4x1 multiplexer was successfully implemented on the Vaman FPGA board. The output matched the expected behavior as per the truth table. This experiment demonstrates how combinational logic can be implemented on FPGA hardware using Verilog HDL.

## Result

A 4x1 MUX was designed, simulated, and verified on the Vaman FPGA board using LEDs as output indicators.