



Tema 1:

El microcontrolador S3C44BOX

modelo de programación

Programación de sistemas y dispositivos

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- ✓ Gestor de reloj y energía.
- ✓ Controlador de cache.
- ✓ Árbitro de bus.
- ✓ Controlador de DMA.
- ✓ Controlador de pines de E/S.
- ✓ Temporizadores.
- ✓ UART.
- ✓ Controlador de interrupciones.
- ✓ Controlador de LCD.
- ✓ Conversor analógico-digital.
- ✓ Reloj de tiempo real.
- ✓ Watchdog timer.
- ✓ Controlador de IIC.
- ✓ Controlador de IIS.
- ✓ Controlador de SIO.

Conceptos previos

MPU, MCU, DSP y SoC



■ Microprocesador (MPU)

- Chip que **integra una CPU** (o varias) de altas prestaciones.
 - 32/64 bits, GHz, 100-1000€
- Por sí solo es inútil: un sistema requiere dispositivos externos que se ubican en placa.

■ Microcontrolador (MCU)

- Chip que **integra una CPU** de bajas prestaciones y un **conjunto reducido de dispositivos internos**:
 - Memoria, GPIO, temporizador, UART, conversores A/D.
 - 4, 8, 16 y 32 bits, 100 MHz, 0,5-10€
- Un microcontrolador puede implementar por sí solo un sistema completo.

■ Procesador digital de señal (DSP)

- Chip que **integra una CPU especializada** en el procesado de señales continuas digitalizadas y un **conjunto reducido de dispositivos internos**.

■ System-on-chip (SoC)

- Es un término comercial que se usa para referirse a un MCU/DSP de gama alta.
- Chip que **integra una CPU de mayores prestaciones** y/o una mayor variedad y número de **dispositivos internos** que un MCU/DSP.
 - DMA, controladores de buses estándar, aceleradores...

Conceptos previos

Conexión procesador-dispositivo



- Conceptualmente un **dispositivo** puede conectarse al procesador
 - **Directamente** a través del bus del sistema.
 - **Indirectamente** a través de algún tipo de adaptador/controlador que hace de puente entre el bus del sistema y el dispositivo .
- Existen 2 esquemas de **conexión directa**:
 - **E/S aislada**
 - Los dispositivos y la memoria tienen un **espacio de direccionamiento distinto**.
 - El programador usa instrucciones distintas para acceder a memoria o al dispositivo.
 - El bus del sistema tiene señales ad-hoc que indican si el acceso es a memoria o a dispositivo.
 - **E/S mapeada en memoria**
 - Los dispositivos y la memoria comparten un **espacio de direccionamiento común**. Los rangos de direcciones de dispositivos y memoria no solapan.
 - El programador usa la misma instrucción para acceder a memoria o al dispositivo.
- La **conexión indirecta** puede hacerse a través de:
 - Puertos de E/S genéricos digitales (GPIOs) o analógicos (conversores AD/DA)
 - El programador genera las formas de onda que sean necesarias para la transferencia.
 - Interfaces de E/S específicos (RS232, IIC, IIS, SPI, CAN, USB...)
 - Un hardware dedicado genera las formas de onda que sean necesarias para la transferencia.

Conceptos previos

Acceso a dispositivos

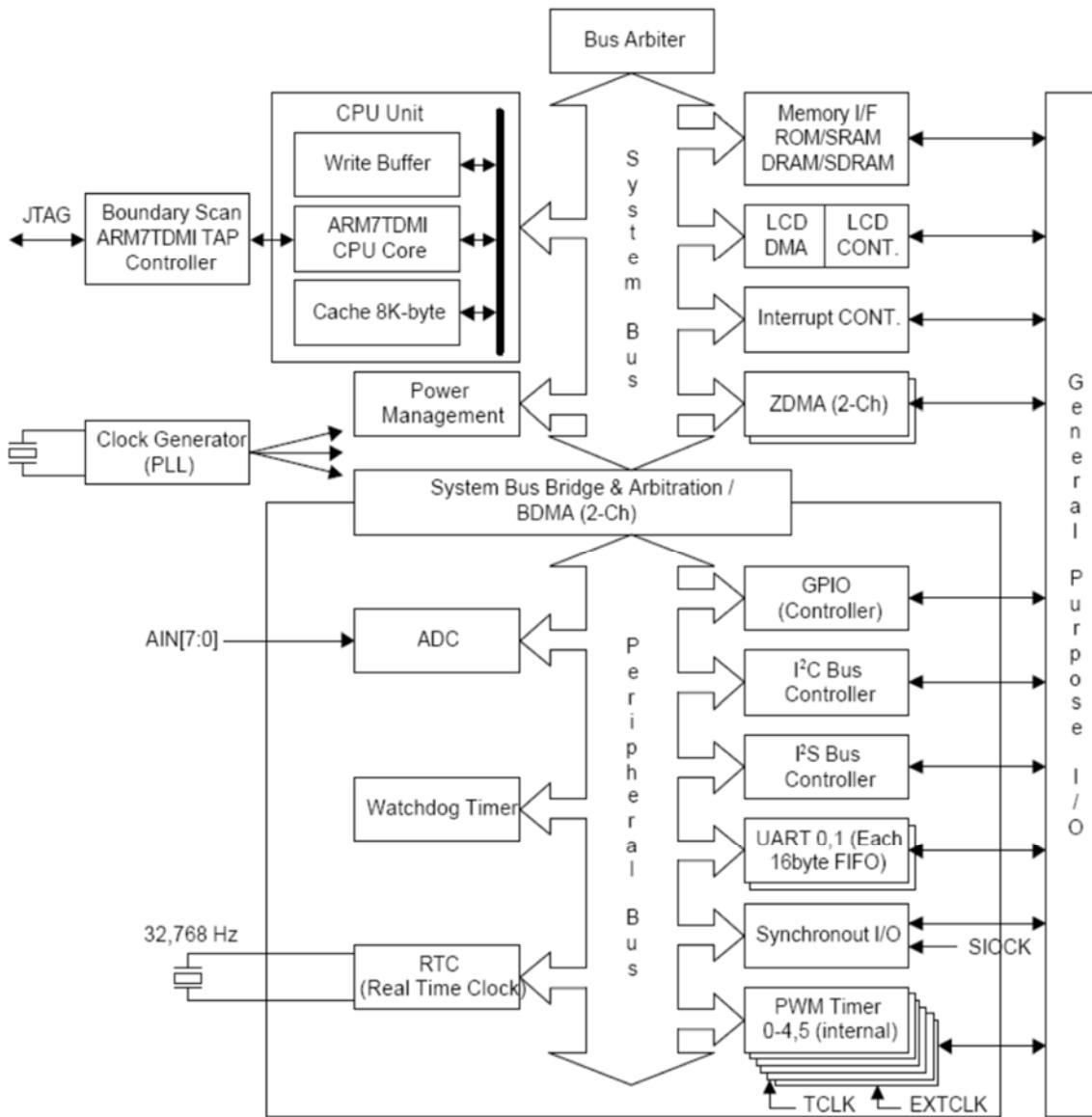


- Desde el punto de vista del programador un dispositivo es colección de registros cada uno de los cuales tiene una dirección asociada.
 - Registros de control (W): Permiten regular el modo de funcionamiento del dispositivo.
 - Registros de estado (R): Informan sobre el desarrollo de la operación de E/S
 - Registros de datos (RW): Contienen temporalmente los datos a transferir.

- Para programar un sistema empotrado es necesario saber:
 - La arquitectura del procesador
 - Repertorio de instrucciones, modos de direccionamiento, excepciones, etc.
 - Queda parcialmente oculta cuando se programa en un lenguaje de alto nivel.
 - La arquitectura de cada dispositivo.
 - Registros internos, modos de funcionamiento, etc.
 - Modo en que cada dispositivo está conectado al procesador.
 - Determina el método a usar para acceder a cada registro del dispositivo.



Estructura del S3C44BOX



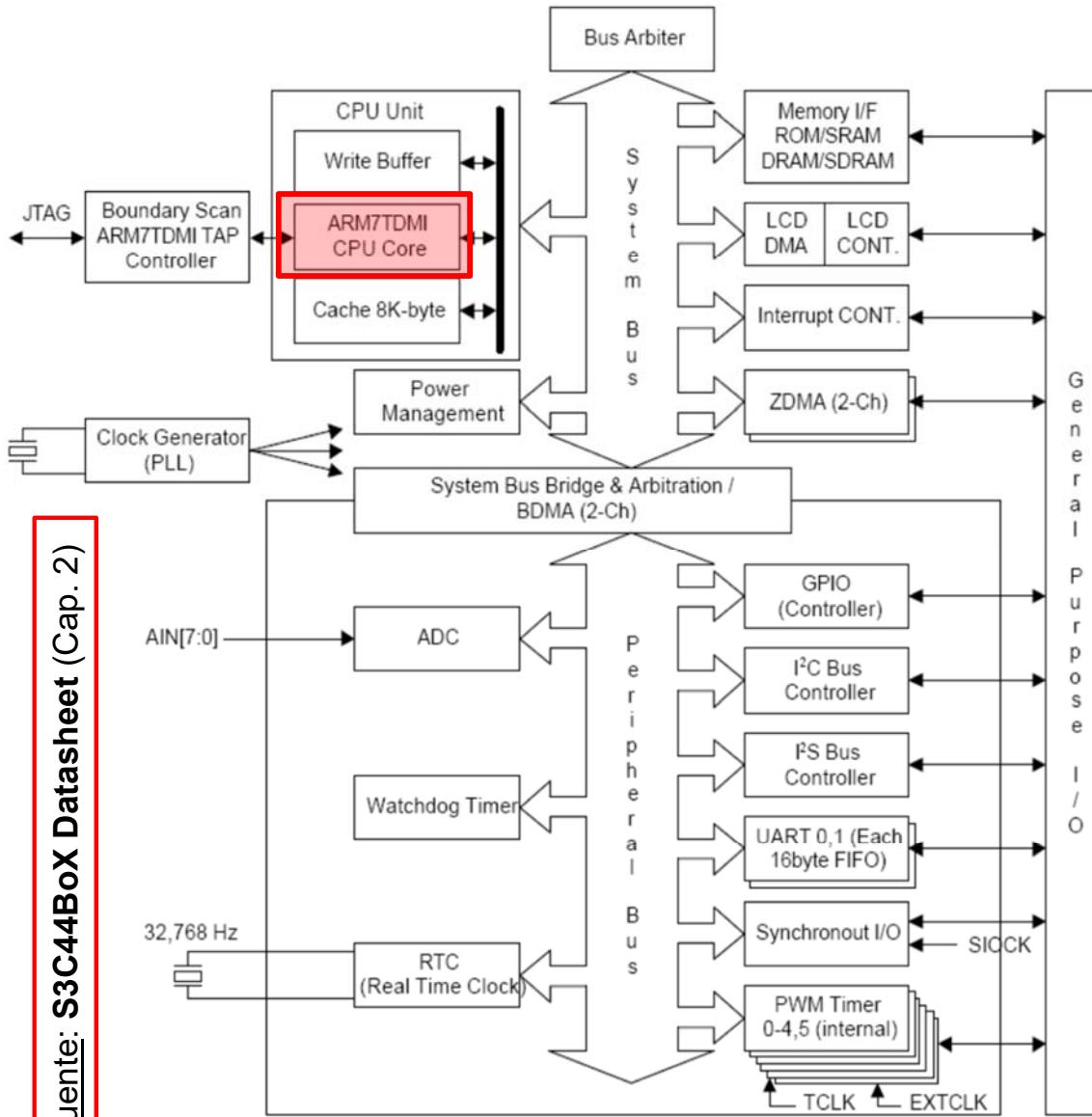
System-on-Chip de Samsung

- 1 Core ARM7TDMI (66 MHz)
- 1 Cache configurable
- 3 Buses: local, sistema y de periféricos
- 26 dispositivos internos (controladores) mapeados en memoria y configurables

tecnología:

- Standard cells
- CMOS 0,25 μm

ARM7TDMI Core



- Procesador de 32 bits
- Arquitectura Load-Store
- Segmentado en 3 etapas: Fetch, Decode, Execute
- Doble repertorio
- Formato de 3 operandos
- Todas las instrucciones están predicadas.
- No tiene coprocesador



ARM7TDMI Core

estados

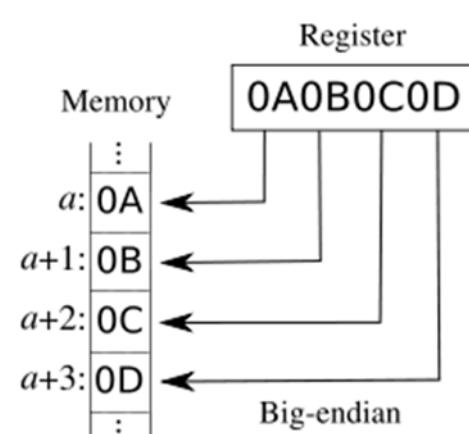
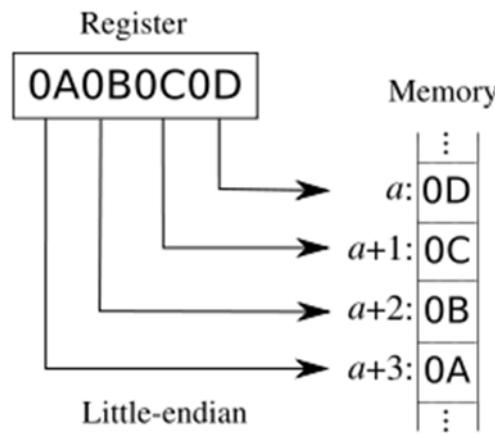
- La CPU del S3C44B0X puede estar en uno de los **2 estados** siguientes:
 - **ARM**: ejecuta instrucciones del repertorio ARM (32b).
 - **Thumb**: ejecuta instrucciones compactas del repertorio THUMB (16b).
- El **estado tras reset** es **ARM**.
- El **cambio de estado** se efectúa:
 - Ejecutando una **instrucción BX** con un argumento adecuado.
 - **Tras una excepción la CPU siempre pasa a estado ARM**, el retorno de la RTI devolverá el estado previo que tuviera.



ARM7TDMI Core

instrucciones y datos

- Instrucciones de **longitud fija**
 - repertorio ARM: 32b (alineadas en direcciones múltiplo de 4)
 - repertorio Thumb: 16b (alineadas en direcciones múltiplo de 2)
 - Un **programa ocupará en bytes**, según el caso, el **(núm. de instrucciones) ×4** ó **×2**
- Tipos de datos: **enteros**
 - byte: 8b
 - media palabra: 16b (alineadas en direcciones múltiplo de 2)
 - palabra: 32b (alineadas en direcciones múltiplo de 4)
 - El **ordenamiento** de los bytes (little/big endian) de una palabra es seleccionable según el valor del pin ENDIAN tras reset.



ARM7TDMI Core

modos de operación



- El ARM7TDMI soporta 7 modos de operación distintos:
 - User (USR): modo de usuario normal para la ejecución de programas.
 - FIQ: modo de servicio a interrupciones rápidas.
 - IRQ: modo de servicio a interrupciones de propósito general.
 - Supervisor (SVC): modo privilegiado de sistema operativo.
 - Abort (ABT): modo de servicio a fallos de acceso a datos o instrucciones.
 - System (SYS): modo de usuario de sistema operativo.
 - Undefined (UND): modo de servicio a fallos por instrucción no definidas.
- USR y SYS son modos de usuario, el resto son modos privilegiados.
- El modo de operación tras reset es SVC.
- El cambio de modo se efectúa:
 - Ejecutando una instrucción MSR con un argumento adecuado.
 - Tras la llegada de una excepción o de una interrupción externa.



ARM7TDMI Core

registros (i)

- El ARM7TDMI dispone de **37 registros de 32b.**
 - El estado y modo en el que se encuentra el procesador determina los registros accesibles en cada momento.
 - Algunos son visibles en cualquier modo y otros solo desde uno de ellos.
- En cualquier modo del estado ARM son accesibles:
 - **15 registros de propósito general** (R0-R14)
 - R11 (**FP**) suele usarse como puntero al marco de activación de funciones.
 - R12 (**IP**) suele usarse como registro auxiliar en la construcción de marcos de activación.
 - R13 (**SP**) suele usarse como puntero de pila.
 - R14 (**LR**) se usa como registro de enlace: almacena la dirección de retorno de subrutina.
 - **1 contador de programa** (R15/**PC**)
 - **1 registro de estado** actual del programa (**CPSR**)
- En los modos privilegiados también es accesible:
 - 1 registro que almacena un **valor anterior del CPSR** (**SPSR**).
- En cada modo del estado THUMB solo son accesibles un subconjunto de los registros visibles en el correspondiente modo ARM
 - R0-R7, SP, LR y CPSR (si está en modo privilegiado además SPSR).

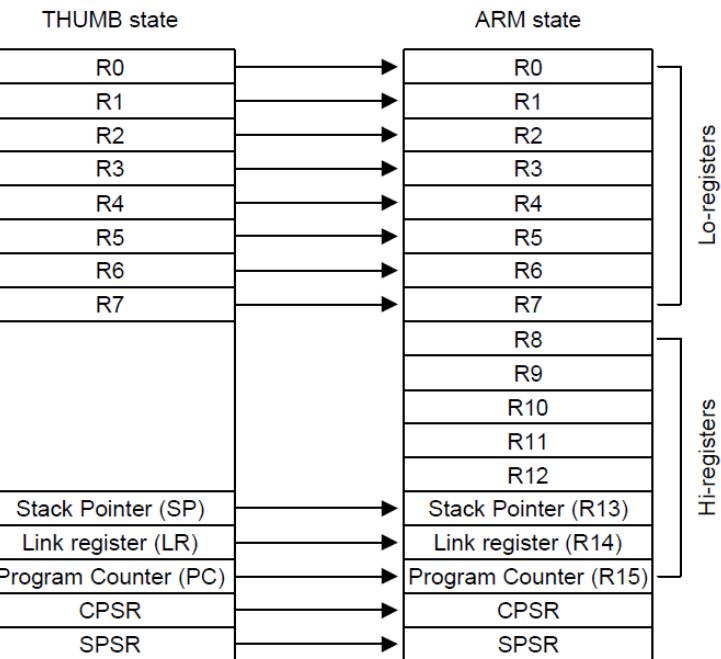
ARM7TDMI Core

registros (ii)

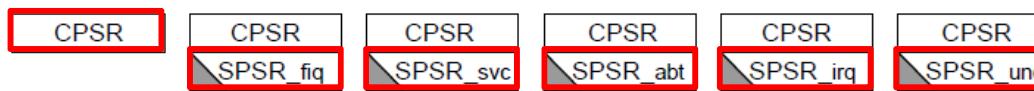


ARM State General Registers and Program Counter

| System & User | FIQ | Supervisor | Abort | IRQ | Undefined |
|---------------|----------|------------|----------|----------|-----------|
| R0 | R0 | R0 | R0 | R0 | R0 |
| R1 | R1 | R1 | R1 | R1 | R1 |
| R2 | R2 | R2 | R2 | R2 | R2 |
| R3 | R3 | R3 | R3 | R3 | R3 |
| R4 | R4 | R4 | R4 | R4 | R4 |
| R5 | R5 | R5 | R5 | R5 | R5 |
| R6 | R6 | R6 | R6 | R6 | R6 |
| R7 | R7 | R7 | R7 | R7 | R7 |
| R8 | R8_fiq | R8 | R8 | R8 | R8 |
| R9 | R9_fiq | R9 | R9 | R9 | R9 |
| R10 | R10_fiq | R10 | R10 | R10 | R10 |
| R11 | R11_fiq | R11 | R11 | R11 | R11 |
| R12 | R12_fiq | R12 | R12 | R12 | R12 |
| R13 | R13_fiq | R13_svc | R13_abt | R13_irq | R13_und |
| R14 | R14_fiq | R14_svc | R14_abt | R14_irq | R14_und |
| PC | R15 (PC) | R15 (PC) | R15 (PC) | R15 (PC) | R15 (PC) |



ARM State Program Status Registers



Mapping of THUMB State Registers onto ARM State Registers

CPSR previo

= banked register

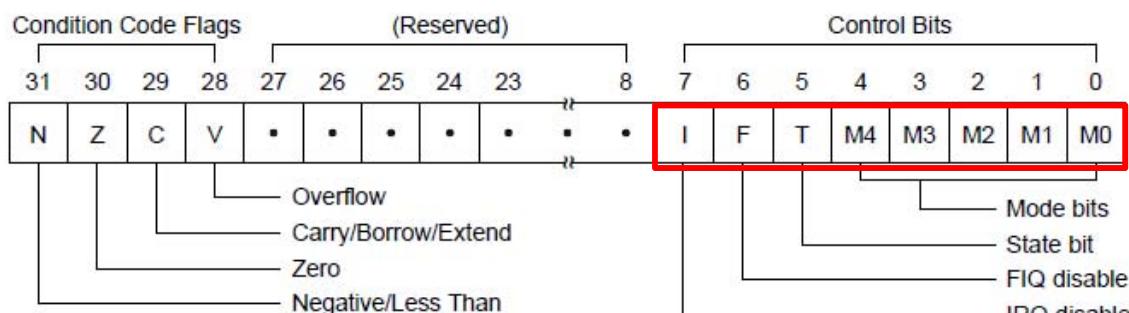
ARM7TDMI Core

registros (iii)



- El **registro de estado** permite:

- Obtener información de la última operación aritmética realizada (flags de condición)
- Conocer (que no cambiar) el estado del procesador (0/1 = ARM/Thumb)
- Habilitar/deshabilitar (0/1) interrupciones.
- Fijar el modo de operación.



estos bits solo pueden cambiarse en modo privilegiado ejecutando una instrucción MSR

| Modo | Código |
|------|--------------|
| USR | 10000 (0x10) |
| FIQ | 10001 (0x11) |
| IRQ | 10010 (0x12) |
| SVC | 10011 (0x13) |
| ABT | 10111 (0x17) |
| UND | 11011 (0x1b) |
| SYS | 11111 (0x1f) |

- Existen un total de **6 registros de estado**:

- 1 CPSR (Current Program Status Register) visible desde cualquier modo.
- 5 SPSR (Saved Program Status Register) cada uno de ellos contiene una copia del CPSR previo a la excepción que provocó el cambio de modo.

ARM7TDMI Core

repertorio ARM (i)



| Mnemonic | Instruction | Action |
|----------|---|---|
| ADC | Add with carry | Rd: = Rn + Op2 + Carry |
| ADD | Add | Rd: = Rn + Op2 |
| AND | AND | Rd: = Rn AND Op2 |
| B | Branch | R15: = address |
| BIC | Bit Clear | Rd: = Rn AND NOT Op2 |
| BL | Branch with Link | R14: = R15, R15: = address |
| BX | Branch and Exchange | R15: = Rn, T bit: = Rn[0] |
| CDP | Coprocessor Data Processing | (Coprocessor-specific) |
| CMN | Compare Negative | CPSR flags: = Rn + Op2 |
| CMP | Compare | CPSR flags: = Rn - Op2 |
| EOR | Exclusive OR | Rd: = (Rn AND NOT Op2) OR (Op2 AND NOT Rn) |
| LDC | Load coprocessor from memory | Coprocessor load |
| LDM | Load multiple registers | Stack manipulation (Pop) |
| LDR | Load register from memory | Rd: = (address) |
| MCR | Move CPU register to coprocessor register | cRn: = rRn {<op>cRm} |
| MLA | Multiply Accumulate | Rd: = (Rm × Rs) + Rn |
| MOV | Move register or constant | Rd: = Op2 |

No aplican: S3C44B0X no incluye coprocesador.

Orientadas a programación de sistemas

ARM7TDMI Core

repertorio ARM (ii)



| Mnemonic | Instruction | Action |
|----------|--|----------------------------|
| MRC | Move from coprocessor register to CPU register | Rn: = cRn {<op>cRm} |
| MRS | Move PSR status	flags to register | Rn: = PSR |
| MSR | Move register to PSR status	flags | PSR: = Rm |
| MUL | Multiply | Rd: = Rm × Rs |
| MVN | Move negative register | Rd: = 0 × FFFFFFFF EOR Op2 |
| ORR | OR | Rd: = Rn OR Op2 |
| RSB | Reverse Subtract | Rd: = Op2 - Rn |
| RSC | Reverse Subtract with Carry | Rd: = Op2 - Rn - 1 + Carry |
| SBC | Subtract with Carry | Rd: = Rn - Op2 - 1 + Carry |
| STC | Store coprocessor register to memory | address: = CRn |
| STM | Store Multiple | Stack manipulation (Push) |
| STR | Store register to memory | <address>: = Rd |
| SUB | Subtract | Rd: = Rn - Op2 |
| SWI | Software Interrupt | OS call |
| SWP | Swap register with memory | Rd: = [Rn], [Rn] := Rm |
| TEQ | Test bitwise equality | CPSR flags: = Rn EOR Op2 |
| TST | Test bits | CPSR flags: = Rn AND Op2 |

No aplican: S3C44B0X no incluye coprocesador.

Orientadas a programación de sistemas

ARM7TDMI Core

repertorio ARM (iii)



- La ejecución de toda instrucción pueden estar condicionada.

| Suffix | Flags | Meaning |
|--------|-----------------------------|-------------------------|
| EQ | Z set | equal |
| NE | Z clear | not equal |
| CS | C set | unsigned higher or same |
| CC | C clear | unsigned lower |
| MI | N set | negative |
| PL | N clear | positive or zero |
| VS | V set | overflow |
| VC | V clear | no overflow |
| HI | C set and Z clear | unsigned higher |
| LS | C clear or Z set | unsigned lower or same |
| GE | N equals V | greater or equal |
| LT | N not equal to V | less than |
| GT | Z clear AND (N equals V) | greater than |
| LE | Z set OR (N not equal to V) | less than or equal |
| AL | (ignored) | always |

ARM7TDMI Core

modos de direccionamiento



- Instrucciones aritmético-logicas:
 - Primer operando: registro (Rn).
 - Segundo operando: inmediato (#n) o registro (Rm) desplazado/rotado un número de posiciones indicado por inmediato (#m) o registro (Rx).
 - Existe la opción de indicar si se **modifican o no flags**.

- Instrucciones con acceso a memoria:
 - Primer operando: registro (Rn).
 - Segundo operando: registro base (Rm) +/- offset pre/post indexado
 - Offset: inmediato (#n) o registro (Rm) desplazado/rotado un número de posiciones indicado por inmediato (#m)
 - Existe la opción de indicar el **tipo de dato**.

ARM7TDMI Core

tiempos de ejecución de instrucciones (i)



- El ARM7TDMI es un **procesador segmentado** en 3 etapas:
 - Puede tener en ejecución hasta 3 instrucciones simultáneamente cuyos tiempos de ejecución se solapan.
 - Por ello, el tiempo de ejecución de una porción de código es menor que la suma de los tiempos de ejecución de las instrucciones que lo forman.
- El **tiempo de ejecución de una instrucción** se mide como el **número de ciclos que añade** dicha instrucción al tiempo de ejecución global.
- Sin embargo, como **toda instrucción implica al menos un acceso a memoria** (fetch) su tiempo de ejecución **se mide en ciclos de bus**.
 - Los ciclos de bus, en función de la organización de la memoria, las tecnologías usadas y el patrón de referencias se podrán traducir (con cierto grado de incertidumbre) a ciclos de reloj.

ARM7TDMI Core

tiempos de ejecución de instrucciones (ii)



- El interfaz de bus del procesador ARM7TDMI puede realizar 4 tipos diferentes de ciclos de bus:
 - Ciclo no secuencial (N-cycle): realiza una **transferencia con memoria** cuya dirección **no tiene relación** con la dirección de memoria usada del ciclo de bus anterior.
 - Dependiendo de la tecnología de memoria, puede requerir más de 1 ciclo de reloj.
 - Ciclo secuencial (S-cycle): realiza una **transferencia con memoria** cuya dirección es la **misma o la siguiente** a la dirección de memoria usada en el ciclo de bus anterior.
 - Si la tecnología de memoria permite transferencias en ráfaga (DRAM), requerirá un menor número de ciclos de reloj que un ciclo no secuencial.
 - Una ráfaga comienza con una N-Cycle y continúa con S-cycles
 - Ciclo interno (I-cycle): **no realiza transferencia con memoria** porque el procesador está realizando alguna función interna.
 - Ciclo de transferencia de registros con el coprocesador (C-Cycle): **no realiza transferencia con memoria** porque el procesador comunica datos con el coprocesador.

ARM7TDMI Core

tiempos de ejecución de instrucciones (iii)



| Instrucción | Ciclos | Ciclos adicionales |
|---|------------------|--|
| ADC, ADD, AND, BIC, CMN, EOR, MOV, MVN, ORR, RSB, RSC, SBC, SUB, TEQ, TST | S | +I si contienen SHIFT(Rs) +S +N si se escribe el PC |
| MSR, MRS | S | - |
| LDR | S + N + I | +S +N si se escribe el PC |
| STR | 2N | - |
| LDM | nS + N + I | +S +N si se escribe el PC |
| STM | (n-1)S + 2N | - |
| SWP | S + 2N + I | - |
| B, BL, BX, SWI | 2S + N | - |
| MUL | S + mI | - |
| MLA, MULL, MLAL | S + (m+1) I | - |
| CDP | S + bl | - |
| LDC, STC | (n-1)S + 2N + bl | - |
| MCR | N + bl + C | - |
| MRC | S + (b+1)I + C | - |
| cualquiera no ejecutada (condición falsa) | S | - |

- n = número de palabras transferidas
- b = número de ciclos de espera por coprocesador ocupado
- m = {1, 2, 3} si los bits [31:{8,16,24}] del multiplicador son todos 0 ó 1; 4 en otro caso

ARM7TDMI Core

excepciones



- Existen **7 tipos de excepciones/interrupciones** en el ARM7TDMI y todas son vectorizadas.

- Cuando se producen, se salta a una dirección fija (vector) dependiente del tipo de excepción/interrupción producida.

| Address | Exception | Mode in Entry |
|------------|-----------------------|---------------|
| 0x00000000 | Reset | Supervisor |
| 0x00000004 | Undefined instruction | Undefined |
| 0x00000008 | Software Interrupt | Supervisor |
| 0x0000000C | Abort (prefetch) | Abort |
| 0x00000010 | Abort (data) | Abort |
| 0x00000014 | Reserved | Reserved |
| 0x00000018 | IRQ | IRQ |
| 0x0000001C | FIQ | FIQ |

- Si se producen **simultáneamente** existe un mecanismo fijo de arbitraje:
 - Reset > Data Abort > FIQ > IRQ > Prefecth Abort > Undefined Instruction, SWI
- Latencias:
 - **FIQ:** máxima = 28 ciclos, mínima = 4 ciclos
 - **IRQ:** iguales a FIQ + tiempo arbitrario (debido a la ejecución de la ISR de FIQ) en el caso de que se produzca una FIQ inmediatamente a continuación

ARM7TDMI Core

excepciones

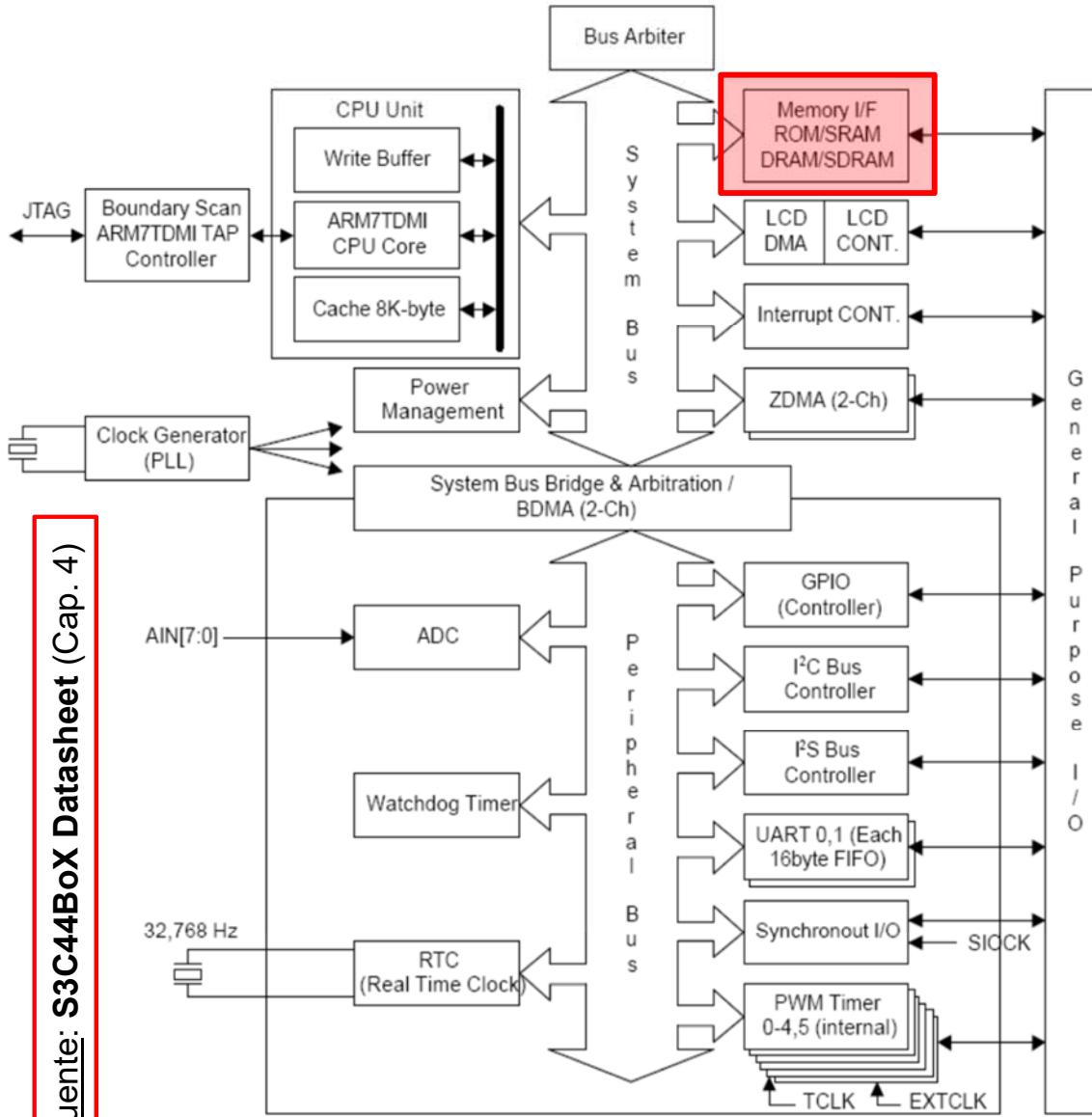


- Cuando se produce una excepción/interrupción, el ARM7TDMI:
 - Copia la dirección de las siguiente instrucción en LR_<modo>
 - Copia el CPSR en SPSR_<modo>
 - Modifica adecuadamente el CPSR
 - Pasa a estado ARM (T=0), pasa <modo> y deshabilita interrupciones
 - Carga el PC con la dirección indicada por el vector
- Al finalizar el tratamiento de excepción, la ISR debe ejecutar una instrucción MOVS/SUBS que :
 - Restaure el CPSR con el valor de SPSR_<modo>
 - Restaure el PC con el valor de LR_<modo> corregido según el tipo de excepción

| | Return Instruction | Previous State | |
|-------|----------------------|----------------|-------------|
| | | ARM R14_x | THUMB R14_x |
| BL | MOV PC, R14 | PC + 4 | PC + 2 |
| SWI | MOVS PC, R14_svc | PC + 4 | PC + 2 |
| UDEF | MOVS PC, R14_und | PC + 4 | PC + 2 |
| FIQ | SUBS PC, R14_fiq, #4 | PC + 4 | PC + 4 |
| IRQ | SUBS PC, R14_irq, #4 | PC + 4 | PC + 4 |
| PABT | SUBS PC, R14_abt, #4 | PC + 4 | PC + 4 |
| DABT | SUBS PC, R14_abt, #8 | PC + 8 | PC + 8 |
| RESET | NA | - | - |



Controlador de memoria



- Configurable mediante 13 registros mapeados en memoria (banco 0).

que permiten:

- Indicar el tipo de memorias conectadas al sistema
- Fijar la temporización del ciclo de acceso de cada memoria

Los 13 registros deben ser escritos en bloque usando una instrucción STMIA

Controlador de memoria

espacio de direcciones (i)

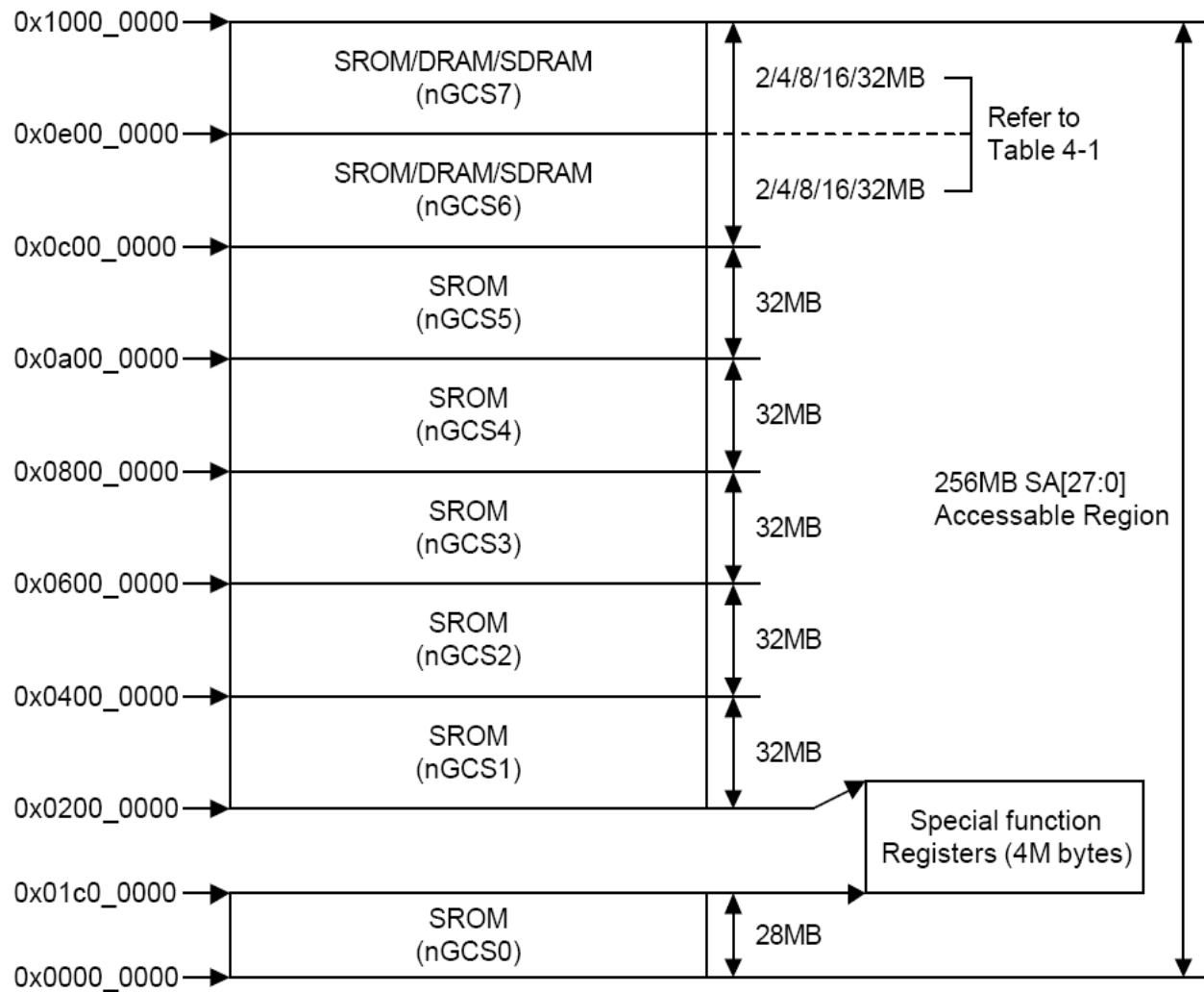


- El S3C44B0X puede direccionar hasta 256 MB organizados en 8 bancos de 32MB.
 - 6 bancos para ROM/SRAM
 - 2 bancos para ROM/SRAM/DRAM/SDRAM
 - Cada banco se selecciona por una señal nGCS0-7 obtenida decodificando los 3 bits más significativos de la dirección (A27, A26, A25).
 - El número de ciclos de acceso, anchura y profundidad de cada banco es programable.
 - La dirección de comienzo es fija en todos los bancos menos en el 7 que es programable.
 - Soporta auto refresco de DRAM/SDRAM en power-down
- El sistema accede al banco 0 (booting ROM bank) tras reset.
 - Su anchura es seleccionable según el valor de los pines OM[1:0] tras reset.
 - En su último tramo (4MB) están mapeados todos los registros de configuración de los controladores internos de periféricos.
 - El modo de acceso al resto de bancos debe programarse antes de su uso.



Controlador de memoria

espacio de direcciones (ii)



NOTE: SROM means ROM or SRAM type memory



Controlador de memoria

configuración: registro BWSCON (i)



- 0x01C80000 (**BWSCON – Bus Width & Wait Control**)
 - 32b, R/W, reset = 0x00000000
 - Para cada banco, configura el ancho del bus de datos, des/habilita la línea de petición de prolongación del ciclo de acceso y fija el modo de selección de byte en SRAM.

| BWSCON | Bit | Description | Initial state |
|--------|---------|--|---------------|
| ST3 | [15] | This bit determines SRAM for using UB/LB for bank 3 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0]) | 0 |
| WS3 | [14] | This bit determines WAIT status for bank 3 0 = WAIT disable 1 = WAIT enable | 0 |
| DW3 | [13:12] | These two bits determine data bus width for bank 3 00 = 8-bit 01 = 16-bit, 10 = 32-bit | 0 |
| ST2 | [11] | This bit determines SRAM for using UB/LB for bank 2 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0]) | 0 |
| WS2 | [10] | This bit determines WAIT status for bank 2 0 = WAIT disable 1 = WAIT enable | 0 |
| DW2 | [9:8] | These two bits determine data bus width for bank 2 00 = 8-bit 01 = 16-bit, 10 = 32-bit | 0 |
| ST1 | [7] | This bit determines SRAM for using UB/LB for bank 1 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0]) | 0 |
| WS1 | [6] | This bit determines WAIT status for bank 1 0 = WAIT disable, 1 = WAIT enable | 0 |
| DW1 | [5:4] | These two bits determine data bus width for bank 1 00 = 8-bit 01 = 16-bit, 10 = 32-bit | 0 |
| DW0 | [2:1] | Indicates data bus width for bank 0 (read only) 00 = 8-bit 01 = 16-bit, 10 = 32-bit The states are selected by OM[1:0] pins | - |
| ENDIAN | [0] | Indicates endian mode (read only) 0 = Little endian 1 = Big endian The states are selected by ENDIAN pins | - |



Controlador de memoria

configuración: registro BWSCON (ii)

| BWSCON | Bit | Description | Initial state |
|--------|---------|--|---------------|
| ST7 | [31] | This bit determines SRAM for using UB/LB for bank 7 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0]) | 0 |
| WS7 | [30] | This bit determines WAIT status for bank 7 (If bank7 has DRAM or SDRAM, WAIT function is not supported) 0 = WAIT disable 1 = WAIT enable | 0 |
| DW7 | [29:28] | These two bits determine data bus width for bank 7 00 = 8-bit 01 = 16-bit, 10 = 32-bit | 0 |
| ST6 | [27] | This bit determines SRAM for using UB/LB for bank 6 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0]) | 0 |
| WS6 | [26] | This bit determines WAIT status for bank 6 (If bank6 has DRAM or SDRAM, WAIT function is not supported) 0 = WAIT disable, 1 = WAIT enable | 0 |
| DW6 | [25:24] | These two bits determine data bus width for bank 6 00 = 8-bit 01 = 16-bit, 10 = 32-bit | 0 |
| ST5 | [23] | This bit determines SRAM for using UB/LB for bank 5 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0]) | 0 |
| WS5 | [22] | This bit determines WAIT status for bank 5 0 = WAIT disable, 1 = WAIT enable | 0 |
| DW5 | [21:20] | These two bits determine data bus width for bank 5 00 = 8-bit 01 = 16-bit, 10 = 32-bit | 0 |
| ST4 | [19] | This bit determines SRAM for using UB/LB for bank 4 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0]) | 0 |
| WS4 | [18] | This bit determines WAIT status for bank 4 0 = WAIT disable 1 = WAIT enable | 0 |
| DW4 | [17:16] | These two bits determine data bus width for bank 4 00 = 8-bit 01 = 16-bit, 10 = 32-bit | 0 |



Controlador de memoria

configuración: registros BANKCON0-5

- 0x01C80004 - 0x01C80018 (**BANKCON0-5 – Bank Control**)
 - 15b, R/W, reset = 0x0700
 - Fija de la temporización del ciclo de acceso de los bancos 0 al 5.

| BANKCONn | Bit | Description | Initial State |
|----------|---------|---|---------------|
| Tacs | [14:13] | Address set-up before nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks | 00 |
| Tcos | [12:11] | Chip selection set-up nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks | 00 |
| Tacc | [10:8] | Access cycle 000 = 1 clock 001 = 2 clocks 010 = 3 clocks 011 = 4 clocks 100 = 6 clocks 101 = 8 clocks 110 = 10 clocks 111 = 14 clocks | 111 |
| Toch | [7:6] | Chip selection hold on nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks | 000 |
| Tcah | [5:4] | Address holding time after nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks | 00 |
| Tpac | [3:2] | Page mode access cycle @ Page mode 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 6 clocks | 00 |
| PMC | [1:0] | Page mode configuration 00 = normal (1 data) 01 = 4 data 10 = 8 data 11 = 16 data | 00 |

Controlador de memoria

configuración: registros BANKCON6-7 (i)



- 0x01C8001C - 0x01C80020 (**BANKCON6-7 – Bank Control**)
 - 17b, R/W, reset = 0x18008
 - Indica el tipo de memoria y fija la temporización del ciclo de acceso a los bancos 6 y 7.

| BANKCONn | Bit | Description | Initial State |
|----------|---------|--|---------------|
| MT | [16:15] | These two bits determine the memory type for bank6 and bank7 00 = ROM or SRAM 01 = FP DRAM 10 = EDO DRAM 11 = Sync. DRAM | 11 |

| Memory Type = FP DRAM [MT=01] or EDO DRAM [MT=10] (6-bit) | | | |
|---|-------|---|----|
| Trcd | [5:4] | RAS to CAS delay 00 = 1 clock 01 = 2 clocks 10 = 3 clocks 11 = 4 clocks | 00 |
| Tcas | [3] | CAS pulse width 0 = 1 clock 1 = 2 clocks | 0 |
| Tcp | [2] | CAS pre-charge 0 = 1 clock 1 = 2 clocks | 0 |
| CAN | [1:0] | Column address number 00 = 8-bit 01 = 9-bit 10 = 10-bit 11 = 11-bit | 00 |

| Memory Type = SDRAM [MT=11] (4-bit) | | | |
|-------------------------------------|-------|---|----|
| Trcd | [3:2] | RAS to CAS delay 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks | 10 |
| SCAN | [1:0] | Column address number 00 = 8-bit 01 = 9-bit 10 = 10-bit | 00 |

Controlador de memoria

configuración: registros BANKCON6-7 (ii)



| Memory Type = ROM or SRAM [MT=00] (15-bit) | | | | | | |
|--|---------|---|--------|--|-----|--|
| Tacs | [14:13] | Address set-up before nGCS 00 = 0 clock 01 = 1 clock 10 = 2 clocks clocks | 11 = 4 | | 00 | |
| Tcos | [12:11] | Chip selection set-up nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks clocks | 11 = 4 | | 00 | |
| Tacc | [10:8] | Access cycle 000 = 1 clock 001 = 2 clocks 010 = 3 clocks 011 = 4 clocks 100 = 6 clocks 101 = 8 clocks 110 = 10 clocks 111 = 14 clocks | | | 111 | |
| Toch | [7:6] | Chip selection hold on nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks | | | 00 | |
| Tcah | [5:4] | Address hold time on nGCSn 00 = 0 clock 01 = 1clock 10 = 2 clocks 11 = 4 clocks | | | 00 | |
| Tpac | [3:2] | Page mode access cycle @ Page mode 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 6 clocks | | | 00 | |
| PMC | [1:0] | Page mode configuration 00 = normal (1 data) 01 = 4 consecutive accesses 10 = 8 consecutive accesses 11 = 16 consecutive accesses | | | 00 | |



Controlador de memoria

configuración: registro REFRESH

- 0x01C80024 (**REFRESH – Refresh Control**)
 - 24b, R/W, reset = 0xAC0000
 - Activa el refresco automático de la memoria DRAM/SDRAM y fija su temporización.

| REFRESH | Bit | Description | Initial State |
|-----------------|---------|---|---------------|
| REFEN | [23] | DRAM/SDRAM Refresh Enable 0 = Disable 1 = Enable(self or CBR/auto refresh) | 1 |
| TREFMD | [22] | DRAM/SDRAM Refresh Mode 0 = CBR/Auto Refresh 1 = Self Refresh In self-refresh time, the DRAM/SDRAM control signals are driven to the appropriate level. | 0 |
| Trp | [21:20] | DRAM/SDRAM RAS pre-charge Time DRAM : 00 = 1.5 clocks 01 = 2.5 clocks 10 = 3.5 clocks 11 = 4.5 clocks SDRAM : 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = Not support | 10 |
| Trc | [19:18] | SDRAM RC minimum Time 00 = 4 clocks 01 = 5 clocks 10 = 6 clocks 11 = 7 clocks | 11 |
| Tchr | [17:16] | CAS Hold Time(DRAM) 00 = 1 clock 01 = 2 clocks 10 = 3 clocks 11 = 4 clocks | 00 |
| Reserved | [15:11] | Not use | 0000 |
| Refresh Counter | [10:0] | DRAM/SDRAM refresh count value. Please, refer to chap. 6 DRAM refresh controller bus priority section. Refresh period = $(2^{11}-\text{refresh_count}+1)/\text{MCLK}$ Ex) If refresh period is 15.6 us and MCLK is 60 MHz, the refresh count is as follows; refresh count = $2^{11} + 1 - 60 \times 15.6 = 1113$ | 0 |

Controlador de memoria

configuración: registro BANKSIZE



- 0x01C80028 (**BANKSIZE - Banksize**)
 - 5b, R/W, reset = 0x00
 - Indica la profundidad de las memorias del banco 6 y 7.

| BANKSIZE | Bit | Description | Initial State |
|----------|-------|--|---------------|
| SCLKEN | [4] | SCLK will be generated only during SDRAM access cycle. This feature will reduce the power consumption. 1 is recommended. 0 = normal SCLK 1 = SCLK for reducing power consumption | 0 |
| Reserved | [3] | Not use | 0 |
| BK76MAP | [2:0] | BANK6/7 memory map 000 = 32M/32M 100 = 2M/2M 101 = 4M/4M 110 = 8M/8M 111 = 16M/16M | 000 |

Controlador de memoria

configuración: registros MRSR6-7

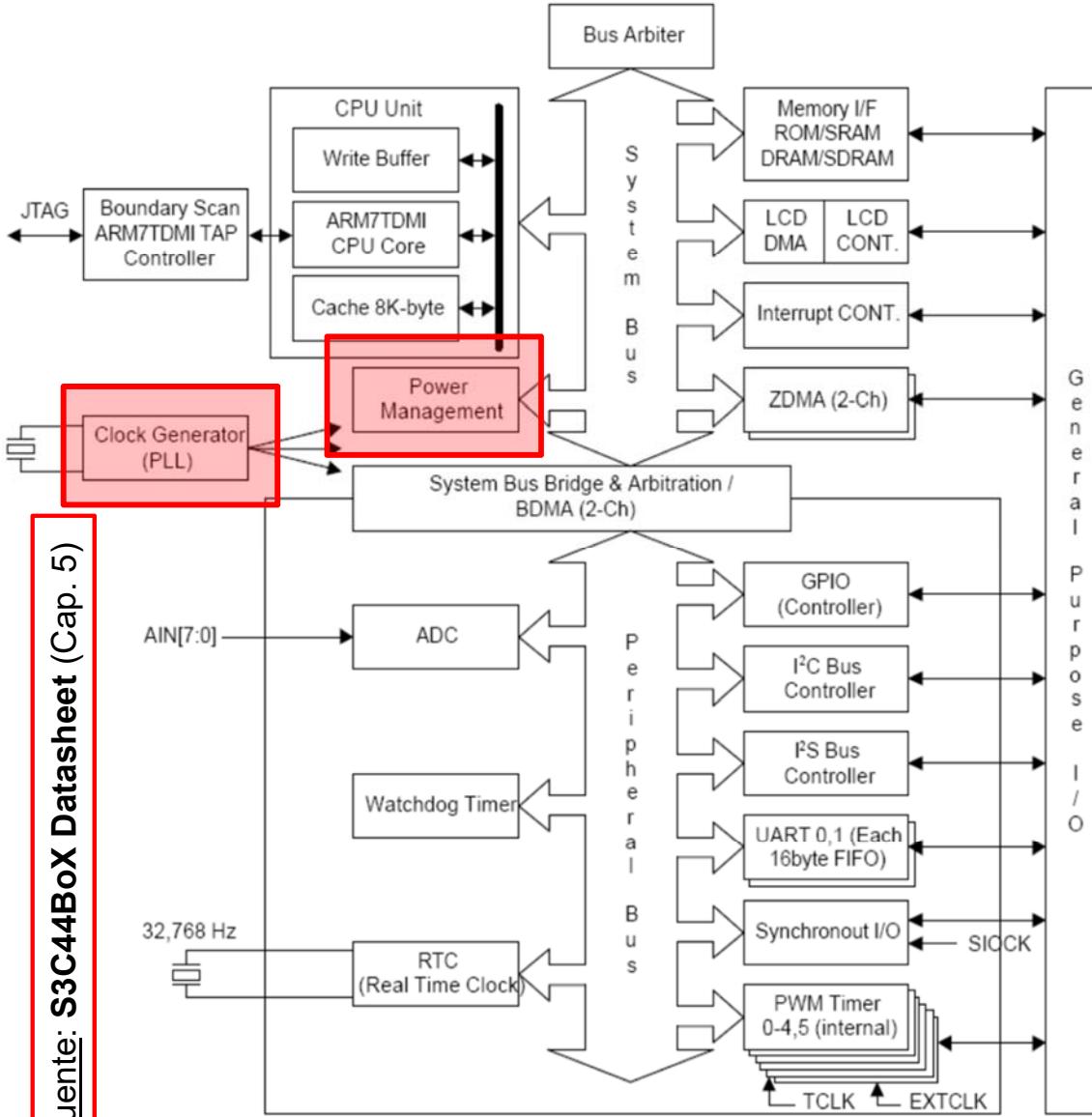


- 0x01C8002C - 0x01C80030 (**MRSRB6-7 – SDRAM Mode Set**)
 - 12b, R/W, reset = indefinido
 - Fija aspectos adicionales de la temporización del ciclo de acceso a memorias SDRAM de los bancos 6 y 7.

| MRSR | Bit | Description | Initial State |
|----------|---------|---|---------------|
| Reserved | [11:10] | Not use | - |
| WBL | [9] | Write burst length 0 is the recommended value | x |
| TM | [8:7] | Test mode 00: mode register set, 01, 10, 11: reserved | xx |
| CL | [6:4] | CAS latency 000 = 1 clock, 010 = 2 clocks, 011=3 clocks the others = reserved | xxx |
| BT | [3] | Burst type 0: Sequential (recommended) 1: N/A | x |
| BL | [2:0] | Burst length 000: 1 the others: N/A | xxx |



Gestor de reloj y energía



- Configurable mediante 4 registros mapeados en memoria (banco 0).

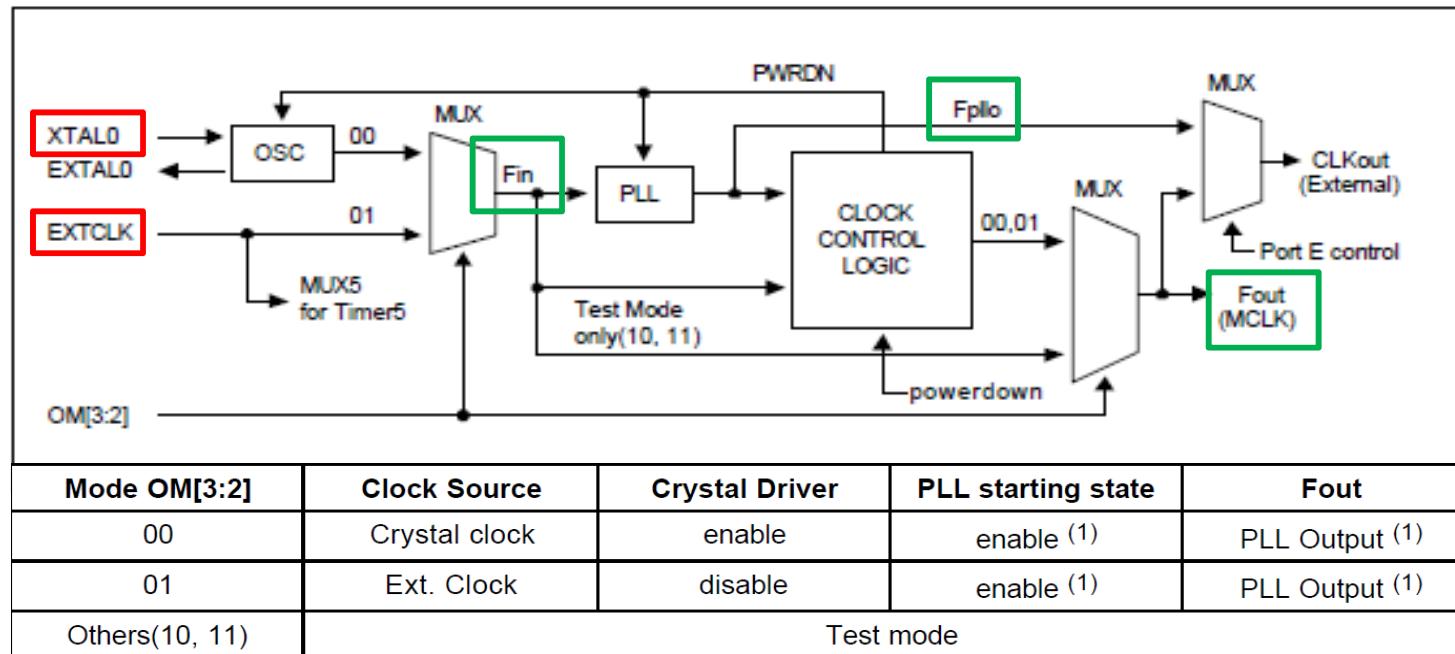
que permiten:

- Fijar la frecuencia del reloj del sistema (máx. 66MHz).
- Inhabilitar selectivamente el reloj de los controladores de periféricos.
- Comutar el sistema a modos de bajo consumo.



Gestor de reloj y energía

generación de reloj



- La **procedencia** (cristal o reloj externos) de la fuente primaria de reloj es seleccionable según el valor de los pines OM[3:2] tras reset.
- El S3C44B0X dispone de un PLL que permite programar la **frecuencia (Fout)** del reloj del sistema (MCLK):
 - Tras el reset $Fout = Fin$, $Fout$ no será $Fpilo$ hasta no se escriba el registro PPLCON.
 - Es posible variar $Fout$ en cualquier momento reprogramando PPLCON: MCLK se inhabilitará durante PLL-LOCKTIME hasta que la nueva frecuencia se estabilice.

Gestor de reloj y energía

gestión de energía (i)



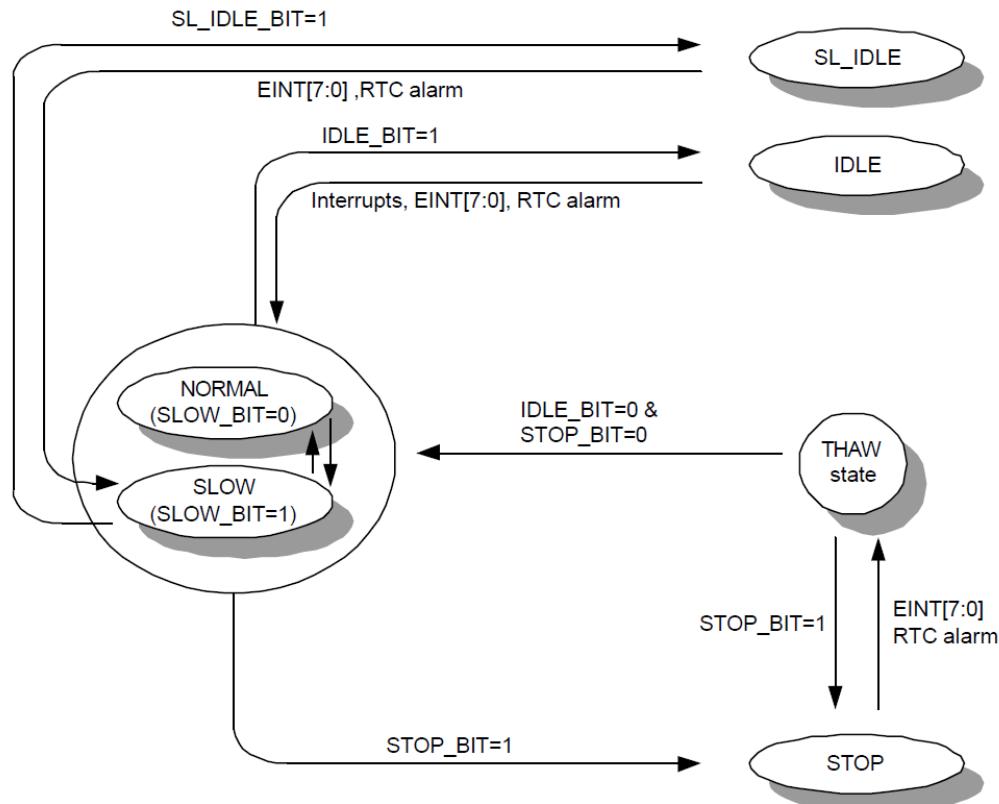
- Una gestión eficiente de energía se consigue:
 - Fijando una frecuencia del reloj del sistema adecuada.
 - Inhabilitando selectivamente la distribución del reloj a los periféricos.
 - Comutando el sistema a modos de funcionamiento de bajo consumo.
- Existen cinco modos de funcionamiento:
 - **NORMAL**: el sistema funciona a alta frecuencia: $F_{out} = F_{plo}$
 - **SLOW**: el sistema funciona a baja frecuencia: $F_{out} = Fin/(2 \times SLOW_VAL)$ y el PPL puede desabilitarse.
 - **IDLE**: se inhabilita el reloj del CPU Core (únicamente permanecen activos los controladores de bus, memoria, interrupciones y energía)
 - **SL_IDLE**: se inhabilitan todos los relojes menos el controlador de LCD.
 - la SDRAM debe estar configurada en modo de refresco automático.
 - **STOP**: se inhabilitan todos los relojes del SoC.
 - la SDRAM debe estar configurada en modo de refresco automático .



Gestor de reloj y energía

gestión de energía (ii)

- El **paso de NORMAL a otro modo** se hace escribiendo en CLKCON.
- La **vuelta a NORMAL** desde **SLOW** se hace escribiendo CLKCON.
- La **vuelta a NORMAL** desde el **resto de modos**, según el caso, se hace por interrupción interna, interrupción externa o alarma del RTC.



Gestor de reloj y energía

configuración: registros PLLCON y LOCKTIME



- 0x01D80000 (**PLLCON – PLL Control**)
 - 20b, R/W, reset = 0x38080
 - Fija la frecuencia del reloj del sistema en modo NORMAL.

| PLLCON | Bit | Description | Initial State |
|--------|---------|----------------------|---------------|
| MDIV | [19:12] | Main divider control | 0x38 |
| PDIV | [9:4] | Pre-divider control | 0x08 |
| SDIV | [1:0] | Post divider control | 0x0 |

PLL CONTROL REGISTER (PLLCON)

$$F_{pillo} = (m * F_{in}) / (p * 2^s)$$

$$m = (MDIV + 8), \quad p = (PDIV + 2), \quad s = SDIV$$

NOTE: F_{pillo} must be greater than 20Mhz and less than 68Mhz.

PLL VALUE SELECTION GUIDE

1. $F_{pillo} * 2^s$ has to be less than 170 MHz.
2. S should be as great as possible.
3. (F_{in} / p) is recommended to be 1Mhz or above. But, $(F_{in} / p) < 2$ Mhz.

- 0x01D8000C (**LOCKTIME – Lock Time Count**)
 - 12b, R/W, reset = 0xFFFF
 - Fija el tiempo de espera por estabilización del PLL ($>208 \mu s$)

| LOCKTIME | Bit | Description | Initial State |
|-----------|--------|---------------------------|---------------|
| LTIME CNT | [11:0] | PLL lock time count value | 0xffff |

$$t_{lock}(\text{the PLL lock time by H/W logic}) = (1/F_{in}) \times n, \quad (n = LTIMECNT \text{ value})$$

Gestor de reloj y energía

configuración y operación: registro CLKCON



| CLKCON | Bit | Description | Initial State |
|----------|------|---|---------------|
| IIS | [14] | Controls MCLK into IIS block 0 = Disable, 1 = Enable | 1 |
| IIC | [13] | Controls MCLK into IIC block 0 = Disable, 1 = Enable | 1 |
| ADC | [12] | Controls MCLK into ADC block 0 = Disable, 1 = Enable | 1 |
| RTC | [11] | Controls MCLK into RTC control block. Even if this bit is cleared to 0, RTC timer is alive. 0 = Disable, 1 = Enable | 1 |
| GPIO | [10] | Controls MCLK into GPIO block Set to 1 to use interrupt requests by EINT[4:7] 0 = Disable, 1 = Enable | 1 |
| UART1 | [9] | Controls MCLK into UART1 block 0 = Disable, 1 = Enable | 1 |
| UART0 | [8] | Controls MCLK into UART0 block 0 = Disable, 1 = Enable | 1 |
| BDMA0,1 | [7] | Controls MCLK into BDMA block 0 = Disable, 1 = Enable (If BDMA is turned off, the peripherals in the peripheral bus may not be accessed) | 1 |
| LCDC | [6] | Controls MCLK into LCDC block 0 = Disable, 1 = Enable | 1 |
| SIO | [5] | Controls MCLK into SIO block 0 = Disable, 1 = Enable | 1 |
| ZDMA0,1 | [4] | Controls MCLK into ZDMA block 0 = Disable, 1 = Enable | 1 |
| PWMTIMER | [3] | Controls MCLK into PWMTIMER block 0 = Disable, 1 = Enable | 1 |
| IDLE BIT | [2] | Enters IDLE mode. This bit can't be cleared automatically. 0 = Disable, 1 = Transition to IDLE(SL_IDLE) mode | 0 |
| SL_IDLE | [1] | SL_IDLE mode option. This bit can't be cleared automatically. 0 = Disable, 1 = SL_IDLE mode. To enter SL_IDLE mode, CLKCON register has to be 0x46. | 0 |
| STOP BIT | [0] | Enters STOP mode. This bit can't be cleared automatically. 0 = Disable, 1 = Transition to STOP mode | 0 |

- 0x01D80004
(CLKCON – Clock Control)
 - 15b, R/W, reset = 0x7FF8
 - Regula la distribución del reloj a los controladores periféricos y permite comutar del modo NORMAL a modos de inactividad.

Gestor de reloj y energía

configuración y operación: registro CLKSLOW



- 0x01D80008 (**CLKSLOW – Clock Slow**)
 - 6b, R/W, reset = 0x09
 - Permite comutar entre los modos SLOW y NORMAL, fijar la frecuencia del reloj del sistema en modo SLOW y apagar el PLL.

| CLKSLOW | Bit | Description | Initial State |
|----------|-------|--|---------------|
| PLL_OFF | [5] | <p>0 : PLL is turned on. PLL is turned on only when SLOW_BIT is 1. After PLL stabilization time (minimum 150uS), SLOW_BIT may be cleared to 0.</p> <p>1 : PLL is turned off. PLL is turned off only when SLOW_BIT is 1.</p> | 0x0 |
| SLOW_BIT | [4] | <p>0 : $F_{out} = F_{p1lo}$ (PLL output)</p> <p>1: $F_{out} = F_{in} / (2 \times SLOW_VAL)$, ($SLOW_VAL > 0$) $F_{out} = F_{in}$, ($SLOW_VAL = 0$)</p> | 0x0 |
| SLOW_VAL | [3:0] | The divider value for the slow clock when SLOW_BIT is on. | 0x9 |

Gestor de reloj y energía

consumo medio



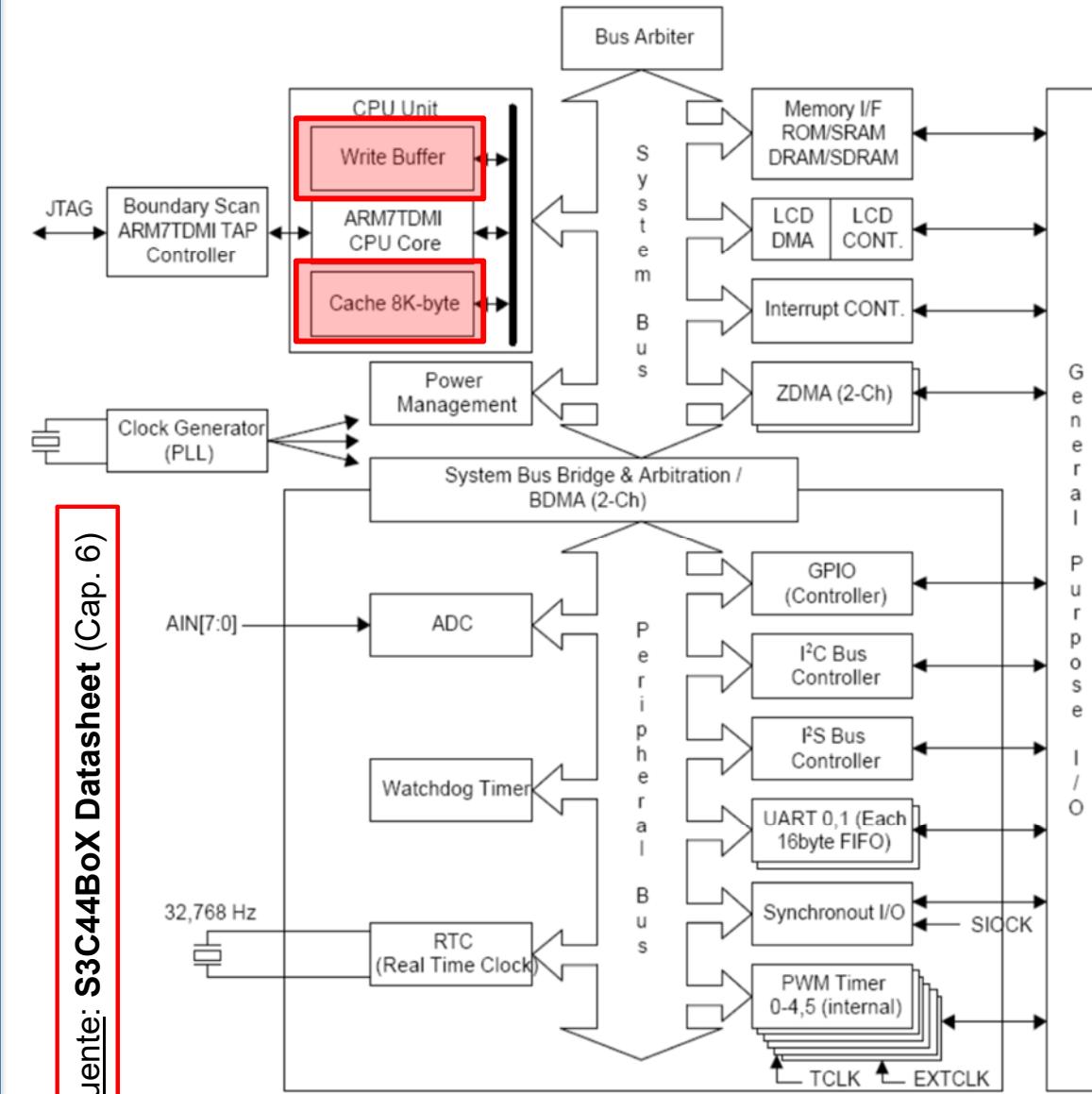
(TA = 0 to 70 °C)

| Item | Symbol | Min | Typ | Max | Unit | Remarks |
|------------------------|-------------|-----|-----|----------------|------|---|
| Normal operation | I_{DDCPU} | – | 60* | 80 | mA | * : 66MHz |
| Idle mode | | | 23* | 28 | | Both oscillators running, CPU static, LCD refresh active |
| ** Slow mode(@1MHz) | | | 2.1 | – | | ** : Total current consumption. (CPU+I/O) |
| ** SL-Idle mode(@1MHz) | I_{TOTAL} | – | 1 | uA (@25 °C) | | Just running 32KHz oscillator(for RTC), all other I/O static. |
| ** Stop mode | | | 5 | | | |
| RTC consumption | I_{RTC} | – | 2 | 5 | uA | x-tal = 32.768KHz for RTC |

(Unit: %)

| Peri | IIS | IIC | ADC | RTC | UART1 | SIO | ZDMA0/1 | Timer012345 | LCD | Total |
|----------------|------|------|------|------|-------|------|---------|-------------|------|-------|
| Current saving | 1.3% | 1.6% | 0.7% | 0.8% | 3.8% | 0.9% | 2.2% | 2.2% | 3.2% | 16.7 |

| Tipo de pila | CR1212 | CR1620 | CR2032 | Alcalina AAA | Alcalina AA | Ion Li |
|-----------------|--------|--------|--------|--------------|-------------|--------|
| Capacidad (mAh) | 18 | 75 | 220 | 1250 | 2890 | 850 |



- Configurable mediante 3 **registros** mapeados en memoria (banco 0).

que permiten:

- Habilitar la cache
- Organizar su estructura
- Fijar las regiones de memoria no cacheables





Controlador de cache

- La CPU del S3C44B0X dispone de **8KB de memoria SRAM** interna que puede ser configurada como:
 - **8KB de cache** unificada (instrucciones y datos) asociativa por conjuntos de 4 vías.
 - **4KB de cache** unificada asociativa por conjuntos de 2 vías + **4KB de scratchpad**.
 - **8KB de scratchpad** (**opción tras reset**).
- Cuando se **configura como cache** (8/4 KB):
 - Se organiza en líneas de 16B (4 palabras), con emplazamiento asociativo por conjuntos de 4/2 vías, reemplazamiento LRU y escritura inmediata con un write buffer de 4 referencias.
 - Todos los bloques pueden invalidarse (flushing) cuando estando deshabilitada se escribe 0 en la región de la SRAM donde se hayan los registros de edad LRU.
 - Pueden especificarse 2 regiones de **memoria como no cacheables** (la línea de cache no se actualiza cuando hay un fallo de lectura).
 - Para mantener coherencia deben marcarse aquellas zonas de memoria que puedan cambiar su contenido sin intervención directa de la CPU: buffers DMA, dispositivos externos mapeados en memoria...

Controlador de cache



- Cuando se configura como scratchpad:
 - Puede accederse normalmente a la memoria usada para implementar los distintos elementos que forman la cache.
 - Si el scratchpad es de 8KB, se puede acceder a la SRAM completa.
 - Si el scratchpad es de 4 KB, solo se puede acceder a la región de SRAM usada por los conjuntos 2 y 3.

| Area(Set/Cache) | Memory Map Address | Size |
|-----------------|-------------------------|-----------------|
| cache set 0 | 0x10000000 - 0x100007ff | 2KB |
| cache set 1 | 0x10000800 - 0x10000fff | 2KB |
| cache set 2 | 0x10001000 - 0x100017ff | 2KB |
| cache set 3 | 0x10001800 - 0x10001fff | 2KB |
| cache tag 0 | 0x10002000 - 0x100027f0 | 512bytes (note) |
| cache tag 1 | 0x10002800 - 0x10002ff0 | 512bytes (note) |
| cache tag 2 | 0x10003000 - 0x100037f0 | 512bytes (note) |
| cache tag 3 | 0x10003800 - 0x10003ff0 | 512bytes (note) |
| LRU | 0x10004000 - 0x100047f0 | 512bytes (note) |

NOTE: The cache tag3:0 & LRU must be read/written by word access (32bit). The address bit[3:0] of .tag & LRU must be 0. For example, if you want to read the 2nd item among 128 cache tag 0 items, you should not read the address 0x10002004, but 0x10002010. Therefore, the tag0 addresses are 0x10002000, 0x10002010, 0x10002020,..., 0x100027f0.

- Dado que el acceso a la SRAM es de un ciclo, suele usarse para almacenar rutinas/datos de uso frecuente y que requieran un acceso rápido (por ejemplo, ISR).

Controlador de cache

configuración: registro SYSCONF



- 0x01C00000 (**SYSCFG – System Configuration**)
 - 8b, R/W, reset = 0x01,
 - Fija la organización de la memoria cache.

| SYSCFG | Bit | Description | Initial State |
|---------------|-------|---|---------------|
| Reserved | [7] | Reserved to 0 | 0 |
| Reserved | [6] | Reserved to 0 | 0 |
| DA(reserved) | [5] | DATA ABORT controls. This bit is recommended to be 0. 0: Enable data abort 1: Disable data abort | 0 |
| RSE(reserved) | [4] | Enable read stall option. This bit is recommended to be 0. 0: read stall disable 1: read stall enable (Read stall option: Insert one internal wait cycle when reading data for cache & CPU core.) | 0 |
| WE | [3] | This bit determines write buffer enable / disable. Some external devices, which require the minimum writing cycle time, do not operate normally because the period between consecutive writings is shortened the write buffer. 0 = Disable write buffer operation 1 = Enable write buffer operation | 0 |
| CM | [2:1] | These two bits determine cache mode 00 = Disable cache (8KB internal SRAM) 01 = Half cache enable (4KB cache, 4KB internal SRAM) 10 = Reserved 11 = Full Cache enable (8KB cache) | 00 |
| SE | [0] | Enable stall option. This bit is recommended to be 0. 0:stall disable 1:stall enable (Stall option: Insert one internal wait cycle when a non-sequential address is generated for caching) | 1 |



Controlador de cache

configuración: registros nCACHBEx

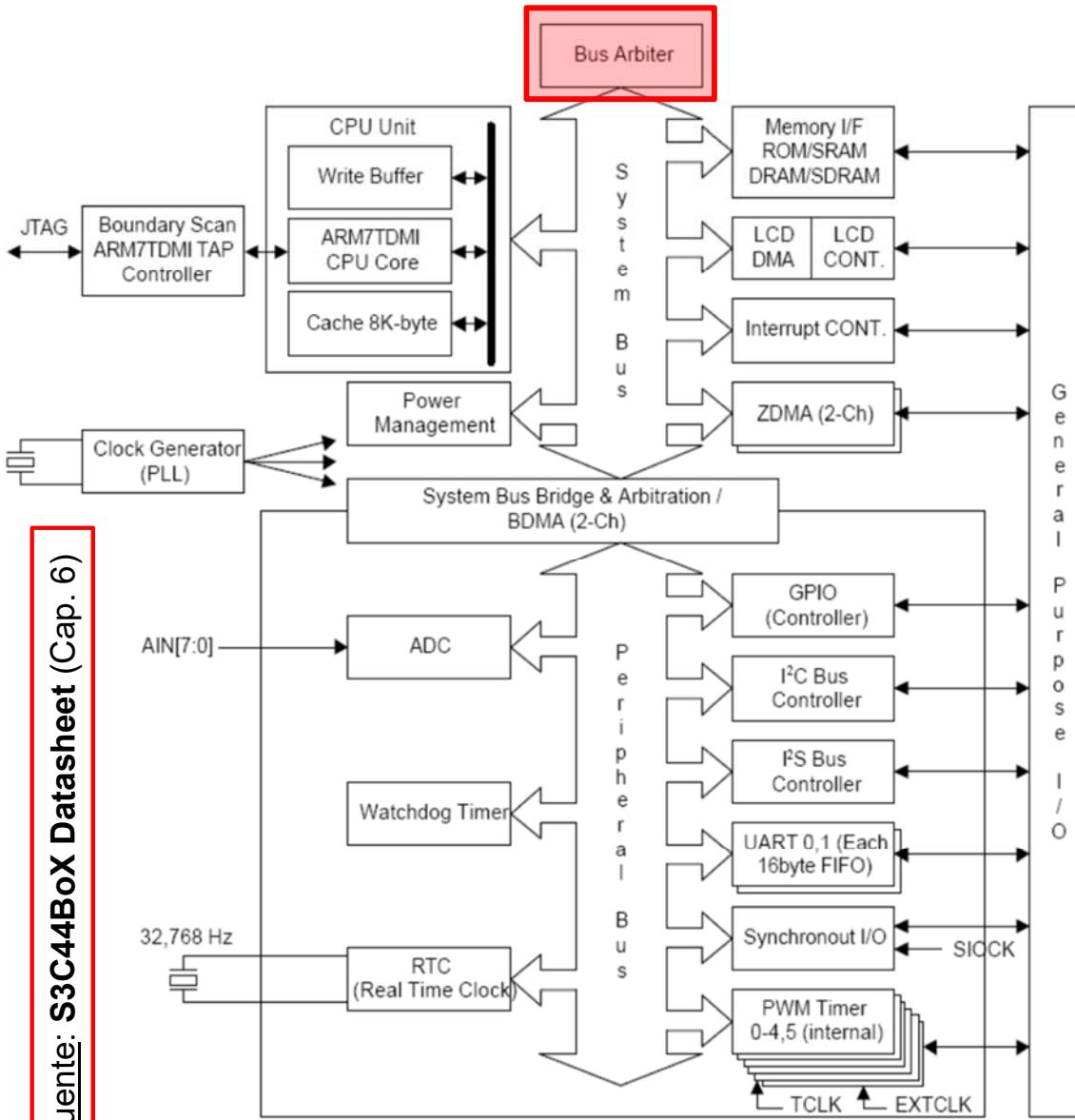
- 0x01C00004 (**NCACHBE0 – Non-Cacheable Area Control**)
- 0x01C00008 (**NCACHBE1 – Non-Cacheable Area Control**)
 - 32b, R/W, reset = 0x00000000
 - Establece la dirección de comienzo y final de un área no cacheable de memoria (en bloques contiguos de 16 KB) .

| NCACHBE0 | Bit | Description | Initial State |
|----------|---------|--|---------------|
| SE0 | [31:16] | End address of non-cacheable area 0. These 16 bits provide the end address of non-cacheable area 0. The minimum non-cacheable area is 4 Kbytes. $SE0 = (\text{End address} + 1)/4K$ | 0x0000 |
| SA0 | [15:0] | Start address of non-cacheable area 0. These 16 bits provide the start address of non-cacheable area 0. $SA0 = \text{Start address}/4K$ | 0x0000 |

| NCACHBE1 | Bit | Description | Initial State |
|----------|---------|---|---------------|
| SE1 | [31:16] | End address of non-cacheable area 1 These 16 bits provide the end address of non-cacheable area 1. The minimum non-cacheable area is 4Kbytes. $SE1 = (\text{End address} + 1)/4K$ | 0x0000 |
| SA1 | [15:0] | Start address of non-cacheable area 1. These 16 bits provide the start address of non-cacheable area 1. The minimum non-cacheable area is 4Kbytes. $SA1 = \text{Start address}/4K$ | 0x0000 |



Árbitro de bus



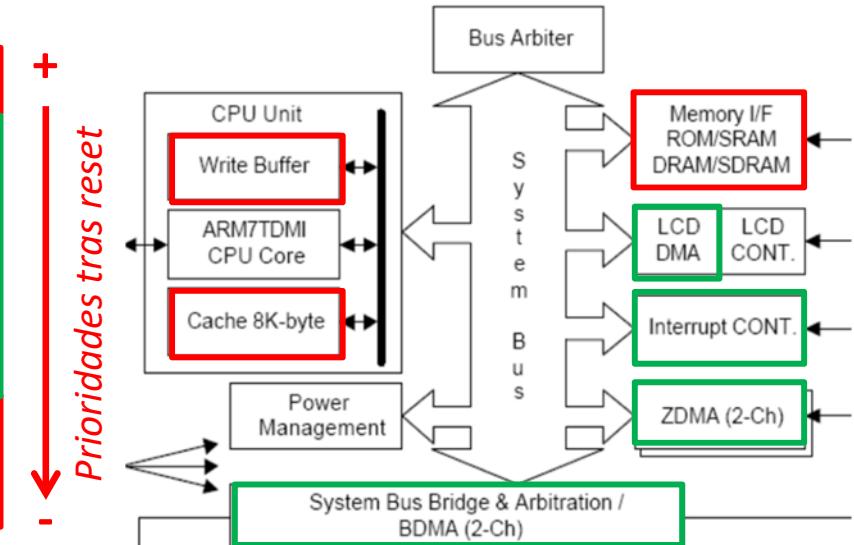
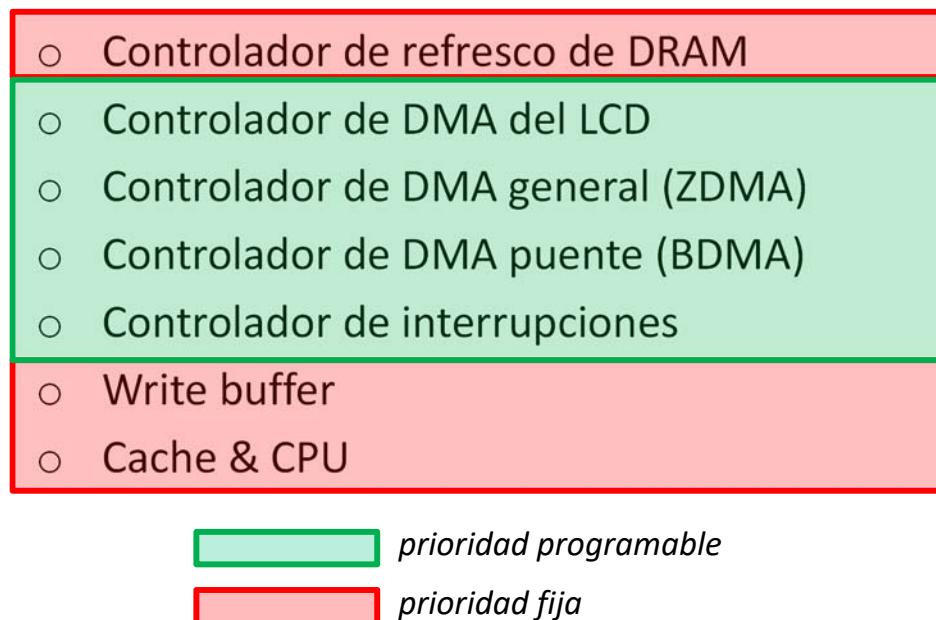
fuente: S3C44B0x Datasheet (Cap. 6)

- Configurable mediante 1 registro mapeado en memoria (banco 0).
- que permite:
- Fijar la prioridad relativa de servicio de cada uno de los maestros conectados al bus del sistema.



Árbitro de bus

- El bus del sistema del S3C44B0X tiene 7 maestros:



- Las prioridades relativas entre algunos de ellos es programable y puede ser:
 - **fija**: los másteres siempre se sirven en el orden programado.
 - **rotatoria**: el master que ha sido servido pasa a tener la mínima prioridad.

Árbitro de bus

configuración: registro SBUSCON



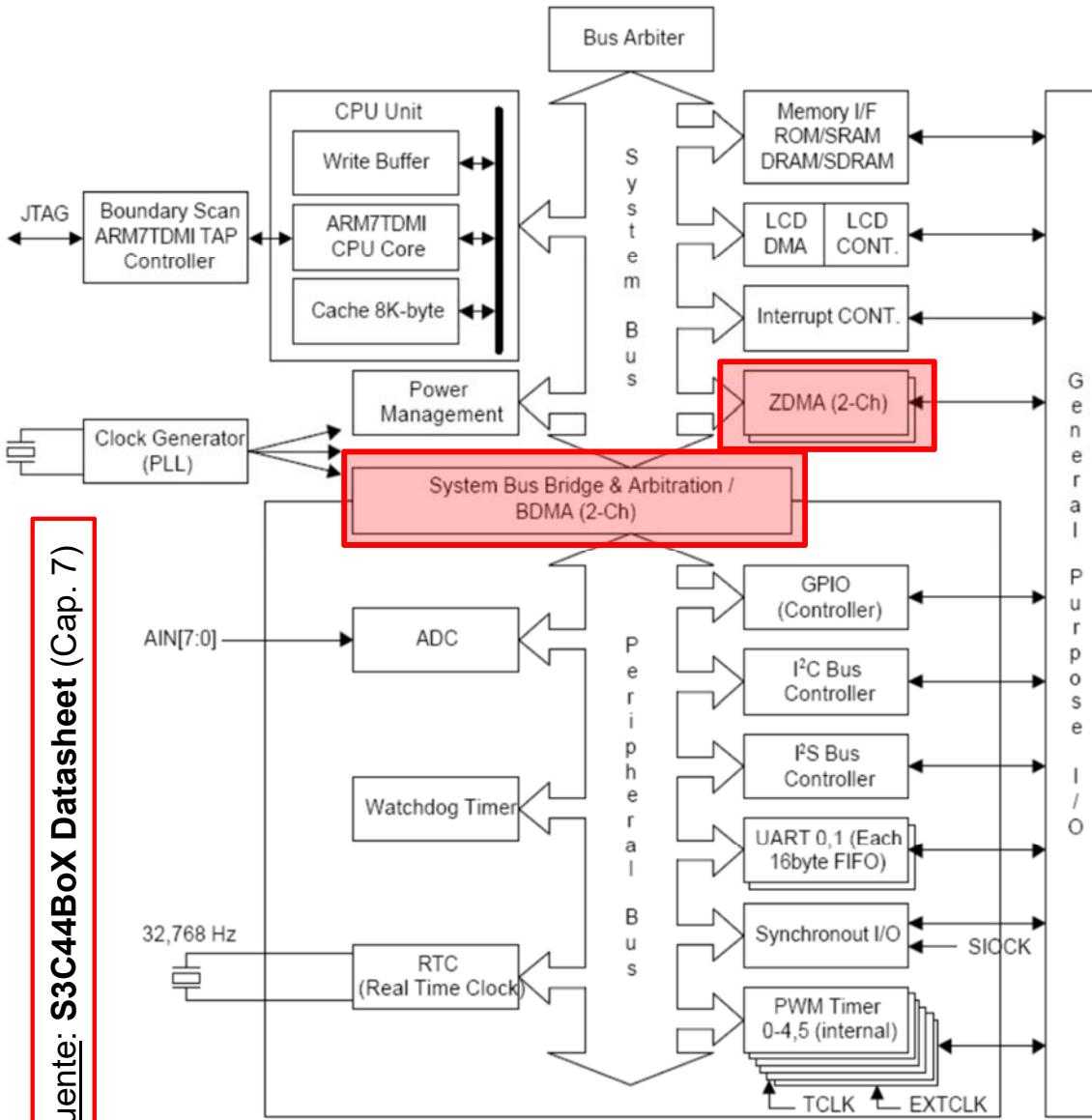
- 0x01C40000 (**SBUSCON – System Bus Priority**)
 - 32b, R/W, reset = 0x80001B1B
 - Permite establecer la prioridad relativa entre 4 de los másteres que comparten el bus del sistema y si las prioridades son fijas o rotatorias. Asimismo indica la prioridad relativa existente entre los másteres.

| SBUSCON | Bit | Description | Initial State |
|-----------|---------|---|---------------|
| FIX | [31] | 0: round-robin priorities 1: fixed priorities | 0x1 |
| S_LCD_DMA | [15:14] | Indicates the LCD_DMA bus priority (read only) 00: 1st 01: 2nd 10: 3rd 11: 4th | 00 |
| S_ZDMA | [13:12] | Indicates the ZDMA bus priority (read only) 00: 1st 01: 2nd 10: 3rd 11: 4th | 01 |
| S_BDMA | [11:10] | Indicates the BDMA bus priority (read only) 00: 1st 01: 2nd 10: 3rd 11: 4th | 10 |
| S_nBREQ | [9:8] | Indicates the nBREQ bus priority (read only) 00: 1st 01: 2nd 10: 3rd 11: 4th | 11 |
| LCD_DMA | [7:6] | Determines the LCD_DMA bus priority 00: 1st 01: 2nd 10: 3rd 11: 4th | 00 |
| ZDMA | [5:4] | Determines the ZDMA bus priority 00: 1st 01: 2nd 10: 3rd 11: 4th | 01 |
| BDMA | [3:2] | Determines the BDMA bus priority 00: 1st 01: 2nd 10: 3rd 11: 4th | 10 |
| nBREQ | [1:0] | Determines the nBREQ bus priority 00: 1st 01: 2nd 10: 3rd 11: 4th | 11 |

NOTE: The priorities are only valid in the fixed priority mode.



Controlador de DMA



- Configurable mediante **28 registros** mapeados en memoria (banco 0).

que permiten:

- Configurar el modo de funcionamiento de cada cada canal.
- Ordenar y controlar las transferencias por DMA:
 - memoria ↔ memoria
 - memoria ↔ periférico
 - periférico ↔ periférico.



Controlador de DMA

- El S3C44B0X dispone de 2 controladores de DMA de 2 canales cada uno.
- **ZDMA: Controlador de DMA general**, conectado al bus del sistema.
 - Realiza transferencias: Memoria ↔ Memoria / Dispositivos externos.
 - Admite solicitudes de DMA de dispositivos externos a través de 2 pares de líneas:
 - XREQ0/XACK0 y XREQ1/XACK1
 - Puede configurarse el **protocolo de transferencia** de cada canal:
 - **Handshake**: cada solicitud de XREQ inicia la transferencia de un único dato en un ciclo inseparable de lectura/escritura.
 - **Single Step**: cada solicitud de XREQ inicia la transferencia de un único dato en dos ciclos separables de lectura/escritura.
 - **Whole Service**: una única solicitud de XREQ inicia una operación completa DMA (formada la transferencia en ciclos inseparables de lectura/escritura de múltiples datos). Tras cada transferencia individual el bus puede ser cedido a otros másteres.
 - **Demand**: mientras XREQ esté activa se realizan continuamente ciclos de transferencias sin ceder el bus a otros másteres.
 - Así como el **modo de transferencia**:
 - **Unit** : 1 dato leído, 1 dato escrito.
 - **Block**: 4 datos leídos en ráfaga, 4 datos escritos en ráfaga.
 - **On-the-fly**: cada dato es leído y escrito simultáneamente.

Controlador de DMA



- **BDMA:** Controlador de DMA puente, conectado al bus del sistema y al de periféricos.
 - Realiza transferencias: Memoria / Dispositivos internos ↔ Dispositivos internos
 - Solo admite solicitudes de DMA de algunos dispositivos internos:
 - controladores de UART (2 canales), SIO, ISS, Temporizadores
 - Protocolo de transferencia es fijo: **handshake**.
 - Modo de transferencia es fijo: **unit**.
- Ambos controladores:
 - Admiten inicio transferencias de DMA por SW.
 - Admiten **Auto Reload**: la posibilidad de programar los parámetros de una nueva transferencia de DMA que se inicie automáticamente (previa solicitud) una vez finalice la transferencia en curso.

Controlador DMA

configuración del ZDMA: registros ZDCONx



- 0x01E80000 (**ZDCON0 – ZDMA 0 Control**)
- 0x01E80020 (**ZDCON1 – ZDMA 1 Control**)
 - 8b, R/W, reset = 0x00
 - Permite habilitar/deshabilitar las peticiones externas de DMA, conocer el estado del canal e iniciar por SW/pausar/cancelar una operación de DMA.

| ZDCONn | Bit | Description | Initial State |
|--------|-------|---|---------------|
| INT | [7:6] | Reserved | 00 |
| STE | [5:4] | Status of DMA channel (Read only) 00 = Ready 01 = Not TC yet 10 = Terminal Count 11 = N/A Before the DMA counter decreases from the initial counter value, STE is still in the ready state. | 00 |
| QDS | [3:2] | Disable/Enable External DMA request (nXDREQ) 00 = Enable other = Disable | 00 |
| CMD | [1:0] | Software commands 00: No command. After writing 01,10,11, CMD bit is cleared automatically. nXDREQ is available. 01: Starts DMA operation by S/W without nXDREQ. S/W start function can be used only in the whole mode. As DMA is in the whole mode, the DMA will operate until the counter is 0. If nXDREQ is used, this command must not be issued. 10: Pauses DMA operation. But nXDREQ is still available. 11: Cancels DMA operation. | 00 |

NOTE: If users start the ZDMA operation by CMD=01b, the DREQ protocol must be whole service mode.



Controlador DMA

operación del ZDMA: registros ZDxSRCx

- 0x01E80004 (**ZDISRC0 – ZDMA 0 Inicial Source Address**)
 - 32b, R/W, reset = 0x00000000
 - Permite fijar la dirección origen inicial, el tamaño del dato atómico a transferir y cómo esta dirección debe cambiarse para completar la transferencia.
- 0x01E80010 (**ZDCSRC0 – ZDMA 0 Current Source Address**)
- 0x01E80030 (**ZDCSRC1 – ZDMA 1 Current Source Address**)
 - 32b, R, reset = 0x00000000
 - Indica la dirección origen actual. Se carga con el correspondiente valor de ZDISCRx cuando comienza la transferencia y se actualiza durante el transcurso de ésta.

| ZDISRCn/ZDCSRCn | Bit | Description | Initial State |
|-----------------|---------|--|---------------|
| DST | [31:30] | Data size for transfer 00 = Byte, 01 = Half word 10 = Word, 11 = Not used If the block transfer mode is used, the DST must be 10. | 00 |
| DAL | [29:28] | Direction of address for load 00 = N/A, 01 = Increment 10 = Decrement, 11 = Fixed | 00 |
| ISADDR/CSADDR | [27:0] | Initial/current source address for ZDMA | 0x00000000 |

Controlador DMA

operación del ZDMA: registros ZDxDESx



- 0x01E80008 (**ZDIDES0 – ZDMA 0 Inicial Destination Address**)
 - 32b, R/W, reset = 0x00000000
 - Permite fijar la dirección destino inicial, el tamaño de la transferencia y cómo esta dirección debe cambiarse para completar la transferencia.
- 0x01E80014 (**ZDCDES0 – ZDMA 0 Current Destination Address**)
- 0x01E80034 (**ZDCDES1 – ZDMA 1 Current Destination Address**)
 - 32b, R, reset = 0x00000000
 - Indica la dirección destino actual. Se carga con el correspondiente valor de ZDIDESx cuando comienza la transferencia y se actualiza durante el transcurso de ésta.

| ZDIDESn/ZDCDESn | Bit | Description | Initial State |
|-----------------|---------|--|---------------|
| OPT | [31:30] | DMA internal options. OPT = 10 is recommended. bit 31: Indicates how nXDREQ is sampled in the single step mode. 1 is recommended. bit 30: If the DST is half-word or word and if the DMA mode is not the block transfer mode, this bit takes a role. 1: DMA does word-swap or half-word swap Before transfer: B0,B1,B2,B3,B4,B5,B6,B7... word-swapped data: B3,B2,B1,B0,B7,B6,B5,B4,... half-word-swapped data: B1,B0,B3,B2,B5,B4,B7,B6,... 0: normal | 00 |
| DAS | [29:28] | Direction of address for store 00 = N/A 01 = Increment 10 = Decrement 11 = Fixed | 00 |
| IDADDR/CDADDR | [27:0] | Initial/current destination address for ZDMA _n | 0x00000000 |

Controlador DMA

operación del ZDMA: registros ZDxCNTx (i)



- 0x01E8000C (**ZDICNT0 – ZDMA 0 Inicial Count**)
- 0x01E8002C (**ZDICNT1 – ZDMA 1 Inicial Count**)
 - 32b, R/W, reset = 0x00000000
 - Permite fijar la fuente, protocolo y modo de la transferencia DMA, el comportamiento del controlador al finalizar la ésta y el número inicial de bytes a transferir
- 0x01E80018 (**ZDCCNT0 – ZDMA 0 Current Count**)
- 0x01E80038 (**ZDCCNT1 – ZDMA 1 Current Count**)
 - 32b, R, reset = 0x00000000
 - Indica el número actual de bytes transferidos.



Controlador DMA

operación del ZDMA: registros ZDxCNTx (ii)



| ZDICNTn/ZDCCNTn | Bit | Description | Initial State |
|-----------------|---------|--|---------------|
| QSC | [31:30] | DREQ(DMA request) source selection 00 = nXDREQ[0] 01 = nXDREQ[1] 10 = N/A 11 = N/A | 00 |
| QTY | [29:28] | DREQ protocol 00 = Handshake 01 = Single step 10 = Whole Service 11 = Demand | 00 |
| TMD | [27:26] | Transfer mode 00 = Not used 01 = Unit transfer mode 10 = Block(4-word) transfer mode 11 = On the fly If block transfer mode is selected, the ADDR[3:0] should be '0' to meet 16-byte align condition. | 00 |
| OTF | [25:24] | On the fly mode 00 = N/A 01 = N/A 10 = Read time on the fly 11 = Write time on the fly | 00 |
| INTS | [23:22] | Interrupt mode set 00 = Polling mode 01 = N/A 10 = Int. whenever transferred 11 = Int. whenever terminated count | 00 |
| AR | [21] | Auto-reload and Auto-start after DMA count are 0. 0 = Disable 1 = Enable. Even after DMA count is 0, the DMA H/W enable bit (EN bit) is still 1. But, DMA will start to operate only if the start command or nXDREQ is activated. | 0 |
| EN | [20] | DMA H/W enable/disable 0 = Disable DMA 1 = Enable DMA. If the QDS bit is 00b, DMA request can be serviced. Also if the S/W command is started, the DMA operation will occur. If the EN bit is 0, DMA will not operate even though S/W command is started. If the S/W command is canceled, the DMA operation will be canceled and EN bit will be cleared to 0. At the terminal count, the EN bit will be cleared to 0. NOTE: Do not set the EN bit and the other bits of ZDICNT register at the same time. User have to set EN bit after setting the other bits of ZDICNT register as following steps, 1. Set ZDICNT register with disabled En bit. 2. Set EN bit enable. | 0 |
| ICNT/CCNT | [19:0] | Initial/current transfer count for ZDMA <i>n</i> . If 1 byte is transferred, the ICNT will be decreased by 1. If 1 half-word is transferred, the ICNT will be decreased by 2. If 1 word is transferred, the ICNT will be decreased by 4. For example, if the data size of a transfer is word and the count is 4n+3, the last 3 bytes will not be transferred. | 0x00000 |



Controlador DMA

configuración del BDMA: registros BDCONx

- 0x01F80000 (**BDCON0 – BDMA 0 Control**)
- 0x01F80020 (**BDCON1 – BDMA 1 Control**)
 - 8b, R/W, reset = 0x00
 - Permite habilitar/deshabilitar las peticiones internas de DMA, conocer el estado del canal y cancelar una operación de DMA.

| BDCONn | Bit | Description | Initial State |
|--------|-------|--|---------------|
| INT | [7:6] | Reserved | 00 |
| STE | [5:4] | Status of DMA channel (Read only) 00 = Ready 01 = Not TC yet 10 = Terminal Count 11 = N/A Before the DMA counter decreases from a initial counter value, STE is still the ready state. | 00 |
| QDS | [3:2] | Disable/Enable External/Internal DMA request (UARTn, SIO, IIS, Timer) 00 = Enable Other = Disable | 00 |
| CMD | [1:0] | Software commands 00: No command. After writing 01, 10, 11, CMD bits are cleared automatically. 01: Reserved 10: Reserved 11: Cancels DMA operation. | 00 |

Controlador DMA

operación del BDMA: registros BDxSRCx



- 0x01F80004 (**BDISRC0 – BDMA 0 Inicial Source Address**)
 - 0x01F80024 (**BDISRC1 – BDMA 1 Inicial Source Address**)
 - 32b, R/W, reset = 0x00000000
 - Permite fijar la dirección origen inicial, el tamaño del dato atómico a transferir y cómo esta dirección debe cambiarse para completar la transferencia.
- 0x01F80010 (**BDCSRC0 – BDMA 0 Current Source Address**)
- 0x01F80030 (**BDCSRC1 – BDMA 1 Current Source Address**)
 - 32b, R, reset = 0x00000000
 - Indica la dirección origen actual. Se carga con el correspondiente valor de BDISCRx cuando comienza la transferencia y se actualiza durante el transcurso de ésta.

| BDISRCn/BDCSRCn | Bit | Description | Initial State |
|------------------------|------------|---|----------------------|
| DST | [31:30] | Data size for transfer 00 = Byte 01 = Half word 10 = Word 11 = Not used | 00 |
| DAL | [29:28] | Direction of address for load 00 = N/A 01 = Increment 10 = Decrement 11 = Internal peripheral (fixed address) | 00 |
| ISADDR/CSADDR | [27:0] | Initial/current source address for BDMA _n . If the destination is the internal peripherals, the SFR address has to be used. For example, if the source is the UART0 Rx buffer, the UART0 Rx buffer address will be used. | 0x00000000 |

Controlador DMA

operación del BDMA: registros BDxDESx



- 0x01F80008 (**BDIDES0 – BDMA 0 Inicial Destination Address**)
- 0x01F80028 (**BDIDES1 – BDMA 1 Inicial Destination Address**)
 - 32b, R/W, reset = 0x00000000
 - Permite fijar la dirección destino inicial, el sentido de la transferencia y cómo esta dirección debe cambiarse para completar la transferencia.
- 0x01F80014 (**BDCDES0 – BDMA 0 Current Destination Address**)
- 0x01F80034 (**BDCDES1 – BDMA 1 Current Destination Address**)
 - 32b, R, reset = 0x00000000
 - Indica la dirección destino actual. Se carga con el correspondiente valor de BDIDESx cuando comienza la transferencia y se actualiza durante el transcurso de ésta.

| BDIDESn/BDCDESn | Bit | Description | Initial State |
|-----------------|---------|---|---------------|
| TDM | [31:30] | Transfer direction mode 00 = Reserved 01 = M2IO (from external memory to internal peripheral) 10 = IO2M (from internal peripheral to external memory) 11 = IO2IO (from internal peripheral to internal peripheral) NOTE: The initial value is '00', but you must change TDM value as another though the BDMA channel is unused. | 00 |
| DAS | [29:28] | Direction of address for store 00 = N/A 01 = Increment 10 = Decrement 11 = Internal peripheral (fixed address) | 00 |
| IDADDR/CDADDR | [27:0] | Initial/current destination address for BDMA If the destination is the internal peripherals, the SFR address has to be used. For example, if the destination is UART0 Tx buffer, the UART0 Tx buffer address will be used. | 0x00000000 |



Controlador DMA

operación del BDMA: registros BDxCNTx (i)

- 0x01F8000C (**BDICNT0 – BDMA 0 Inicial Count**)
- 0x01F8002C (**BDICNT1 – BDMA 1 Inicial Count**)
 - 32b, R/W, reset = 0x00000000
 - Permite fijar la fuente y modo de la transferencia DMA, el comportamiento del controlador al finalizar la ésta y el número inicial de bytes a transferir
- 0x01F80018 (**BDCCNT0 – BDMA 0 Current Count**)
- 0x01F80038 (**BDCCNT1 – BDMA 1 Current Count**)
 - 32b, R, reset = 0x00000000
 - Indica el número actual de bytes a transferir.

Controlador DMA

operación del BDMA: registros BDxCNT0 (ii)



| BDICNT0/BDCCNT0 | Bit | Description | Initial State |
|------------------------|------------|--|----------------------|
| QSC | [31:30] | DMA request source selection 00 = N/A 01 = IIS 10 = UART0 11 = SIO | 00 |
| Reserved | [29:28] | 00: handshake mode | 00 |
| Reserved | [27:26] | 01: unit transfer mode | 01 |
| Reserved | [25:24] | 00: on-the-fly mode is not supported in BDMA | 00 |
| INTS | [23:22] | Interrupt mode set 00 = Polling mode 01 = N/A 10 = Int. whenever transferred 11 = Int. whenever terminated count | 00 |
| AR | [21] | Auto-reload and Auto-start after DMA count are 0. 0= Disable 1= Enable. Even after DMA count is 0, the DMA H/W enable bit (EN bit) is still 1. But, DMA will start to operate only if the start command or DMA request is activated | 0 |
| EN | [20] | DMA H/W enable/disable 0 = Disable DMA 1 = Enable DMA. If the QDS bit is 00b, DMA request can be serviced. Also if the S/W command is started, the DMA operation will occur. If the EN bit is 0, DMA will not operate even though S/W command is started. If the S/W command is canceled, the DMA operation will be canceled and EN bit will be cleared to 0. At the terminal count, the EN bit will be cleared to 0. NOTE: Do not set the EN bit and the other bits of BDICNT register at the same time. User have to set EN bit after setting the other bits of BDICNT register as following steps, 1. Set BDICNT register with disabled En bit. 2. Set EN bit enable. | 0 |
| ICNT/CCNT | [19:0] | Transfer count for BDMA0. The transfer count must be right value. For example, if DST is word, ICNT must be 4n. If 1 byte is transferred, the ICNT will be decreased by 1. If 1 half-word is transferred, the ICNT will be decreased by 2. If 1 word is transferred, the ICNT will be decreased by 4. | 0x00000 |



Controlador DMA

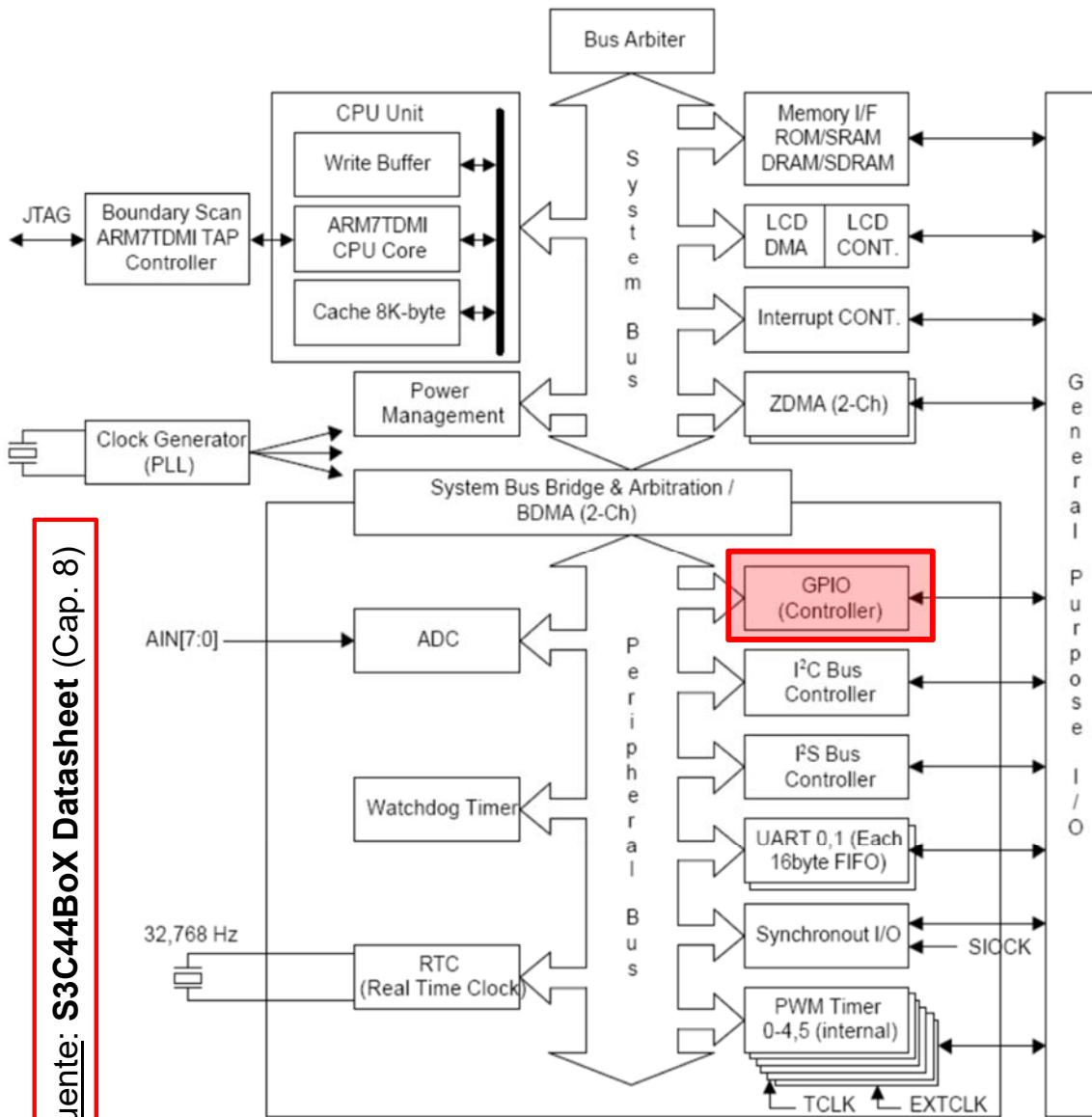
operación del BDMA: registros BDxCNT1 (iii)



| BDICNT1/BDCCNT1 | Bit | Description | Initial State |
|------------------------|------------|--|----------------------|
| QSC | [31:30] | DMA request source selection 00 = N/A 01 = Timer 10 = UART1 11 = SIO | 00 |
| Reserved | [29:28] | 00: handshake mode | 00 |
| Reserved | [27:26] | 01: unit transfer mode | 01 |
| Reserved | [25:24] | 00: on-the-fly mode is not supported in BDMan | 00 |
| INTS | [23:22] | Interrupt mode set 00 = Polling mode 01 = N/A 10 = Int. whenever transferred 11 = Int. whenever terminated count | 00 |
| AR | [21] | Auto-reload and Auto-start after DMA count are 0. 0= Disable 1= Enable. Even after DMA count is 0, the DMA H/W enable bit (EN bit) is still 1. But, DMA will start to operate only if the start command or DMA request is activated | 0 |
| EN | [20] | DMA H/W enable/disable 0 = Disable DMA 1 = Enable DMA. If the QDS bit is 00b, DMA request can be serviced. Also if the S/W command is started, the DMA operation will occur. If the EN bit is 0, DMA will not operate even though S/W command is started. If the S/W command is canceled, the DMA operation will be canceled and EN bit will be cleared to 0. At the terminal count, the EN bit will be cleared to 0. NOTE: Do not set the EN bit and the other bits of BDICNT register at the same time. User have to set EN bit after setting the other bits of BDICNT register as following steps, 1. Set BDICNT register with disabled En bit. 2. Set EN bit enable. | 0 |
| ICNT/CCNT | [19:0] | Transfer count for BDMA1. The transfer count must be right value. For example, if DST is word, ICNT must be 4n. If 1 byte is transferred, the ICNT will be decreased by 1. If 1 half-word is transferred, the ICNT will be decreased by 2. If 1 word is transferred, the ICNT will be decreased by 4. | 0x00000 |



Controlador de pines de E/S



- Configurable mediante 22 registros mapeados en memoria (banco 0).

que permiten:

- Fijar la función de algunos los pines multiplexados del sistema



Controlador de pines de E/S

- El S3C44B0X dispone de **71 pines multiplexados** (de un total de 160) organizados en **7 puertos** (grupos)
 - 2 puertos de solo salida (puertos A y B)
 - 5 puertos de entrada/salida (puertos C, D, E, F y G)
- Cada pin de cada puerto puede ser configurado individualmente:
 - Para estar conectado a una **línea interna** del microcontrolador
 - No pueden escribirse y si se leen se obtiene un valor indefinido.
 - Como **salida**
 - El valor del pin puede cambiarse escribiendo un bit de un registro del controlador.
 - Como **entrada**
 - El valor del pin puede conocerse leyendo un bit de un registro del controlador.
- El controlador tiene 2 registros para gestionar cada puerto:
 - **PCONx** (registro de control) que configura la funcionalidad de cada pin
 - **PDATx** (registro de datos) que permite escribir/leer un valor en el cada pin
- Adicionalmente, tiene un registro adicional para cada puerto de E/S:
 - **PUPx** que permite activar/desactivar (0/1) la resistencia de pull-up de $50\text{K}\Omega$ interna que tiene cada pin.

Controlador de pines de E/S

configuración y operación: puerto A



- Puerto de solo salida de 10 bits.
- 0x01D20000 (**PCONA – Port A Control**)
 - 10b, R/W, inicial = 0x3FF
- 0x01D20004 (**PDATA – Port A Data**)
 - 10b, R/W, inicial = indefinido

| PCONA | Bit | Description | |
|-------|-----|-------------|------------|
| PA9 | [9] | 0 = Output | 1 = ADDR24 |
| PA8 | [8] | 0 = Output | 1 = ADDR23 |
| PA7 | [7] | 0 = Output | 1 = ADDR22 |
| PA6 | [6] | 0 = Output | 1 = ADDR21 |
| PA5 | [5] | 0 = Output | 1 = ADDR20 |
| PA4 | [4] | 0 = Output | 1 = ADDR19 |
| PA3 | [3] | 0 = Output | 1 = ADDR18 |
| PA2 | [2] | 0 = Output | 1 = ADDR17 |
| PA1 | [1] | 0 = Output | 1 = ADDR16 |
| PA0 | [0] | 0 = Output | 1 = ADDR0 |

Controlador de pines de E/S

configuración y operación: puerto B



- Puerto de solo salida de 11 bits.
- 0x01D20008 (**PCONB – Port B Control**)
 - 11b, R/W, inicial = 0x7FF
- 0x01D2000C (**PDATB – Port B Data**)
 - 11b, R/W, inicial = indefinido

| PCONB | Bit | Description | |
|-------|------|-------------|---------------------|
| PB10 | [10] | 0 = Output | 1 = nGCS5 |
| PB9 | [9] | 0 = Output | 1 = nGCS4 |
| PB8 | [8] | 0 = Output | 1 = nGCS3 |
| PB7 | [7] | 0 = Output | 1 = nGCS2 |
| PB6 | [6] | 0 = Output | 1 = nGCS1 |
| PB5 | [5] | 0 = Output | 1 = nWBE3/nBE3/DQM3 |
| PB4 | [4] | 0 = Output | 1 = nWBE2/nBE2/DQM2 |
| PB3 | [3] | 0 = Output | 1 = nSRAS/nCAS3 |
| PB2 | [2] | 0 = Output | 1 = nSCAS/nCAS2 |
| PB1 | [1] | 0 = Output | 1 = SCLK |
| PB0 | [0] | 0 = Output | 1 = SCKE |

Controlador de pines de E/S

configuración y operación: puerto C



- Puerto de entrada/salida de 16 bits.
- 0x01D20010 (**PCONC – Port C Control**)
 - 32b, R/W, inicial = 0xAAAAAAA
- 0x01D20014 (**PDATC – Port C Data**)
 - 16b, R/W, inicial = indefinido
- 0x01D20018 (**PUPC – Port C Pull-up Disable**)
 - 16b, R/W, inicial = 0x0000

| PCONC | Bit | Description | | |
|-------|---------|---------------------------|-----------------------------|--|
| PC15 | [31:30] | 00 = Input 10 = DATA31 | 01 = Output 11 = nCTS0 | |
| PC14 | [29:28] | 00 = Input 10 = DATA30 | 01 = Output 11 = nRTS0 | |
| PC13 | [27:26] | 00 = Input 10 = DATA29 | 01 = Output 11 = RxD1 | |
| PC12 | [25:24] | 00 = Input 10 = DATA28 | 01 = Output 11 = TxD1 | |
| PC11 | [23:22] | 00 = Input 10 = DATA27 | 01 = Output 11 = nCTS1 | |
| PC10 | [21:20] | 00 = Input 10 = DATA26 | 01 = Output 11 = nRTS1 | |
| PC9 | [19:18] | 00 = Input 10 = DATA25 | 01 = Output 11 = nXDREQ1 | |
| PC8 | [17:16] | 00 = Input 10 = DATA24 | 01 = Output 11 = nXDACK1 | |

| PCONC | Bit | Description | | |
|-------|---------|---------------------------|-----------------------------|--|
| PC7 | [15:14] | 00 = Input 10 = DATA23 | 01 = Output 11 = VD4 | |
| PC6 | [13:12] | 00 = Input 10 = DATA22 | 01 = Output 11 = VD5 | |
| PC5 | [11:10] | 00 = Input 10 = DATA21 | 01 = Output 11 = VD6 | |
| PC4 | [9:8] | 00 = Input 10 = DATA20 | 01 = Output 11 = VD7 | |
| PC3 | [7:6] | 00 = Input 10 = DATA19 | 01 = Output 11 = IISCLK | |
| PC2 | [5:4] | 00 = Input 10 = DATA18 | 01 = Output 11 = IISDI | |
| PC1 | [3:2] | 00 = Input 10 = DATA17 | 01 = Output 11 = IISDO | |
| PC0 | [1:0] | 00 = Input 10 = DATA16 | 01 = Output 11 = IISLRCK | |

Controlador de pines de E/S

configuración y operación: puerto D



- Puerto de **entrada/salida** de 8 bits.
- 0x01D2001C (**PCOND – Port D Control**)
 - 16b, R/W, inicial = 0x0000
- 0x01D20020 (**PDATD – Port D Data**)
 - 8b, R/W, inicial = indefinido
- 0x01D20024 (**PUPD – Port D Pull-up Disable**)
 - 8b, R/W, inicial = 0x00

| PCOND | Bit | Description | | |
|-------|---------|---------------------------|------------------------------|--|
| PD7 | [15:14] | 00 = Input 10 = VFRAME | 01 = Output 11 = Reserved | |
| PD6 | [13:12] | 00 = Input 10 = VM | 01 = Output 11 = Reserved | |
| PD5 | [11:10] | 00 = Input 10 = VLIN | 01 = Output 11 = Reserved | |
| PD4 | [9:8] | 00 = Input 10 = VCLK | 01 = Output 11 = Reserved | |
| PD3 | [7:6] | 00 = Input 10 = VD3 | 01 = Output 11 = Reserved | |
| PD2 | [5:4] | 00 = Input 10 = VD2 | 01 = Output 11 = Reserved | |
| PD1 | [3:2] | 00 = Input 10 = VD1 | 01 = Output 11 = Reserved | |
| PD0 | [1:0] | 00 = Input 10 = VD0 | 01 = Output 11 = Reserved | |



Controlador de pines de E/S

configuración y operación: puerto E



- Puerto de entrada/salida de 9 bits.
- 0x01D20028 (**PCONE – Port E Control**)
 - 18b, R/W, inicial = 0x00000
- 0x01D2002C (**PDATE – Port E Data**)
 - 9b, R/W, inicial = indefinido
- 0x01D20030 (**PUPE – Port E Pull-up Disable**)
 - 9b, R/W, inicial = 0x000

| PCONE | Bit | Description | | |
|-------|---------|--|---------------|--|
| PE8 | [17:16] | 00 = Reserved(ENDIAN) | 01 = Output | |
| | | 10 = CODECLK | 11 = Reserved | |
| | | PE8 can be used as ENDIAN only during the reset cycle. | | |
| PE7 | [15:14] | 00 = Input | 01 = Output | |
| | | 10 = TOUT4 | 11 = VD7 | |
| PE6 | [13:12] | 00 = Input | 01 = Output | |
| | | 10 = TOUT3 | 11 = VD6 | |
| PE5 | [11:10] | 00 = Input | 01 = Output | |
| | | 10 = TOUT2 | 11 = TCLK in | |
| PE4 | [9:8] | 00 = Input | 01 = Output | |
| | | 10 = TOUT1 | 11 = TCLK in | |
| PE3 | [7:6] | 00 = Input | 01 = Output | |
| | | 10 = TOUT0 | 11 = Reserved | |
| PE2 | [5:4] | 00 = Input | 01 = Output | |
| | | 10 = RxDO | 11 = Reserved | |
| PE1 | [3:2] | 00 = Input | 01 = Output | |
| | | 10 = TxDO | 11 = Reserved | |
| PE0 | [1:0] | 00 = Input | 01 = Output | |
| | | 10 = Fplo out | 11 = Fout out | |

Controlador de pines de E/S

configuración y operación: puerto F



- Puerto de **entrada/salida** de 9 bits.
- 0x01D20034 (**PCONF – Port F Control**)
 - 22b, R/W, inicial = 0x0000
- 0x01D20038 (**PDATF – Port F Data**)
 - 9b, R/W, inicial = indefinido
- 0x01D2003C (**PUPF – Port F Pull-up Disable**)
 - 9b, R/W, inicial = 0x000

| PCONF | Bit | Description | | |
|-------|---------|-----------------------------|-------------------------------|----------------------------------|
| PF8 | [21:19] | 000 = Input 011 = SIOCLK | 001 = Output 100 = IISCLK | 010 = nCTS1 Others = Reserved |
| PF7 | [18:16] | 000 = Input 011 = SIORxD | 001 = Output 100 = IISDI | 010 = RxD1 Others = Reserved |
| PF6 | [15:13] | 000 = Input 011 = SIORDY | 001 = Output 100 = IISDO | 010 = TxD1 Others = Reserved |
| PF5 | [12:10] | 000 = Input 011 = SIOTxD | 001 = Output 100 = IISLRCK | 010 = nRTS1 Others = Reserved |
| PF4 | [9:8] | 00 = Input 10 = nXBREQ | 01 = Output 11 = nXDREQ0 | |
| PF3 | [7:6] | 00 = Input 10 = nXBACK | 01 = Output 11 = nXDACK0 | |
| PF2 | [5:4] | 00 = Input 10 = nWAIT | 01 = Output 11 = Reserved | |
| PF1 | [3:2] | 00 = Input 10 = IICSDA | 01 = Output 11 = Reserved | |
| PF0 | [1:0] | 00 = Input 10 = IICSCL | 01 = Output 11 = Reserved | |

Controlador de pines de E/S

configuración y operación: puerto G



- Puerto de **entrada/salida** de 8 bits.
- 0x01D20040 (**PCONG – Port G Control**)
 - 16b, R/W, inicial = 0x0000
- 0x01D20044 (**PDATG – Port G Data**)
 - 8b, R/W, inicial = indefinido
- 0x01D20048 (**PUPG – Port G Pull-up Disable**)
 - 8b, R/W, inicial = 0x00

| PCONG | Bit | Description | |
|-------|---------|----------------------------|---------------------------|
| PG7 | [15:14] | 00 = Input 10 = IISLRCK | 01 = Output 11 = EINT7 |
| PG6 | [13:12] | 00 = Input 10 = IISDO | 01 = Output 11 = EINT6 |
| PG5 | [11:10] | 00 = Input 10 = IISDI | 01 = Output 11 = EINT5 |
| PG4 | [9:8] | 00 = Input 10 = IISCLK | 01 = Output 11 = EINT4 |
| PG3 | [7:6] | 00 = Input 10 = nRTS0 | 01 = Output 11 = EINT3 |
| PG2 | [5:4] | 00 = Input 10 = nCTS0 | 01 = Output 11 = EINT2 |
| PG1 | [3:2] | 00 = Input 10 = VD5 | 01 = Output 11 = EINT1 |
| PG0 | [1:0] | 00 = Input 10 = VD4 | 01 = Output 11 = EINT0 |

Controlador de pines de E/S

configuración: registro EXINT



- 0x01D20050 (**EXTINT – External Interrupt Control**)
 - 31b, R/W, inicial = 0x00000000
 - Permite configurar el modo de señalización de las líneas externas de interrupción.

| EXTINT | Bit | Description | | | |
|--------|---------|--|-----------------------------|----------------------------|--|
| EINT7 | [30:28] | Setting the signaling method of the EINT7. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |
| EINT6 | [26:24] | Setting the signaling method of the EINT6. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |
| EINT5 | [22:20] | Setting the signaling method of the EINT5. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |
| EINT4 | [18:16] | Setting the signaling method of the EINT4. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |
| EINT3 | [14:12] | Setting the signaling method of the EINT3. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |
| EINT2 | [10:8] | Setting the signaling method of the EINT2. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |
| EINT1 | [6:4] | Setting the signaling method of the EINT1. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |
| EINT0 | [2:0] | Setting the signaling method of the EINT0. | 000 = Low level interrupt | 001 = High level interrupt | |
| | | 01x = Falling edge triggered | 10x = Rising edge triggered | | |
| | | 11x = Both edge triggered | | | |



Controlador de pines de E/S

configuración: registros EXTINTPND y SPUCR

- 0x01D20054 (**EXTINTPND – External Interrupt Pending**)
 - 4b, R/W, inicial = 0x0
 - Dado que EINT7...EINT4 comparten línea en el controlador de interrupciones, este registro indica la línea que tiene una solicitud pendiente. Una vez atendida, la RTI debe borrar el bit correspondiente escribiendo un 1 en él.

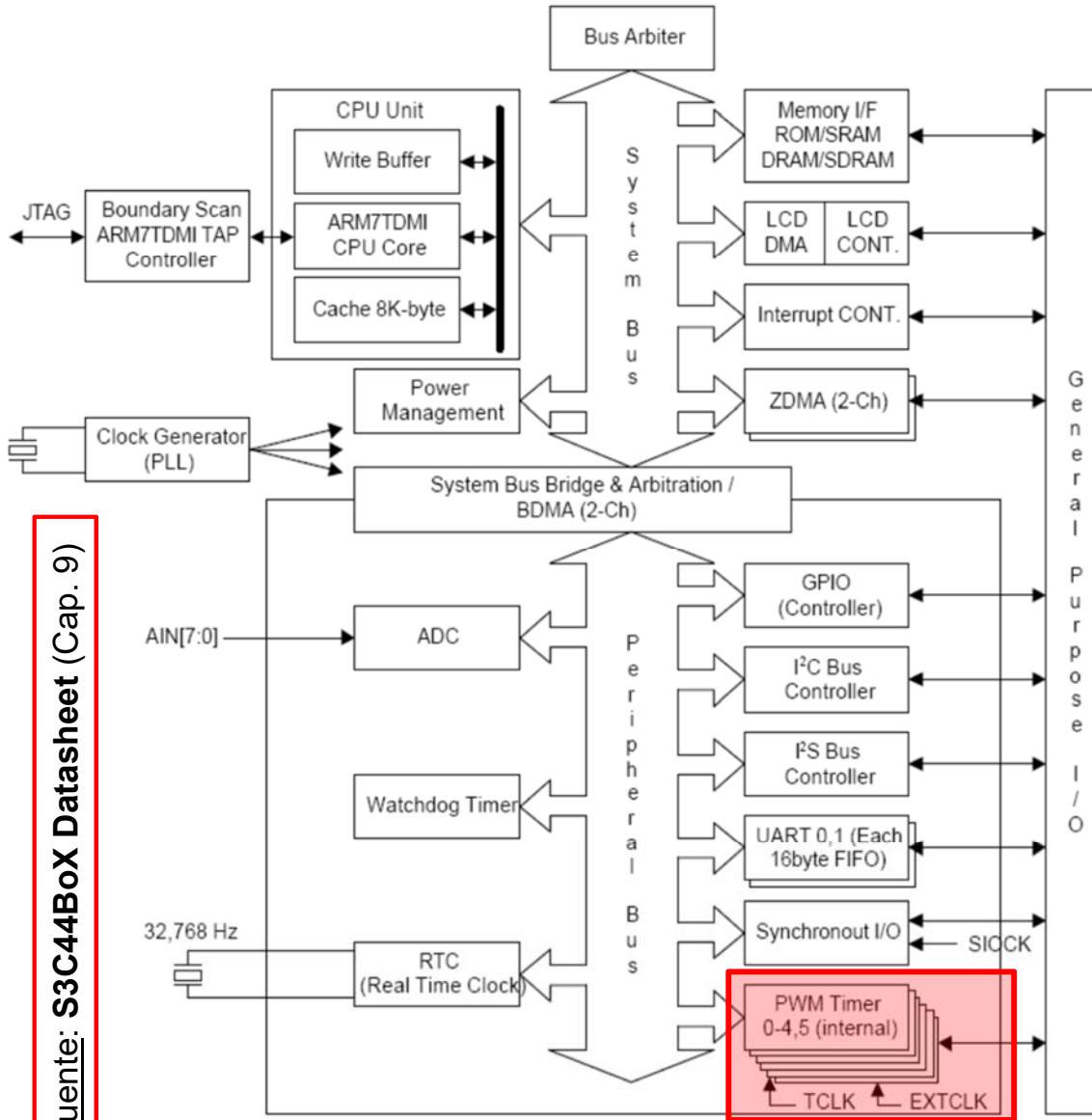
| PUPS | Bit | Description |
|------------|-----|--|
| EXTINTPND3 | [3] | If EINT7 is activated, EXINTPND3 bit is set to 1, and also INTPND[21] is set to 1. |
| EXTINTPND2 | [2] | If EINT6 is activated, EXINTPND2 bit is set to 1, and also INTPND[21] is set to 1. |
| EXTINTPND1 | [1] | If EINT5 is activated, EXINTPND1 bit is set to 1, and also INTPND[21] is set to 1. |
| EXTINTPND0 | [0] | If EINT4 is activated, EXINTPND0 bit is set to 1, and also INTPND[21] is set to 1. |

- 0x01D2004C (**SPUCR – Special Pull-up Resistor Control**)
 - 4b, R/W, inicial = 0x4
 - Permite habilitar/deshabilitar las resistencias de pull-up de la parte baja del bus de datos, así como indicar el valor de las mismas durante el modo STOP.

| PCONG | Bit | Description |
|---------|-----|---|
| HZ@STOP | [2] | 0 = Previous state of PAD 1 = HZ @ stop |
| SPUCR1 | [1] | 0 = DATA[15:8] port pull-up resistor is enabled 1 = DATA[15:8] port pull-up resistor is disabled |
| SPUCR0 | [0] | 0 = DATA[7:0] port pull-up resistor is enabled 1 = DATA[7:0] port pull-up resistor is disabled |



Temporizadores



- Configurable mediante 20 registros mapeados en memoria (banco 0).

que permiten:

- Fijar el modo de funcionamiento de cada temporizador.
- Iniciar y parar las cuentas.



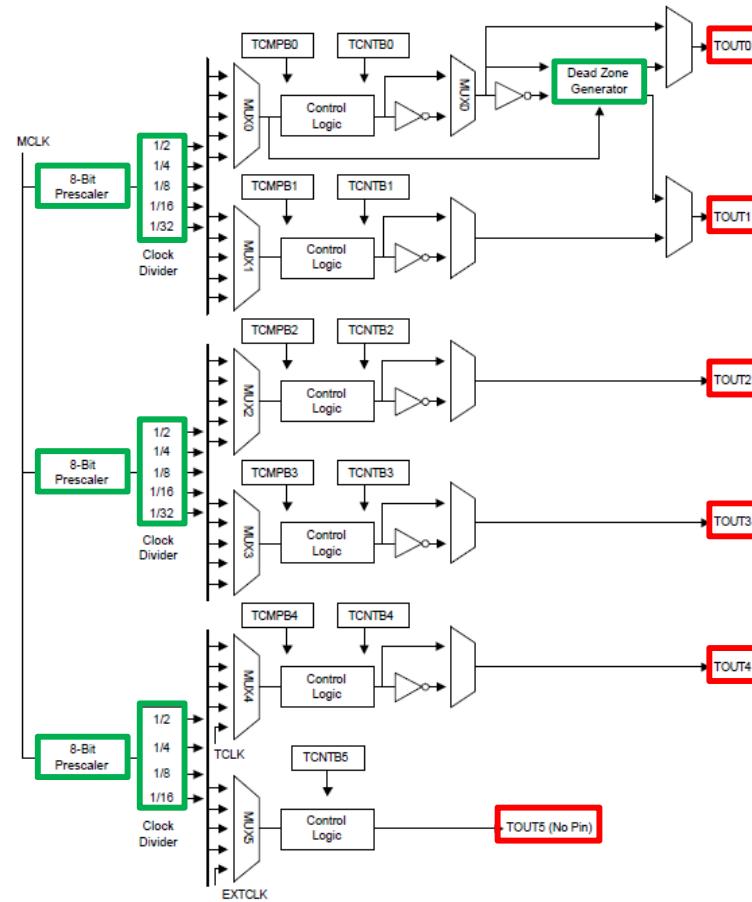
Temporizadores

- El S3C44B0X dispone de **6 temporizadores de 16 bits**, que permiten:
 - Generar una cierta forma de onda binaria distinta y no necesariamente periódica a través de 5 pines de salida (PWM: pulse width modulation)
 - Programar la generación de interrupciones/peticiones de DMA en el tiempo (con cadencias no necesariamente periódicas).
 - Medir tiempos.
- Todos los temporizadores están formados por:
 - 1 contador descendente que lleva la cuenta del temporizador (TCONx)
 - 1 registro que almacena el valor inicial de la cuenta (TCONBx)
- Además los **temporizadores 0-4** (con función PWM) disponen de:
 - 1 registro de comparación que determina el factor de trabajo de la salida (TCMPx)
 - 1 registro que almacena el valor inicial de la comparación (TCMPBx)
 - Su salida TOUTx conmuta de valor cuando TCONx alcanza el valor TCMPx.
- El **temporizador 0** tiene función de **generación de dead-zone**.
 - Cuando está activada, TOUT1 es opuesta a TOUT0 pero a cada transición de TOUT0 se añade un retardo a TOUT1 para que ambas salidas nunca estén activas simultáneamente.
- El **temporizador 5** no tiene salida al exterior.



Temporizadores

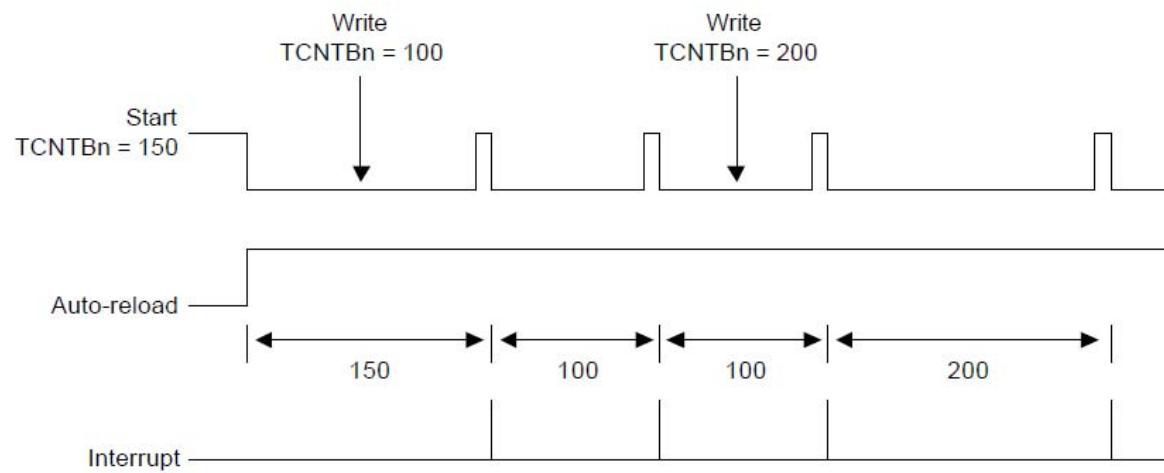
- La **polaridad de las salidas** es programable.
- La **frecuencia** de cada contador se deriva de la del reloj del sistema
 - Programando 3 módulos de pre-escalado y 3 divisores de frecuencia compartidos.





Temporizadores

- El **funcionamiento** de un temporizador es el siguiente:
 - Al capacitarlo, TCONx se inicializa con el valor del registro TCONBx.
 - La carga del valor inicial de TCMPx debe ordenarse por SW.
 - Cuando TCONx llega 0
 - puede generar una interrupción/petición de DMA.
 - si está activada la opción **auto-reload**, TCONx y TCMPx se inicializan con el valor de los registros TCONBx y TCMPBx.
 - Los dobles registros permiten programar la siguiente cuenta mientras se realiza la actual.
 - Si el temporizador se para, TCON y TCMP conservan su valor
 - pueden reprogramarse por SW.





Temporizadores

configuración: registro TCFG0

- 0x01D50000 (**TCFG0 – Timer Configuration Register 0**)
 - 32b, R/W, inicial = 0x00000000
 - Permite fijar el valor de los módulos de preescalado y la longitud de la dead-zone del temporizador 0.

| TCFG0 | Bit | Description | Initial State |
|------------------|---------|--|---------------|
| Dead zone length | [31:24] | These 8 bits determine the dead zone length. The 1 unit time of the dead zone length is equal to the 1 unit time of timer 0. | 0x00 |
| Prescaler 2 | [23:16] | These 8 bits determine prescaler value for Timer 4 & 5 | 0x00 |
| Prescaler 1 | [15:8] | These 8 bits determine prescaler value for Timer 2 & 3 | 0x00 |
| Prescaler 0 | [7:0] | These 8 bits determine prescaler value for Timer 0 & 1 | 0x00 |

Timer input clock Frequency = MCLK / {prescaler value + 1} / {divider value}

{prescaler value} = 0-255

{divider value} = 2, 4, 8, 16, 32

| 4-bit divider settings | minimum resolution (prescaler = 1) | maximum resolution (prescaler = 255) | maximum interval (TCNTBn = 65535) |
|------------------------|---------------------------------------|---|--------------------------------------|
| 1/2 (MCLK = 66 MHz) | 0.030 us (33.0 MHz) | 7.75 us (58.6 KHz) | 0.50 sec |
| 1/4 (MCLK = 66 MHz) | 0.060 us (16.5 MHz) | 15.5 us (58.6 KHz) | 1.02 sec |
| 1/8 (MCLK = 66 MHz) | 0.121 us (8.25 MHz) | 31.0 us (29.3 KHz) | 2.03 sec |
| 1/16 (MCLK = 66 MHz) | 0.242 us (4.13 MHz) | 62.1 us (14.6 KHz) | 4.07 sec |
| 1/32 (MCLK = 66 MHz) | 0.485 us (2.06 MHz) | 125 us (7.32 KHz) | 8.13 sec |



Temporizadores

configuración: registro TCFG1

- 0x01D50004 (**TCFG1 – Timer Configuration Register 1**)
 - 28b, R/W, inicial = 0x00000000
 - Permite fijar el divisor de frecuencia usado por cada temporizador y el temporizador que podrá realizar solicitudes de DMA.

| TCFG1 | Bit | Description | Initial State |
|----------|---------|---|---------------|
| DMA mode | [27:24] | Select DMA request channel 0000 = No select (all interrupt) 0001 = Timer0 0010 = Timer1 0011 = Timer2 0100 = Timer3 0101 = Timer4 0110 = Timer5 0111 = Reserved | 000 |
| MUX 5 | [23:20] | Select MUX input for PWM Timer5. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = EXTCLK | 000 |
| MUX 4 | [19:16] | Select MUX input for PWM Timer4. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = TCLK | 000 |
| MUX 3 | [15:12] | Select MUX input for PWM Timer3. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = 1/32 | 000 |
| MUX 2 | [11:8] | Select MUX input for PWM Timer2. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = 1/32 | 000 |
| MUX 1 | [7:4] | Select MUX input for PWM Timer1. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = 1/32 | 000 |
| MUX 0 | [3:0] | Select MUX input for PWM Timer0. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = 1/32 | 000 |

Temporizadores

configuración y operación: registro TCON (i)



- 0x01D500008 (**TCON – Timer Control**)
 - 27b, R/W, inicial = 0x0000000
 - Según el temporizador, permite arrancarlo, inicializar por SW su valor de TCNTx y TCMPx, habilitar el modo auto-reload, habilitar la generación de la dead-zone y fijar la polaridad de la salida.

| TCON | Bit | Description | initial state |
|--------------------------------|------|--|---------------|
| Timer 1 auto reload on/off | [11] | This bit determines the auto reload on/off for Timer1. 0 = One-shot 1 = Interval mode (auto reload) | 0 |
| Timer 1 output inverter on/off | [10] | This bit determines the output inverter on/off for Timer1. 0 = Inverter off 1 = Inverter on for TOUT1 | 0 |
| Timer 1 manual update (note) | [9] | This bit determines the manual update for Timer 1. 0 = No operation 1 = Update TCNTB1, TCMPB1 | 0 |
| Timer 1 start/stop | [8] | This bit determines start/stop for Timer 1. 0 = Stop 1 = Start for Timer 1 | 0 |
| Dead zone enable | [4] | This bit determines the dead zone operation. 0 = Disable 1 = Enable | 0 |
| Timer 0 auto reload on/off | [3] | This bit determines auto reload on/off for Timer 0. 0 = One-shot 1 = Interval mode(auto reload) | 0 |
| Timer 0 output inverter on/off | [2] | This bit determines the output inverter on/off for Timer 0. 0 = Inverter off 1 = Inverter on for TOUT0 | 0 |
| Timer 0 manual update (note) | [1] | This bit determines the manual update for Timer 0. 0 = No operation 1 = Update TCNTB0, TCMPB0 | 0 |
| Timer 0 start/stop | [0] | This bit determines start/stop for Timer 0. 0 = Stop 1 = Start for Timer 0 | 0 |

NOTE: This bit has to be cleared at next writing.



Temporizadores

configuración y operación: registro TCON (ii)



| TCON | Bit | Description | initial state |
|--------------------------------|------|--|---------------|
| Timer 5 auto reload on/off | [26] | This bit determines auto reload on/off for Timer 5. 0 = One-shot 1 = Interval mode (auto reload) | 0 |
| Timer 5 manual update (note) | [25] | This bit determines the manual update for Timer 5. 0 = No operation 1 = Update TCNTB5 | 0 |
| Timer 5 start/stop | [24] | This bit determines start/stop for Timer 5. 0 = Stop 1 = Start for Timer 5 | 0 |
| Timer 4 auto reload on/off | [23] | This bit determines auto reload on/off for Timer 4. 0 = One-shot 1 = Interval mode (auto reload) | 0 |
| Timer 4 output inverter on/off | [22] | This bit determines output inverter on/off for Timer4. 0 = Inverter off 1 = Inverter on for TOUT4 | 0 |
| Timer 4 manual update (note) | [21] | This bit determines the manual update for Timer 4. 0 = No operation 1 = Update TCNTB4, TCMPB4 | 0 |
| Timer 4 start/stop | [20] | This bit determines start/stop for Timer 4. 0 = Stop 1 = Start for Timer 4 | 0 |
| Timer 3 auto reload on/off | [19] | This bit determines auto reload on/off for Timer 3. 0 = One-shot 1 = Interval mode (auto reload) | 0 |
| Timer 3 output inverter on/off | [18] | This bit determines output inverter on/off for Timer 3. 0 = Inverter off 1 = Inverter on for TOUT3 | 0 |
| Timer 3 manual update (note) | [17] | This bit determine manual update for Timer 3. 0 = No operation 1 = Update TCNTB3, TCMPB3 | 0 |
| Timer 3 start/stop | [16] | This bit determines start/stop for Timer 3. 0 = Stop 1 = Start for Timer 3 | 0 |
| Timer 2 auto reload on/off | [15] | This bit determines auto reload on/off for Timer 2. 0 = One-shot 1 = Interval mode (auto reload) | 0 |
| Timer 2 output inverter on/off | [14] | This bit determines output inverter on/off for Timer 2. 0 = Inverter off 1 = Inverter on for TOUT2 | 0 |
| Timer 2 manual update (note) | [13] | This bit determines the manual update for Timer 2. 0 = No operation 1 = Update TCNTB2, TCMPB2 | 0 |
| Timer 2 start/stop | [12] | This bit determines start/stop for Timer 2. 0 = Stop 1 = Start for Timer 2 | 0 |

NOTE: This bit has to be cleared at next writing.

Temporizadores

operación: registros TCNTBx



- 0x01D5000C (**TCNTB0 – Timer 0 Count Buffer**)
- 0x01D50018 (**TCNTB1 – Timer 1 Count Buffer**)
- 0x01D50024 (**TCNTB2 – Timer 2 Count Buffer**)
- 0x01D50030 (**TCNTB3 – Timer 3 Count Buffer**)
- 0x01D5003C (**TCNTB4 – Timer 4 Count Buffer**)
- 0x01D50048 (**TCNTB5 – Timer 5 Count Buffer**)
 - 16b, R/W, inicial = 0x0000
 - Permite fijar el número de ciclos inicial que cargará TCNTx.

| TCNTB0 | Bit | Description | Initial State |
|-------------------------------|--------|--|---------------|
| Timer 0 count buffer register | [15:0] | Setting count buffer value for Timer 0 | 0x00000000 |

Temporizadores

operación: registros TCMPBx



- 0x01D50010 (**TCMPBx – Timer 0 Compare Buffer**)
- 0x01D5001C (**TCMPBx – Timer 1 Compare Buffer**)
- 0x01D50028 (**TCMPBx – Timer 2 Compare Buffer**)
- 0x01D50034 (**TCMPBx – Timer 3 Compare Buffer**)
- 0x01D50040 (**TCMPBx – Timer 4 Compare Buffer**)
 - 16b, R/W, reset = 0x0000
 - Permite fijar el número de ciclos inicial que cargará TCMPx.

| TCMPB0 | Bit | Description | Initial State |
|---------------------------------|--------|---|---------------|
| Timer 0 compare buffer register | [15:0] | Setting compare buffer value for Timer 0 NOTE: This value must be smaller than TCNTB0 | 0x00000000 |

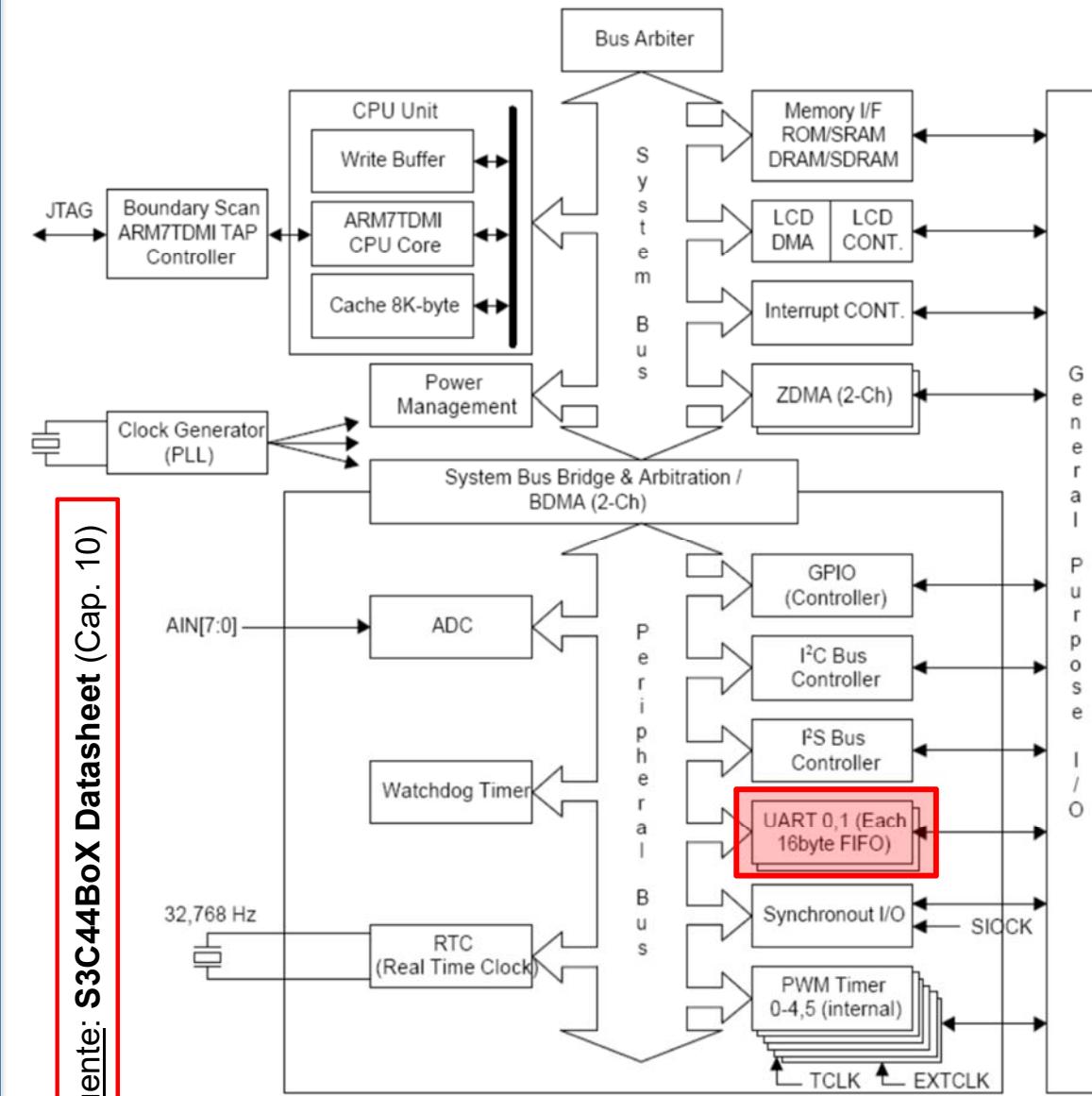
Temporizadores

operación: registros TCNT0x



- 0x01D50014 (**TCNT00** – Timer 0 Count Observation)
- 0x01D50020 (**TCNT01** – Timer 1 Count Observation)
- 0x01D5002C (**TCNT02** – Timer 2 Count Observation)
- 0x01D50038 (**TCNT03** – Timer 3 Count Observation)
- 0x01D50044 (**TCNT04** – Timer 4 Count Observation)
- 0x01D5004C (**TCNT05** – Timer 5 Count Observation)
 - 16b, R, reset = 0x0000
 - Indica el valor actual de TCNTx.

| TCNT00 | Bit | Description | Initial State |
|------------------------------|--------|---|---------------|
| Timer 0 observation register | [15:0] | Setting count observation value for Timer 0 | 0x00000000 |



UART



- Configurable mediante 22 registros mapeados en memoria (banco 0).

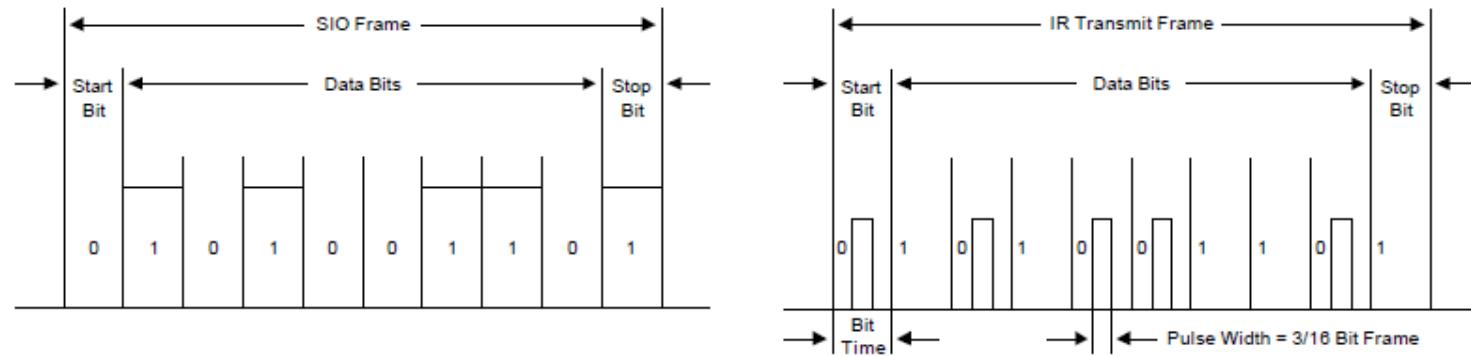
que permiten:

- Configurar el modo de funcionamiento de cada cada canal.
- Ordenar y controlar las transferencias serie.

UART



- EL S3C44B0X dispone de una **UART** de **2 canales**
 - Permite la comunicación a través **2 puertos bidireccionales** de E/S serie asíncrona.
- Cada canal dispone de **4 líneas unidireccionales**:
 - **2 líneas de datos serie**: TxD (salida) y RxD (entrada).
 - **2 líneas para control de flujo** por handshake: RTS (salida) y CTS (entrada).
- Cada canal puede programarse para transmitir
 - En modo normal (RS-232) o en modo infrarrojos (IrDA 1.0).
 - Usando un cierto formato de datos y una tasa de transferencia determinada.
 - Mediante encuesta (programado), interrupción o DMA.
 - Utilizando las 2 FIFOs internas de 16B que dispone (una de envío y otra de recepción).
 - Con control de flujo es opcional y puede ser manual o automático





UART

configuración: registro ULCONx

- 0x01D00000 (**ULCON0 – UART Channel 0 Line Control**)
- 0x01D04000 (**ULCON1 – UART Channel 1 Line Control**)
 - 8b, R/W, reset = 0x00
 - Permite configurar el formato de los datos serie.

| ULCONn | Bit | Description | Initial State |
|--------------------|-------|--|---------------|
| Reserved | [7] | | 0 |
| Infra-Red Mode | [6] | The Infra-Red mode determines whether or not to use the Infra-Red mode. 0 = Normal mode operation 1 = Infra-Red Tx/Rx mode | 0 |
| Parity Mode | [5:3] | The parity mode specifies how parity generation and checking are to be performed during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/checked as 1 111 = Parity forced/checked as 0 | 000 |
| Number of stop bit | [2] | The number of stop bits specifies how many stop bits are to be used to signal end-of-frame. 0 = One stop bit per frame 1 = Two stop bit per frame | 0 |
| Word length | [1:0] | The word length indicates the number of data bits to be transmitted or received per frame. 00 = 5-bits 01 = 6-bits 10 = 7-bits 11 = 8-bits | 00 |



UART

configuración: registro UBRDIVx

- 0x01D00028 (**UBRDIV0** – UART Channel 0 Baud Rate Division)
- 0x01D04028 (**UBRDIV1** – UART Channel 1 Baud Rate Division)
 - 16b, R/W, reset = indefinido
 - Permite configurar la velocidad de comunicación.

| UBRDIV n | Bit | Description | Initial State |
|----------|--------|---|---------------|
| UBRDIV | [15:0] | Baud rate division value UBRDIVn > 0 | - |

$$UBRDIVn = (\text{round_off})(MCLK / (\text{bps} \times 16)) - 1$$

UART

configuración: registro UCONx



- 0x01D00004 (**UCON0 – UART Channel 0 Control**)
- 0x01D04004 (**UCON1 – UART Channel 1 Control**)
 - 10b, R/W, reset = 0x000
 - Permite configurar el modo de transmisión (por interrupciones/DMA) de la UART.

| UCONn | Bit | Description | Initial State |
|----------------------------------|-------|--|---------------|
| Tx interrupt type | [9] | Interrupt request type 0 = Pulse (Interrupt is requested the instant Tx buffer becomes empty) 1 = Level (Interrupt is requested while Tx buffer is empty) | 0 |
| Rx interrupt type | [8] | Interrupt request type 0 = Pulse (Interrupt is requested the instant Rx buffer receives the data) 1 = Level (Interrupt is requested while Rx buffer is receiving data) | 0 |
| Rx time out enable | [7] | Enable/Disable Rx time out interrupt when UART FIFO is enabled. The interrupt is a receive interrupt. 0 = Disable 1 = Enable | 0 |
| Rx error status interrupt enable | [6] | This bit enables the UART to generate an interrupt if an exception, such as a break, frame error, parity error, or overrun error occurs during a receive operation. 0 = Do not generate receive error status interrupt 1 = Generate receive error status interrupt | 0 |
| Loop-back Mode | [5] | Setting loop-back bit to 1 causes the UART to enter the loop-back mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loop-back mode | 0 |
| Send Break Signal | [4] | Setting this bit causes the UART to send a break during 1 frame time. This bit is auto-cleared after sending the break signal. 0 = Normal transmit 1 = Send break signal | 0 |
| Transmit Mode | [3:2] | These two bits determine which function is currently able to write Tx data to the UART transmit holding register. 00 = Disable 01 = Interrupt request or polling mode 10 = BDMA0 request (Only for UART0) 11 = BDMA1 request (Only for UART1) | 00 |
| Receive Mode | [1:0] | These two bits determine which function is currently able to read data from UART receive buffer register. 00 = Disable, 01 = Interrupt request or polling mode 10 = BDMA0 request (Only for UART0) 11 = BDMA1 request (Only for UART1) | 00 |



UART

configuración: registro UFCONx

- 0x01D00008 (**UFCON0 – UART Channel 0 FIFO Control**)
- 0x01D04008 (**UFCON1 – UART Channel 1 FIFO Control**)
 - 8b, R/W, reset = 0x00
 - Permite habilitar las FIFOs de datos, borrarlas y fijar el nivel de ocupación a partir del cual se dispara una interrupción o solicitud de DMA.

| UFCONn | Bit | Description | Initial State |
|-----------------------|------------|---|----------------------|
| Tx FIFO Trigger Level | [7:6] | These two bits determine the trigger level of transmit FIFO. 00 = Empty 10 = 8-byte 11 = 12-byte | 00 |
| Rx FIFO Trigger Level | [5:4] | These two bits determine the trigger level of receive FIFO. 00 = 4-byte 10 = 12-byte 01 = 8-byte 11 = 16-byte | 00 |
| Reserved | [3] | | 0 |
| Tx FIFO Reset | [2] | This bit is auto-cleared after resetting FIFO 0 = Normal 1= Tx FIFO reset | 0 |
| Rx FIFO Reset | [1] | This bit is auto-cleared after resetting FIFO 0 = Normal 1= Rx FIFO reset | 0 |
| FIFO Enable | [0] | 0 = FIFO disable 1 = FIFO mode | 0 |

NOTE: When the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out), and the users should check the FIFO status and read out the rest.

UART

operación: registro UTRSTATx



- 0x01D00010 (**UTRSTAT0** – UART Channel 0 Tx/Rx Status)
- 0x01D04010 (**UTRSTAT1** – UART Channel 1 Tx/Rx Status)
 - 3b, R, reset = 0x6
 - Indica de estado de la transmisión/recepción.

| UTRSTATn | Bit | Description | Initial State |
|---------------------------|------------|--|----------------------|
| Transmit shifter empty | [2] | This bit is automatically set to 1 when the transmit shift register has no valid data to transmit and the transmit shift register is empty. 0 = Not empty 1 = Transmit holding & shifter register empty | 1 |
| Transmit buffer empty | [1] | This bit is automatically set to 1 when the transmit buffer register does not contain valid data. 0 = The buffer register is not empty 1 = Empty If the UART uses the FIFO, users should check Tx FIFO Count bits and Tx FIFO Full bit in the UFSTAT register instead of this bit. | 1 |
| Receive buffer data ready | [0] | This bit is automatically set to 1 whenever the receive buffer register contains valid data, received over the RXDn port. 0 = Completely empty 1 = The buffer register has a received data If the UART uses the FIFO, users should check Rx FIFO Count bits in the UFSTAT register instead of this bit. | 0 |



UART

operación: registro UERSTATx

- 0x01D00014 (**UERSTAT0 – UART Channel 0 Rx Error Status**)
- 0x01D04014 (**UERSTAT0 – UART Channel 1 Rx Error Status**)
 - 4b, R, reset = 0x0
 - Indica el error producido en la recepción (si lo hubiera).

| UERSTATn | Bit | Description | Initial State |
|---------------|-----|---|---------------|
| Break Detect | [3] | This bit is automatically set to 1 to indicate that a break signal has been received. 0 = No break receive 1 = Break receive | 0 |
| Frame Error | [2] | This bit is automatically set to 1 whenever a frame error occurs during receive operation. 0 = No frame error during receive 1 = Frame error | 0 |
| Parity Error | [1] | This bit is automatically set to 1 whenever a parity error occurs during receive operation. 0 = No parity error during receive 1 = Parity error | 0 |
| Overrun Error | [0] | This bit is automatically set to 1 whenever an overrun error occurs during receive operation. 0 = No overrun error during receive 1 = Overrun error | 0 |

NOTE: These bits (UERSATn[3:0]) are automatically cleared to 0 when the UART error status register is read.



UART

operación: registro UFSTATx

- 0x01D00014 (**UFSTAT0 – UART Channel 0 FIFO Status**)
- 0x01D04014 (**UFSTAT1 – UART Channel 1 FIFO Status**)
 - 16b, R, reset = 0x0000
 - Indica el de estado de las FIFOs de datos.

| UFSTATn | Bit | Description | Initial State |
|---------------|---------|--|---------------|
| Reserved | [15:10] | | 0 |
| Tx FIFO Full | [9] | This bit is automatically set to 1 whenever transmit FIFO is full during transmit operation 0 = 0-byte ≤ Tx FIFO data ≤ 15-byte 1 = Full | 0 |
| Rx FIFO Full | [8] | This bit is automatically set to 1 whenever receive FIFO is full during receive operation 0 = 0-byte ≤ Rx FIFO data ≤ 15-byte 1 = Full | 0 |
| Tx FIFO Count | [7:4] | Number of data in Tx FIFO | 0 |
| Rx FIFO Count | [3:0] | Number of data in Rx FIFO | 0 |

UART

operación: registros UMCONx y UMSTATx



- 0x01D0000C (**UMCON0 – UART Channel 0 Modem Control**)
- 0x01D0400C (**UMCON1 – UART Channel 1 Modem Control**)
 - 8b, R/W, reset = 0x00
 - Permite activar el control de flujo automático o controla la señal RTS.

| UMCONn | Bit | Description | Initial State |
|------------------------|-------|--|---------------|
| Reserved | [7:5] | These bits must be 0's | 00 |
| AFC(Auto Flow Control) | [4] | 0 = Disable 1 = Enable | 0 |
| Reserved | [3:1] | These bits must be 0's | 00 |
| Request to Send | [0] | If AFC bit is enabled, this value will be ignored. In this case the S3C44B0X will control nRTS automatically. If AFC bit is disabled, nRTS must be controlled by S/W. 0 = 'H' level(Inactivate nRTS) 1 = 'L' level(Activate nRTS) | 0 |

- x01D0001C (**UMSTAT0 – UART Channel 0 Modem Status**)
- 0x01D0401C (**UMSTAT1 – UART Channel 1 Modem Status**)
 - 5b, R, reset = 0x00
 - Indica el estado de la línea CTS.

| UMSTATn | Bit | Description | Initial State |
|---------------|-------|--|---------------|
| Delta CTS | [4] | This bit indicates that the nCTS input to S3C44B0X has changed state since the last time it was read by CPU. (Refer to Fig. 10-7) 0 = Has not changed 1 = Has changed | 0 |
| Reserved | [3:1] | Reserved | |
| Clear to Send | [0] | 0 = CTS signal is not activated(nCTS pin is high) 1 = CTS signal is activated(nCTS pin is low) | 0 |



UART

operación: registros UTXHx y URXHx

- 0x01D00020 (**UTXH0** – UART Channel 0 Transmit Holding)
- 0x01D04020 (**UTXH1** – UART Channel 1 Transmit Holding)
 - 8b, W, reset = indefinido
 - Registro del dato a transmitir.

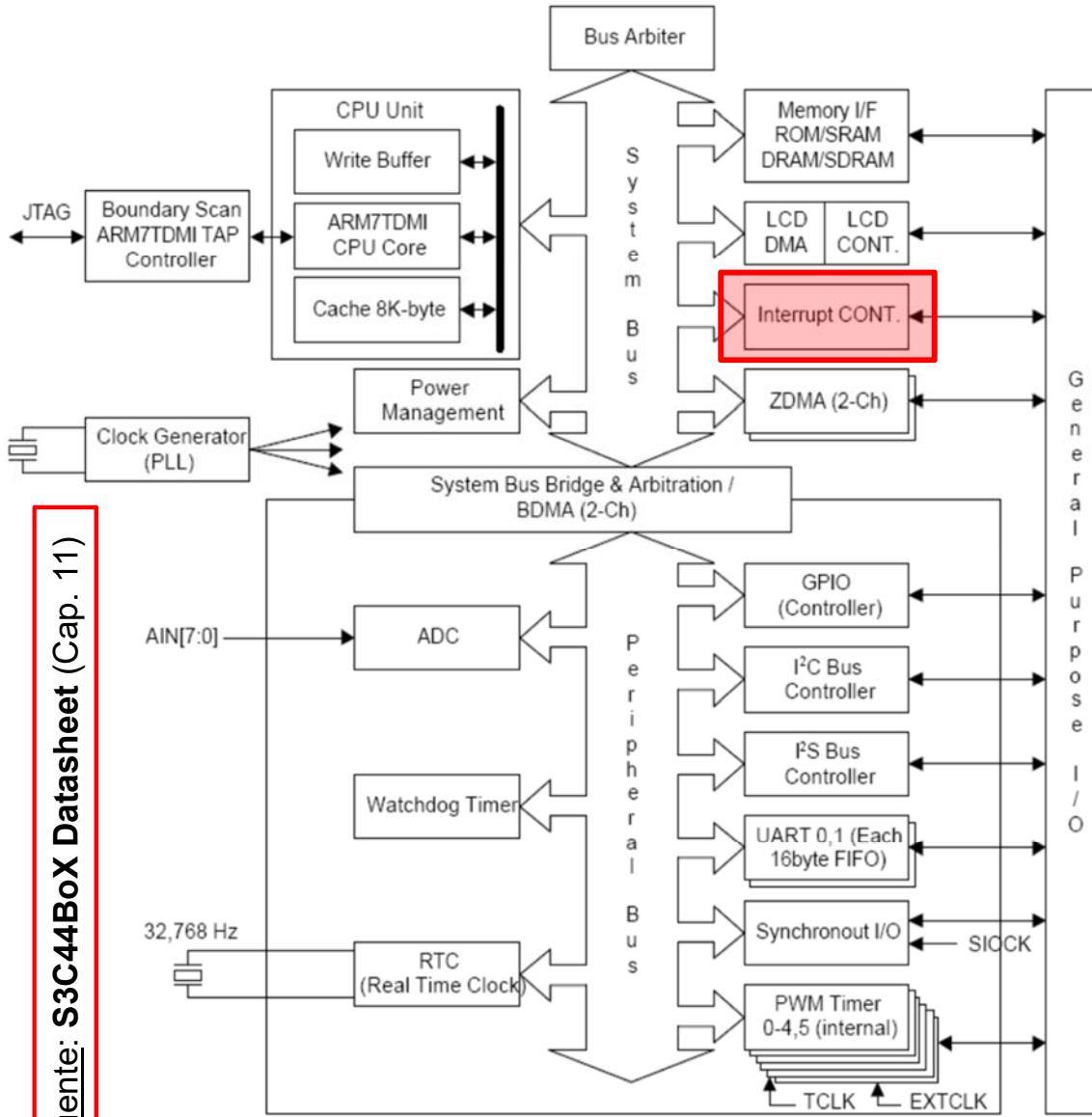
| UTXHn | Bit | Description | Initial State |
|--------------|------------|-------------------------|----------------------|
| TXDATAn | [7:0] | Transmit data for UARTn | - |

- 0x01D00024 (**URXH0** – UART Channel 0 Receive Holding)
- 0x01D04024 (**URXH1** – UART Channel 1 Receive Holding)
 - 8b, R, reset = indefinido
 - Registro del dato recibido.

| URXHn | Bit | Description | Initial State |
|--------------|------------|------------------------|----------------------|
| RXDATAn | [7:0] | Receive data for UARTn | - |



Controlador de interrupciones



■ Configurable mediante 12 registros mapeados en memoria (banco 0).

que permiten:

- Establecer un mecanismo de arbitraje entre peticiones simultáneas
- Dar soporte a la operación con interrupciones



Controlador de interrupciones

- La CPU del S3C44B0X dispone únicamente de **2 líneas de interrupción vectorizadas**: IRQ y FIQ.
- El **controlador de interrupciones** permite:
 - Ampliar el número de **fuentes de interrupción a 30**: 21 internas al SOC y 8 externas.
 - Ampliar el número de **líneas de interrupción a 26**: 21 internas al SOC y 5 externas (4 dispositivos externos deben compartir línea de interrupción).
 - Fijar el modo de interrupción de cada fuente (si activa la línea FIQ o IRQ de la CPU).
 - Vectorizar (si se desea) las interrupciones en modo IRQ.
 - Cuando se activa la línea IRQ, el core ARM7TDMI hace fetch de la dirección 0x00000018 (vector nativo de IRQ)
 - Cuando el controlador de interrupciones está en modo vectorizado y detecta en el bus la petición de lectura de dicha dirección, vuelca en las líneas de datos la instrucción B <vector>
 - La CPU al ejecutar la instrucción, salta a la dirección del nuevo vector.
 - Hacer un proceso de arbitraje por HW cuando hay varias peticiones de interrupción simultáneas en modo IRQ.

Controlador de interrupciones

fuentes de interrupción y vectores asociados



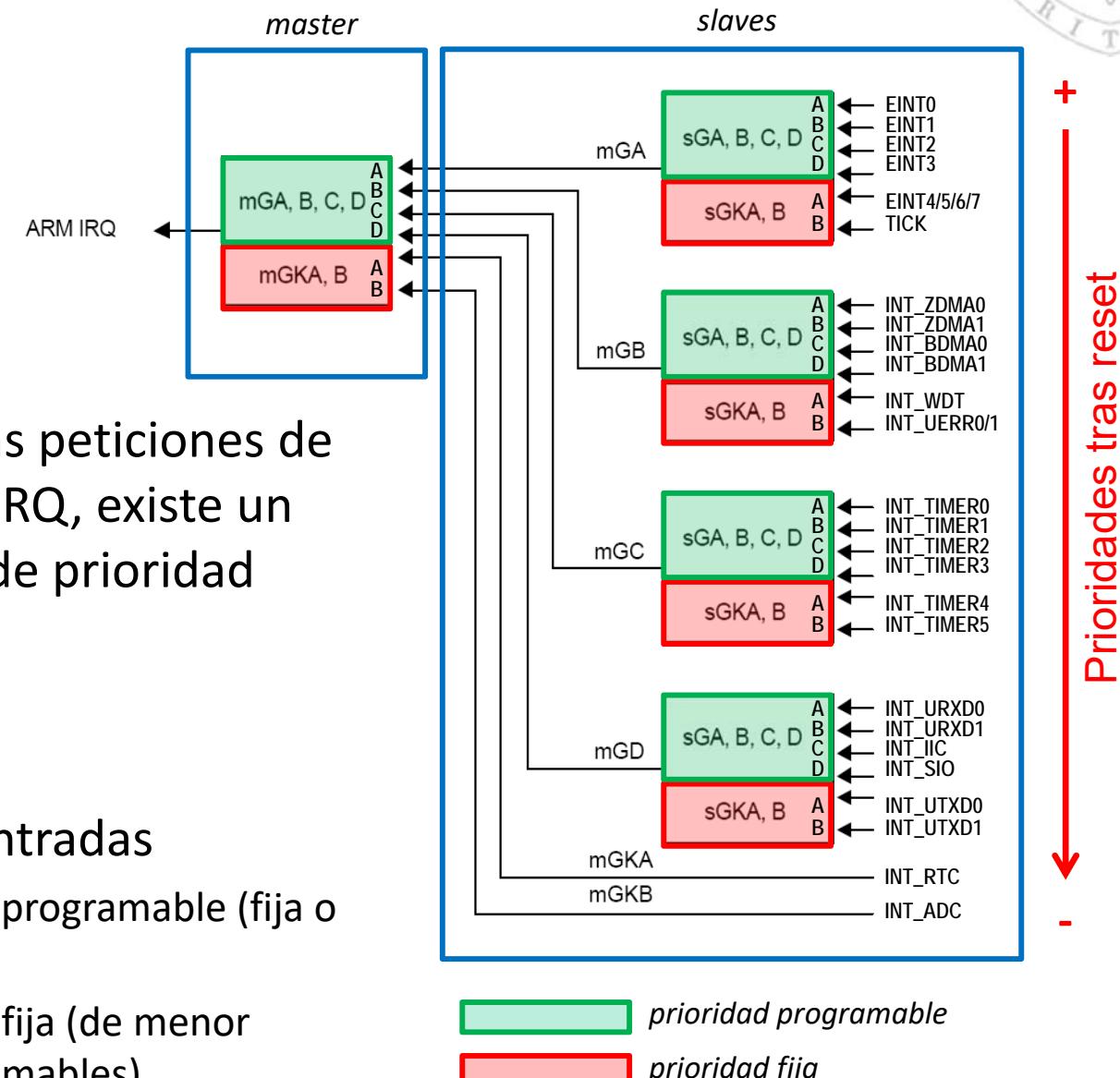
| Sources | Descriptions | Master Group | Slave ID | Vector Address |
|-------------|----------------------------|--------------|----------|----------------|
| EINT0 | External interrupt 0 | mGA | sGA | 0x00000020 |
| EINT1 | External interrupt 1 | mGA | sGB | 0x00000024 |
| EINT2 | External interrupt 2 | mGA | sGC | 0x00000028 |
| EINT3 | External interrupt 3 | mGA | sGD | 0x0000002c |
| EINT4/5/6/7 | External interrupt 4/5/6/7 | mGA | sGKA | 0x00000030 |
| TICK | RTC Time tick interrupt | mGA | sGKB | 0x00000034 |
| INT_ZDMA0 | General DMA0 interrupt | mGB | sGA | 0x00000040 |
| INT_ZDMA1 | General DMA1 interrupt | mGB | sGB | 0x00000044 |
| INT_BDMA0 | Bridge DMA0 interrupt | mGB | sGC | 0x00000048 |
| INT_BDMA1 | Bridge DMA1 interrupt | mGB | sGD | 0x0000004c |
| INT_WDT | Watch-Dog timer interrupt | mGB | sGKA | 0x00000050 |
| INT_UERR0/1 | UART0/1 error Interrupt | mGB | sGKB | 0x00000054 |
| INT_TIMER0 | Timer0 interrupt | mGC | sGA | 0x00000060 |
| INT_TIMER1 | Timer1 interrupt | mGC | sGB | 0x00000064 |
| INT_TIMER2 | Timer2 interrupt | mGC | sGC | 0x00000068 |
| INT_TIMER3 | Timer3 interrupt | mGC | sGD | 0x0000006c |
| INT_TIMER4 | Timer4 interrupt | mGC | sGKA | 0x00000070 |
| INT_TIMER5 | Timer5 interrupt | mGC | sGKB | 0x00000074 |
| INT_URXD0 | UART0 receive interrupt | mGD | sGA | 0x00000080 |
| INT_URXD1 | UART1 receive interrupt | mGD | sGB | 0x00000084 |
| INT_IIC | IIC interrupt | mGD | sGC | 0x00000088 |
| INT_SIO | SIO interrupt | mGD | sGD | 0x0000008c |
| INT_UTXD0 | UART0 transmit interrupt | mGD | sGKA | 0x00000090 |
| INT_UTXD1 | UART1 transmit interrupt | mGD | sGKB | 0x00000094 |
| INT_RTC | RTC alarm interrupt | mGKA | – | 0x000000a0 |
| INT_ADC | ADC EOC interrupt | mGKB | – | 0x000000c0 |

Controlador de interrupciones

arbitraje



- Para arbitrar por HW las peticiones de interrupción en modo IRQ, existe un bloque de generación de prioridad formado por:
 - 1 unidad master
 - 4 unidades esclavas
- Cada unidad tiene: 6 entradas
 - 4 entradas de prioridad programable (fija o rotatorio)
 - 2 entradas de prioridad fija (de menor prioridad que las programables)



Controlador de interrupciones

configuración: registro I_PSLV (i)



- 0x01E00010 (I_PSLV – IRQ Priority of Slave)
 - 32b, R/W, inicial = 0x1B1B1B1B
 - Para cada grupo esclavo, permite establecer la prioridad relativa entre las 4 líneas de interrupción de prioridad programable que lo forman.

| <u>I_PSLV</u> | Bit | Description | Initial State |
|---------------|---------|---|---------------|
| PSLAVE@mGA | [31:24] | Determine the priorities among sGA, B, C, D of mGA. Each sGn must have a different priority. | 0x1b |
| PSLAVE@mGB | [23:16] | Determine the priorities among sGA, B, C, D of mGB. Each sGn must have a different priority. | 0x1b |
| PSLAVE@mGC | [15:8] | Determine the priorities among sGA, B, C, D of mGC. Each sGn must have a different priority. | 0x1b |
| PSLAVE@mGD | [7:0] | Determine the priorities among sGA, B, C, D of mGD. Each sGn must have a different priority. | 0x1b |

Controlador de interrupciones

configuración: registro I_PSLV (ii)



| PSLAVE@mGA | Bit | Description | | | | | Initial State |
|-------------------|------------|---------------------|---------------------|---------------------|---------------------|--|----------------------|
| sGA (EINT0) | [31:30] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (EINT1) | [29:28] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| sGC (EINT2) | [27:26] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (EINT3) | [25:24] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |
| PSLAVE@mGB | Bit | Description | | | | | Initial State |
| sGA (INT_ZDMA0) | [23:22] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (INT_ZDMA1) | [21:20] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| sGC (INT_BDMA0) | [19:18] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (INT_BDMA1) | [17:16] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |
| PSLAVE@mGC | Bit | Description | | | | | Initial State |
| sGA (TIMER0) | [15:14] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (TIMER1) | [13:12] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| sGC (TIMER2) | [11:10] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (TIMER3) | [9:8] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |
| PSLAVE@mGD | Bit | Description | | | | | Initial State |
| sGA (INT_URXD0) | [7:6] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (INT_URXD1) | [5:4] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| Sgc (INT_IIC) | [3:2] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (INT_SIO) | [1:0] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |

NOTE: The items in I_PSLAVE must be configured with different priorities even if the corresponding interrupt source is not used.



Controlador de interrupciones

configuración: registro I_PMST

- 0x01E00014 (I_PMST – IRQ Priority of Master)
 - 16b, R/W, inicial = 0x1F1B
 - Permite establecer la prioridad relativa entre los 4 grupos esclavos de prioridad programable y si las prioridades son fijas o rotatorias.

| <u>I_PMST</u> | Bit | Description | Initial State |
|---------------|---------|--|---------------|
| Reserved | [15:13] | | 000 |
| M | [12] | Master operating mode 0 = round robin 1 = fix mode | 1 |
| FxSLV[A:D] | [11:8] | Slave operating mode 0 = round robin 1 = fix mode | 1111 |
| PMMASTER | [7:0] | Determine the priorities among 4 slave units. | 0x1b |

| <u>FxSLV</u> | Bit | Description | Initial State |
|--------------|------|--|---------------|
| Fx@mGA | [11] | Determines the operating mode of slave unit @mGA | 1 |
| Fx@mGB | [10] | Determines the operating mode of slave unit @mGB | 1 |
| Fx@mGC | [9] | Determines the operating mode of slave unit @mGC | 1 |
| Fx@mGD | [8] | Determines the operating mode of slave unit @mGD | 1 |

| <u>PMMASTER</u> | Bit | Description | Initial State |
|-----------------|-------|---|---------------|
| mGA | [7:6] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 00 |
| mGB | [5:4] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 01 |
| mGC | [3:2] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 10 |
| mGD | [1:0] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 11 |

NOTE: The items in I_PMST must be configured with different priorities even if the corresponding interrupt source is not used.

Controlador de interrupciones

operación: registro I_CSLV (i)



- 0x01E00018 (I_CSLV – Current IRQ Priority of Slave)
 - 32b, R, inicial = 0x1B1B1B1B
 - Para cada grupo esclavo, indica la prioridad relativa existente entre las 4 líneas de interrupción de prioridad programable que lo forman
 - Solo si está activada la prioridad rotatoria en los esclavos, I_CSLV podrá ser distinto de I_PSLV .

| I_CSLV | Bit | Description | Initial State |
|------------|---------|---|---------------|
| CSLAVE@mGA | [31:24] | Indicate the current priority status of mGA | 0x1b |
| CSLAVE@mGB | [23:16] | Indicate the current priority status of mGB | 0x1b |
| CSLAVE@mGC | [15:8] | Indicate the current priority status of mGC | 0x1b |
| CSLAVE@mGD | [7:0] | Indicate the current priority status of mGD | 0x1b |

Controlador de interrupciones

configuración: registro I CSLV (ii)



| PSLAVE@mGA | Bit | Description | | | | | Initial State |
|-------------------|------------|---------------------|---------------------|---------------------|---------------------|--|----------------------|
| sGA (EINT0) | [31:30] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (EINT1) | [29:28] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| sGC (EINT2) | [27:26] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (EINT3) | [25:24] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |

| PSLAVE@mGB | Bit | Description | | | | | Initial State |
|-------------------|------------|---------------------|---------------------|---------------------|---------------------|--|----------------------|
| sGA (INT_ZDMA0) | [23:22] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (INT_ZDMA1) | [21:20] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| sGC (INT_BDMA0) | [19:18] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (INT_BDMA1) | [17:16] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |

| PSLAVE@mGC | Bit | Description | | | | | Initial State |
|-------------------|------------|---------------------|---------------------|---------------------|---------------------|--|----------------------|
| sGA (TIMER0) | [15:14] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (TIMER1) | [13:12] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| sGC (TIMER2) | [11:10] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (TIMER3) | [9:8] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |

| PSLAVE@mGD | Bit | Description | | | | | Initial State |
|-------------------|------------|---------------------|---------------------|---------------------|---------------------|--|----------------------|
| sGA (INT_URXD0) | [7:6] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 00 |
| sGB (INT_URXD1) | [5:4] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 01 |
| Sgc (INT_IIC) | [3:2] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 10 |
| sGD (INT_SIO) | [1:0] | 00: 1 st | 01: 2 nd | 10: 3 rd | 11: 4 th | | 11 |

Controlador de interrupciones

operación: registro I_PMST



- 0x01E0001C (I_CMST – Current IRQ Priority of Master)
 - 16b, R, inicial = 0xXX1B
 - Indica la prioridad relativa existente entre los 4 grupos esclavos de prioridad programable.
 - Solo si está activada la prioridad rotatoria en el master, I_CMST podrá ser distinto de I_PMST).

| <u>I_CMST</u> | Bit | Description | Initial State |
|---------------|---------|---|---------------|
| Reserved | [15:14] | | 00 |
| VECTOR | [13:8] | The lower 6 bits of corresponding branch machine code | unknown |
| CMASTER | [7:0] | Current priority of master | 00011011 |

| <u>PMASTER</u> | Bit | Description | Initial State |
|----------------|-------|---|---------------|
| mGA | [7:6] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 00 |
| mGB | [5:4] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 01 |
| mGC | [3:2] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 10 |
| mGD | [1:0] | 00: 1 st 01: 2 nd 10: 3 rd 11: 4 th | 11 |

Controlador de interrupciones

configuración: registro INTCON



■ 0x01E00000 (INTCON – Interrupt Control)

- 4b, R/W, inicial = 0x7,
- Permite habilitar las líneas IRQ/FIQ hacia la CPU y el modo de interrupción de las IRQ.

| INTCON | Bit | Description | initial state |
|----------|-----|--|---------------|
| Reserved | [3] | 0 | 0 |
| V | [2] | This bit disables/enables vector mode for IRQ 0 = Vectored interrupt mode 1 = Non-vectored interrupt mode | 1 |
| I | [1] | This bit enables IRQ interrupt request line to CPU 0 = IRQ interrupt enable 1 = Reserved Note : Before using the IRQ interrupt this bit must be cleared. | 1 |
| F | [0] | This bit enables FIQ interrupt request line to CPU 0 = FIQ interrupt enable (Not allowed vectored interrupt mode) 1 = Reserved Note : Before using the FIQ interrupt this bit must be cleared. | 1 |

NOTE: FIQ interrupt mode does not support vectored interrupt mode.

Controlador de interrupciones

configuración: registro INTMOD



- 0x01E00008 (**INTMOD – Interrupt Mode**)

- 26b, R/W, inicial = 0x0000000
- Para cada línea de interrupción, permite establecer el modo IRQ/FIQ de la misma.

| INTMOD | Bit | Description | | initial state |
|-------------|------|--------------|--------------|---------------|
| EINT0 | [25] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| EINT1 | [24] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| EINT2 | [23] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| EINT3 | [22] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| EINT4/5/6/7 | [21] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_TICK | [20] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_ZDMA0 | [19] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_ZDMA1 | [18] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_BDMA0 | [17] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_BDMA1 | [16] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_WDT | [15] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_UERR0/1 | [14] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_TIMER0 | [13] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_TIMER1 | [12] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_TIMER2 | [11] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_TIMER3 | [10] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_TIMER4 | [9] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_TIMER5 | [8] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_URXD0 | [7] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_URXD1 | [6] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_IIC | [5] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_SIO | [4] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_UTXD0 | [3] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_UTXD1 | [2] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_RTC | [1] | 0 = IRQ mode | 1 = FIQ mode | 0 |
| INT_ADC | [0] | 0 = IRQ mode | 1 = FIQ mode | 0 |

Controlador de interrupciones

operación: registro INTPND



■ 0x01E00004 (INTPND – Interrupt Pending)

- 26b, R, inicial = 0x0000000
- Para cada línea de interrupción, indica si hay una solicitud pendiente.
- Una vez atendida, la RTI debe borrar el bit correspondiente escribiendo un 1 en los registros I_ISPC/F_ISPC.

| INTPND | Bit | Description | Initial State |
|-------------|------|----------------------------------|---------------|
| EINT0 | [25] | 0 = Not requested, 1 = Requested | 0 |
| EINT1 | [24] | 0 = Not requested, 1 = Requested | 0 |
| EINT2 | [23] | 0 = Not requested, 1 = Requested | 0 |
| EINT3 | [22] | 0 = Not requested, 1 = Requested | 0 |
| EINT4/5/6/7 | [21] | 0 = Not requested, 1 = Requested | 0 |
| INT_TICK | [20] | 0 = Not requested, 1 = Requested | 0 |
| INT_ZDMA0 | [19] | 0 = Not requested, 1 = Requested | 0 |
| INT_ZDMA1 | [18] | 0 = Not requested, 1 = Requested | 0 |
| INT_BDMA0 | [17] | 0 = Not requested, 1 = Requested | 0 |
| INT_BDMA1 | [16] | 0 = Not requested, 1 = Requested | 0 |
| INT_WDT | [15] | 0 = Not requested, 1 = Requested | 0 |
| INT_UERR0/1 | [14] | 0 = Not requested, 1 = Requested | 0 |
| INT_TIMER0 | [13] | 0 = Not requested, 1 = Requested | 0 |
| INT_TIMER1 | [12] | 0 = Not requested, 1 = Requested | 0 |
| INT_TIMER2 | [11] | 0 = Not requested, 1 = Requested | 0 |
| INT_TIMER3 | [10] | 0 = Not requested, 1 = Requested | 0 |
| INT_TIMER4 | [9] | 0 = Not requested, 1 = Requested | 0 |
| INT_TIMER5 | [8] | 0 = Not requested, 1 = Requested | 0 |
| INT_URXD0 | [7] | 0 = Not requested, 1 = Requested | 0 |
| INT_URXD1 | [6] | 0 = Not requested, 1 = Requested | 0 |
| INT_IIC | [5] | 0 = Not requested, 1 = Requested | 0 |
| INT_SIO | [4] | 0 = Not requested, 1 = Requested | 0 |
| INT_UTXD0 | [3] | 0 = Not requested, 1 = Requested | 0 |
| INT_UTXD1 | [2] | 0 = Not requested, 1 = Requested | 0 |
| INT_RTC | [1] | 0 = Not requested, 1 = Requested | 0 |
| INT_ADC | [0] | 0 = Not requested, 1 = Requested | 0 |

Controlador de interrupciones

operación: registro INTMSK



■ 0x01E0000C (INTMSK – Interrupt Mask)

- 28b, R/W, inicial = 0xFFFFFFFF
- Permite enmascarar global o individualmente cada una de las líneas de interrupción.

| INTMSK | Bit | Description | | initial state |
|-------------|------|-----------------------|------------|---------------|
| Reserved | [27] | | | 0 |
| Global | [26] | 0 = Service available | 1 = Masked | 1 |
| EINT0 | [25] | 0 = Service available | 1 = Masked | 1 |
| EINT1 | [24] | 0 = Service available | 1 = Masked | 1 |
| EINT2 | [23] | 0 = Service available | 1 = Masked | 1 |
| EINT3 | [22] | 0 = Service available | 1 = Masked | 1 |
| EINT4/5/6/7 | [21] | 0 = Service available | 1 = Masked | 1 |
| INT_TICK | [20] | 0 = Service available | 1 = Masked | 1 |
| INT_ZDMA0 | [19] | 0 = Service available | 1 = Masked | 1 |
| INT_ZDMA1 | [18] | 0 = Service available | 1 = Masked | 1 |
| INT_BDMA0 | [17] | 0 = Service available | 1 = Masked | 1 |
| INT_BDMA1 | [16] | 0 = Service available | 1 = Masked | 1 |
| INT_WDT | [15] | 0 = Service available | 1 = Masked | 1 |
| INT_UERR0/1 | [14] | 0 = Service available | 1 = Masked | 1 |
| INT_TIMER0 | [13] | 0 = Service available | 1 = Masked | 1 |
| INT_TIMER1 | [12] | 0 = Service available | 1 = Masked | 1 |
| INT_TIMER2 | [11] | 0 = Service available | 1 = Masked | 1 |
| INT_TIMER3 | [10] | 0 = Service available | 1 = Masked | 1 |
| INT_TIMER4 | [9] | 0 = Service available | 1 = Masked | 1 |
| INT_TIMER5 | [8] | 0 = Service available | 1 = Masked | 1 |
| INT_URXD0 | [7] | 0 = Service available | 1 = Masked | 1 |
| INT_URXD1 | [6] | 0 = Service available | 1 = Masked | 1 |
| INT_IIC | [5] | 0 = Service available | 1 = Masked | 1 |
| INT_SIO | [4] | 0 = Service available | 1 = Masked | 1 |
| INT_UTXD0 | [3] | 0 = Service available | 1 = Masked | 1 |
| INT_UTXD1 | [2] | 0 = Service available | 1 = Masked | 1 |
| INT_RTC | [1] | 0 = Service available | 1 = Masked | 1 |
| INT_ADC | [0] | 0 = Service available | 1 = Masked | 1 |

Controlador de interrupciones

operación: registros I_ISPC y F_ISPC



- 0x01E00024 (**I_ISPC** – IRQ Interrupt Service Pending Clear)
- 0x01E0003C (**F_ISPC** – FIQ Interrupt Service Pending Clear)
 - 16b, W, inicial = indefinido
 - Para cada línea de interrupción, permite borrar (escribiendo un 1) el correspondiente bit del registro de solicitudes pendientes (INTPND) para indicar al controlador que la interrupción ha sido servida.

| I_ISPC/F_ISPC | Bit | Description | | Initial State |
|---------------|------|---------------|---------------------------|---------------|
| EINT0 | [25] | 0 = No change | 1 = clear the pending bit | 0 |
| EINT1 | [24] | 0 = No change | 1 = clear the pending bit | 0 |
| EINT2 | [23] | 0 = No change | 1 = clear the pending bit | 0 |
| EINT3 | [22] | 0 = No change | 1 = clear the pending bit | 0 |
| EINT4/5/6/7 | [21] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_TICK | [20] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_ZDMA0 | [19] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_ZDMA1 | [18] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_BDMA0 | [17] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_BDMA1 | [16] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_WDT | [15] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_UERR0/1 | [14] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_TIMER0 | [13] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_TIMER1 | [12] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_TIMER2 | [11] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_TIMER3 | [10] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_TIMER4 | [9] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_TIMER5 | [8] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_URXD0 | [7] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_URXD1 | [6] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_IIC | [5] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_SIO | [4] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_UTXD0 | [3] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_UTXD1 | [2] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_RTC | [1] | 0 = No change | 1 = clear the pending bit | 0 |
| INT_ADC | [0] | 0 = No change | 1 = clear the pending bit | 0 |

Controlador de interrupciones

operación: registro I_ISPR



■ 0x01E00020 (I_ISPR – IRQ Interrupt Service Pending)

- 26b, R, inicial = 0x00000000
- Indica la interrupción que está siendo servida.

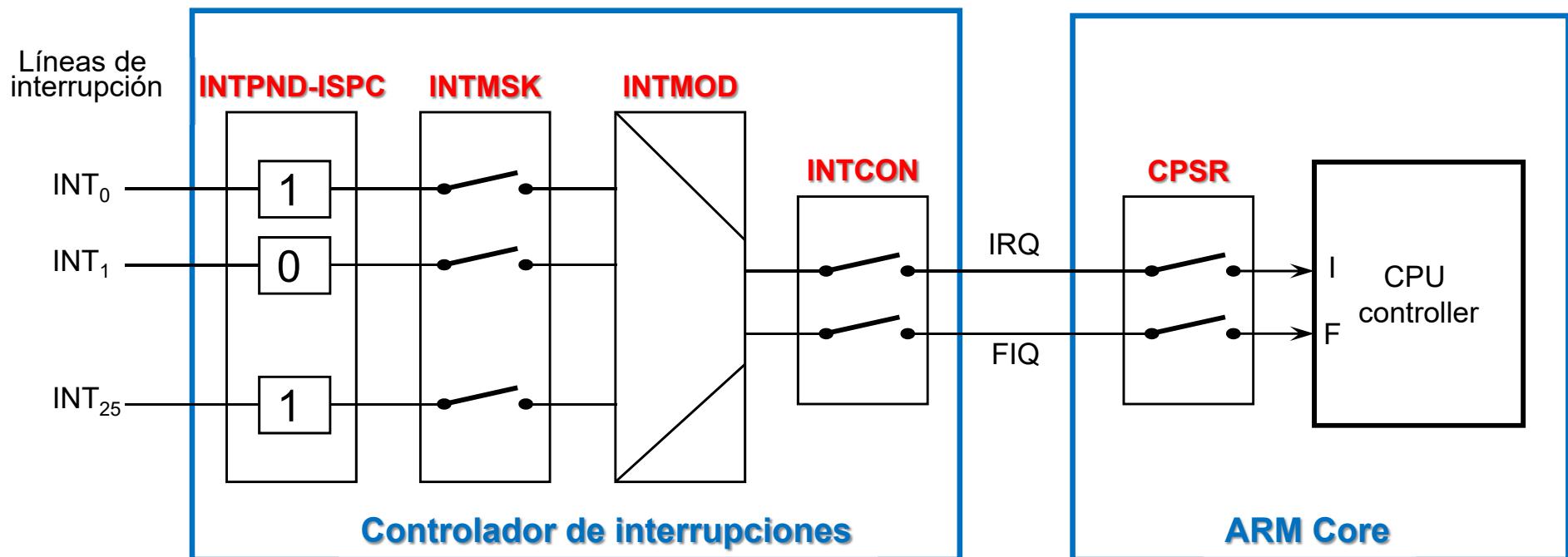
| I_ISPR | Bit | Description | Initial State |
|-------------|------|-----------------------------------|---------------|
| EINT0 | [25] | 0 = not serviced 1 = serviced now | 0 |
| EINT1 | [24] | 0 = not serviced 1 = serviced now | 0 |
| EINT2 | [23] | 0 = not serviced 1 = serviced now | 0 |
| EINT3 | [22] | 0 = not serviced 1 = serviced now | 0 |
| EINT4/5/6/7 | [21] | 0 = not serviced 1 = serviced now | 0 |
| INT_TICK | [20] | 0 = not serviced 1 = serviced now | 0 |
| INT_ZDMA0 | [19] | 0 = not serviced 1 = serviced now | 0 |
| INT_ZDMA1 | [18] | 0 = not serviced 1 = serviced now | 0 |
| INT_BDMA0 | [17] | 0 = not serviced 1 = serviced now | 0 |
| INT_BDMA1 | [16] | 0 = not serviced 1 = serviced now | 0 |
| INT_WDT | [15] | 0 = not serviced 1 = serviced now | 0 |
| INT_UERR0/1 | [14] | 0 = not serviced 1 = serviced now | 0 |
| INT_TIMER0 | [13] | 0 = not serviced 1 = serviced now | 0 |
| INT_TIMER1 | [12] | 0 = not serviced 1 = serviced now | 0 |
| INT_TIMER2 | [11] | 0 = not serviced 1 = serviced now | 0 |
| INT_TIMER3 | [10] | 0 = not serviced 1 = serviced now | 0 |
| INT_TIMER4 | [9] | 0 = not serviced 1 = serviced now | 0 |
| INT_TIMER5 | [8] | 0 = not serviced 1 = serviced now | 0 |
| INT_URXD0 | [7] | 0 = not serviced 1 = serviced now | 0 |
| INT_URXD1 | [6] | 0 = not serviced 1 = serviced now | 0 |
| INT_IIC | [5] | 0 = not serviced 1 = serviced now | 0 |
| INT_SIO | [4] | 0 = not serviced 1 = serviced now | 0 |
| INT_UTXD0 | [3] | 0 = not serviced 1 = serviced now | 0 |
| INT_UTXD1 | [2] | 0 = not serviced 1 = serviced now | 0 |
| INT_RTC | [1] | 0 = not serviced 1 = serviced now | 0 |
| INT_ADC | [0] | 0 = not serviced 1 = serviced now | 0 |



Controlador de interrupciones

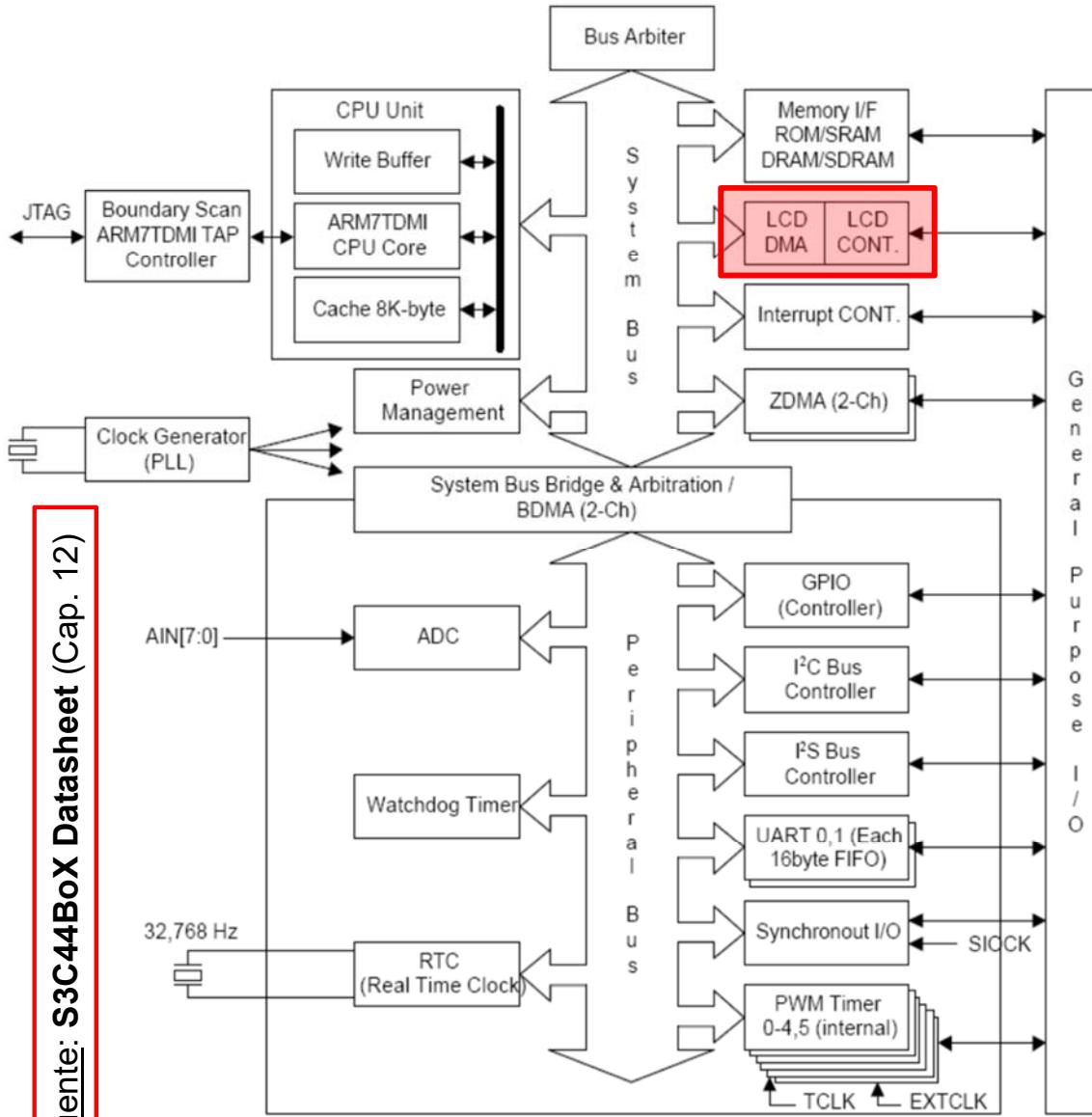
recapitulación

- ¿Qué condiciones tienen que darse para que el procesador sea interrumpido por el periférico conectado a INT_x ?
 - Que el procesador admita interrupciones: $\text{CPSR.F} / \text{CPSR.I} = 0$
 - Que el controlador admita interrupciones: $\text{INTCON.F} / \text{INTCON.I} = 0$
 - Que el controlador no las enmascare: $\text{INTMSK.x} = 0$
 - Que el dispositivo lo solicite: $\text{INT}_x = 1$
 - Dependiendo del valor de INTMOD.x interumpirá por la línea IRQ o por la FIQ.





Controlador de LCD



fuente: **S3C44B0X Datasheet** (Cap. 12)

- Configurable mediante **18 registros** mapeados en memoria (banco 0).

que permiten:

- Indicar las características de la pantalla de LCD conectada al sistema.



Controlador de LCD

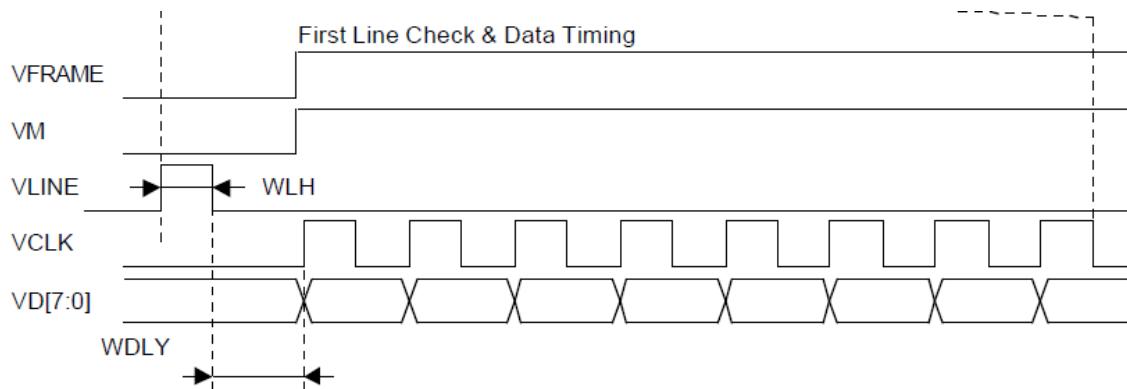
- El S3C44B0X dispone de un controlador genérico de LCD
 - Genera todas las señales requeridas por el LCD leyendo por un DMA propio los datos de un buffer de vídeo localizado en memoria principal:
 - VFRAME: sincronismo vertical
 - VLINE: sincronismo horizontal
 - VD: datos vídeo
 - VCLK: reloj de muestreo de datos de vídeo
 - VM: alternancia de la polaridad del voltaje de fila y columna (apagado/encendido pixel)
 - Soporta varios tipos de **tamaños de pantalla**: 160×160, 320×240 y 640×480
 - Soporta LCDs color (8b/px), monogramo con generación de 4/16 niveles de gris por Frame Rate Control (2b/px y 4b/px) y monocromo puro (1b/px).
 - Soporta varios tipos de **barrido**: 4/8 bits dual/single scan
 - Permite gestionar pantallas virtuales (para scrolling)
 - Puede auto-refrescarse y soporta el modo SL_IDLE del procesador.

Controlador de LCD

configuración: registro LCDCON1 (i)



- 0x01F00000 (LCDCON1 – LCD Control 1)
 - 32b, R/W, inicial = 0x00000000
 - Permite activar/desactivar la salida de vídeo, fijar la polaridad de las señales enviadas al LCD, fijar el tipo de scan, la frecuencia del reloj de muestreo del driver, la forma de onda de la señal VLINE, lo de MVAL.
 - Además permite conocer el valor del contador de línea LINEVAL.



$$\text{frame_rate(Hz)} = 1 / [((1/\text{VCLK}) \times (\text{HOZVAL}+1)) + ((1/\text{MCLK}) \times (\text{WLH}+\text{WDLY}+\text{LINEBLANK})) \times (\text{LINEVAL}+1)]$$

$$\text{VCLK(Hz)} = (\text{HOZVAL}+1) / [(1 / \text{frame_rate} \times (\text{LINEVAL}+1)) - ((\text{WLH}+\text{WDLY}+\text{LINEBLANK}) / \text{MCLK})]$$

LINEVAL = (Vertical display size) -1: In case of single scan display type

LINEVAL = (Vertical display size / 2) -1: In case of dual scan display type

HOZVAL = (Horizontal display size / Number of the valid VD data line) -1

*In color mode: Horizontal display size = 3 * Number of Horizontal Pixel*

Controlador de LCD

configuración: registro LCDCON1 (ii)



| LCDCON1 | Bit | Description | Initial State |
|---------------------|---------|---|---------------|
| LINECNT (read only) | [31:22] | These bits provide the status of the line counter. Down count from LINEVAL to 0 | 0000000000 |
| CLKVAL | [21:12] | These bits determine the rate of VCLK. If this value can be changed when ENVID=1, the new value will be used next frame. $VCLK = MCLK / (CLKVAL \times 2)$ ($CLKVAL \geq 2$) | 0000000000 |
| WLH | [11:10] | These bits determine the VLINE pulse's high level width by counting the number of the system clock. 00 = 4 clock, 01 = 8 clock, 10 = 12 clock, 11 = 16 clock | 00 |
| WDLY | [9:8] | These bits determine the delay between VLINE and VCLK by counting the number of the system clock 00 = 4clock, 01 = 8 clock, 10 = 12 clock, 11 = 16 clock | 00 |
| MMODE | [7] | This bit determines the toggle rate of the VM. 0 = Each Frame, 1 = The rate defined by the MVAL | 0 |
| DISMODE | [6:5] | These bits select the display mode. 00 = 4-bit dual scan display mode 01 = 4-bit single scan display mode 10 = 8-bit single scan display mode 11 = Not used | 00 |
| INVCLK | [4] | This bit controls the polarity of the VCLK active edge. 0 = The video data is fetched at VCLK falling edge 1 = The video data is fetched at VCLK rising edge | 0 |
| INVLIN | [3] | This bit indicates the line pulse polarity. 0 = normal 1 = inverted | 0 |
| INVFRAME | [2] | This bit indicates the frame pulse polarity. 0 = normal 1 = inverted | 0 |
| INVVD | [1] | This bit indicates the video data(VD[7:0]) polarity. 0 = Normal 1 = VD[7:0] output is inverted. | 0 |
| ENVID | [0] | LCD video output and the logic enable/disable. 0 = Disable the video output and the logic. The LCD FIFO is cleared. 1 = Enable the video output and the logic. | 0 |

Controlador de LCD

configuración: registros LCDCON2 y LCDCON3



- **0x01F00004 (LCDCON2 – LCD Control 2)**
 - 32b, R/W, inicial = 0x00000000
 - Permite fijar indirectamente el tamaño en píxeles de la pantalla y la duración del periodo de blanking horizontal.

| LCDCON2 | Bit | Description | Initial State |
|-----------|---------|--|---------------|
| LINEBLANK | [31:21] | These bits indicate the blank time in one horizontal line duration time. These bits adjust the rate of the VLINE finely. The unit of LINEBLANK is MCLK. Ex) If the value of LINEBLANK is 10, the blank time is inserted to VCLK during 10 system clocks. | 0x000 |
| HOZVAL | [20:10] | These bits determine the horizontal size of the LCD panel. HOZVAL has to be determined to meet the condition that total bytes of 1 line be 2n bytes. If the x size of LCD is 120 dots in mono mode, x=120 can not be supported because 1 line consists of 15 bytes. Instead, x=128 in mono mode can be supported because 1 line consists of 16 bytes(2n). The additional 8 dot will be discarded by LCD panel driver. | 0x000 |
| LINEVAL | [9:0] | These bits determine the vertical size of LCD panel. | 0x000 |

- **0x01F00040 (LCDCON3 – LCD Control 3)**
 - 3b, R/W, inicial = 0x0
 - Permite activar el modo self-refresh (soportado por aquellos LCD drivers que dispongan de memoria de refresco interna).

| LCDCON3 | Bit | Description | initial state |
|----------|-------|---|---------------|
| Reserved | [2:1] | reserved for test | 0 |
| SELFREF | [0] | LCD self refresh mode enable bit 0 : LCD self refresh mode disable 1 : LCD self refresh mode enable | 0 |

Controlador de LCD

configuración: registro LCDSADDR1



- 0x01F00008 (LCDSADDR1 – Frame Buffer Start Address 1)
 - 29b, R/W, inicial = 0x00000000
 - Permite fijar el modo del LCD y la dirección de memoria principal en donde comienza el frame buffer (memoria de refresco).

| LCDSADDR1 | Bit | Description | Initial State |
|-----------|---------|---|---------------|
| MODESEL | [28:27] | These bits select the monochrome, gray, or color mode. 00 = monochrome mode 01 = 4-level gray mode 10 = 16-level gray mode 11 = color mode | 00 |
| LCD BANK | [26:21] | These bits indicate A[27:22] of the bank location for the video buffer in the system memory. LCD BANK value can not be changed even when moving the view port. LCD frame buffer should be inside aligned 4MB region, which ensures that LCD BANK value should not be changed when moving the view port. So, using the malloc function care should be taken. | 0x00 |
| LCD BASEU | [20:0] | These bits indicate A[21:1] of the start address of the upper address counter, which is for the upper frame memory of dual scan LCD or the frame memory of single scan LCD. | 0x000000 |

NOTES:

1. LCD BANK can't be changed while ENVID=1
2. If LCD BASEU, LCD BASEL is changed during ENVID=1, the new value will be used next frame. If you use several frame buffer for better display quality and if you write the previous frame memory just after changing LCD BASEU, LCD BASEL, the items drawn on the previous frame memory may be shown. To avoid this undesirable phenomenon, you may have to check LINECNT.

Controlador de LCD

configuración: registro LCDSADDR2



- 0x01F0000C (**LCDSADDR2 – Frame Buffer Start Address 2**)
 - 30b, R/W, inicial = 0x00000000
 - Permite fijar la dirección de memoria principal en donde comienza la segunda porción del frame buffer (dual scan LCD) y la frecuencia de cambio de VM.

| LCDSADDR2 | Bit | Description | Initial State |
|-----------|---------|--|---------------|
| BSWP | [29] | Byte swap control bit 1 : Swap Enable 0 : Swap Disable LCD DMA fetches the frame memory data by 4 word burst access. In little endian mode and BSWP is 0, the frame memory data are displayed in the sequence, 4n+3th, 4n+2th ,4n+1th ,4n-th data. If BSWP is 1, the sequence will be 4n-th, 4n+1th, 4n+2th, 4n+3th. If the CPU is little endian mode, the frame buffer may be accessed by only byte access mode, Because BSWP is 1, the byte accessed data will be shown correctly also in the little endian mode. In the other case, BSWP has to be 0. | 0 |
| MVAL | [28:21] | These bits define the rate at which the VM signal will toggle if the MMODE bit is set to logic '1'. | 0x00 |
| LCDBASEL | [20:0] | These bits indicate A[21:1] of the start address of the lower address counter, which is used for the lower frame memory of dual scan LCD. LCDBASEL = $\text{LCDBASEU} + (\text{PAGEWIDTH} + \text{OFFSIZE}) \times (\text{LINEVAL} + 1)$ | 0x0000 |

NOTE: Users can change the LCDBASEU and LCDBASEL values for scrolling while LCD controller is turned on. But, users

must not change the LCDBASEU and LCDBASEL registers at the end of FRAME by referring to the LINECNT field in LCDCON1 register. Because of the LCD FIFO fetches the next frame data prior to the change in the frame. So, if you change the frame, the pre-fetched FIFO data will be obsolete and LCD controller will display the incorrect screen. To check the LINECNT, interrupt should be masked. If any interrupt is executed just after reading LINECNT, the read LINECNT value may be obsolete because of the execution time of ISR(interrupt service routine).

Controlador de LCD

configuración: registro LCDSADDR3



- **0x01F00010 (LCDSADD3 – Frame Buffer Start Address 3)**
 - 20b, R/W, inicial = 0x00000
 - Permite fijar indirectamente el tamaño de la línea de la pantalla virtual y la porción de esta línea que debe visualizarse en el LCD.

| LCDSADDR3 | Bit | Description | Initial State |
|-----------|--------|--|---------------|
| OFFSIZE | [19:9] | Virtual screen offset size(the number of half words) This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line. | 0x0000 |
| PAGEWIDTH | [8:0] | Virtual screen page width(the number of half words) This value defines the width of the view port in the frame | 0x000 |

NOTE: The values of PAGEWIDTH and OFFSIZE must be changed when ENVID bit is 0.



Controlador de LCD

configuración: registros xLUT

- **0x01F00014 (REDLUT – Red Lookup Table)**
 - 32b, R/W, inicial = 0x00000000
- **0x01F00018 (GREENLUT – Green Lookup Table)**
 - 32b, R/W, inicial = 0x00000000
- **0x01F0001C (BLUELUT – Blue Lookup Table)**
 - 16b, R/W, inicial = 0x0000
 - Paletas de color rojo/verde/azul. La paleta azul se usa en modo 4 niveles de gris.

| REDLUT | Bit | Description | Initial State | | | | | | | | |
|------------------------|-----------------------|--|----------------------|---------------------|-----------------------|-----------------------|------------------------|-----------------------|------------------------|-----------------------|------------|
| REDVAL | [31:0] | <p>These bits define which of the 16 shades each of the 8 possible red combinations will choose.</p> <table style="margin-left: 20px; margin-top: 0;"> <tr><td>000 = REDVAL[3:0],</td><td>001 = REDVAL[7:4]</td></tr> <tr><td>010 = REDVAL[11:8],</td><td>011 = REDVAL[15:12]</td></tr> <tr><td>100 = REDVAL[19:16],</td><td>101 = REDVAL[23:20]</td></tr> <tr><td>110 = REDVAL[27:24],</td><td>111 = REDVAL[31:28]</td></tr> </table> | 000 = REDVAL[3:0], | 001 = REDVAL[7:4] | 010 = REDVAL[11:8], | 011 = REDVAL[15:12] | 100 = REDVAL[19:16], | 101 = REDVAL[23:20] | 110 = REDVAL[27:24], | 111 = REDVAL[31:28] | 0x00000000 |
| 000 = REDVAL[3:0], | 001 = REDVAL[7:4] | | | | | | | | | | |
| 010 = REDVAL[11:8], | 011 = REDVAL[15:12] | | | | | | | | | | |
| 100 = REDVAL[19:16], | 101 = REDVAL[23:20] | | | | | | | | | | |
| 110 = REDVAL[27:24], | 111 = REDVAL[31:28] | | | | | | | | | | |
| GREENLUT | Bit | Description | Initial State | | | | | | | | |
| GREENVAL | [31:0] | <p>These bits define which of the 16 shades each of the 8 possible green combinations will choose.</p> <table style="margin-left: 20px; margin-top: 0;"> <tr><td>000 = GREENVAL[3:0],</td><td>001 = GREENVAL[7:4]</td></tr> <tr><td>010 = GREENVAL[11:8],</td><td>011 = GREENVAL[15:12]</td></tr> <tr><td>100 = GREENVAL[19:16],</td><td>101 = GREENVAL[23:20]</td></tr> <tr><td>110 = GREENVAL[27:24],</td><td>111 = GREENVAL[31:28]</td></tr> </table> | 000 = GREENVAL[3:0], | 001 = GREENVAL[7:4] | 010 = GREENVAL[11:8], | 011 = GREENVAL[15:12] | 100 = GREENVAL[19:16], | 101 = GREENVAL[23:20] | 110 = GREENVAL[27:24], | 111 = GREENVAL[31:28] | 0x00000000 |
| 000 = GREENVAL[3:0], | 001 = GREENVAL[7:4] | | | | | | | | | | |
| 010 = GREENVAL[11:8], | 011 = GREENVAL[15:12] | | | | | | | | | | |
| 100 = GREENVAL[19:16], | 101 = GREENVAL[23:20] | | | | | | | | | | |
| 110 = GREENVAL[27:24], | 111 = GREENVAL[31:28] | | | | | | | | | | |
| BULELUT | Bit | Description | Initial State | | | | | | | | |
| BLUEVAL | [15:0] | <p>These bits define which of the 16 shades each of the 4 possible blue combinations will choose</p> <table style="margin-left: 20px; margin-top: 0;"> <tr><td>00 = BLUEVAL[3:0],</td><td>01 = BLUEVAL[7:4]</td></tr> <tr><td>10 = BLUEVAL[11:8],</td><td>11 = BLUEVAL[15:12]</td></tr> </table> | 00 = BLUEVAL[3:0], | 01 = BLUEVAL[7:4] | 10 = BLUEVAL[11:8], | 11 = BLUEVAL[15:12] | 0x0000 | | | | |
| 00 = BLUEVAL[3:0], | 01 = BLUEVAL[7:4] | | | | | | | | | | |
| 10 = BLUEVAL[11:8], | 11 = BLUEVAL[15:12] | | | | | | | | | | |



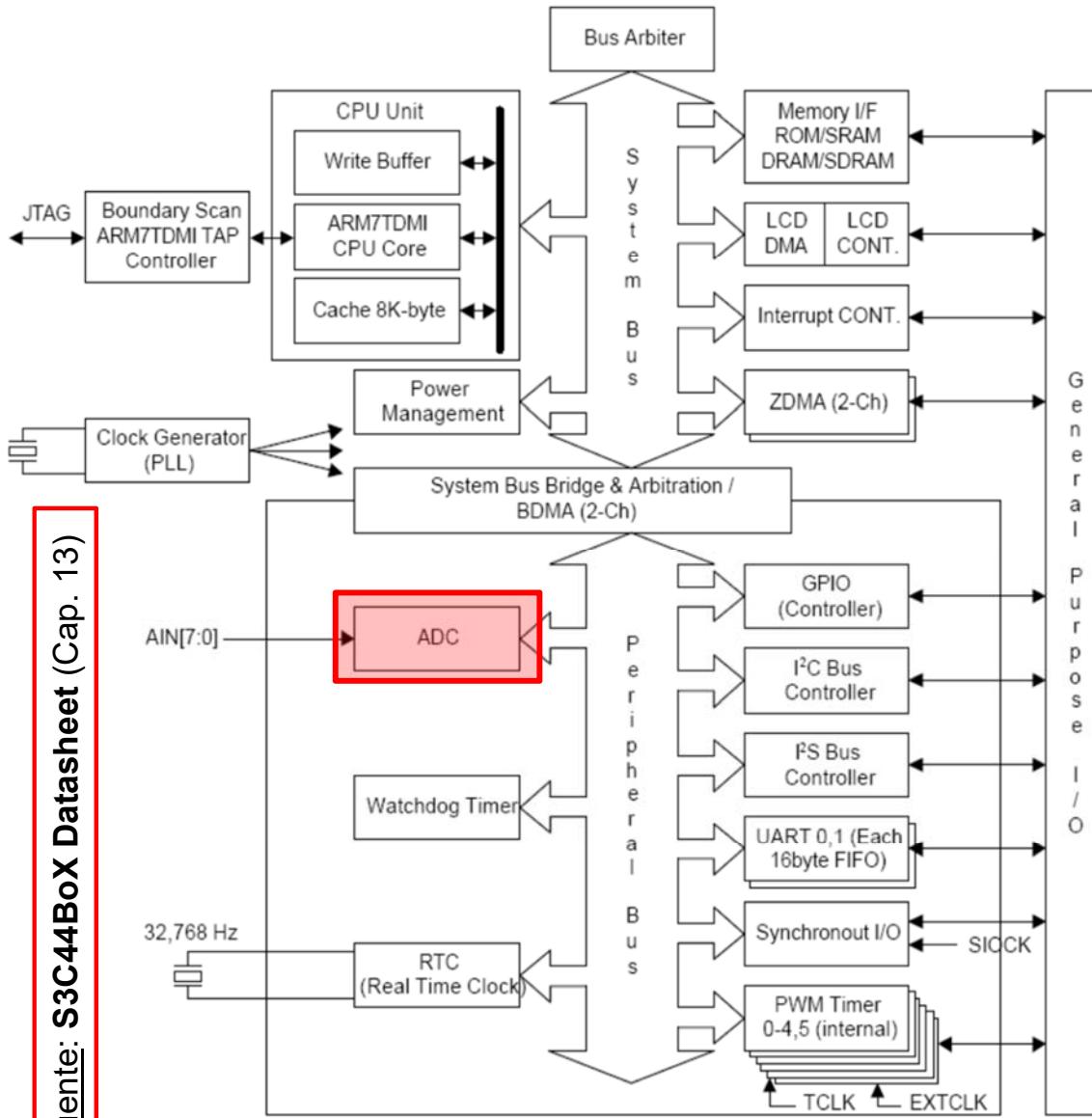
Controlador de LCD

configuración: registros DITHMODE y Dlx_x

- 0x01F0001C (**DITHMODE – Dithering Mode**)
 - 19b, R/W, inicial = 0x00000 (debe programarse a 0x12210).
- 0x01F00020 (**DP1_2 – Dithering Pattern Duty 1/2**)
 - 16b, R/W, inicial = 0xA5A5 (recomendado)
- 0x01F00024 (**DP4_7 – Dithering Pattern Duty 4/7**)
 - 28b, R/W, inicial = 0xBA5DA65 (recomendado)
- 0x01F0_0028 (**DP3_5 – Dithering Pattern Duty 3/5**)
 - 20b, R/W, inicial = 0xA5A5F (recomendado)
- 0x01F0002C (**DP2_3 – Dithering Pattern Duty 2/3**)
 - 12b, R/W, inicial = 0xD6B (recomendado)
- 0x01F00030 (**DP5_7 – Dithering Pattern Duty 5/7**)
 - 28b, R/W, inicial = 0xEB7B5ED (recomendado)
- 0x01F00034 (**DP3_4 – Dithering Pattern Duty 3/4**)
 - 16b, R/W, inicial = 0x7DBE (recomendado)
- 0x01F00038 (**DP4_5 – Dithering Pattern Duty 4/5**)
 - 20b, R/W, inicial = 0x7EBDF (recomendado)
- 0x01F0003C (**DP6_7 – Dithering Pattern Duty 6/7**)
 - 28b, R/W, inicial = 0x7FDFBF (recomendado)



Conversor analógico digital



- Configurable mediante 3 registros mapeados en memoria.

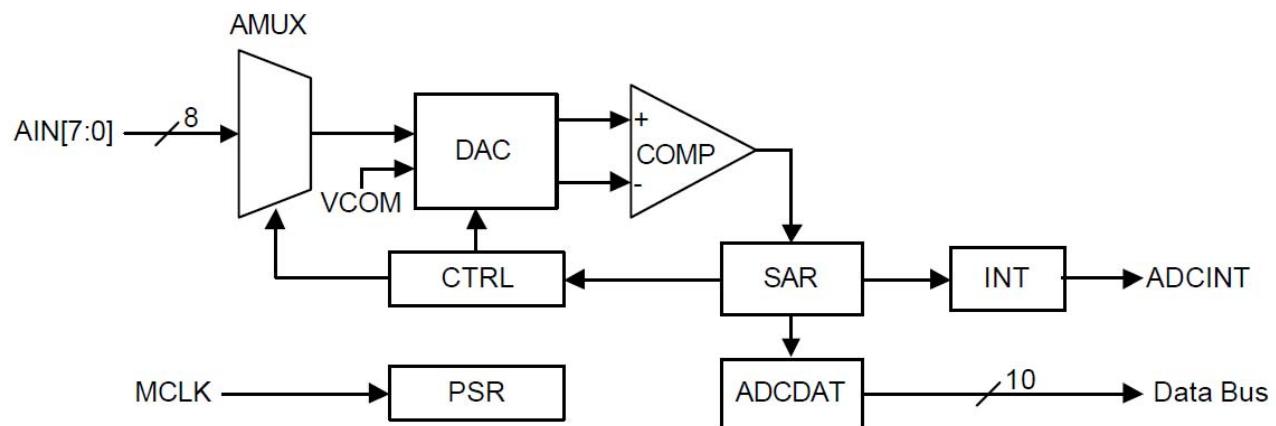
que permiten:

- seleccionar el canal analógico a muestrear.
- fijar el tiempo de muestreo.



Conversor analógico digital

- El S3C44B0X dispone de un conversor A/D:
 - 8 canales analógicos multiplexados de entrada.
 - 10b de resolución.
 - frecuencia máxima de muestreo: 100 kSPS.
 - frecuencia máxima de entrada: 100 Hz.
- Realiza la conversión mediante la comparación sucesiva de la señal de entrada y la generada por un conversor D/A conectado a un registro de aproximación.



Conversor analógico digital

configuración y operación: registro ADDCON



- 0x01D40000 (**ADCCON – A/D Converter Control**)
 - 7b, R/W, inicial = 0x20,
 - Permite habilitar/deshabilitar el conversor, seleccionar el canal analógico fuente, conocer el estado de la conversión y fijar el modo de iniciar una conversión.
 - Tras un cambio de canal deben esperarse 10 µs
 - Tras la habilitación del conversor deben esperarse 10 ms

| ADCCON | Bit | Description | Initial State |
|--------------|-------|--|---------------|
| FLAG | [6] | A/D converter state flag (Read Only). 0 = A/D conversion in process 1 = End of A/D conversion If check this bit please refer to workaround in page13-3. | 0 |
| SLEEP | [5] | System power down 0 = Normal operation, 1 = Sleep mode | 1 |
| INPUT SELECT | [4:2] | Clock source select 000 = AIN0 001 = AIN1 010 = AIN2 011 = AIN3 100 = AIN4 101 = AIN5 110 = AIN6 111 = AIN7 | 00 |
| READ_START | [1] | A/D conversion start by read 0 = Disable start by read operation 1 = Enable start by read operation | 00 |
| ENABLE_START | [0] | A/D conversion start by enable. If READ_START is enabled, this value is not valid. 0 = No operation 1 = A/D conversion starts and this bit is cleared after the start-up. | 0 |

Conversor analógico digital

configuración y operación: registros ADDCON/DAT

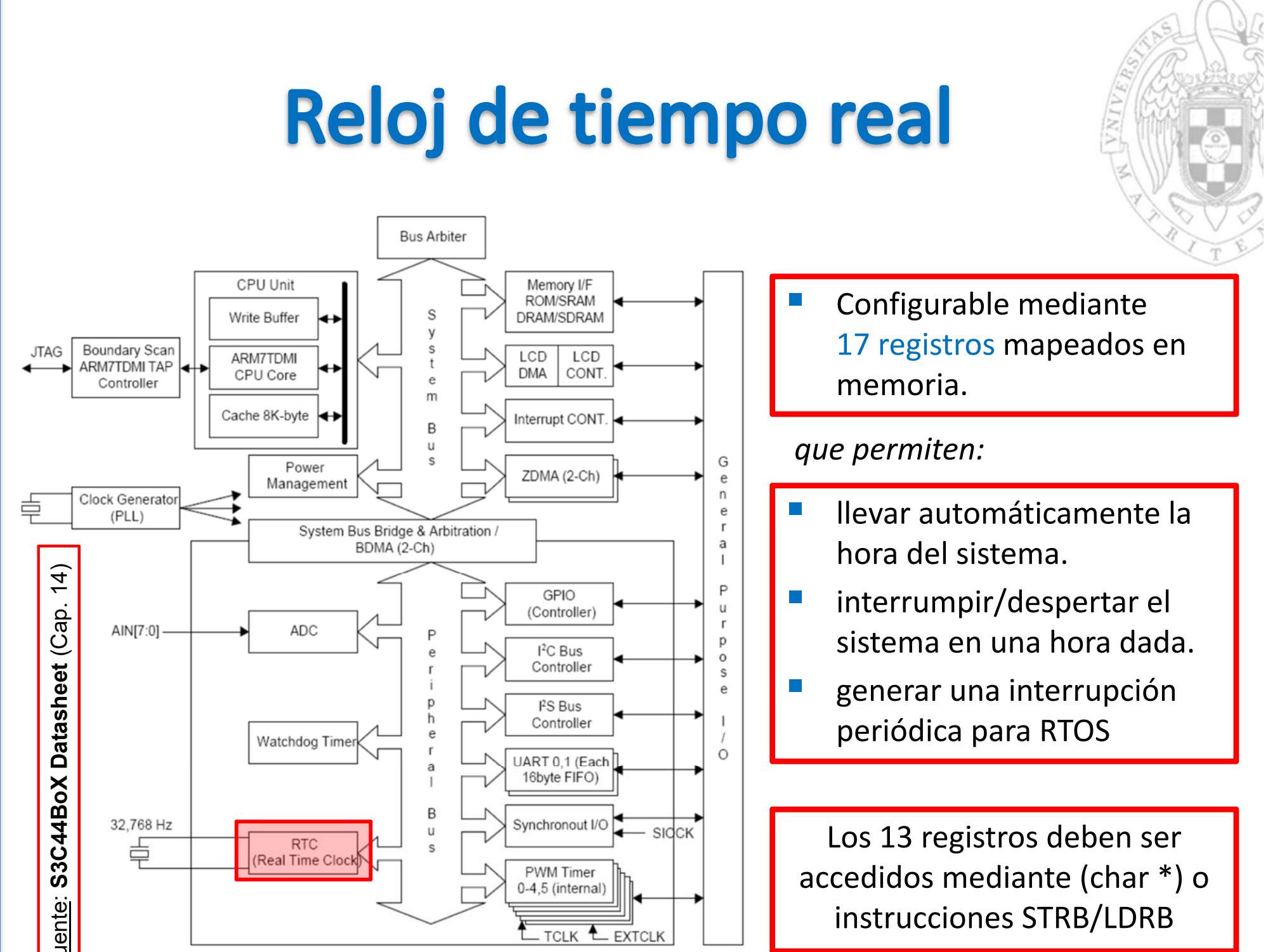


- 0x01D00004 (ADCPSR – A/D Converter Prescaler)
 - 8b, R/W, inicial = 0x00
 - Fija el tiempo de conversión A/D.

| ADCPSR | Bit | Description | Initial State |
|-----------|-------|---|---------------|
| PRESCALER | [7:0] | Prescaler value (0-255) Division factor = 2 (prescaler_value+1). Total clocks for ADC converstion = 2*(Prescalser_value+1)*16 | 0 |

- 0x01D00008 (ADCDAT – A/D Converter Data)
 - 10b, R, inicial = indefinido
 - Registro de datos de conversión.

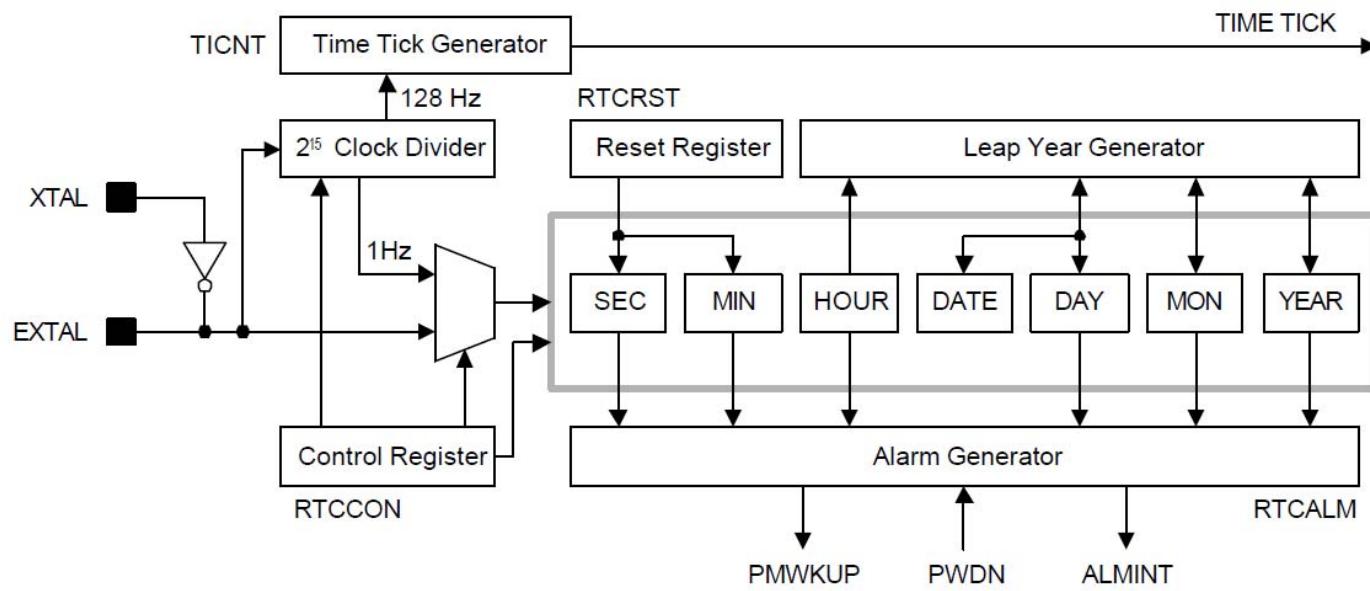
| ADCDAT | Bit | Description | Initial State |
|--------|-------|---------------------------------|---------------|
| ADCDAT | [9:0] | A/D converter output data value | - |





Reloj de tiempo real

- El S3C44B0X dispone de **reloj de tiempo real**:
 - Que incluye desde el segundo hasta el año.
 - Con función alarma para generar una interrupción (ALMINT) en una hora y fecha determinada (y en modo power-down además activa PMWKUP)
 - Con funcionamiento autónomo por batería cuando el SoC está apagado.
 - Con generación de interrupciones periódicas (tick de RTOS).
 - Con función de redondeo en puesta a 0 de segundos.



Reloj de tiempo real

configuración y operación: registro RTCCON



- 0x01D70040 (**RTCCON – RTC Control**)
 - 4b, R/W, inicial = 0x0
 - Permite seleccionar la fuente de reloj, resetear los contadores y habilitar/deshabilitar la posibilidad de lectura de los registros del RTC (opción de bajo consumo).

| RTCCON | Bit | Description | Initial State |
|--------|-----|--|---------------|
| CLKRST | [3] | RTC clock count reset 0 = No reset, 1 = Reset | 0 |
| CNTSEL | [2] | BCD count select 0 = Merge BCD counters 1 = Reserved (Separate BCD counters) | 0 |
| CLKSEL | [1] | BCD clock select 0 = XTAL 1/2 ¹⁵ divided clock 1 = Reserved (XTAL clock only for test) | 0 |
| RTCEN | [0] | RTC read/write enable 0 = Disable, 1 = Enable If RTC read/write feature is enabled, The STOP current will be consumed excessively. To reduce STOP current, this bit should be 0 while not accessing RTC. Although this bit is 0, the RTC clock is still alive. | 0 |

Reloj de tiempo real

operación: registro RTCALM



- 0x01D70050 (**RTCALM – RTC Alarm Control**)
 - 8b, R/W, inicial = 0x00
 - Permite habilitar/deshabilitar la alarma.

| RTCALM | Bit | Description | Initial State |
|----------|-----|--|---------------|
| Reserved | [7] | | 0 |
| ALMEN | [6] | Alarm global enable 0 = Disable, 1 = Enable | 0 |
| YEAREN | [5] | Year alarm enable 0 = Disable, 1 = Enable | 0 |
| MONREN | [4] | Month alarm enable 0 = Disable, 1 = Enable | 0 |
| DAYEN | [3] | Day alarm enable 0 = Disable, 1 = Enable | 0 |
| HOUREN | [2] | Hour alarm enable 0 = Disable, 1 = Enable | 0 |
| MINEN | [1] | Minute alarm enable 0 = Disable, 1 = Enable | 0 |
| SECEN | [0] | Second alarm enable 0 = Disable, 1 = Enable | 0 |



Reloj de tiempo real

configuración y operación: registros RTCRST y TICNT

- 0x01D7006C (RTCRST – RTC Round Reset)
 - 4b, R/W, inicial = 0x0
 - Permite habilitar/deshabilitar el redondeo de segundos en reset.

| RTCRST | Bit | Description | Initial State |
|--------|-------|--|---------------|
| SRSTEN | [3] | Round second reset enable 0 = Disable, 1 = Enable | 0 |
| SECCR | [2:0] | Round boundary for second carry generation. (note) 011 = over than 30 sec 100 = over than 40 sec 101 = over than 50 sec | 00 |

- 0x01D7006C (TICNT – Tick Time Counter)
 - 8b, R/W, inicial = 0x00
 - Habilita/deshabilita interrupciones periódicas.

| TICNT | Bit | Description | Initial State |
|-----------------|-------|---|---------------|
| TICK INT ENABLE | [7] | Tick time interrupt enable 0 = disable 1 = enable | 0 |
| TICK TIME COUNT | [6:0] | Tick time count value. (1-127) This counter value decreases internally, and users can not read this real counter value in working. | 000000 |

Period = (n+1) / 128 second
 n : Tick time count value (1-127)

Reloj de tiempo real

operación: registros BCDxxx



- 0x01D70070 (**BCDSEC** – BCD Second Data)
- 0x01D70074 (**BCDMIN** – BCD Minute Data)
- 0x01D70078 (**BCDHOUR** – BCD Hour Data)
- 0x01D7007C (**BCDDAY** – BCD Day Data)
- 0x01D70080 (**BCDDATE** – BCD Date Data)
- 0x01D70084 (**BCDMON** – BCD Month Data)
- 0x01D70088 (**BCDYEAR** – BCD Year Data)
 - 8b, R/W, inicial = indefinido
 - Valor BCD del segundo/minuto/hora/día/dia de la semana/mes/año del reloj.
 - Deben leerse de YEAR a SEC, y si SEC=0 repetir la lectura porque puede haber inconsistencia por la posible desviación de un segundo debida a la lectura de múltiples registros.

| BCDSEC | Bit | |
|----------|-------|----------------------------------|
| Reserved | [7] | |
| SECDATA | [6:4] | BCD value for second from 0 to 5 |
| | [3:0] | from 0 to 9 |
| BCDMIN | Bit | |
| Reserved | [7] | |
| MINDATA | [6:4] | BCD value for minute from 0 to 5 |
| | [3:0] | from 0 to 9 |
| BCDHOUR | Bit | |
| Reserved | [7:6] | |
| HOURDATA | [5:4] | BCD value for hour from 0 to 2 |
| | [3:0] | from 0 to 9 |
| BCDDAY | Bit | |
| Reserved | [7:6] | |
| DAYDATA | [5:4] | BCD value for day from 0 to 3 |
| | [3:0] | from 0 to 9 |
| BCDDATE | Bit | |
| Reserved | [7:3] | |
| DATEDATA | [2:0] | BCD value for date from 1 to 7 |
| BCDMON | Bit | |
| Reserved | [7:5] | |
| MONDATA | [4] | BCD value for month from 0 to 1 |
| | [3:0] | from 0 to 9 |
| BCDYEAR | Bit | |
| YEARDATA | [7:0] | BCD value for year from 00 to 99 |

Reloj de tiempo real

operación: registros ALMxxx

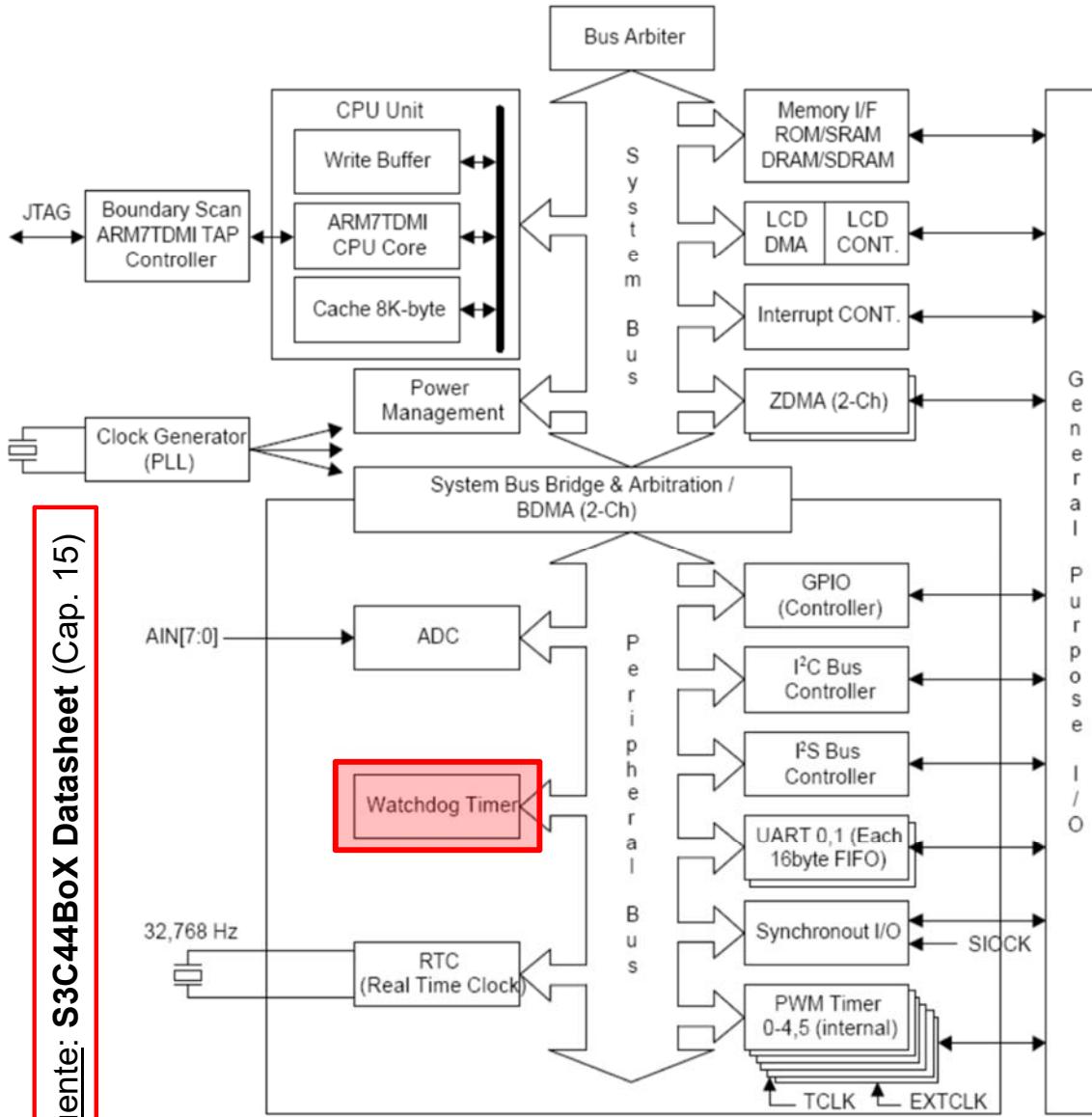


- 0x01D70054 (**ALMSEC** – Alarm Second Data)
- 0x01D70058 (**ALMMIN** – Alarm MinuteData)
- 0x01D7005C (**ALMHOUR** – Alarm Hour Data)
- 0x01D70060 (**ALMDAY** – Alarm Day Data)
- 0x01D70064 (**ALMMON** – Alarm Month Data)
- 0x01D70068 (**ALMYEAR** – Alarm Year Data)
 - 8b, R/W, inicial = 0x00
 - Valor BCD del segundo/minuto/hora/día/mes/año de la alarma.

| ALMSEC | Bit | |
|----------|-------|--|
| Reserved | [7] | |
| SECDATA | [6:4] | BCD value for alarm second from 0 to 5 |
| | [3:0] | from 0 to 9 |
| ALMMIN | Bit | |
| Reserved | [7] | |
| MINDATA | [6:4] | BCD value for alarm minute from 0 to 5 |
| | [3:0] | from 0 to 9 |
| ALMHOUR | Bit | |
| Reserved | [7:6] | |
| HOURDATA | [5:4] | BCD value for alarm hour from 0 to 2 |
| | [3:0] | from 0 to 9 |
| ALMDAY | Bit | |
| Reserved | [7:6] | |
| DAYDATA | [5:4] | BCD value for alarm day from 0 to 3 |
| | [3:0] | from 0 to 9 |
| ALMMON | Bit | |
| Reserved | [7:5] | |
| MONDATA | [4] | BCD value for alarm month from 0 to 1 |
| | [3:0] | from 0 to 9 |
| ALMYEAR | Bit | |
| YEARDATA | [7:0] | BCD value for year from 00 to 99 |



Watchdog timer



- Configurable mediante 3 registros mapeado en memoria (banco 0).

que permiten:

- Fijar su modo de funcionamiento.
- Iniciar y parar la cuentas.



Watchdog timer

- Un watchdog es un temporizador especial que permite:
 - Resetear el sistema tras un cierto timeout (recuperación de bloqueos)
 - Generar interrupciones periódicas.
- El S3C44B0X dispone de **watchdog** de 16 bits formado por:
 - 1 contador descendente que lleva la cuenta del temporizador (WDCNT)
 - 1 registro que almacena el valor inicial de la cuenta (WDDAT)
- La **frecuencia** del contador se deriva de la del reloj del sistema
 - Programando 1 módulo de pre-escalado y 1 divisor de frecuencia.
- Según la configuración, cuando WDCNT llega a 0:
 - Se recarga con el valor de WDDAT
 - Genera una interrupción
 - Genera una excepción de RESET.

Watchdog timer

configuración y operación: registro WTCON



- 0x01D30000 (WTCON – Watchdog Timer Control)
 - 16b, R/W, inicial = 0x8021
 - Permite fijar la frecuencia del reloj base usada por el temporizador, así como habilitar/deshabilitar: el temporizador, la generación de interrupciones y la activación de la señal de reset tras time-out.

| WTCON | Bit | Description | Initial State |
|-------------------------------|--------|--|---------------|
| Prescaler value | [15:8] | the prescaler value The valid range is from 0 to (2^8 -1) | 0x80 |
| Reserved | [7:6] | Reserved. These two bits must be 00 in normal operation. | 00 |
| watchdog timer enable/disable | [5] | Enable or disable bit of watchdog timer. 0 = Disable watchdog timer 1 = Enable watchdog timer | 1 |
| Clock select | [4:3] | This two bits determines the clock division factor 00: 1/16 01: 1/32 10: 1/64 11: 1/128 | 00 |
| Interrupt enable/disable | [2] | Enable or disable bit of the interrupt. 0 = Disable interrupt generation 1 = Enable interrupt generation | 0 |
| Reserved | [1] | Reserved. This bit must be 0 in normal operation | 0 |
| Reset enable/disable | [0] | Enable or disable bit of watchdog timer output for reset signal 1: asserts reset signal of the S3C44B0X at watchdog time-out 0: disables the reset function of the watchdog timer. | 1 |

$$t_{\text{watchdog}} = 1 / (\text{MCLK} / (\text{Prescaler value} + 1) / \text{Division_factor})$$

Watchdog timer

configuración y operación: registros WTDAT y WTCNT



- 0x01D30004 (**WTDAT** – Watchdog Timer Data)
 - 16b, R/W, inicial = 0x8000
 - Permite fijar la duración del time-out (como número de ciclos del reloj base).

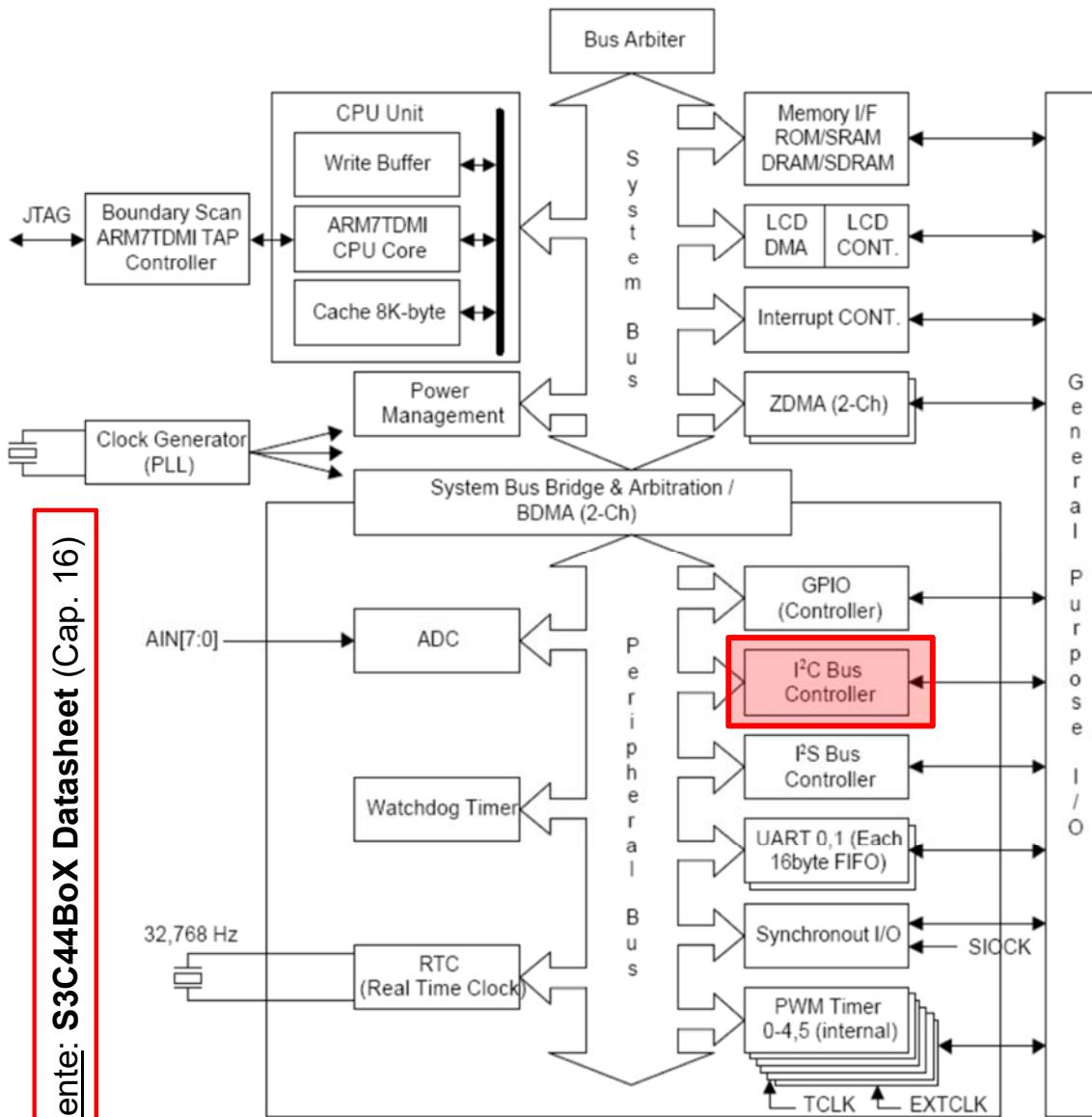
| WTDAT | Bit | Description | Initial State |
|--------------------|--------|--|---------------|
| Count reload value | [15:0] | Watchdog timer count value for reload. | 0x8000 |

- 0x01D30008 (**WTCNT** – Watchdog Timer Count)
 - 16b, R/W, inicial = 0x8000
 - Indica el valor actual de la cuenta de ciclos. Cuando llega el time-out se carga automáticamente con el valor de WTDAT, excepto cuando se habilita el watchdog por primera vez en cuyo caso debe ser escrito explícitamente.

| WTCNT | Bit | Description | Initial State |
|-------------|--------|---|---------------|
| Count value | [15:0] | The current count value of the watchdog timer | 0x8000 |



Controlador de IIC



fuente: **S3C44B0X Datasheet** (Cap. 16)

- Configurable mediante 4 **registros** mapeados en memoria (banco 0).

que permiten:

- Configurar el modo de funcionamiento del canal.
- Ordenar y controlar las transferencias serie.



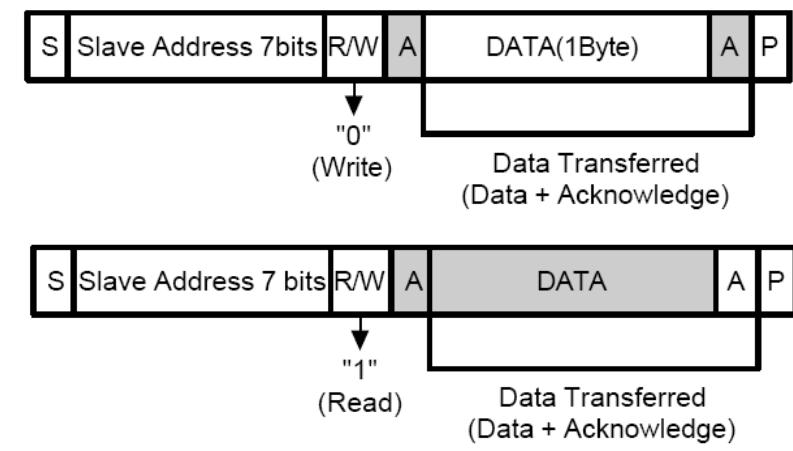
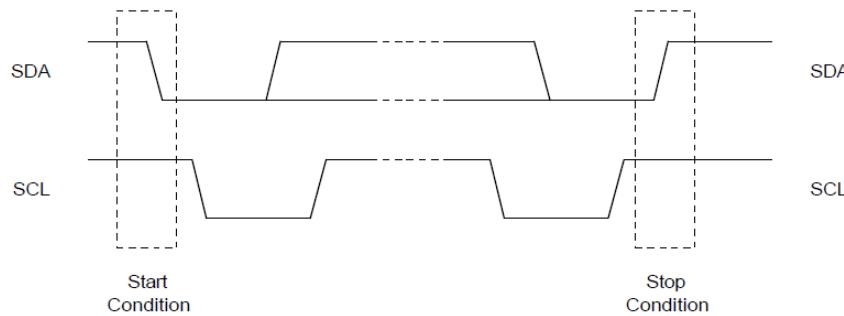
Bus IIC

- IIC (Inter Integrated Circuits) es un **bus serie síncrono multi-master**
 - Tiene 2 líneas bidireccionales: **SDA** (datos serie) y **SCL** (reloj).
 - Si el bus está libre ambas están en alta.
 - Comunicación master-slave
 - El maestro gobierna el inicio/fin de las transferencia y genera el reloj.
 - Puede haber varios maestros/esclavos conectados en un mismo bus
 - Existe un mecanismo de arbitraje.
 - Todos los datos transmitidos son de 8 bits (MSB first) y deben ser reconocidos individualmente (ACK).
 - Soporta altas tasas de transferencia (hasta 400 Kb/s)
- **Protocolo básico:**
 - El maestro inicia la transmisión generando la start condition (transición 1-0 en SDA).
 - todos los esclavos se ponen en alerta
 - El maestro envía la dirección del esclavo (7b) y el tipo de operación R/W (1b)
 - todos esclavos comparan la dirección con la suya y el esclavo aludido envía ACK
 - si la dirección es de 10b se envía en 2 trozos
 - Se transmiten un numero indefinido de datos (8b) reconocidos individualmente (1b).
 - El maestro finaliza la transmisión generando la stop condition (transición 0-1 en SDA)



Controlador de IIC

- El S3C44B0X dispone de un controlador de interfaz bus IIC con 4 modos de operación:
 - **Master transmitter**: el microprocesador actúa como maestro y envía datos a un esclavo.
 - **Master receive**: el microprocesador actúa como maestro y recibe datos de un esclavo.
 - **Slave transmitter**: el microprocesador actúa como esclavo y envía datos a un maestro.
 - **Slave receive**: el microprocesador actúa como esclavo y recibe datos de un maestro.
- El controlador se encarga de gestionar la señalización/transferencia de datos individuales.



Controlador de IIC

configuración: registro ICCCON



■ 0x01D60000 (ICCCON – IIC-Bus Control)

- 8b, R/W, inicial = 0x8X
- Permite indicar la frecuencia del reloj de transmisión, gestionar interrupciones, habilitar la generación del ACK.

| IICCON | Bit | Description | Initial State |
|--------------------------------|-------|---|---------------|
| Acknowledge enable (1) | [7] | IIC-bus acknowledge enable bit 0=Disable ACK generation 1=Enable ACK generation In Tx mode, the IICSDA is free in the ack time. In Rx mode, the IICSDA is L in the ack time. | 0 |
| Tx clock source selection | [6] | Source clock of IIC-bus transmit clock prescaler selection bit 0 = IICCLK = $f_{MCLK}/16$ 1 = IICCLK = $f_{MCLK}/512$ | 0 |
| Tx/Rx Interrupt enable | [5] | IIC-Bus Tx/Rx interrupt enable/disable bit 0 = Disable interrupt, 1 = Enable interrupt | 0 |
| Interrupt pending flag (2) (3) | [4] | IIC-bus Tx/Rx interrupt pending flag. Writing 1 is impossible. When this bit is read as 1, the IICSCL is tied to L and the IIC is stopped. To resume the operation, clear this bit as 0. 0 = 1) No interrupt pending (when read), 2) Clear pending condition & Resume the operation (when write). 1 = 1) Interrupt is pending (when read) 2) N/A (when write) | 0 |
| Transmit clock value (4) | [3:0] | IIC-Bus transmit clock prescaler IIC-Bus transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: $Tx\ clock = IICCLK/(IICCON[3:0]+1)$ | Undefined |

NOTES:

1. Interfacing with EEPROM, the ack generation may be disabled before reading the last data in order to generate the STOP condition in Rx mode.
2. A IIC-bus interrupt occurs 1)when a 1-byte transmit or receive operation is completed, 2)when a general call or a slave address match occurs, or 3) if bus arbitration fails.
3. To time the setup time of IICSDA before IICSCL rising edge, IICDS has to be written before clearing the IIC interrupt pending bit.
4. IICCLK is determined by IICCON[6].
Tx clock can vary by SCL transition time.
When IICCON[6]=0, IICCON[3:0]=0x0 or 0x1 is not available.
5. If the IICON[5]=0, IICON[4] does not operate correctly.
So, it is recommended to set IICCON[5]=1, although you does not use the IIC interrupt.



Controlador de IIC

configuración y operación: registro ICCSTAT



- 0x01D60004 (**IICSTAT – IIC-Bus Control/Status**)
 - 8b, R/W, inicial = 0x00
 - Permite fijar el modo de transmisión, habilitarla y conocer el estado de la misma.

| IICSTAT | Bit | Description | Initial State |
|--|-------|--|---------------|
| Mode selection | [7:6] | IIC-bus master/slave Tx/Rx mode select bits: 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode | 0 |
| Busy signal status/ START STOP condition | [5] | IIC-Bus busy signal status bit: 0 = read) IIC-bus not busy (when read) write) IIC-bus STOP signal generation 1 = read) IIC-bus busy (when read) write) IIC-bus START signal generation. The data in IICDS will be transferred automatically just after the start signal. | 0 |
| Serial output enable | [4] | IIC-bus data output enable/disable bit: 0=Disable Rx/Tx, 1=Enable Rx/Tx | 0 |
| Arbitration status flag | [3] | IIC-bus arbitration procedure status flag bit: 0 = Bus arbitration successful 1 = Bus arbitration failed during serial I/O | 0 |
| Address-as-slave status flag | [2] | IIC-bus address-as-slave status flag bit: 0 = cleared when START/STOP condition was detected 1 = Received slave address matches the address value in the IICADD. | 0 |
| Address zero status flag | [1] | IIC-bus address zero status flag bit: 0 = cleared when START/STOP condition was detected. 1 = Received slave address is 00000000b | 0 |
| Last-received bit status flag | [0] | IIC-bus last-received bit status flag bit 0 = Last-received bit is 0 (ACK was received) 1 = Last-receive bit is 1 (ACK was not received) | 0 |



Controlador de IIC

operación: registros ICCADD e ICCDS

- 0x01D60008 (IICADD – IIC-Bus Address)
 - 8b, R/W, inicial = indefinido
 - Dirección del dispositivo esclavo conectado al bus IIC.

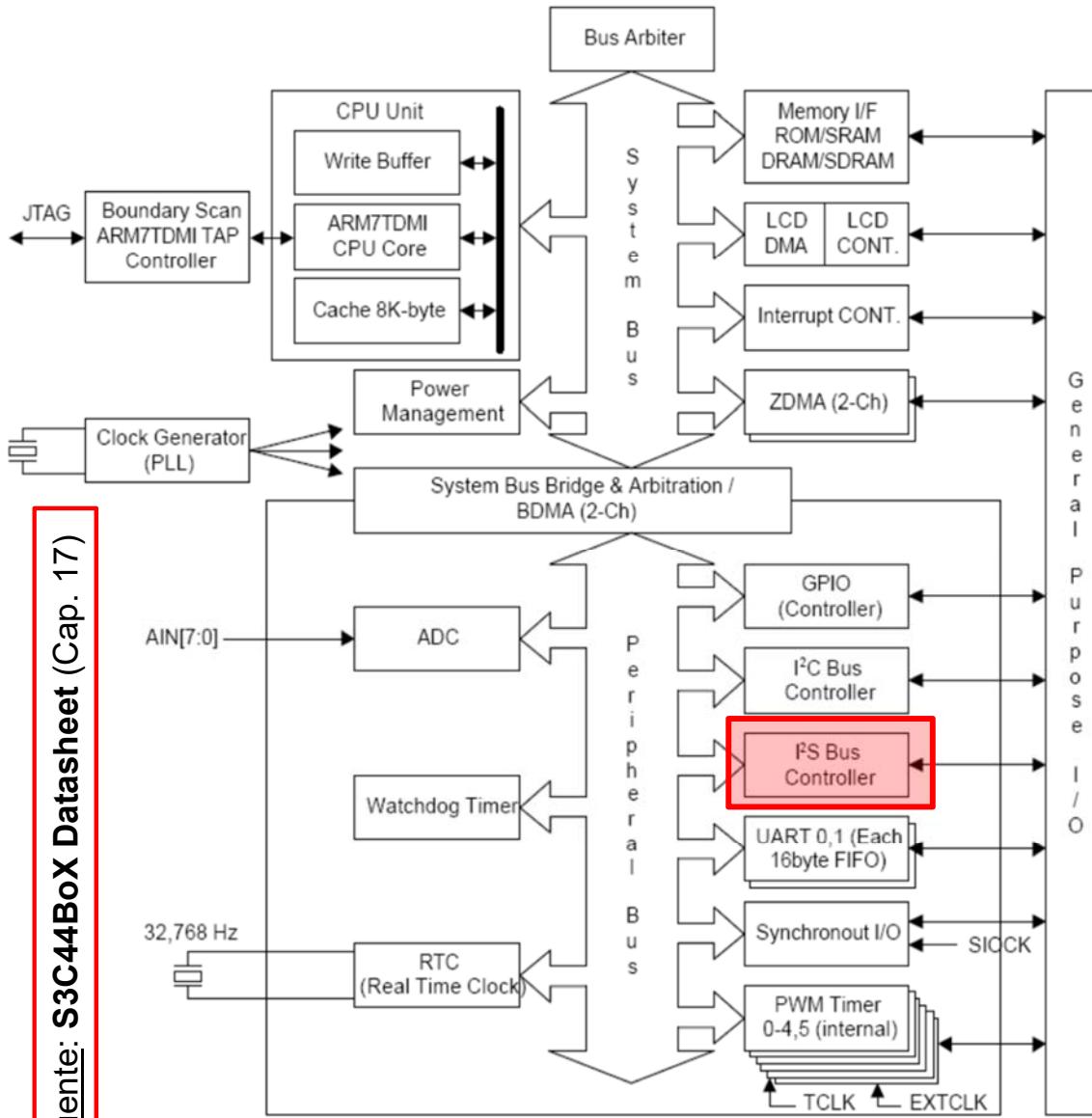
| IICADD | Bit | Description | Initial State |
|---------------|-------|--|---------------|
| Slave address | [7:0] | 7-bit slave address, latched from the IIC-bus: When serial output enable=0 in the IICSTAT, IICADD is write-enabled. The IICADD value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting. Slave address = [7:1] Not mapped = [0] | xxxx_xxxx |

- 0x01D6000C (IICDS – IIC-Bus Transmit/Receive Data Shift)
 - 8b, R/W, inicial = indefinido
 - Dato a transmitir/recibido por el bus IIC.

| IICDS | Bit | Description | Initial State |
|------------|-------|--|---------------|
| Data shift | [7:0] | 8-bit data shift register for IIC-bus Tx/Rx operation: When serial output enable = 1 in the IICSTAT, IICDS is write-enabled. The IICDS value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting | xxxx_xxxx |



Controlador de IIS



- Configurable mediante 5 registros mapeados en memoria (banco 0).

que permiten:

- Configurar el modo de funcionamiento del canal.
- Ordenar y controlar las transferencias serie.



Bus IIS

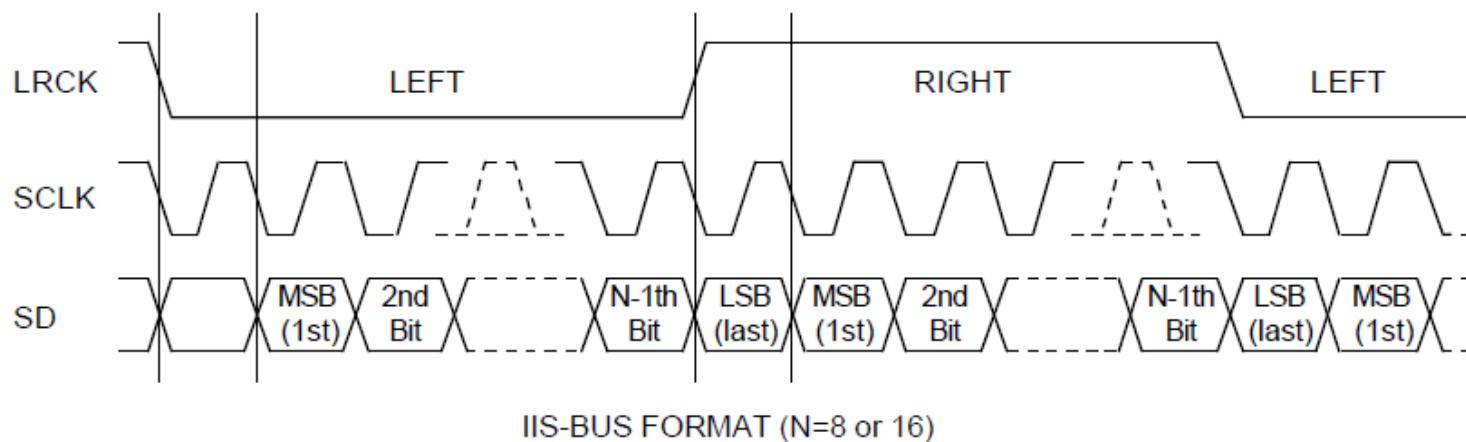
- IIS (Integrated Interchip Sound) es un **bus serie síncrono** para la transmisión de audio stéreo entre dispositivos digitales.
 - Tiene 2 líneas unidireccionales de datos serie: **IISDI** (entrada) y **IISDO** (salida).
 - Permite el envío/recepción simultánea de datos de sonido.
 - Otros datos (p.e. control) deben transmitirse por líneas aparte.
 - Tiene 3 líneas de reloj: **IISCLK** (transmisión de datos serie), **IISLRCLK** (selección de canal izquierdo/derecho), **CODECCLK** (reloj principal)
 - Todos los datos transmitidos están codificados en C2 (MSB first) con un número de bits no definido (depende del emisor/receptor).
 - Los datos serán truncados o extendidos con 0 según convenga en el emisor/receptor.
 - La transmisión de datos es continua
 - El maestro genera las señales de reloj
 - Emisor y receptor generan las señales de datos de audio alternando muestras del canal izquierdo y derecho.

Controlador de IIS

configuración: registro ICCCON



- El S3C44B0X dispone de un controlador de interfaz bus IIS que puede programarse para transmitir:
 - Usando un cierto formato de datos y una tasa de transferencia determinada (función de la frecuencia de muestreo del sonido).
 - Mediante encuesta (programado) o DMA.
 - Utilizando las 2 FIFOs internas de 16B que dispone (una de envío y otra de recepción).
- El controlador se encarga de gestionar la señalización/transferencia de datos individuales.



Controlador de IIS

configuración: registro IISCON



- 0x01D18000 (IISCON – IIS Control)
 - 9b, R/W, inicial = 0x100
 - Permite iniciar/parar la transmisión, habilitar el módulo de prescalado del reloj, conocer el estado de las FIFOs, el canal que está transmitiendo y habilitar las peticiones de DMA.

| IISCON | Bit | Description | Initial State |
|--------------------------------------|-----|---|---------------|
| Left/Right channel index (read only) | [8] | 0 = Left channel 1 = Right channel | 1 |
| Transmit FIFO ready flag (read only) | [7] | 0 = FIFO is not ready (empty) 1 = FIFO is ready (not empty) | 0 |
| Receive FIFO ready flag (read only) | [6] | 0 = FIFO is not ready (full) 1 = FIFO is ready (not full) | 0 |
| Transmit DMA service request enable | [5] | 0 = Request disable 1 = Request enable | 0 |
| Receive DMA service request enable | [4] | 0 = Request disable 1 = Request enable | 0 |
| Transmit channel idle command | [3] | In Idle state the IISLRCK is inactive(pause Tx). This bit is only effective if the IIS is a master. 0 = IISLRCK is generated. 1 = IISLRCK is not generated. | 0 |
| Receive channel idle command | [2] | In Idle state the IISLRCK is inactive(pause Rx). This bit is only effective if the IIS is a master. 0 = IISLRCK is generated. 1 = IISLRCK is not generated. | 0 |
| IIS prescaler enable | [1] | 0 = Prescaler disable 1 = Prescaler enable | 0 |
| IIS interface enable (start) | [0] | 0 = IIS disable (stop) 1 = IIS enable (start) | 0 |

Controlador de IIS

configuración: registro IISMOD



- 0x01D18004 (**IISMOD – IIS Mode**)
 - 9b, R/W, inicial = 0x000
 - Permite establecer el maestro de la comunicación, modo transmisión, el formato de transmisión, el número de bits por canal, la polaridad de la señal de selección de canal y la relación entre la frecuencia de muestreo y las frecuencias de CODECLK y IISCLK.

| IISMOD | Bit | Description | Initial State |
|--|-------|--|---------------|
| Master/slave mode select | [8] | 0 = Master mode (IISLRCK and IISCLK are output mode) 1 = Slave mode (IISLRCK and IISCLK are input mode) | 0 |
| Transmit/receive mode select | [7:6] | 00 = No transfer 01 = Receive mode 10 = Transmit mode 11 = Transmit and receive mode | 00 |
| Active level of left/right channel | [5] | 0 = Low for left channel (high for right channel) 1 = High for left channel (low for right channel) | 0 |
| Serial interface format | [4] | 0 = IIS compatible format 1 = MSB(Left)-justified format | 0 |
| Serial data bit per channel | [3] | 0 = 8-bit 1 = 16-bit | 0 |
| Master clock(CODECLK) frequency select | [2] | 0 = 256fs (fs : sampling frequency) 1 = 384fs | 0 |
| Serial bit clock frequency select | [1:0] | 00 = 16fs 10 = 48fs (fs : sampling frequency) 01 = 32fs 11 = N/A | 00 |

Controlador de IIS

configuración: registro IISPSR



- 0x01D18008 (IISPSR – IIS Prescaler)
 - 8b, R/W, inicial = 0x00
 - Fija la frecuencia del reloj principal a partir de la frecuencia del MCLK.

| IISPSR | Bit | Description | Initial State |
|-------------------|-------|---|---------------|
| Prescaler value A | [7:4] | prescaler division factor for the prescaler A $clock_{prescaler_A} = MCLK / <division\ factor>$ | 0x0 |
| Prescaler value B | [3:0] | prescaler division factor for the prescaler B $clock_{prescaler_B} = MCLK / <division\ factor>$ | 0x0 |

| IISPSR[3:0] / [7:4] | Division Factor | IISPSR[3:0] / [7:4] | Division Factor |
|---------------------|-----------------|---------------------|-----------------|
| 0000b | 2 | 1000b | 1 |
| 0001b | 4 | 1001b | – |
| 0010b | 6 | 1010b | 3* |
| 0011b | 8 | 1011b | – |
| 0100b | 10 | 1100b | 5* |
| 0101b | 12 | 1101b | – |
| 0110b | 14 | 1110b | 7* |
| 0111b | 16 | 1111b | – |

NOTES:

1. If the prescaler value is 3,5,7, the duty is not 50%. In this case, the H duration is 0.5 MCLK.



Controlador de IIS

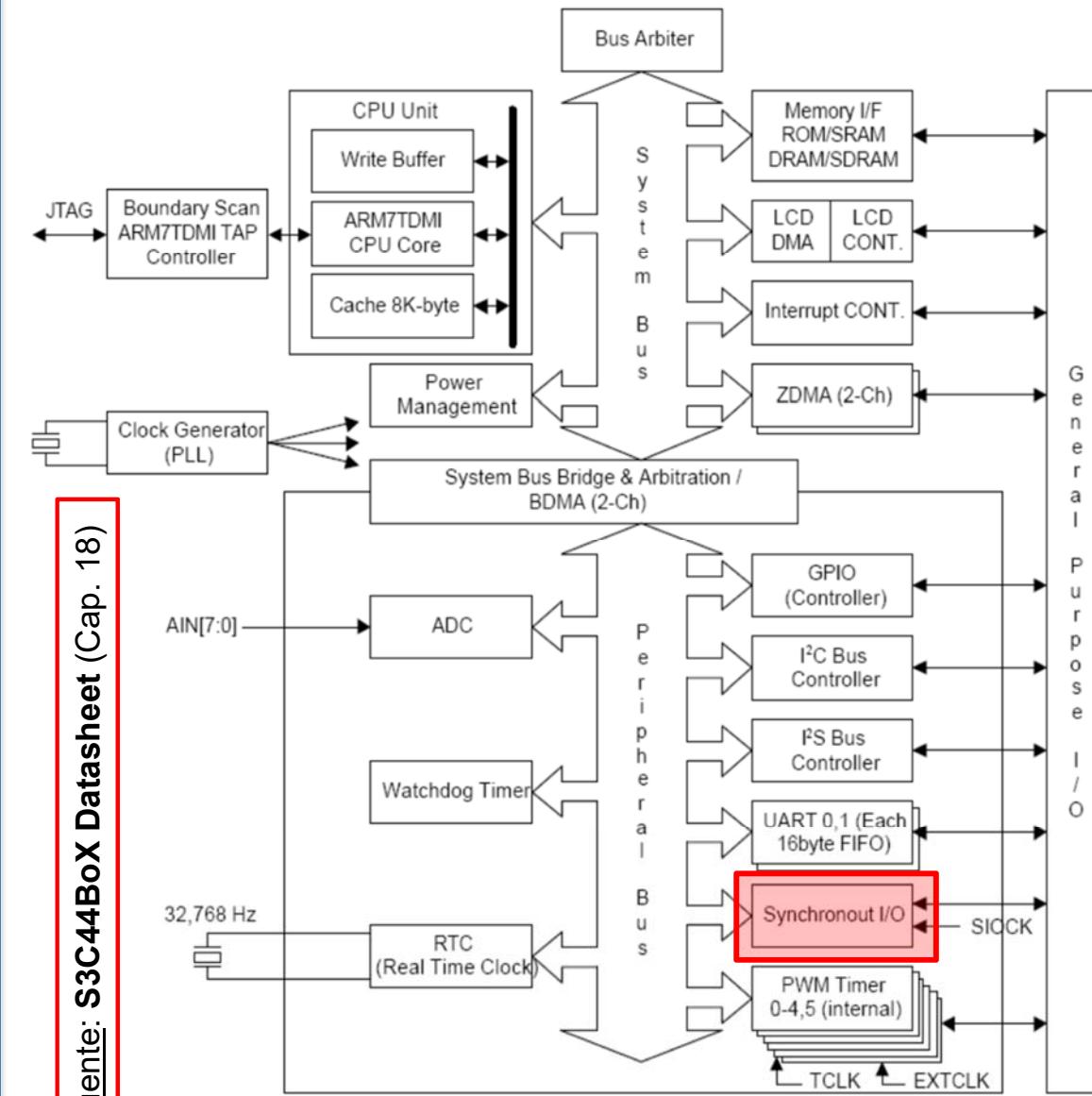
configuración: registro IISMOD

- 0x01D1800C (**IISFCON – ISS FIFO Control**)
 - 12b, R/W, inicial = 0x000
 - Permite habilitar/desabilitar la FIFO de transmisión/recepción, indicar el modo de acceso ella y conocer el número de datos que contiene.

| IISFCON | Bit | Description | Initial State |
|--------------------------------------|-------|---|---------------|
| Transmit FIFO access mode select | [11] | 0 = Normal access mode 1 = DMA access mode | 0 |
| Receive FIFO access mode select | [10] | 0 = Normal access mode 1 = DMA access mode | 0 |
| Transmit FIFO enable | [9] | 0 = FIFO disable 1 = FIFO enable | 0 |
| Receive FIFO enable | [8] | 0 = FIFO disable 1 = FIFO enable | 0 |
| Transmit FIFO data count (read only) | [7:4] | Data count value = 0-8 | 000 |
| Receive FIFO data count (read only) | [3:0] | Data count value = 0-8 | 000 |

- 0x01D18010 (**IISFIF – IIS FIFO**)
 - 16b, R/W, inicial = 0x0000
 - Dato a transmitir / recibido por el bus IIS.

| IISFIF | Bit | Description | Initial State |
|--------|--------|-------------------------------|---------------|
| FENTRY | [15:0] | Transmit/Receive data for IIS | 0 |



- Configurable mediante 5 registros mapeados en memoria (banco 0).

que permiten:

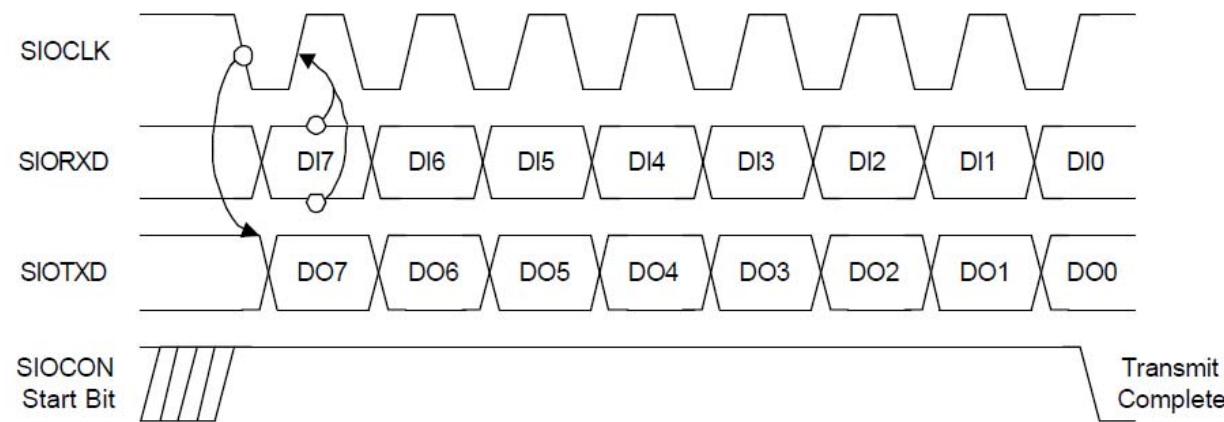
- Configurar el modo de funcionamiento de cada cada canal.
- Ordenar y controlar las transferencias serie:



Controlador de SIO



- El S3C44B0X dispone de un controlador de interfaz serie síncrono para la transmisión de datos de 8 bits a través de
 - 2 líneas unidireccionales de datos serie: **SIOTXD** (salida), **SIORXD** (entrada).
 - 1 línea de reloj **SCL**.
- El controlador puede programarse para transmitir
 - Usando un cierto formato de datos y una tasa de transferencia determinada.
 - Mediante encuesta (programado), interrupción o DMA.
- El controlador se encarga de gestionar la señalización/transferencia de datos individuales.





Controlador de SIO

configuración: registro SIOCON

- 0x01D11400 (SIOCON – SIO Control)
 - 8b, R/W, inicial = 0x00
 - Permite fijar la fuente de la frecuencia base de comunicación, el formato de datos, el método de E/S y habilitar la comunicación.

| SIOCON | Bit | Description | Initial State |
|---------------------|-------|---|---------------|
| Clock source select | [7] | SIO shift clock source select bit. 0 = Internal clock, 1 = External clock | 0 |
| Data direction | [6] | This bit controls whether MSB is transmitted first or LSB is transmitted first. 0 = MSB mode, 1 = LSB mode | 0 |
| Tx/Rx selection | [5] | This bit decides whether to enable the transmit operation enabled. If you want to only transmit, the received data in SIODAT will be ignored. If users want to transmit and receive, SIO supports data transmission and reception simultaneously. Users write the data transmitted in the SIODAT register and then SIO will transmit the data serially. At the same time, SIO will receive the data from an external SIO device. After the SIO transmission is completed, the contents of SIODAT, will have the received data. 0 = Receive only mode, 1 = Transmit/Receive mode | 0 |
| Clock edge select | [4] | This bit determines the clock to be used for serial transmit or receive operation. 0 = falling edge clock, 1 = rising edge clock | 0 |
| SIO start | [3] | This bit determines whether the SIO functions is running or has stopped. When BDMA Tx is used, this bit should be '0'. 0 = No action 1 = Clear 3-bit counter and start shift. This bit is cleared just after writing this bit as 1. | 0 |
| Shift operation | [2] | Determines SIO shift operation 0 = Non hand-shaking mode(Auto run mode) 1 = Reserved | 0 |
| SIO mode select | [1:0] | Determines how and by what SIODATA is read/written. 00 = no operations 01 = SIO interrupt mode 10 = BDMA0 mode 11 = BDMA1 mode | 00 |



Controlador de SIO

configuración y operación: registros SIODAT, SBRDR y IVTCNT

- 0x01D11404 (**SIODAT – SIO Data**)
 - 8b, R/W, inicial = 0x00
 - Dato a transmitir / recibido por el bus SIO.

| SIODAT | Bit | Description | Initial State |
|----------|-------|--|---------------|
| SIO DATA | [7:0] | This field contains the data to be transmitted or received over the SIO channel. | 0x00 |

- 0x01D11408 (**SBRDR – SIO Baud Rate Prescaler**)
 - 12b, R/W, inicial = 0x00
 - Fija la frecuencia de transmisión/recepción.

| SBRDR | Bit | Description | Initial State |
|-------|--------|---|---------------|
| SBRDR | [11:0] | This field contains the prescaler value for the baud rate | 0x00 |

Baud rate = $MCLK / 2 / (\text{Prescaler value} + 1)$

- 0x01D1140C (**IVTCNT – SIO Interval Counter**)
 - 8b, R/W, inicial = 0x00
 - Fija el intervalo de tiempo entre 2 envíos.

| IVTCNT | Bit | Description | Initial State |
|--------|-------|-------------------------------|---------------|
| IVTCNT | [7:0] | SIO interval counter register | 0x00 |

Intervals (between 8-bit data) = $MCLK / 4 / (IVTCNT + 1)$



Controlador de SIO

configuración: registro DCNTZ

- 0x01D11410 (DCNTZ – SIO DMA Count Zero)
 - 2b, R/W, inicial = 0x0
 - Habilita/deshabilita la transmisión por DMA.

| DCNTZ | Bit | Description | Initial State |
|--------|-----|--|---------------|
| DCNTZ1 | [1] | 0: Enables BDMA1 service request. When this bit is 0, the SIO can request the DMA service. 1: Disables BDMA1 service request | 0 |
| DCNTZ0 | [0] | 0: Enables BDMA0 service request When this bit is 0, the SIO can request the DMA service. 1: Disables BDMA0 service request | 0 |

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