Yuan-Peng (Patrick) Yu

Software Developer

patrick.yp.yu@gmail.com

% https://patrick-yp-yu.github.io/

5 979-676-8186

PROFESSIONAL SUMMARY

- Skilled in C++ and Python. Accomplished multiple projects in computer vision and data science field.
- Experience in simultaneous localization and mapping (SLAM) methods using cameras and LIDARs.
- Proficient in the back-end of Integrated Circuits (IC) design flow for mixed-signal circuits.

EDUCATION

Research Assistant

NetBot Laboratory, Texas A&M University

♀ College Station, TX June 2016 - Present

- Conducted research on visual simultaneous localization and mapping (SLAM) to advance the development of robots and autonomous vehicles. Achieved tasks include camera calibration, features detection, and camera pose estimation. Allow indoor robots to localize and build maps.
- Implemented the automatic map initialization in the current state-of-the-art algorithm, ORB-SLAM. Computed the mathematics model and acquired the camera pose from any scene pairs. Investigated the limitations of ORB-SLAM and proposed methods to improve indoor SLAM performances.
- Created an image stitching program to present a panoramic image. Detected and matched image keypoints by the SIFT algorithm. Automatically estimated homography matrix through the RANSAC method. Generated a 180° view landscape image by combining multiple images.

Bachelor of Science in Computer Engineering

♀ College Station, TX

Texas A&M University, College Station

Overall GPA: 3.75/4.0

Major GPA: 3.82/4.0

- Graduation honor as an Undergraduate Research Scholar
- Analyzed the top 4000 Kickstarter projects to acquire investment insights. Applied web scraping skills to collect data. Built database by Python Pandas and NumPy. Utilize Scikits-learn to cluster data trend and classify labels. Concluded 8 business analyses through data visualization.

Associate of Science in Electronic Engineering **National Taipei University of Technology**

♀ Taipei, Taiwan

September 1994 - June 1999

- Overall GPA: 3.6/4.0 (top 10%)
- Earned the Distinguished Student Award in 1998 & 1999, respectively. Awarded students are excellent in ethical, intellectual, physical education, and social skills.
- Built an application to diagnose the possible locations of brain cancer in MRI. Developed 3 detection algorithms in C++. Reconstructed a 3D model from 2D MRI to show the relative positions.

EXPERIENCE

Senior IC CAD/Physical Design Engineer Jian Yu Co., Ltd

♀ Taipei, Taiwan M October 2009 - August 2014

• Led project-based teams to shorten physical design flow. Created at least 50 kinds of Cadence SKILLs, Parameterized Cells, and Dracula Command files to reduce processing time. Completed more than 40 tape-out and the projects were done ahead of schedule.

IC CAD/Layout Engineer

♥ Hsinchu, Taiwan

June 2004 - September 2009

Leadtrend Technology Corporation

 Implemented AC/DC controller ICs in different processes, ranging from Bipolar/CMOS/DMOS high-voltage processes to mixed-signal processes. Jobs include IC full chip floorplanning, place and route, and physical verifications. Completed at least 30 projects. The works became star products of the company and contributed to the successful initial public offering of the start-up company.

Management Information System Engineer **Air Grand Corporation**

▼ Taipei, Taiwan

₩ July 2001 - May 2004

 Provided technological services to 50 users. Constructed the company website and network infrastructures. Completed the project within 70% of its budget and achieved a 90% satisfaction.

SKILLS

Programming:

C C++ Python

Matlab GDB debugger

git) (github) (LTFX)

CMake HTML CSS

Bootstrap

Computer Vision:

Multiple View Geometry

SLAM Visual SLAM

ORB-SLAM ROS

OpenCV Unity

Images Stitching

Features Detection

SIFT Pose Estimation

3D Reconstruction

Camera Calibration

Perspective Rectification

Data Mining:

SQL XML Pandas

Web Scraping

Beautiful Soup

Machine Learning:

NumPy SciPy

Scikits-learn NetworkX

Data Visualization:

Matplotlib Seaborn

Plotly Pygal

ASIC Design Flow:

(HSPICE) (Mentor Calibre)

Cadence SOC Encounter

Virtuoso Verilog

Floorplan Place & Route

Layout Versus Schematics

Design Rules Checking

Layout Parasitic Extraction

Certificates:

Digital IC Design

Analog IC Design

System-on-Chip Design

Semiconductor Physics

Semiconductor Devices