

## CENG4120 Hw3

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### Standard Cell Library

1)

a) 2 input pins, Pin(A) and Pin(B)

b) 1 output pins, Pin(Y)

c) function : “(!A B)”;

d) cell\_leakage\_power : 3.29145

2)

a) 0.76 by 2.47

b) 3.61 by 2.47

c) Layer metal 1: Horizontal

Layer metal 2: Vertical

### Synthesis Using Synopsys Design Compiler

1) -0.12

2) 0.21 or 0.22 if 0 is consider negative as shown in below image

```
phyung0@linux5.cse.cuhk.edu.hk
Terminal Sessions View X server Tools Games Settings Macros Help
Quick connect...
[data0/y20/phyung0/22hw3/
  Name
  synopsys
  FreePDK45
  setup.sh
  HA.mv
  HA-verilog.syn
  HA-verilog.pvt
  FA.mv
  FA-verilog.syn
  FA-verilog.pvt
  default.sdf
  dc.tcl
  command.log
  clat_synth.mv
  clat_synth.sdc
  CLAT.mv
  clat-verilog.syn
  clat-verilog.pvt
  Follow terminal folder

  -delay max
  -max_paths 1
Design : clat4
Version: 6-2012.06-SP5
Date : Sun Apr 3 18:09:58 2022
*****
Operating Conditions: typical Library: gsc145nm
Wire Load Model Mode: top

Startpoint: adder0/ha_ab_c/cout_reg
(rising edge-triggered flip-flop clocked by clock)
Endpoint: adder0/cout_reg
(rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: max

Point                                Incr                                Path
-----
clock clock (rise edge)              0.00                                0.00
clock network delay (ideal)          0.00                                0.00
adder0/ha_ab_c/cout_reg/CLK (DFFPOSX1) 0.00                                0.00 r
adder0/ha_ab_c/cout_reg/Q (DFFPOSX1)  0.10                                0.10 f
adder0/ha_ab_c/cout (HA_7)            0.00                                0.10 f
adder0/U3/Y (OR2X1)                   0.05                                0.15 f
adder0/cout_reg/D (DFFPOSX1)          0.00                                0.15 f
data arrival time                     0.15
-----
clock clock (rise edge)              0.21                                0.21
clock network delay (ideal)          0.00                                0.21
adder0/cout_reg/CLK (DFFPOSX1)        0.00                                0.21 r
library setup time                    -0.06                                0.15
data required time                    0.15
-----
data required time                    0.15
data arrival time                     -0.15
-----
slack (MET)                          0.00

1
exit
Thank you...
linux5:~/22hw3>
```

- 3) 4.76190476 Ghz
- 4) See attach file, run file at folder 22hw3.

### Place and Route Using Cadence Innovus

- 1) Total Area:256.707  
Total Power:2.77946173  
Slack: -0.004
- 2) 268.9089 square micron = aspect ratios: 10 row densities: 1.0
- 3) Check Attached files
- 4)

