CENG4120 Hw3

1155141320

Yung Pak Hong Patrick

Standard Cell Library

1)

a) 2 input pins, Pin(A) and Pin(B)

b) 1 output pins, Pin(Y)

c) function : “(!(A B))”;

d)cell_leakage_power : 3.29145

2)

a) 0.76 by 2.47

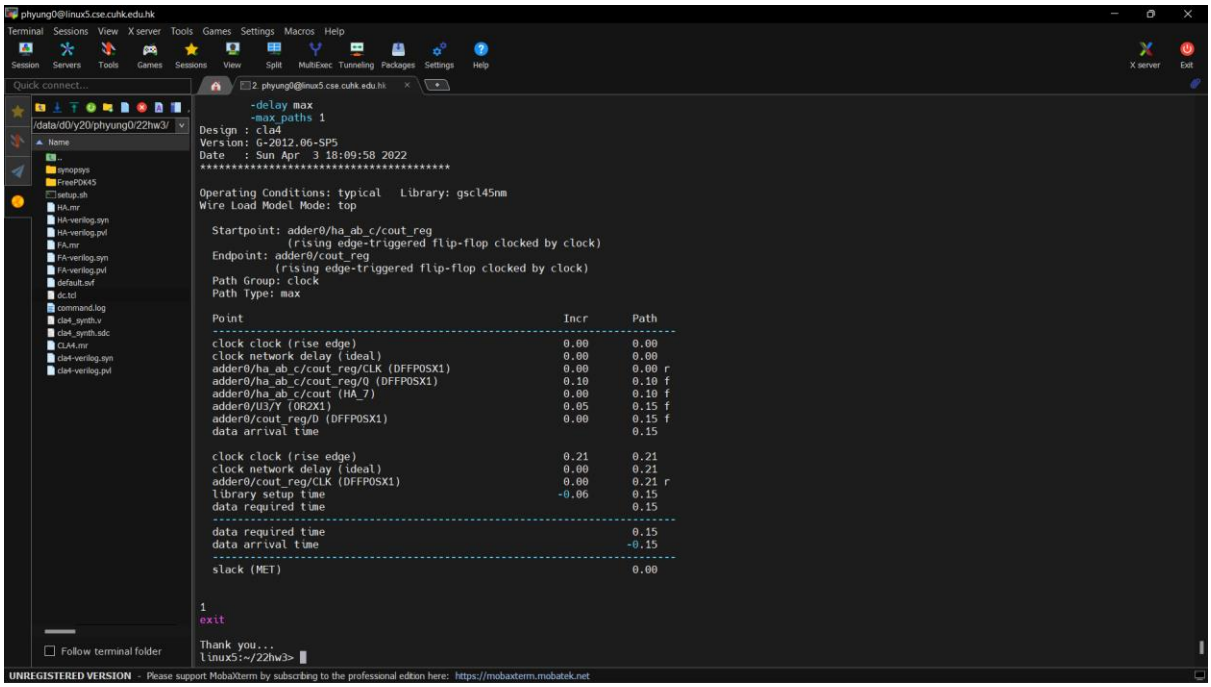
b)3.61 by 2.47

c) Layer metal 1: Horizontal

Layer metal 2: Vertical

Synthesis Using Synopsys Design Compiler

1) -0.12
2) 0.21 or 0.22 if 0 is consider negative as shown in below image



3) 4.76190476 Ghz
4) See attach file, run file at folder 22hw3.

Place and Route Using Cadence Innovus

1) Total Area:256.707
   Total Power:2.77946173
   Slack: -0.004
2) 268.9089 square micron = aspect ratios: 10 row densities: 1.0
3) Check Attached files
4)