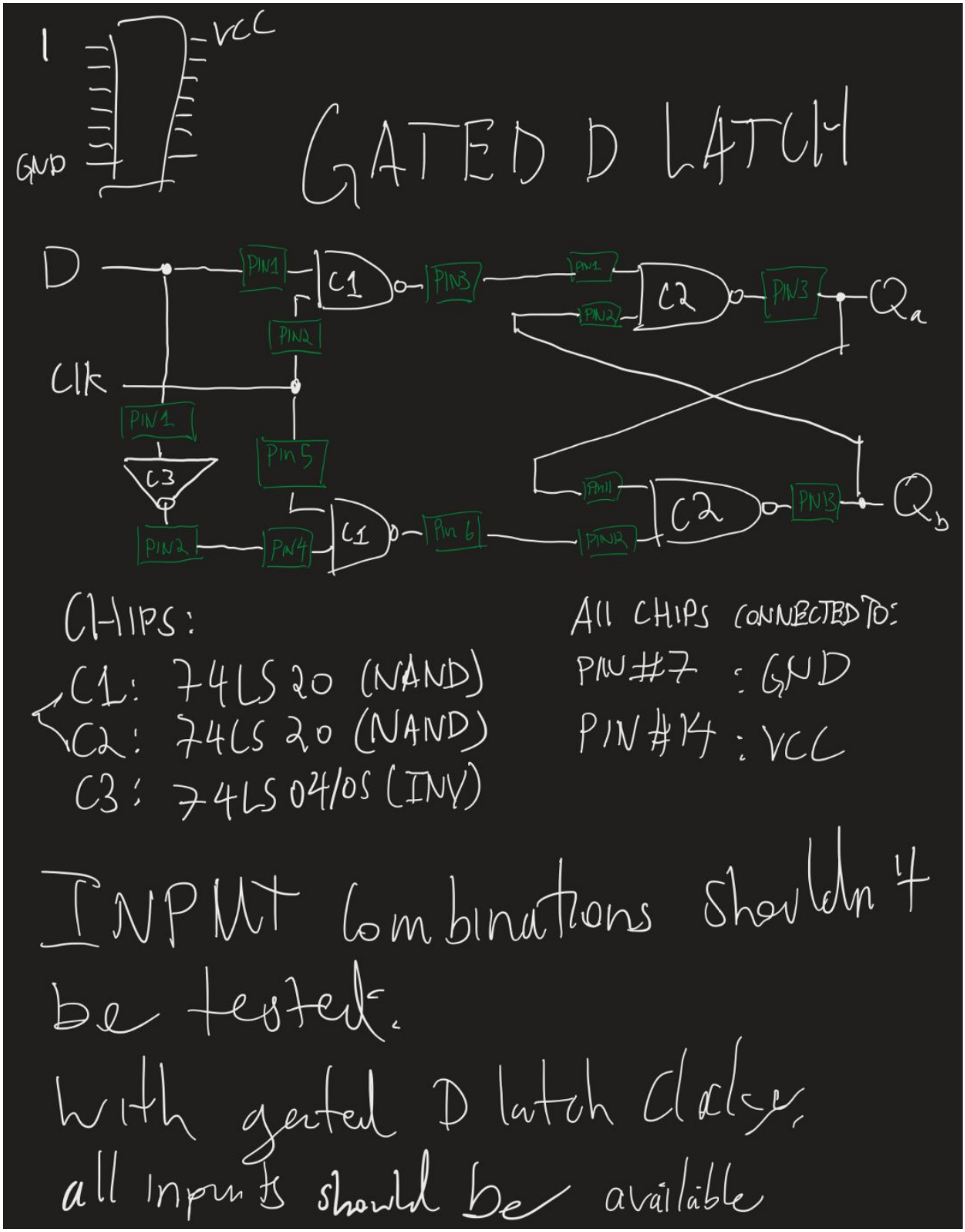
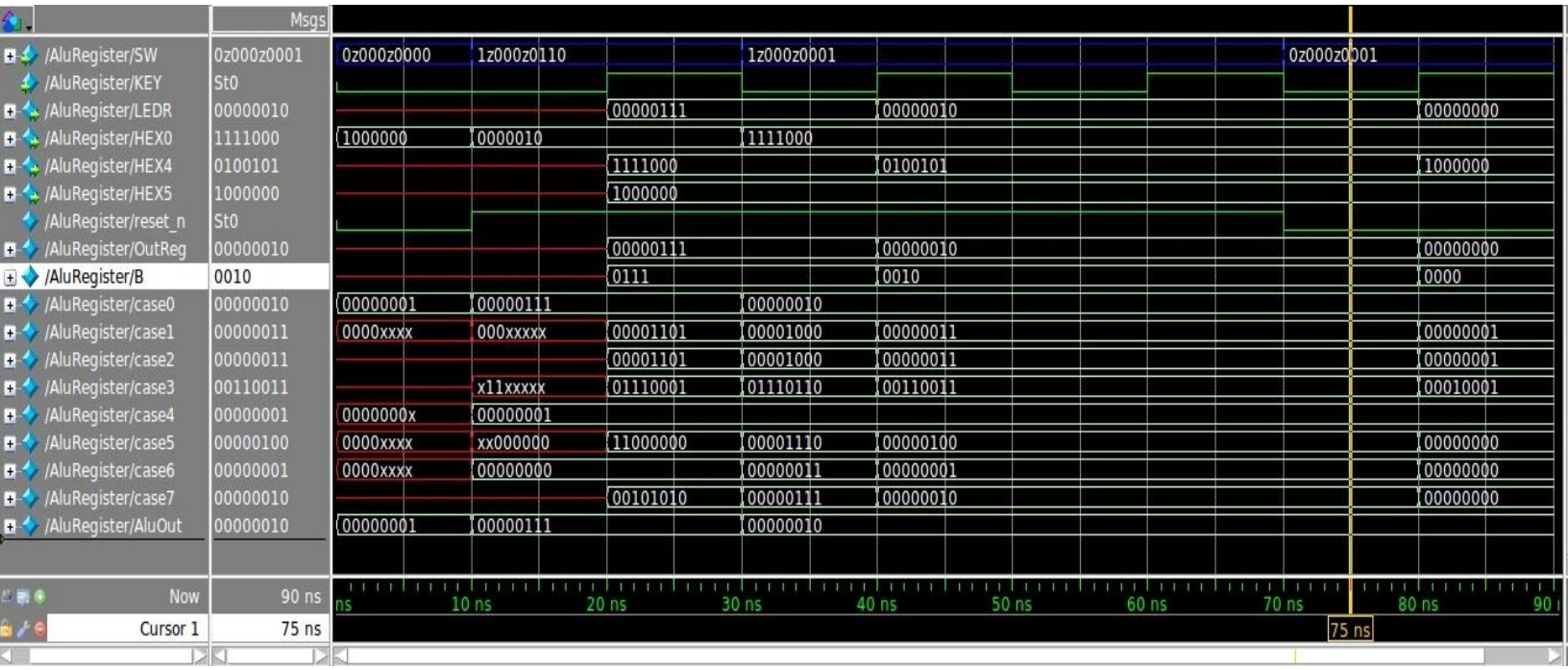
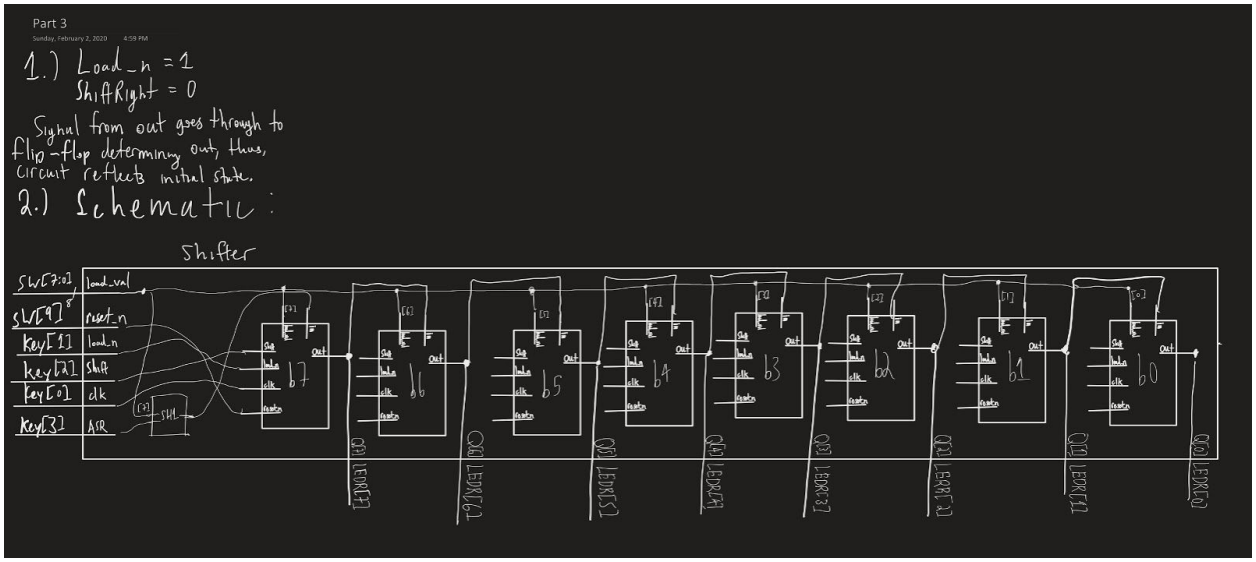
Part1:

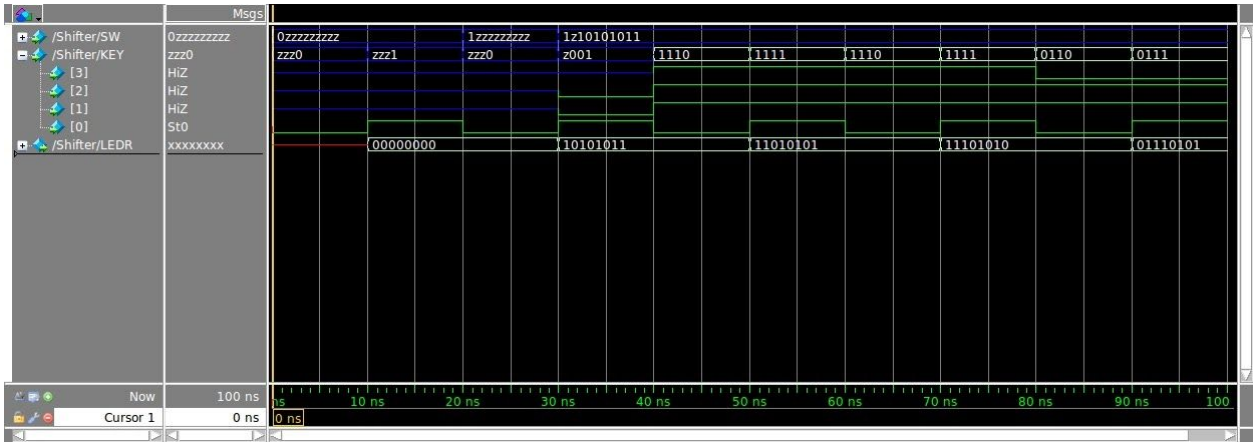

VCC
GND
GATED D LATCH
D
Clk
PIN1
PIN2
PIN3
PIN4
PIN5
PIN6
PIN11
PIN12
PIN13
C1
C2
C3
Q_a
Q_b
CHIPS:
C1: 74LS20 (NAND)
C2: 74LS20 (NAND)
C3: 74LS04/05 (INV)
ALL CHIPS CONNECTED TO:
PIN #7 : GND
PIN #14 : VCC
INPUT combinations shouldn't be tested.
with gated D latch clock.
all inputs should be available

Part 2: waveform for AluRegister.



Part3:





Pretty visibly shifts