

Quantum Hardware

- Part 2 and 3 -

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Outline

Part 1: Superconducting qubits

- Physics of the superconducting qubits
- Qubit control
- Quantum non-demolition measurement
- Qubit demonstration: qubit spectroscopy
- Two-qubit gate

Part 2: Device map and calibration data

- Hands-on: extracting the device information

Part 3: Qubit scaling

- Modularity
- Microwave component development

Summary

Device map and calibration data

<https://quantum.ibm.com/services/resources>

ibm_kawasaki

OpenQASM 3

Details

127

Qubits

2.4%

EPLG

5K

CLOPS

Status:

Online

Median ECR error:

7.653e-3

System region:

us-east

Median SX error:

2.340e-4

Total pending jobs:

210 jobs

Median readout error:

1.080e-2

Processor type ⓘ:

Eagle r3

Median T1:

183.48 us

Version:

2.1.28

Median T2:

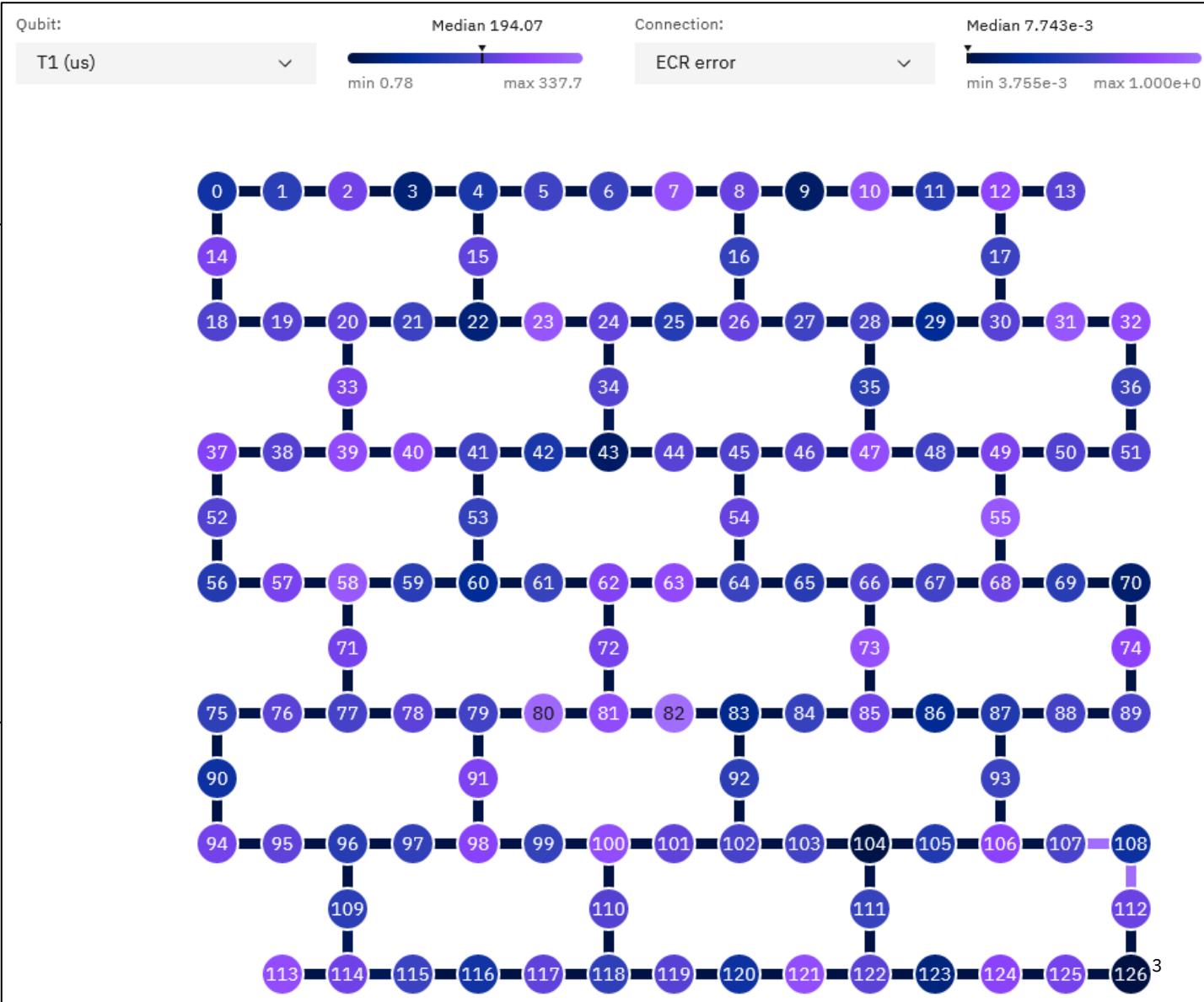
138.56 us

Basis gates:

ECR, ID, RZ, SX, X

Your instance usage:

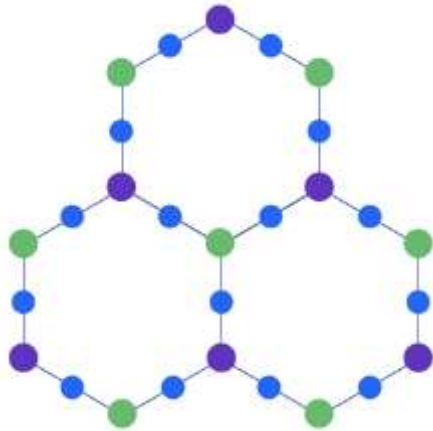
0 jobs



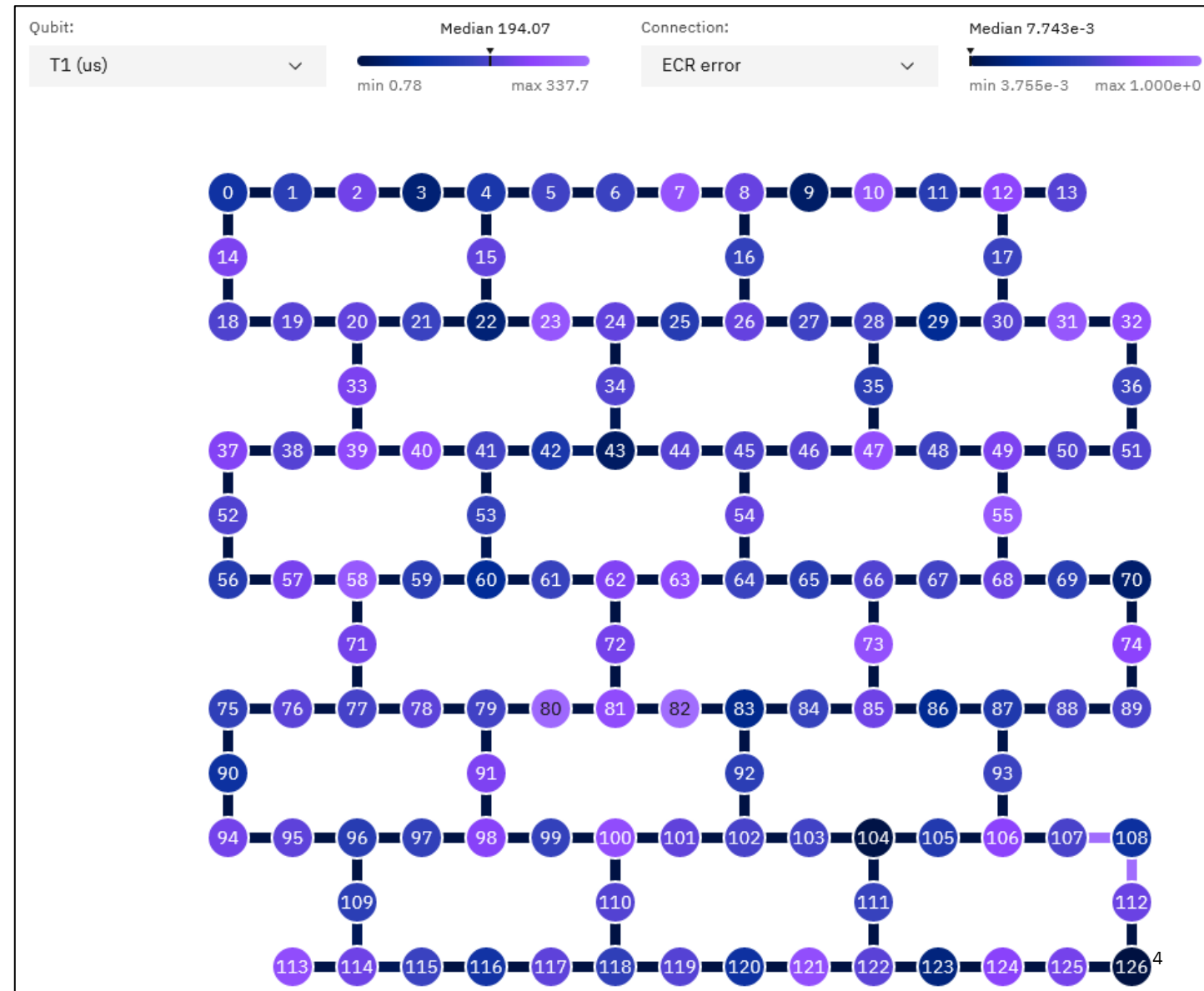
Device map – heavy-hex lattice

Heavy hexagonal code

- For quantum error correction
- Low connectivity (up to 3 neighbor qubits) to avoid frequency collision
- Modest fault tolerant threshold



<https://www.ibm.com/quantum/blog/heavy-hex-lattice>



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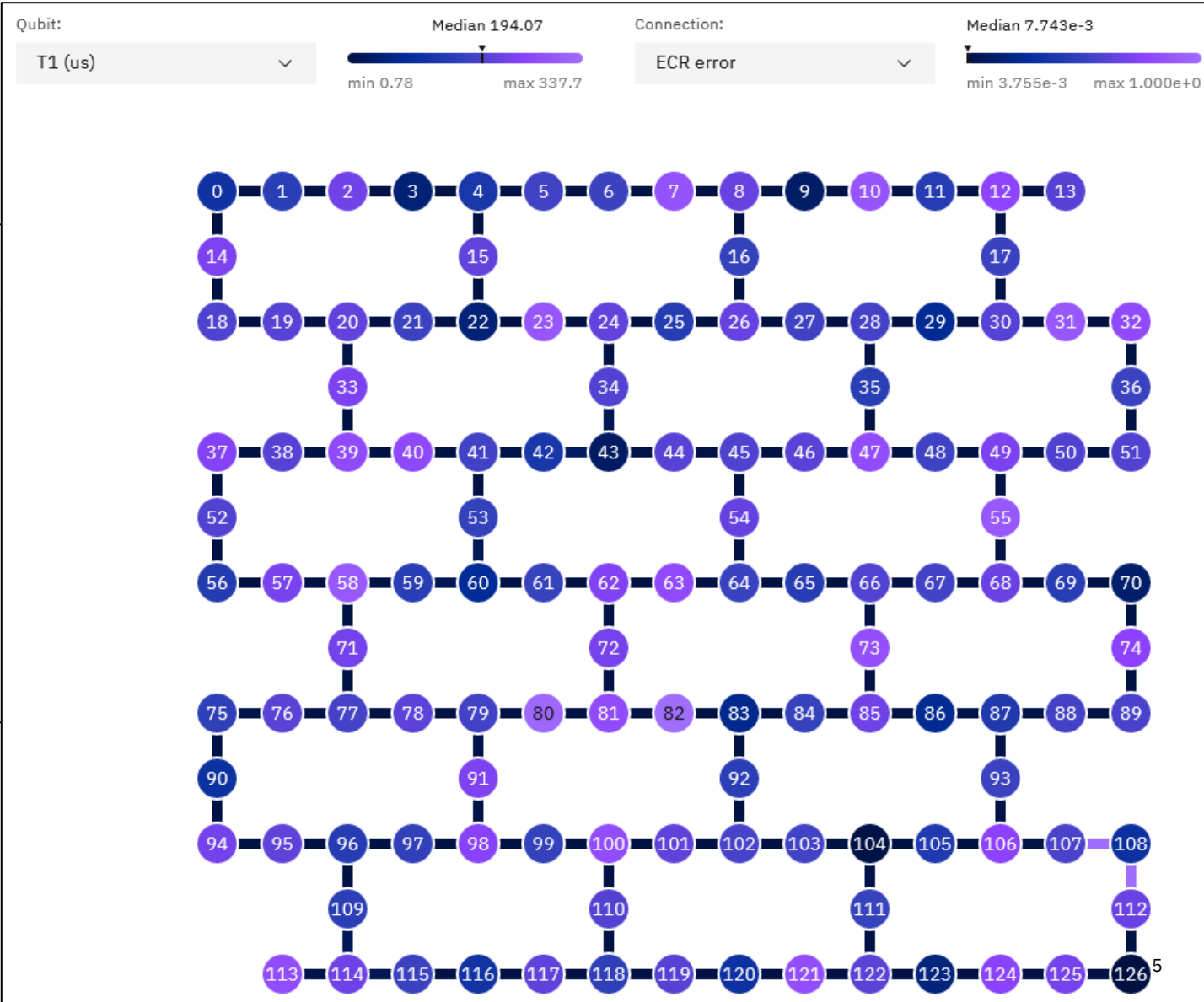
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5

Basis gates

- ECR: Echoed Cross Resonance, $ECR = XI_{\pi} \cdot ZX_{\pi/2} = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 & 0 & 1 & i \\ 0 & 0 & i & 1 \\ 1 & -i & 0 & 0 \\ -i & 1 & 0 & 0 \end{pmatrix}$
- ID: Identity, $I = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$
- RZ: single-qubit rotation about Z-axis, $RZ(\theta) = \begin{pmatrix} e^{-i\frac{\theta}{2}} & 0 \\ 0 & e^{i\frac{\theta}{2}} \end{pmatrix}$
Implemented virtually in hardware via frame changes.
- X: single-qubit pauli X gate, bit-flip, $X_{\pi} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$
- SX: sqrt X gate, $\sqrt{X}, X_{\pi/2} = \frac{1}{2} \begin{pmatrix} 1+i & 1-i \\ 1-i & 1+i \end{pmatrix}$

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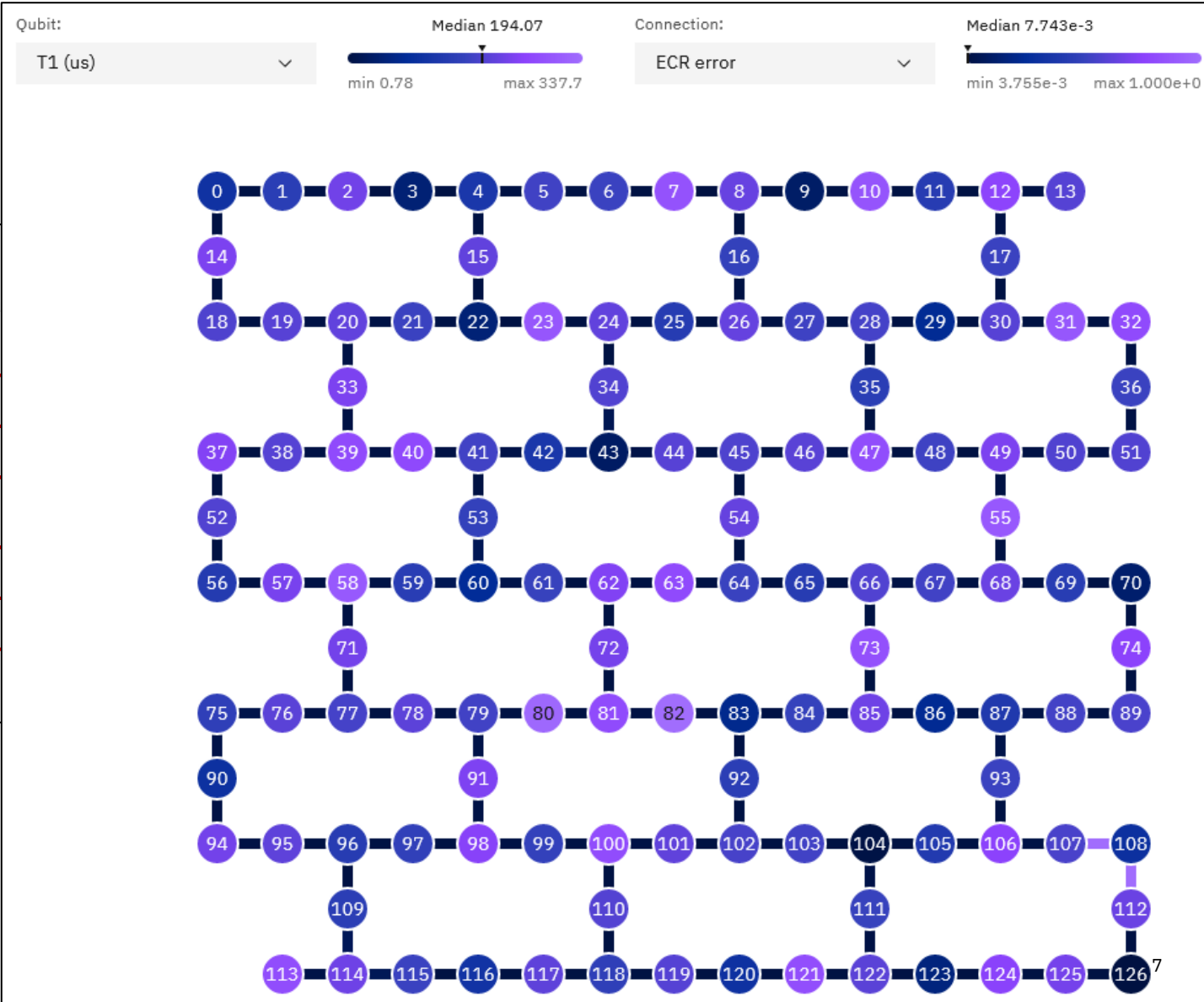
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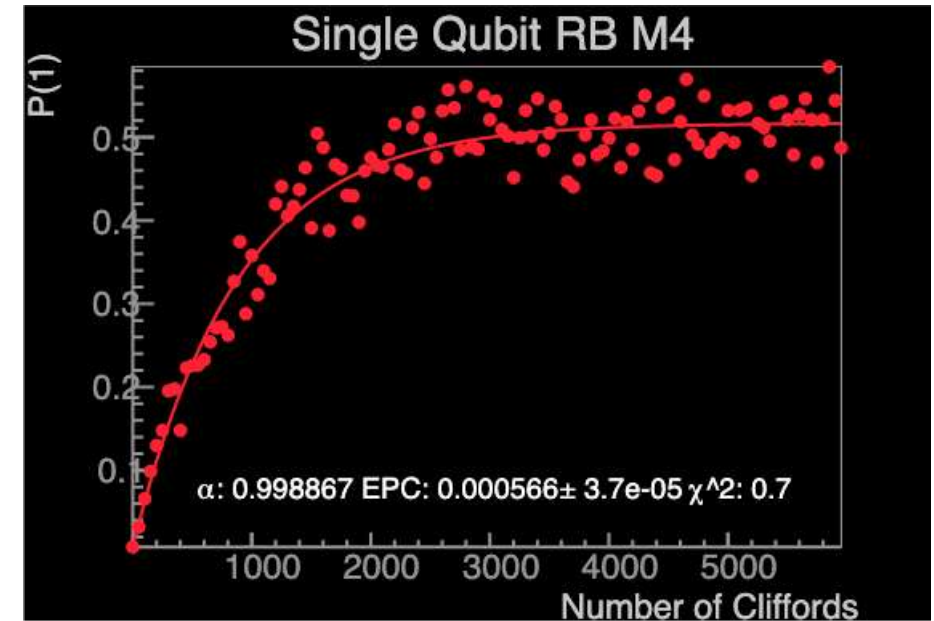
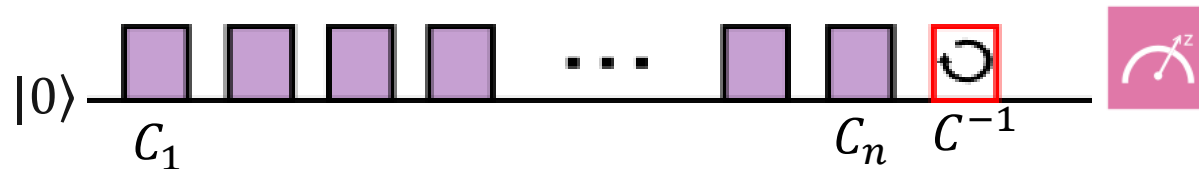
Gate error – Randomized benchmarking

Randomized Benchmarking

- Technique for characterizing gate errors
- Perform a random series of Clifford gates and undo
- Single qubit RB \rightarrow 1Q gate error, SX error
- Two qubit RB \rightarrow ECR error

Pulse sequence: N random Cliffords - inverse Clifford – measure

- C_i is a random gate sampled from a finite Clifford gate set
- C^{-1} is performed to make the total sequence equal to identity
- Measure the probabilities to get back to the ground state at the end of the sequence
- Vary sequence length, fit the fidelity decay to an exponential curve to report Error Per Clifford

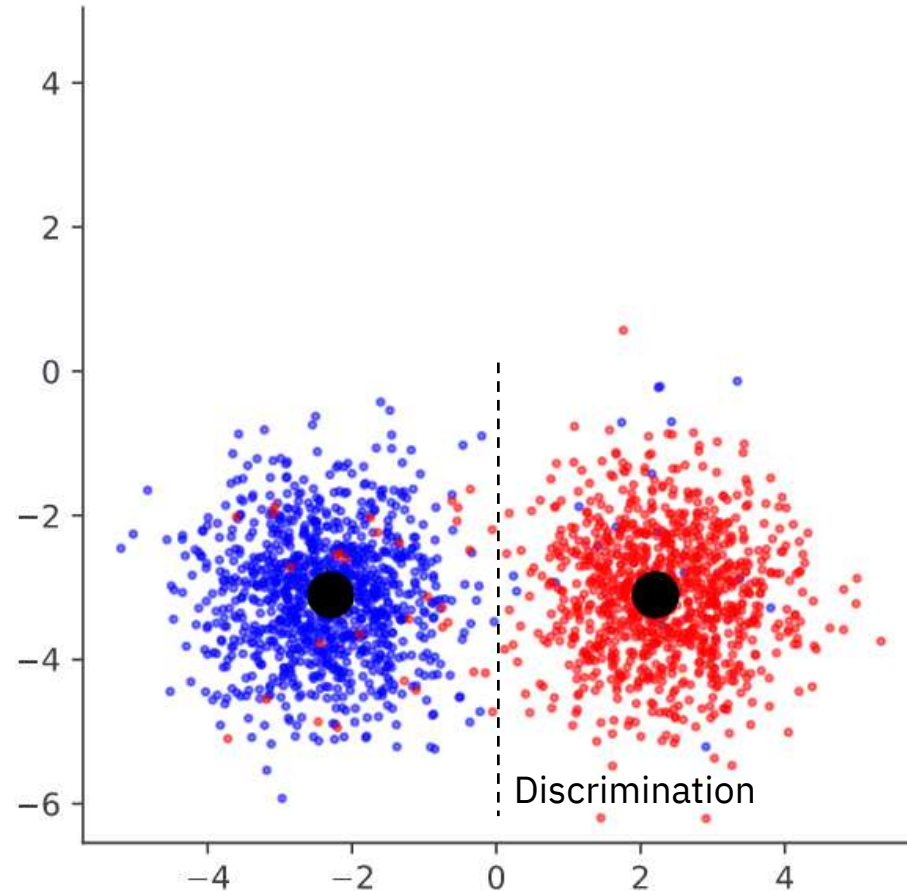


Readout error

Pulse sequence

- I - measure (blue)
- X_π - measure (red)
- Plot on IQ plane and discriminate 0/1

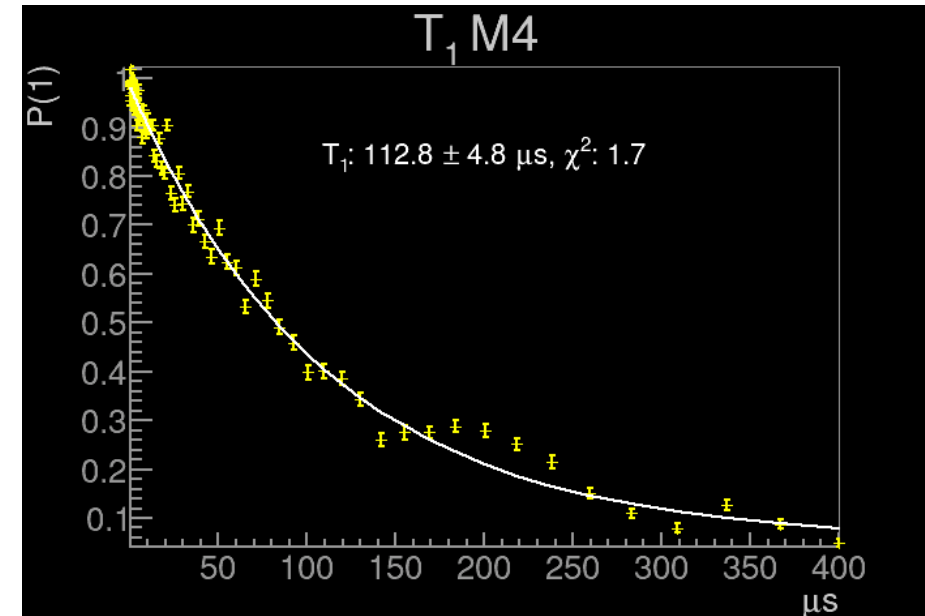
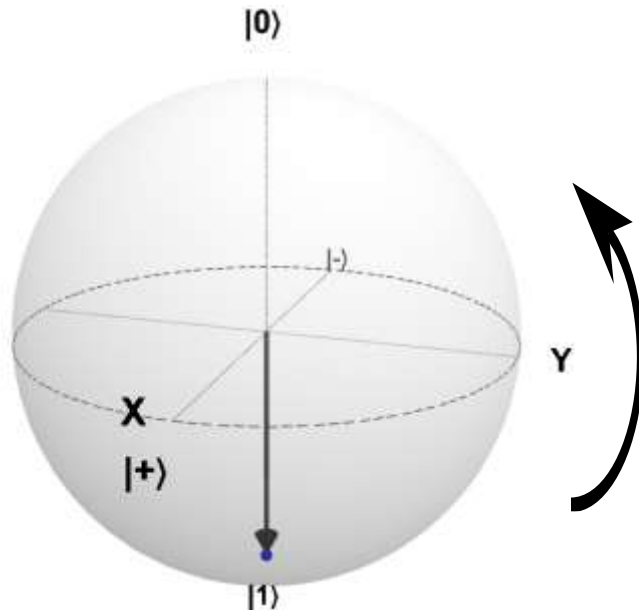
It is difficult to separate readout error and state preparation error



Relaxation time (T_1): amplitude damping

Energy decay from the excited state $|1\rangle$ to the ground state $|0\rangle$

- Spontaneous emission due to electromagnetic environment
 - Coupling to two-level systems (TLSs) or any other channel
 - Superconductor phenomena: quasiparticles and vortices
-
- Energy relaxation is characterized by the timescale T_1
 - The probability of a relaxation error is given by $1 - e^{-t/T_1}$
 - Pulse sequence : X_π - (vary delay) - measure



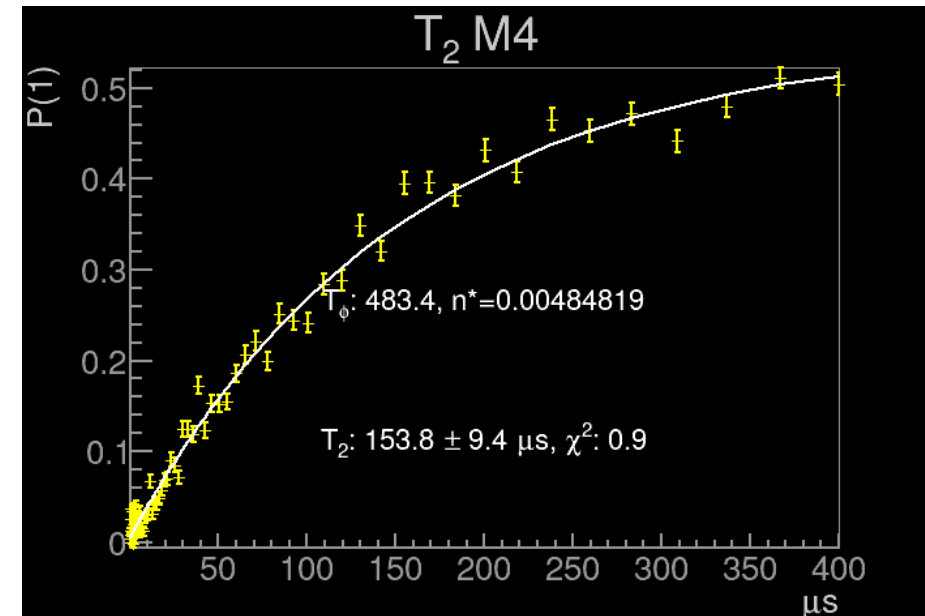
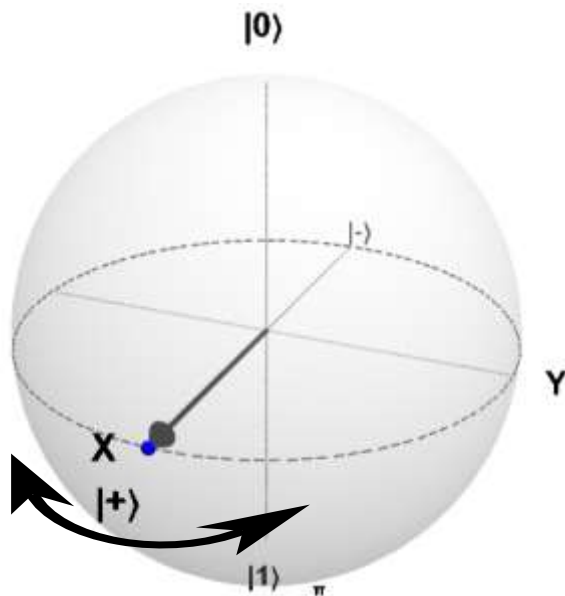
Decoherence time (T_2): phase damping

Fluctuations in energy levels due to thermal broadening or magnetic noise

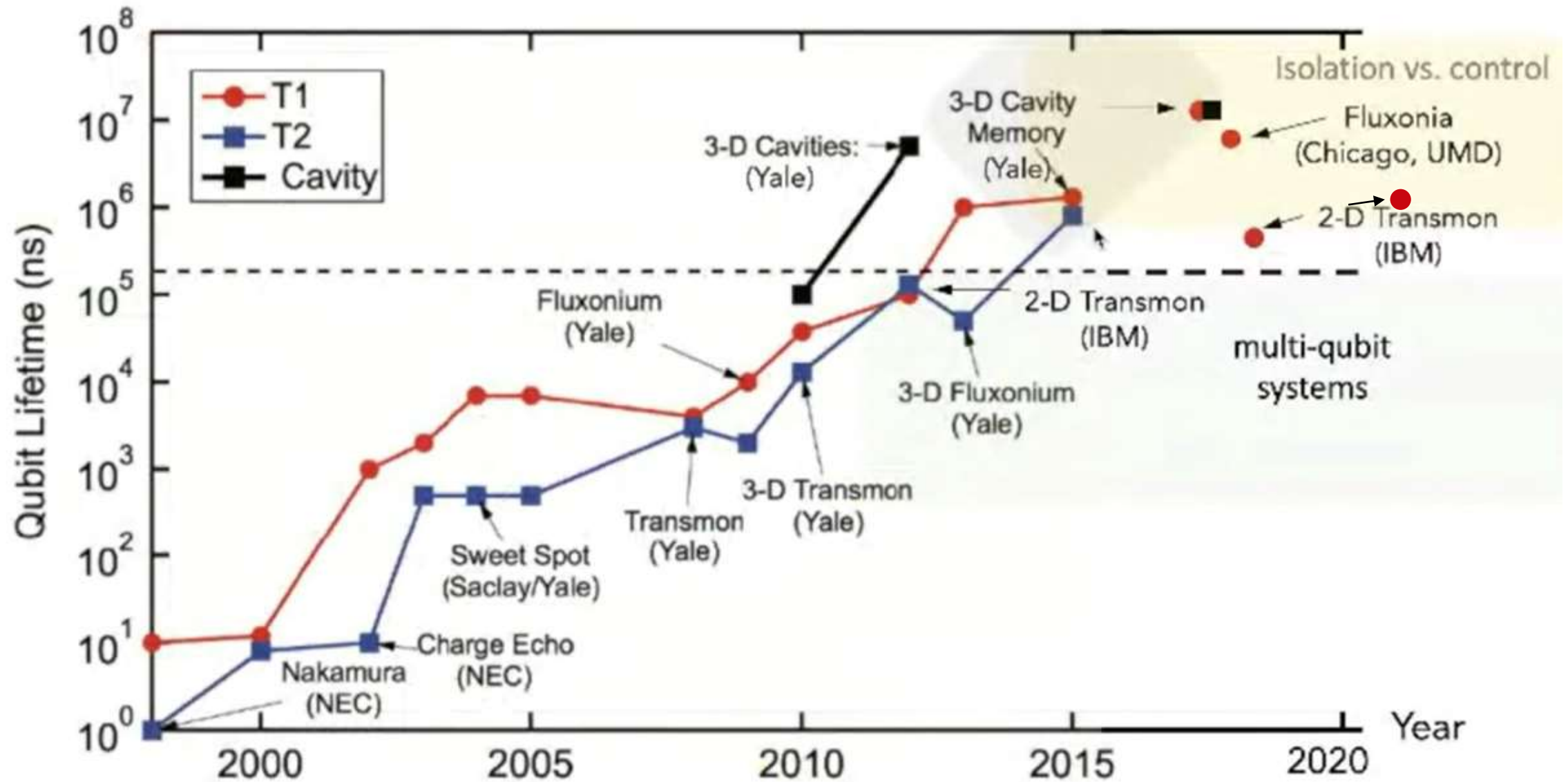
- Superposition states become classical, and a coherent state lose its phase information
- Ultimately limited by qubit relaxation (T_1), even with dephasing (T_ϕ) improvements

$$\frac{1}{T_2} = \frac{1}{2T_1} + \frac{1}{T_\phi}$$

- Decoherence is characterized by the timescale T_2
- The probability of a relaxation error is given by $1 - e^{-t/T_2}$
- Pulse sequence : $X_{\pi/2}$ - (vary delay) - X_π - (vary delay) - $X_{\pi/2}$ - measure



Coherence in superconducting circuits



Hands-on

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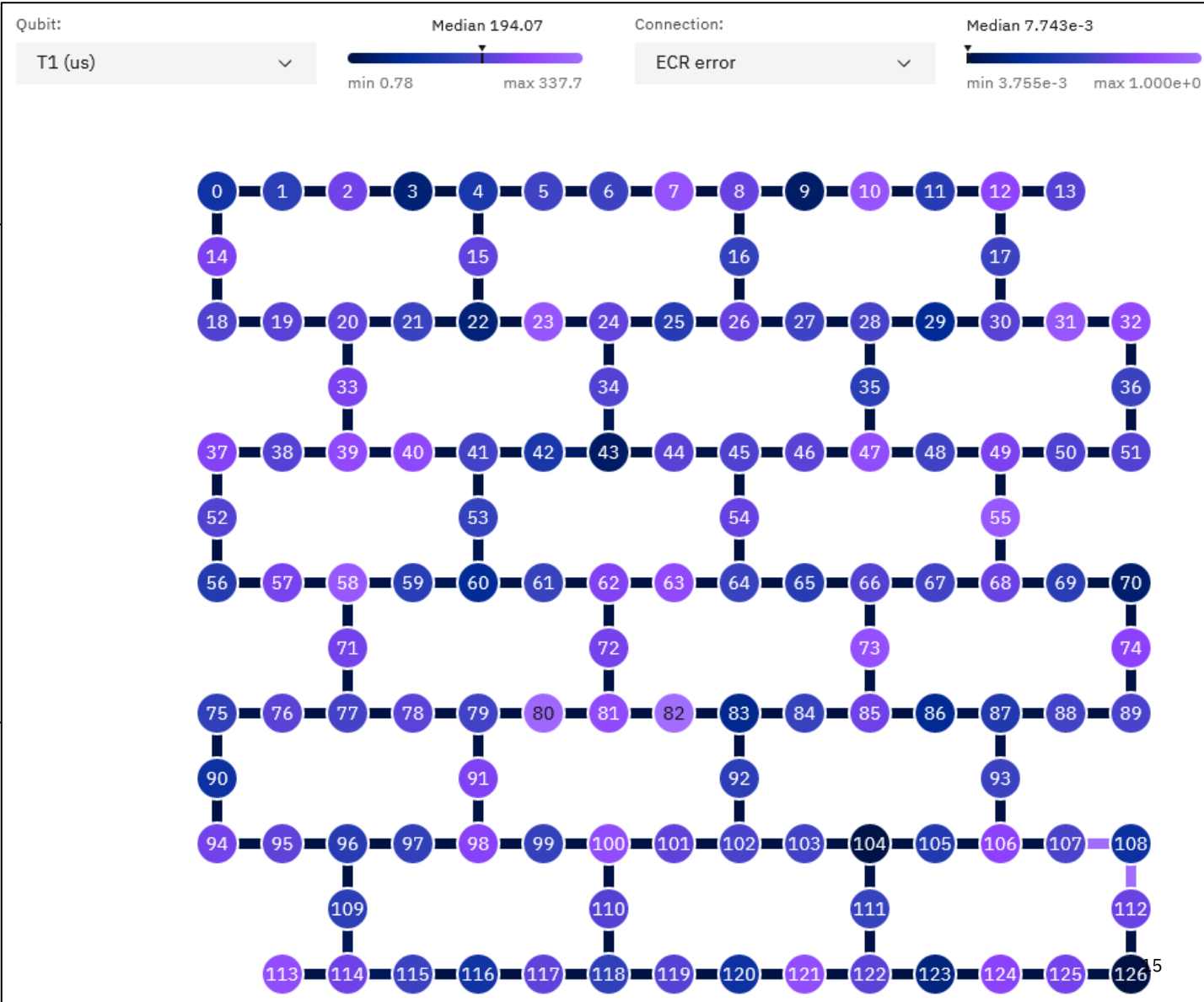
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5

2016

2017

2018

→ 2019



2016

2017

2018

2019

→ 2020



2016

2017

2018

2019

2020

→ 2021



2016

2017

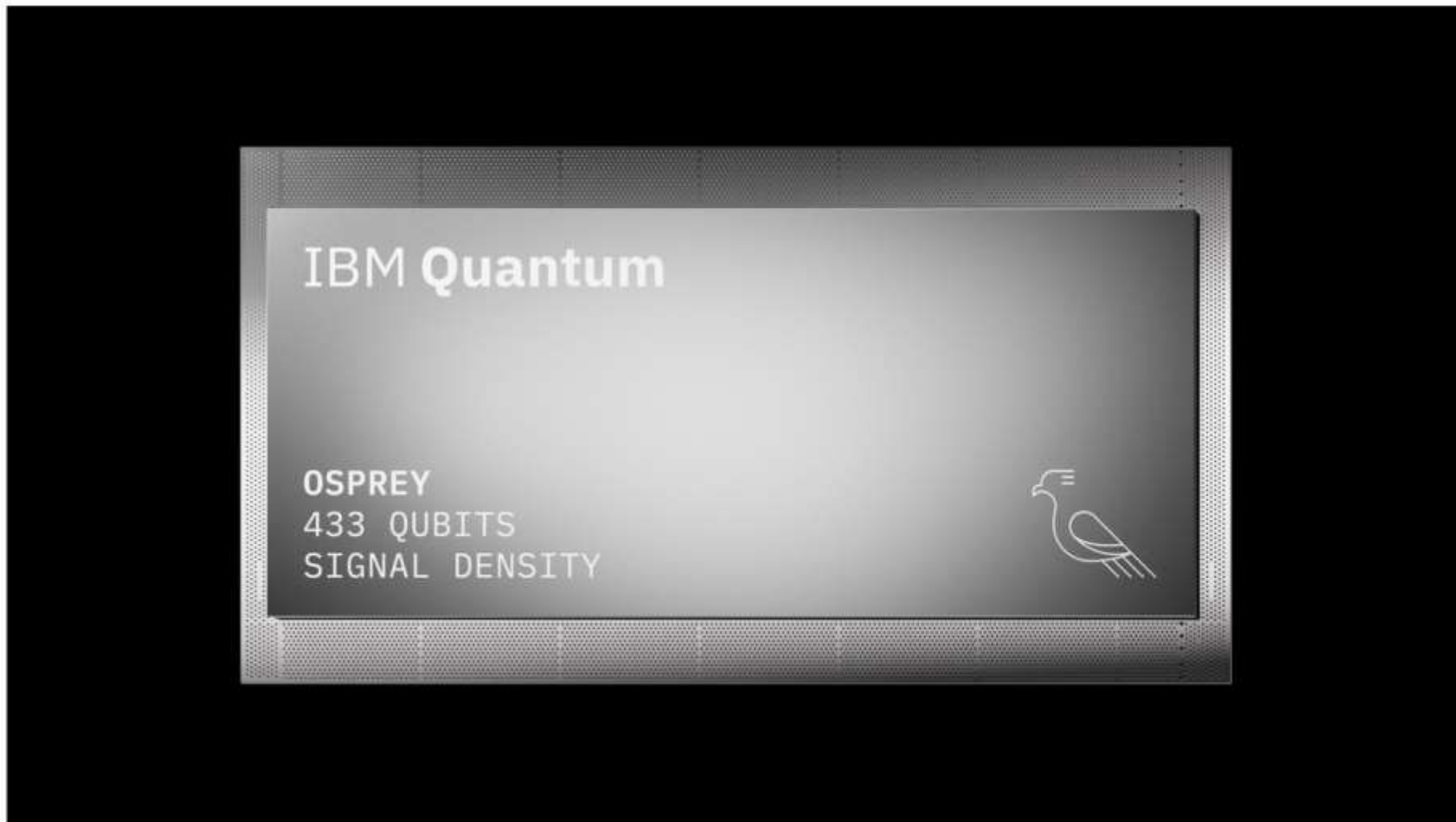
2018

2019

2020

2021

→ 2022



2016

2017

2018

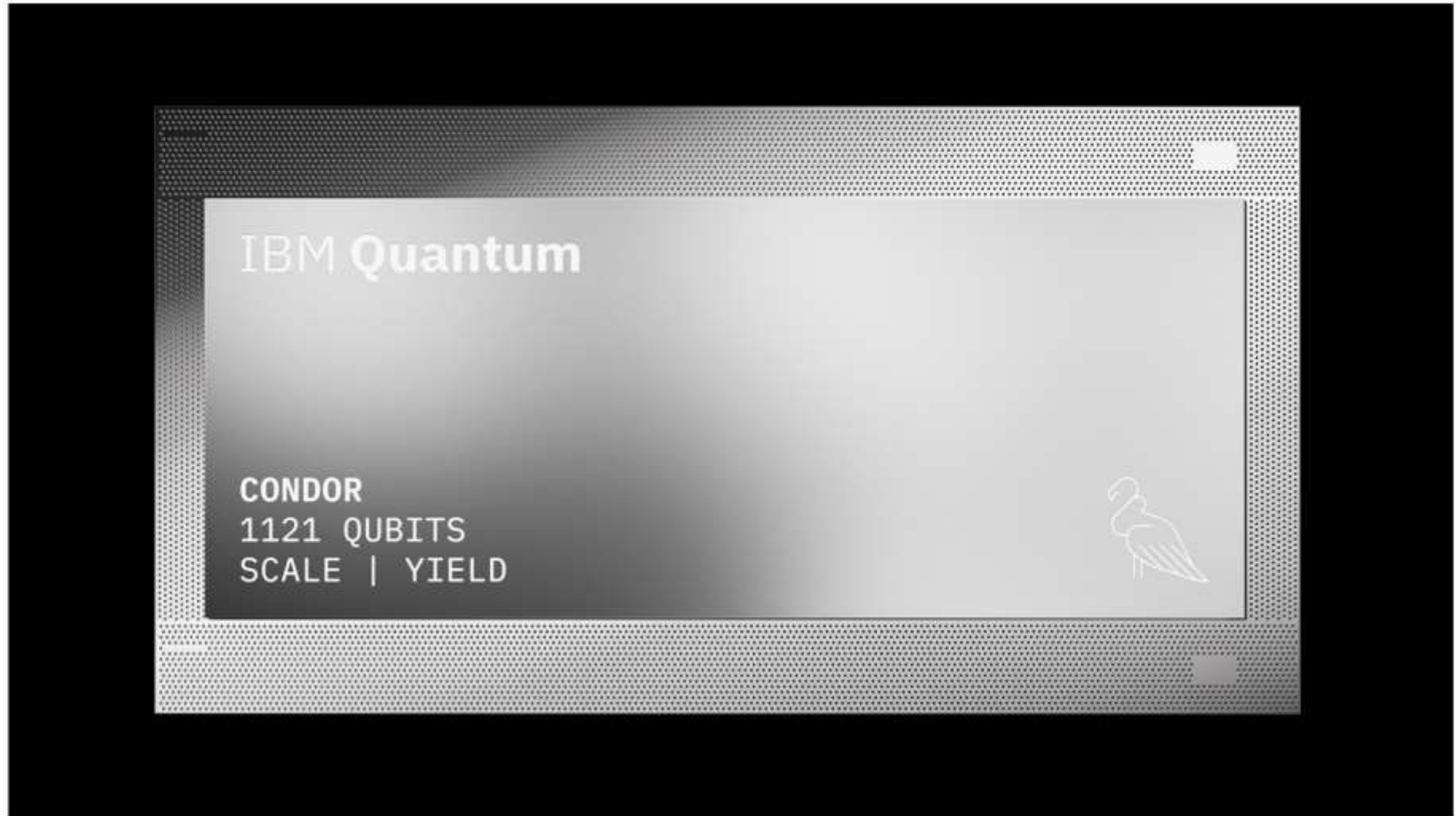
2019

2020

2021

2022

→ 2023



Condor

Pushing the limits of scale & yield

1,121

Superconducting qubits

50%

Increase in qubit density

1 mile +

Of flex cabling



Condor unblocked the
road to scaling.

We now need to focus on
gate depth and quality

2016

2017

2018

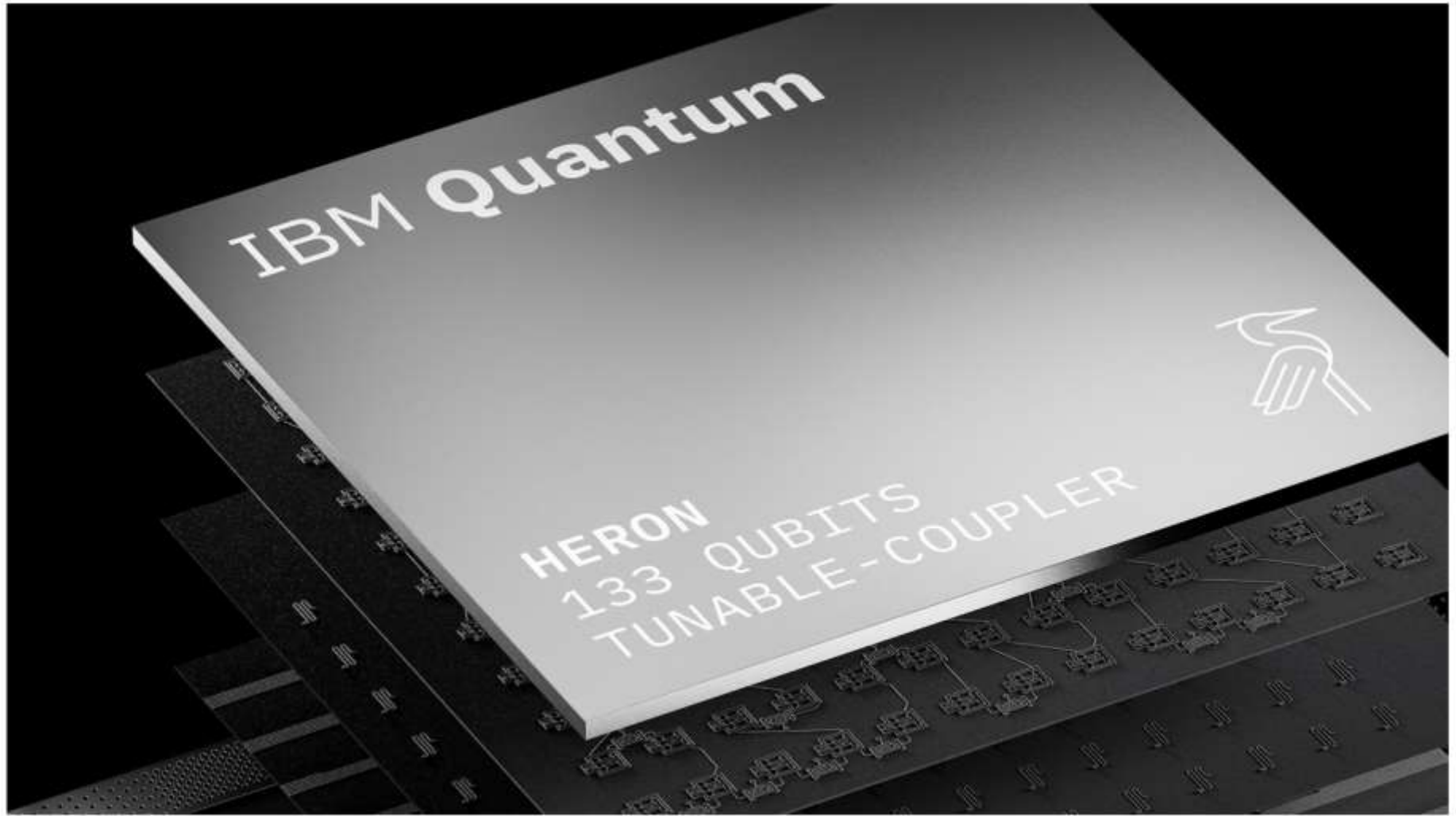
2019

2020

2021

2022

→ 2023



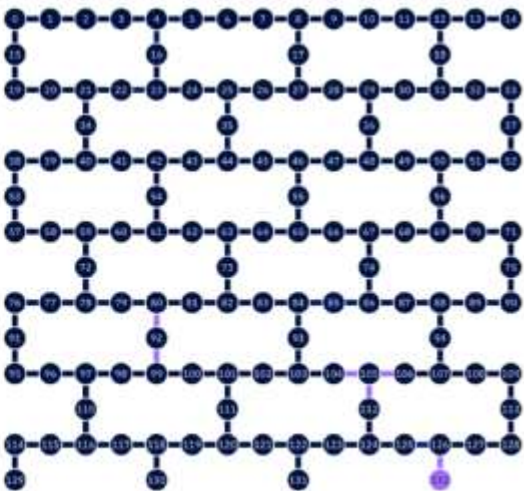
Introducing

Heron

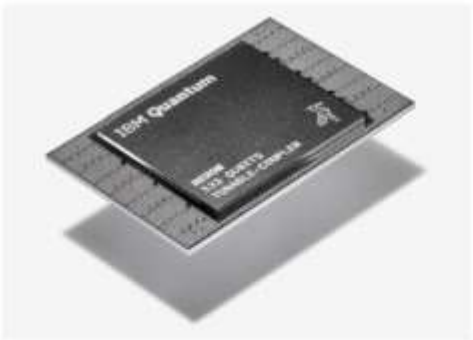
133 qubit systems

Tunable coupler
architecture

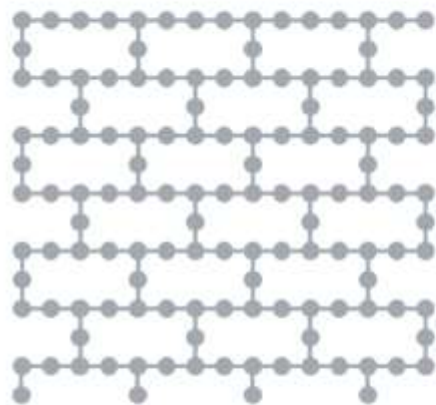
ibm_montecarlo



	<i>ibm_sherbrooke Eagle</i>	<i>ibm_montecarlo (Heron)</i>
Gate Error (best system)	0.6-0.7%	0.3% - Best ~ 0.1%
Crosstalk	High (qubit-qubit collisions)	Almost zero!
Gate time	500-600ns	90-100ns



Tunable Coupler architecture - Performance



A major milestone in system performance:

A clear runway to our goal of 5K gates and beyond

Eagle R3

Mean T1 = 269 μ s
Mean ECR gate time = 537 ns

2772 gates

100 qubit circuit

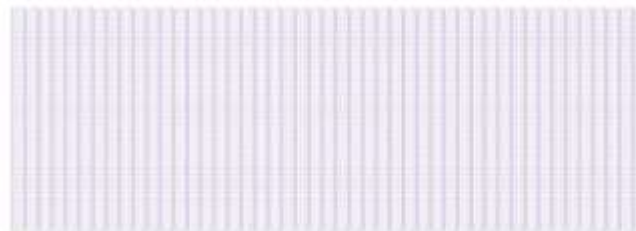


Heron R1

Mean T1 = 174 μ s
Mean CZ gate time = 96 ns

9300 gates (*estimate*)

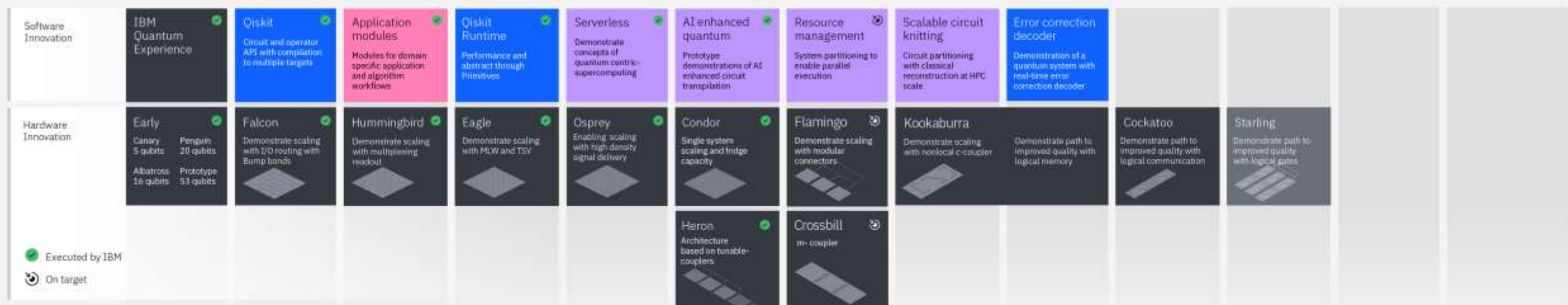
100 qubit circuit



Development Roadmap



Innovation Roadmap



Executed by IBM

On target

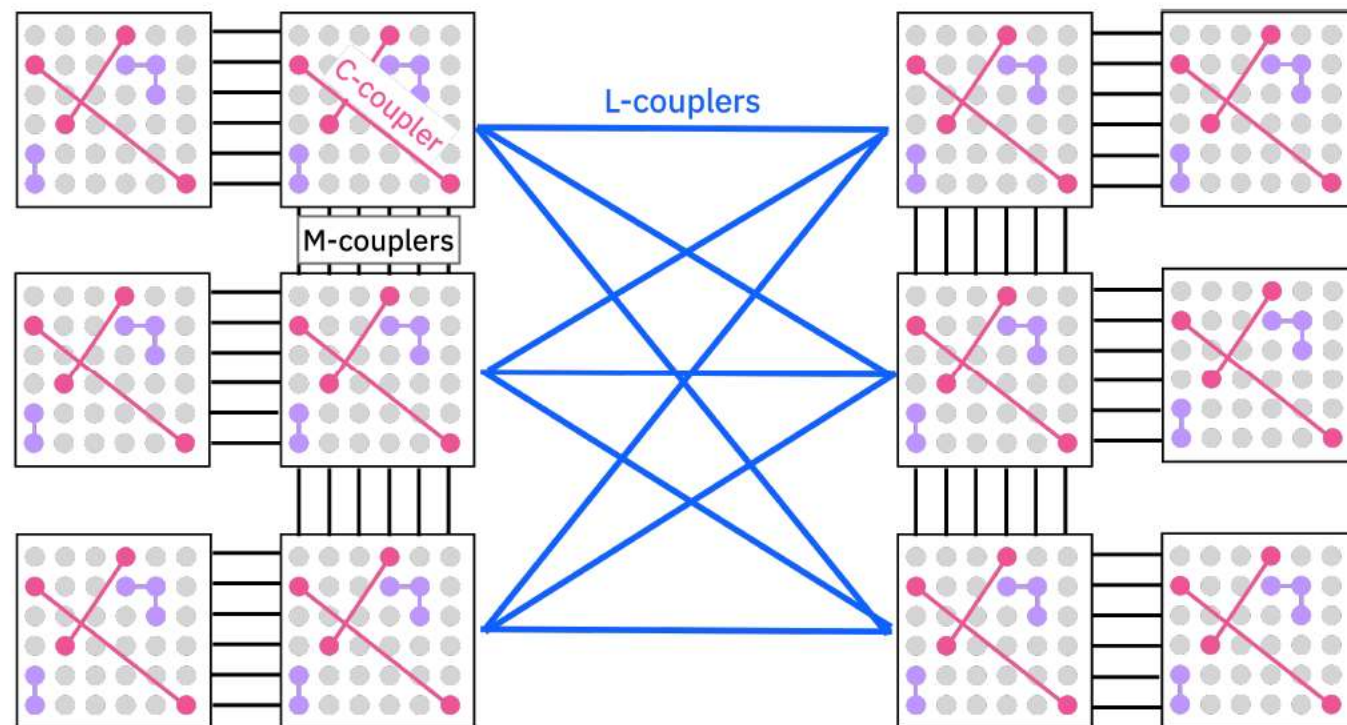
			orchestration	Toolbox
ne				
✓	Dynamic circuits ✓	Execution Modes ↻	Error suppression and mitigation	
✓	Osprey 433 qubits ✓	Condor 1,121 qubits ✓	Flamingo 1,386+ qubits	Kookaburra 4,158+ qubits
		Heron 133 qubits x p ↻	Crossbill 408 qubits	

New error correction codes
and system modularity

C-coupler enables long-range
on-chip connections for high-rate
LDPC codes

L-coupler enables joining
multiple logical memories to
create large-scale systems

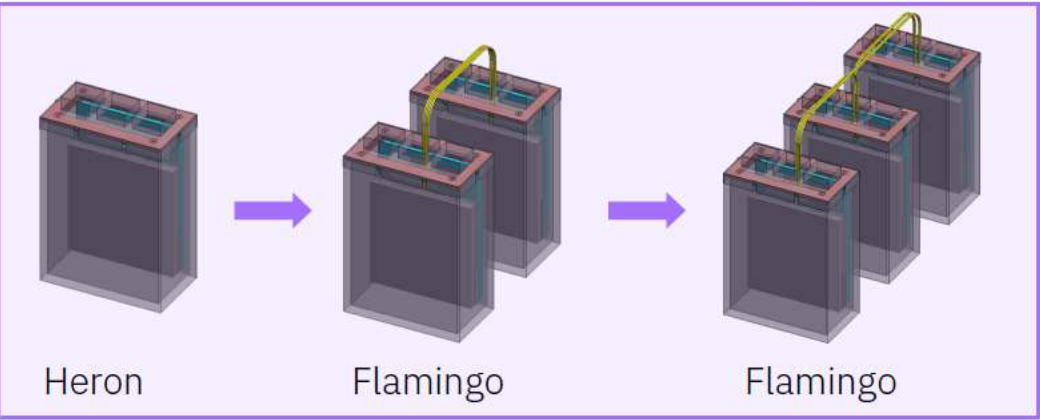
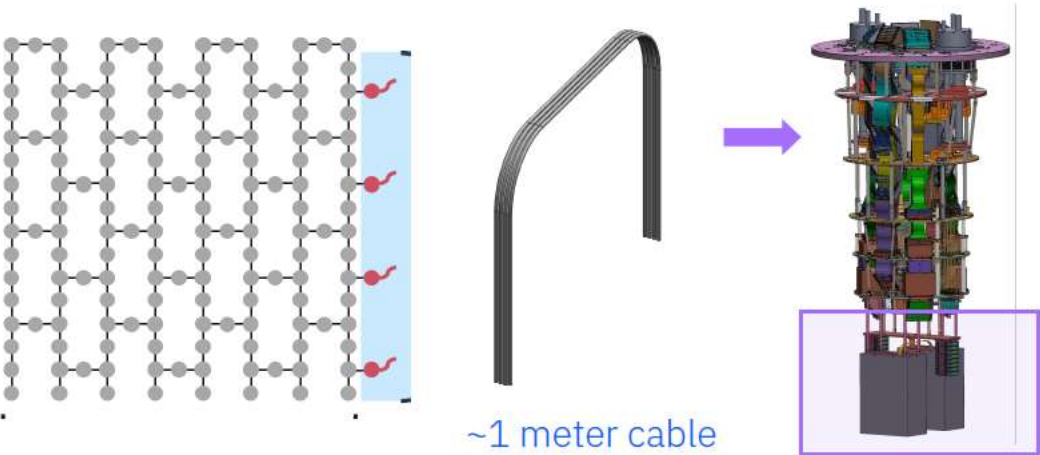
M-coupler enables joining multiple
short-range chip-to-chip connections



Extending Heron platform through modular coupling

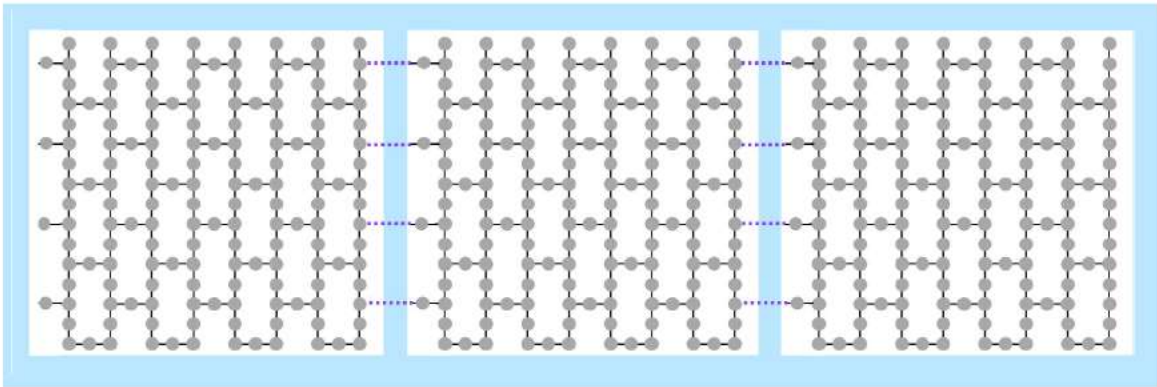
Flamingo

Heron platform + *l-coupler gate* + *l-coupler cable*

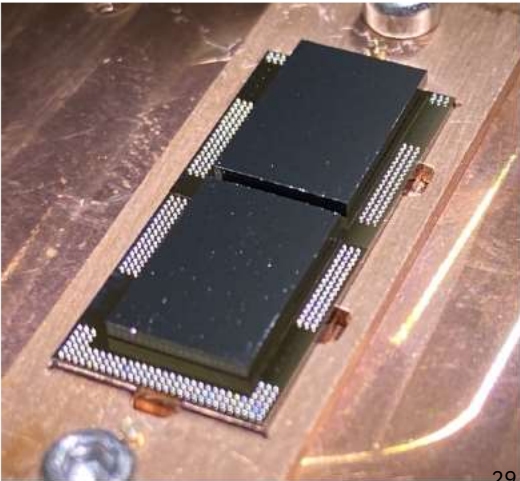


Crossbill

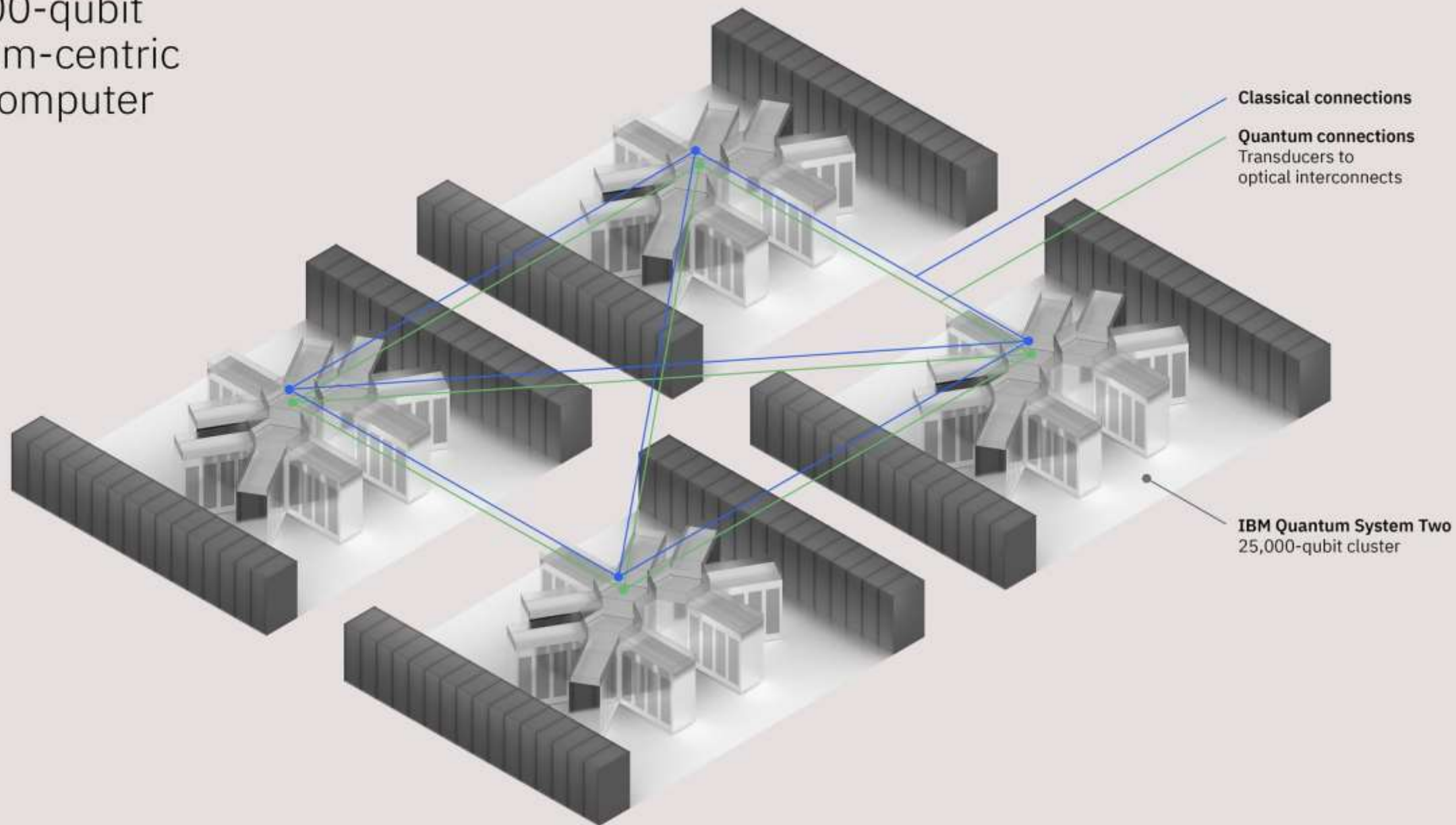
Heron platform + *m-coupler bus* + *m-coupler packaging*



Qubit chiplets within a multi-chip module

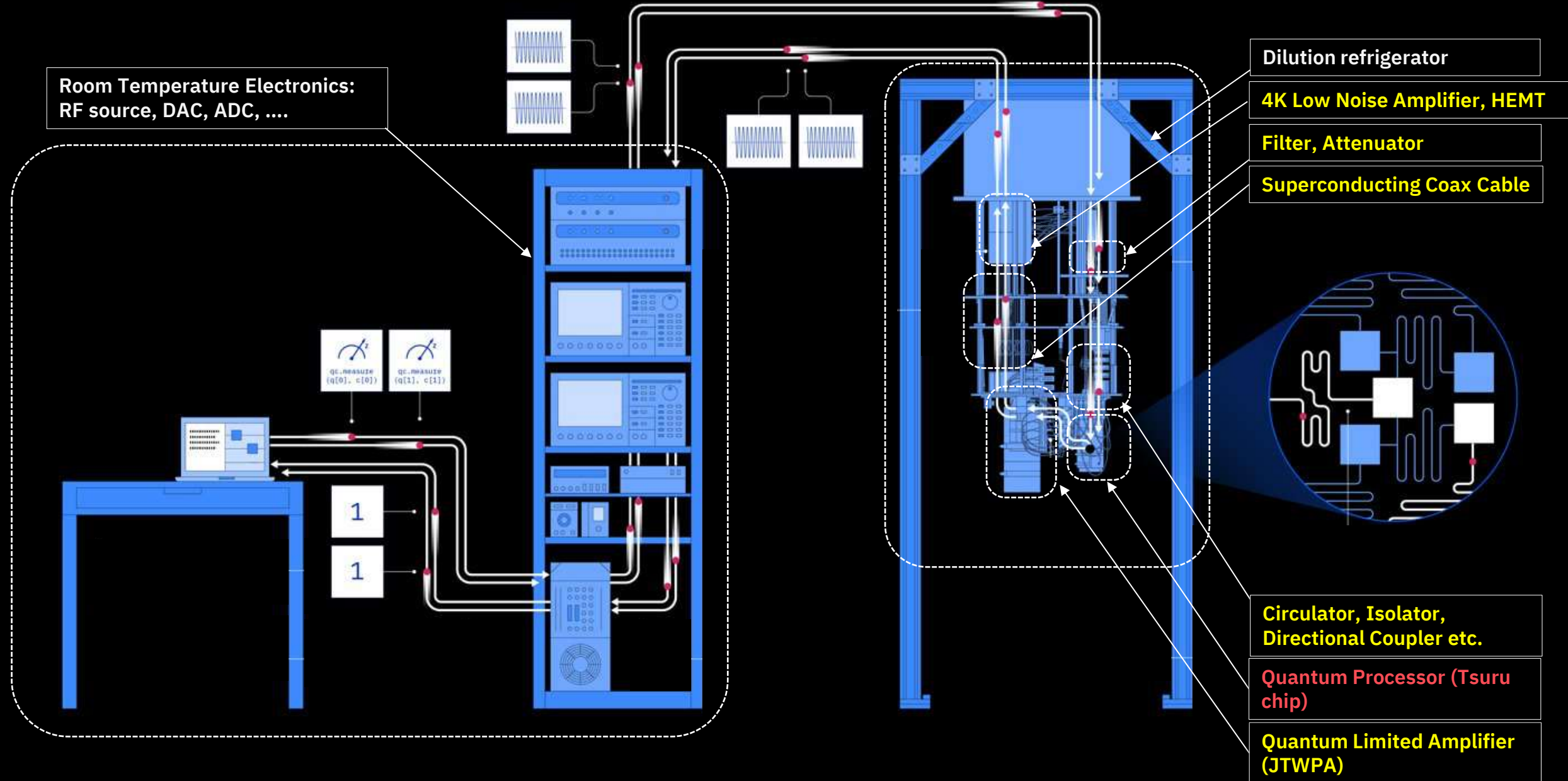


100,000-qubit
quantum-centric
supercomputer
—
2033



Schematic of superconducting quantum computer

IBM Quantum



Quantum systems using coaxial cable wiring (and SMA connectors)



IBM

IBM Quantum / © 2023 IBM Corporation

N. Masluk et al., 2023 CEC/ICMC



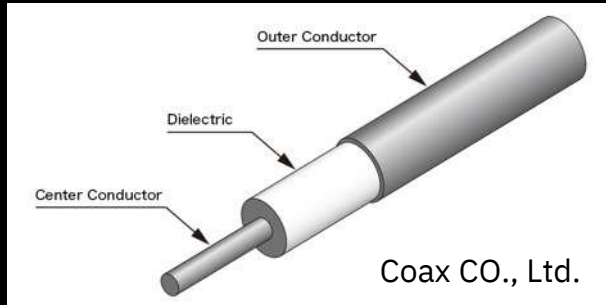
Google

Microwave components innovation is also crucial for further qubit scaling!

Components required for cryogenic microwave measurements

Wiring for microwave input/output

- Low thermal conductivity
- Low loss (for readout line)

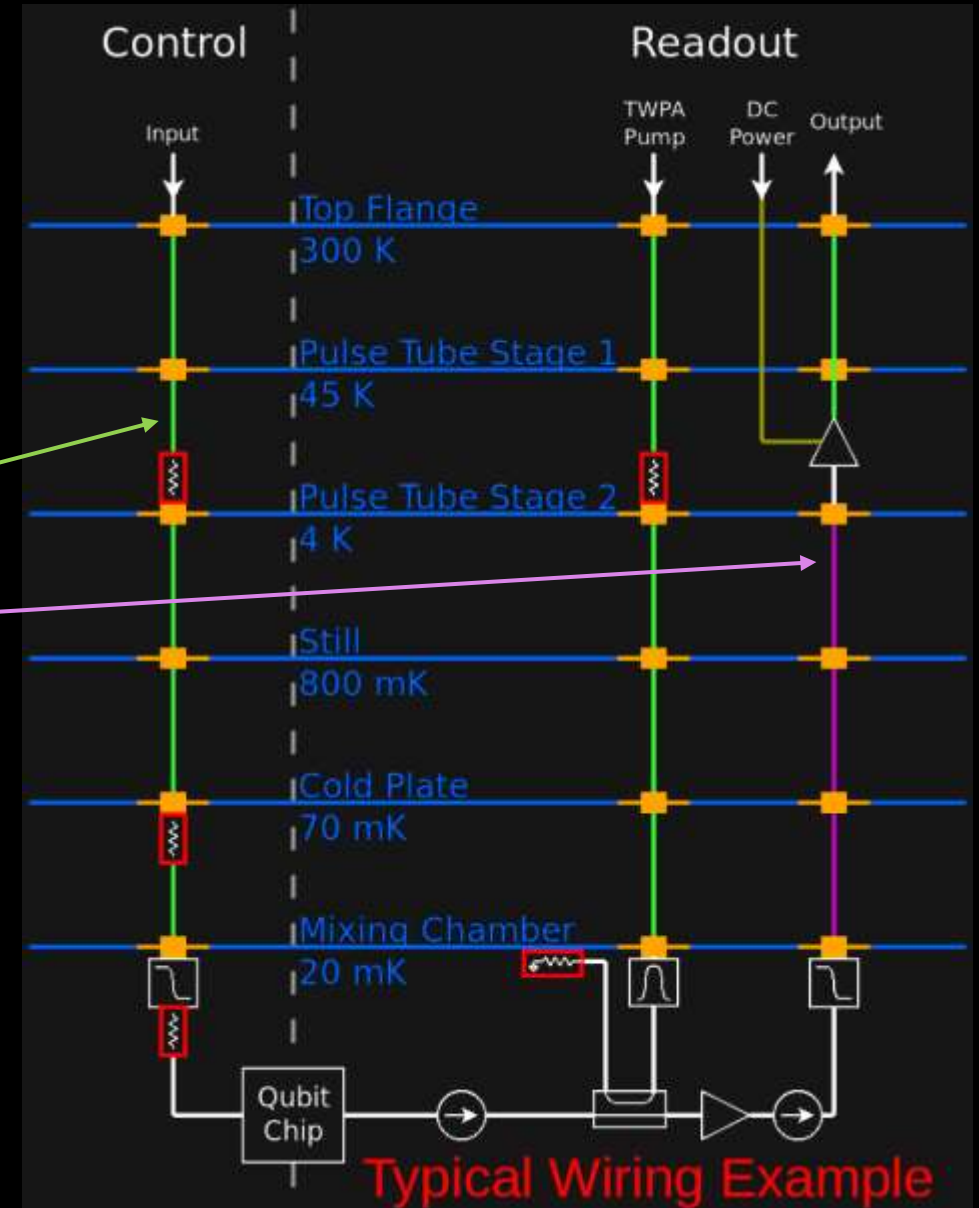


Normal conducting coax for control (e.g. CuNi)

Superconducting coax for readout (e.g. NbTi)



Development of higher density flex wiring is ongoing for more qubit scaling



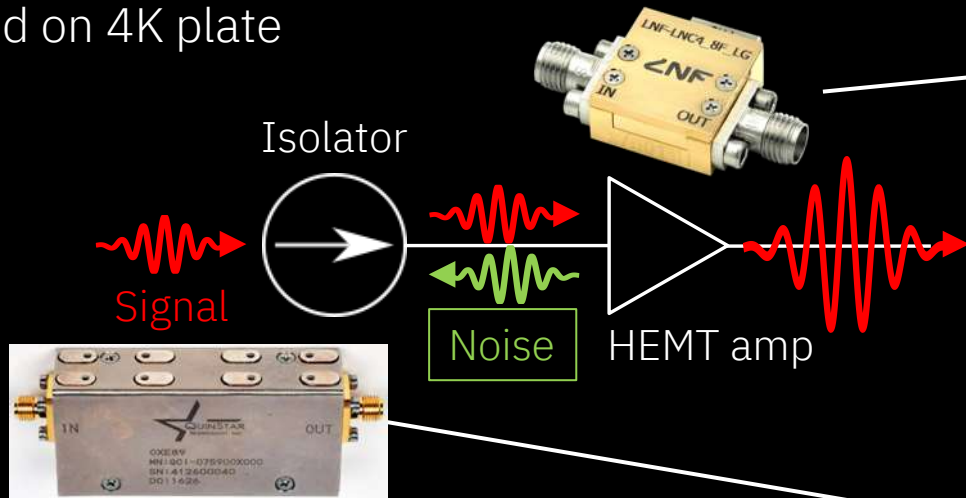
Components required for cryogenic microwave measurements

QLA (Quantum Limited Amplifier)

- Superconducting amplifiers (e.g. TWPA, JPC)
- Utilize nonlinearity of Josephson junctions

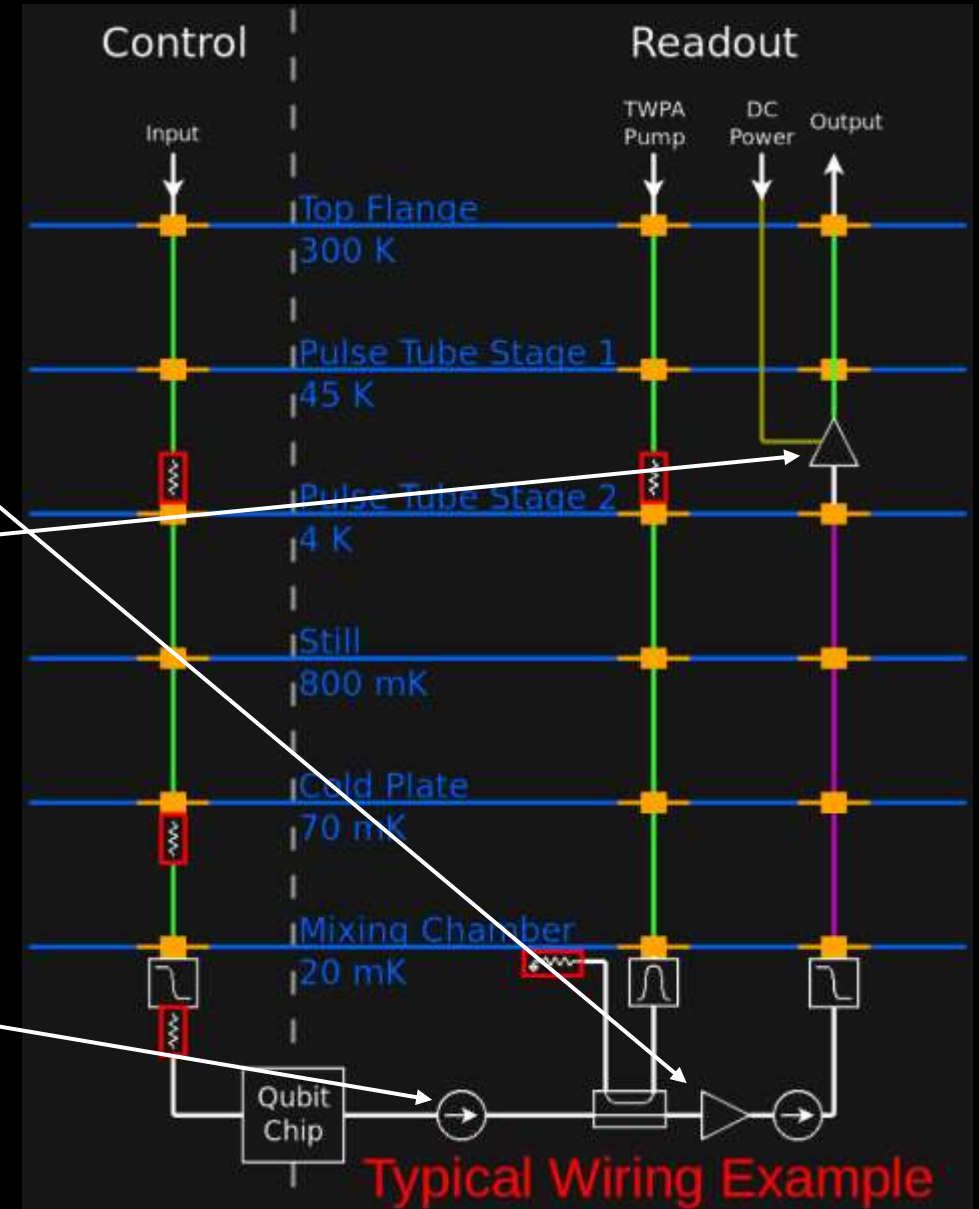
LNA (Low Noise Amplifier), HEMT

- III-V semiconductor amplifiers (e.g. InP, GaAs, etc.)
- Placed on 4K plate



Isolators

- Microwave irreciprocal directional device using magnetism
- Thermal noise isolation



Quantum Hardware Test Center

- Key microwave component development for a robust supply chain
- Established at the University of Tokyo in 2022
- Testbed with IBM qubits



Summary

- Superconducting qubits are non-linear LC oscillators
- Qubit is controlled and measured by microwave drive pulse
- Qubit measurement is done by quantum non-demolition measurement
- Review of the ibm_kawasaki device map and calibration data
- Qubit scaling is done with modularity
- Development of cryogenic microwave components are also crucial for scaling

References

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<https://github.com/Qiskit/textbook/blob/main/translations/ja/ch-quantum-hardware/cQED-JC-SW.ipynb>
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- Nick Masluk, Cryogenic infrastructure for 400 qubits and beyond, Presented at the CEC/ICMC (2023).

Thank you