Design Sanity Check List – Strick Rules

Introduction

This Schematics Sanity check document aims to help customer for make a first verification. It brings some explanations and hints to avoid classical pitfalls.

This document can be used as check list and can be a start point for schematic review. In a second time questions can be shared to ST support in this document. There are areas in this document to lay down questions or ask for ST verification on a precise point.

The review focuses on the STM32MP1, the STPMIC, the DDR DRAM, the boot memories, USB connection and Ethernet.

Other components connected to STMP31MP1 are not in the scope of the sanity check list.

Table of Contents

1 PMIC

ST supplies different part number of STPMIC1. **A or B suffix** are pre-programmed devices to support default power distribution scheme for STM32MP15x family and **C or E suffix** for the STM32MP13 family. Depending on the suffix, it assigns voltages level and rank of the STPMIC regulators to suite with STM32MP1x supplies.

A suffix with VIN= 3.3V or D suffix- with VIN=4V is for STM32MP1 I/Os in 3.3V I/Os typically for wall adaptor or USB bus-powered applications.

B/E Suffix with VIN=3.6V meant for ST3M32MP1 1.8V I/Os typically for 1-cell 3.6 V Li-Ion / Li-PO battery powered application.

C suffix requires programming of non-volatile memory of PMIC (warning: board with C suffix does not start if not programmed). Details regarding default configuration can be found in DS in table *Default NVM configuration vs part number.*

Warning! NVM write operation require VIN>3.8V (cf DataSheet) so a bench with VIN=3.8V is needed to reprogram NVM

1.1.1 PMIC external components

It is strongly recommended to use the part numbers (P/N) given in the PMIC Data Sheet BOM in § Recommended external components

The choice of inductance and capacitors is very sensitive, for the BUCKs in particular. Their characteristic (effective capacitance, inductance) must be the equivalent as the P/N given in the data sheet BOM.

Values and sizes of all the capacitors must be equivalent to the ones of this BOM. This set of external components is already at a certain level of size optimization. *It has been validated by testing* in ST and aims to sustain longevity and good PMIC operating.

☐ Check values and size of the below table2 are correct on schematics.

Table 2. Passive components

Component	Manufacturer	Part number	Value	Size
CVIN, CLDO1OUT, CLDO2OUT, CLDO4OUT, CLDO5OUT, CLDO6OUT, CINTLDO	Murata	GRM155R60J475ME47#(1)	4.7 µF	0402
CVLXBST, CBUCK1IN, CBUCK2IN, CBUCK3IN, CBUCK4IN, CLDO3IN, CLDO3OUT(2)		GRM188R61A106KE69D	10 µF	0603
CLDO16IN, CLDO25IN, CVREF		GRM155R61E105KA12	1 µF	0402
CVBUSOTG		GRM188R61C475KE11#	4.7 µF	0603
CBSTOUT, CVOUT1, CVOUT2, CVOUT3, CVOUT4		GRM188R60J226MEA0	22 µF	0603
CSWOUT		GRM31CR60J227ME11L	220 µF	1206
LX1, LX2, LX3, LX4, LXB		DFE252012P-1R0M=P2	1 µH	1008

1. *# is the last P/N digit; it indicates a package specification code.*
2. *4.7 µF normal mode - 10 µF sink/source mode - no cap bypass mode.*

For an alternative component set choice read below in STPMIC recommendation chapter below.

☐ On LDOs and BUCKs inputs, place the decoupling capacitor as close as possible to the relative input pins to minimize the induced noise

☐ PMIC regulators may be assigned to proper power domains according to the default PMIC default power scheme below. OpenSTLinux software device tree configuration follow by default this.

STM32MP15x or STM32MP13 with STMPIC 1A or 1B

BUCK1 (rank2) -> VDD_CORE and VDDCPU (for MP13)
BUCK2 (rank0) -> VDD_DDR
BUCK3 (rank1) -> VDD
BUCK4 (rank2) -> 3V3
LDO3 (rank0) -> VTT_DDR3 (0.675 V) ("fly-by" topology)
or VDD1_DDR (1.8V) (LPDDR design)
LDO3in <- BUCK2out (VDD_DDR 1.35V), when VTT_DDR3 is needed
or BUCK3out(VDD 1.8V)
LDO4 (rank3) -> VDD_USB
LDO5-(rank2) > SD card or boot flash

STM32MP13 with STPMIC1D or 1E

BUCK1 (rank3) -> VDD_CPU
BUCK2 (rank0) -> VDD_DDR
BUCK3 (rank1) -> VDD optionally -> VCC boot flash (eMMC(VCC+VCCQ), NOR, NAND)
BUCK4 (rank2) -> VDD_CORE
LDO4 (rank3) -> VDD_USB
LDO3 (rank0) -> VTT_DDR3 ("fly-by" topology) or VDD1_DDR(LPDDR design)
LDO3in <- BUCK2out (VDD_DDR 1.35V), when VTT_DDR3 is needed
or BUCK3out(VDD 1.8V)
LDO5 (rank2) -> SD card or VCC boot blash (eMMC, NOR, NAND)
LDO2 (rank 0) -> VDDSDx to supply SD card IOs in 1.8V option if UHS-I mode needed

Caution***: supply on VDD3V3_USB be switched ON after VDDA1V8_REG.*** This is the case when using the STMPIC power scheme above.

Note: BUCK2 is rank 0, so not automatically enabled. The TF-A (fist stage boot loader) will make I2C access to set the correct voltage value given in the device tree and enable it. The NVM voltage value is not used for BUCK2 initialization.
Note: This default PMIC power scheme matches the STM32MP1 *power supplies characteristics requirements*. It complies also with the expected STM32MP1 power ON/OFF/low-power sequences.

☐Every BUCK input must be connected to same supply as VIN (2.8V - 5.5V DC) as internally connected inside STPMIC

☐Every BUCK input BUCKxIN must be decoupled with 10uF capacitor

PMIC pinout	Value
BUCK1IN, BUCK2IN, BUCK3IN, BUCK4IN	10 uF

Note: In case BUCK4 are not used, it is recommended to connect BUCK4 input pins to PGND reference.

☐1 uH inductor must be populated in loop VLX node - VOUTx node for each BUCK converter

PMIC pinout	Value
VLX1, VLX2, VLX3, VLX4	1 uH

☐BOOST input VLXBT must be decoupled with 10uF capacitor to PGN reference

PMIC pinout	Value
VLXBST	10 uF

☐1 uH inductor must be populated between VLXBST input and VIN

PMIC pinout	Value
LXB	1 uH

☐Every BUCK converter output VOUTx must be decoupled with 22uF capacitor

PMIC pinout	Value
VOUT1, VOUT2, VOUT3, VOUT4	22 uF

☐Inputs of LDO16 and LDO25 must be decoupled with 1uF capacitor

PMIC pinout		Value
LDO16IN, LDO25IN		1 uF

☐ Input and Output of LDO3 must be decoupled with 10 uF capacitors

PMIC pinout	Value
LDO3IN, LDO3OUT	10 uF

☐ VIN input must be decoupled with 4.7uF

Caution, for train or bus applications, VIN should not have transient voltage out of Absolute Max Rating -0.5 to 6.5 V (STPMIC DS table4)

☐ VREFDDR output must be decoupled with 1uF capacitor

☐ LDO1/2/4/5/6 , INTLDO **output** pins are decoupled with 4.7uF capacitor.

☐ VBUSOTG pin is decoupled with 4.7 uF capacitor near the USB connector.

☐ VIN : For battery application with LPDDR, a bulk decoupling capacitor (a few hundred µF) may be inserted on PMIC VIN pin to limit the dropping speed to avoid “lpDDR2 / lpDDR3 uncontrolled power-off sequence” (AN5260)

☐ when PWR_SW has “CSWOUT” decoupling capacitor value avoid voltage drop when connecting USB peripheral. Can be smaller if PWR_SW do not supply USB connector but a component (10-20 uF enough).

☐ PMIC VIO must be connected to VDD domain

☐ when VTT_DDR is needed, ensure input voltage for LDO3 is VDD_DDR domain (from BUCK2 output), Note: VTT_DDR is not needed in point-to-point topology

☐ when SWOUT pin is used for 5V USB host. BOOST can ensure a stable 5V even if VIN is < 5V. BOOST is bypassed within PMIC when VIN > 5.2V. **SWIN pin must be connected to BSTOUT pin in this case.**

☐ when VBUSOTG pin is used, the BOOST converter must enabled (internally, the BOOST -> PWR_USB_SW -> VBUSOTG pin) => 1 uH inductor must be populated between VLXBST input and VIN + VLXBST decoupling

☐ Analog supplies (VDDA, VREF+) must not be provided by BUCK converters, LDO from PMIC should be used. Otherwise, the ADC performance will be significantly degraded.
This usually means that VDDA is around 3V max.

Note: The PMIC power scheme is VIN (5V) -> PMIC BUCK -> 3.3V -> PMIC LDO1 -> VDDA.
Alternative: VDDA can be connected to VDD through an inductor-based filter.

☐ when BUCKx is not used, BUCKx output pin floating. BUCK1&2 input pin have always to be connected to VIN (to ensure LDO functionality) , BUCK3&4 input pin connected to GND

☐ when LDOx is not used, LDOx output pin floating and LDOx input pin connected to PGND

Note: In case of design where LDOx input pin is powered but LDOx output floating, ensure the LDO is not enabled, otherwise over consumption.

☐ when BOOST is not used, VLXBST, BSTOUT, VBUSOTG pins could be left floating but PGND5 connected to GND.

☐ when PWR_SW is not used, SWIN, SWOUT pins could be left floating (even if BOOST is ON).

Please leave comments or questions regarding PMIC design in case of any doubts.

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Please leave here comments or question regarding PMIC design in case of any doubts

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1.1.2 PMIC control pins

☐ 1.5 Kohm pull-up I2C SDA, SCL lines between STPMIC and STM32MP1

☐ It is highly recommended to use I2C4 or I2C6, since they are securable. it protects the STPMIC power configuration from attack or software failure.
Also Prefers I2C4 to use the default OpenSTLinux configuration (using other I2Cx instance will require modifying TF-A code).

☐ **PMIC PWRCTRL pin must be connected to *STMP32MP1* PWR_ON** pin that is driven by STM32MP1 PWR block when entering/exiting in low-power modes. PWR_ON pin (active high): "supply request signal" is inactive in STM32MP1 *Standby mode*, in *VBAT mode,* in power Off. PWR_ON pin has a push-pull and driven (high or low) by STM32MP1 in all power modes whenever VDD is present. **No pull-up is needed on the line**. PMIC internal pull-up/down is not set by default but the pin is not used by PMIC to boot STPMIC into MAIN mode.

☐ **PMIC WAKEUP pin should be connected to STM32MP1 PC13** (RTC_OUT1), to have capability to wake-up PMIC from Standby from internal RTC. This PMIC pin has an internal pull-up, **no external pull-up is needed.** In case PMIC WAKEUP pin is not used it can left floating

☐ PMIC PONKeyn pin can be connected to Push button.
This pin has an internal pull-up, If no push button can be left unconnected.
Note: PONKEY pin has a debouncing that is not in WAKEUP pin.

☐ **PMIC INTn pin to be connected to a STM32MP1 wake-up pin** (any WKUPx GPIO AF) to exit from Standby mode with the STPMIC PONKey. Needed also for communication with STMP32MP1.

List in RefMman PWR_WKUPCR reg and data sheet

STM32MP13 : PF8 WKUP1 / PI3 WKUP2 / PA4 WKUP4 / PI2 WKUP5 / PA3 WKUP6

STM32MP15 : PA0 WKUP1 / PA2 WKUP2 / PI8 WKUP4 / PI11 WKUP5/ PC1 WKUP6

☐ **PMIC RST pin connected to the STM32 reset line**. A 0 Ohm resistor should be placed between MP1 and PMIC. This is to turn MP1 into RMA mode (Return Material Acceptance. RAM is product live cycle state to permit MPU chip default analysis test in ST manufacturing) , in this case MP1 must be reset with VDDCORE is kept ON (ie no rest on STPMIC) .

Please leave comments or questions regarding PMIC Control pins design in case of any doubts.

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2 STM32MP1

2.1.1 STM32MP1 internal regulators and supplies

☐ The VBAT pin can be connected to the external battery (1.2 V < VBAT < 3.6 V). If **no external battery** is used, **it is mandatory to connect this pin to VDD.**

☐ When VDD < 2.25V, BYPASS_REG1V8 pin must be connected to VDD pin and VDDA1V8_REG pin supplied by VDDA_1V8 power domain. Otherwise, BYPASS_REG1V8 pin must be connected to VSS pin.

☐ for STM32MP13, VDDSDMMC1/2 must be connected to 1.8V power domain. When not used , must be connected to VDD

☐ The VDDA is the analogue supply (ADC/DAC/VREFBUF), can be connected to an independent power supply . Alternatively, VDDA can be connected to VDD, through an inductor based filter for additional precautions.

☐ Connect VDD3V3_USB (HS/FS) pin to "VDD_USB3V3 power domain".

Caution for discrete power supply : **supply on VDD3V3_USB must be switched ON *after* VDDA1V8_REG**.

VDDA1V8_REG is supplied by VDD, when BYPASS_REG1V8 pin=VSS. In this case with discrete power supply, VDDA1V8_REG can control a power switch or MOFSET transistors to enable supply of VDD3V3_USB(HS/FS) pins. (ref example in AN5256 or AN5474)

This is fine in the case when design follows the default PMIC power scheme: LDO4 (rank2) powers VDD3V3_USB after VDD (supply of VDDA1V8_REG if not by passed) or after BUCK3 (rank1) (VDDA1V8_REG if by passed)

☐ check on VDDA1V8_REG & VDDA1V1_REG a 2.2uF decoupling capacitor *for each pin* to VSS for USB subsystem

☐ When USB is not used

Leave VDD3V3_USB (HS/FS) pins unconnected or to VSS

Leave VDDA1V1_REG pin unconnected without the decoupling capacitor,

Leave VDDA1V8_REG pin unconnected without the decoupling capacitor if DSI not used

☐ VDDA1V8_DSI (depends on product) connect VDDA1V8_REG

☐ VDDA1V2_DSI_PHY (depends on product) connected VDDA1V2_DSI_REG

☐ When DSI is not used

Leave VDDA1V8_DSI, VDDA1V2_DSI_PHY pins unconnected or to VSS

Leave VDDA1V2_DSI_REG pin unconnected without the decoupling capacitor, if USB not used leave VDDA1V8_REG pin unconnected without the decoupling capacitor

☐ The STM32MP1 embedded regulators must NOT be used to supply external components unless specifically mentioned. It relates to DSI, USB PHY regulator.

☐ Connect VDD_ANA, VDD_PLL, VDD_PLL2, VDD_DSI pins (on STM32MP15) to VDD power domain

☐ Connect VSS_ANA, VSS_PLL, VSS_PLL2, VSS_USB to VSS

☐ Connect VREF+ pin to external supply (VREF+ may range from 1.62 V to VDDA). It can be connected to VDDA power domain directly. Alternatively, VREF+ can be supplied internally by VREFBUF block, keep decoupling capacitor with VREF- in this case and avoid external voltage supply.

☐ VREFBUF can be used to as supply for external circuitry on VREF+ pin but in this case ADC conversions may be affected.

☐ When available (depending on package), VREF– pin must be externally tied to GND

☐ VSS pin and VSSA pins should be connected to GND layer

☐ When analog peripherals (ADC/DAC/VREFBUF) are not used (for minimalist designs):

Leave VREF+ unconnected to VSS without decoupling capacitors.

VDDA connected to VSS or to VDD or left unconnected

Note In this case, internal temperature measurement with ADC is not more usable, DTS and temperature monitoring sensors are still available.

☐ For discrete power supply solution, the voltage regulator modules that supply the MP1 (VDD, VDDCORE, VDDCPU (MP13), VDD_DDR) should to follow the characteristics detailed in § Voltage regulator module (VRM) specification of in AN5256 (MP15), in AN5586 (MP13) .

2.1.2 Decoupling

2.1.2.1 STM32MP1 external components

A sanity check can be done on *values* of the capacitors present on the schematic.

The *number* of capacitors, their *size*, their *characteristics* is customer choice and responsibility.

Decoupling capacitor table for STM32MP15 table 4 AN5031 :

Table 4. Amount of decoupling recommendation by package(1)

Supplies pins	Decoupling point(2)	Value	LFBGA354 xAB	TFBGA257 xAD	TFBGA361 xAC	LFBGA448 xAA	Comments
V_{BAT}	V_{SS}	100 nF	1	1	1	1	could be skipped if V_{BAT} is connected to V_{DD} or if a supercapacitor is used instead of a battery
V_{DDCORE}	V_{SS}	1 µF(3)	15	15	15	15	Not including capacitors on PMIC/SMPS
V_{DDQ_DDR}	V_{SS}	1 nF	2	2	2	2	Not including capacitors on PMIC/SMPS and additional capacitors on DDR memory
		3.3 nF	0	3	0	0	
		1 µF(3)	4	2	7	7	
V_{DD_ANA}	V_{SS_ANA}	1 µF(3)	1	-(4)	1	1	-
V_{DD_PLL}, V_{DD_PLL2}	V_{SS_PLL}, V_{SS_PLL2}	1 µF(3)	2	-(4)	-(4)	2	Not including capacitors on PMIC/SMPS.
V_{DD}, V_{DD_DSI}	V_{SS}	1 µF(3)	4	4	4	4	
$V_{DD1V2\_DSI\_REG}$, $V_{DD1V2\_DSI\_PHY}$	V_{SS_DSI}	2.2 µF(3)	1	-	1	1	-
	V_{SS}		-	1(5)	-	-	
V_{DDA1V8_REG}	V_{SS_USBHS}	2.2 µF(3)	1	-	1	1	-
	V_{SS}		-	1(5)	-	-	
V_{DDA1V8_DSI}	V_{SS_DSI}	1 µF(3)	1	-	1	1	V_{DDA1V8_DSI} must be connected to V_{DDA1V8_REG}
	V_{SS}		-	1(5)	-	-	
V_{DDA1V1_REG}	V_{SS_USBHS}	2.2 µF(3)	1	-	1	1	-
	V_{SS}		-	1(5)	-	-	
V_{DD3V3_USBHS}, V_{DD3V3_USBFS}	V_{SS_USBHS}	1 µF(3)	1	-	1	1	-
V_{DD3V3_USB}	V_{SS}		-	1(5)	-	-	
V_{DDA}	V_{SSA}	100 nF + 1 µF(3)	1+1	1+1	1+1	1+1	V_{SSA} must be connected to V_{SS} plane
V_{REF+}	V_{REF-} and V_{SSA}	100 nF + 1 µF(3)	1+1	-	-	1+1	V_{REF-} must be connected to V_{SSA} then V_{SS} plane
	V_{SSA}		-	1+1 (6)	1+1 (6)	-	V_{SSA} must be connected to V_{SS} plane

1. This table could be used as a guideline, the real count and values of capacitors could be adapted depending of various parameters: capacitor size, capacitor dielectric, PCB technology, and using results of product power integrity simulations.
2. All V_{SS_x} and V_{SSA} must be connected to a common V_{SS} plane.
3. Multi Layer Ceramic Capacitor type (MLCC).
4. Supply internally merged with V_{DD}.
5. Supply return path internally merged with V_{SS}.
6. V_{REF-} internally merged with V_{SSA}.

Decoupling capacitor table for STM32MP13 table 4 AN5474 :

Table 4. Decoupling recommendations by package

Supply pin	Decoupling point(1)	Value(2)	TFBGA289 (9 x 9)	TFBGA320 (11 x 1)	LFBGA289 (14 x 14)	Comments
VBAT	VSS	100 nF(3)	1	1	1	Can be skipped if VBAT is connected to VDD, or if a super capacitor is used instead of a battery.
VDDCORE	VSS	1 µF	8	8	8	Not including capacitors on PMIC/SMPS
VDDCPU	VSS	1 µF	7	7	7	Not including capacitors on PMIC/SMPS
VDDQ_DDR	VSS	1 nF	7	7	6	Not including capacitors on PMIC/SMPS and additional capacitors on DDR memory
		1 µF	3	3	3	
VDD_ANA	VSS_ANA	1 µF	1	1	1	-
VDD_PLL, VDD_PLL2	VSS_PLL, VSS_PLL2	1 µF	2	2	2	Not including capacitors on PMIC/SMPS
VDD	VSS	1 µF	4	4	4	
VDDSD1/VDDSD2	VSS	1 µF	1/1	1/1	1/1	
VDDA1V8_REG	VSS_USBHS	2.2 µF	1	1	1	-
VDDA1V1_REG						
VDD3V3_USBHS		1 µF				
VDD3V3_USB	VSS	1 µF				
VDDA	VSSA	100 nF + 1 µF	1+1	1+1	1+1	VSSA must be connected to VSS plane.
VREF+	VREF- and VSSA					VREF- must be connected to VSSA, then to the VSS plane.

1. *All VSS_X and VSSA must be connected to a common VSS plane.*
2. *All µF capacitors are MLCC (multilayer ceramic).*
3. *Rise time should be less than 33 us/V.*

☐ Add it in your schematic: "*Place the input capacitor as close as possible to the relative input pins to provide a clean input voltage (avoiding noise switching)".*

☐ It is recommended to use one capacitor rather that multiple decoupling capacitors.

☐ MP1 DDR_VREF pin must have a100nF decoupling to VSS

☐ Avoid ferrite bead in digital power domain.

Note: Ferrite bead between *power domains* and VDD, VDD_CORE, VDD_DDR pins increases the PDN impedance: On VDD_CORE risk of crash on voltage undershoot is to evaluate. On VDDQ_DDR risk of DDCR Clk jitter, on VDD risk to disturb LTDC signals

Please leave comments or questions regarding MP1 Power distribution design in case of any doubts.

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2.1.2.2 DDR decoupling (DDR Memory side)

DDR decoupling is not under scope of the sanity check list. You will find DDR decoupling capacitors, guidance for values expected in DDR data sheet or with the memory manufacturer.

If DDR decoupling scheme is not accessible from manufacturers, ST recommends the values proposed in MP1-DDR Layout examples zip file under 'Gerber files' : https://www.st.com/en/microcontrollers-microprocessors/STM32MP17.html#resource

2.1.3 Specific MP1 connection

2.1.3.1 Reset / PDR

☐ STM32MP1 pins PDR_ON, (PDR_ON_CORE for STM32MP15x), must be connected to VDD, even with STPMIC

☐ Check NRST line is connected at least between STM32MP1, STPMIC, Boot memories (please see the Boot memories section, not always), JTAG, discrete power supplies.

☐ Avoid push-pull output on NRST line (e.g. external watchdog)

☐ on STMP32MP1 NRST pin one 10nF decoupling capacitor is required (data sheet states conservative 100nF value, can be less). No external pull-up resistor is connected to NRST because of 40Kohms internal one. Always Keep the decoupling on the pin (even if connected to other device like a Push-button with smart reset as STM6519)

☐ NRST_CORE pin (for STMP32MP15x), should be decoupled with 10nF, when NRST and NRST_CORE are not connected together.

☐ For *discrete* power supply for STM32MP15x, for design where there is no VDDCORE Power on cycle on NRST, NRST and NRST_CORE must be connected with a capacitor of 1/10th the capacitor put on NRST. See further details in AN5031 §4.3.3 or STM32P1 DS.

☐ For *discrete* power supply for STM32MP13x, there must be a VDDCPU Power on cycle when NRST is asserted. VDDCPU power supply enable pin must be controlled by PWR_PCU_ON&NRST signal.

Same for VDDCORE, VDDCORE power supply, the enable pin must be controlled by PWR_ON&NRST signal. (because VDDCORE cannot stay when VDDCPU is OFF)

Note: & function uses diode. See AN5474 §8.5.1 figure 22 and AN5586 §5.5.1. In the case of entering RMA state (“Return for Material Analysis” ie when returning devices for failure analysis), the power cycling should not be done while NRSTR is asserted. So, the two diodes connected to PWR_ONRST and PWR_CPU_ONRST must be removed.

2.1.3.2 Wake-up pins and interrupts

☐ Check that line interrupt *toward* STM32MPU from devices that could wake it up (PMIC INTn pin , Charger) is connected to MP1 wakeup pins type (see above the PMIC control pin for wake-up pin list).

Note that GPIO EXTI interrupt are not able to wake-up STM32MP1 from Vbat mode (= system Standby mode (VDDCore off) but in addition with VDD off), only the WKUP pins can.

☐ When multiple interrupt lines c*oming to* STM32MP1

Ensure the EXTI GPIO pins are not connected to the same GPIO number on different port. Example If PA0 is used in EXTI, it cannot use PB0, PC0, PD0...PZ0 in EXTI.

☐ If GPIO pin under VSW (ie VBAT) power domain goes toward a connector,

GPIO under VSW domain are frequency limited. The maximum frequency is 2 MHz with a maximum load of 30 pF. Only one I/O at a time can be used as GPIO output and these I/Os *must not be used as a current source* (e.g to drive a LED). For theses IOs, the speed value must be kept to (default) 00.

STM32MP**15**: PC13, PC14, PC15, PI8

STM32MP**13**; PC13, PC14, PC15, PI0, PI1, PI2, PI3

2.1.3.3 Unused pin (depends on package)

☐ Pins like VDDxx_unused, VDDA1V8_Unused, VDDA1V2_Unused, NDU, can be left unconnected (opened, floating) on PCB

Note: AN5031 *§ Package compatibility between versions* explains how to put connections to have the option of MP157 be replaced by MP151 or MP153 , this is not mandatory.

Note : AN5031 or AN5474 table 5 summary of how to connect the MP1 supply pins in case of unused features

2.2 Boot pins

☐ Check the external **pull-up** value is max. 1k Ohms on BOOTx pins. Boot pins have internal 10k Ohms pull-down

2.3 Clocks

Refer to Oscillator design guide for ST microcontrollers dedicated application note (AN2867) and electrical characteristics sections in the MP1 datasheet for more details.

2.3.1 HSE

STM32MP1 platform must be used along with a HSE with an accurate/stable crystal or oscillator.
This is required for many purposed (e.g. USB, DDR, etc...). It is not foreseen to use the platform without HSE. The platform (especially SW deliveries) is intended to use HSE. The product is not designed to work with HSI clock, except for some experiments or tests purposes.

☐ Application with LTDC with RGB parallel interface *an external oscillator* (XO) mandatory depending on LTDC signal frequency.

See the ES0438 Limitation with crystal resonator and LTDC.
Design a footprint for an external oscillator in case of issue with crystal/resonator.

☐ When design with external oscillator XO, (HSE in bypass), the clock on OSC_IN input should be stable within 10 ms after the STM32MP1 PWR_ON rising edge occurs (ROM code has got a 10ms time-out on HSE ready) => max set-up time = 10ms for XO or ext. clock generator (ie FPGA)

☐ When design with external oscillator XO , HSE bypass mode must be defined by OSC_OUT connected to GND (digital bypass) or VDD (analog bypass). Connection could be done directly using a copper wire, or a resistor <1kΩ
Note: digital bypass should be used for only for square signal input in full range (CMOS digital level). See datasheet for detailed information ("External clock source characteristics")

☐ STM32MP1 PWR_ON pin can be used to enable/disable external oscillator (XO) (AN5031 § Clock see resistors pull up/down)

☐ When design with HSE crystal, you can provide Data Sheet of proposed crystal and ask to ST support a compatibility sanity check.

2.3.2 LSE

LSE is needed and application operates in low power mode where HSE is switch off, the Low Speed External clock is required to clock the internal Real-time clock (RTC). External oscillator or Crystal/Ceramic component is needed.

It is recommended to use STM32 RTC rather an external RTC. Many customers use internal STM32MP1 RTC.

☐ When design with LSE in bypass, connect External clock source in to OSC32_IN and OSC32_OUT keep floating.

Note: Selected source must have a frequency of up to 1 MHz, Output voltage in CMOS level or analog (amplitude of 200 mV pk-pk minimum) and duty cycle of about 50%.

☐ When design with LSE crystal, connect crystal OSC32_IN and OSC32_OUT together with load capacitors CL1 and CL2.

Note: Total Load Capacitance (parameter of crystal) is calculated as parallel combination of CL1 and CL2 plus parasitic one (pin, traces,…). Parasitic capacitance can be found in range 1.5 – 4 pF typically. .

☐ series or parallel resistor is not recommended in oscillation loop.

☐ When design with LSE crystal, please provide DataSheet of proposed crystal and Load Capacitance parameter (if optional) together with this document for compatibility review

☐ If LSE is not used OSC32_IN should be connected to VSS (with a 0 ohms) for STM32MP13 family

Please leave comments or questions regarding LSE design in case of any doubts.

Click or tap here to enter text.

Please leave comments or questions regarding Specific MP1 connection design in case of any doubts.

Click or tap here to enter text.

2.3.3 Debug

☐ for Linux debug trace/console, prefer **UART4** with TX ->**PG11**, RX-> **PB2** on STM32MP15. TX ->**PD6** and RX ->**PD8** on STM32MP13. This is the default pin muxing of FSBL, SSBL, Kernel.

☐ On MP1 UART_RX pin of the console/debug UART (for traces and commands), an external or internal pull-up is needed. In case of Internal pull on this pin add it in u-boot device tree. (When UART is disconnected If Rx pin is floating, a Null character on received on Uboot console will prevent u-boot from starting the DFU feature (for flash programming)).

☐ When possible, test points or connect LEDs to following GPIO

PA13 for ROM code debugging *AN5031 or AN5474 § Debug triggers and LEDs*

PA14 for the FSBL and SSBL state (please refer article *LED debug scheme* on wiki.st.com)

☐ PA13 and PA14 shouldn't be used during boot phase, e.g. for driving motor as toggling

☐ JTDI must be wired to a connector. When device is reopen for RMA (Return Material Acceptance) , the device is set in RMA state with the RMA pwd entered via JTDI pin.

2.3.4 Tampers

Passive **Level driven** tampers and **active tamper** need a RTC clock , Passive **edge driven** doesn't.

Clock to feed RTC clck can be LSE for *design allowing VBAT mode* Or *LSI* to feed RTC clock for design that not allow VBAT mode but only Standby mode.

☐ if external RTC is present and application intended to have tamper protection in VABT mode design can only use the **level driven passive tampers** (In other configuration there is no clock to control tamper pin)

☐ For design with LSE, LSE CSS monitoring and iTamp3 must be enabled to ensure the RTC clock is functional and to guarantee protection and tamper detection with the active & passive level driven tampers

.

3 Boot Memories

ROMCode options are available after modifying one-time programmable (OTP) memory. For example, ROM code can boot on eMMC from SDMMC2 instead of SDMMC1. However, it is better to use default options to avoid OTP modification, since improper OTP setup can “brick” the device or making it unusable for the layout.

☐ At least one bootable memory must be connected (eMMC, SD card, NAND flash, NOR flash)

Note: The device can also boot from UART or USB interface, this is usually used only for debugging or programming/updating the flash memories.

Please select all memories which are booting from (at least one)

☐ eMMC ☐ SD Card ☐ FMC NAND Flash ☐ QSPI NAND Flash ☐ QSPI NOR Flash

☐ Bootable memory must use compatible pinout with Boot ROM (please check below in the memory-specific section)

Note: ROMcode custom pinout (based on remapping options) is also possible, however it requires changing one-time programmable (OTP) memory.

Note: Boot ROM uses only the minimal subset of the signals/pins for selected memory. Full interface is configured in first stage bootloader and additional pins can be assigned freely without need to modify OTP.

☐ Bootable memory must be powered just after reset at same time as VDD_CORE with proper voltage.

Note: For STPMIC, regulator with Rank > 0 must be used since switched ON/OFF automatically by STMPIC. The option is BUCK3 (rank2), BUCK4(rank2), LDO5(rank2).

Note: Separating power-supply of memories from VDD might be useful to reduce power consumption (memory supply can be switched off).

Note : Memories/interfaces not used during boot process might not need to follow these guidelines

☐ Small resistor in the range of 10-60 Ω, typically 22Ω in series (close to STM32MP1) is recommended for high-speed clock signals (SDMMCx_CK, QSPI_CLK).

Note: Exact value might depend on application

3.1 Boot SD card

☐ Pinout in the below table should be used (unless changed in OTP)

SD card pinout		
PC12	SDMMC1_CK	External 10k pull up or down resistor. Small resistor in series
PD2	SDMMC1_CMD	
PB9	SDMMC1_CDIR	Optional. Will toggle during SD card boot
PC8	SDMMC1_D0	

Note: SDMMC1 used by default by ROM Code. SDMMC2 can be used by programming OTP

☐ When level shifter used, SDMMC1_D0DIR and SDMMC1_D123DIR should have external 10k pull-down resistor.

☐ External 10k pull-up or pull-down must be on SDMMC1_CK signal

☐ Other signals can be without external pull-up/pull-downs

Note: internal pull-ups should be activated in device tree files

☐ When level shifter not used, PB9 will toggle, so user must check if this might disturb the application. If this would be problem, it might be removed by programming OTP.

☐ ESD protection is highly recommended

Note: Otherwise the device could be damaged by ESD when manipulating with SD card.

As ROMCode boot is always done in 'Standard' mode (3 V IOs), if the card is used by the application in USH-I, a power cycle on card supply is required after Reset or Standby.

The SDcard might be used in USH-I mode (1.8V IOs) , After Standby exit or after platform reset the Sd card need to be set back to standard mode (by a power-on cycle) in order the RomCode can boot on it again.

☐ If your application uses USH-I mode (device tree config), check supply of SD card is connected to a power domain that make power-on cycle when STM32MP1 reset .

In default power scheme with PMIC OpenStlinux config SDcard, power supply can be connected to **BUCK4** 3V3 with PMIC1A/B or LDO5 with PMIC1D

Note : **No need to have power on cycle** on SD Card power supply upon STANDBY mode exit when :

-the SDcard power supply remains ON and STM32MP1 in STANDBY mode and its SDMMC peripheral OFF

or

-The SD card is used only in ‘standard’ mode by application

In this case, the ROMcode is able to re-initialize the SDCard with SDCard reset command. This is the case OpenSTlinux configuration with the DK2 design.

(See AN5031 SD Card example for more info)

Please leave comments or questions regarding Boot SD card design in case of any doubts.

Click or tap here to enter text.

3.2 Boot UART

☐ External 10k Ohms Pull-up is required for UARTx TX pin

Note: Avoid signal floating during ensure that PC host side doesn't get garbage characters when ROM code sends its first answer to it.

3.3 Boot eMMC

☐ Default ROM code Pin is in the below table. Should be used (unless changed in OTP)

eMMC pinout		
PE3	SDMMC2_CK	External 10k pull-up resistor. Small resistor in series
PG6	SDMMC2_CMD	External 10k pull-up resistor
PB14	SDMMC2_D0	External 10k pull-up resistor

Note : SDMMC2 used by default by ROM Code. SDMMC1 can be used by programming OTP

☐ Pull-up resistors (internal/external) on D1-D7 data signals *are not required*. For D1-D7 the eMMC standards state device have enabled internal pull-up.

Note: Theses CLK, CMD et DAT0 external pull-up to ensure undesired glitch on eMMC side. Also to avoid current consumption to avoid internal eMMC leakage when MP1 is in standby.

ROM code sends a GO_PRE_IDLE_STATE command (CMD0 + 0xF0F0F0F0F0) at each reboot to reset the eMMC. No need of a power cycle or eMMC upon when MP1 reboot (MP1 NRST event)

Please leave comments or questions regarding Boot eMMC design in case of any doubts.

Click or tap here to enter text.

3.4 Boot QSPI NOR

☐ Pinout in the below table should be used (unless changed in OTP)

QSPI pinout		
PB6 PB2 (MP13)	QUADSPI_BK1_NCS	External 10k pull-up resistor
PF10	QUADSPI_CLK	Small resistor in series
PF8	QUADSPI_BK1_IO0	
PF9	QUADSPI_BK1_IO1	
PH2	QUADSPI_BK2_IO0	Might toggle even if single flash is used
PH3 PG10 (MP13)	QUADSPI_BK2_IO1	Might toggle even if single flash is used

☐ If dual-flash scheme is used for boot, both devices chip-select are tied to PB6/QUADSPI_BK1_NCS

BK2_nCS can remain unused or be used for other functions.

☐ In single flash scheme, ROMCode can drive PH2/PH3 pins during the ROMCode FSBL loading phase (in case of empty/corrupted Flash, single-flash is not auto-detected).

Note: Usage of PH2(PG10) and PH3 could be avoided by programming OTP

(Words 3, 5 and 6) for the 4 pins used in 'single' configuration only.

In order to allow a correct QSPI flash memory re-initialization in case of reboot of the platform e.g. watchdog or STANDBY mode exit, the flash memory need a power cycle to reboot.

For designs where QSPI Flash power supply (VCC) is NOT connected on the VDD power domain

Check the design make a power on reset on the flash memory power supply (VCC) (power cycle) upon reset event.

or

use MP2 NRSTC1MS with the QSPI flash memory #RESET (if present) but ensure #RESET is not directly connected to MP1 NRST (please refer to options in AN5031 or AN5474 §Serial NOR/NAND flash) Otherwise, the MP1 NRST might be pulled low by memory internal protections when memory I/O supply is not present

or

leave memory RESET# is not connected , assuming the memory has an internal power on reset (cf memory Ds) and the MP1 NRST is used to generate a power cycle on flash memory supply (VCC)

The serial flash memory supply (VCC) must be cut for >1ms in order to allow reboot (on reset or standby exit).

☐ During SPI mode boot using SI/SO, some serial memories could use I/O2 and I/O3 pins as an additional feature like HOLD. In order to make this device boot, it might be necessary to set those pins to an inactive level by adding external pull-ups.

Please leave comments or questions regarding Boot QSPI design in case of any doubts.

Click or tap here to enter text.

3.5 Boot FMC NAND flash or QSPI NAND

☐ FMC NAND Pinout in the below table should be used (unless changed in OTP)

FMC NAND pinout		
PG9	FMC_NCE	**External 10k pull-up resistor**
PD12	FMC_ALE	
PD11	FMC_CLE	
PD4	FMC_NOE	
PD5	FMC_NWE	
PD6 /PA9 (MP13)	FMC_NWAIT	Internal pull-up should be active to enhance performance (a little)
PD14-15, PD0-1, PE7-10	FMC_D0 – FMC_D7	
PE11-PE15, PD8/PB8(STMP32MP13) -PD10	FMC_D8 –FMC_D12 FMC_D13-FMC_CD15	Only for 16-bit interface

☒ QSPI NAND Pinout in the below table should be used (unless changed in OTP)

QSPI pinout		
PB6 PB2 (MP13)	QUADSPI_BK1_NCS	External 10k pull-up resistor
PF10	QUADSPI_CLK	Small resistor in series
PF8	QUADSPI_BK1_IO0	
PF9	QUADSPI_BK1_IO1	
PH2	QUADSPI_BK2_IO0	Might toggle even if single flash is used
PH3 PG10 (MP13)	QUADSPI_BK2_IO1	Might toggle even if single flash is used

NAND VCC must be cut for >1ms to allow reboot on reset or Standby exit. With NANDs the erase phase can be long. If during this NAND erase phase a reset happens (NRST with Button or application reset like

IWatch dog) ROM might not start with NAND in this state. Linux OS terminate the erase phase before entering to Standby.

☐ Memory must be supported by ROM code with following parameters (NAND without on-die ECC):

Block size (kB)	Page size (kB)	Data width	ECC bits
128	2	8, 16	4 (bch), 8 (bch), 1 (hamming)
256	4	8, 16	4 (bch), 8 (bch), 1 (hamming)
512	4	8, 16	4 (bch), 8 (bch), 1 (hamming)
512	8	8, 16	4 (bch), 8 (bch), 1 (hamming)

Note: Parameters are read by ROM code according to ONFI standard, if ONFI is not supported parameters must be specified in OTPs

☐ Check memory is not on-die Ecc, Linux does not support this memory

☐ Ensure there is a power on cycle upon NRST when power discrete is used in the design

Please leave comments or questions regarding Boot FMC NAND flash design in case of any doubts.

Click or tap here to enter text.

3.6 Boot USB

☐ Pinout of USB OTG HS PHY must be used (not USB-DM**1**/DP**1** pins)

USB pinout		
USB_DM**2** (dedicated pin)	D- signal	No external resistors
USB_DP**2** (dedicated pin)	D+ signal	No external resistors

☐ Follow general USB guidelines (link to USB section)

☐ HSE frequency must be one of following: 8, 10, 12, 14, 16, 20, 24, 32, 36, 28, 40, or 48 MHz

Note: Autodetection is done by ROMcode, for 25MHz and 26MHz HSE values are supported via OTP modification.

☐ For STM32MP1 OTG_VBUS and OTG_ID pins requirements please refer to USB section below.

Please leave comments or questions regarding Boot USB design in case of any doubts.

Click or tap here to enter text.

3.7 Boot UART

☐ Avoid same UART for BOOT and Trace (for U-boot/TF-A)

Peripheral	Signal	Pin
UART2	RX	PA3
	TX	PA2
UART3	RX	PB12
	TX	PB10
UART4	RX	PB2
	TX	PG11
UART5	RX	PB5
	TX	PB13
UART6	RX	PC7
	TX	PC6
UART7	RX	PF6
	TX	PF7
UART8	RX	PE0
	TX	PE1

Please leave comments or questions regarding Boot UART design in case of any doubts.

Click or tap here to enter text.

4 Tampers

Passive Level driven tampers and active tamper need a RTC clock , Passive edge driven doesn't.

can be LSE to feed RTC clck for design allowing VBAT mode.

☐ if external RTC is present and application intended to have tamper protection in VABT mode design can only use the level driven passive tampers

☐ For design with LSE is needed for the active & passive level driven tampers, the LSE CSS monitoring and iTamp3 must be enabled to ensure the RTC clock is functional.

☐ If design does not have LSE, no active tamper can be used , only a Passive edge tamper

(LSI in VDD domain is OFF in VBAT mode, LSI should not be RTC source otherwise time is frozen)

5 DDR memory

☐ Pull-down resistor 240 Ohm 1% must be connected to DDR_ZQ of MPU side and ZQ on DDR side.

Note: This resistor must not be shared with ZQ resistors required on each DDR3/DDR3L components.

☐ CLK_N/CLK_P signals must be connected using one **100 Ω resistor** close to DRAM memory **after** the DRAM balls (chained connection) to implement a differential termination.

☐ Pull-down resistor 10 kΩ is required on DDR_CKE line

☐ Pull-down resistor 10 kΩ is required on DDR_RESETN line

☐ DR_DTO0 , DDR_DTO1 and ATO pin can be left unconnected (for ST test purpose).

☐ DDR_ODT must connected to GND for LPDDR3 on both sides (memory and MP1 DDRPHY)

☐ Check undesired signals swap between both MP1 and DRAM sides on signals for **DQx, DQSx, DQMx, CLK/CLK#** For example on DDR3L check on MP1 DDR_DQM0/DDR_DQM1 are really connected to DRAM DDR_DMU/DDR_UDL (and not to DDR_DML/DDR_DMU)

☐ 100nF decoupling to VSS on each MP1 DDR_VREF pin and DRAM VREFCA/VREFDQ pins

☐ In design where VREF generated 1K ohm/100nF divider on VDD_DDR, 2 of them should be locally present on MP1 VREF pin and DRAM VREF pin.

Note: *DQx lines swap* within each byte (byte 0 specifically of interest) is not permitted for *LPDDR2/3* whereas allowed in DDR3/3L.

More info AN5122 or AN5692 DDR memory routing guidelines

Please leave comments or questions regarding DDR memory design in case of any doubts.

Click or tap here to enter text.

6 USB

☐ ST32MP1 USB_RREF pin must be populated with 3k Ohms 1% resistor connected to GND.

When USB *is not used*, as USB PHY is supplied by VDDA1V8 REG, it is safer to keep the 3 k Ohm Pull-Down Resistor on USB_RREF pin.

☐ If multiple USB Host ports are used, minimum 120uF low-ESR capacitance should be connected to VBUS on each port. This is not needed for single port or OTG/Dual-role application.

Note: This is specified by USB2.0 specification. This is to keep voltage level stable when connected new unpowered device. Otherwise in-rush current flowing to new device might cause voltage drop on all other connected devices.

☐ On USB bus powered application, on **OTG_VBUS pin**, the total bypassed capacitance on the line should not exceed 10µF to limit the inrush current to follow USB compliances.

Note: Due to fast regulator response the total bypassed capacitance is typically higher than 100uF, then the USB device must incorporate some form of VBUS surge current limiting.

☐ **For USB bus powered application (VBUS on connector supplies application), STM32MP1 OTG_VBUS pin should be left uconnected** *on VBUS* type AB receptacle. Instead GPIO pin **via *discrete resistor voltage divider*** *on VBUS* type AB receptacle because when **VDD=0V** (STM32MP1 in Vbat mode) STMP32MP1 **cannot support 6V on OTG_VBUS** pin.

AN4879 recommended resistor divider values for VBUS detection with the following values:
Assumed resistor values are assessed allowing for a +/- 0.1% variation.
For VDD in range 3.0-3.6 V : 68 kohms (to GND); 82 kohms (to VBUS)
For VDD in range 1.8-2.0 V : 82 kohms (to GND); 33 kohms (to VBUS)"

Same for OTG_ID pin should be let un-connected, a GPIO pin should be used to resistor voltage divider too.

Note: Customers could connect VBUS on PMIC VBUSOTG pin instead of using voltage divider. The PMIC PWR_USB_SW has been designed (in addition to be a power switch) to detect VBUS. It is OTG compliant regarding VBUS valid voltage thresholds ***BUT* this is *not supported* by OpenSTLinux BSP software**, customer has to make its own implementation.

☐ The use of the ST32MP1 OTG_VBUS pin may prevent USB certification in some cases. See AN5474 8.12

☐ STM32MP1 **OTG_VBUS pin** is required by Uboot DFU for external flash programming (eMMC,SDcard…), and by Linux USB OTG driver (but mandatory not for the ROM code),

OTG_VBUS pin must be connected to type B receptacle for USB in device mode or to AB receptacle for USB in Dual-role mode (device or host). With USB-TypeC receptacle, STM32MP1 OTG_VBUS pin sensing is not needed and must be deactivated.

When USB OTG is only used for Uboot DFU (USB OTG in device mode only) to program the flash,

the **OTG_VBUS pin can be let unconnected**. In this case Uboot *device tree configuration* **is needed** to disable VBUS sensing. See wiki article "How_to_configure_U-Boot_for_your_board#USB_OTG_node"

☐ STM32MP1 **OTG_ID pin** for OTG Dual-Role(DR), must be connected to typeAB receptacle, with USB-TypeC receptacle, OTG_ID pin is not needed and must be deactivated

Note: same note as for OTG_VBUS , If USB is only used for Uboot DFU for external flash programming, **OTG_ID pin can be left unconnected**. Follow Uboot *device tree config* in wiki article "How_to_configure_U-Boot_for_your_board#USB_OTG_node"

☐ If using TypeC and no controller used, 5.1kOhms pull-downs should be populated on CC lines.

Note: Please see AN5260 and AN5225 for more information and more complex designs.

☐ ESD and common-mode filter should be placed close to connector for high-speed, for full-speed only the ESD is needed (Combined ESD+EMI filter is recommended: reference ECMF02-4CMX8)

Note: Protection is not needed between MP1 and on-board USB hub component

☐ It is not needed to add resistors on the DP/DM lines.

☐ Common mode choke on the DP/DM line could degrade signal integrity so when customer do not face EMI issue it's not best option to add "in advance"

☐ When USB is not used

Leave VDD3V3_USB (HS/FS) pins unconnected or to VSS

Leave VDDA1V1 _REG pin unconnected without the decoupling capacitor, if DSI not used leave VDDA1V8_REG pin unconnected without the decoupling capacitor

Please leave comments or questions regarding USB design in case of any doubts.

Click or tap here to enter text.

7 Ethernet

Please follow recommended schematic in Ethernet PHY Data Sheet or check examples in AN5031

Note: Due to various type on Ethernet PHY market we cannot cover unique requirements each of them.

☐ pull-up/pull-down configuration for the selected PHY. This configures e.g. PHY address or selected interface (MII/RMII). This depends on selected PHY. *To be check by customer.*

☐ PHY requires precise system clock provided by an external Crystal/resonator. Alternatively, this system clock can be feed by STMP32MP1. 25/50/125MHz clock from PA1, PB5 or PG8.

Note: Only possible if PHY allows it and if RCC can provide a precise 25/50/125 MHz clock (depending on HSE selection and RCC settings). Also, not possible to wake-up on line (WOL) from GMAC when in low-power Standby mode. WOL from PHY interrupt connected to WKUP pin is an alternative in this case.

☐ Series resistors in range of 10-60 Ohms should be placed as close as possible of the output driver pins (Clock, TX, RX) To keep good signal integrity and avoid EMEI issue.

☐ Magnetics ratio depends on the selected PHY. This should be specified in PHY datasheet.

☐ Signals from RJ45 connector should be isolated from the rest of the board (except for LEDs). Shielding must not be connected to board ground.

☐ NRST of PHY is optional. It can be connected to a pull-up, or to GPIO if independent reset is needed by the PHY Linux driver.

☐ ESD protection is recommended to be placed between PHY and magnetics or RJ45 connector (if magnetics inside). ESD should be placed close to magnetics. Reference USBLC 6-4SC6 or 2 x HSP051- 4M10 for Gigabit PHY.

Note: Typical PHY does not embedded ESD protection.

☐ PHY interrupt can be connected to STM32MP1 wake-up pin to allow remote wake-up WOL (optional)

Please leave comments or questions regarding Ethernet design in case of any doubts.

Click or tap here to enter text.

8 DSI

☐ VDDA1V8_DSI must be connected VDDA1V8_REG with the decoupling capacitors

☐ VDDA1V2_DSI_PHY must be connected VDDA1V2_DSI_REG with the decoupling capacitors

☐ All DSI differential signals must have 100Ω differential trace impedance

☐ ESD and common-mode filter should be placed close to connector.

2x ECMF04-4HSWM10 as reference

☐ When DSI is not used

Leave DSI D0N/P D1N/P CKN/P pins unconnected
Leave VDDA1V8_DSI, VDDA1V2_DSI_PHY pin unconnected

Leave VDDA1V2_DSI_REG unconnected if USB not used leave also VDDA1V8_REG unconnected

☐ For compatibility between STM32MP151 and STM32MP157 in case STM32MP151 is not available and STM32MP157 is available

VDDA1V8_DSI connected VDDA1V8_REG with the decoupling capacitors
VDDA1V2_DSI connected VDDA1V2_DSI_REG with the decoupling capacitors
VDD_DSI connected to VDD
See AN5031 5.3 Package compatibility between versions

Please leave comments or questions regarding DSI design in case of any doubts.

Click or tap here to enter text.

9 SDMMC/eMMC

☒ Check the power domains of the pins when memory 1.8 IO (resp 3.3V) and VDD 3.3V (resp 1.8V)

STM32MP13x VDDSD1 powered pins can be used for SDMMC1 CLK+CMD+D0/1/2/3, but not for D4/5/6/7; the same, STM32MP13x VDDSD2 powered pins can be used for SDMMC2 CLK+CMD+D0/1/2/3, but not for D4/5/6/7.
So if D4/5/6/7 are connected directly between eMMC and MP13x, MP13x VDD and VDDSD1 or VDDSD2 should be the same level.

For High speed with IO at 1.8V, a possible workaround is using bi-direction level-shifter (for example : TI LSF0204-Q1) for D4/5/6/7 signals between eMMC and MP13x.

If lower performance is acceptable, 4-data-line modes can be used: in such case, MP13x VDD and VDDSD1/2 can be independent, and VDDSD1/2 can be 3.3V or 1.8V as needed.

10 Design Sanity Check List – General Recommendation

10.1 STPMIC

- Different power tree architectures possible for an application
  - With PMIC with VDD=V3.3 or with VDD=1.8 in AN5031 and in AN5260 *battery supplied application*
  - Without PMIC with discrete power supplies in AN5256
- For 3.3V VIN application, reprogram PMIC NVM with:
  - STPMIC1B.VINOK_Rise = 3.1V (else product never start)
  - STPMIC1B.VINOK_Hyst = 200mV (to respect VIN minimum value 2.8V)

  (else not enough time between VINOK_fall and VIN_POR_fall to initiate power-down sequence)

  See PMIC DS table *Electrical and timing parameters*

  Warning: NVM write operation require VIN>3.8V (cf DS) so a bench with VIN=3.8V is needed to reprogram NVM
- The set of PMIC external components in the data sheet is already at a certain level of size optimization. This BOM has been carefully validated by ST and aim to sustain longevity and good operation condition
- Some design request to wakeup STPMIC via PONKEY. PONKEY is active low with internal pull-up whereas WAKEUP active high with internal pull-down.

In case customer want to use other reference part number than BOM in DS:

- For the inductors at the output of the BUCKS customer can use a smaller one that is high-quality that ST validated. The reference for inductor is the Murata DFE201612P-1R0M=P2. There are other less expensive ones but ST have not tested them. Not a good idea to use them.

- Regarding the BUCK capacitors, we need to be careful especially at the BUCK inputs where switch noise is the most important.
- If you want to take other BUCK capacitor references keep the same size as PMIC BOM because the track still needs to be big enough for the return current.
- Ensure that at the voltage the capacitor operates, the effective capacitance is equivalent to the capacitor of part number in the PMIC BOM. The effective capacitance depends on the rated voltage&size and the operating voltage. We need to consider derating capacitor value in regard to DC-bias, rating voltage, temperature, dielectric or package.
- For the all other capacitors the same precautions have to be taken.
- Use low ESR capacitor like MLCC capacitors.

10.2 STM32MP1 decoupling

No ferrite bead is needed between VDDA power domain and STM32MP1 VDDA pin when supply from dedicated LDO regulator

- However, ferrite can be placed between VDD and VDDA when VDDA is derived from same supply (e.g. as on DK2)

STM32MP1 VDDA is required for ADC/DAC/VREFINT operation.

10.3 DDR memory

- Design with a single DDR3/3L x16 is used, VTT_DDR, additional line termination and capacitor could *be avoided* on A/C lines (point-to-point). Similarly in this case, the series resistors 33ohm on A/C lines *are not needed*.
- Design can foresee 2x16 bits DDR devices in fly-by topology and board produced with only one populated. The termination resistors are in the end of the PCB lines, no issue to depopulating the device which is close to the termination resistor (the one connected to byte2 and byte3 in figure 1 of AN5122).
- Detailed routing rules are described in STM32MP1 Series DDR memory routing guidelines application note (AN5122)
- Layout example for Altium Designer with STM32MP1/DDRL3/LPDDR/STMPIC can be found on st.com web. See the zip file under 'Gerber files' : https://www.st.com/en/microcontrollers-microprocessors/STM32MP17.html#resource
  Signal integrity test on DDR-STM32MP1 track have been done on these layout examples.

10.4 Boot device

- Foresee a serial interface (UART or USB) in case of memory boot device failure

10.5 Debug

Connector STDC14 is recommended to connect serial console and debug interface (UART4 and JTAG) with STlinkV3.

- If available, it is recommended to connect the debugger probe system reset pin to NRST. (This permits to reset the application from the debugger)
- In order to use the RMA (return material acceptance) the JTAG pins (JTDI, JTCK, JTMS) must be accessible

  Please follow chapter in AN5031 /AN5474 *Debug port and UART connection with STDC14 connector*
  Reference example for STDC14 header is FTSH-107-01-L-DV-K-A

10.6 USB

- For PCB routing avoid any stubs/derivation on USB-HS DM/DP signals (signals 480MHz)
- USB HS routing rules: D + / D- tracks with 90R controlled impedance (ground plane below) no 90° angles and avoid vias or test points on the tracks (breaks bus impedance).
  - If design absolutely needs to put test points: put them as close as possible to the connector where the tracks separate because the difference between the 2 pins of the connector is greater than the ISO between the 2 tracks)

- STM32MP1 does not support USB Bus powered device USB logo certification due to power/time needed to boot Linux which cannot fit USB rules. This does not avoid the system to work.

10.7 ADC

- ANA0 and ANA1 pins are recommended (if available) for best ADC performance. Those pins are connected directly to ADC.
- Ensure the high-speed signals are far from ADC_IN pins.
    - Some induced noise (e.g. 125MHz from Ethernet) may occur on ADC analog input (which is high-impedance).

10.8 USB OTG serial link

- For minimal and closed designs (without Ethernet, SD card) with only UART4, it's possible to this UART for debug/console link, for flash-loading with STM32CubeProgrammer, for DDR tuning.
    - 1Gbit de flash (128MBytes) at 115200bits/s (~11kBytes/s), is very slow, **takes 3 hours.**
- Really Prefer to keep in the design USB OTG serial link for DFU flash loading with STM32CubeProgrammer with test pins only (no USB connector for smaller design). USB OTG in device mode is very convenient for development phase. Can be to update some in partitions or some files in partitions. "dd" command with Uboot setting the MP1 flash storage seen as a USB mass storage or "scp" command with Linux Ethernet over USB gadget feature to update files in rootfs,userfs,etc or extract file from target.

  USB-OTG as device only does not imply many additional components, the design involves:
    - OTG_HS_DM2/DP2 pin connected to a type B receptacle or to test pins
    - OTG_ID pin can be left unconnected
    - OTG_VBUS pin can be unconnected (need special Uboot Device tree setting see USB rules above)
    - USB_RREF 240 1% pull down
    - VDD3V3_USB (HS, FS) must be supplied with 1uF decoupling capacitor
    - When VDDA1V8_REG is by-passed (cases VDD<2.25v), VDD3V3_USB must be supplied in order after VDD Note: This is the case when design follows the default PMIC power scheme: VDD3V3_USB=LDO4 (rank3) powered after VDD & VDDA1V8_REG =BUCK3 (rank1)

10.9 Ethernet

- When STM32MP1 provides the clock on PHY on ETH_CLK pad ,

  a precision of 25ppm is fine for HSE source is an oscillator. As HSE source is an oscillator the precision is not affected by STMP32 noise. Some jitter might be added inside the STM32MP1 circuitry. HSE must be set in digital bypass, PLL should have high VCO frequency to minimize jitter, FRAC-N should be avoided if possible, but as there is PLLs inside the PHY, this is usually not a big issue (150 - 200ps p-p jitter is accepted).

  ST uses crystal clock source on PHY because those board are for evaluations purposes, and by having separate crystal for Ethernet PHY, we have less constrains on the clock tree choice (as written in AN5031, the 50MHz on ETH_CLK constrain one PLL frequency to a multiple of 50MHz). We tested both ETH_CLK 25MHz and 50MHz with respectively RGMII PHY and RMII PHY.

10.10 STM32MP1 Unused pins

Can be left unconnected see AN5031 or AN7554 for M13 for pin and supplies.

10.11 EMC/EMI

- Any high-speed clock signals (QSPI, eMCC, ETH, SDIO,..) are recommended to populate with series resistor in range 10 - 60 ohm to avoid EMI issue.
- ESD protection is highly recommended for all accessible human-interface (SD card, USB, HDMI?)

NOTE: Otherwise the device could be damaged by ESD when manipulating with SD card, cables.

Recommended ST protection is ECMF02-4CMX8 (used on EVAL motherboard), which contains ESD and EMI common filter in single device.

- It is recommended to use fly-by topology even for single DDR3/DDR3L chip. It reaches better EMI performance.

10.12 STM32MP1 supplies power up sequence order (discrete power supplies)

- VDD must be powered first before VDD_CORE, VDD_CPU and the others VDD
- During power-up and power-down phases, the following MP1 DS *Power sequence requirements* must be respected:
  - When VDD is below 1 V, other power supplies (VDDCORE, VDDA, VDDA1V8_REG, VDDA1V8_DSI, VDDA1V1_REG, VDD3V3_USBHS/FS, VDDQ_DDR) must remain below VDD + 300 mV.
  - When VDD is above 1 V, all power supplies are independent.
  - During the power-down phase, VDD can temporarily become lower than other supplies only if the energy provided to the STM32MP1 device remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power- down transient phase
- Memory Boot device supplies are switched ON at the same time as VDD_CORE

10.13 STM32MP1 800Mhz

- 800MHz sale-types are pin to pin compatible with non-800MHz sale-types
- Higher voltage is required for VDD_CORE domain. This can be changed dynamically when PMIC is used (no HW changed required)
- With discrete power supply, change in VDD_CORE regulator might be necessary

10.14 All documents for Design

https://community.st.com/s/article/FAQ-STM32MP1-What-ST-offers-to-make-a-PCB-design-that-ensures-signal-integrity

https://community.st.com/s/article/FAQ-STM32MP1-what-alternative-to-STPMIC-for-application-supply

https://community.st.com/s/article/FAQ-STM32MP1-different-power-distribution-for-your-application

https://community.st.com/s/article/FAQ-STM32MP1-low-power-management-documentation

https://community.st.com/s/article/FAQ-STM32MP1-Bring-up-procedure

https://community.st.com/s/article/FAQ-STM32MP1-bring-up-troubleshooting-guide