

This seminar on Friday 16 March 2018, it's about Cortex-M deice. Arm Cortex-M processors have the programmer model that the processor family many cores are developed over the years. Separate to 3 major type application processor, real-time processor, and microcontroller processor. Arm Cortex-M has 5 different model, Cortex-M0 the lowest size (9nm), Cortex-M0+ the highest energy efficiency, Cortex-M3 energy balancing, Cortex-M4 blended MCU and Digital signal processing, and Cortex-M7 the highest performance. The Cortex-M are serving for all application such as energy grid, automotive, smart city, sensor, farming, industrial, smart lighting, retail, healthcare, and etc.

Armv6-M(Cortex-M0/0+) are efficient instruction set for simple application cause they are ultra low power and not full optimized(fewer memory) and it's ideal for 8/16 bits(ultra low design).

Armv7-M are powerful instruction set. For example Cortex-M3 is very capable for many applications such as high performance, low power, rich debug, and trace features

Armv8-M brings trustZone to the cortex-M family (Cortex-M23/33)

They chosen by leading MCU suppliers such as NXP, Toshiba, Microchip, Nuvoton, etc. Their design start by the fastest route to silicon such as Fast, simple, and no risk-access, design with confidence.

The next topic is about baseline of programmer model. First register banks they have 16 banks(R0 to R15). R13 is stack pointer, R14 is link register, and R15 is program counter. They also have special register for "program register status" and "CONTROL" (M3/M4 have additional register). They also defined memory map of Cortex-M; 4GB linear memory space; Standard across to all Cortex-M implementations; Optional protection unit; Support both 32/64 bits except Cortex-M0/0+ 32 bits only.

System Timer or SysTick is a flexible timer because it is 24 bits self-reloading counter. It will reload when count equal 0, and also reloading register.

What is CMSIS?

A vendor independent standard for silicon partner, tool vendors and end users. Establishes a software foundation.

Nested vector interrupt controller (NVIC) consist of 5 properties. First, support multi sources. Second, vectored interrupt/exception service. Third, stack exception handling. Forth, automatic nested IQR handling. And fifth, each interrupt has a programmable priority level (priority level register are 8 bits, with 2 bits implemented for Armv6-M or 3-8 bits implemented for Armv7-M, and high priority IQR can pre-empt a lower priority IQR.)

Debug and Trace

- Debug
 - Multicore debug support
 - Memory access while the processor is running
- Trace
 - Program trace with ETM on Cortex-M3/4/7
 - Low cost program trace with MTB on Cortex-M0/0+

CMSIS5

Consistent software framework for Arm Cortex-M and Cortex-A5/7/9 based systems

Has own software pack to communicate with microcontroller .

CMSIS-DSP library

collection of 61 algorithm for basic math, filtering, matrix

CMSIS-RTOS implementation

CMSIS-NN: Optimum ML performance on Arm

MDK-Middleware

enable user to develop faster

Device support

support for 5000+ devices family packs