

1. Description

1.1. Project

Project Name	Dashboard_V2
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	10/05/2022

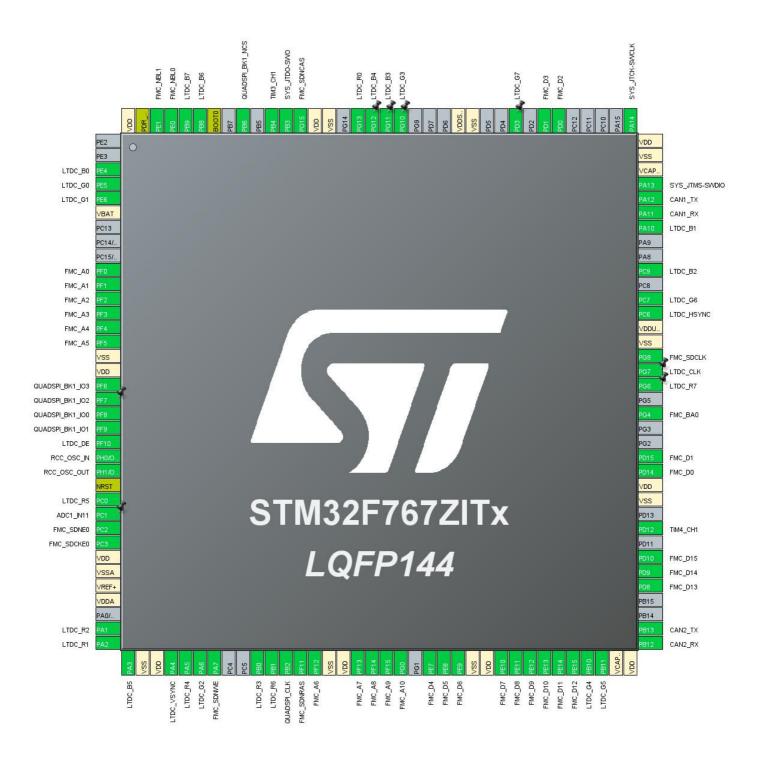
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



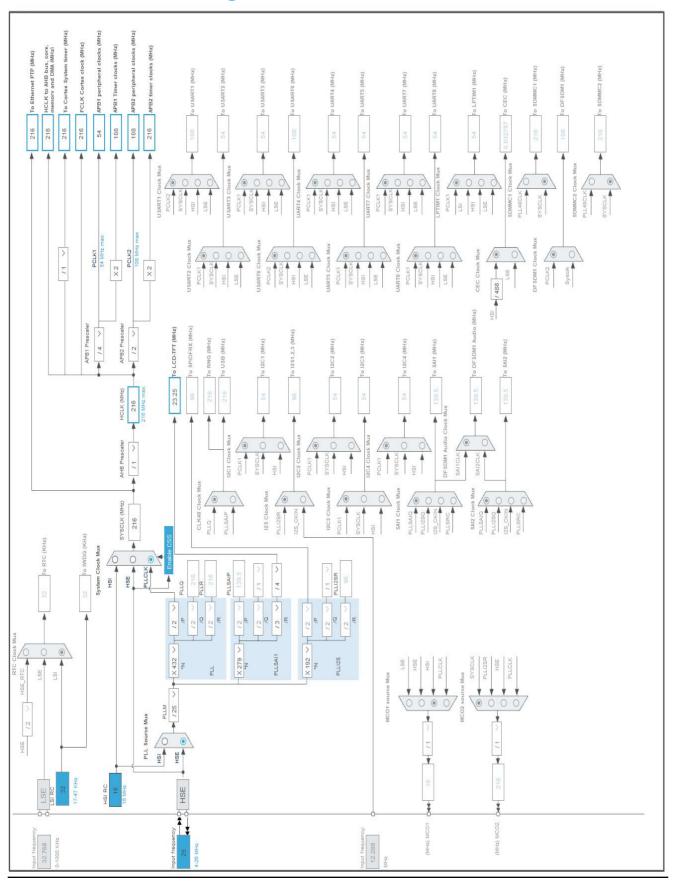
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after reset)		Function(s)	
3	PE4	I/O	LTDC_B0	
4	PE5	I/O	LTDC_G0	
5	PE6	I/O	LTDC_G1	
6	VBAT	Power		
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	QUADSPI_BK1_IO3	
19	PF7	I/O	QUADSPI_BK1_IO2	
20	PF8	I/O	QUADSPI_BK1_IO0	
21	PF9	I/O	QUADSPI_BK1_IO1	
22	PF10	I/O	LTDC_DE	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	LTDC_R5	
27	PC1	I/O	ADC1_IN11	
28	PC2	I/O	FMC_SDNE0	
29	PC3	I/O	FMC_SDCKE0	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1	I/O	LTDC_R2	
36	PA2	I/O	LTDC_R1	
37	PA3	I/O	LTDC_B5	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	LTDC_VSYNC	
41	PA5	I/O	LTDC_R4	
42	PA6	I/O	LTDC_G2	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
43	PA7	I/O	FMC_SDNWE	
46	PB0	I/O	LTDC_R3	
47	PB1	I/O	LTDC_R6	
48	PB2	I/O	QUADSPI_CLK	
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power	1 WO_//O	
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power	o_50	
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	LTDC_G4	
70	PB11	I/O	LTDC_G5	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	CAN2_RX	
74	PB13	I/O	CAN2_TX	
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
81	PD12	I/O	TIM4_CH1	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
89	PG4	I/O	FMC_BA0	
91	PG6	I/O	LTDC_R7	

Pin Number LQFP144	Pin Name (function after	Pin Type	Alternate Function(s)	Label
	reset)			
92	PG7	I/O	LTDC_CLK	
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	LTDC_HSYNC	
97	PC7	I/O	LTDC_G6	
99	PC9	I/O	LTDC_B2	
102	PA10	I/O	LTDC_B1	
103	PA11	I/O	CAN1_RX	
104	PA12	I/O	CAN1_TX	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
117	PD3	I/O	LTDC_G7	
120	VSS	Power		
121	VDDSDMMC	Power		
125	PG10	I/O	LTDC_G3	
126	PG11	I/O	LTDC_B3	
127	PG12	I/O	LTDC_B4	
128	PG13	I/O	LTDC_R0	
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
133	PB3	I/O	SYS_JTDO-SWO	
134	PB4	I/O	TIM3_CH1	
136	PB6	I/O	QUADSPI_BK1_NCS	
138	воото	Boot		
139	PB8	I/O	LTDC_B6	
140	PB9	I/O	LTDC_B7	
141	PE0	I/O	FMC_NBL0	
142	PE1	I/O	FMC_NBL1	
143	PDR_ON	Reset		
144	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Dashboard_V2
Project Folder	F:\Marcin\Documents\Studia\PGRacing\PGRacingElectronics\Dashboard\Code\D
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_CRC_Init	CRC
4	MX_DMA2D_Init	DMA2D
5	MX_LTDC_Init	LTDC
6	MX_ADC1_Init	ADC1
7	MX_CAN1_Init	CAN1
8	MX_CAN2_Init	CAN2
9	MX_FMC_Init	FMC
10	MX_JPEG_Init	JPEG
11	MX_QUADSPI_Init	QUADSPI

Rank	Function Name	Peripheral Instance Name
12	MX_TIM3_Init	TIM3
13	MX_TIM4_Init	TIM4
14	MX_DMA_Init	DMA
15	MX_TIM8_Init	TIM8
17	MX_TouchGFX_Init	STMicroelectronics.X-CUBE-TOUCHGFX.4.20.0
18	MX_TouchGFX_Process	STMicroelectronics.X-CUBE-TOUCHGFX.4.20.0

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	DS11532_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

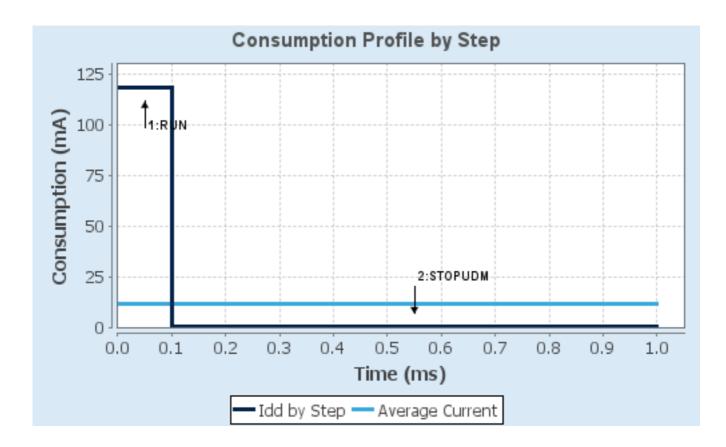
6.4. Sequence

04-22	014	01 0
Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	89.42	104.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005
			DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN11

mode: Temperature Sensor Channel

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Enabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 2 *

External Trigger Conversion Source Timer 8 Trigger Out event *

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 11
Sampling Time 480 Cycles *

<u>Rank</u> 2 *

Channel Temperature Sensor *

Sampling Time 480 Cycles *

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. CAN1

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 9 *

Time Quantum 166.6666666666666 *

Time Quanta in Bit Segment 1 2 Times *
Time Quanta in Bit Segment 2 3 Times *

Time for one Bit 1000

Baud Rate 999999 *

ReSynchronization Jump Width 2 Times *

Basic Parameters:

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Automatic Retransmission

Enable *

Receive Fifo Locked Mode

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

7.3. CAN2

mode: Activated

7.3.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 9 *

Time Quanta in Bit Segment 1 2 Times *

Time Quanta in Bit Segment 2 3 Times *

Time for one Bit 1000

Baud Rate 999999 *

ReSynchronization Jump Width 2 Times *

Basic Parameters:

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Disable

Automatic Retransmission

Enable *

Receive Fifo Locked Mode

Disable

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

7.4. CRC

mode: Activated

7.4.1. Parameter Settings:

Basic Parameters:

Default Polynomial State Enable

Default Init Value State Enable

Advanced Parameters:

Input Data Inversion Mode None
Output Data Inversion Mode Disable
Input Data Format Bytes

7.5. DMA2D

mode: Activated

7.5.1. Parameter Settings:

Basic Parameters:

Transfer Mode Memory to Memory
Color Mode RGB888 *

Output Offset 0

Foreground layer Configuration:

DMA2D Input Color Mode RGB888

DMA2D ALPHA MODE

No modification of the alpha channel value

Input Alpha 0
Input Offset 0

DMA2D ALPHA Inversion Regular Alpha

DMA2D Red and Blue swap Regular mode (RGB or ARGB)

7.6. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 2 banks

Address: 11 bits Data: 16 bits Byte enable: set 7.6.1. SDRAM 1:

SDRAM control:

Bank SDRAM bank 1

Number of column address bits 8 bits
Number of row address bits 11 bits

CAS latency 2 memory clock cycles *

Write protection Disabled

SDRAM common clock 2 HCLK clock cycles *

SDRAM common burst read Enabled *

SDRAM common read pipe delay 0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay 2 *

Exit self-refresh delay 7 *

Self-refresh time 4 *

SDRAM common row cycle delay 6 *

Write recovery time 3 *

SDRAM common row precharge delay 2 *

Row to column delay 2 *

7.7. JPEG

mode: Activated

7.7.1. Parameter Settings:

Version:

JPEG version jpeg1_v1_0

JPEG Software options:

ENCODE Enabled
DECODE Enabled

RGB_FORMAT JPEG_ARGB8888

JPEG_SWAP_RG 0

7.8. LTDC

Display Type: RGB888 (24 bits)

7.8.1. Parameter Settings:

Horizontal Synchronization Width	4 *
Horizontal Back Porch	8 *
Active Width	800 *
Horizontal Front Porch	8 *
HSync Width	3
Accumulated Horizontal Back Porch Width	11
Accumulated Active Width	811
Total Width	819

Synchronization for Height:

Vertical Synchronization Height	40 *
Vertical Back Porch	8 *
Active Height	480
Vertical Front Porch	8 *
VSync Height	39
Accumulated Vertical Back Porch Height	47
Accumulated Active Height	527
Total Height	535

Signal Polarity:

Horizontal Synchronization Polarity

Vertical Synchronization Polarity

Data Enable Polarity

Pixel Clock Polarity

Active Low

Normal Input

BackGround Color:

 Red
 0

 Green
 0

 Blue
 0

7.8.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Number of Layers:

Number of Layers 1 layer *

Windows Position:

Layer 0 - Window Horizontal Start 0

Layer 0 - Window Horizontal Stop 800 *

Layer 0 - Window Vertical Start 0

Layer 0 - Window Vertical Stop 480 *

Pixel Parameters:

Layer 0 - Pixel Format ARGB8888

Blending:

Layer 0 - Alpha constant for blending 255 *

Layer 0 - Default Alpha value 0

Layer 0 - Blending Factor1 Alpha constant
Layer 0 - Blending Factor2 Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress 0xC0000000 *

Layer 0 - Color Frame Buffer Line Length (Image **800 **

Width)

Layer 0 - Color Frame Buffer Number of Lines (Image 480 *

Height)

7.9. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.9.1. Parameter Settings:

General Parameters:

Clock Prescaler 3 *

Fifo Threshold 1

Sample Shifting Half Cycle *

Flash Size 23 *

Chip Select High Time 6 Cycles *

Clock Mode Low
Flash ID Flash ID 1

Dual Flash Disabled

7.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.10.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Over Drive Enabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.11. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM6

7.12. TIM3

Clock Source : Internal Clock
Channel1: PWM Generation CH1

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 134 *
Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable
CH Polarity High

7.13. TIM4

Clock Source: Internal Clock
Channel1: PWM Generation CH1

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 215 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.14. TIM8

Clock Source: Internal Clock

Channel1: PWM Generation No Output

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 216-1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 5000-1 *
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 16 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

BRK Sources Configuration

- Digital Input- DFSDMDisable

Break And Dead Time management - BRK2 Configuration:

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

BRK2 Sources Configuration

- Digital Input- DFSDMDisable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

7.15. FREERTOS

Interface: CMSIS_V2

7.15.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.2.1 CMSIS-RTOS version 2.00

MPU/FPU:

ENABLE_MPU Disabled
ENABLE_FPU Disabled

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000 56 MAX_PRIORITIES MINIMAL_STACK_SIZE 128 MAX_TASK_NAME_LEN 16 USE_16_BIT_TICKS Disabled IDLE_SHOULD_YIELD Enabled USE_MUTEXES Enabled Enabled USE_RECURSIVE_MUTEXES USE_COUNTING_SEMAPHORES Enabled QUEUE_REGISTRY_SIZE USE_APPLICATION_TASK_TAG Disabled ENABLE_BACKWARD_COMPATIBILITY Enabled USE_PORT_OPTIMISED_TASK_SELECTION Disabled USE_TICKLESS_IDLE Disabled USE_TASK_NOTIFICATIONS Enabled

Memory management settings:

RECORD_STACK_HIGH_ADDRESS

Memory Allocation Dynamic / Static
TOTAL_HEAP_SIZE 204800 *

Memory Management scheme heap_4

Disabled

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Enabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled
MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled

TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10
TIMER_TASK_STACK_DEPTH 256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE size_t
USE_POSIX_ERRNO Disabled

7.15.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled vTaskDelete Enabled vTaskCleanUpResources Disabled Enabled vTaskSuspend Enabled vTaskDelayUntil vTaskDelay Enabled Enabled xTaskGetSchedulerState Enabled xTaskResumeFromISR xQueueGetMutexHolder Enabled Disabled xSemaphoreGetMutexHolder Disabled pcTaskGetTaskName Enabled uxTaskGetStackHighWaterMark Disabled xTaskGetCurrentTaskHandle Enabled eTaskGetState xEventGroupSetBitFromISR Disabled Enabled xTimerPendFunctionCall Disabled xTaskAbortDelay Disabled xTaskGetHandle Disabled uxTaskGetStackHighWaterMark2

7.15.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Disabled

Project settings (see parameter description first):

Use FW pack heap file Enabled

0xC0000000 *

7.16. STMicroelectronics.X-CUBE-TOUCHGFX.4.20.0 mode: GraphicsJjApplication

7.16.1. TouchGFX Generator:

Display:

Interface Parallel RGB (LTDC) *
Framebuffer Pixel Format (LTDC) ARGB8888
Width (LTDC) 800
Height (LTDC) 480
Framebuffer Strategy Single Buffer
Buffer Location By Address *

Start Address

Driver:

Application Tick Source

DMA2D Accelerator (ChromART)

Real-Time Operating System

LTDC *

Enabled *

CMSIS_RTOS_V2

Video Decoding:

Type Hardware *

Concurrent videos 1

Strategy Single buffer
Buffer Width 0
Buffer Height 0

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
CAN1	PA11	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA12	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
CAN2	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB13	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA7	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
LIBO	PE5	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF10	LTDC_OT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC0	LTDC_BE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA5	LTDC_V3TNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10					
		LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	LTDC_B2	Alternate Function Push Pull Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	LTDC_B1		No pull-up and no pull-down	Low	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG13	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
OUADOS	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PF6	QUADSPI_BK1_I O3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF7	QUADSPI_BK1_I O2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF8	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF9	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB6	QUADSPI_BK1_ NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PH0/OSC_I	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM3_CH1/TRIG	DMA1_Stream4	Peripheral To Memory	Low
TIM4_CH1	DMA1_Stream0	Peripheral To Memory	Low

TIM3_CH1/TRIG: DMA1_Stream4 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

TIM4_CH1: DMA1_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream4 global interrupt	true	5	0
ADC1, ADC2 and ADC3 global interrupts	true	5	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	15	0
LTDC global interrupt	true	5	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
CAN1 TX interrupts		unused	
CAN1 RX0 interrupts		unused	
CAN1 RX1 interrupt		unused	
CAN1 SCE interrupt		unused	
TIM3 global interrupt		unused	
TIM4 global interrupt		unused	
TIM8 break interrupt and TIM12 global interrupt		unused	
TIM8 update interrupt and TIM13 global interrupt		unused	
TIM8 trigger and commutation interrupts and TIM14 global interrupt		unused	
TIM8 capture compare interrupt		unused	
FMC global interrupt		unused	
CAN2 TX interrupts		unused	
CAN2 RX0 interrupts	unused		
CAN2 RX1 interrupt	unused		
CAN2 SCE interrupt	unused		
FPU global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		
QUADSPI global interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
JPEG global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream4 global interrupt	false	true	true
ADC1, ADC2 and ADC3 global interrupts	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true
LTDC global interrupt	false	true	true

^{*} User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronic	X-CUBE-	4.20.0	Class : Graphics
s	TOUCHGFX		Group :
			Application
			Variant :
			TouchGFX
			Generator
			Version : 4.20.0

11. Docs & Resources

Type Link

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stm8_embedded_software_solutions.pdf

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