Implement full subtractor using VHDL

C:/modeltech64_10.5/examples/full_sub.vhd - Default

```
Ln#
 1
 2  Library ieee;
 3  use ieee.std_logic_1164.all;
 4
 5  entity full_sub is
 6     port(a,b,c:in bit; sub,borrow:out bit);
 7  end full_sub;
 8
 9  architecture data of full_sub is
10  begin
11     sub<= a xor b xor c;
12     borrow <= ((b xor c) and (not a)) or (b and c);
13  end data;
```