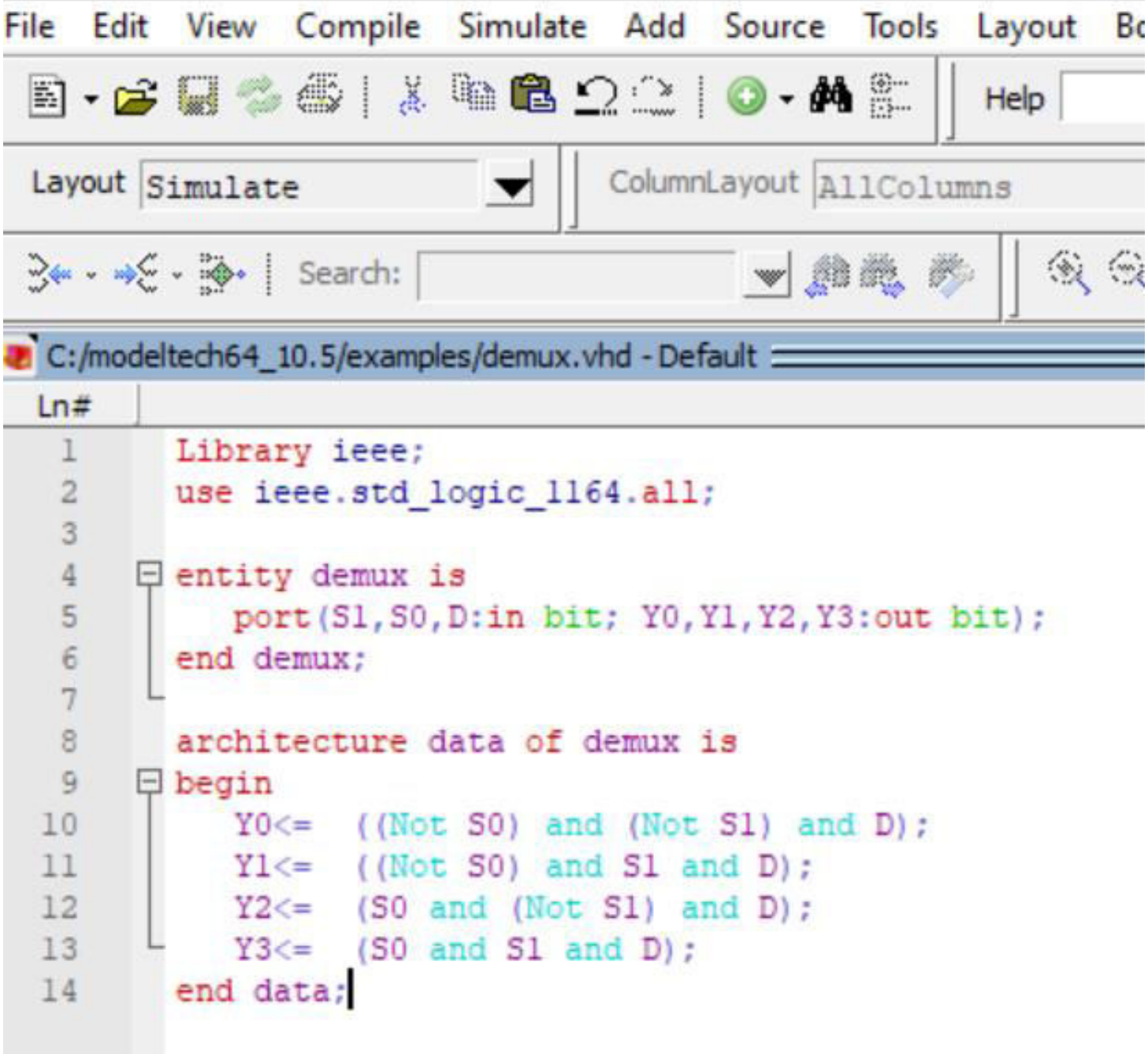


Implement 1*4 demux using VHDL

 ModelSim SE-64 10.5



The screenshot shows the ModelSim SE-64 10.5 software interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, and Bo. Below the menu bar is a toolbar with various icons for file operations, simulation, and layout. The 'Layout' dropdown is set to 'Simulate', and the 'ColumnLayout' dropdown is set to 'AllColumns'. The active window is titled 'C:/modeltech64_10.5/examples/demux.vhd - Default'. The VHDL code is displayed in a text editor with line numbers (Ln#) on the left. The code defines an entity 'demux' with two input bits 'S1' and 'S0', and one input bit 'D'. It has four output bits 'Y0', 'Y1', 'Y2', and 'Y3'. The architecture 'data' implements the demultiplexer logic using conditional assignments.

```
Ln# 1      Library ieee;
    2      use ieee.std_logic_1164.all;
    3
    4  entity demux is
    5      port(S1,S0,D:in bit; Y0,Y1,Y2,Y3:out bit);
    6  end demux;
    7
    8  architecture data of demux is
    9  begin
   10      Y0<= ((Not S0) and (Not S1) and D);
   11      Y1<= ((Not S0) and S1 and D);
   12      Y2<= (S0 and (Not S1) and D);
   13      Y3<= (S0 and S1 and D);
   14  end data;
```