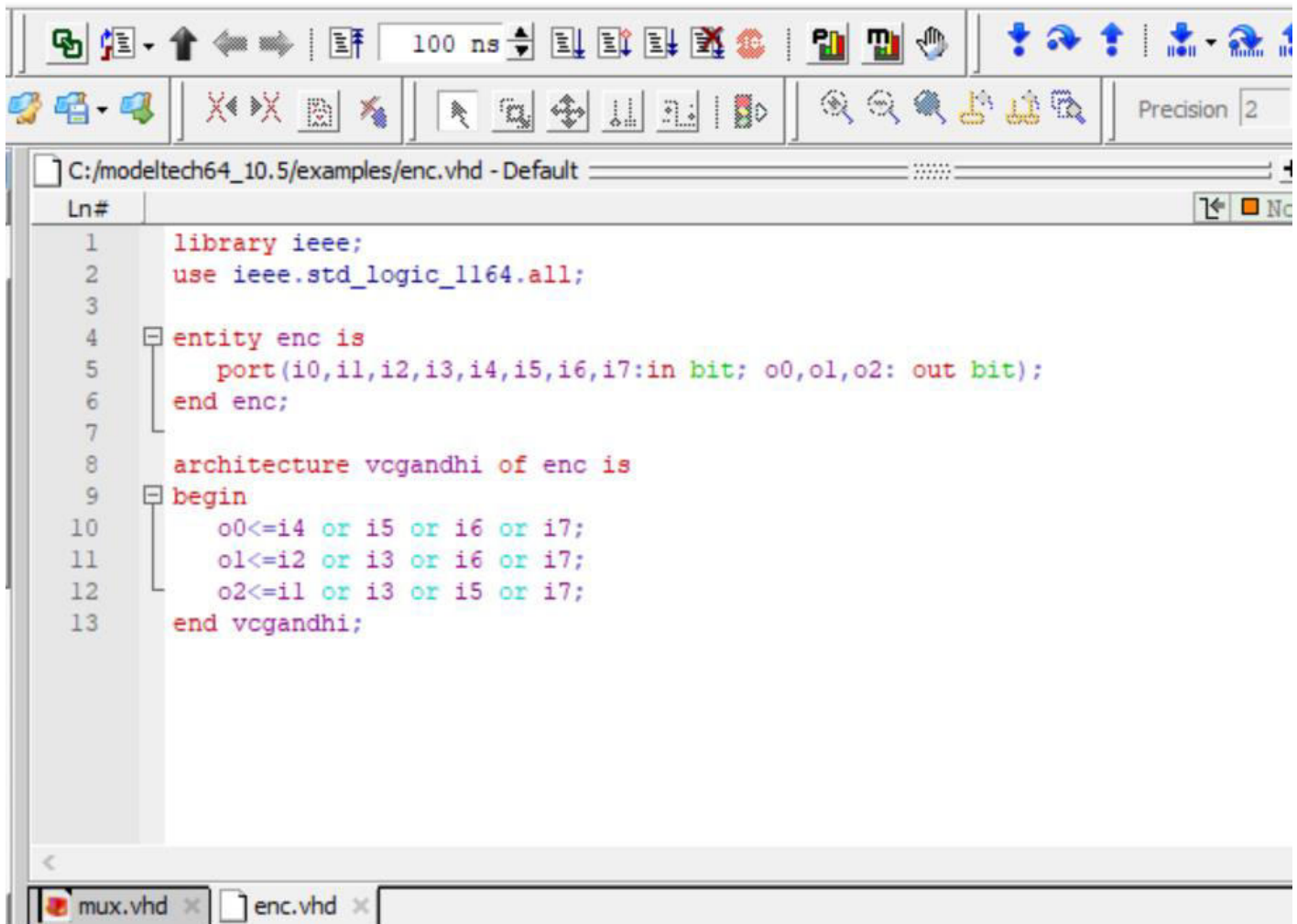


Implement 8*3 Encoder using VHDL



The screenshot shows a VHDL editor window with the following code:

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity enc is
5      port (i0,i1,i2,i3,i4,i5,i6,i7:in bit; o0,o1,o2: out bit);
6  end enc;
7
8  architecture vcgandhi of enc is
9  begin
10     o0<=i4 or i5 or i6 or i7;
11     o1<=i2 or i3 or i6 or i7;
12     o2<=i1 or i3 or i5 or i7;
13 end vcgandhi;
```

The editor has a toolbar at the top with various icons for file operations, editing, and simulation. The status bar at the bottom shows two open files: mux.vhd and enc.vhd.