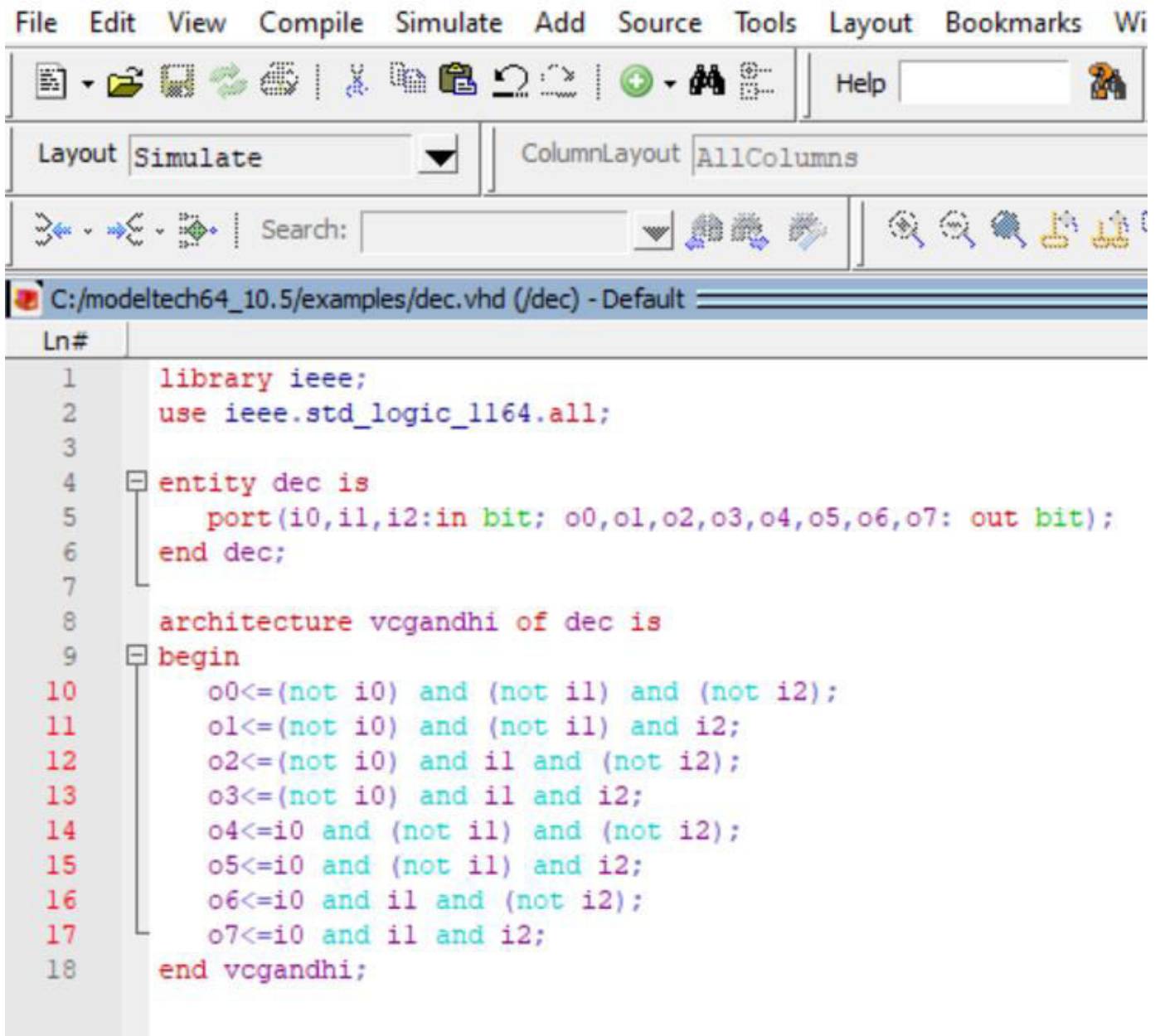


Implement 3*8 decoder using VHDL

 ModelSim SE-64 10.5



The screenshot displays the ModelSim SE-64 10.5 software interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, and Windows. Below the menu is a toolbar with various icons for file operations, simulation, and search. The 'Layout' dropdown is set to 'Simulate', and the 'ColumnLayout' dropdown is set to 'AllColumns'. The active window shows a VHDL file named 'C:/modeltech64_10.5/examples/dec.vhd (/dec) - Default'. The code is as follows:

```
Ln# |  
1   | library ieee;  
2   | use ieee.std_logic_1164.all;  
3   |  
4   | entity dec is  
5   |     port(i0,i1,i2:in bit; o0,o1,o2,o3,o4,o5,o6,o7: out bit);  
6   | end dec;  
7   |  
8   | architecture vcgandhi of dec is  
9   | begin  
10  |     o0<=(not i0) and (not i1) and (not i2);  
11  |     o1<=(not i0) and (not i1) and i2;  
12  |     o2<=(not i0) and i1 and (not i2);  
13  |     o3<=(not i0) and i1 and i2;  
14  |     o4<=i0 and (not i1) and (not i2);  
15  |     o5<=i0 and (not i1) and i2;  
16  |     o6<=i0 and i1 and (not i2);  
17  |     o7<=i0 and i1 and i2;  
18  | end vcgandhi;
```