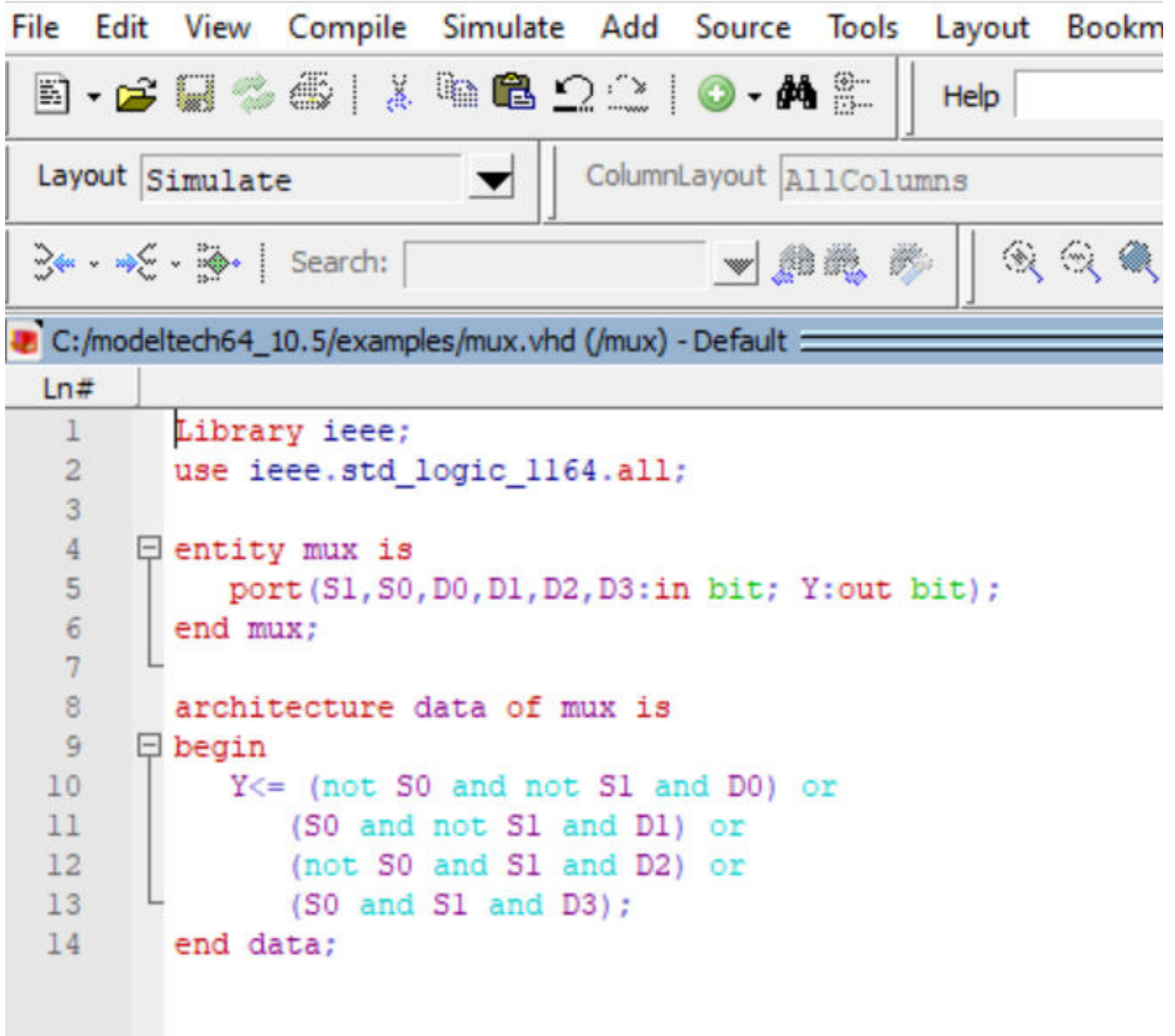


Implement 4*1 Mux using VHDL

 ModelSim SE-64 10.5



The screenshot shows the ModelSim SE-64 10.5 interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, and Bookmarks. Below the menu is a toolbar with various icons for file operations, simulation, and layout. The 'Layout' dropdown is set to 'Simulate' and the 'ColumnLayout' dropdown is set to 'AllColumns'. The active window is titled 'C:/modeltech64_10.5/examples/mux.vhd (/mux) - Default'. The code editor displays the following VHDL code:

```
Ln# |
1   | Library ieee;
2   | use ieee.std_logic_1164.all;
3   |
4   | entity mux is
5   |     port(S1,S0,D0,D1,D2,D3:in bit; Y:out bit);
6   | end mux;
7   |
8   | architecture data of mux is
9   | begin
10  |     Y<= (not S0 and not S1 and D0) or
11  |         (S0 and not S1 and D1) or
12  |         (not S0 and S1 and D2) or
13  |         (S0 and S1 and D3);
14  | end data;
```