

```
Library ieee;
```

```
use ieee.std_logic_1164.all;
```

```
entity half_adder is
```

```
    port(a,b:in bit; sum,carry:out bit);
```

```
end half_adder;
```

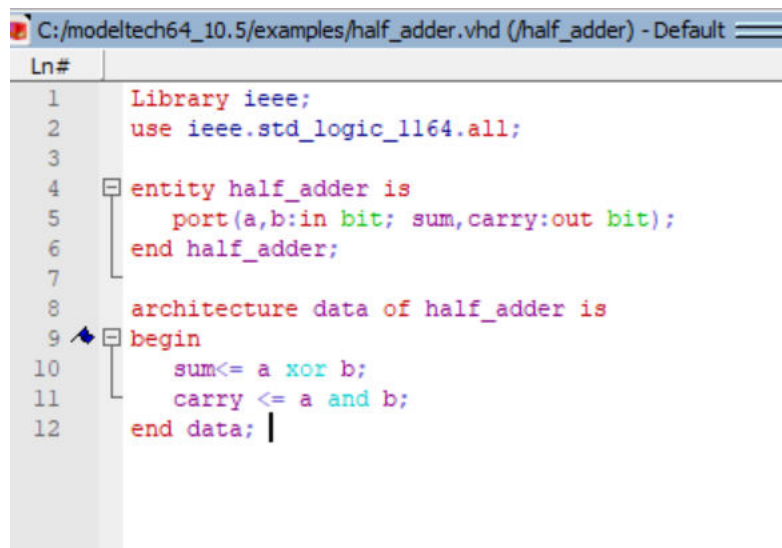
```
architecture data of half_adder is
```

```
begin
```

```
    sum<= a xor b;
```

```
    carry <= a and b;
```

```
end data;
```



```
C:/modeltech64_10.5/examples/half_adder.vhd (/half_adder) - Default
Ln#
1      Library ieee;
2      use ieee.std_logic_1164.all;
3
4      entity half_adder is
5          port(a,b:in bit; sum,carry:out bit);
6      end half_adder;
7
8      architecture data of half_adder is
9      begin
10         sum<= a xor b;
11         carry <= a and b;
12     end data;
```