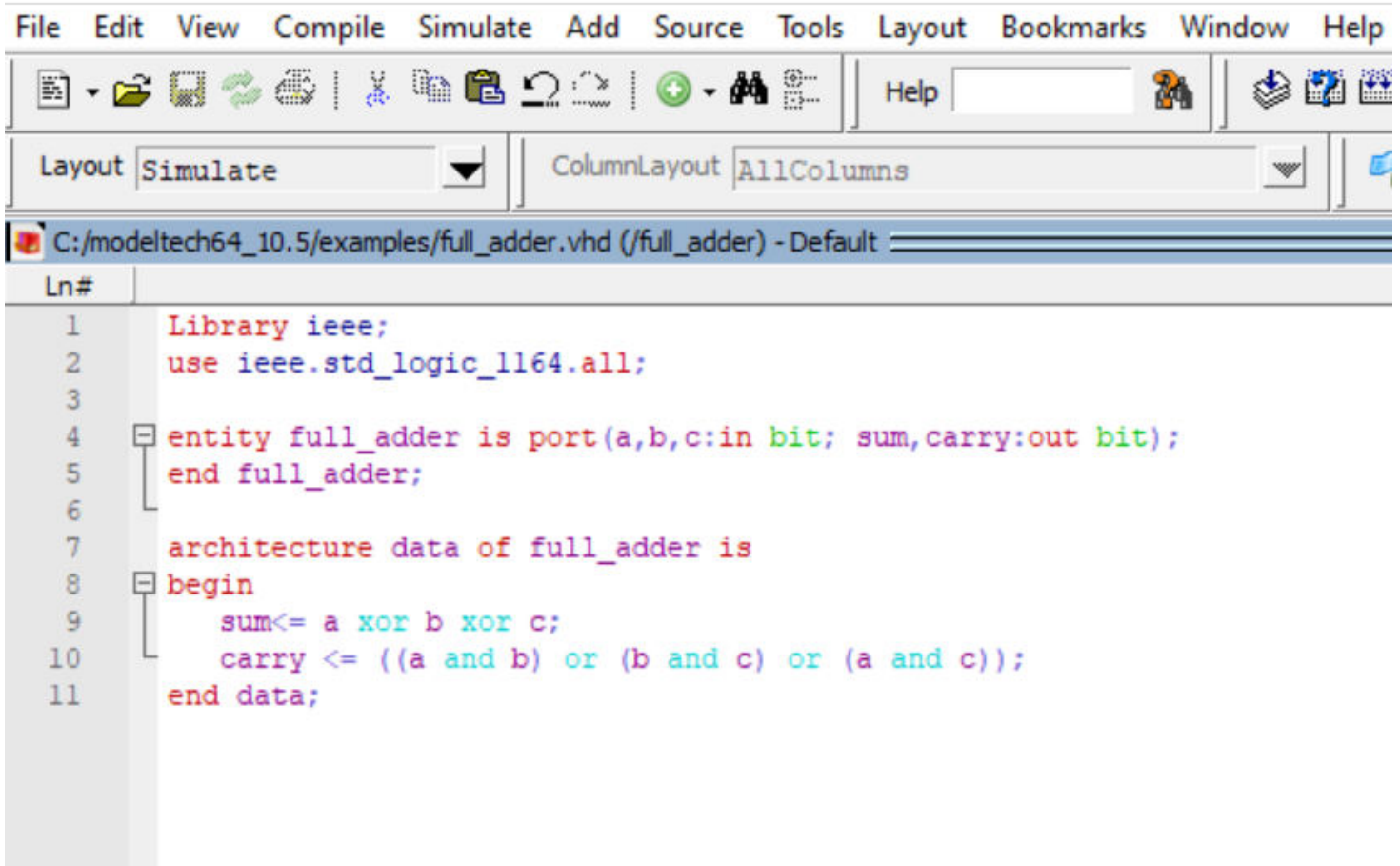


Title: Implement full adder using VHDL.

 ModelSim SE-64 10.5



The screenshot displays the ModelSim SE-64 10.5 software interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, and Help. Below the menu is a toolbar with various icons for file operations, simulation, and layout. The 'Layout' dropdown is set to 'Simulate', and the 'ColumnLayout' dropdown is set to 'AllColumns'. The main window shows the source code for a VHDL file named 'C:/modeltech64\_10.5/examples/full\_adder.vhd (/full\_adder) - Default'. The code is as follows:

```
Ln#   1  Library ieee;
      2  use ieee.std_logic_1164.all;
      3
      4  entity full_adder is port(a,b,c:in bit; sum,carry:out bit);
      5  end full_adder;
      6
      7  architecture data of full_adder is
      8  begin
      9      sum<= a xor b xor c;
     10      carry <= ((a and b) or (b and c) or (a and c));
     11  end data;
```