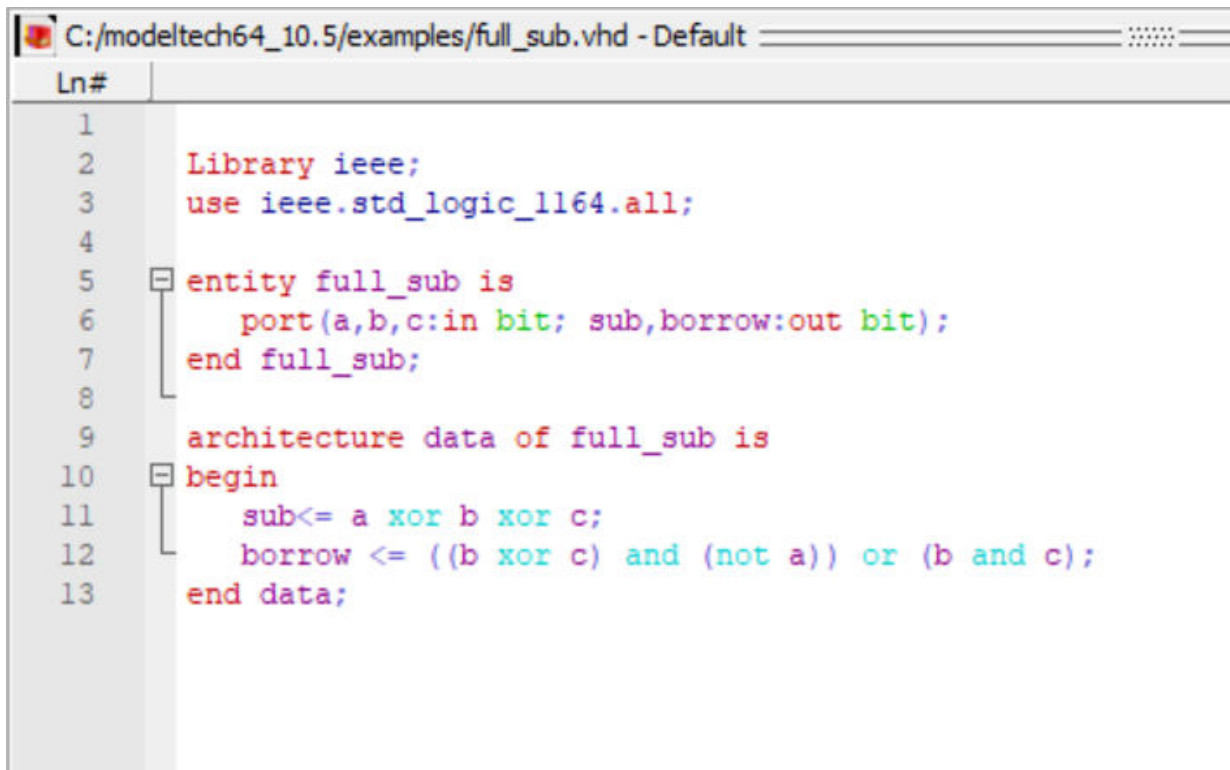


Implement full subtractor using VHDL



The image shows a screenshot of a VHDL code editor window. The title bar indicates the file path is C:/modeltech64_10.5/examples/full_sub.vhd and it is set to 'Default'. The editor displays VHDL code for a full subtractor. On the left side, there is a line number column (Ln#) ranging from 1 to 13. The code is as follows:

```
1
2  Library ieee;
3  use ieee.std_logic_1164.all;
4
5  entity full_sub is
6      port(a,b,c:in bit; sub,borrow:out bit);
7  end full_sub;
8
9  architecture data of full_sub is
10     begin
11         sub<= a xor b xor c;
12         borrow <= ((b xor c) and (not a)) or (b and c);
13     end data;
```