Implement half subtractor using VHDL.

ModelSim SE-64 10.5

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half_sub.vhd	✓	VHDL	1	11/19/2022 11:25:26 ...

C:/modeltech64_10.5/examples/half_sub.vhd - Default

```
Ln#
1      Library ieee;
2      use ieee.std_logic_1164.all;
3
4      entity half_sub is
5          port(a,c:in bit; d,b:out bit);
6      end half_sub;
7
8      architecture data of half_sub is
9      begin
10         d<= a xor c;
11         b<= (a and (not c));
12     end data;
```