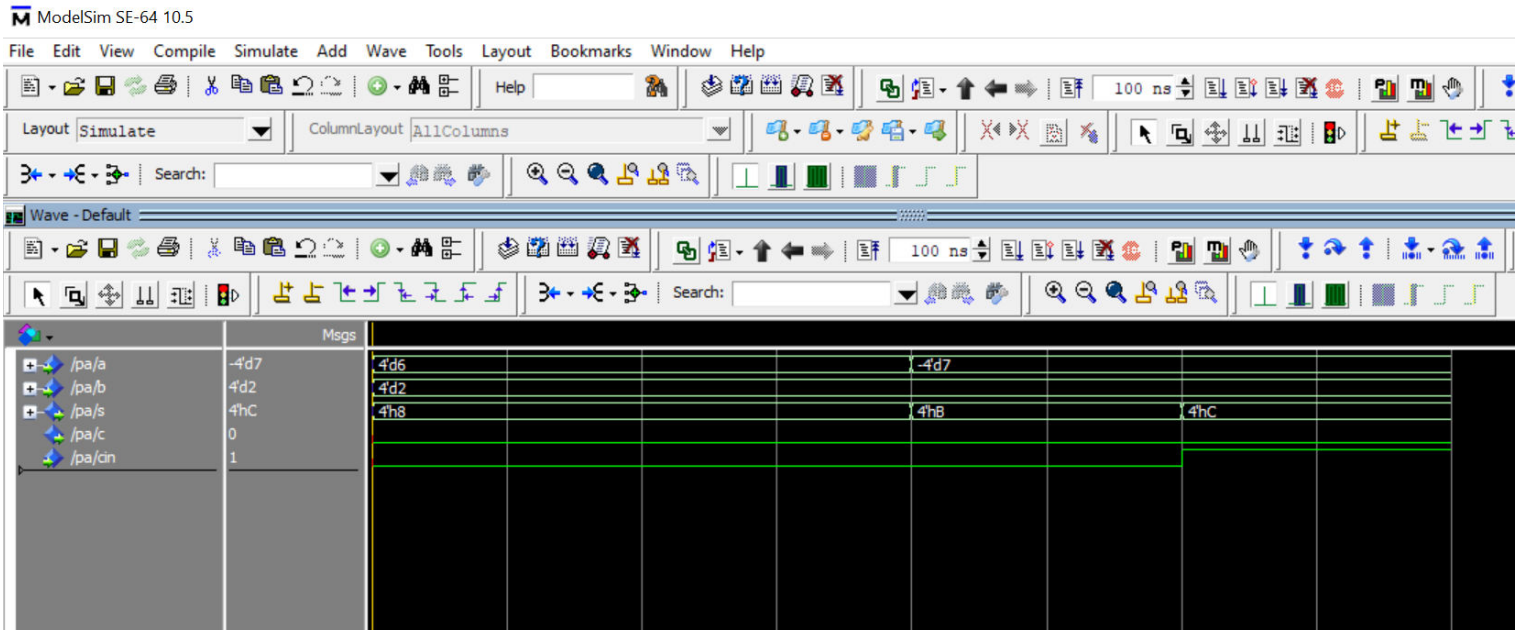
Implement 4 bit parallel adder using VHDL and demonstrate the result using simulation.

C:/modeltech64_10.5/examples/pa.vhd (/pa) - Default *

```
Ln#
 1  library IEEE;
 2  use IEEE.STD_LOGIC_1164.ALL;
 3  use IEEE.STD_LOGIC_ARITH.ALL;
 4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
 5
 6  entity pa is
 7      Port ( a : in std_logic_vector(3 downto 0);
 8             b : in std_logic_vector(3 downto 0);
 9             s : out std_logic_vector(3 downto 0);
10             c : out std_logic;
11             cin : in std_logic);
12  end pa;
13
14  architecture pa11 of pa is
15
16  begin
17  process(a,b,cin)
18  variable u:std_logic;
19  begin
20  u:=cin;
21  for i in 0 to 3 loop
22  s(i)<=a(i) xor b(i) xor u;
23  u:=(a(i) and b(i))or(b(i) and u) or(u and a(i));
24  end loop;
25  c<=u;
26  end process;
27
28  end pa11;
```

Result


ModelSim SE-64 10.5
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Help
100 ns
Layout Simulate
ColumnLayout AllColumns
Search:
Wave - Default
100 ns
Search:
Msgs
/pa/a
/pa/b
/pa/s
/pa/c
/pa/cin
-4'd7
4'd2
4'hC
0
1
4'd6
-4'd7
4'd2
4'h8
4'hB
4'hC