

# Sealed Lead-Acid Battery Charger

## FEATURES

- Optimum Control for Maximum Battery Capacity and Life
- Internal State Logic Provides Three Charge States
- Precision Reference Tracks Battery Requirements Over Temperature
- Controls Both Voltage and Current at Charger Output
- System Interface Functions
- Typical Standby Supply Current of only 1.6mA

## DESCRIPTION

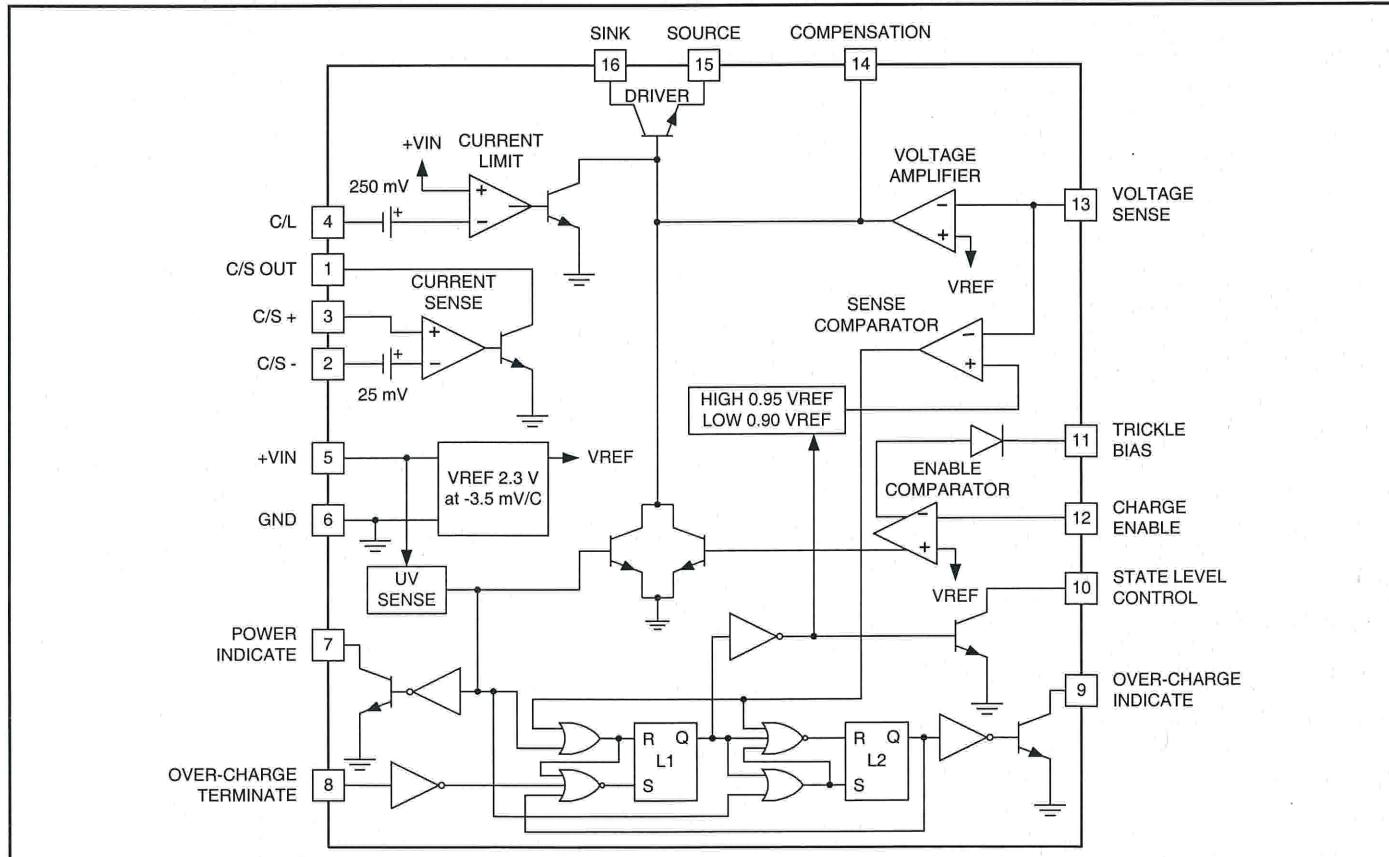
The UC2906 series of battery charger controllers contains all of the necessary circuitry to optimally control the charge and hold cycle for sealed lead-acid batteries. These integrated circuits monitor and control both the output voltage and current of the charger through three separate charge states; a high current bulk-charge state, a controlled over-charge, and a precision float-charge, or standby, state.

Optimum charging conditions are maintained over an extended temperature range with an internal reference that tracks the nominal temperature characteristics of the lead-acid cell. A typical standby supply current requirement of only 1.6mA allows these ICs to predictably monitor ambient temperatures.

Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply at least 25mA of base drive to an external pass device. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. A charge enable comparator with a trickle bias output can be used to implement a low current turn-on mode of the charger, preventing high current charging during abnormal conditions such as a shorted battery cell.

Other features include a supply under-voltage sense circuit with a logic output to indicate when input power is present. In addition the over-charge state of the charger can be externally monitored and terminated using the over-charge indicate output and over-charge terminate input.

## BLOCK DIAGRAM

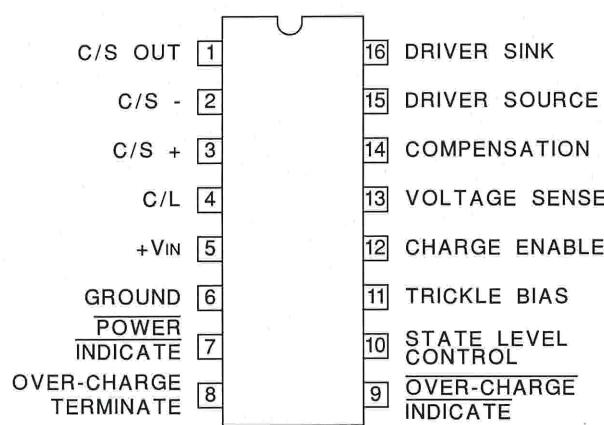


**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (+V <sub>IN</sub> ) .....	40V
Open Collector Output Voltages .....	40V
Amplifier and Comparator Input Voltages .....	-0.3V to +40V
Over-Charge Terminate Input Voltage .....	-0.3V to +40V
Current Sense Amplifier Output Current.....	80mA
Other Open Collector Output Currents.....	20mA
Trickle Bias Voltage Differential with respect to V <sub>IN</sub> .....	-32V
Trickle Bias Output Current .....	-40mA
Driver Current.....	80mA
Power Dissipation at T <sub>A</sub> = 25°C (Note 2).....	1000mW
Power Dissipation at T <sub>C</sub> = 25°C (Note 2).....	2000mW
Operating Junction Temperature .....	-55°C to +150°C
Storage Temperature .....	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) .....	300°C

**Note 1:** Voltages are referenced to ground (Pin 6). Currents are positive into, negative out of, the specified terminals.

**Note 2:** Consult Packaging section of Databook for thermal limitations and considerations of packages.

**DIL-16, SOIC-16 (TOP VIEW)**  
**J or N Package, DW Package**

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for T<sub>A</sub> = -40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, +V<sub>IN</sub> = 10V, T<sub>A</sub> = T<sub>J</sub>.

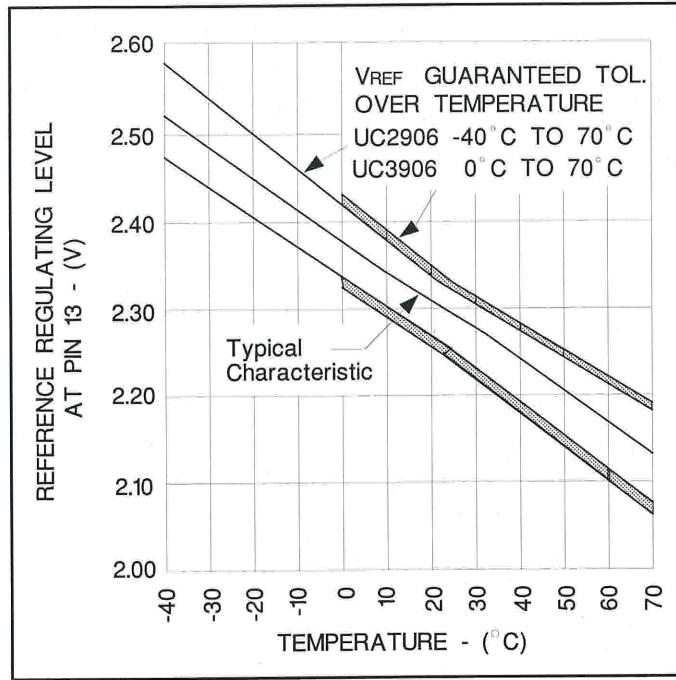
PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Input Supply</b>								
Supply Current	+V <sub>IN</sub> = 10V		1.6	3.3		1.6	3.3	mA
	+V <sub>IN</sub> = 40V		1.8	3.6		1.8	3.6	mA
	+V <sub>IN</sub> = 40V, T <sub>A</sub> = -40°C to 85°C		1.8	4				mA
Supply Under-Voltage Threshold	+V <sub>IN</sub> = Low to High	4.2	4.5	4.8	4.2	4.5	4.8	V
Supply Under-Voltage Hysteresis			0.20	0.30		0.20	0.30	V
<b>Internal Reference (V<sub>REF</sub>)</b>								
Voltage Level (Note 3)	Measured as Regulating Level at Pin 13 w/ Driver Current = 1mA, T <sub>J</sub> = 25°C	2.275	2.3	2.325	2.270	2.3	2.330	V
Line Regulation	+V <sub>IN</sub> = 5 to 40V		3	8		3	8	mV
Temperature Coefficient			-3.5			-3.5		mV/°C

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC2906 and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3906,  $+V_{IN} = 10\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Voltage Amplifier</b>								
Input Bias Current	Total Input Bias at Regulating Level	-0.5	-0.2		-0.5	-0.2		$\mu\text{A}$
Maximum Output Current	Source	-45	-30	-15	-45	-30	-15	$\mu\text{A}$
	Sink	30	60	90	30	60	90	$\mu\text{A}$
Open Loop Gain	Driver current = 1mA	50	65		50	65		dB
Output Voltage Swing	Volts above GND or below $+V_{IN}$		0.2			0.2		V
<b>Driver</b>								
Minimum Supply to Source Differential	Pin 16 = $+V_{IN}$ , $I_O = 10\text{mA}$		2.0	2.2		2.0	2.2	V
Maximum Output Current	Pin 16 to Pin 15 = 2V	25	40		25	40		mA
Saturation Voltage			0.2	0.45		0.2	0.45	V
<b>Current Limit Amplifier</b>								
Input Bias Current			0.2	1.0		0.2	1.0	$\mu\text{A}$
Threshold Voltage	Offset below $+V_{IN}$	225	250	275	225	250	275	mV
Threshold Supply Sensitivity	$+V_{IN} = 5$ to 40V		0.03	0.25		0.03	0.25	%/V
<b>Voltage Sense Comparator</b>								
Threshold Voltage	As a function of $V_{REF}$ , $L_1 = \text{RESET}$	0.94	0.949	0.960	0.94	0.949	0.960	V/V
	As a function of $V_{REF}$ , $L_1 = \text{SET}$	0.895	0.90	0.910	0.895	0.90	0.910	V/V
Input Bias Current	Total Input Bias at Thresholds	-0.5	-0.2		-0.5	-0.2		$\mu\text{A}$
<b>Current Sense Comparator</b>								
Input Bias Current			0.1	0.5		0.1	0.5	$\mu\text{A}$
Input Offset Current			0.01	0.2		0.01	0.2	$\mu\text{A}$
Input Offset Voltage	Referenced to Pin 2, $I_{OUT} = 1\text{mA}$	20	25	30	20	25	30	mV
Offset Supply Sensitivity	$+V_{IN} = 5$ to 40V		0.05	0.35		0.05	0.35	%/V
Offset Common Mode Sensitivity	CMV = 2V to $+V_{IN}$		0.05	0.35		0.05	0.35	%/V
Maximum Output Current	$V_{OUT} = 2\text{V}$	25	40		25	40		mA
Output Saturation Voltage	$I_{OUT} = 10\text{mA}$		0.2	0.45		0.2	0.45	V
<b>Enable Comparator</b>								
Threshold Voltage	As a function of $V_{REF}$	0.99	1.0	1.01	0.99	1.0	1.01	V/V
Input Bias Current		-0.5	-0.2		-0.5	-0.2		$\mu\text{A}$
Trickle Bias Maximum Output Current	$V_{OUT} = +V_{IN} - 3\text{V}$	25	40		25	40		mA
Trickle Bias Maximum Output Voltage	Volts below $+V_{IN}$ , $I_{OUT} = 10\text{mA}$		2.0	2.6		2.0	2.6	V
Trickle Bias Reverse Hold-Off Voltage	$+V_{IN} = 0\text{V}$ , $I_{OUT} = -10\mu\text{A}$	6.3	7.0		6.3	7.0		V
<b>Over-Charge Terminate Input</b>								
Threshold Voltage		0.7	1.0	1.3	0.7	1.0	1.3	V
Internal Pull-Up Current	At Threshold		10			10		$\mu\text{A}$
<b>Open Collector Outputs (Pins 7, 9, and 10)</b>								
Maximum Output Current	$V_{OUT} = 2\text{V}$	2.5	5		2.5	5		mA
Saturation Voltage	$I_{OUT} = 1.6\text{mA}$		0.25	0.45		0.25	0.45	V
	$I_{OUT} = 50\mu\text{A}$		0.03	0.05		0.03	0.05	V
Leakage Current	$V_{OUT} = 40\text{V}$		1	3		1	3	$\mu\text{A}$

Note 3. The reference voltage will change as a function of power dissipation on the die according to the temperature coefficient of the reference and the thermal resistance, junction-to-ambient.

## OPERATION AND APPLICATION INFORMATION



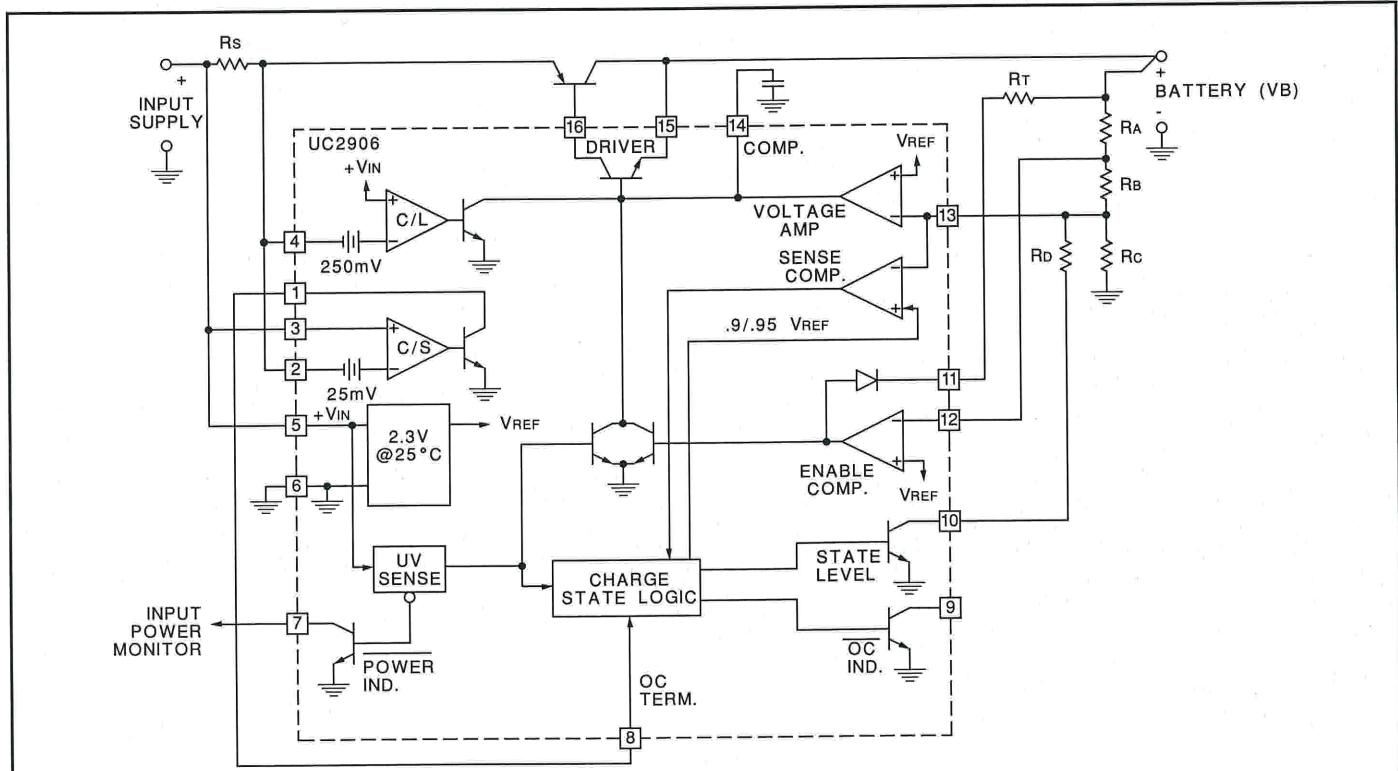
*Internal reference temperature characteristic and tolerance.*

### Dual Level Float Charger Operations

The UC2906 is shown configured as a dual level float charger in Figure 1. All high currents are handled by the external PNP pass transistor with the driver supplying base drive to this device. This scheme uses the TRICKLE BIAS output and the charge enable comparator

to give the charger a low current turn on mode. The output current of the charger is limited to a low-level until the battery reaches a specified voltage, preventing a high current charging if a battery cell is shorted. Figure 2 shows the state diagram of the charger. Upon turn on the UV sense circuitry puts the charger in state 1, the high rate bulk-charge state. In this state, once the enable threshold has been exceeded, the charger will supply a peak current that is determined by the 250mV offset in the C/L amplifier and the sensing resistor  $R_s$ .

To guarantee full re-charge of the battery, the charger's voltage loop has an elevated regulating level,  $V_{OC}$ , during state 1 and state 2. When the battery voltage reaches 95% of  $V_{OC}$ , the charger enters the over-charge state, state 2. The charger stays in this state until the OVER-CHARGE TERMINATE pin goes high. In Figure 1, the charger uses the current sense amplifier to generate this signal by sensing when the charge current has tapered to a specified level,  $I_{OCT}$ . Alternatively the over-charge could have been controlled by an external source, such as a timer, by using the OVER-CHARGE INDICATE signal at Pin 9. If a load is applied to the battery and begins to discharge it, the charger will contribute its full output to the load. If the battery drops 10% below the float level, the charger will reset itself to state 1. When the load is removed a full charge cycle will follow. A graphical representation of a charge, and discharge, cycle of the dual lever float charger is shown in Figure 3.



*Figure 1. The UC2906 in a dual level float charger.*

## OPERATION AND APPLICATION INFORMATION (cont.)

## Design Procedure

1) Pick divider current,  $I_D$ . Recommended value is 50 $\mu A$  to 100 $\mu A$ .

$$2) R_C = 2.3V / I_D$$

$$3) R_A + R_B = R_{SUM} = (V_F - 2.3V) / I_D$$

$$4) R_D = 2.3V \cdot R_{SUM} / (V_{OC} - V_F)$$

$$5) R_A = (R_{SUM} + R_X)(1 - 2.3V / V_T)$$

WHERE:  $R_X = R_C \cdot R_D / (R_C + R_D)$

$$6) R_B = R_{SUM} - R_A$$

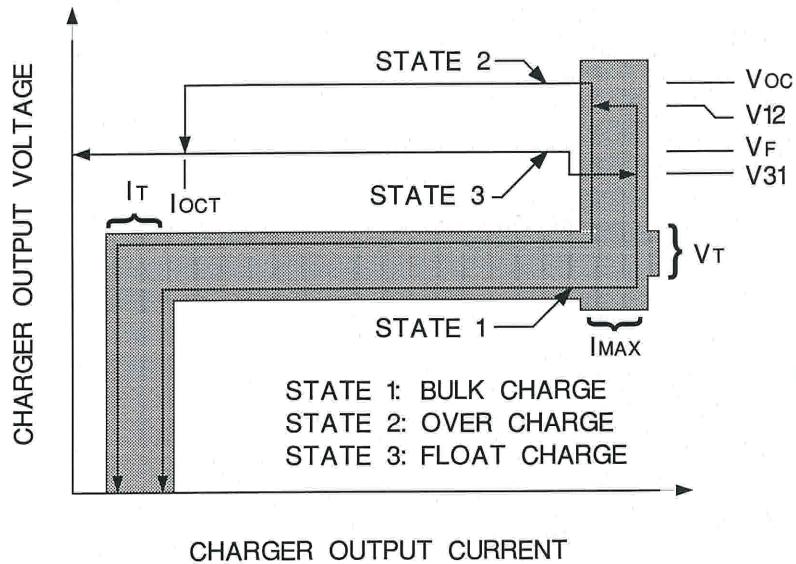
$$7) R_S = 0.25V / I_{MAX}$$

$$8) R_T = (V_{IN} - V_T - 2.5V) / I_T$$

$$9) I_{OCT} = \frac{I_{MAX}}{10}$$

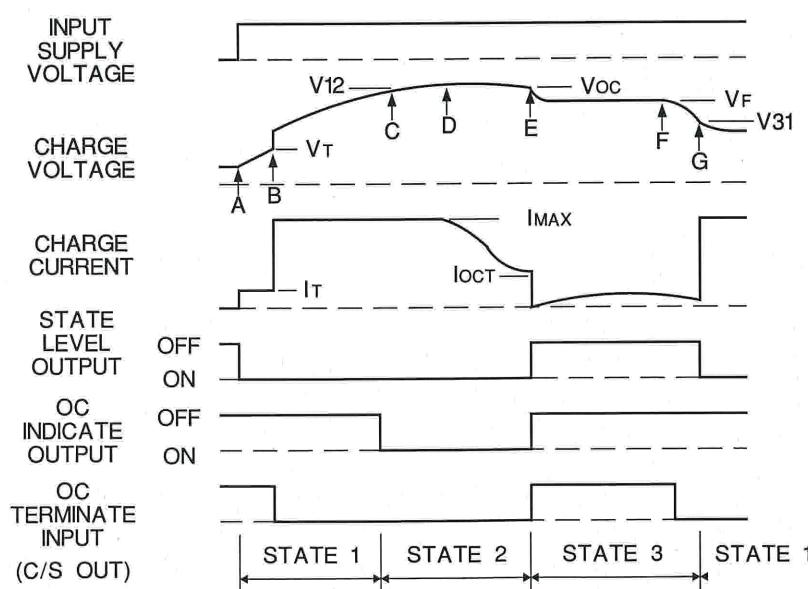
Note:  $V_{12} = 0.95 V_{OC}$ ,

$V_{31} = 0.90 V_F$ ,



For further design and application information see  
UICC Application Note U-104

Figure 2. State diagram and design equations for the dual level float charger.



## Explanation: Dual Level Float Charger

- A. Input power turns on, battery charges at trickle current rate.
- B. Battery voltage reaches  $V_T$  enabling the driver and turning off the trickle bias output, battery charges at  $I_{MAX}$  rate.
- C. Transition voltage  $V_{12}$  is reached and the charger indicates that it is now in the over-charge state, state 2.
- D. Battery voltage approaches the over-charge level  $V_{OC}$  and the charge current begins to taper.
- E. Charge current tapers to  $I_{OCT}$ . The current sense amplifier output, in this case tied to the OC TERMINATE input, goes high. The charger changes to the float state and holds the battery voltage at  $V_F$ .
- F. Here a load ( $>I_{MAX}$ ) begins to discharge the battery.
- G. The load discharges the battery such that the battery voltage falls below  $V_{31}$ . The charger is now in state 1, again.

Figure 3. Typical charge cycle: UC2906 dual level float charger.

**OPERATION AND APPLICATION INFORMATION (cont.)****Compensated Reference Matches Battery Requirements**

When the charger is in the float state, the battery will be maintained at a precise float voltage,  $V_F$ . The accuracy of this float state will maximize the standby life of the battery while the bulk-charge and over-charge states guarantee rapid and full re-charge. All of the voltage thresholds on the UC2906 are derived from the internal reference. This reference has a temperature coefficient that tracks the temperature characteristic of the optimum-charge and hold levels for sealed lead-acid cells. This further guarantees that proper charging occurs, even at temperature extremes.

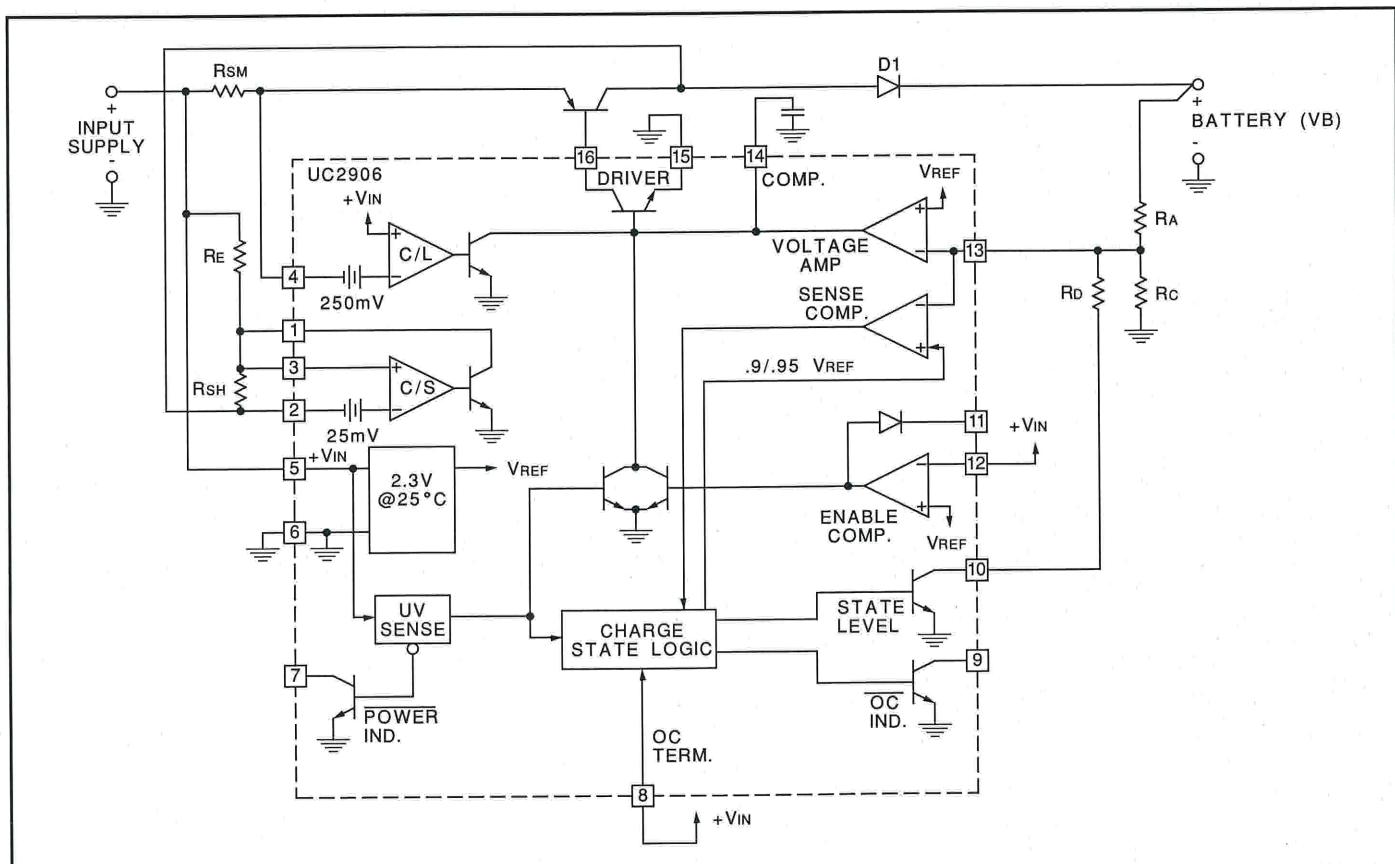
**Dual Step Current Charger Operation**

Figures 4, 5 and 6 illustrate the UC2906's use in a different charging scheme. The dual step current charger is useful when a large string of series cells must be charged. The holding-charge state maintains a slightly elevated voltage across the batteries with the holding current,  $I_H$ . This will tend to guarantee equal charge distribution between the cells. The bulk-charge state is similar to that of the float charger with the exception that when  $V_{12}$  is reached, no over-charge state occurs since Pin 8 is tied high at all times. The current sense amplifier is used to regulate the holding current. In some applica-

tions a series resistor, or external buffering transistor, may be required at the current sense output to prevent excessive power dissipation on the UC2906.

**A PNP Pass Device Reduces Minimum Input to Output Differential**

The configuration of the driver on the UC2906 allows a good bit of flexibility when interfacing to an external pass transistor. The two chargers shown in Figures 1 and 4 both use PNP pass devices, although an NPN device driven from the source output of the UC2906 driver can also be used. In situations where the charger must operate with low input to output differentials the PNP pass device should be configured as shown in Figure 4. The PNP can be operated in a saturated mode with only the series diode and sense resistor adding to the minimum differential. The series diode, D1, in many applications, can be eliminated. This diode prevents any discharging of the battery, except through the sensing divider, when the charger is attached to the battery with no input supply voltage. If discharging under this condition must be kept to an absolute minimum, the sense divider can be referenced to the POWER INDICATE pin, Pin 7, instead of ground. In this manner the open collector off state of Pin 7 will prevent the divider resistors from discharging the battery when the input supply is removed.



*Figure 4. The UC2906 in a dual step current charger.*

## OPERATION AND APPLICATION INFORMATION (cont.)

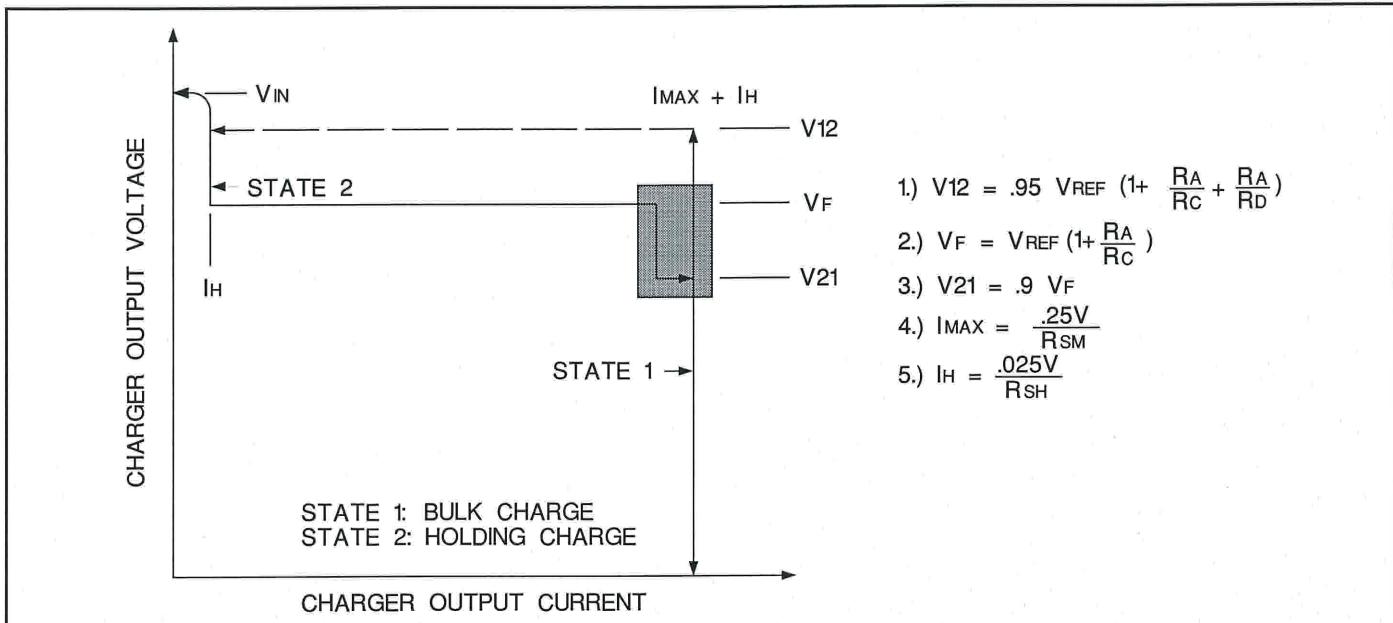
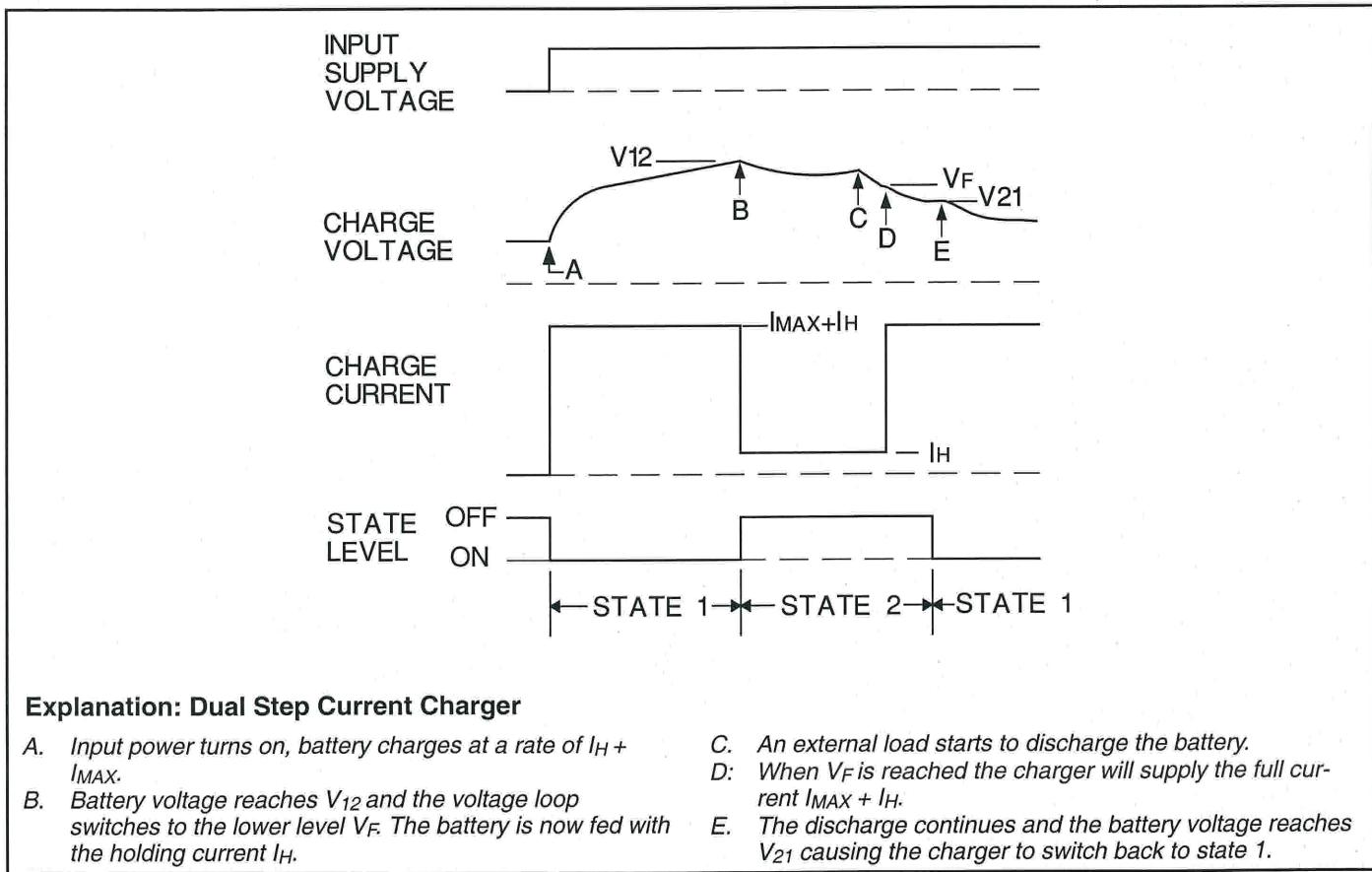


Figure 5. State Diagram and design equations for the dual step current charger.



### Explanation: Dual Step Current Charger

- A. Input power turns on, battery charges at a rate of  $I_H + I_{MAX}$ .
- B. Battery voltage reaches  $V_{12}$  and the voltage loop switches to the lower level  $V_F$ . The battery is now fed with the holding current  $I_H$ .
- C. An external load starts to discharge the battery.
- D. When  $V_F$  is reached the charger will supply the full current  $I_{MAX} + I_H$ .
- E. The discharge continues and the battery voltage reaches  $V_{21}$  causing the charger to switch back to state 1.

Figure 6. Typical charge cycle: UC2906 dual step current charger

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2906DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	UC2906DW	<span style="background-color: red; color: white;">Samples</span>
UC2906DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	UC2906DW	<span style="background-color: red; color: white;">Samples</span>
UC2906DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	UC2906DW	<span style="background-color: red; color: white;">Samples</span>
UC2906N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 70	UC2906N	<span style="background-color: red; color: white;">Samples</span>
UC2906NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 70	UC2906N	<span style="background-color: red; color: white;">Samples</span>
UC3906DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	<span style="background-color: red; color: white;">Samples</span>
UC3906DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	<span style="background-color: red; color: white;">Samples</span>
UC3906DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	<span style="background-color: red; color: white;">Samples</span>
UC3906DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	<span style="background-color: red; color: white;">Samples</span>
UC3906N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-20 to 70	UC3906N	<span style="background-color: red; color: white;">Samples</span>
UC3906NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-20 to 70	UC3906N	<span style="background-color: red; color: white;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

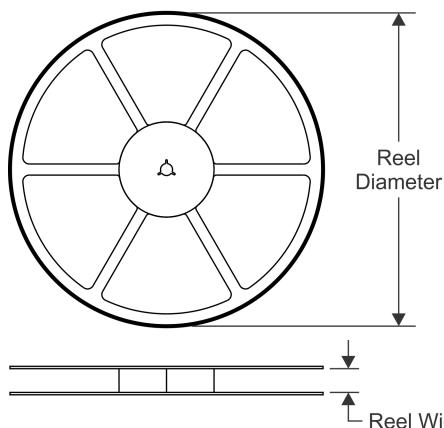
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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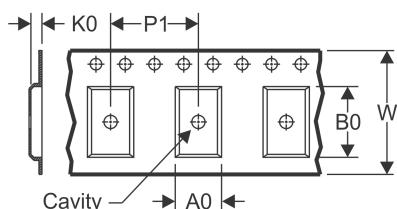
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

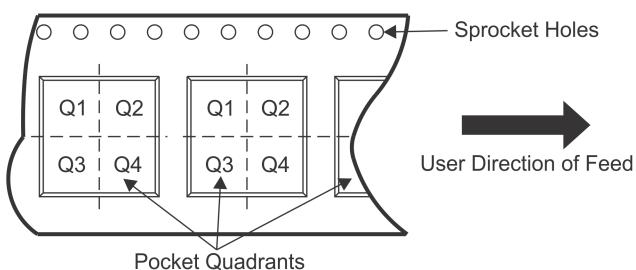


### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

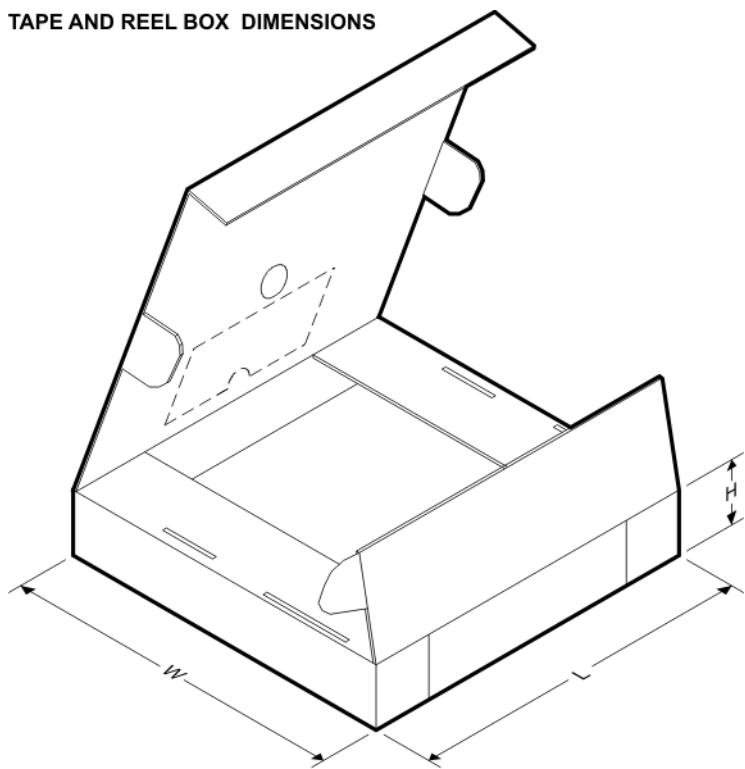
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2906DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3906DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2906DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3906DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

# GENERIC PACKAGE VIEW

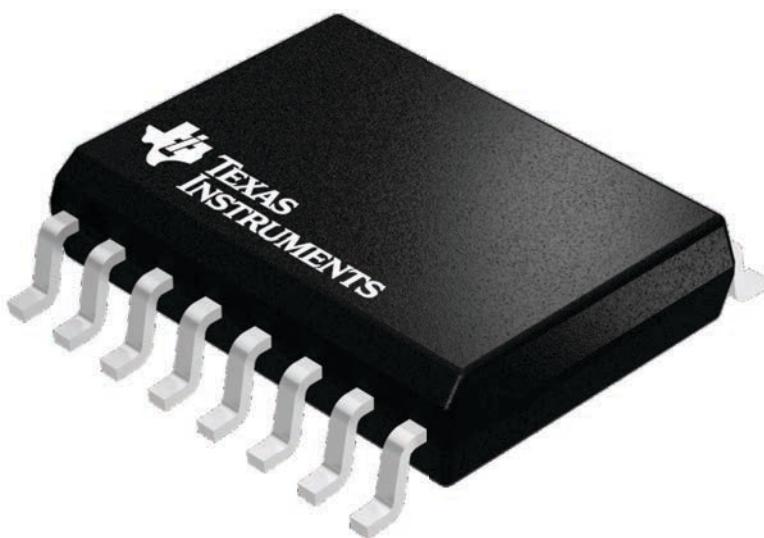
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

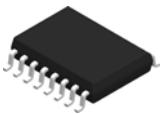
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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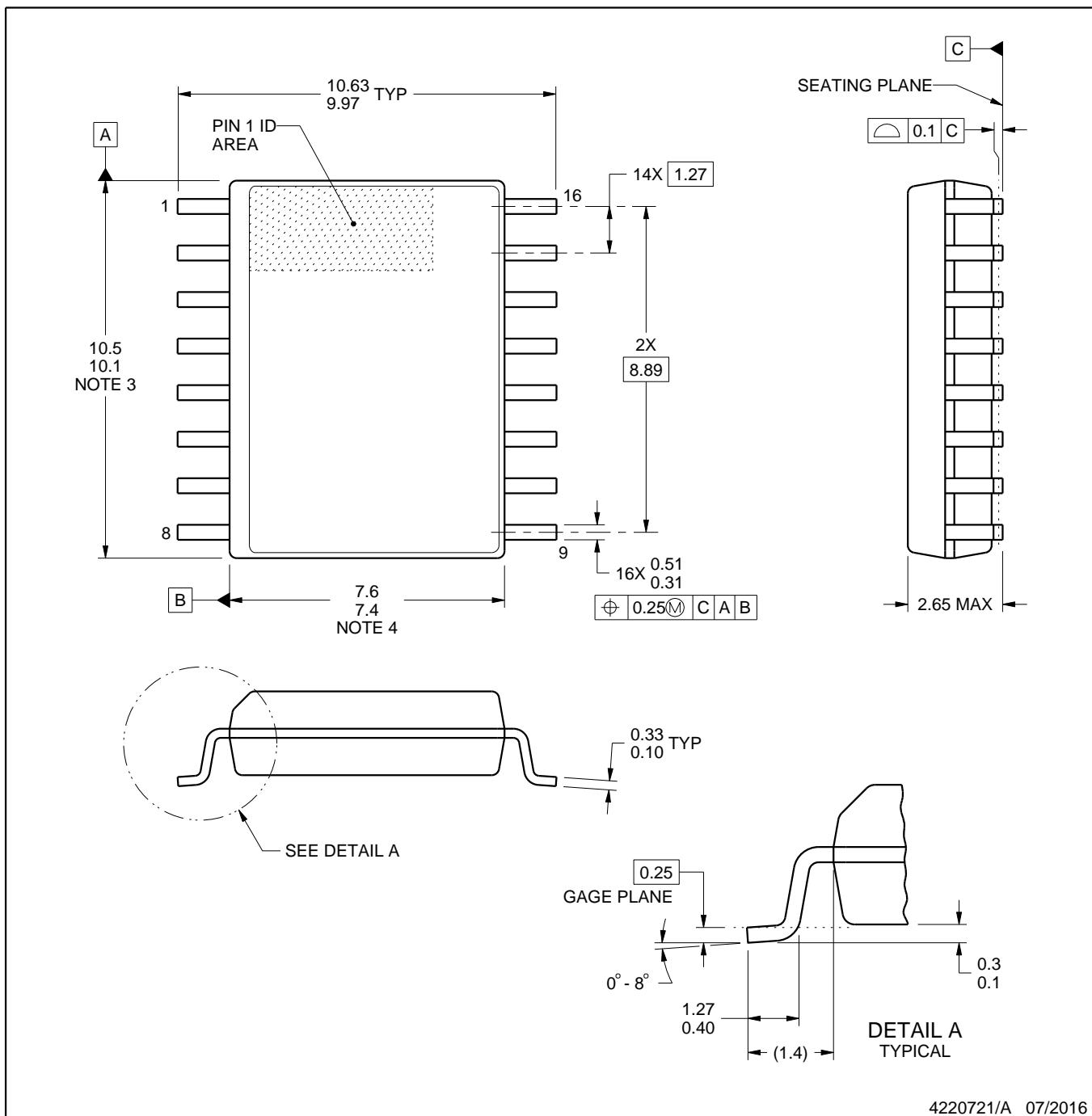
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# PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



## NOTES:

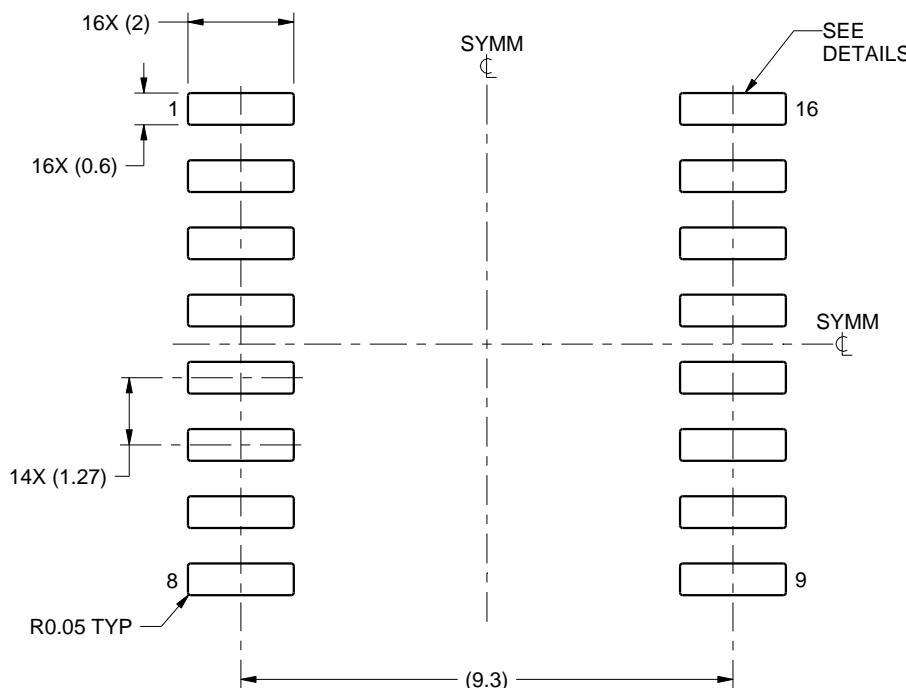
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

## **EXAMPLE BOARD LAYOUT**

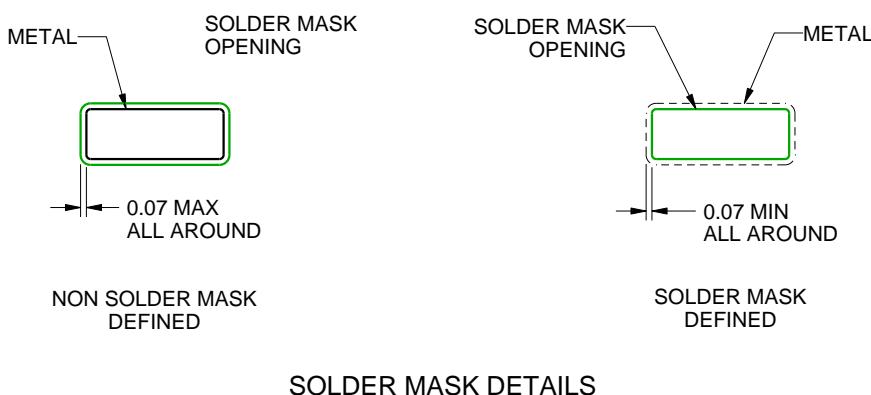
DW0016A

## **SOIC - 2.65 mm max height**

so|c



## LAND PATTERN EXAMPLE SCALE:7X



4220721/A 07/2016

## NOTES: (continued)

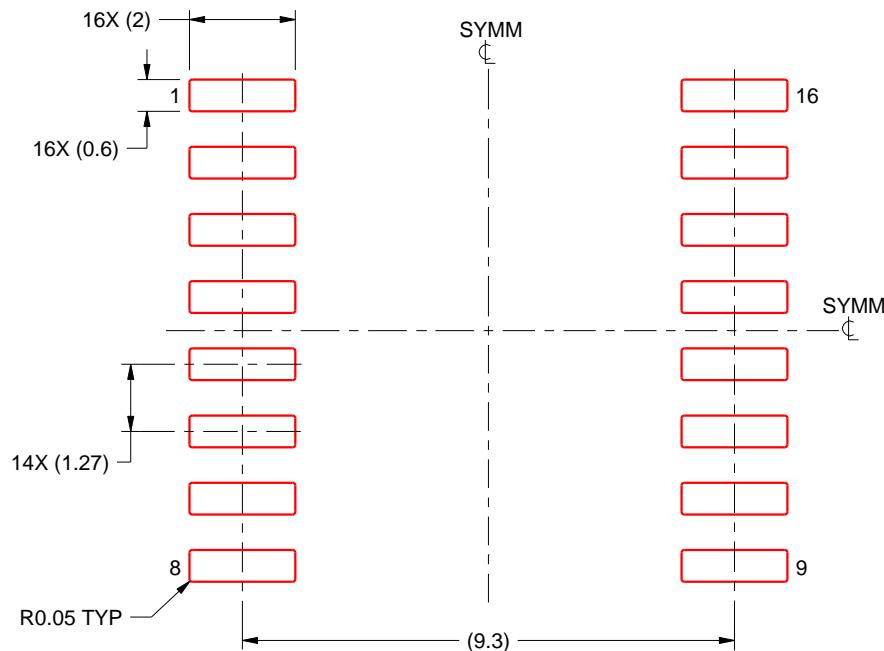
6. Publication IPC-7351 may have alternate designs.
  7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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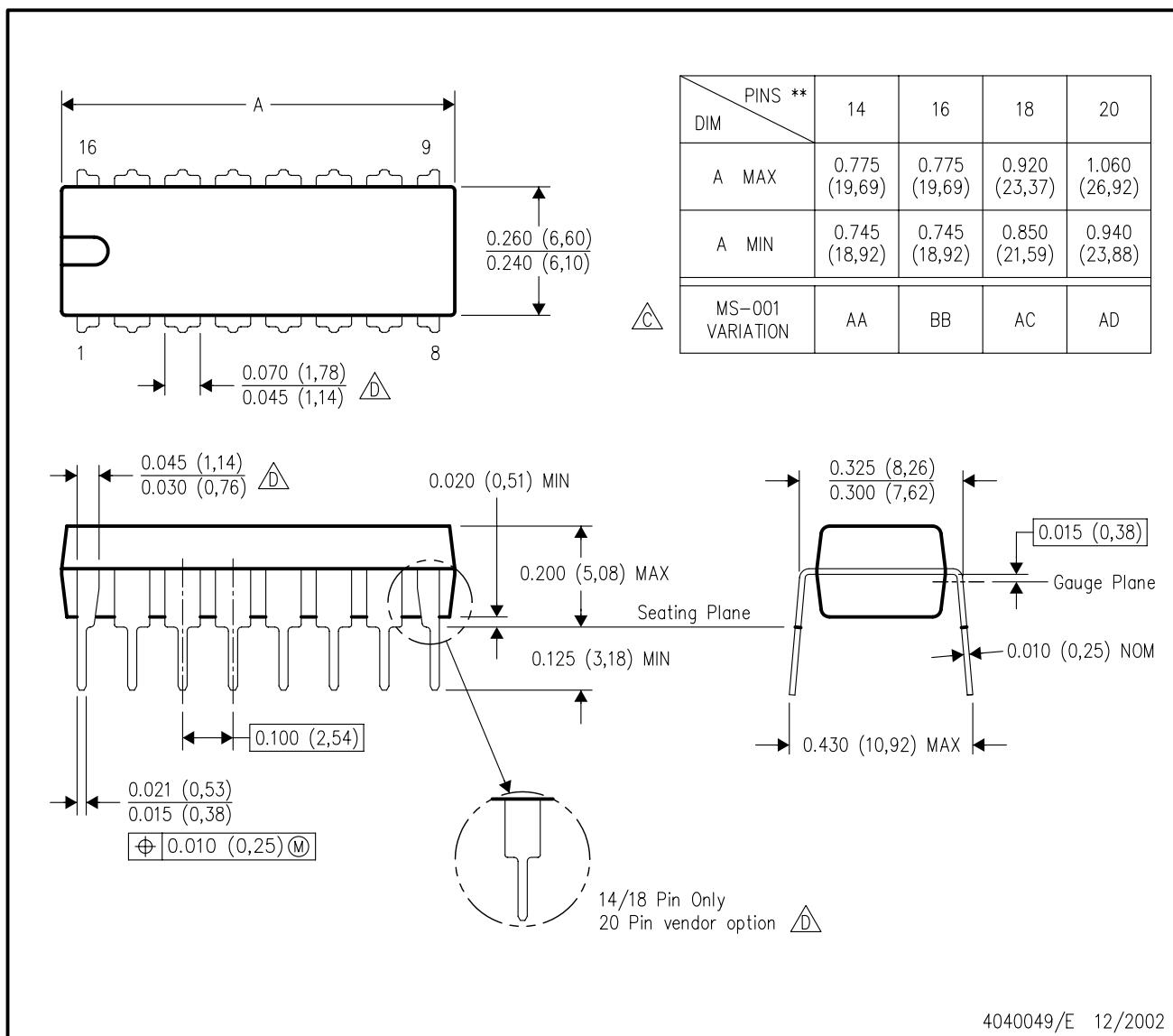
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

Symbol C: Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

Symbol D: The 20 pin end lead shoulder width is a vendor option, either half or full width.

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