



SOC Design Lab10

BNN accelerator

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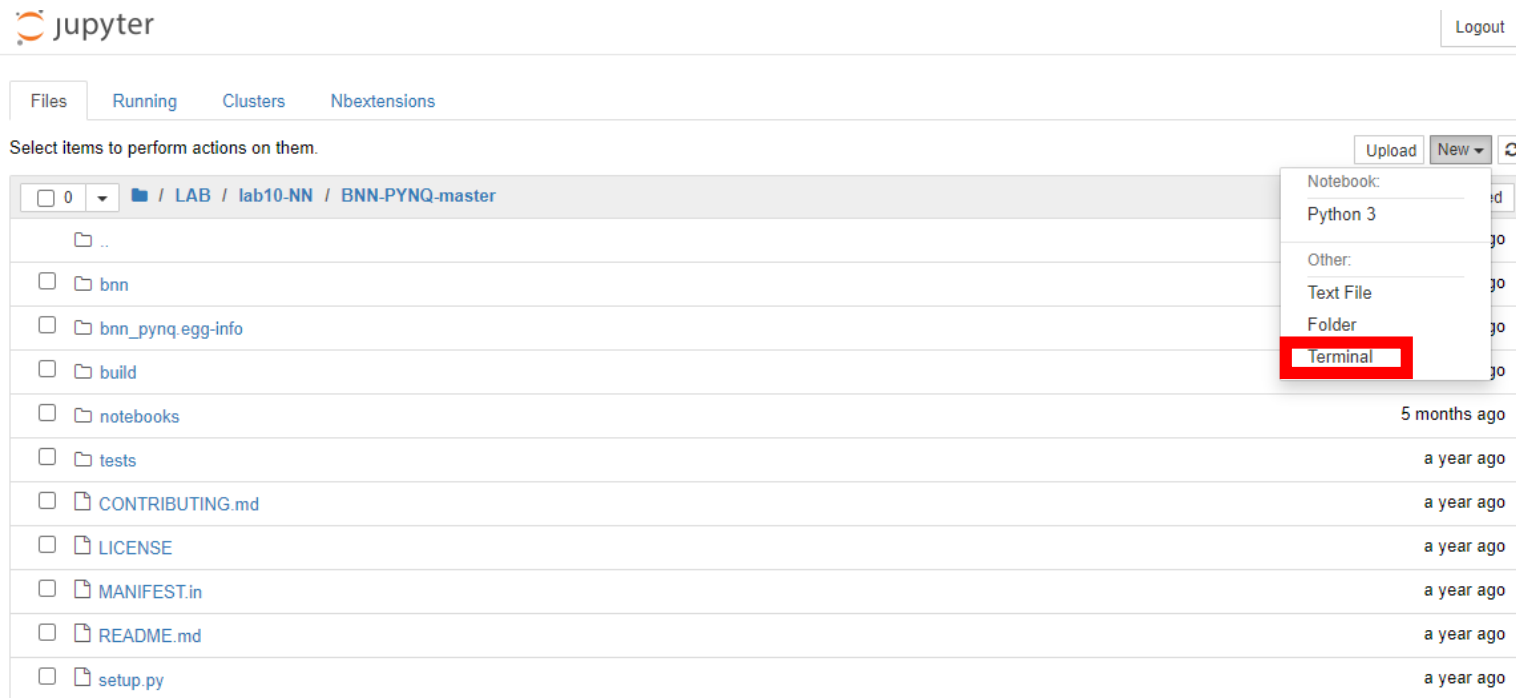
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Contents


- **BNN inference on PYNQ-Z2**
- **BNN Hardware design rebuilt**

- Download BNN-PYNQ master from <https://github.com/Xilinx/BNN-PYNQ>
- Clone the folder to the PYNQ
- Open the terminal



- `cd <your own clone path>`
- `python3 setup.py install`










- For inference , there are some examples provided from FINN paper (<https://arxiv.org/abs/1612.07119>)

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Files Running Clusters Nbextensions

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☐ 0 ▾ / LAB / lab10-NN / BNN-PYNQ-master / notebooks Name ▾ Last Modified

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<input type="checkbox"/> pictures	a year ago
<input type="checkbox"/>  CNV-BNN_Cifar10.ipynb	Running 5 months ago
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<input type="checkbox"/>  CNV-QNN_Cifar10.ipynb	a year ago
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<input type="checkbox"/>  CNV-QNN_Cifar10_Webcam.ipynb	a year ago
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For hardware design rebuilt

- You must follow the steps on **LINUX** operating system
- You must install Vivado 2018.2 on Linux

Hardware design rebuilt

- 設置臨時的环境變量
- `PATH=$PATH:/opt/Xilinx/Vivado/2018.2/bin`
`XILINX_BNN_ROOT=$XILINX_BNN_ROOT:/home/yourname/bnn/BNN-PYNQ-master/bnn/src/`



Launch the shell script make-hw.sh with passing parameters for target network, target platform and mode, with the command

./make-hw.sh {network} {platform} {mode}

where:

- **network** can be cnvW1A1, cnvW1A2, cnvW2A2 or lfcW1A1, lfcW1A2;
- **platform** can be pynqZ1-Z2 or ultra96;
- **mode** can be _h to launch Vivado HLS synthesis, _b to launch the Vivado project (needs HLS synthesis results), _a to launch both;

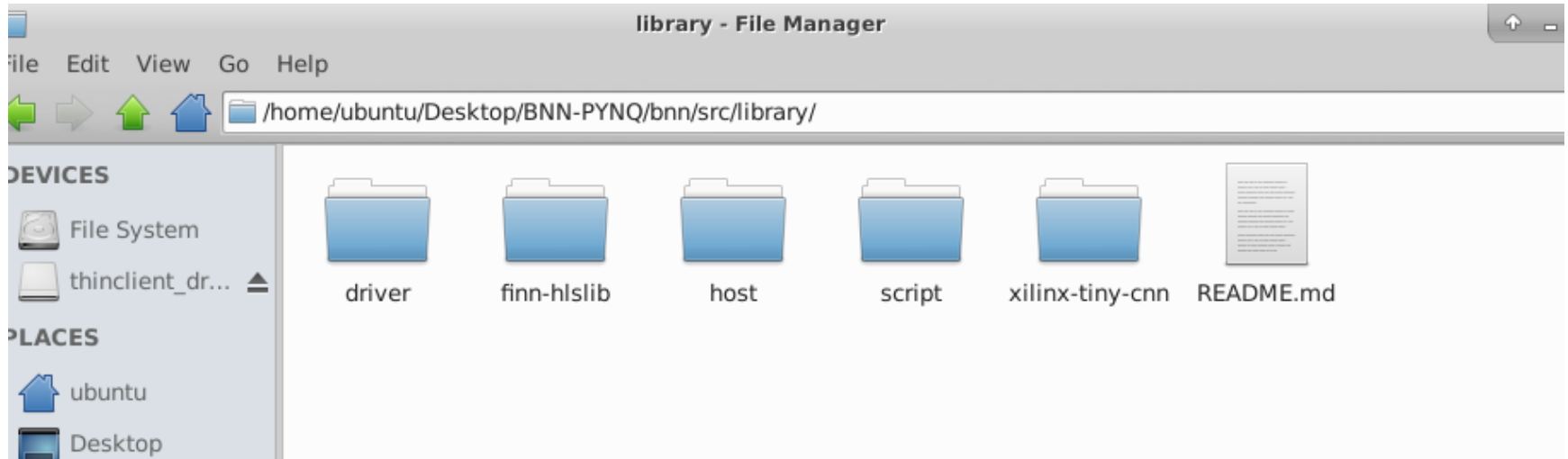
生成HLS IP

./make-hw.sh cnvW1A1 pynqZ1-Z2 h

生成vivado專案

./make-hw.sh cnvW1A1 pynqZ1-Z2 b

- **make-hw.sh script**中仍缺失了兩個檔案，**ubuntu**下**git**也很容易失敗，建議在**windows**上下載好兩個檔案放在指定路徑即可。將**xilinx-tiny-cnn**放在**BNN-PYNQ-master/bnn/src**文件夾下，將**finn-hlslib**放在**BNN-PYNQ-master/bnn/src/library**文件夾下。



xilinx-tiny-cnn

<https://github.com/Xilinx/xilinx-tiny-cnn>

finn-hlslib

<https://github.com/Xilinx/finn-hlslib/tree/8b7f5f5dcd4e3dd17eddc41253040931af28179a>

生成專案

cnvW1A1-pynqZ1-Z2 - [/home/ubuntu/Desktop/BNN-PYNQ/bnn/src/network/output/vivado/cnvW1A1-pynqZ1-Z2/cnvW1A1-pynqZ1-Z2.xpr] - Vivado 2018.2

Window Layout View Help Quick Access

write_bitstream Complete ✓

Default Layout

BLOCK DESIGN - procsys

Sources Design x Signals ? □ □ □

- Interface Connections
- Nets
- axi_mem_intercon
- BlackBoxjam_0 (Blackboxjam:1.0)
 - m_axi_hostmem
 - s_axi_control
 - ap_clk
 - ap_rst_n
 - interrupt
- ps7 (ZYNQ7 Processing System:5.5)
- ps7_axi_periph
- rst_ps7_100M (Processor System Reset:5.0)

Block Properties ? □ □ □ □

BlackBoxjam_0

License: included

Change Log: [View Change Log](#)

Vendor: Xilinx, Inc.

VLNV: xilinx.com:hls:BlackBoxjam:1.0

Repository: /home/ubuntu/Desktop/BNN-PYNQ/bnn/src/

General Properties IP

Diagram x Address Editor x ? □ □ □

The diagram illustrates the hardware architecture for a BlackBoxjam_0 IP block. It shows the following components and their interconnections:

- rst_ps7_100M (Processor System Reset):** Provides reset signals to the system.
- ps7_axi_periph (AXI Interconnect):** Acts as a bridge between the BlackBoxjam_0 IP and the ZYNQ7 Processing System.
- axi_mem_intercon (AXI Interconnect):** Manages memory access between the BlackBoxjam_0 IP and the ZYNQ7 Processing System.
- BlackBoxjam_0 (Blackboxjam:1.0):** The main IP block, which includes an **m_axi_hostmem** block and an **interrupt** signal.
- ps7 (ZYNQ7 Processing System):** The target hardware, including DDR, FIXED_IO, USB0_0, M_AXI_GPO, FCLK_CLK0, FCLK_CLK1, FCLK_CLK2, FCLK_CLK3, and FCLK_RESET0_N.

Key signals and connections include:

- Control Signals:** `s_axi_control` (AWADDR[6:0], AWVALID, AWREADY, WSTRB[3:0], WVALID, WREADY, BRESP[1:0], BVALID, BREADY, LARADDR[6:0], LARREADY, LRDATA[31:0], LRREADY, RVALID, RREADY).
- Interrupt:** `interrupt` signal from the BlackBoxjam_0 IP to the ZYNQ7 Processing System.
- Memory:** `m_axi_hostmem` block within the BlackBoxjam_0 IP.
- AXI Interconnects:** `ps7_axi_periph` and `axi_mem_intercon` blocks.
- Reset:** `rst_ps7_100M` block.