Sa se genereze simultan pe RB0 si RB1 doua semnale PWM cu factor de umplere 25% respectiv 75%. T=1ms, f=4MHz

```
tema4n - MPLAB IDE v8.70 - [C:\Users\Paula\Desktop\tema4.asm]
File Edit View Project Debugger Programmer
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                                                 Debug
         #include pl6f84.inc
         n equ 0x20
         i equ 0x21
         main:
               MOVLW D'10'
               MOVWF n
               BSF STATUS, RPO
               MOVLW B'111111100'
               MOVWF TRISE; RBO, RB1 output
               BCF STATUS, RP0
         semnal:
              BSF PORTE, RB0
              BSF PORTE, RB1
              CALL delay_250us
              BCF PORTB, RB0
               CALL delay_250us
               CALL delay_250us
               BCF PORTE, RB1
               CALL delay 250us
               DECFSZ n, 1
                 GOTO semnal
              NOP
         delay_250us:
             MOVLW D'81'
             MOVWF i
             loop:
                 DECFSZ i, 1
                     goto loop
                 NOP
                 return
                 end
```

