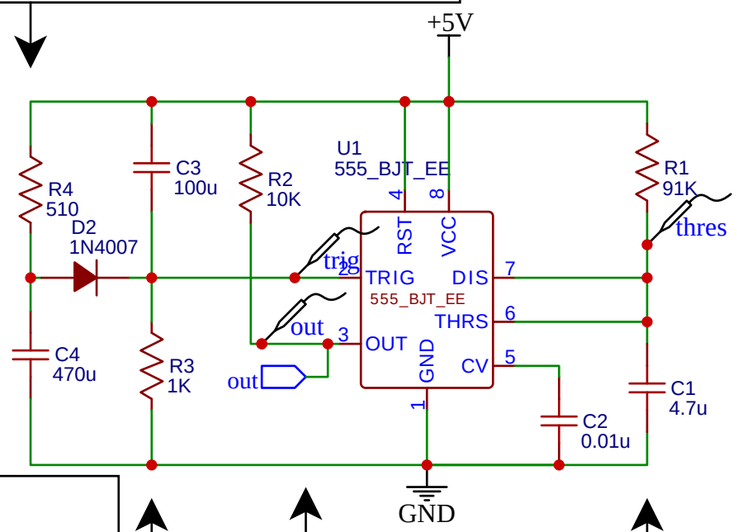
* Trst = 1.1*R4*C4
* Trst > Ttrig
* delay to resetting TRIG
* C4 charges to provide the high value for TRIG
  (in order for the pulse to stop after THRS becomes high as well)



* Ttrig = 1.1*R3*C3
* delay to triggering the pulse
* C3 discharges to provide the
  negative going pulse for TRIG (<1/3)

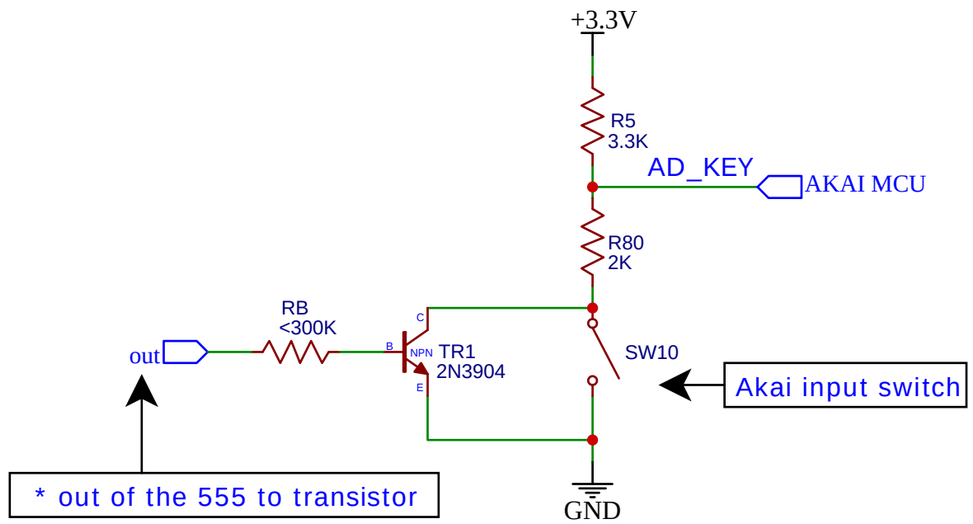
* out to transistor driving the load

* Ton = 1.1*R1*C1
* pulse on-time

.tran 0 2s 0 10ms startup

* startup needed to proper simulate real-life initial conditions

TITLE: Delayed, single-pulse 555 timer (monostable)	REV: 1.0
EasyEDA	Company: Your Company / Sheet: 1/1
	Date: 2020-09-19 Drawn By: Paul Barbu Gheorghe



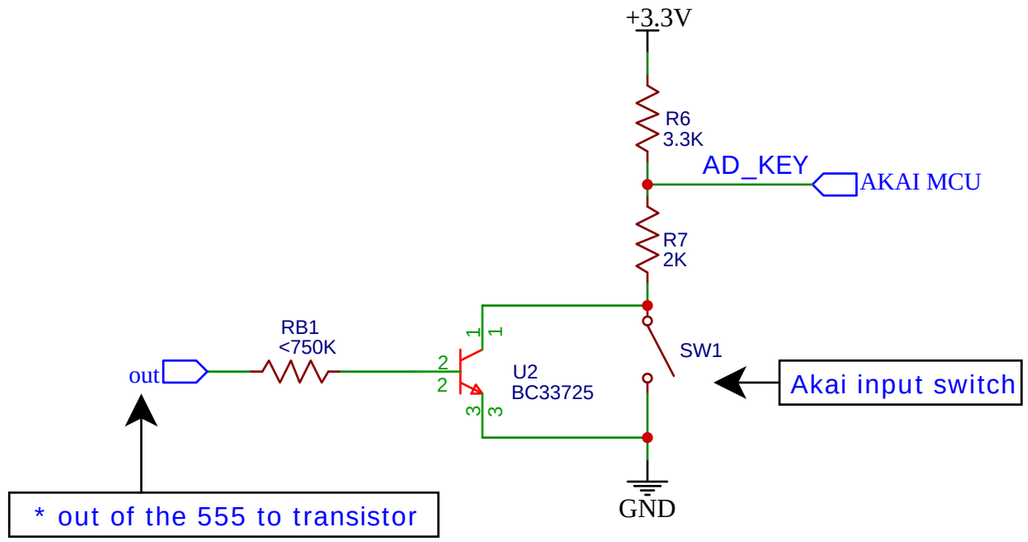
TITLE:
Output stage of the delayed pulse with 2N3904 transistor

REV: 1.0

Company: Your Company

Sheet: 1/1

Date: 2020-09-20 Drawn By: Paul Barbu Gheorghe



TITLE: Output stage of the delayed pulse with BC337 transistor		REV: 1.0
EasyEDA	Company: Your Company	Sheet: 1/1
	Date: 2020-09-20 Drawn By: Paul Barbu Gheorghe	