Data Sheet

S6B33BC

132 RGB Segment & 162 Common Driver For 65K Color STN LCD

June. 2. 2005
Ver. 0.3

System LSI Division
Semiconductor Business
SAMSUNG ELECTRONICS CO., LTD.

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

CONTENTS

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INTRODUCTION

S6B33BC is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip CR oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 162 output) corresponding to the display data and the internal bit-map display RAM of 132 ×162 ×19-bit, S6B33BC is capable of operating max. 132 RGB x 162 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 19-bit data and S6B33BC can display max 65,536 color out of 524,288 color palettes.

FEATURES

Driver Output

−   132 RGB x 162

Gray Scale Function

−   65,536 color display of R: 32 gray scale, G: 64 gray scale, B: 32 gray scale (using gamma correction with 524k palettes)
−   4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale
−   256 color display of R: 8 gray scale, G: 8 gray scale, B: 4 gray scale

On-chip Display Data RAM

−   Capacity: 132 x 19 x 162 = 406.296 kbits

Display Mode

−   Normal display mode: Entire duty displaying, Partial display mode: Partial duty displaying
−   Area scroll mode: Particular area scrolling, Standby mode: Internal display clocks off

Microprocessor Interface

−   8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
−   3/4 Pin SPI (only write operation)

On-chip Low Power Analog Circuit

−   On-chip CR oscillator (Internal cap. & external resistor), external clock available
−   Voltage converter / Voltage regulator / Voltage follower
−   On-chip electronic contrast control (256 steps)

Operating Voltage Range

−   VDD = 1.65 to 1.95 [V] (Typical 1.8 [V])
−   VDD3 = 1.65 to 3.3[V]
    When VDD3 = 1.65 to 1.95 [V], VDD = VDD3 (No using Internal Regulator, REG_ENB = 〝 VDD3〞)
    When VDD3 > 1.95 [V], VDD = REG_OUT (Using Internal Regulator, REG_ENB = 〝 VSS〞)
−   VIN1 = 2.4 ~ 3.6 [V]
−   Display operating voltage (V1): 2.0 to 4.0 V
−   LCD Operating Voltage Range: Max. 20 V

Low Power Consumption

−   TBD μA Typ. (Refer to DC CHARACTERISTICS (2))

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Package Type

COG (Output Pad Pitch Min. 30 μm)

Special Features

−   Non-Volatile Memory (OTP) for V1 Calibration

BLOCK DIAGRAM
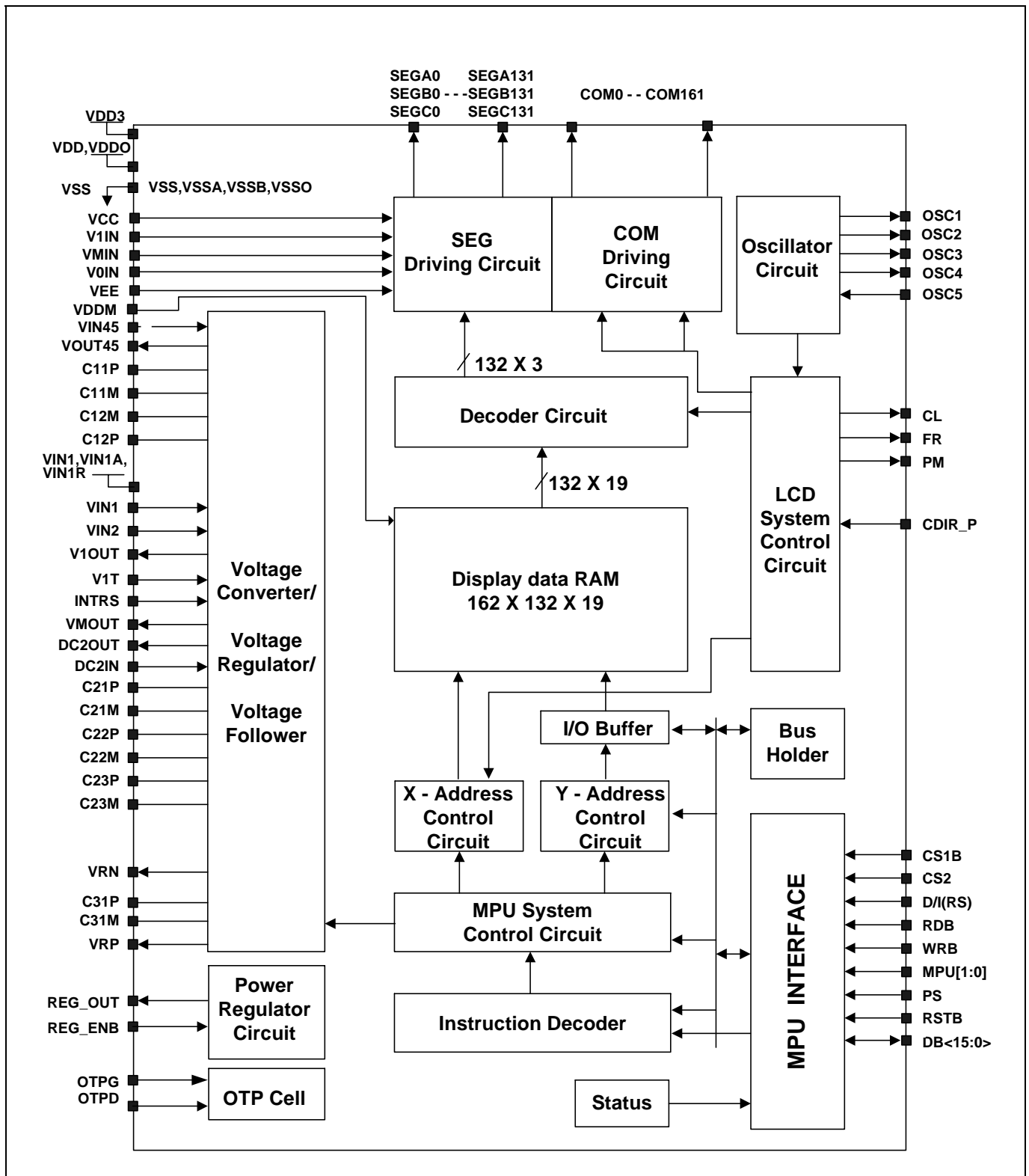
Figure 1. Block Diagram

PAD CONFIGURATION
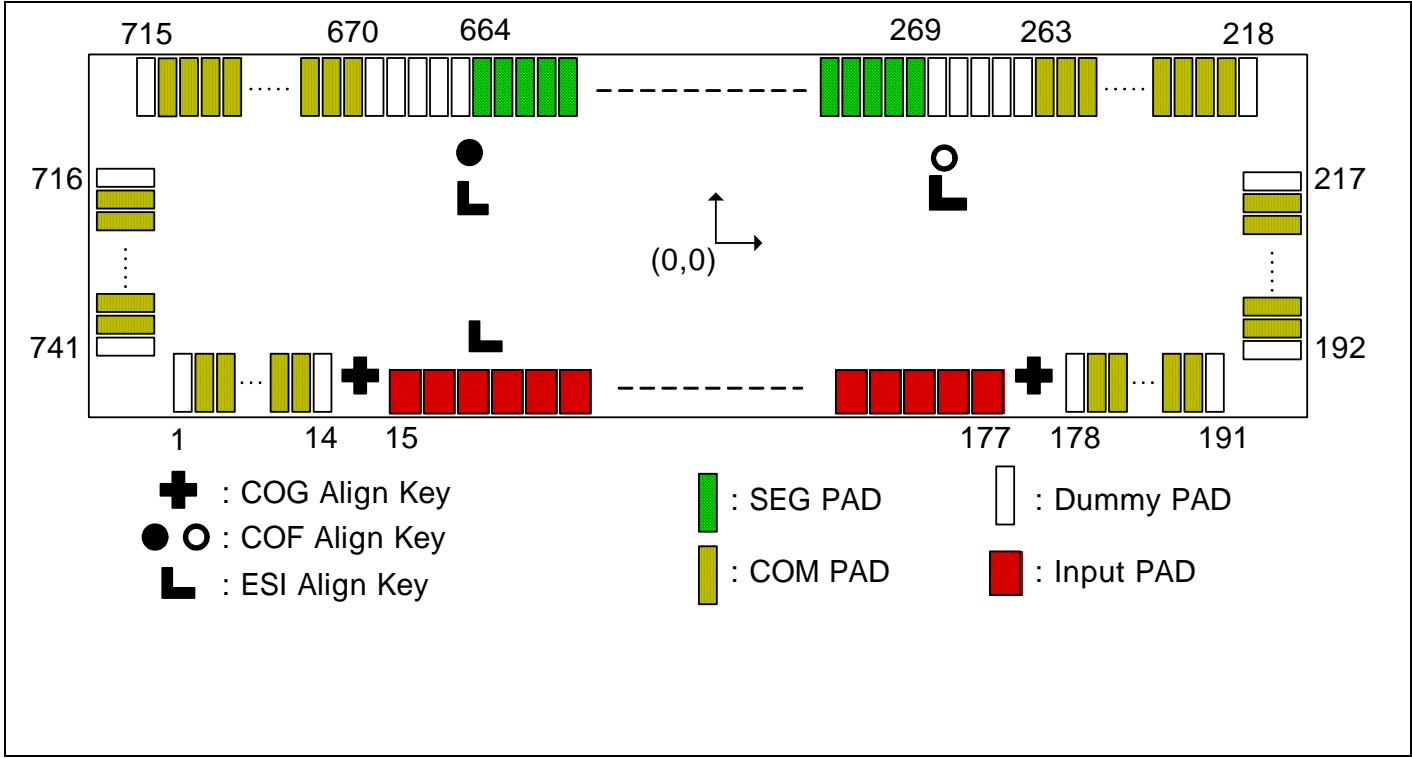
Figure 2. S6B33BC Chip Pad Configuration

Table 1. S6B33BC Pad Dimensions

Item	Pad No.	Size		Unit
		X	**Y**	
Chip size (with S/L 100μm)	-	15130	1260	μm
Pad pitch	15~79,96~177	80		μm
	80~95	100		
	1~14,178~741	30		
Top size of bumped pad	15~177	60	104	
	1~14,178~191,218~715	17	120	
	192~217, 716~741	120	17	
Bumped pad height	All Pad	17		

Figure 3. COG Align Key Coordinate

Figure 4. ESI Align Key Coordinate

Figure 5. COF Align Key Coordinate

PIN CONFIGURATION

Figure 6. S6B33BCX Chip Pin Configuration

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PAD Center Coordinates

Table 2. Pad Center Coordinates

[Unit: μm]

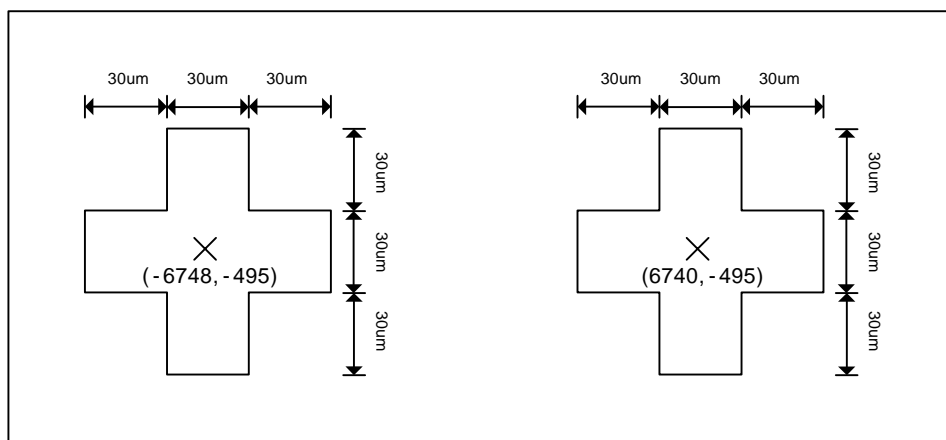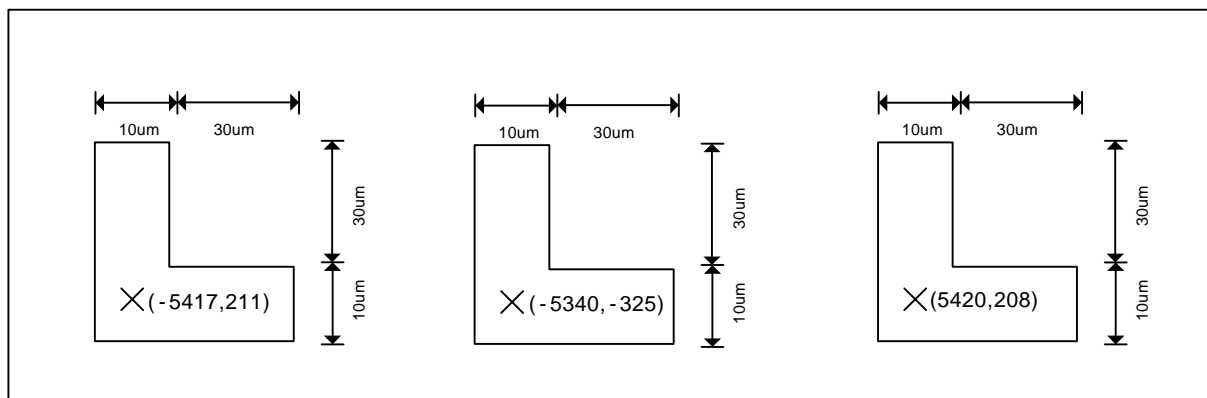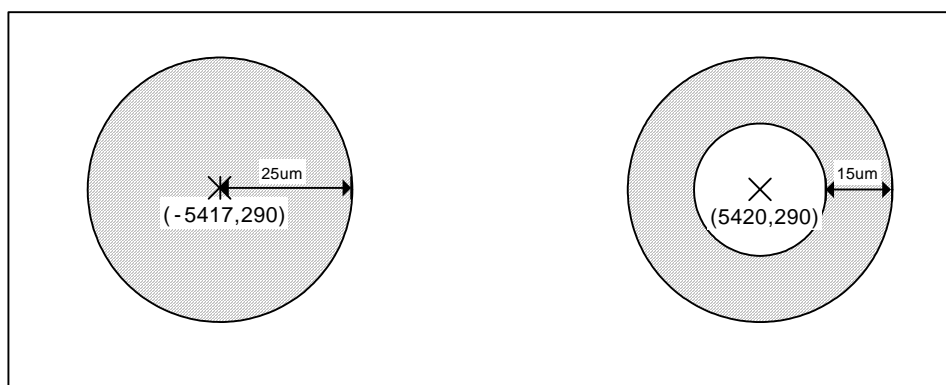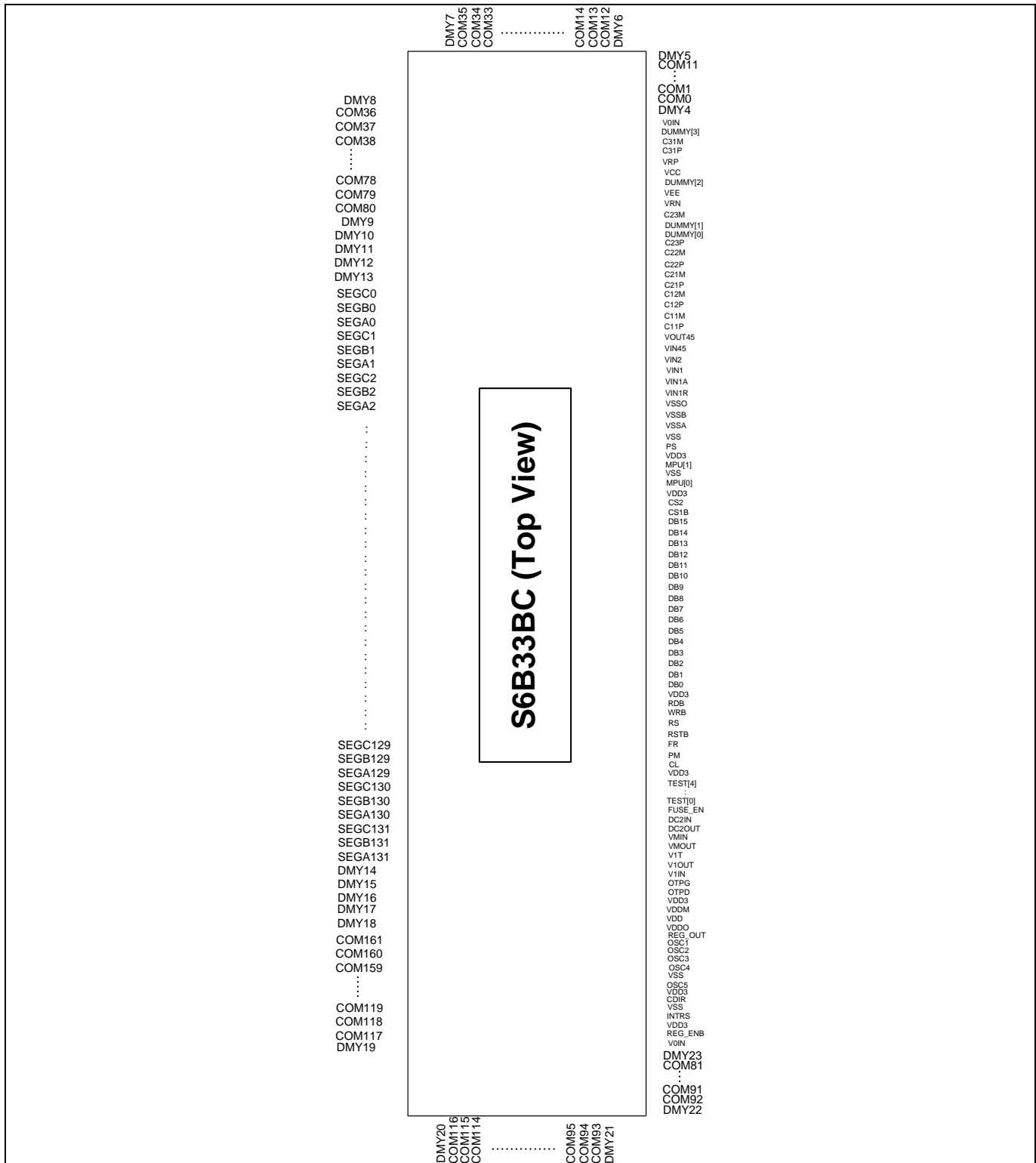| NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY<22>	-7305	-513	51	OTPG	-3760	-521	101	MPU<1>	560	-521
2	COM<92>	-7275	-513	52	V1IN	-3680	-521	102	VDD3	640	-521
3	COM<91>	-7245	-513	53	V1IN	-3600	-521	103	PS	720	-521
4	COM<90>	-7215	-513	54	V1OUT	-3520	-521	104	VSS	800	-521
5	COM<89>	-7185	-513	55	V1OUT	-3440	-521	105	VSS	880	-521
6	COM<88>	-7155	-513	56	V1T	-3360	-521	106	VSS	960	-521
7	COM<87>	-7125	-513	57	VMOUT	-3280	-521	107	VSS	1040	-521
8	COM<86>	-7095	-513	58	VMOUT	-3200	-521	108	VSS	1120	-521
9	COM<85>	-7065	-513	59	VMIN	-3120	-521	109	VSS	1200	-521
10	COM<84>	-7035	-513	60	VMIN	-3040	-521	110	VSSA	1280	-521
11	COM<83>	-7005	-513	61	DC2OUT	-2960	-521	111	VSSA	1360	-521
12	COM<82>	-6975	-513	62	DC2OUT	-2880	-521	112	VSSA	1440	-521
13	COM<81>	-6945	-513	63	DC2IN	-2800	-521	113	VSSB	1520	-521
14	DUMMY<23>	-6915	-513	64	DC2IN	-2720	-521	114	VSSB	1600	-521
15	VOIN	-6640	-521	65	FUSE_EN	-2640	-521	115	VSSB	1680	-521
16	REG_ENB	-6560	-521	66	TEST<0>	-2560	-521	116	VSSB	1760	-521
17	VDD3	-6480	-521	67	TEST<1>	-2480	-521	117	VSSB	1840	-521
18	INTRS	-6400	-521	68	TEST<2>	-2400	-521	118	VSSO	1920	-521
19	VSS	-6320	-521	69	TEST<3>	-2320	-521	119	VSSO	2000	-521
20	CDIR_P	-6240	-521	70	TEST<4>	-2240	-521	120	VIN1R	2080	-521
21	VDD3	-6160	-521	71	VDD3	-2160	-521	121	VIN1R	2160	-521
22	OSC5	-6080	-521	72	CL	-2080	-521	122	VIN1R	2240	-521
23	VSS	-6000	-521	73	PM	-2000	-521	123	VIN1A	2320	-521
24	OSC4	-5920	-521	74	FR	-1920	-521	124	VIN1A	2400	-521
25	OSC3	-5840	-521	75	RSTB	-1840	-521	125	VIN1A	2480	-521
26	OSC2	-5760	-521	76	RS	-1760	-521	126	VIN1	2560	-521
27	OSC1	-5680	-521	77	WRB	-1680	-521	127	VIN1	2640	-521
28	REG_OUT	-5600	-521	78	RDB	-1600	-521	128	VIN1	2720	-521
29	REG_OUT	-5520	-521	79	VDD3	-1520	-521	129	VIN1	2800	-521
30	VDDO	-5440	-521	80	DB<0>	-1440	-521	130	VIN1	2880	-521
31	VDDO	-5360	-521	81	DB<1>	-1340	-521	131	VIN2	2960	-521
32	VDD	-5280	-521	82	DB<2>	-1240	-521	132	VIN2	3040	-521
33	VDD	-5200	-521	83	DB<3>	-1140	-521	133	VIN45	3120	-521
34	VDD	-5120	-521	84	DB<4>	-1040	-521	134	VIN45	3200	-521
35	VDD	-5040	-521	85	DB<5>	-940	-521	135	VOUT45	3280	-521
36	VDDM	-4960	-521	86	DB<6>	-840	-521	136	VOUT45	3360	-521
37	VDDM	-4880	-521	87	DB<7>	-740	-521	137	C11P	3440	-521
38	VDDM	-4800	-521	88	DB<8>	-640	-521	138	C11P	3520	-521
39	VDDM	-4720	-521	89	DB<9>	-540	-521	139	C11M	3600	-521
40	VDD3	-4640	-521	90	DB<10>	-440	-521	140	C11M	3680	-521
41	VDD3	-4560	-521	91	DB<11>	-340	-521	141	C12P	3760	-521
42	VDD3	-4480	-521	92	DB<12>	-240	-521	142	C12P	3840	-521
43	VDD3	-4400	-521	93	DB<13>	-140	-521	143	C12M	3920	-521
44	OTPD	-4320	-521	94	DB<14>	-40	-521	144	C12M	4000	-521
45	OTPD	-4240	-521	95	DB<15>	60	-521	145	C21P	4080	-521
46	OTPD	-4160	-521	96	CS1B	160	-521	146	C21P	4160	-521
47	OTPD	-4080	-521	97	CS2	240	-521	147	C21M	4240	-521
48	OTPG	-4000	-521	98	VDD3	320	-521	148	C21M	4320	-521
49	OTPG	-3920	-521	99	MPU<0>	400	-521	149	C22P	4400	-521
50	OTPG	-3840	-521	100	VSS	480	-521	150	C22P	4480	-521

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Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	C22M	4560	-521	201	COM<20>	7448	-189	251	COM<68>	6465	513
152	C22M	4640	-521	202	COM<21>	7448	-159	252	COM<69>	6435	513
153	C23P	4720	-521	203	COM<22>	7448	-129	253	COM<70>	6405	513
154	C23P	4800	-521	204	COM<23>	7448	-99	254	COM<71>	6375	513
155	DUMMY<0>	4880	-521	205	COM<24>	7448	-69	255	COM<72>	6345	513
156	DUMMY<1>	4960	-521	206	COM<25>	7448	-39	256	COM<73>	6315	513
157	C23M	5040	-521	207	COM<26>	7448	-9	257	COM<74>	6285	513
158	C23M	5120	-521	208	COM<27>	7448	21	258	COM<75>	6255	513
159	VRN	5200	-521	209	COM<28>	7448	51	259	COM<76>	6225	513
160	VRN	5280	-521	210	COM<29>	7448	81	260	COM<77>	6195	513
161	VRN	5360	-521	211	COM<30>	7448	111	261	COM<78>	6165	513
162	VEE	5440	-521	212	COM<31>	7448	141	262	COM<79>	6135	513
163	VEE	5520	-521	213	COM<32>	7448	171	263	COM<80>	6105	513
164	VEE	5600	-521	214	COM<33>	7448	201	264	DUMMY<9>	6075	513
165	DUMMY<2>	5680	-521	215	COM<34>	7448	231	265	DUMMY<10>	6045	513
166	VCC	5760	-521	216	COM<35>	7448	261	266	DUMMY<11>	6015	513
167	VCC	5840	-521	217	DUMMY<7>	7448	291	267	DUMMY<12>	5985	513
168	VCC	5920	-521	218	DUMMY<8>	7455	513	268	DUMMY<13>	5955	513
169	VRP	6000	-521	219	COM<36>	7425	513	269	SEGC<0>	5925	513
170	VRP	6080	-521	220	COM<37>	7395	513	270	SEGB<0>	5895	513
171	VRP	6160	-521	221	COM<38>	7365	513	271	SEGA<0>	5865	513
172	C31P	6240	-521	222	COM<39>	7335	513	272	SEGC<1>	5835	513
173	C31P	6320	-521	223	COM<40>	7305	513	273	SEGB<1>	5805	513
174	C31M	6400	-521	224	COM<41>	7275	513	274	SEGA<1>	5775	513
175	C31M	6480	-521	225	COM<42>	7245	513	275	SEGC<2>	5745	513
176	DUMMY<3>	6560	-521	226	COM<43>	7215	513	276	SEGB<2>	5715	513
177	VOIN	6640	-521	227	COM<44>	7185	513	277	SEGA<2>	5685	513
178	DUMMY<4>	6915	-513	228	COM<45>	7155	513	278	SEGC<3>	5655	513
179	COM<0>	6945	-513	229	COM<46>	7125	513	279	SEGB<3>	5625	513
180	COM<1>	6975	-513	230	COM<47>	7095	513	280	SEGA<3>	5595	513
181	COM<2>	7005	-513	231	COM<48>	7065	513	281	SEGC<4>	5565	513
182	COM<3>	7035	-513	232	COM<49>	7035	513	282	SEGB<4>	5535	513
183	COM<4>	7065	-513	233	COM<50>	7005	513	283	SEGA<4>	5505	513
184	COM<5>	7095	-513	234	COM<51>	6975	513	284	SEGC<5>	5475	513
185	COM<6>	7125	-513	235	COM<52>	6945	513	285	SEGB<5>	5445	513
186	COM<7>	7155	-513	236	COM<53>	6915	513	286	SEGA<5>	5415	513
187	COM<8>	7185	-513	237	COM<54>	6885	513	287	SEGC<6>	5385	513
188	COM<9>	7215	-513	238	COM<55>	6855	513	288	SEGB<6>	5355	513
189	COM<10>	7245	-513	239	COM<56>	6825	513	289	SEGA<6>	5325	513
190	COM<11>	7275	-513	240	COM<57>	6795	513	290	SEGC<7>	5295	513
191	DUMMY<5>	7305	-513	241	COM<58>	6765	513	291	SEGB<7>	5265	513
192	DUMMY<6>	7448	-459	242	COM<59>	6735	513	292	SEGA<7>	5235	513
193	COM<12>	7448	-429	243	COM<60>	6705	513	293	SEGC<8>	5205	513
194	COM<13>	7448	-399	244	COM<61>	6675	513	294	SEGB<8>	5175	513
195	COM<14>	7448	-369	245	COM<62>	6645	513	295	SEGA<8>	5145	513
196	COM<15>	7448	-339	246	COM<63>	6615	513	296	SEGC<9>	5115	513
197	COM<16>	7448	-309	247	COM<64>	6585	513	297	SEGB<9>	5085	513
198	COM<17>	7448	-279	248	COM<65>	6555	513	298	SEGA<9>	5055	513
199	COM<18>	7448	-249	249	COM<66>	6525	513	299	SEGC<10>	5025	513
200	COM<19>	7448	-219	250	COM<67>	6495	513	300	SEGB<10>	4995	513

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Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
301	SEGA<10>	4965	513	351	SEGB<27>	3465	513	401	SEGC<44>	1965	513
302	SEGC<11>	4935	513	352	SEGA<27>	3435	513	402	SEGB<44>	1935	513
303	SEGB<11>	4905	513	353	SEGC<28>	3405	513	403	SEGA<44>	1905	513
304	SEGA<11>	4875	513	354	SEGB<28>	3375	513	404	SEGC<45>	1875	513
305	SEGC<12>	4845	513	355	SEGA<28>	3345	513	405	SEGB<45>	1845	513
306	SEGB<12>	4815	513	356	SEGC<29>	3315	513	406	SEGA<45>	1815	513
307	SEGA<12>	4785	513	357	SEGB<29>	3285	513	407	SEGC<46>	1785	513
308	SEGC<13>	4755	513	358	SEGA<29>	3255	513	408	SEGB<46>	1755	513
309	SEGB<13>	4725	513	359	SEGC<30>	3225	513	409	SEGA<46>	1725	513
310	SEGA<13>	4695	513	360	SEGB<30>	3195	513	410	SEGC<47>	1695	513
311	SEGC<14>	4665	513	361	SEGA<30>	3165	513	411	SEGB<47>	1665	513
312	SEGB<14>	4635	513	362	SEGC<31>	3135	513	412	SEGA<47>	1635	513
313	SEGA<14>	4605	513	363	SEGB<31>	3105	513	413	SEGC<48>	1605	513
314	SEGC<15>	4575	513	364	SEGA<31>	3075	513	414	SEGB<48>	1575	513
315	SEGB<15>	4545	513	365	SEGC<32>	3045	513	415	SEGA<48>	1545	513
316	SEGA<15>	4515	513	366	SEGB<32>	3015	513	416	SEGC<49>	1515	513
317	SEGC<16>	4485	513	367	SEGA<32>	2985	513	417	SEGB<49>	1485	513
318	SEGB<16>	4455	513	368	SEGC<33>	2955	513	418	SEGA<49>	1455	513
319	SEGA<16>	4425	513	369	SEGB<33>	2925	513	419	SEGC<50>	1425	513
320	SEGC<17>	4395	513	370	SEGA<33>	2895	513	420	SEGB<50>	1395	513
321	SEGB<17>	4365	513	371	SEGC<34>	2865	513	421	SEGA<50>	1365	513
322	SEGA<17>	4335	513	372	SEGB<34>	2835	513	422	SEGC<51>	1335	513
323	SEGC<18>	4305	513	373	SEGA<34>	2805	513	423	SEGB<51>	1305	513
324	SEGB<18>	4275	513	374	SEGC<35>	2775	513	424	SEGA<51>	1275	513
325	SEGA<18>	4245	513	375	SEGB<35>	2745	513	425	SEGC<52>	1245	513
326	SEGC<19>	4215	513	376	SEGA<35>	2715	513	426	SEGB<52>	1215	513
327	SEGB<19>	4185	513	377	SEGC<36>	2685	513	427	SEGA<52>	1185	513
328	SEGA<19>	4155	513	378	SEGB<36>	2655	513	428	SEGC<53>	1155	513
329	SEGC<20>	4125	513	379	SEGA<36>	2625	513	429	SEGB<53>	1125	513
330	SEGB<20>	4095	513	380	SEGC<37>	2595	513	430	SEGA<53>	1095	513
331	SEGA<20>	4065	513	381	SEGB<37>	2565	513	431	SEGC<54>	1065	513
332	SEGC<21>	4035	513	382	SEGA<37>	2535	513	432	SEGB<54>	1035	513
333	SEGB<21>	4005	513	383	SEGC<38>	2505	513	433	SEGA<54>	1005	513
334	SEGA<21>	3975	513	384	SEGB<38>	2475	513	434	SEGC<55>	975	513
335	SEGC<22>	3945	513	385	SEGA<38>	2445	513	435	SEGB<55>	945	513
336	SEGB<22>	3915	513	386	SEGC<39>	2415	513	436	SEGA<55>	915	513
337	SEGA<22>	3885	513	387	SEGB<39>	2385	513	437	SEGC<56>	885	513
338	SEGC<23>	3855	513	388	SEGA<39>	2355	513	438	SEGB<56>	855	513
339	SEGB<23>	3825	513	389	SEGC<40>	2325	513	439	SEGA<56>	825	513
340	SEGA<23>	3795	513	390	SEGB<40>	2295	513	440	SEGC<57>	795	513
341	SEGC<24>	3765	513	391	SEGA<40>	2265	513	441	SEGB<57>	765	513
342	SEGB<24>	3735	513	392	SEGC<41>	2235	513	442	SEGA<57>	735	513
343	SEGA<24>	3705	513	393	SEGB<41>	2205	513	443	SEGC<58>	705	513
344	SEGC<25>	3675	513	394	SEGA<41>	2175	513	444	SEGB<58>	675	513
345	SEGB<25>	3645	513	395	SEGC<42>	2145	513	445	SEGA<58>	645	513
346	SEGA<25>	3615	513	396	SEGB<42>	2115	513	446	SEGC<59>	615	513
347	SEGC<26>	3585	513	397	SEGA<42>	2085	513	447	SEGB<59>	585	513
348	SEGB<26>	3555	513	398	SEGC<43>	2055	513	448	SEGA<59>	555	513
349	SEGA<26>	3525	513	399	SEGB<43>	2025	513	449	SEGC<60>	525	513
350	SEGC<27>	3495	513	400	SEGA<43>	1995	513	450	SEGB<60>	495	513

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Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
451	SEGA<60>	465	513	501	SEGB<77>	-1035	513	551	SEGC<94>	-2535	513
452	SEGC<61>	435	513	502	SEGA<77>	-1065	513	552	SEGB<94>	-2565	513
453	SEGB<61>	405	513	503	SEGC<78>	-1095	513	553	SEGA<94>	-2595	513
454	SEGA<61>	375	513	504	SEGB<78>	-1125	513	554	SEGC<95>	-2625	513
455	SEGC<62>	345	513	505	SEGA<78>	-1155	513	555	SEGB<95>	-2655	513
456	SEGB<62>	315	513	506	SEGC<79>	-1185	513	556	SEGA<95>	-2685	513
457	SEGA<62>	285	513	507	SEGB<79>	-1215	513	557	SEGC<96>	-2715	513
458	SEGC<63>	255	513	508	SEGA<79>	-1245	513	558	SEGB<96>	-2745	513
459	SEGB<63>	225	513	509	SEGC<80>	-1275	513	559	SEGA<96>	-2775	513
460	SEGA<63>	195	513	510	SEGB<80>	-1305	513	560	SEGC<97>	-2805	513
461	SEGC<64>	165	513	511	SEGA<80>	-1335	513	561	SEGB<97>	-2835	513
462	SEGB<64>	135	513	512	SEGC<81>	-1365	513	562	SEGA<97>	-2865	513
463	SEGA<64>	105	513	513	SEGB<81>	-1395	513	563	SEGC<98>	-2895	513
464	SEGC<65>	75	513	514	SEGA<81>	-1425	513	564	SEGB<98>	-2925	513
465	SEGB<65>	45	513	515	SEGC<82>	-1455	513	565	SEGA<98>	-2955	513
466	SEGA<65>	15	513	516	SEGB<82>	-1485	513	566	SEGC<99>	-2985	513
467	SEGC<66>	-15	513	517	SEGA<82>	-1515	513	567	SEGB<99>	-3015	513
468	SEGB<66>	-45	513	518	SEGC<83>	-1545	513	568	SEGA<99>	-3045	513
469	SEGA<66>	-75	513	519	SEGB<83>	-1575	513	569	SEGC<100>	-3075	513
470	SEGC<67>	-105	513	520	SEGA<83>	-1605	513	570	SEGB<100>	-3105	513
471	SEGB<67>	-135	513	521	SEGC<84>	-1635	513	571	SEGA<100>	-3135	513
472	SEGA<67>	-165	513	522	SEGB<84>	-1665	513	572	SEGC<101>	-3165	513
473	SEGC<68>	-195	513	523	SEGA<84>	-1695	513	573	SEGB<101>	-3195	513
474	SEGB<68>	-225	513	524	SEGC<85>	-1725	513	574	SEGA<101>	-3225	513
475	SEGA<68>	-255	513	525	SEGB<85>	-1755	513	575	SEGC<102>	-3255	513
476	SEGC<69>	-285	513	526	SEGA<85>	-1785	513	576	SEGB<102>	-3285	513
477	SEGB<69>	-315	513	527	SEGC<86>	-1815	513	577	SEGA<102>	-3315	513
478	SEGA<69>	-345	513	528	SEGB<86>	-1845	513	578	SEGC<103>	-3345	513
479	SEGC<70>	-375	513	529	SEGA<86>	-1875	513	579	SEGB<103>	-3375	513
480	SEGB<70>	-405	513	530	SEGC<87>	-1905	513	580	SEGA<103>	-3405	513
481	SEGA<70>	-435	513	531	SEGB<87>	-1935	513	581	SEGC<104>	-3435	513
482	SEGC<71>	-465	513	532	SEGA<87>	-1965	513	582	SEGB<104>	-3465	513
483	SEGB<71>	-495	513	533	SEGC<88>	-1995	513	583	SEGA<104>	-3495	513
484	SEGA<71>	-525	513	534	SEGB<88>	-2025	513	584	SEGC<105>	-3525	513
485	SEGC<72>	-555	513	535	SEGA<88>	-2055	513	585	SEGB<105>	-3555	513
486	SEGB<72>	-585	513	536	SEGC<89>	-2085	513	586	SEGA<105>	-3585	513
487	SEGA<72>	-615	513	537	SEGB<89>	-2115	513	587	SEGC<106>	-3615	513
488	SEGC<73>	-645	513	538	SEGA<89>	-2145	513	588	SEGB<106>	-3645	513
489	SEGB<73>	-675	513	539	SEGC<90>	-2175	513	589	SEGA<106>	-3675	513
490	SEGA<73>	-705	513	540	SEGB<90>	-2205	513	590	SEGC<107>	-3705	513
491	SEGC<74>	-735	513	541	SEGA<90>	-2235	513	591	SEGB<107>	-3735	513
492	SEGB<74>	-765	513	542	SEGC<91>	-2265	513	592	SEGA<107>	-3765	513
493	SEGA<74>	-795	513	543	SEGB<91>	-2295	513	593	SEGC<108>	-3795	513
494	SEGC<75>	-825	513	544	SEGA<91>	-2325	513	594	SEGB<108>	-3825	513
495	SEGB<75>	-855	513	545	SEGC<92>	-2355	513	595	SEGA<108>	-3855	513
496	SEGA<75>	-885	513	546	SEGB<92>	-2385	513	596	SEGC<109>	-3885	513
497	SEGC<76>	-915	513	547	SEGA<92>	-2415	513	597	SEGB<109>	-3915	513
498	SEGB<76>	-945	513	548	SEGC<93>	-2445	513	598	SEGA<109>	-3945	513
499	SEGA<76>	-975	513	549	SEGB<93>	-2475	513	599	SEGC<110>	-3975	513
500	SEGC<77>	-1005	513	550	SEGA<93>	-2505	513	600	SEGB<110>	-4005	513

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Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
601	SEGA<110>	- 4035	513	651	SEGB<127>	- 5535	513	701	COM<130>	- 7035	513
602	SEGC<111>	- 4065	513	652	SEGA<127>	- 5565	513	702	COM<129>	- 7065	513
603	SEGB<111>	- 4095	513	653	SEGC<128>	- 5595	513	703	COM<128>	- 7095	513
604	SEGA<111>	- 4125	513	654	SEGB<128>	- 5625	513	704	COM<127>	- 7125	513
605	SEGC<112>	- 4155	513	655	SEGA<128>	- 5655	513	705	COM<126>	- 7155	513
606	SEGB<112>	- 4185	513	656	SEGC<129>	- 5685	513	706	COM<125>	- 7185	513
607	SEGA<112>	- 4215	513	657	SEGB<129>	- 5715	513	707	COM<124>	- 7215	513
608	SEGC<113>	- 4245	513	658	SEGA<129>	- 5745	513	708	COM<123>	- 7245	513
609	SEGB<113>	- 4275	513	659	SEGC<130>	- 5775	513	709	COM<122>	- 7275	513
610	SEGA<113>	- 4305	513	660	SEGB<130>	- 5805	513	710	COM<121>	- 7305	513
611	SEGC<114>	- 4335	513	661	SEGA<130>	- 5835	513	711	COM<120>	- 7335	513
612	SEGB<114>	- 4365	513	662	SEGC<131>	- 5865	513	712	COM<119>	- 7365	513
613	SEGA<114>	- 4395	513	663	SEGB<131>	- 5895	513	713	COM<118>	- 7395	513
614	SEGC<115>	- 4425	513	664	SEGA<131>	- 5925	513	714	COM<117>	- 7425	513
615	SEGB<115>	- 4455	513	665	DUMMY<14>	- 5955	513	715	DUMMY<19>	- 7455	513
616	SEGA<115>	- 4485	513	666	DUMMY<15>	- 5985	513	716	DUMMY<20>	- 7448	291
617	SEGC<116>	- 4515	513	667	DUMMY<16>	- 6015	513	717	COM<116>	- 7448	261
618	SEGB<116>	- 4545	513	668	DUMMY<17>	- 6045	513	718	COM<115>	- 7448	231
619	SEGA<116>	- 4575	513	669	DUMMY<18>	- 6075	513	719	COM<114>	- 7448	201
620	SEGC<117>	- 4605	513	670	COM<161>	- 6105	513	720	COM<113>	- 7448	171
621	SEGB<117>	- 4635	513	671	COM<160>	- 6135	513	721	COM<112>	- 7448	141
622	SEGA<117>	- 4665	513	672	COM<159>	- 6165	513	722	COM<111>	- 7448	111
623	SEGC<118>	- 4695	513	673	COM<158>	- 6195	513	723	COM<110>	- 7448	81
624	SEGB<118>	- 4725	513	674	COM<157>	- 6225	513	724	COM<109>	- 7448	51
625	SEGA<118>	- 4755	513	675	COM<156>	- 6255	513	725	COM<108>	- 7448	21
626	SEGC<119>	- 4785	513	676	COM<155>	- 6285	513	726	COM<107>	- 7448	- 9
627	SEGB<119>	- 4815	513	677	COM<154>	- 6315	513	727	COM<106>	- 7448	- 39
628	SEGA<119>	- 4845	513	678	COM<153>	- 6345	513	728	COM<105>	- 7448	- 69
629	SEGC<120>	- 4875	513	679	COM<152>	- 6375	513	729	COM<104>	- 7448	- 99
630	SEGB<120>	- 4905	513	680	COM<151>	- 6405	513	730	COM<103>	- 7448	- 129
631	SEGA<120>	- 4935	513	681	COM<150>	- 6435	513	731	COM<102>	- 7448	- 159
632	SEGC<121>	- 4965	513	682	COM<149>	- 6465	513	732	COM<101>	- 7448	- 189
633	SEGB<121>	- 4995	513	683	COM<148>	- 6495	513	733	COM<100>	- 7448	- 219
634	SEGA<121>	- 5025	513	684	COM<147>	- 6525	513	734	COM<99>	- 7448	- 249
635	SEGC<122>	- 5055	513	685	COM<146>	- 6555	513	735	COM<98>	- 7448	- 279
636	SEGB<122>	- 5085	513	686	COM<145>	- 6585	513	736	COM<97>	- 7448	- 309
637	SEGA<122>	- 5115	513	687	COM<144>	- 6615	513	737	COM<96>	- 7448	- 339
638	SEGC<123>	- 5145	513	688	COM<143>	- 6645	513	738	COM<95>	- 7448	- 369
639	SEGB<123>	- 5175	513	689	COM<142>	- 6675	513	739	COM<94>	- 7448	- 399
640	SEGA<123>	- 5205	513	690	COM<141>	- 6705	513	740	COM<93>	- 7448	- 429
641	SEGC<124>	- 5235	513	691	COM<140>	- 6735	513	741	DUMMY<21>	- 7448	- 459
642	SEGB<124>	- 5265	513	692	COM<139>	- 6765	513				
643	SEGA<124>	- 5295	513	693	COM<138>	- 6795	513				
644	SEGC<125>	- 5325	513	694	COM<137>	- 6825	513				
645	SEGB<125>	- 5355	513	695	COM<136>	- 6855	513				
646	SEGA<125>	- 5385	513	696	COM<135>	- 6885	513				
647	SEGC<126>	- 5415	513	697	COM<134>	- 6915	513				
648	SEGB<126>	- 5445	513	698	COM<133>	- 6945	513				
649	SEGA<126>	- 5475	513	699	COM<132>	- 6975	513				
650	SEGC<127>	- 5505	513	700	COM<131>	- 7005	513				

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PIN DESCRIPTION

Table 3. Power Supply Pins

Name	I/O	Description
VDD3	Supply	I/O power supply. VDD3 is more than VDD.
VDD	Supply	Regulated power supply input pin for internal digital block. This pin is connected to REG_OUT outside the chip with stabilization capacitor. When the internal regulator is not used,VDD should be tied to external 1.8V directly.
VDDO	Supply	Internal oscillator power supply This pin is connected to VDD.
VDDM	Supply	Display Data RAM power supply, this pin is connected to VDD.
VSS VSSO VSSA VSSB	GND	Ground
V1IN / V1OUT	I / O	LCD segment high selected driving voltage input / output pin
VMIN / VMOUT	I / O	LCD common/segment non-selected driving voltage input / output pin
V0IN	I	LCD segment low selected driving voltage input pin
VCC / VRP	I / O	LCD common high selected driving voltage input / output pin
VEE / VRN	I / O	LCD common low selected driving voltage input / output pin The relationship between VCC, V1, VM, V0 and VEE: VCC > V1 > VM > V0(=VSS) > VEE (V1 - VM = VM – V0, VCC –VM = VM - VEE)
VIN1R	Supply	Internal regulator power supply This pin is connected to VIN1.
VIN1 VIN1A	I	Power supply for 1'st booster circuit and VM Amp
VIN2	I	Power supply for DC2-Amp
VOUT45	O	1'st booster output pin
VIN45	I	Power supply for V1. Connect to VOUT45 or VIN1
C11P C11M C12P C12M	O	External capacitor connection pins used for 1'st booster circuit
V1T	I	Thermistor resistor connection pin
INTRS	I	External resistor select pin for temperature compensation circuit - INTRS = L : External resistor mode, INTRS = H : Internal resistor mode
DC2IN	I	Power supply for 2'nd booster. Connect to DC2OUT pin
DC2OUT	O	Power output pin for 2'nd booster input
C21P C21M C22P C22M C23P C23M	O	External capacitor connection pins used for 2'nd booster circuit
C31P C31M	O	External capacitor connection pins used for 3'rd booster circuit
OTPG	I	Gate Voltage for OTP programming
OTPD	I	Drain Voltage for OTP programming

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Table 4. MPU Interface Pins

Name	I/O	Description				
RSTB	I	Reset input pin. When RSTB is "L", initialization is executed.				
PS MPU[1:0]	I	MPU interface select pin				
		PS	MPU[1]	MPU[0]	Description	
		H	L	L	8080-series 8bit interface	
		H	L	H	8080-series 16bit interface	
		H	H	L	6800-series 8bit interface	
		H	H	H	6800-series 16bit interface	
		L	L	X	3 pin SPI(Write only)	
		L	H	X	4 pin SPI(Write only)	
		NOTE : In serial mode, WRB and RDB must be fixed to either VDD3 or VSS.				
CS1B CS2	I	Chip select input pins Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0 to DB15 may be high impedance.				
D/I (RS)	I	Data / Instruction select input pin − D/I = "H": DB0 to DB15 are display data − D/I = "L": DB0 to DB7 are instruction data				
WRB (R/W)	I	Read / Write execution control pin				
		PS	MPU[1]	MPU Type	WRB	Description
		H	H	6800-series	R/W	Read / Write control input pin − R/W = "H": read − R/W = "L": write
		H	L	8080-series	WRB	Write enable clock input pin The data on DB0 to DB15 are latched at the rising edge of the WRB signal.
RDB (E)	I	Read / Write execution control pin				
		PS	MPU[1]	MPU type	RDB	Description
		H	H	6800-series	E	Read / Write control input pin − R/W = "H": When E is "H", DB0 to DB15 are in an output status. − R/W = "L": The data on DB0 to DB15 are latched at the falling edge of the E signal.
		H	L	8080-series	RDB	Read enable clock input pin When RDB is "L", DB0 to DB15 are in an output status.
DB[15:8] DB[7]/SDI DB[6]/SCL DB[5:0]	I/O	-DB[15:0]: 16-bit bi-directional data bus. -SDI: Serial data input pin. The data is latched at the rising edge of SCL. -SCL: Serial clock input pin. When these pins are not used according to mode, these pins must be connected to VDD3 or VSS				
CDIR_P	I	Common direction select pin.				

Table 5. Oscillator and Power Regulator Pins

Name	I/O	Description
OSC1 OSC2 OSC3 OSC4	I/O	CR oscillator output pin When the internal CR oscillator is used, connect to OSC1, OSC3 through a resistor. OSC1 – OSC2: Using in normal display mode, partial display mode 0 OSC3 – OSC4: Using in partial display mode 1 When an external oscillator is used, OSC1 pin is connected to VSS.
OSC5	I	External clock input pin When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD3 or VSS.
REG_ENB	I	Internal regulator enable/disable input pin - REG_ENB = "L" (tied to VSS) : enable internal regulator - REG_ENB = "H" (tied to VDD3) : disable internal regulator
REG_OUT	O	Internal voltage regulator output pin The regulator output port from this pin is used as a power supplier for an internal digital block via VDD pins.

Table 6. Timing signal Pins for monitoring

Name	I/O	Description
CL	O	Shift clock output pin
PM	O	Field delimiter output pin
FR	O	Liquid crystal alternating current output pin

Table 7. LCD driver output pins

Name	I/O	Description
SEGA0 to 131	O	LCD driving segment output (Red or Blue)
SEGB0 to 131	O	LCD driving segment output (Green)
SEGC0 to131	O	LCD driving segment output (Blue or Red)
COM0 to 161	O	LCD common outputs

Table 8. Test pins

Name	I/O	Description
TEST[4:0]	I	Don't use these pins. IC maker's test pins These pins must be tied to VDD3.
FUSE_EN	I	Don't use this pin. IC maker's test pin. This pin must be tied to VDD3.

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FUNCTIONAL DESCRIPTION

MPU INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B33BC can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, D/I, RDB, and WRB inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel/Serial Interface

The S6B33BC has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table9.

Table 9. Parallel / Serial Interface Mode.

PS	MPU[1]	CS1B	CS2	MPU bus type
H	L	CS1B	CS2	8080-Series MPU
	H			6800-Series MPU
L	L	CS1B	CS2	3–Pin SPI
	H			4-Pin SPI

Parallel Interface (PS="H")

The 8-bit/16-bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU[1] and the mode of data-bus is controlled by MPU[0] as shown in below. In accessing internal registers (D/I = "L"), only DB[7:0] are valid.

Table 10. Microprocessor Selection for Parallel Interface

MPU[1]	MPU[0]	CS1B	CS2	RDB	WRB	Data Bus	MPU bus type
L	L	CS1B	CS2	RDB	WRB	DB[7:0]	8080-series MPU
	H					DB[15:0]	
H	L	CS1B	CS2	E	R/W	DB[7:0]	6800-series MPU
	H					DB[15:0]	

Table 11. Parallel Data Transfer

D/I	6800-series		8080-series		Description
	RDB	WRB	RDB	WRB	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data
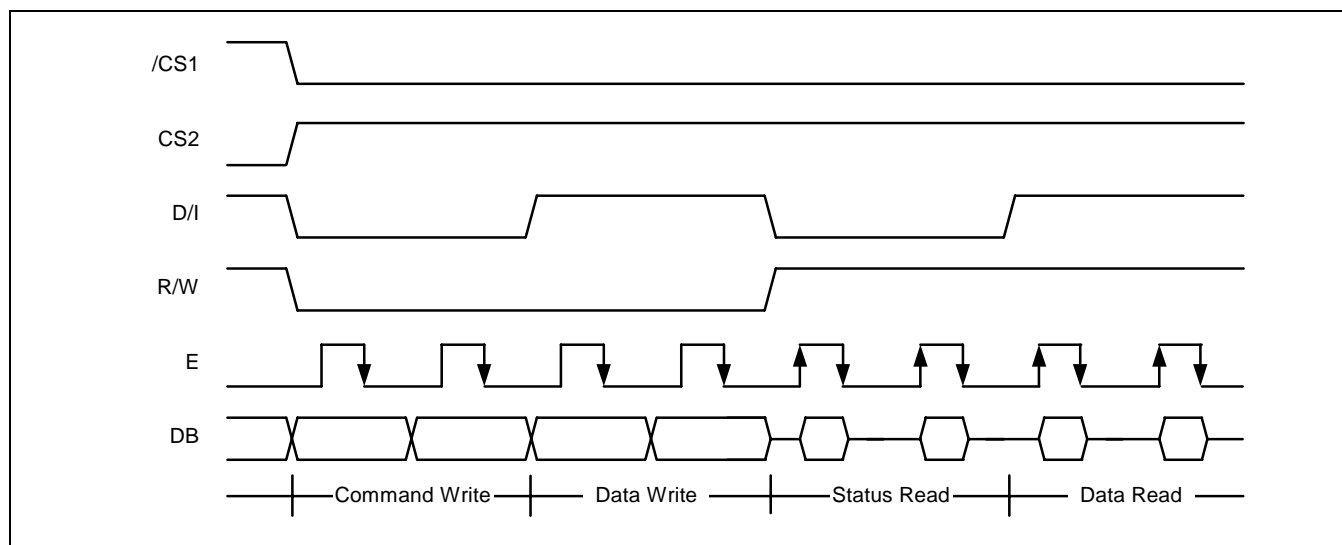
Figure 7.   6800-Series MPU Interface protocol (MPU[1]="H")
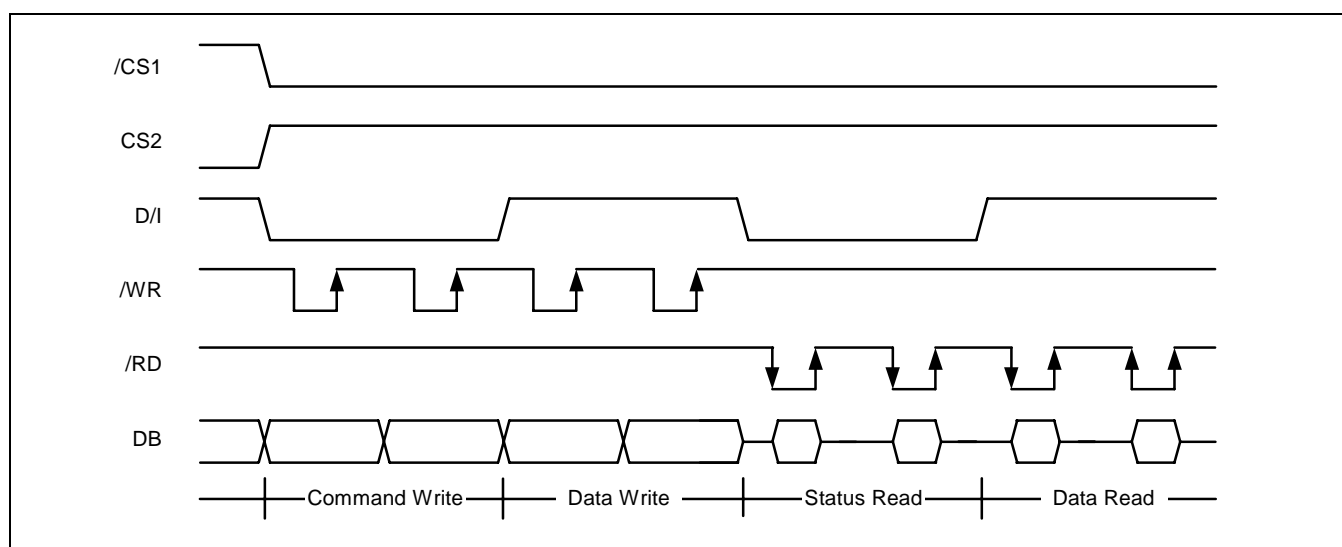
Figure 8.   8080-Series MPU Interface Protocol (MPU[1]="L")

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Serial Interface(PS="L")

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset.
The serial interface type is selected by setting PS as shown in Table12.

Table 12. Microprocessor Selection for Serial Interface

PS	MPU[1]	CS1B	CS2	D/I	Serial Data	Serial Clock	SPI Mode
L	L	CS1B	CS2	By S/W	DB[7]	DB[6]	3-Pin
	H	CS1B	CS2	D/I			4-Pin

3-Pin SPI Interface (PS = "L" & MPU[1] = "L")

In 3-Pin SPI Interface mode, the first bit of serial 9bits is used to indicate whether serial data input is display or instruction data instead of D/I pin. The serial data format consists of D/I (1bit) and DATA (8bits).   For details, refer the Figure 8.
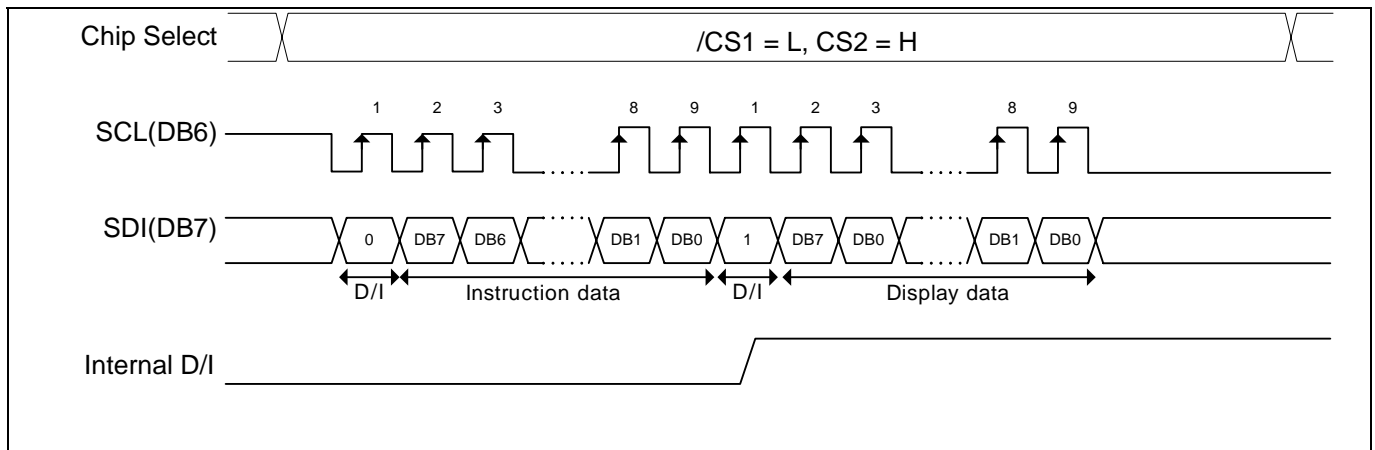
Figure 9. 3-Pin SPI Timing (D/I is not used)

4-Pin Serial Interface (PS="L" & MPU[1]="H")

In 4-pin SPI interface mode, D/I pin is used for indicating whether serial data input is display or instruction data. Data is display data when D/I is high and instruction data when D/I is low.
Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.
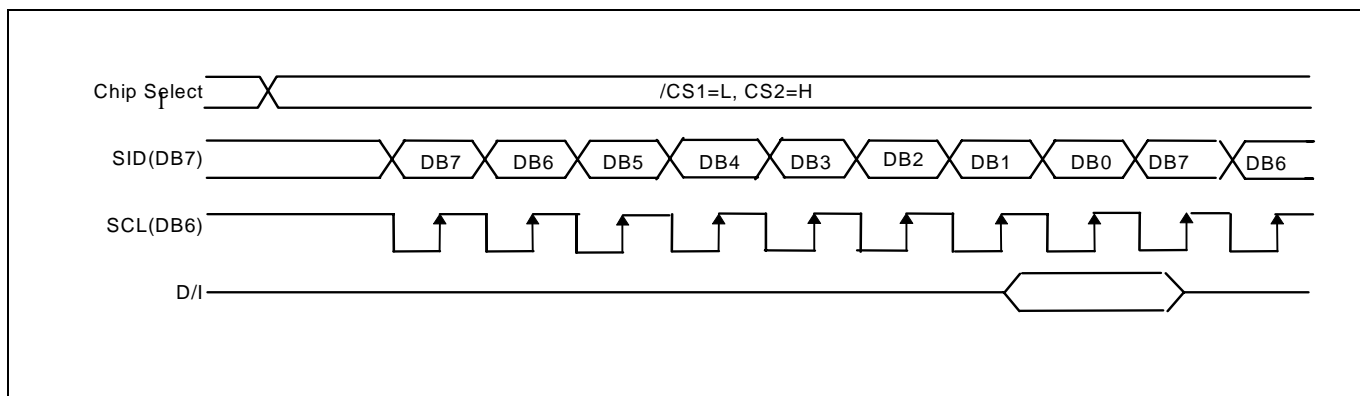
Figure 10. 4-Pin Serial Interface Timing

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DISPLAY DATA RAM

The on-chip display data RAM of S6B33BC is a static RAM that is stored the data for the display. It is a 132 x 19 x 162 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

DDRAM Address Area Selection

A part of DDRAM address area of S6B33BC can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.
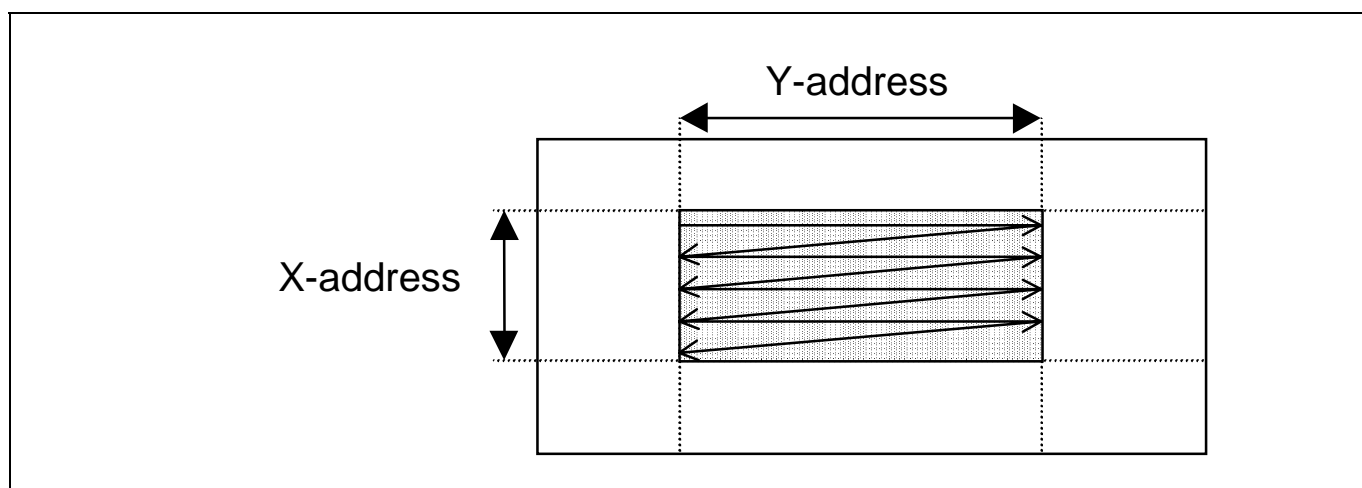
Figure 11. DDRAM Address Area

Table 13. X address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	0	0	0	1
P1	X start address set(Initial Status = 00H)							
P2	X end address set(Initial Status = A1H)							

Table 14. Y address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	1	0	0	0	1
P1	Y start address set (Initial status = 00H)							
P2	Y end address set (Initial status =83H)							

RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

Y address count mode (Y address = 00h to 83h, X address = 00h to A1h)

Figure 12. Y address count mode

X address count mode (Y address =00h to 83h, X address = 00h to A1h)

Figure 13. X address count mode

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XA
Address   00H 01H 02H 03H 04H 05H 06H 07H

00H
01H
02H
03H
04H
05H
06H
07H
08H
09H
0AH
0BH
0CH
0EH
0FH
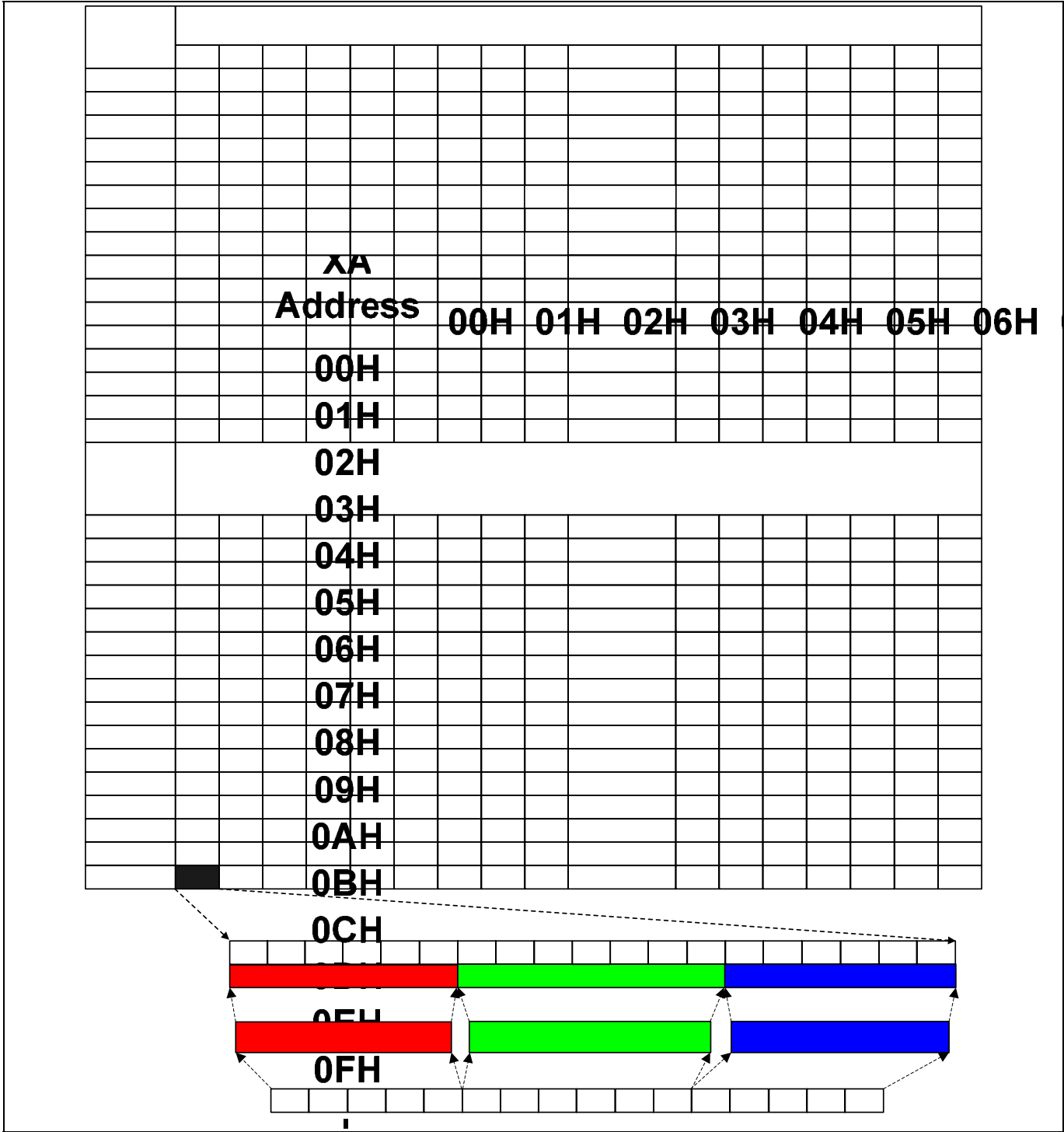
Figure 14. Display Data RAM Map

B2H
B3H
B4H
B5H
B6H
B7H

Partial Display Mode

The S6B33BC realizes the partial display function with low duty driving for saving power consumption and showing the various display duties. It is set as display start/end line number.

Area Scroll Function

The S6B33BC realizes the specific area scroll function. (1/162 duty case).
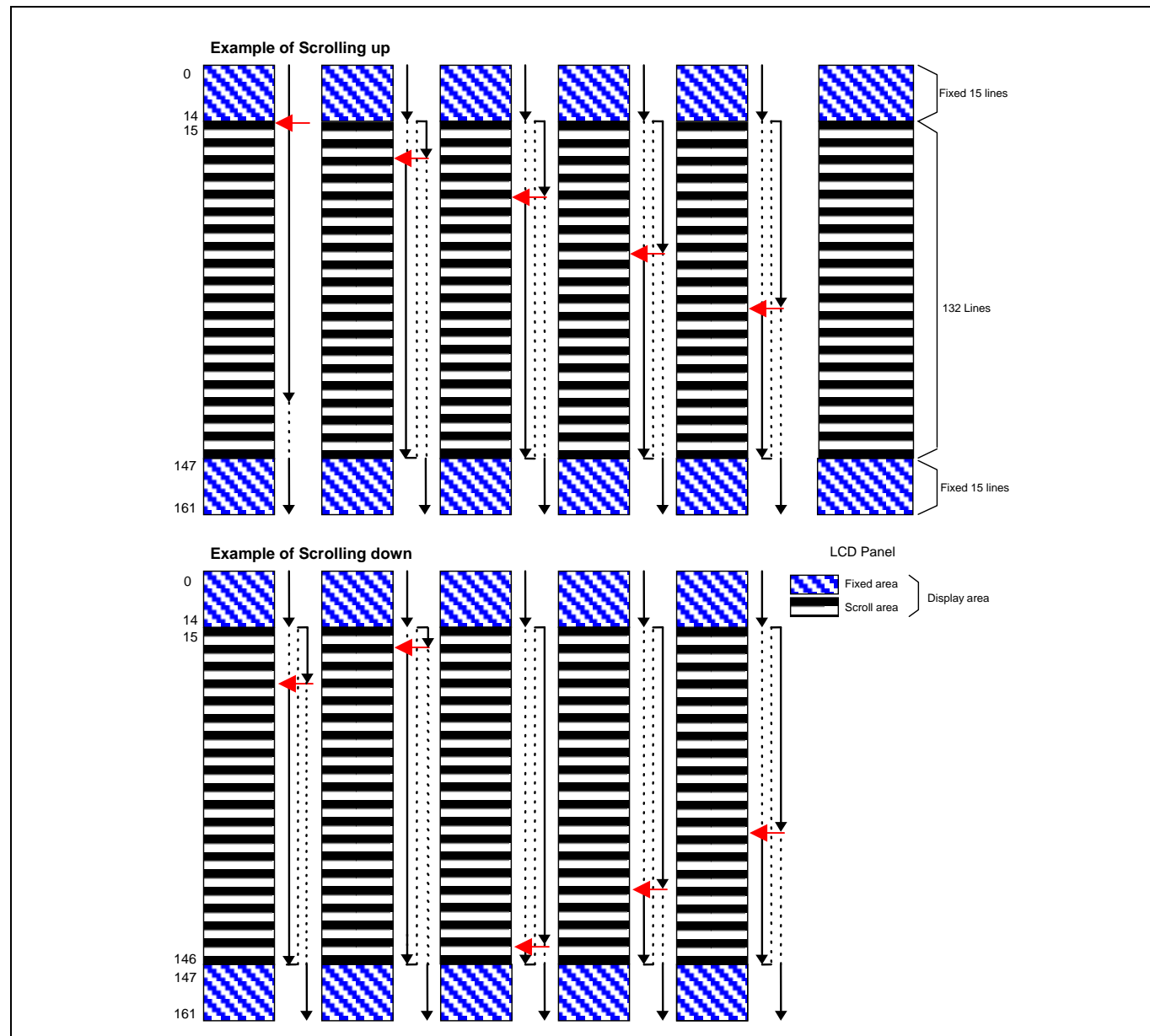
Figure 15. Area scroll examples (duty = 1/162, center scroll mode)

Display Direction

SDIR

   The SDIR flag of Driver Output Mode Set instruction selects the direction of segment display.
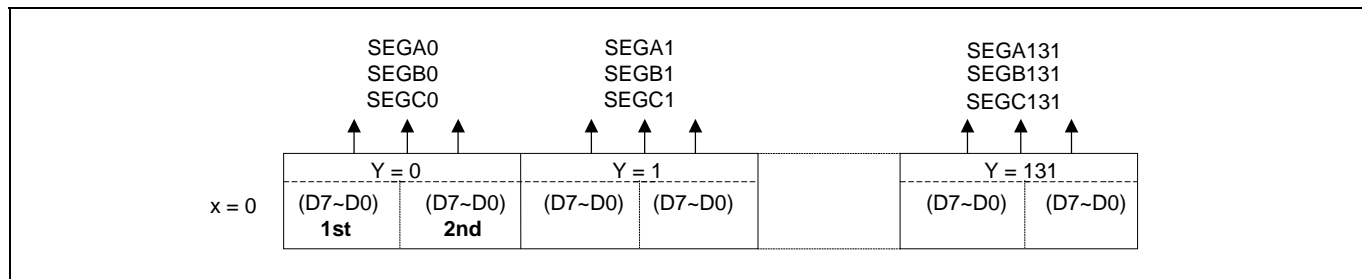
Figure 16. 8-bit data bus mode when SDIR = L
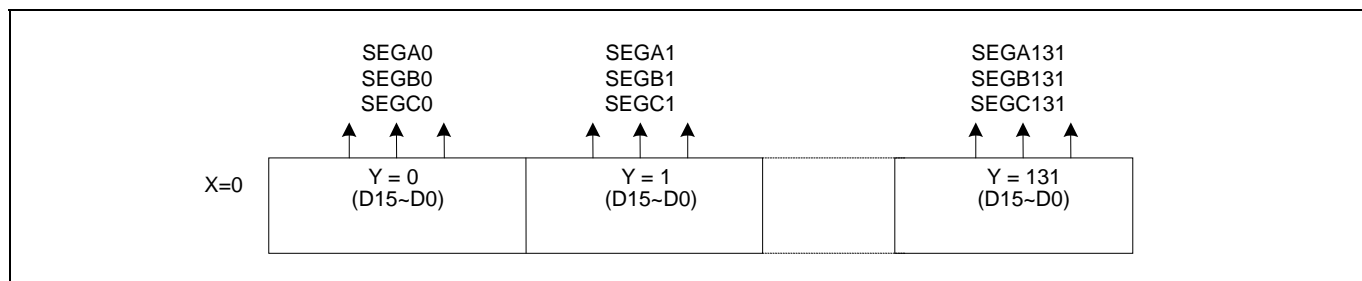
Figure 17. 16-bit data bus mode when SDIR = L
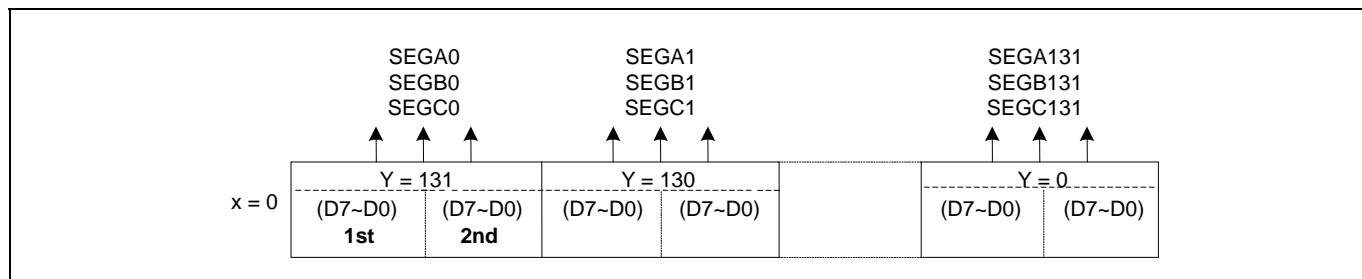
Figure 18. 8-bit data bus mode when SDIR = H
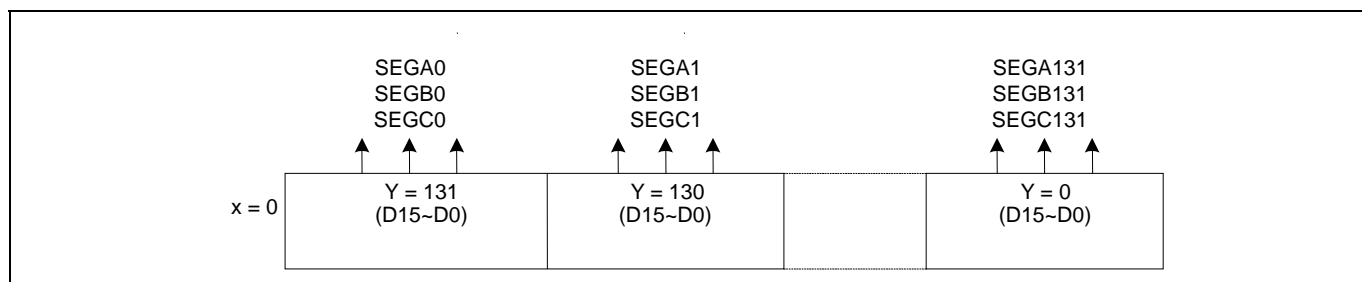
Figure 19. 16-bit data bus mode when SDIR = H

CDIR

The direction of common scanning is selected by CDIR register.

COM 161   SEG132   COM80

COM 81   **Driver**   COM0

132 Display Lines (DLN=00)

<CDIR=0>

COM 0
Display Area — Line number 0
COM 65 — Line number 65

COM 81
Display Area — Line number 66
COM 146 — Line number 131

<CDIR=1>

COM 0
Display Area — Line number 131
COM 65 — Line number 66

COM 81
Display Area — Line number 65
COM 146 — Line number 0

144 Display Lines (DLN=01)

<CDIR=0>

COM 0
Display Area — Line number 0
COM 71 — Line number 71

COM 81
Display Area — Line number 72
COM 152 — Line number 143

<CDIR=1>

COM 0
Display Area — Line number 143
COM 71 — Line number 72

COM 81
Display Area — Line number 71
COM 152 — Line number 0

162 Display Lines (DLN=10)

<CDIR=0>

COM 0 — Line number 0

Display Area

COM 161 — Line number 161

<CDIR=1>

COM 0 — Line number 161

Display Area

COM 161 — Line number 0

96 Display Lines (DLN=11)

<CDIR=0>

COM 0
Display Area — Line number 0
COM 47 — Line number 47

COM 81
Display Area — Line number 48
COM 128 — Line number 95

<CDIR=1>

COM 0
Display Area — Line number 95
COM 47 — Line number 48

COM 81
Display Area — Line number 47
COM 128 — Line number 0

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SWP

The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.
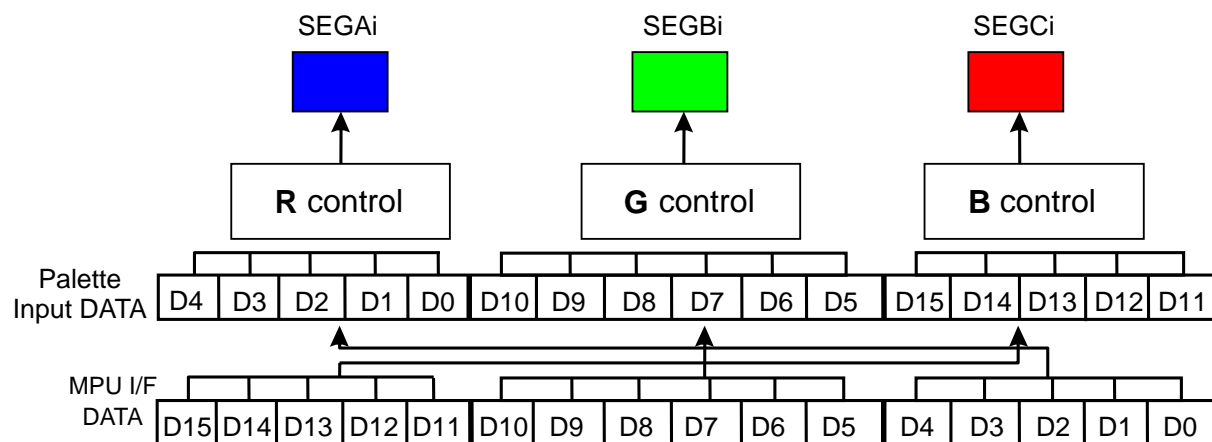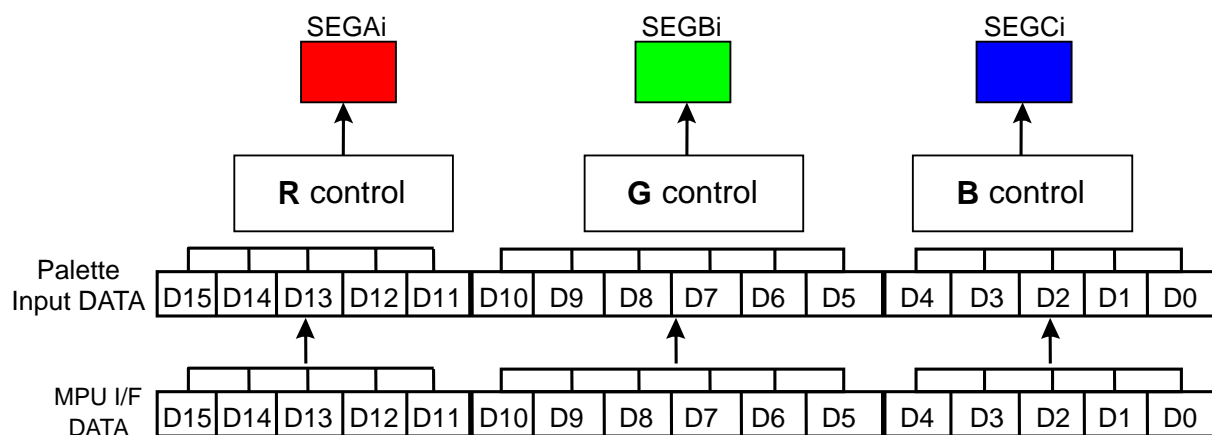
	SEGAi	**SEGBi**	**SEGCi**	
SWP = 0	RED	GREEN	BLUE	**Color**
	D15 ~ D11	D10~ D5	D4 ~ D0	**Assigned Bit**
SWP = 1	BLUE	GREEN	RED	**Color**
	D4~ D0	D10 ~ D5	D15 ~ D11	**Assigned Bit**

Figure 20. The relationship between SEG outputs and RGB color

On-Chip Regulator Configuration
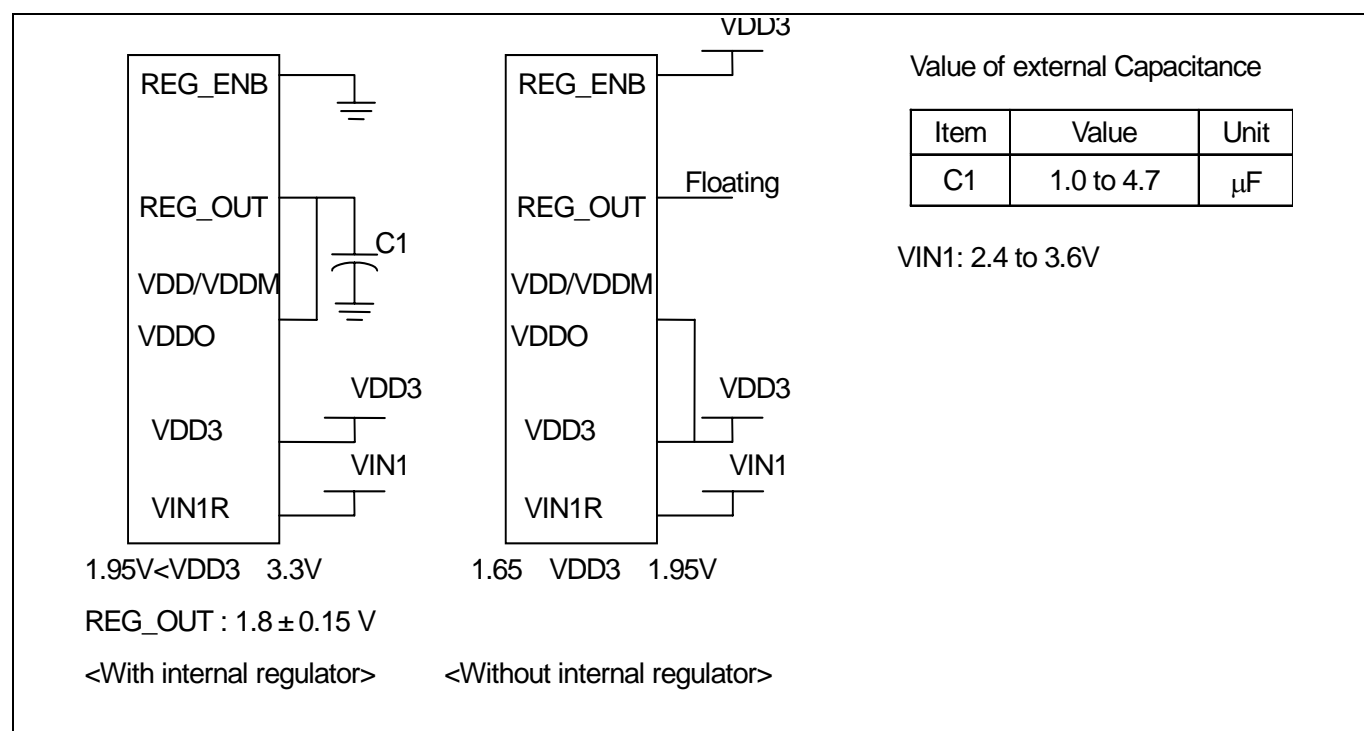
Figure 21. Regulator Application

Oscillator Circuit

When internal oscillator is used(EXT=0), the selection of oscillator resistor is determined by display mode.
- Normal display mode/ Partial display mode 0 : resistor1 between OSC1 and OSC2
- Partial display mode 1 : resistor2 between OSC3 and OSC4
-

Note : In R-C oscillator, the oscillation frequency is changed according to the external resistance value, ITO wire length, or operating power-supply voltage (VDDO).

When external clock is used (EXT=1), clock frequency should be adjusted to display mode that is selected.

Example of external oscillator application
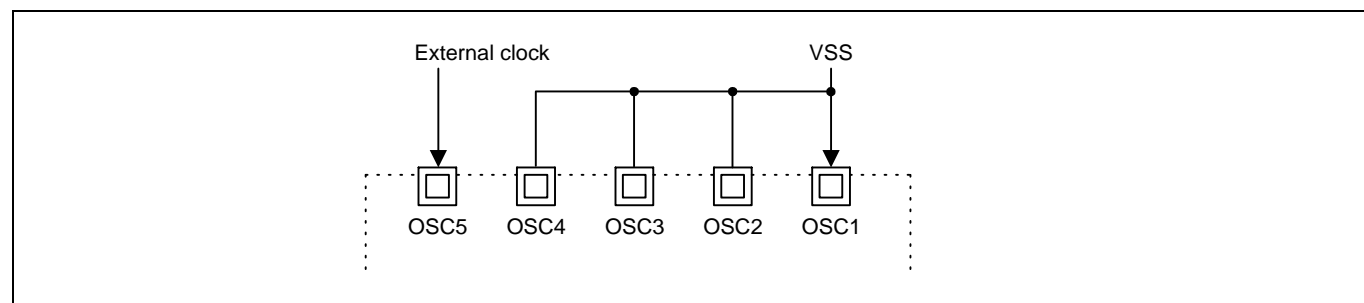
Figure 22. External oscillator application

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Example of internal oscillator application

When normal/partial display mode 0 is used.   When all display mode is used.
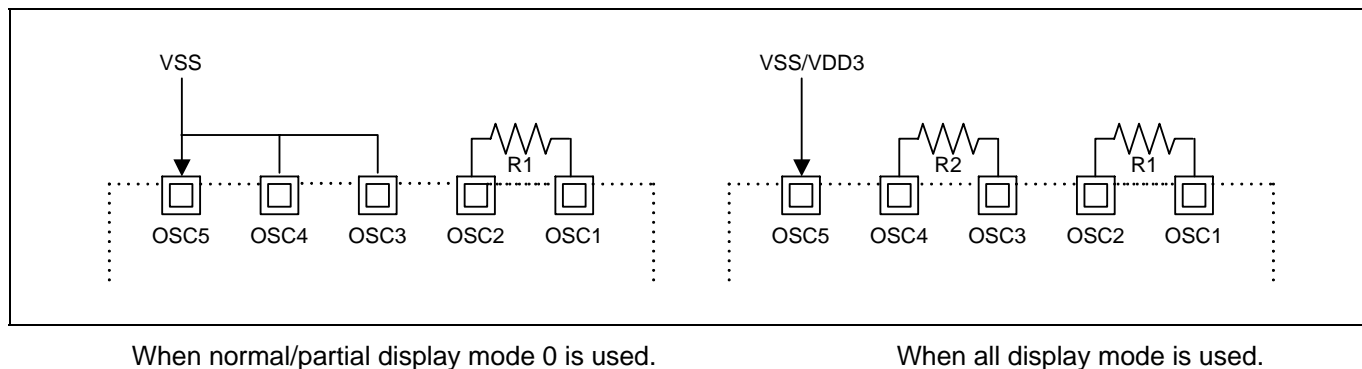
Figure 23. Internal oscillator application

Discharge Circuit

Driving voltage level discharge time at standby ON.
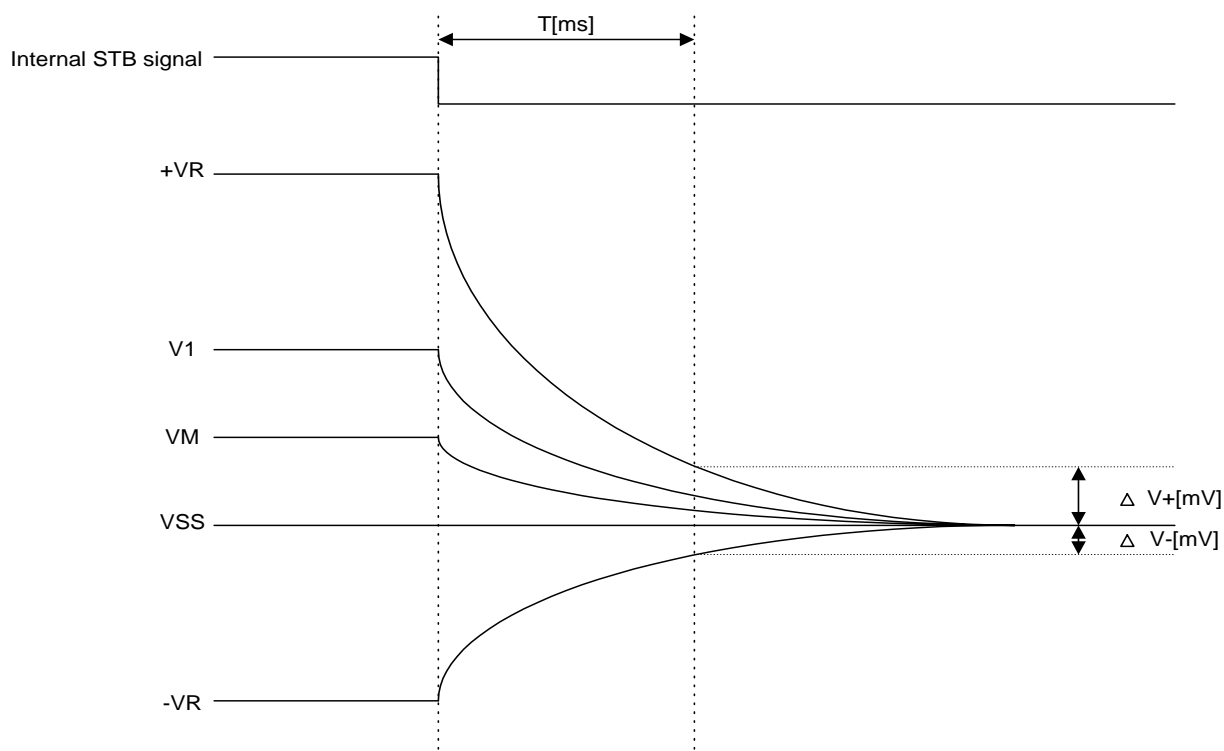
The relation between voltage level and discharge time from when "Standby ON" command is inputted.

LEVEL	CONDITION	T[ms]	ΔV+,ΔV-[mV]
+VR,V1,VM,-VR	+VR=12.0V, V1=3.0V, VM=1.5V, -VR=-9.0V at T=0	100	< 50
		300	< 20

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

Instruction Name	D/I	WRB	RDB	DB15 ~DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1Byte
Monitor Signal Control	0	0	1	*	0	0	0	1	1	0	0	0	18	1Byte
DC-DC Select	0	0	1	*	0	0	1	0	0	0	0	0	20	1Byte
Bias Set	0	0	1	*	0	0	1	0	0	0	1	0	22	1Byte
DCDC Clock Division Set	0	0	1	*	0	0	1	0	0	1	0	0	24	1Byte
DCDC and AMP ON/OFF set	0	0	1	*	0	0	1	0	0	1	1	0	26	1Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1Byte
Contrast Control(1)	0	0	1	*	0	0	1	0	1	0	1	0	2A	1Byte
Contrast Control(2)	0	0	1	*	0	0	1	0	1	0	1	1	2B	1Byte
Standby Mode OFF	0	0	1	*	0	0	1	0	1	1	0	0	2C	-
Standby Mode ON	0	0	1	*	0	0	1	0	1	1	0	1	2D	-
Addressing Mode Set	0	0	1	*	0	0	1	1	0	0	0	0	30	1Byte
ROW Vector Mode Set	0	0	1	*	0	0	1	1	0	0	1	0	32	1Byte
N-line Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1Byte
Frame Frequency control	0	0	1	*	0	0	1	1	0	1	1	0	36	1Byte
256 Color Red Palette	0	0	1	*	0	0	1	1	1	0	0	0	38	8Byte
256 Color Green Palette	0	0	1	*	0	0	1	1	1	0	1	0	3A	8Byte
256 Color Blue Palette	0	0	1	*	0	0	1	1	1	1	0	0	3C	4Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1Byte
X-address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2Byte
Y-address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2Byte
65K Color Red Palette	0	0	1	*	0	1	0	0	1	0	0	0	48	32Byte
65K Color Green Palette	0	0	1	*	0	1	0	0	1	0	1	0	4A	64Byte
65K Color Blue Palette	0	0	1	*	0	1	0	0	1	1	0	0	4C	32Byte
RAM Skip Area Set	0	0	1	*	0	1	0	0	0	1	0	1	45	1Byte
Display OFF	0	0	1	*	0	1	0	1	0	0	0	0	50	-
Display ON	0	0	1	*	0	1	0	1	0	0	0	1	51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1Byte
Partial Display Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1Byte
Partial Display End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1Byte
Area Scroll Mode Set	0	0	1	*	0	1	0	1	1	0	0	1	59	4Byte
Scroll Start Line Set	0	0	1	*	0	1	0	1	1	0	1	0	5A	1Byte
Data Format Select (Format A)	0	0	1	*	0	1	1	0	0	0	0	0	60	-
Data Format Select (Format B)	0	0	1	*	0	1	1	0	0	0	0	1	61	-
Set Display Data Length	X	X	X	*	1	1	1	1	1	1	0	0	FC	1Byte
Display Data Write	1	0	1	Display Data Write									-	-
Display Data Read	1	1	0	Display Data Read									-	-
Status Read	0	1	0	0	Status Data Read								-	-
Test Mode	0	0	1	*	1	1	1	1	*	*	*	*	F*	1Byte
OTP Mode Off	0	0	1	*	1	1	1	0	1	0	1	0	EA	-
OTP Mode On	0	0	1	*	1	1	1	0	1	0	1	1	EB	-
Offset Volume Set	0	0	1	*	1	1	1	0	1	1	0	1	ED	1Byte
OTP Write Enable	0	0	1	*	1	1	1	0	1	1	1	1	EF	-

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*: Don't care
Parameter: The number of parameter bytes that follows instruction data.

Non Operation (00H)

This instruction is Non operation.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0

Oscillation Mode Set (02H)

Setting internal function mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1	0
			0	0	0	0	0	0	EXT	OSC

EXT: External clock selecting
    EXT = 0: Internal clock mode (Initial status)
    EXT = 1: External clock mode

OSC: Internal oscillator ON/OFF
    OSC = 0: Internal oscillator OFF(Initial status)
    OSC = 1: Internal oscillator ON

Driver Output Mode Set(10H)

This instruction sets the display direction.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	DLN		0	SDIR	SWP	CDR

DLN: Display Line number selecting

DB5	DB4	Display Duty
0	0	1/132 (Initial status)
0	1	1/144
1	0	1/162
1	1	1/96

SDIR: Segment direction
    This bit is for controlling the direction of segment driver.
    SDIR = 0 (Initial status)

SWP: Swap segment output SEGAi and SEGCi
    This bit is for swapping the output of segment driver.
    SWP = 0 (Initial status)

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CDR: Software COM direction change register
    This bit and CDIR_P pin are for controlling the direction of common driver.
    CDR = 0 (Initial status)
    In case software control of COM direction, CDIR_P pin must be fixed at VSS.
    In case hardware control of COM direction, CDR register must be set at 0.

CDIR_P	CDR	CDIR (Internal Register)
0	0	**0**
	1	**1**
1	0	**1**
	1	**1**

Monitor Signal Control (18H)

This instruction configures the output enable and timing of monitor signal

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	0	0	0	1	1	0	0	0
			0	0	0	0	0	PM	CL	FR

PM: Enable to transfer field delimiter signal to output pin by active high
    PM = 0 (Initial status)

CL: Enable to transfer shift signal to output pin by active high
    CL = 0 (Initial status)

FR: Enable to transfer liquid crystal alternating signal to output pin by active high
    FR = 0 (Initial status)

DC-DC Select (20H)

Selects DC-DC step-up of the common driver in normal and partial mode

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	0	0	1	0	0	0	0	0
			0	0	0	0	DC(2)		DC(1)	

DC(1) : 1'st DC-DC booster boosting step select for V1 generation in normal mode and partial mode 0.
DC(2) : 1'st DC-DC booster boosting step select for V1 generation in partial mode 1.

DC(2) : In partial mode 1			Oprating voltage range	DC(1) : In normal mode partial mode 0			Oprating voltage range
DB3	DB2	DC-DC step up	VIN1	DB1	DB0	DC-DC step up	VIN1
0	0	X1.0	2.4~3.6[V]	0	0	X1.0	2.4~3.6[V]
0	1	X1.5	2.4~3.6[V]	0	1	X1.5	2.4~3.6[V]
1	0	X2.0	2.4~2.75[V]	1	0	X2.0	2.4~2.75[V]
1	1	X2.0	2.4~2.75[V]	1	1	X2.0	2.4~2.75[V]

DC-DC Select and power supply for V1 Op-Amp.

Even if VIN45 is connected to VOUT45 or VIN1, a setup by software must be able to be performed.
Power supply for V1 Op-Amp. is decided by Hardware setting and Software setting.

The example of usage is shown below.

Figure28. Example :   Hardware Setting   : VIN45 connected to VOUT45

Software Setting 1   : Power supply for V1 Op.Amp. uses 1'st booster output (not VIN1).
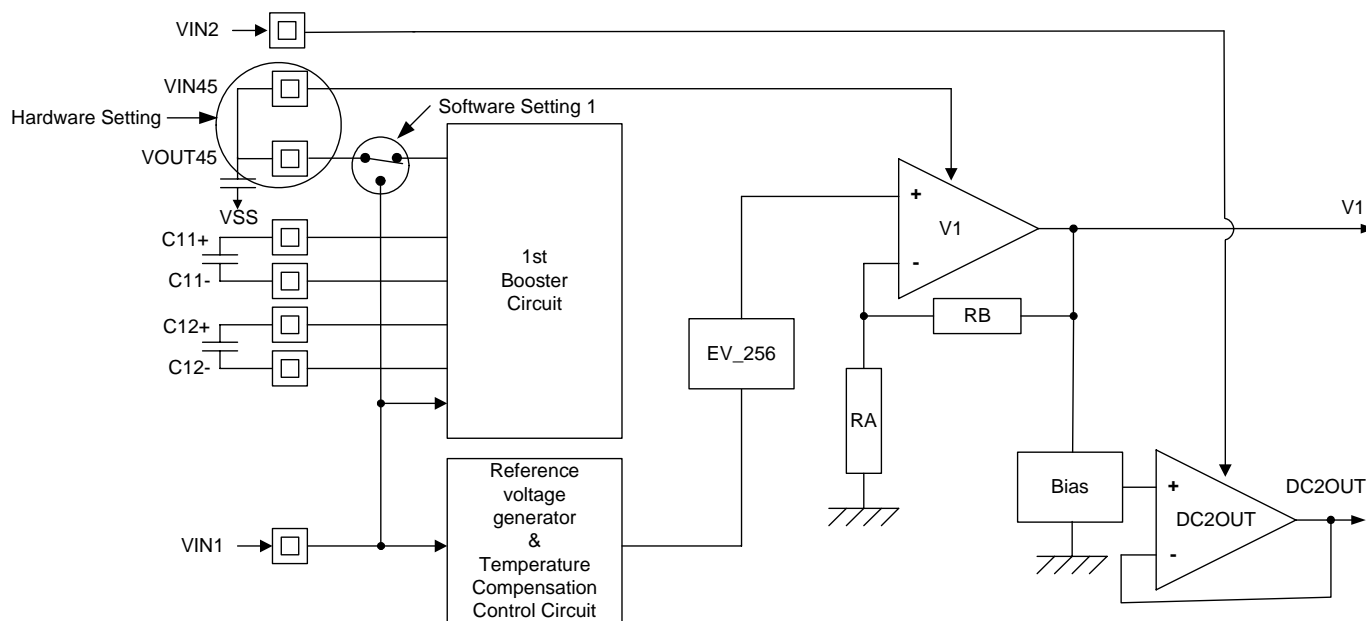
Hardware setting: VIN45 connected to   (1) VOUT45   (when VOUT45 is used)
                                       (2) VIN1   (when VOUT45 is not used)

Instruction setting: DC-DC Select (20H) - DC Register
                             Set value "00" Power supply for 1'st booster output uses 1XVIN1. (Initial status)
                             Set value "01" Power supply for 1'st booster output uses 1.5XVIN1.
                             Set value "10" or "11" Power supply for 1'st booster output uses 2XVIN1.

Software setting 1: DC/DC and AMP ON/OFF (26H) – DCDC1 Register
                             Set value "0" Power supply for VOUT45 uses VIN1. (Initial status)
                             Set value "1" Power supply for VOUT45 uses 1'st booster output.

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Bias Set (22H)

This instruction set up the value of bias in normal mode and in partial mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB9	DB1	DB0
0	0	1	0	0	1	0	0	0	1	0
			0	0	Bias(2)		0	0	Bias(1)	

Bias(1): Bias value selecting in normal mode and partial mode0.
Bias(2): Bias value selecting in partial mode1.

Bias(2): In partial mode 1				
DB5	DB4	Bias	DCDC2 step up	DC2OUT
0	0	1/4	X(-3)	3/4xV1
0	1	1/5	X(-3)	V1
1	0	1/6	X(-4)	5/6xV1
1	1	1/7	X(-4)	V1

Bias(1):In normal, partial mode 0				
DB1	DB0	Bias	DCDC2 step up	DC2OUT
0	0	1/4	X(-3)	3/4xV1
0	1	1/5	X(-3)	V1
1	0	1/6	X(-4)	5/6xV1
1	1	1/7	X(-4)	V1

DCDC Clock Division Set(24H)

This instruction sets the internal booster clock frequency.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	0	0
			0	0	DIV(2)		0	0	DIV(1)	

DIV(1) : DC-DC Charge Pump Division Ratio in Normal Mode Display and Partial Display Mode0
        - DIV(1) = 10 (Initial status)
DIV(2) : Division Ratio in Partial Display Mode1
        - DIV(2) = 10 (Initial status)

DB5	DB4	DIV(2)
0	0	fPCK = fOSC/8
0	1	fPCK = fOSC/16
1	0	fPCK = fOSC/32
1	1	fPCK = fOSC/64

DB1	DB0	DIV(1)
0	0	fPCK = fOSC/16
0	1	fPCK = fOSC/32
1	0	fPCK = fOSC/64
1	1	fPCK = fOSC/128

Note: fOSC = (ROUNDUP (Duty/3) + dummy) x 4 x 16 x frame frequency

DC/DC and AMP ON/OFF Set (26H)

This instruction set up the DC/DC and Op-amp in common start up setting.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	1	0
			0	0	0	0	AMP	DCDC3	DCDC2	DCDC1

AMP: Built-in OP-AMP ON/OFF.
- AMP=0: OP-AMP OFF (Initial status)
- AMP=1: OP-AMP ON

DCDC1: Built-in 1'st Booster ON/OFF
- DCDC1= 0: 1'st Booster OFF (Initial status)
- DCDC1= 1: 1'st Booster ON

DCDC2: Built-in 2'nd Booster ON/OFF
- DCDC2= 0: 2'nd Booster OFF (Initial status)
- DCDC2= 1: 2'nd Booster ON

DCDC3: Built-in 3'rd Booster ON/OFF
- DCDC3= 0: 3'rd Booster OFF (Initial status)
- DCDC3= 1: 3'rd Booster ON

Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	0	TCS	

TCS: Temperature compensation slope set
- TCS = 00 : 0.00%/degC (Initial status)
- TCS = 01 : -0.05%/degC
- TCS = 10 : -0.10%/degC
- TCS = 11 : -0.15%/degC

TCS Register Set *		Temp. Coefficient
DB1	DB0	
0	0	0.00%/°C
0	1	-0.05%/°C
1	0	-0.10%/°C
1	1	-0.15%/°C

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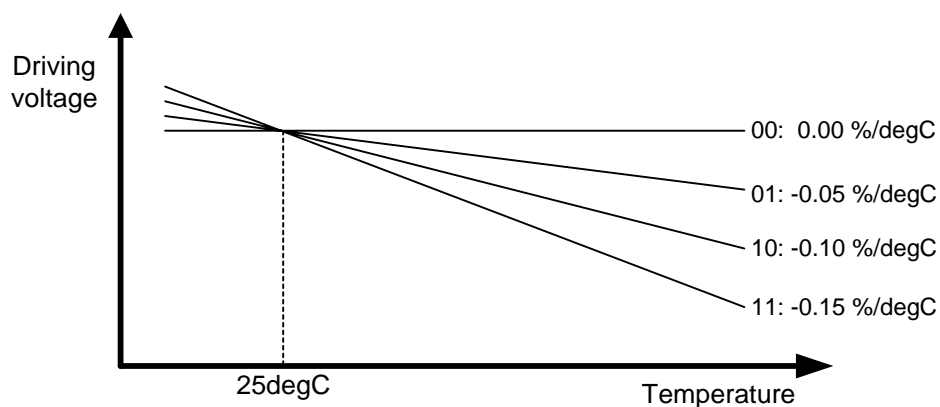
Temperature Compensation

If external temperature compensation is needed, circuit diagram is described as below.
To use temperature compensation, two resistors and one thermistor are needed.
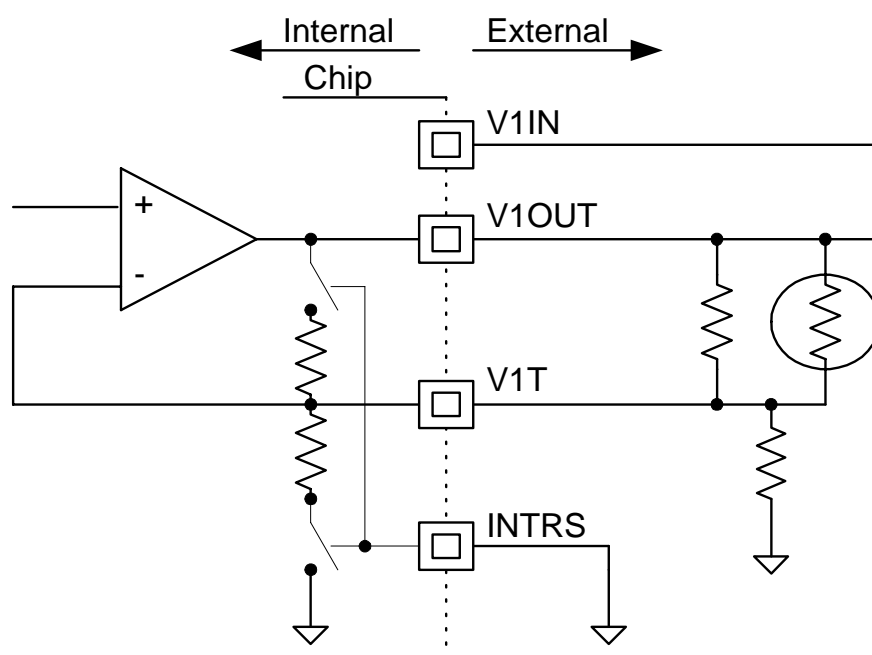
Contrast Control (1) (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode 0.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(1) set value (3bit step case)

Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Contrast Control (2) (2BH)

This instruction updates the contrast control value in partial display mode 1.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(2) set value (3 bit step case)

Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Note :
S6B33BC has a hardware protection for "2VR < 20V". It means the limitation of contrast value in each bias.
If 1/6 bias is set, max contrast value is limited to A9h, and if 1/7 bias is set, max contrast value is limited to 6Dh.

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Standby Mode OFF (2CH)

This instruction releases the standby mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	0

The internal statuses during standby off are as following:
- All common output: +VR or –VR or VM or VSS
- All segment output: VSS or V1
- Oscillator circuit: On (EXT = 0, OSC=1), OFF (others)
- Displaying clocks (FR, PM, CL): In operation

Function and Pin condition at standby OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
COM outputs	+VR or VM or VSS or -VR
SEG outputs	V1 or VSS

Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	1

The internal statuses during standby on are as following:
- All common and segment output: VSS
- Oscillator circuit: OFF
- Displaying clocks (FR, PM, CL) are held.

Function and Pin condition at standby ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	OFF
SEG and COM outputs	VSS

LCD driving power output condition at Standby ON.

level	Condition
+VR	VSS
V1	VSS
VM	VSS
-VR	VSS

Addressing Mode Set (30H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	0	0
			0	GSM		DSG	SGF	SGP		SGM

GSM: Gray Scale Mode
- 00: 65,536 color mode (Initial status)
- 01: 4,096 color mode (refer to "Data Format Select (60H/61H)")
- 10: 256 color mode
- 11: 256 color mode

Note : 256 color mode only supports 8bit access mode.(refer to "Display Data Write/Read")

DSG: Duty Adjust Setting
- 0: Dummy subgroup is one subgroup
- 1: Dummy subgroup is none (Initial status)

SGF: Sub Group Frame Inversion mode setting
- 0: SG Frame inversion OFF
- 1: SG Frame inversion ON (Initial status)

SGM: Sub Group inversion mode setting
- 0: SG inversion OFF
- 1: SG inversion ON (Initial status)

SGP: Sub Group Phase mode setting
- 00: Same phase in all pixels
- 01: Different phase by 1pixel-unit
- 10: Different phase by 2pixel-unit (Initial status)
- 11: Different phase by 4pixel-unit

Row Vector Mode Set (32H)

Setting ROW function.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	1	0
			0	0	0	0	INC			VEC

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period

DB3	DB2	DB1	Row Vector Increment Period
0	0	0	**Every subgroup**
0	0	1	**Every 2subgroup**
0	1	0	**Every 4subgroup**
0	1	1	**Every 8subgroup**
1	0	0	**Every 16subgroup**
1	0	1	**Every 16subgroup**
1	1	0	**Every 16subgroup**
1	1	1	**Every sub-frame (initial status)**

VEC: ROW Vector Sequence Mode
- 0: R1->R2->R3->R4 -> R1… (Initial status)
- 1: R1->R3->R2->R4 -> R1...

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N-block inversion Set (34H)

This instruction set up N block inversion for AC driving.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	0	0
			FIM	FIP	0	N-block inversion				

FIM: Forcing Inversion Mode
    FIM = 0: Forcing Inversion OFF
    FIM = 1: Forcing Inversion ON (Initial status)
FIP: Forcing Inversion Period
    FIP = 0: Forcing Inversion Period is one frame (Initial status)
    FIP = 1: Forcing Inversion Period is two frame
N-block Inversion: This parameter indicates the basic period of polarity inversion.
            The whole period of polarity inversion is decided by FIM, FIP and this parameter.
            (Initial status: 01101)

DB7	DB6	DB5	DB4 – DB0	Polarity Inversion Period
x	X	x	0	every frame
0	X	x	1	every 1 block
:	:	:	:	:
0	X	x	31	every 31 blocks
1	0	x	1	every 1 block and every frame
:	:	:	:	:
1	0	x	31	every 31 blocks and every frame
1	1	x	1	every 1 block and every 2 frames
:	:	:	:	:
1	1	x	31	every 31 blocks and every 2 frames

Frame Frequency Control (36H)

This instruction controls the internal frame frequency.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	1	0
			0	0	0	0	0	0	0	LFS

LFS: Low frame frequency set for low power consumption.
    LFS = 0 : Low frequency set OFF (Initial status)
    LFS = 1 : Low frequency set ON

Note : fFR @(LFS=1) = fFR @(LFS=0) / 2

Gamma correction

The S6B33BC provides the gamma correction function.
Gray scale data can be selected by instruction.

<Red/Green/Blue Palette Initial Value>
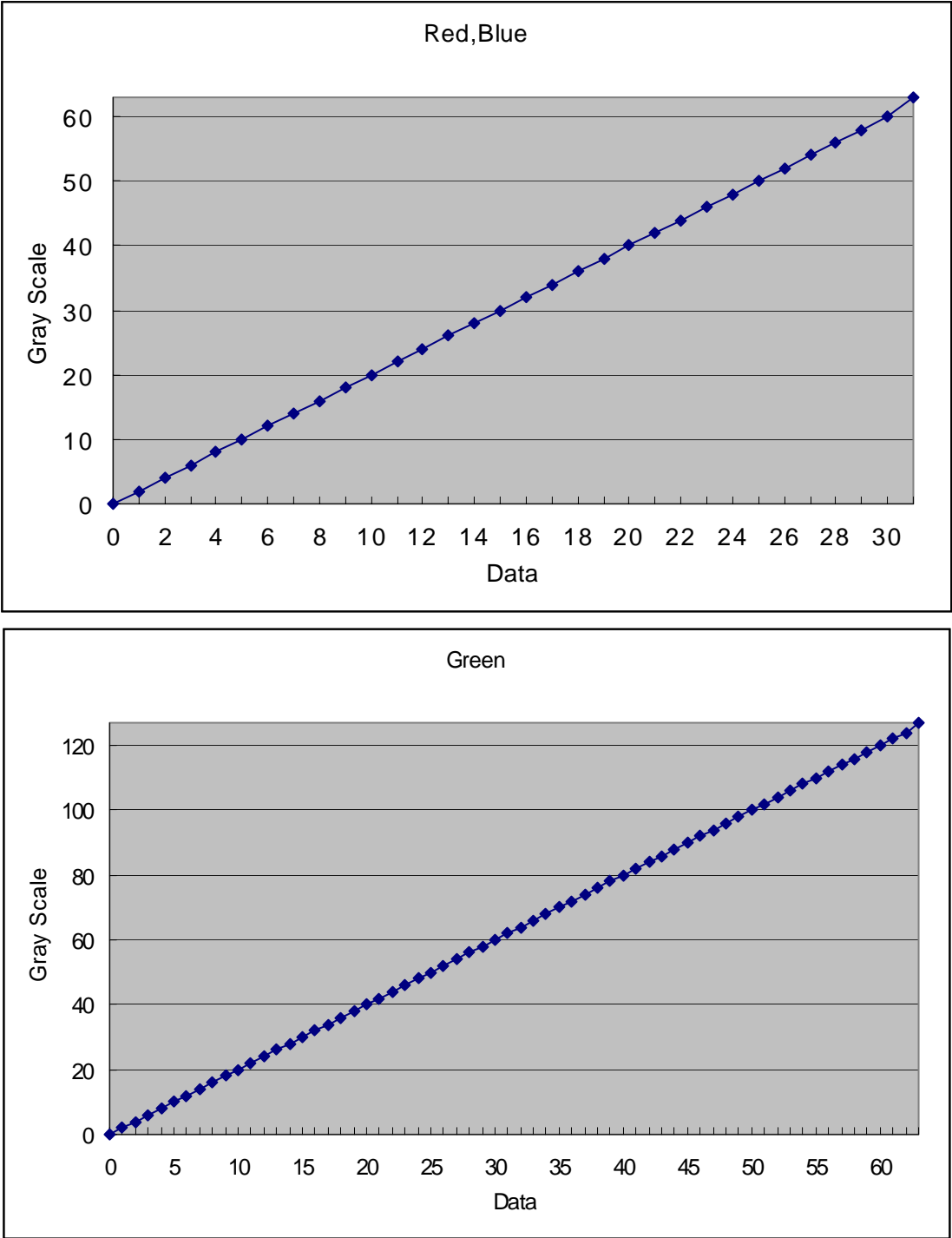
65K Color Mode Palettes

At 65K-color mode, the instruction and parameter below set each Gray Scale level of the Red/Green/Blue. Gray scale level is determined by GS data.

Red Palette (48H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			0	1	0	0	1	0	0	0
			0	0	GS data "00000" to RAM data					
			0	0	GS data "00001" to RAM data					
			0	0	GS data "00010" to RAM data					
			0	0	GS data "00011" to RAM data					
			0	0	GS data "00100" to RAM data					
			0	0	GS data "00101" to RAM data					
			0	0	GS data "00110" to RAM data					
			0	0	GS data "00111" to RAM data					
			0	0	GS data "01000" to RAM data					
			0	0	GS data "01001" to RAM data					
			0	0	GS data "01010" to RAM data					
			0	0	GS data "01011" to RAM data					
			0	0	GS data "01100" to RAM data					
			0	0	GS data "01101" to RAM data					
			0	0	GS data "01110" to RAM data					
0	0	1	0	0	GS data "01111" to RAM data					
			0	0	GS data "10000" to RAM data					
			0	0	GS data "10001" to RAM data					
			0	0	GS data "10010" to RAM data					
			0	0	GS data "10011" to RAM data					
			0	0	GS data "10100" to RAM data					
			0	0	GS data "10101" to RAM data					
			0	0	GS data "10110" to RAM data					
			0	0	GS data "10111" to RAM data					
			0	0	GS data "11000" to RAM data					
			0	0	GS data "11001" to RAM data					
			0	0	GS data "11010" to RAM data					
			0	0	GS data "11011" to RAM data					
			0	0	GS data "11100" to RAM data					
			0	0	GS data "11101" to RAM data					
			0	0	GS data "11110" to RAM data					
			0	0	GS data "11111" to RAM data					

Green Palette (4AH)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			0	1	0	0	1	0	1	0
			0	GS data "000000" to RAM data						
			0	GS data "000001" to RAM data						
			0	GS data "000010" to RAM data						
			0	GS data "000011" to RAM data						
			0	GS data "000100" to RAM data						
			0	GS data "000101" to RAM data						
			0	GS data "000110" to RAM data						
			0	GS data "000111" to RAM data						
			0	GS data "001000" to RAM data						
			0	GS data "001001" to RAM data						
			0	GS data "001010" to RAM data						
			0	GS data "001011" to RAM data						
			0	GS data "001100" to RAM data						
			0	GS data "001101" to RAM data						
			0	GS data "001110" to RAM data						
0	0	1	0	GS data "001111" to RAM data						
			0	GS data "010000" to RAM data						
			0	GS data "010001" to RAM data						
			0	GS data "010010" to RAM data						
			0	GS data "010011" to RAM data						
			0	GS data "010100" to RAM data						
			0	GS data "010101" to RAM data						
			0	GS data "010110" to RAM data						
			0	GS data "010111" to RAM data						
			0	GS data "011000" to RAM data						
			0	GS data "011001" to RAM data						
			0	GS data "011010" to RAM data						
			0	GS data "011011" to RAM data						
			0	GS data "011100" to RAM data						
			0	GS data "011101" to RAM data						
			0	GS data "011110" to RAM data						
			0	GS data "011111" to RAM data						

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Green Palette (Continued)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			0	GS data "100000" to RAM data						
			0	GS data "100001" to RAM data						
			0	GS data "100010" to RAM data						
			0	GS data "100011" to RAM data						
			0	GS data "100100" to RAM data						
			0	GS data "100101" to RAM data						
			0	GS data "100110" to RAM data						
			0	GS data "100111" to RAM data						
			0	GS data "101000" to RAM data						
			0	GS data "101001" to RAM data						
			0	GS data "101010" to RAM data						
			0	GS data "101011" to RAM data						
			0	GS data "101100" to RAM data						
			0	GS data "101101" to RAM data						
			0	GS data "101110" to RAM data						
			0	GS data "101111" to RAM data						
0	0	1	0	GS data "110000" to RAM data						
			0	GS data "110001" to RAM data						
			0	GS data "110010" to RAM data						
			0	GS data "110011" to RAM data						
			0	GS data "110100" to RAM data						
			0	GS data "110101" to RAM data						
			0	GS data "110110" to RAM data						
			0	GS data "110111" to RAM data						
			0	GS data "111000" to RAM data						
			0	GS data "111001" to RAM data						
			0	GS data "111010" to RAM data						
			0	GS data "111011" to RAM data						
			0	GS data "111100" to RAM data						
			0	GS data "111101" to RAM data						
			0	GS data "111110" to RAM data						
			0	GS data "111111" to RAM data						

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Blue Palette (4CH)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			0	1	0	0	1	1	0	0
			0	0	GS data "00000" to RAM data					
			0	0	GS data "00001" to RAM data					
			0	0	GS data "00010" to RAM data					
			0	0	GS data "00011" to RAM data					
			0	0	GS data "00100" to RAM data					
			0	0	GS data "00101" to RAM data					
			0	0	GS data "00110" to RAM data					
			0	0	GS data "00111" to RAM data					
			0	0	GS data "01000" to RAM data					
			0	0	GS data "01001" to RAM data					
			0	0	GS data "01010" to RAM data					
			0	0	GS data "01011" to RAM data					
			0	0	GS data "01100" to RAM data					
			0	0	GS data "01101" to RAM data					
			0	0	GS data "01110" to RAM data					
0	0	1	0	0	GS data "01111" to RAM data					
			0	0	GS data "10000" to RAM data					
			0	0	GS data "10001" to RAM data					
			0	0	GS data "10010" to RAM data					
			0	0	GS data "10011" to RAM data					
			0	0	GS data "10100" to RAM data					
			0	0	GS data "10101" to RAM data					
			0	0	GS data "10110" to RAM data					
			0	0	GS data "10111" to RAM data					
			0	0	GS data "11000" to RAM data					
			0	0	GS data "11001" to RAM data					
			0	0	GS data "11010" to RAM data					
			0	0	GS data "11011" to RAM data					
			0	0	GS data "11100" to RAM data					
			0	0	GS data "11101" to RAM data					
			0	0	GS data "11110" to RAM data					
			0	0	GS data "11111" to RAM data					

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Initial value for each Palette

Gray Scale	Initial Gray Scale Level		
Data	Red	Green	Blue
000000	0	0	0
000001	2	2	2
000010	4	4	4
000011	6	6	6
000100	8	8	8
000101	10	10	10
000110	12	12	12
000111	14	14	14
001000	16	16	16
001001	18	18	18
001010	20	20	20
001011	22	22	22
001100	24	24	24
001101	26	26	26
001110	28	28	28
001111	30	30	30
010000	32	32	32
010001	34	34	34
010010	36	36	36
010011	38	38	38
010100	40	40	40
010101	42	42	42
010110	44	44	44
010111	46	46	46
011000	48	48	48
011001	50	50	50
011010	52	52	52
011011	54	54	54
011100	56	56	56
011101	58	58	58
011110	60	60	60
011111	63	62	63

Initial value for each Palette

Gray Scale Data	Initial Gray Scale Level		
	Red	Green	Blue
100000	-	64	-
100001	-	66	-
100010	-	68	-
100011	-	70	-
100100	-	72	-
100101	-	74	-
100110	-	76	-
100111	-	78	-
101000	-	80	-
101001	-	82	-
101010	-	84	-
101011	-	86	-
101100	-	88	-
101101	-	90	-
101110	-	92	-
101111	-	94	-
110000	-	96	-
110001	-	98	-
110010	-	100	-
110011	-	102	-
110100	-	104	-
110101	-	106	-
110110	-	108	-
110111	-	110	-
111000	-	112	-
111001	-	114	-
111010	-	116	-
111011	-	118	-
111100	-	120	-
111101	-	122	-
111110	-	124	-
111111	-	127	-

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The relationship between Gray Scale level and RAM data for Red/Blue

RAM Data						GS Level	RAM Data						GS Level
DB5	DB4	DB3	DB2	DB1	DB0		DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	0	0	0	0	0	32
0	0	0	0	0	1	1	1	0	0	0	0	1	33
0	0	0	0	1	0	2	1	0	0	0	1	0	34
0	0	0	0	1	1	3	1	0	0	0	1	1	35
0	0	0	1	0	0	4	1	0	0	1	0	0	36
0	0	0	1	0	1	5	1	0	0	1	0	1	37
0	0	0	1	1	0	6	1	0	0	1	1	0	38
0	0	0	1	1	1	7	1	0	0	1	1	1	39
0	0	1	0	0	0	8	1	0	1	0	0	0	40
0	0	1	0	0	1	9	1	0	1	0	0	1	41
0	0	1	0	1	0	10	1	0	1	0	1	0	42
0	0	1	0	1	1	11	1	0	1	0	1	1	43
0	0	1	1	0	0	12	1	0	1	1	0	0	44
0	0	1	1	0	1	13	1	0	1	1	0	1	45
0	0	1	1	1	0	14	1	0	1	1	1	0	46
0	0	1	1	1	1	15	1	0	1	1	1	1	47
0	1	0	0	0	0	16	1	1	0	0	0	0	48
0	1	0	0	0	1	17	1	1	0	0	0	1	49
0	1	0	0	1	0	18	1	1	0	0	1	0	50
0	1	0	0	1	1	19	1	1	0	0	1	1	51
0	1	0	1	0	0	20	1	1	0	1	0	0	52
0	1	0	1	0	1	21	1	1	0	1	0	1	53
0	1	0	1	1	0	22	1	1	0	1	1	0	54
0	1	0	1	1	1	23	1	1	0	1	1	1	55
0	1	1	0	0	0	24	1	1	1	0	0	0	56
0	1	1	0	0	1	25	1	1	1	0	0	1	57
0	1	1	0	1	0	26	1	1	1	0	1	0	58
0	1	1	0	1	1	27	1	1	1	0	1	1	59
0	1	1	1	0	0	28	1	1	1	1	0	0	60
0	1	1	1	0	1	29	1	1	1	1	0	1	61
0	1	1	1	1	0	30	1	1	1	1	1	0	62
0	1	1	1	1	1	31	1	1	1	1	1	1	63

The relationship between Gray Scale level and RAM data for Green

RAM Data							GS Level	RAM Data							GS Level
DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB0	
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	32
0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	33
0	0	0	0	0	1	0	2	0	1	0	0	0	1	0	34
0	0	0	0	0	1	1	3	0	1	0	0	0	1	1	35
0	0	0	0	1	0	0	4	0	1	0	0	1	0	0	36
0	0	0	0	1	0	1	5	0	1	0	0	1	0	1	37
0	0	0	0	1	1	0	6	0	1	0	0	1	1	0	38
0	0	0	0	1	1	1	7	0	1	0	0	1	1	1	39
0	0	0	1	0	0	0	8	0	1	0	1	0	0	0	40
0	0	0	1	0	0	1	9	0	1	0	1	0	0	1	41
0	0	0	1	0	1	0	10	0	1	0	1	0	1	0	42
0	0	0	1	0	1	1	11	0	1	0	1	0	1	1	43
0	0	0	1	1	0	0	12	0	1	0	1	1	0	0	44
0	0	0	1	1	0	1	13	0	1	0	1	1	0	1	45
0	0	0	1	1	1	0	14	0	1	0	1	1	1	0	46
0	0	0	1	1	1	1	15	0	1	0	1	1	1	1	47
0	0	1	0	0	0	0	16	0	1	1	0	0	0	0	48
0	0	1	0	0	0	1	17	0	1	1	0	0	0	1	49
0	0	1	0	0	1	0	18	0	1	1	0	0	1	0	50
0	0	1	0	0	1	1	19	0	1	1	0	0	1	1	51
0	0	1	0	1	0	0	20	0	1	1	0	1	0	0	52
0	0	1	0	1	0	1	21	0	1	1	0	1	0	1	53
0	0	1	0	1	1	0	22	0	1	1	0	1	1	0	54
0	0	1	0	1	1	1	23	0	1	1	0	1	1	1	55
0	0	1	1	0	0	0	24	0	1	1	1	0	0	0	56
0	0	1	1	0	0	1	25	0	1	1	1	0	0	1	57
0	0	1	1	0	1	0	26	0	1	1	1	0	1	0	58
0	0	1	1	0	1	1	27	0	1	1	1	0	1	1	59
0	0	1	1	1	0	0	28	0	1	1	1	1	0	0	60
0	0	1	1	1	0	1	29	0	1	1	1	1	0	1	61
0	0	1	1	1	1	0	30	0	1	1	1	1	1	0	62
0	0	1	1	1	1	1	31	0	1	1	1	1	1	1	63

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The relationship between Gray Scale level and RAM data for Green (Continued)

RAM Data							GS Level	RAM Data							GS Level
DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB0	
1	0	0	0	0	0	0	64	1	1	0	0	0	0	0	96
1	0	0	0	0	0	1	65	1	1	0	0	0	0	1	97
1	0	0	0	0	1	0	66	1	1	0	0	0	1	0	98
1	0	0	0	0	1	1	67	1	1	0	0	0	1	1	99
1	0	0	0	1	0	0	68	1	1	0	0	1	0	0	100
1	0	0	0	1	0	1	69	1	1	0	0	1	0	1	101
1	0	0	0	1	1	0	70	1	1	0	0	1	1	0	102
1	0	0	0	1	1	1	71	1	1	0	0	1	1	1	103
1	0	0	1	0	0	0	72	1	1	0	1	0	0	0	104
1	0	0	1	0	0	1	73	1	1	0	1	0	0	1	105
1	0	0	1	0	1	0	74	1	1	0	1	0	1	0	106
1	0	0	1	0	1	1	75	1	1	0	1	0	1	1	107
1	0	0	1	1	0	0	76	1	1	0	1	1	0	0	108
1	0	0	1	1	0	1	77	1	1	0	1	1	0	1	109
1	0	0	1	1	1	0	78	1	1	0	1	1	1	0	110
1	0	0	1	1	1	1	79	1	1	0	1	1	1	1	111
1	0	1	0	0	0	0	80	1	1	1	0	0	0	0	112
1	0	1	0	0	0	1	81	1	1	1	0	0	0	1	113
1	0	1	0	0	1	0	82	1	1	1	0	0	1	0	114
1	0	1	0	0	1	1	83	1	1	1	0	0	1	1	115
1	0	1	0	1	0	0	84	1	1	1	0	1	0	0	116
1	0	1	0	1	0	1	85	1	1	1	0	1	0	1	117
1	0	1	0	1	1	0	86	1	1	1	0	1	1	0	118
1	0	1	0	1	1	1	87	1	1	1	0	1	1	1	119
1	0	1	1	0	0	0	88	1	1	1	1	0	0	0	120
1	0	1	1	0	0	1	89	1	1	1	1	0	0	1	121
1	0	1	1	0	1	0	90	1	1	1	1	0	1	0	122
1	0	1	1	0	1	1	91	1	1	1	1	0	1	1	123
1	0	1	1	1	0	0	92	1	1	1	1	1	0	0	124
1	0	1	1	1	0	1	93	1	1	1	1	1	0	1	125
1	0	1	1	1	1	0	94	1	1	1	1	1	1	0	126
1	0	1	1	1	1	1	95	1	1	1	1	1	1	1	127

256 Color Mode Palettes

At 256-color mode, the instruction and parameter below set each Gray Scale level of the Red/Green/Blue. Gray scale level is determined by GS data.

Red Palette (38H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	0	0
			0	0	GS data "000" to RAM data					
			0	0	GS data "001" to RAM data					
			0	0	GS data "010" to RAM data					
			0	0	GS data "011" to RAM data					
			0	0	GS data "100" to RAM data					
			0	0	GS data "101" to RAM data					
			0	0	GS data "110" to RAM data					
			0	0	GS data "111" to RAM data					

Green Palette (3AH)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	1	0
			0	GS data "000" to RAM data						
			0	GS data "001" to RAM data						
			0	GS data "010" to RAM data						
			0	GS data "011" to RAM data						
			0	GS data "100" to RAM data						
			0	GS data "101" to RAM data						
			0	GS data "110" to RAM data						
			0	GS data "111" to RAM data						

Blue Palette (3CH)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	1	0	0
			0	0	GS data "00" to RAM data					
			0	0	GS data "01" to RAM data					
			0	0	GS data "10" to RAM data					
			0	0	GS data "11" to RAM data					

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Initial value for each Palette

Gray Scale	Initial Gray Scale Level		
Data	Red	Green	Blue
000	0	0	0
001	24	48	28
010	28	56	36
011	32	64	63
100	34	72	-
101	40	80	-
110	48	89	-
111	63	127	-

Entry Mode Set (40H)

Setting internal function mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0	0
			0	0	0	0	0	MDI	X/Y	RMW

MDI: Memory data inversion setting for low power consumption.
    MDI = 0: Memory data inversion OFF (Initial status)
    MDI = 1: Memory data inversion ON

<MDI=0>   <MDI=1>

	Display Data Write	Display Data Read		Display Data Write	Display Data Read
Data Bus	00h	00h		00h	FFh
Memory	00h	00h		FFh	00h
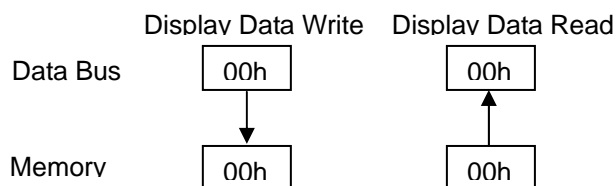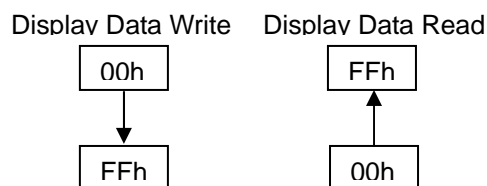
X/Y: Memory address counter mode setting
    X/Y = 0: Y address counter mode (Initial status)
    X/Y = 1: X address counter mode

RMW: Read modify write mode ON/OFF select
    RMW = 0: Read modify write OFF (Initial status)
    RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is not
                increment in reading display data but in writing display data.

X Address Area Set (42H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	0
			X start address set (Initial Status = 00H)							
			X end address set (Initial Status = A1H)							

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X
address count mode (X/Y = "H"), the X address is increased from X start address to X end address. When X
address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start
address. The X start and X end addresses must be set as a pair and X start address must be less than X end
address.

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Y Address Area Set (43H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			0	1	0	0	0	0	1	1
0	0	1	Y start address set (Initial Status = 00H)							
			Y end address set (Initial Status = 83H)							

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (X/Y = "L"), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end address must be set as a pair and Y start address must be less than Y end address.

RAM Skip Area Set (45H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	0	1
			0	0	0	0	0	0	RSK	

RSK : RAM Skip function ON/OFF set
- RSK = 00 : No Skip
- RSK = 01 : Y address 40h - 43h skip(128 RGB)
- RSK = 10 : Y address 3Ch - 47h skip(120 RGB)
- RSK = 11 : Y address 30h – 53h skip(96 RGB)

RAM Skip Area Set

RAM Skip Area Set can skip a part of RAM Y-address area. After setting RAM skip area, Y-address count skip this area and count. In other words, Y address after skip area is changed into Y address which added a part for skip area.
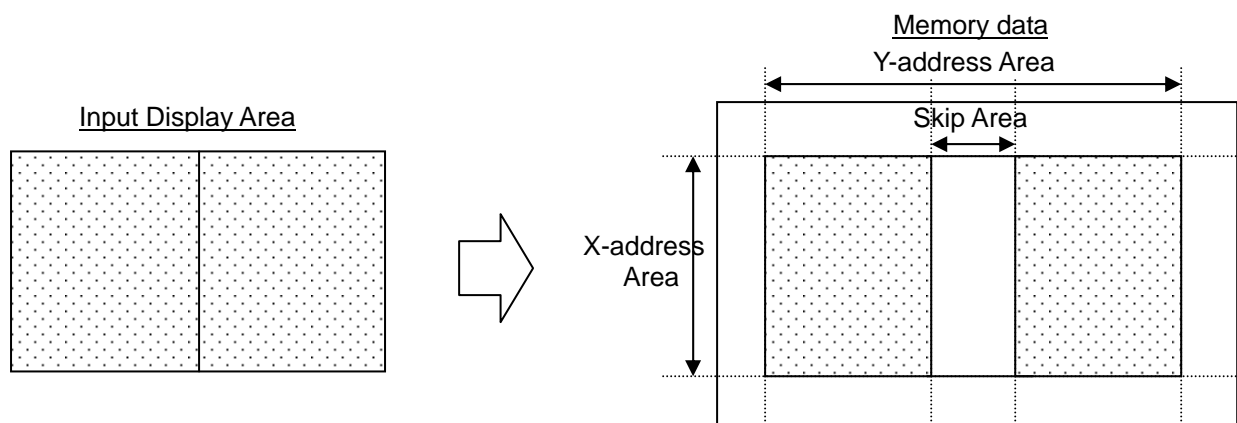
Display OFF (50H)

Turn the display OFF(Initial status).
When display is off, all segment and common output are VSS level.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	0

Function and Pin condition at Display OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
SEG and COM outputs	VSS

Display ON (51H)

Turns the display ON.
In case of being standby mode, this instruction does not work. This instruction is executed after standby mode off.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1

Function and Pin condition at Display ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
COM outputs	+VR or VM or -VR
SEG outputs	V1 or VSS

Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP	

SDP : Specified Display Pattern set
- SDP = 00 : Normal display
- SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM
- SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.
- SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

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Partial Display Mode Set (55H)

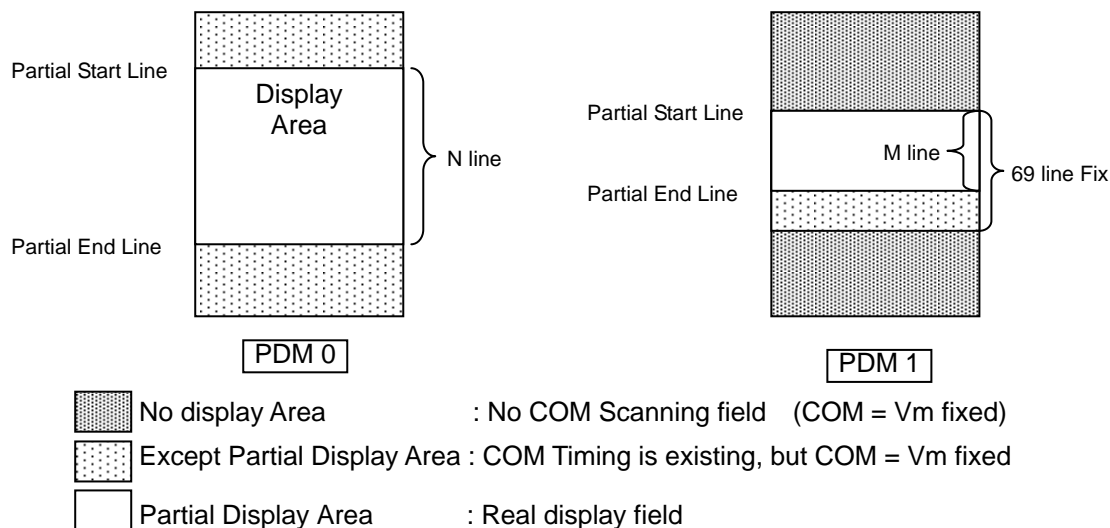| D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	0	PDM	PT

PT: Partial Display ON/OFF
- PT = 0: Partial display OFF = Normal mode (Initial status)
- PT = 1: Partial display ON

PDM: Partial Display mode set
- PDM = 0: Partial mode 0 : Duty ratio is same as Normal display mode(initial status)
- PDM = 1: Partial mode 1 : Duty ratio is changed from Normal display mode
  (DSG = 0 : 69 line fixed(including 1 dummy subgroup),
  DSG = 1 : 66 line fixed(no dummy subgroup))

Applied parameter in PDM0 and PDM1 are summarized as below

PDM	Contrast	Duty	Bias	DC-DC Select	OSC	PCK
0	Contrast control(1)	Normal	Bias(1)	DC(1)	OSC1-OSC2	DIV(1)
1	Contrast control(2)	1/69	Bias(2)	DC(2)	OSC3-OSC4	DIV(2)

Partial Start Line
Display Area
N line
Partial End Line

PDM 0

Partial Start Line
M line
69 line Fix
Partial End Line

PDM 1

No display Area   : No COM Scanning field   (COM = Vm fixed)

Except Partial Display Area : COM Timing is existing, but COM = Vm fixed

Partial Display Area   : Real display field

Operation in Partial Display Mode 0 (PDM=0)
  On scanning except partial display area
   - SEG output select V0 or V1 level depend on "FR" value. Refer to Page58.
   - All of COM output is fixed VM level.
  On scanning partial display area
   - It is equal to be in normal mode

Operation in Partial Display Mode 1 (PDM=1)
  Display area is from partial start line to partial end line.
  (COM driver output is fixed VM except display area, only max69 line output COM signal.
  On scanning except partial display area
   - SEG output select V0 or V1 level depend on "FR" value. Refer to Page58.
   - All of COM output is fixed VM level.
  On scanning partial display area
   - It is equal to be in normal mode

Partial Display Mode0

Item	Partial Display Area	Out of Partial Display Area
Duty	Same as normal display mode	
Bias	Same as normal display mode (Bias(1) setting)	
Contrast	Same as normal display mode (Contrast(1) setting)	
Oscillator	Same as normal display mode (OSC1 – OSC2)	
SEG Output level	Same as normal mode (V1,V0)	Depends on Internal "FR" signal See page 58
COM Output level	Same as normal mode (+VR,VM,-VR)	VM fixed

In case of COM 6 to COM11 Partial display
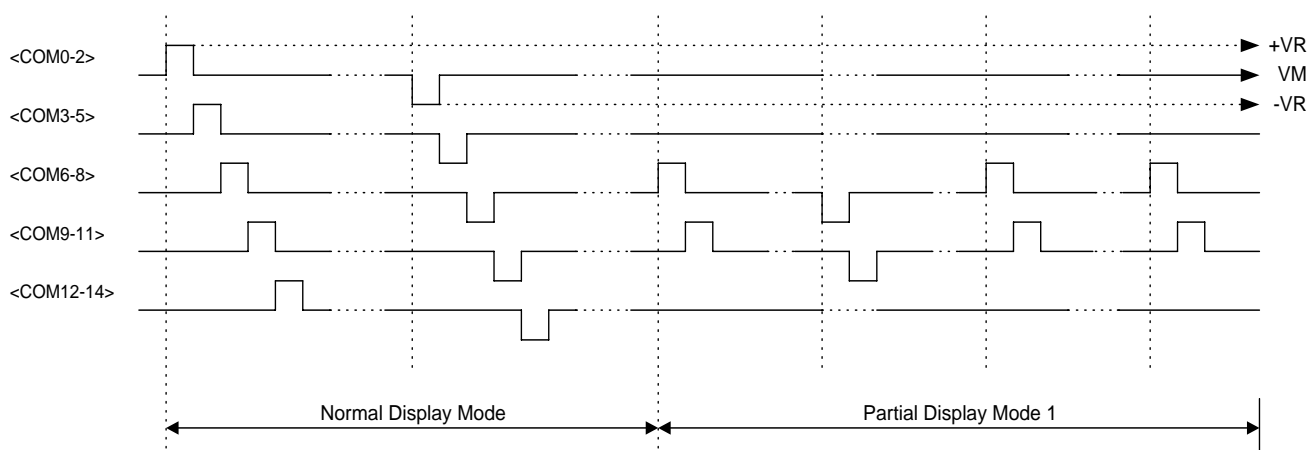
Partial display mode1

Item	Partial Display Area	Out of Partial Display Area	Out of Display Area
Duty	1/66duty		
Bias	Bias(2) setting		
Contrast	Contrast(2) setting		
Oscillator	(OSC3 – OSC4) setting value		
SEG Output level	Same as normal mode (V1,V0)	Depends on "FR" signal See page 58	-
COM Output level	Same as normal mode (+VR, VM, -VR)	VM fixed	VM fixed

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Partial Display Start Line Set (56H), Partial Display End Line Set(57H)

These 2 instructions set the partial display area and it is possible to display a part.

Partial Display Start Line Set (56H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	0
			Partial start line							

Partial Display End Line Set (57H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	1
			Partial end line							

COM 0	**line 0**
COM 1	**line 1**
COM 2	**line 2**
COM 3	**line 3**
	:
	:
	:
COM 158	**line 158**
COM 159	**line 159**
COM 160	**line 160**
COM 161	**line 161**

Parameter set appoints display line number. At PDM 0, Parameter Size is able to be in a number of Display lines. But that is not able to be over max 69 line at PDM 1. Partial end line must set bigger number than Partial start line.

Example of Segment Voltage in non-display area
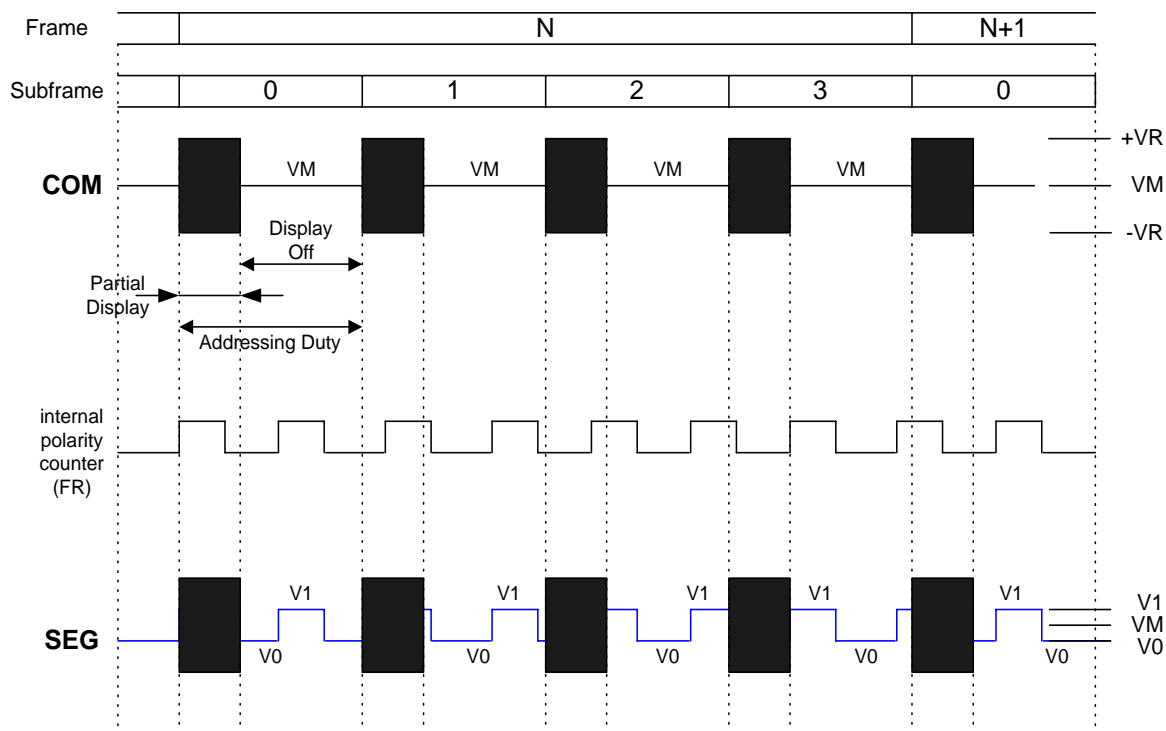
Area scroll Set (59H)

This instruction sets up area scroll field (start line, end line, Lower fixed line number), and it is possible to make screen to display as partial scroll field.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			0	1	0	1	1	0	0	1
			0	0	0	0	0	0	SCM	
0	0	1	Scroll area start line							
			Scroll area end line							
			Lower fixed number							

Note : In lower and center scroll mode, scroll area end line must be smaller than (duty - lower fixed number).

SCM: Scroll mode setting

DB1	DB0	Mode
0	0	Entire display(Initial status)
0	1	Upper scroll display
1	0	Lower scroll display
1	1	Center scroll display

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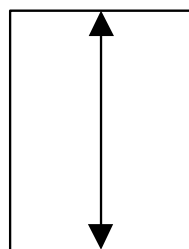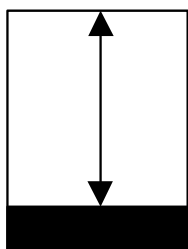
| Entire Display | Upper Display | Lower Display | Center Display |
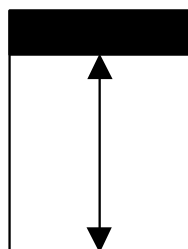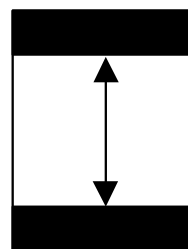
Scroll Start Line Set (5AH)

This instruction and parameter set up scroll start line. On this instruction, scroll start line becomes the first of area scroll field. Scroll operation is occurred every issue of this instruction.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	1	0
			Scroll start line							

<Example>

-DLN   : 2'b10 (1/162 duty)
-SCM   : 2'b11 (Center display mode)
-Scroll area start line   : 6
-Scroll area end line   : 152
-Lower fixed number   : 9
-Scroll start line   : 40

RAM Address.

```
┌─────────────────────────────────────────────────────────────────────────────┐
│                              Normal Mode                                      │
└─────────────────────────────────────────────────────────────────────────────┘
        │                           │                              │
        ▼                           ▼                              ▼
┌──────────────────┐    ┌──────────────────────┐    ┌──────────────────────────┐
│ Set partial      │    │ Set scroll mode      │    │ Set scroll mode          │
│ start line       │    │ Set scroll area      │    │ Set scroll area start    │
│ Set partial      │    │ start line           │    │ line                     │
│ end line         │    │ Set scroll area      │    │ Set scroll area end line │
│ Set partial      │    │ end line             │    │ Set lower fixed line     │
│ mode 0           │    │ Set lower fixed      │    │ Set scroll start line    │
│                  │    │ line no.             │    │ Set partial start line   │
│                  │    │ Set scroll start     │    │ Check busy flag          │
│                  │    │ line                 │    │ Set partial end line     │
│                  │    │                      │    │ Set partial mode 0       │
└──────────────────┘    └──────────────────────┘    └──────────────────────────┘
        │                           │                              │
        ▼                           ▼                              ▼
┌──────────────────┐    ┌──────────────────────┐    ┌──────────────────────────┐
│  Partial Mode 0  │    │     Scroll Mode      │    │   Scroll/Partial Mode 0  │
└──────────────────┘    └──────────────────────┘    └──────────────────────────┘
        │                           │                              │
        ▼                           ▼                              ▼
┌──────────────────┐    ┌──────────────────────┐    ┌──────────────────────────┐
│                  │    │ Set scroll mode      │    │ Set scroll mode          │
│                  │    │ Set scroll area      │    │ Set scroll area start    │
│                  │    │ start line           │    │ line                     │
│ Release partial  │    │ Set scroll area      │    │ Set scroll area end line │
│ mode             │    │ end line             │    │ Set lower fixed line no. │
│                  │    │ Set lower fixed      │    │ Set scroll start line    │
│                  │    │ line no.             │    │ Release partial mode     │
│                  │    │ Set scroll start     │    │                          │
│                  │    │ line                 │    │                          │
└──────────────────┘    └──────────────────────┘    └──────────────────────────┘
        │                           │                              │
        ▼                           ▼                              ▼
┌─────────────────────────────────────────────────────────────────────────────┐
│                              Normal Mode                                      │
└─────────────────────────────────────────────────────────────────────────────┘
```

Data Format Select (60H/61H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	0	0	DFS

DFS: 4,096 Color Mode Data Format Select
- 0 : 4,096 Color Data Format A (Initial Status)
        8 bit mode :
                DB[7:0] : XXXXRRRR (1'st write)
                DB[7:0] : GGGGBBBB(2'nd write)
        16 bit mode :
                DB[15:0] :XXXXRRRRGGGGBBBB (12 bit)
- 1 : 4,096 Color Data Format B
        8 bit mode :
                DB[7:0] : RRRRGGGG(1'st write)
                DB[7:0] : BBBBXXXX(2'nd write)
        16 bit mode :
                DB[15:0] :RRRRGGGGBBBBXXXX (12 bit)

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Display Data Write/Read

D/I	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Display RAM write in data								
1	1	0	Display RAM read out data								

GSM = 00(65,536 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
2'nd cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3
2'nd cycle	G2	G1	G0	B4	B3	B2	B1	B0
3'rd cycle	R4	R3	R2	R1	R0	G5	G4	G3
4'th cycle	G2	G1	G0	B4	B3	B2	B1	B0

GSM = 01(4,096 Color Mode), DFS = 0

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2'nd cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0
2'nd cycle	G3	G2	G1	G0	B3	B2	B1	B0
3'rd cycle	X	X	X	X	R3	R2	R1	R0
4'th cycle	G3	G2	G1	G0	B3	B2	B1	B0

GSM = 01(4,096 Color Mode), DFS = 1

(3) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	X	X	X	X
2'nd cycle	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	X	X	X	X

(4) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R3	R2	R1	R0	G3	G2	G1	G0
2'nd cycle	B3	B2	B1	B0	X	X	X	X
3'rd cycle	R3	R2	R1	R0	G3	G2	G1	G0
4'th cycle	B3	B2	B1	B0	X	X	X	X

GSM = 10 or 11 (256 Color Mode)

(1) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R2	R1	R0	G2	G1	G0	B1	B0
2'nd cycle	R2	R1	R0	G2	G1	G0	B1	B0

Status Read

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	BSY	X/Y	OPRT	PDM	PT	STB	REV	DP

This instruction indicates the internal status of the S6B33BC.

DP: (0 : Display OFF Status, 1 : Display ON Status)
REV: (0 : Display Image Non-Reversing, 1 : Display Image Reversing)
STB: (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)
PT: (0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status)
PDM: (0 : Partial Display Mode 0, 1 : Partial Display Mode 1)
OPRT: (0: OTP mode non-protection status, 1: OTP mode protection status)
X/Y: (0 : Y-address Count Mode, 1 : X-address Count Mode)
BSY: (0 : No Busy, 1 : Busy)

OTP Mode On (EBH)

This command is used to turn OTP mode on. (Initial status)

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	1

OTP Mode Off (EAH)

This command is used to turn OTP mode off

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	0

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Offset Volume Set (EDH)

This command is used to set offset value x (-32 to +31) to electronic volume by 2s complement.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	0	1
0	0	0	0	P15	P14	P13	P12	P11	P10

0 : OTP cell is able to be programmed
1 : OTP cell isn't able to be programmed

P15	P14	P13	P12	P11	P10	Offset Volume(x)
0	1	1	1	1	1	31
:	:	:	:	:	:	
0	0	0	0	0	1	1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
:	:	:	:	:	:	:
1	0	0	0	0	0	-32

OTP Write Enable (EFH)

This command is used to write offset value (OV) into EPROM cells.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	1

INSTRUCTION PARAMETER

Table 16. Instruction Parameter

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02H	1	0	0	0	0	0	0	EXT	OSC
			*	*	*	*	*	*	0	0
Driver Output Mode Set	10H	1	0	0	DLN		0	SDIR	SWP	CDR
			*	*	0	0	*	0	0	0
Monitor Signal Control	18H	1	0	0	0	0	0	PM	CL	FR
			*	*	*	*	*	0	0	0
DC-DC Set	20H	1	0	0	0	0	DC(2)		DC(1)	
			*	*	*	*	0	0	0	0
Bias Set	22H	1	0	0	Bias(2)		0	0	Bias(1)	
			*	*	0	0	*	*	0	0
DCDC Clock Division Set	24H	1	0	0	DIV(2)		0	0	DIV(1)	
			*	*	1	0	*	*	1	0
DCDC and AMP ON/OFF Set	26H	1	0	0	0	0	AMP	DCDC3	DCDC2	DCDC1
			*	*	*	*	0	0	0	0
Temperature Compensation Set	28H	1	0	0	0	0	0	0	TCS	
			*	*	*	*	*	*	0	0
Contrast Control (1)	2AH	1	Contrast control value in normal and partial display mode 0 (0 to 255)							
			0	0	0	0	0	0	0	0
Contrast Control(2)	2BH	1	Contrast control value in partial display mode 1(0 to 255)							
			0	0	0	0	0	0	0	0
Addressing Mode Set	30H	1	0	GSM		DSG	SGF	SGP		SGM
			*	0	0	1	1	1	0	1
ROW Vector Mode Set	32H	1	0	0	0	0	INC			VEC
			*	*	*	*	1	1	1	0
N-line Inversion Set	34H	1	FIM	FIP	0	N-block Inversion				
			1	0	*	0	1	1	0	1
Frame Frequency Control	36H	1	0	0	0	0	0	0	0	LFS
			*	*	*	*	*	*	*	0
Entry Mode Set	40H	1	0	0	0	0	0	MDI	X/Y	RMW
			*	*	*	*	0	0	0	0
X-address Area Set	42H	2	X Start address set							
			0	0	0	0	0	0	0	0
			X end address set							
			1	0	1	0	0	0	0	1
Y-address Area Set	43H	2	Y start address set							
			0	0	0	0	0	0	0	0
			Y end address set							
			1	0	0	0	0	0	1	1
RAM Skip Area Set	45H	1	0	0	0	0	0	0	RSK	
			*	*	*	*	*	*	0	0
Specified Display Pattern Set	53H	1	0	0	0	0	0	0	SDP	
			*	*	*	*	*	*	0	0
Partial Display Mode Set	55H	1	0	0	0	0	0	0	PDM	PT
			*	*	*	*	*	*	0	0
Partial Display Start Line Set	56H	1	Partial start line							
			0	0	0	0	0	0	0	0
Partial Display End Line Set	57H	1	Partial end line							
			1	0	1	0	0	0	0	1

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Table 16. Instruction Parameter (Continued)

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Area Scroll Mode Set	59H	4	0	0	0	0	0	0	SCM	
			*	*	*	*	*	*	0	0
			Scroll area start line							
			0	0	0	0	0	0	0	0
			Scroll area end line							
			1	0	1	0	0	0	0	1
			Lower Fixed number							
			0	0	0	0	0	0	0	0
Scroll Start Line Set	5AH	1	Scroll start line							
			0	0	0	0	0	0	0	0
Offset Volume Set	EDH	1	1	1	1	0	1	1	0	1
			*	*	*	0	0	0	0	0

Reset Operation

When RSTB becomes "L", following procedure is occurred.
  - X start address: 0, X end address: 161,   - Y start address: 0, Y end address: 131
  - Display OFF
  - Read Modify Write Mode OFF
  - Function Mode Set
    MDI = 0: Memory Data Inversion OFF
    OSC = 0: Oscillator OFF
    EXT = 0: Internal Oscillator Mode
    REV = 0: Reversing mode OFF
    X/Y = 0: Y-address Count Mode
    Standby Mode ON
  - DCDC Clock Division Set
    DIV(1) = 10: fPCK = fOSC/64
    DIV(2) = 10: fPCK = fOSC/32
  - Duty Set
    Display Duty = 00: 1/132 duty
  - DC-DC Select
    DC(1) = 0: X1 step-up
    DC(2) = 0: X1 step-up
  - Bias Set
    Bias(1) = 0H: 1/4 bias
    Bias(2) = 0H: 1/4 bias
  - DC/DC and AMP ON/OFF Set
    AMP =0: Built-in OP-AMP OFF
    DCDC1 =0: Built-in 1'st booster OFF
    DCDC2 =0: Built-in 2'nd booster OFF
    DCDC3 =0: Built-in 3'rd booster OFF
  - N-block inversion
    FIM =1: Forcing Inversion ON
    FIP =0: Forcing Inversion Period in one frame
    N-block inversion = 0DH: 13 block inversion
  - Frame Frequency Control
    LFS =0: Low Frequency Set OFF
  - Partial Display Mode
    PT = 0: Partial Display Mode OFF
  - Partial Display Area Set
    Partial start line = 00H
    Partial end line = 81H
  -Area Scroll Set
    Mode = 00H : Entire Display Scroll Mode
    Area Start Line: 00H
    Area End Line: A1H
    Lower Fixed Line Number: 00H
  - Scroll Start Line Set
    Scroll Start Line: 00H
  - Addressing Mode Set
    GSM=00: 65,536 Color Mode
    DSG = 1: No dummy subgroup
    SGF = 1: SG Frame Inversion ON
    SGM = 1: SG Inversion Mode ON
    SGP=10: Different phase by 2pixel-unit
  - Row Vector Mode Set
     INC =111: Increment every sub-frame
     VEC=0: R1->R2->R3->R4->R1->…

POWER ON/OFF SEQENCE

Power ON Sequence

```
                    ┌─────────────┐
                    │  Power On   │
                    └─────────────┘
                           │
                           ▼
                    ┌─────────────┐
                    │    Reset    │
                    └─────────────┘
                           │
                           ▼
                    ┌─────────────┐
                    │  Waiting for │
                    │Releasing Reset│
                    └─────────────┘
                           │
                           ▼
                    ┌─────────────┐
                    │   Standby   │
                    │  mode OFF   │
                    └─────────────┘
            20ms           │
                           ▼
                    ┌─────────────┐
                    │   OSC ON    │
                    └─────────────┘
            20ms           │
                           ▼
                    ┌─────────────┐
                    │  DCDC1 ON   │
                    └─────────────┘
            20ms           │
                           ▼
                    ┌─────────────┐
                    │     AMP     │
                    │     ON      │
                    └─────────────┘
            20ms           │
                           ▼
                    ┌─────────────┐
                    │  DCDC2 ON   │
                    └─────────────┘
            20ms           │
                           ▼
                    ┌─────────────┐
                    │  DCDC3 ON   │
                    └─────────────┘
            20ms           │
                           ▼
        ┌───────────────────────────────────┐
        │ Set various registers and RAM data if needed │
        │        (Y/X,MDI,EXT,DIV,DLN,       │
        │     DC,FIM,FIP,N-block,PT,DSG,SGF,  │
        │    SGP,SGM, INC,VEC, Display Data)  │
        └───────────────────────────────────┘
           100ms          │
                           ▼
                    ┌─────────────┐
                    │  Display ON │
                    └─────────────┘
```
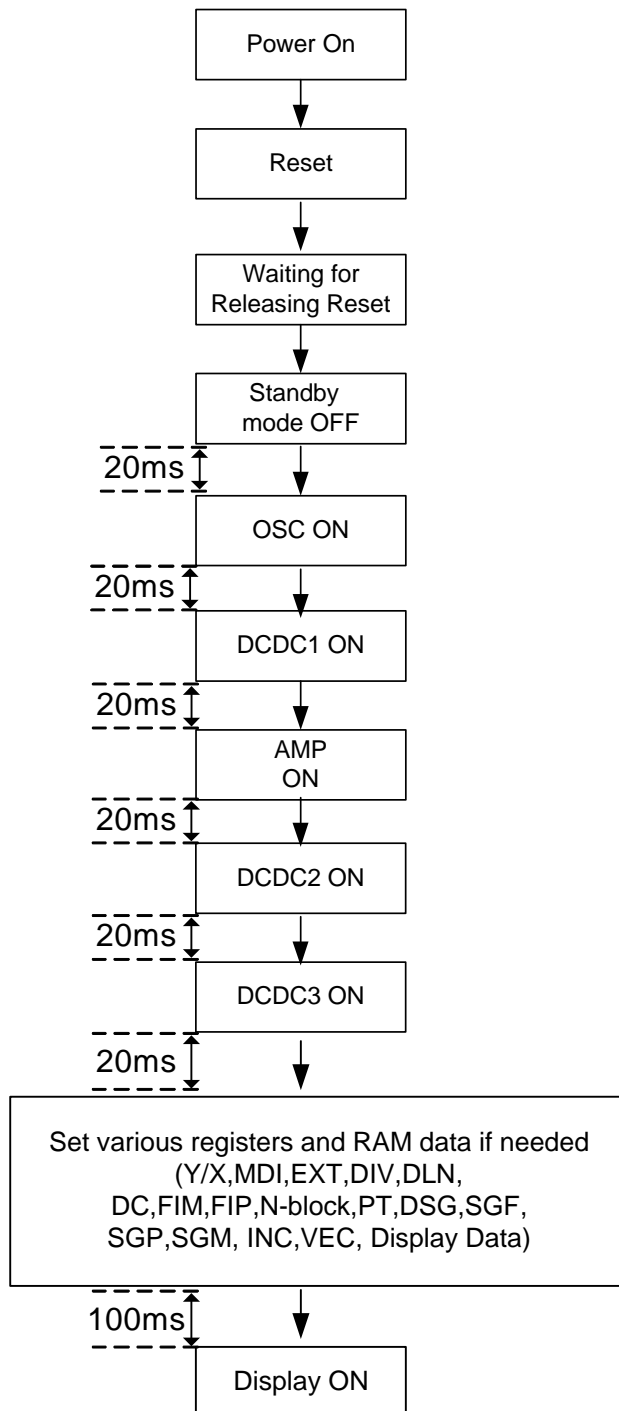
External Power Input Sequence

a) With Internal Regulator
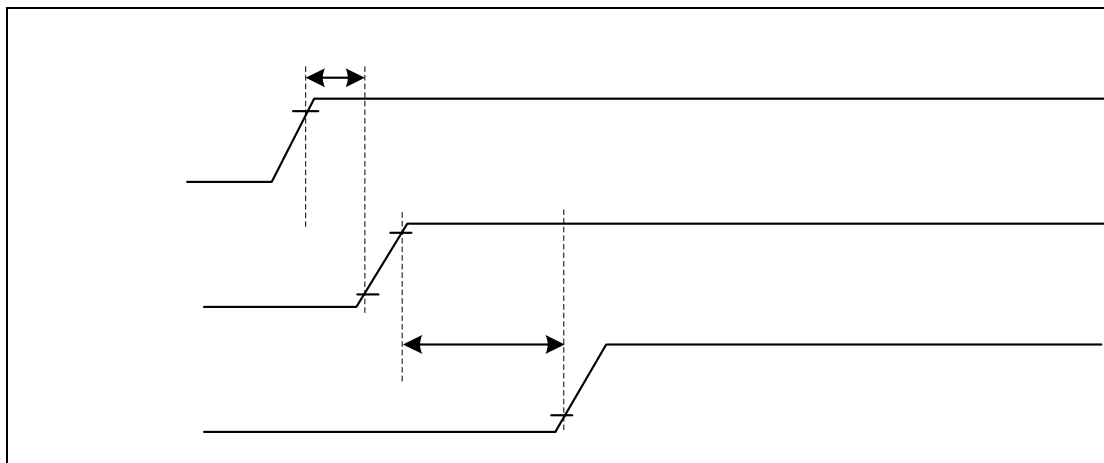
VDD3 must be applied earlier than VIN1/VIN1R/VIN1A or at least applied simultaneously with these signals. When C1 of figure 20. regulator application is 1μF, RSTB must be applied after VIN1/VIN1R/VIN1A have been applied. The applied time gap between VIN1/VIN1R/VIN1A and RSTB is minimum 2ms. As C1 becomes larger, this time gap must be increased. Otherwise function is not guaranteed.
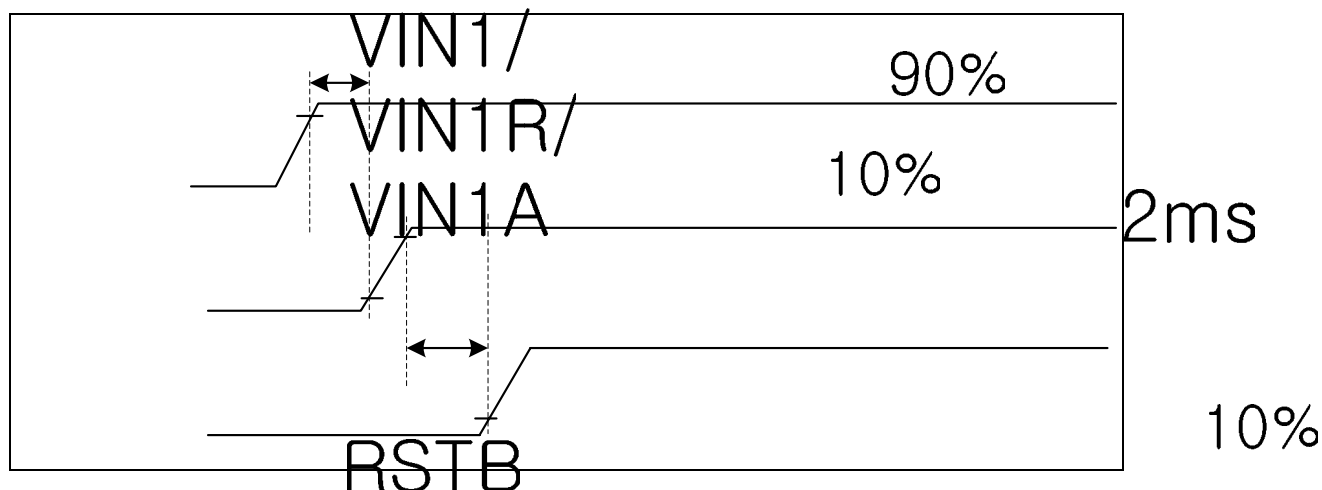
b) Without Internal Regulator

VDD3 must be applied earlier than VIN1/VIN1R/VIN1A or at least applied simultaneously with these signals. RSTB must be applied after VIN1/VIN1R/VIN1A have been applied. The applied time gap between VIN1/VIN1R/VIN1A and RSTB is minimum 1ms. Otherwise function is not guaranteed.

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Power OFF Sequence

Normal Case

```
┌─────────────────────────────┐
│        Stanby ON            │
│ ( Display Off, DCDC3 Off,   │
│    DCDC2 Off, AMP Off,      │
│    DCDC1 Off, OSC Off)      │
└─────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────┐
│         Discharge           │                300ms
└─────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────┐
│   Trun off the power voltage│
└─────────────────────────────┘
```

Emergency Case

```
┌─────────────────────────────┐
│   Turn off the power voltage│
└─────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────┐
│          RSTB = L           │
└─────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────┐
│        Stanby ON            │
│ ( Display Off, DCDC3 Off,   │
│    DCDC2 Off, AMP Off,      │
│    DCDC1 Off, OSC Off)      │
└─────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────┐
│         Discharge           │
└─────────────────────────────┘
```


Power voltage — GND: Turn off the power voltage suddenly

RSTB — GND: RSTB is input as soon as possible

COM/SEG Driver Output (VRP) — GND
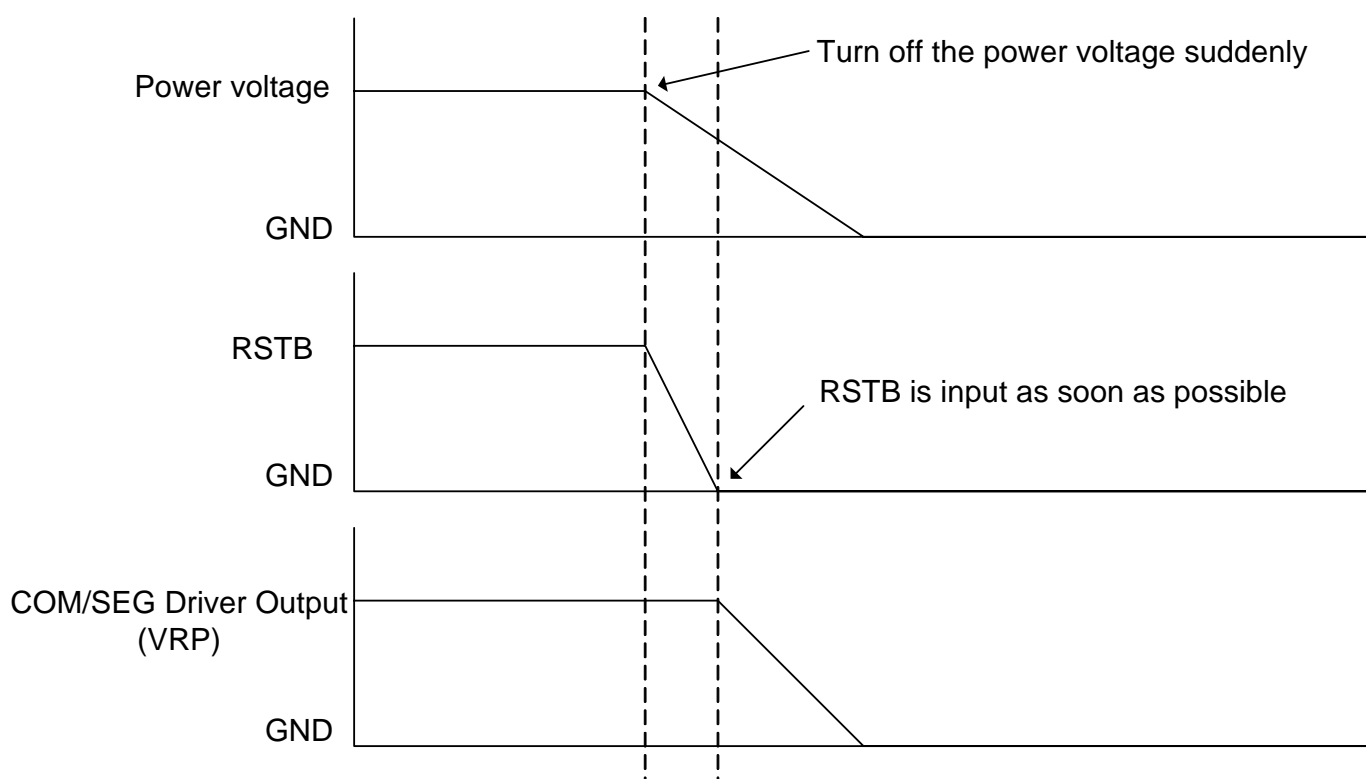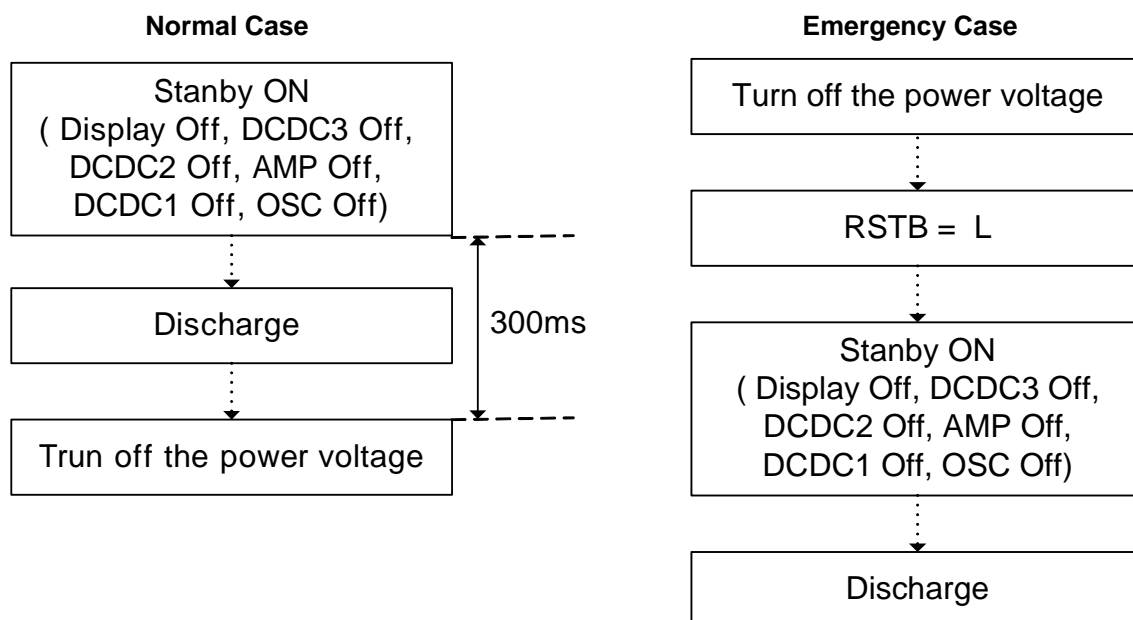
Note: When the signal of the hardware reset comes during the power-off period, COM/SEG output is forcibly lowered to the GND levels. Discharge resistor must be added at VCC pin. Refer application system diagram.

External Power Off Sequence

a) With Internal Regulator
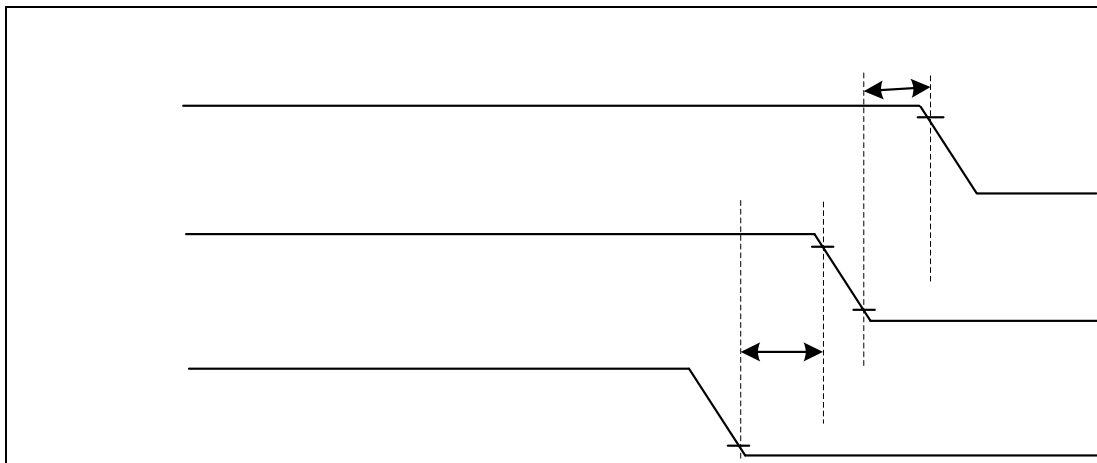
VDD3 must be powered down later than VIN1/VIN1R/VIN1A or at least powered down simultaneously with these signals. VIN1/VIN1R/VIN1A must be powered down after RSTB have been powered down. The time gap of powered down between RSTB and VIN1/VIN1R/VIN1A is minimum 1ms. Otherwise function is not guaranteed.

b) Without Internal Regulator

VDD3 must be powered down later than VIN1/VIN1R/VIN1A or at least powered down simultaneously with these signals. VIN1/VIN1R/VIN1A must be powered down after RSTB have been powered down. The time gap of powered down between RSTB and VIN1/VIN1R/VIN1A is minimum 1ms. Otherwise function is not guaranteed.

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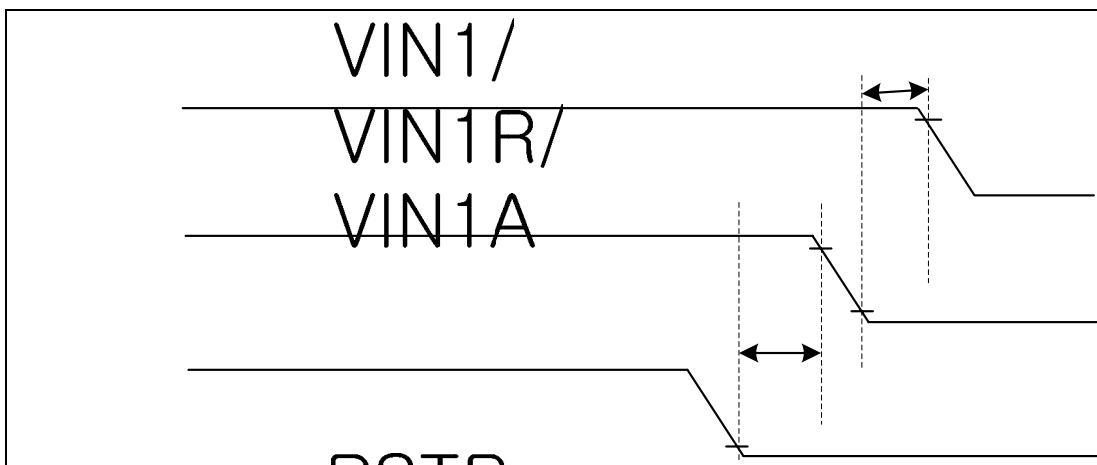
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage range	VDD3	-0.3 to +4.0	V
	VDD	-0.3 to +2.3	
	VIN1	-0.3 to +4.0	
LCD Supply Voltage range	|VCC – VEE|	22	V
Input Voltage range	Vin	- 0.3 to VDD3 +0.3	V
Operating Temperature range	T_{OPR}	-30 to +70	°C
Storage Temperature range	T_{STR}	-55 to +150	°C

OPERATING VOLTAGE

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD3 (*1)	1.65	-	3.3	V
Supply Voltage (2)	VDD	1.65	-	1.95	V
Supply Voltage (3)	VIN1 (*2)	2.4	3.0	3.6	V
Supply Voltage (4)	VIN2	2.4	3.0	5.5	

(*1) When VDD3 = 1.65 to 1.95 [V], VDD = VDD3 (No using Internal Regulator, REG_ENB = "VDD3")
    When VDD3 > 1.95 [V], VDD = REG_OUT (Using Internal Regulator, REG_ENB = "VSS")
(*2) VIN1 = VIN1R, VIN1A

DC CHARACTERISTICS (1)

(Vss = 0V, V$_{DD3}$ = 1.65 to 3.3V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Operating voltage		VDD3(*1)		1.65		3.3	V	VDD3
Operating voltage		VDD		1.65		1.95	V	VDD
Operating voltage		VIN1		2.4	-	3.6	V	VIN1,VIN1A
Operating voltage		VIN2		2.4	-	5.5	V	
Operating voltage		VIN45		2.4	-	5.5	V	VOUT45
Operating voltage		DC2IN	1/4 Bias	1.5	-	3.0	V	DC2OUT
			1/5 Bias	2.0	-	4.0		
			1/6 Bias	1.67	-	3.33		
			1/7 Bias	2.0	-	4.0		
Operating voltage		2Vr	2Vr = |(+VR)- (-VR)|	4.0	-	20	V	+VR, -VR
Output voltage		VREG	REG_OUT voltage	1.8 $\pm$ 0.15			V	VREG
Driving voltage input range		VM	External power supply mode	1.0		2.0	V	VMOUT
		VCC		5.0		12.0	V	VRP
		VEE		-3.0		-8.0	V	VRN
Input voltage	High	V$_{IH}$		0.8VDD3	-	VDD3	V	
	Low	V$_{IL}$		VSS	-	0.2VDD3		
Output voltage	High	V$_{OH}$	IOH = 0.5mA	0.8VDD3	-	VDD3	V	
	Low	V$_{OL}$	IOL = 0.5mA	VSS	-	0.2VDD3		
Input leakage current		I$_{IL}$	VIN = VDD or VSS	-1.0	-	+1.0	µA	
Output leakage current		I$_{OZ}$	VIN = VDD or VSS	-3.0	-	+3.0	µA	
Oscillator Frequency Tolerance	Normal or Partial 0	F$_{OSC1}$	(*R1)=TBD Ohm, (fFR=80Hz target), DSG=0, 162 Duty, Vdd3=3V, Ta=25°C	253.4	281.6	309.7	kHz	OSC1 - OSC2
	Partial 1	F$_{OSC2}$	(*R1)=TBD Ohm, (fFR=60Hz target), DSG=0, 66 Duty Vdd3=3V, Ta=25°C	79.5	88.3	97.2	kHz	OSC3 - OSC4
Oscillator Frequency Range	Normal or Partial 0	F$_{OSC1}$	(*2)	207.3		518.4	kHz	OSC1 - OSC2
	Partial 1	F$_{OSC2}$	(*3)	56.3		168.9	kHz	OSC3 - OSC4
Driving voltage input range		V1		2.0	-	4.0	V	
		VM		1.0		2.0		
Regulator output range		REG_OUT	REG_ENB = "L"	1.65	1.8	1.95	V	

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Note : (*R1),(*R2) resistances are only recommended to get target frame frequency. But the value is not absolute.
   (*1) When VDD3 = 1.65 to 1.95 [V], VDD = VDD3 (No using Internal Regulator, REG_ENB = "VDD3")
        When VDD3 > 1.95 [V], VDD = REG_OUT (Using Internal Regulator, REG_ENB = "VSS")
   (*2) Minimum oscillator frequency range is defined at fFR=60Hz and display line number=96
        Maximum oscillator frequency range is defined at fFR=150Hz and display line number=162
   (*3) Minimum oscillator frequency range is defined at fFR=40Hz and display line number=66
        Maximum oscillator frequency range is defined at fFR=120Hz and display line number=66

DC CHARACTERISTICS (2)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	R_{ON-Seg}	V1=3.0 V, V0=0V, Ta = 25°C, Iload=50uA	-	1.5	2.0	kΩ	SEGn
	COM	R_{ON-Com}	VCC=10.5 V, VM=1.5V, VEE=-7.5V, Ta = 25°C, Iload=100uA	-	1.0	1.5	kΩ	COMn
Current consumption	Normal Mode	IDD	VDD3=VIN1=3.0V, V1=3.0V, Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=162 DSG=1 (No dummy) f_{OSC1}=172.8kHz (fFR=80Hz) No load, No access, All white pattern	-	TBD	TBD	μA	VDD3 + VIN1
	Partial1 Mode		VDD3=VIN1=3.0V, V1=3.0V, Bias(2)=1/5, DC(2)=x1.5, Ta=25°C, 1/66 duty f_{OSC2}=49.28kHz (fFR=60Hz) No load, No access, All white pattern	-	TBD	TBD	μA	

* : "IDD" is determined from lowest power consumption for dc-dc converter.

DC CHARACTERISTICS (3)

(Vss = 0V, V$_{DD3}$ = 1.65 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 $^\circ$C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ (+VR)	Isource = 80uA	-	-	200	mV	+VR
	Δ (V1)	Isource = 250uA	-	-	50	mV	V1
	Δ (VM)	Isource,sink = 250uA	-	-	50	mV	VM
	Δ (-VR)	Isink = 80uA	-	-	200	mV	-VR

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
  Refer to the following figure. (in case of source current mode)
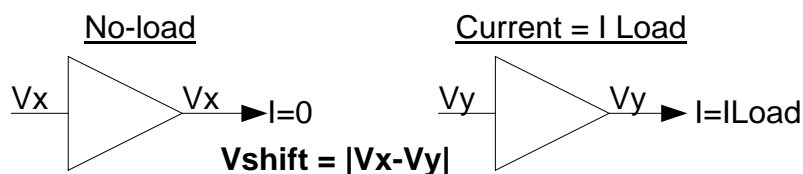
Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ (+VR)_0 Δ (-VR)_0(*1)	No load	-200	-	+200	mV	+VR -VR

(*1) Tolerance of bias ratio definition
  Δ (+VR)_0 = ((+VR) - VM) – VM / Bias
  Δ (-VR)_0 = (VM - (-VR)) – VM / Bias

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DC CHARACTERISTICS (4)

(Vss = 0V, V$_{DD3}$ = 1.65 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Remarks
Temperature compensation	ΔVt	VDD3=VIN1=V1=3.0V, -20 to 70 °C		-0.02	-	+0.02	%/°C	V1
Tolerance of Contrast step of V1	ΔVstep			3.92	7.84	11.76	mV	V1
Voltage range	ΔV1 ΔVM	Contrast set = FFh	V1	3.95	4.00	4.05	V	V1
			VM	1.95	2.00	2.05	V	VM
		Contrast set = 00h	V1	1.95	2.00	2.05	V	V1
			VM	0.95	1.00	1.05	V	VM

Item		Condition		Max	Unit	Ref
		Load current	Voltage range			
Offset Voltage	||+VR-VM| -|VM -(-VR)||	I Load = +100uA (+VR) I Load = -100uA (-VR)	+VR=5.0~12.0 V V1=2.0~4.0V VM=1.0~2.0V -VR=-3.0~-8.0 V	150	mV	Fig.1
	||V1-VM| -|VM-V0|| A	I Load = +100uA (V1, VM)		50	mV	Fig.2
	B	I Load = +100uA (+VR) I Load = -100uA (-VR)				
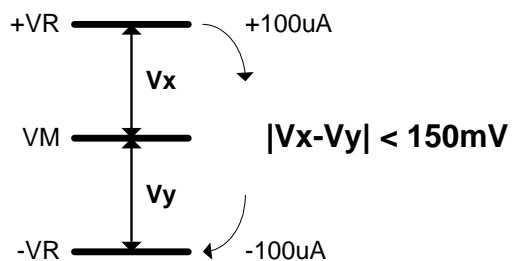
Fig. 1: Offset voltage definition (+VR,VM,-VR)
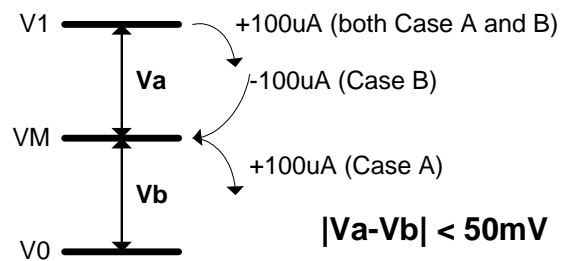
Fig. 2: Offset voltage definition (V1,VM,V0)

DC CHARACTERISTICS (5)

(Vss = 0V, V$_{DD3}$ = 1.65 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 $\degree$C)

Item		Range	
		Min	Max
Voltage Level	V1OUT	2.0 V	4.0 V (DC(1) and DC(2) = X2) (*1)
	VMOUT	1.0 V	2.0 V (DC(1) and DC(2) = X2) (*2)
	DC2OUT	1.5V (1/4 Bias, V1OUT = 2V)	4.0V (DC(1) and DC(2) = X2) (*3) (1/5 bias, V1OUT = 4V)

(*1) This definition is shown as below

VIN45

Delta V

V1OUT

Delta V > 0.3 V (External VIN45)

Delta V > 0.5 V (VIN45 = VOUT45)
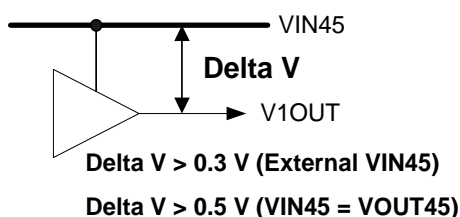
If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1

V1OUT Output

VIN45

VIN45 - Delta V

VIN45

V1OUT Input

Fig. 1

(*2) This definition is shown as below

VIN1

Delta V

VMOUT

Delta V > 0.3 V
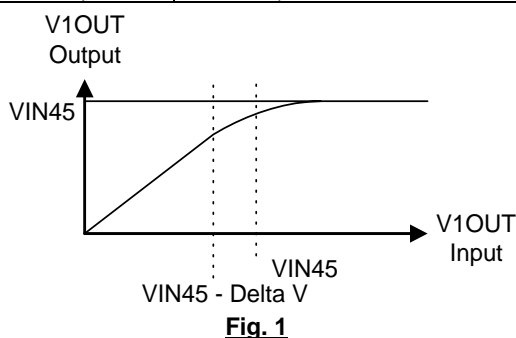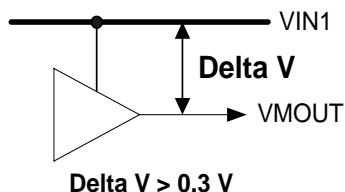
If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1.
In this case, VMOUT output level must not be unstable. Refer to Fig.2

VMOUT Output

VIN1

VIN1 - Delta V

VIN1

VMOUT Input

Fig. 2

(*3) This definition is shown as below

VIN2

Delta V

DC2OUT

Delta V > 0.3 V (External VIN2)

Delta V > 0.5 V (VIN2 = VOUT45)
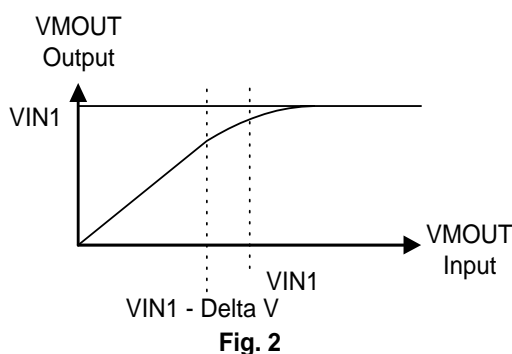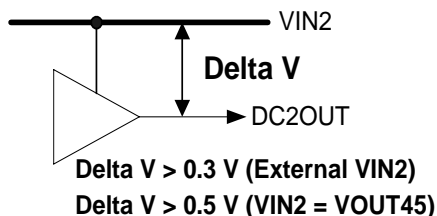
If DC2OUT input voltage is set over VIN2, DC2OUT output voltage must be clipped near VIN2. In this case, DC2OUT output level must not be unstable. Refer to Fig.3

DC2OUT Output

VIN2

VIN2 - Delta V

VIN2

DC2OUT Input

Fig. 3

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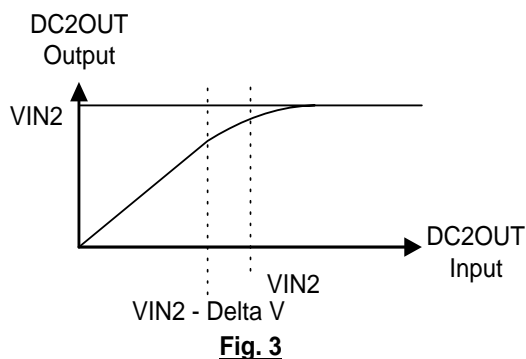
AC CHARACTERISTICS

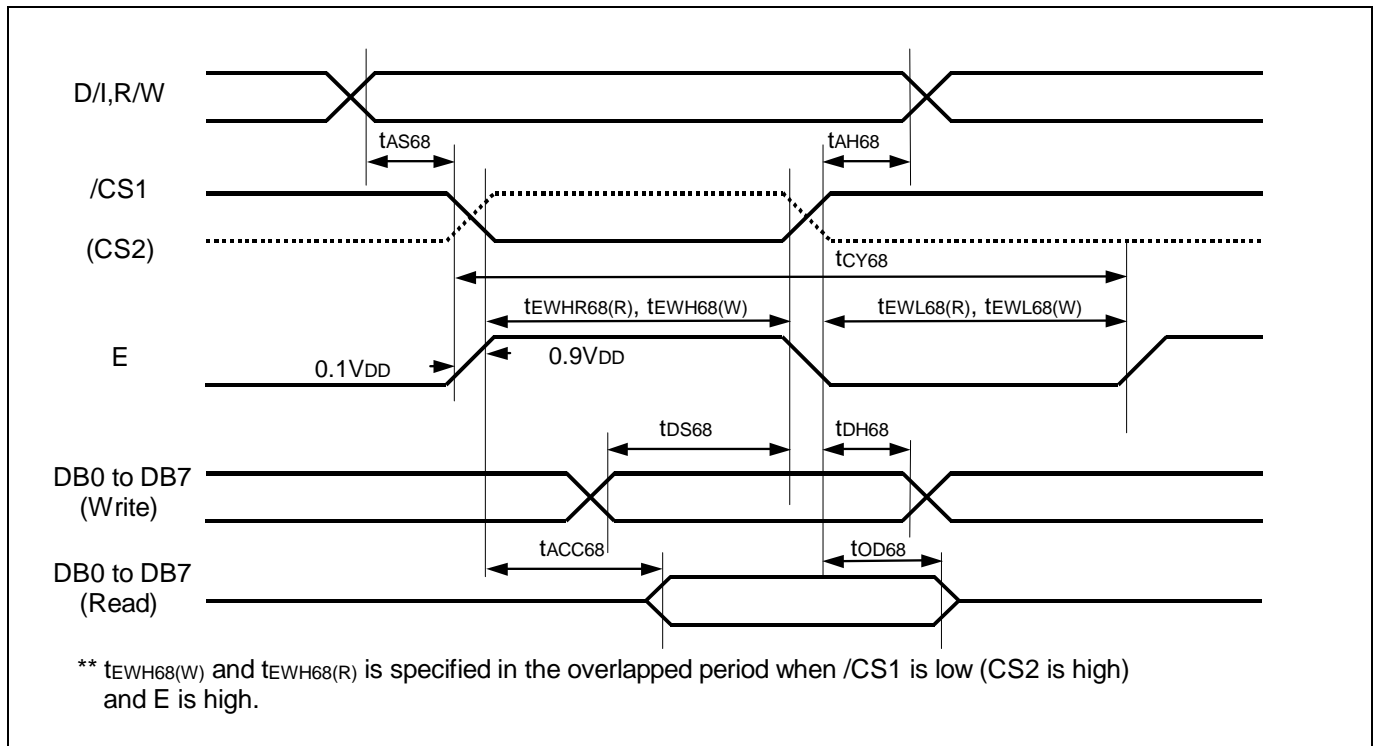### Read / Write Characteristics (8080-series MPU)
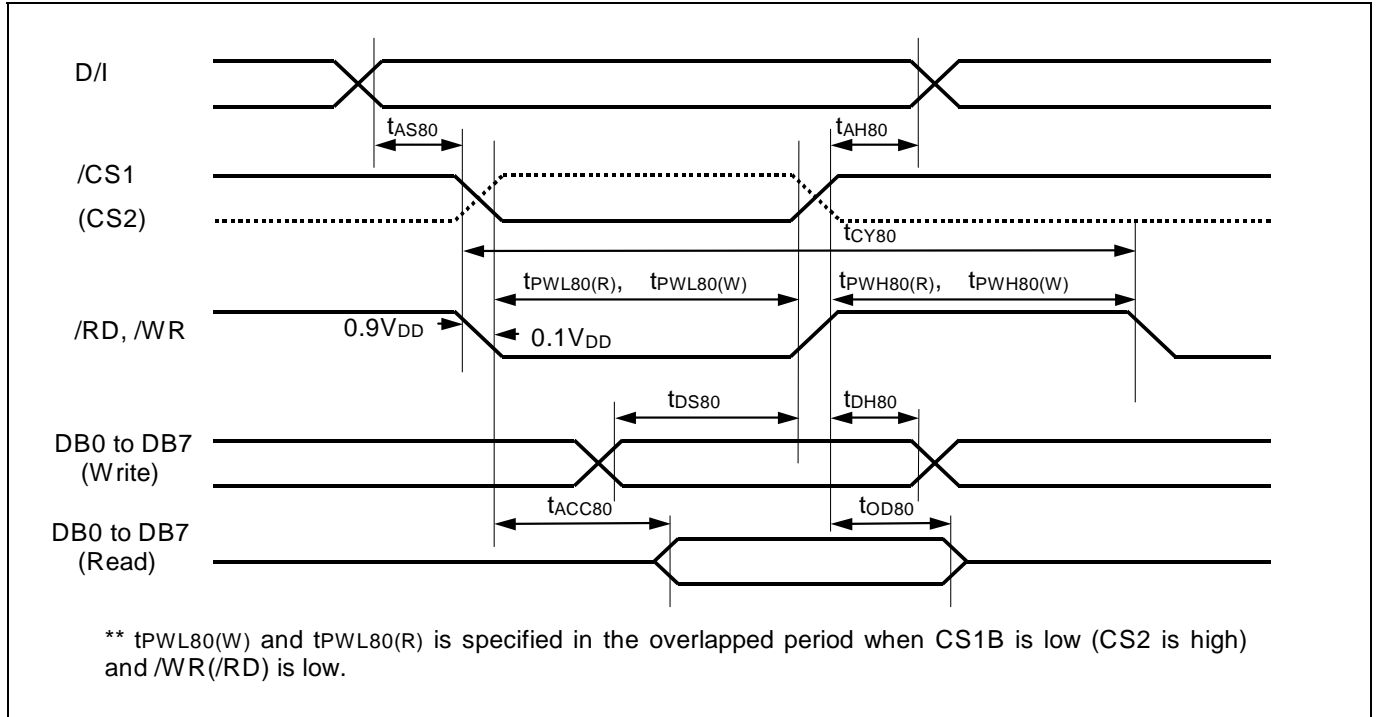
Figure 24.Parallel Interface (8080-series MPU) Timing Diagram

Table 5.AC Characteristics (8080-series Parallel Mode)

(V_{DD3} = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	D/I	t_{AS80} t_{AH80}		TBD TBD		ns
System cycle time(Write)		t_{CY80}		TBD		ns
Pulse width low for write Pulse width High for write	WRB (WRB)	$t_{PWL80(W)}$ $t_{PWH80(W)}$		TBD TBD		ns
Pulse width low for read Pulse width high for read	RDB (RDB)	$t_{PWL80(R)}$ $t_{PWH80(R)}$		TBD TBD		ns
Data setup time Data hold time	DB0 to DB15	t_{DS80} t_{DH80}		TBD TBD		ns
Read access time		t_{ACC80}	CL = 100 pF		TBD	ns
Output disable time		t_{OD80}	no load	TBD		ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.

(tr + tf) < (tCY80 − tPWL80(W) − tPWH80(W)) for write, (tr + tf) < (tCY80 − tPWLR80 − tPWHR80) for read

Read / Write Characteristics (6800-series Microprocessor)

** $t_{EWH68(W)}$ and $t_{EWH68(R)}$ is specified in the overlapped period when /CS1 is low (CS2 is high) and E is high.

Figure 25.Parallel Interface (6800-series MPU) Timing Diagram

Table 6.AC Characteristics (6800-series Parallel Mode)

(VDD3 = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	D/I R/W	t_{AS68} t_{AH68}		TBD TBD		ns
System cycle time(Write)		t_{CY68}		TBD		ns
Enable width high for write Enable width low for write	RDB (E)	$t_{EWH68(W)}$ $t_{EWL68(W)}$		TBD TBD		ns
Enable width high for read Enable width low for read	RDB (E)	$t_{EWH68(R)}$ $t_{EWL68(R)}$		TBD TBD		ns
Data setup time Data hold time	DB0 to DB15	t_{DS68} t_{DH68}		TBD TBD		ns
Read access time		T_{ACC68}	C_L = 100 pF		TBD	ns
Output disable time		t_{OD68}	no load	TBD		ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.

     (tr + tf) < (t_{CY68} − $t_{EWH68(W)}$ − $t_{EWL68(W)}$) for write, (tr + tf) < (t_{CY68} − $t_{EWH68(R)}$ − $t_{EWL68(R)}$) for read

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Serial Data Interface (4 Pin) Timing
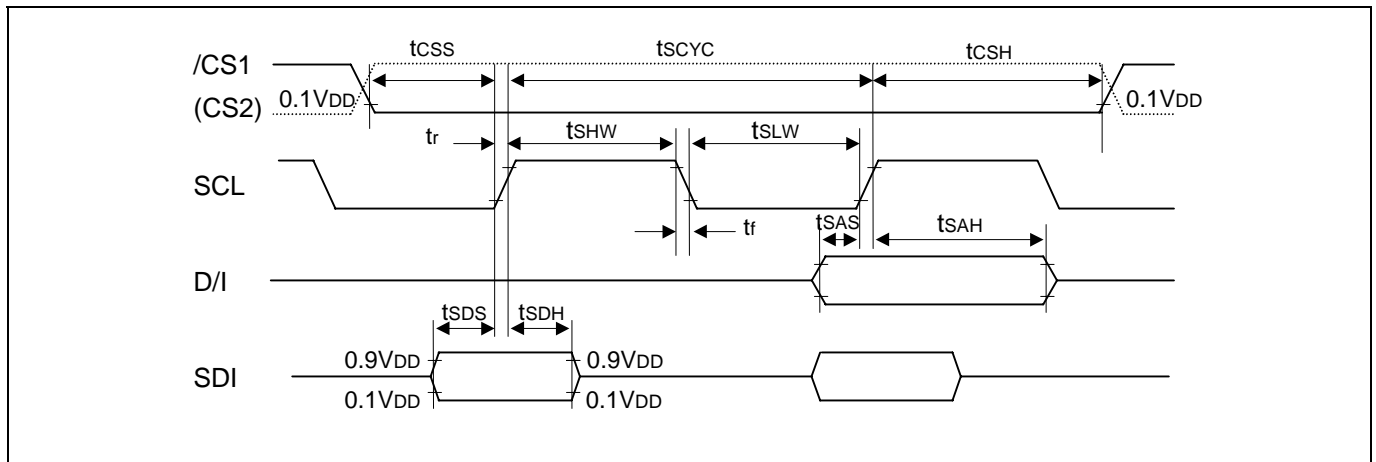
Figure 26.Serial Interface (4 Pin) Timing Diagram

Table 7.Serial Data Interface Timing

$(V_{DD3} = 1.65 \sim 3.3V, Ta = -30 \text{ to } +70°C)$

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	t_{SCYC}		TBD	ns
SCL High Pulse Width	SCL	t_{SHW}		TBD	ns
SCL Low Pulse Width	SCL	t_{SLW}		TBD	ns
SDI Setup time	SDI	t_{SDS}		TBD	ns
SDI Hold time	SDI	t_{SDH}		TBD	ns
D/I Setup time	D/I	t_{SAS}		TBD	ns
D/I Hold time	D/I	t_{SAH}		TBD	ns
Chip Select Setup time	CS1B (CS2)	t_{CSS}		TBD	ns
Chip Select Hold time	CS1B (CS2)	t_{CSH}		TBD	ns

Serial Data Interface (3 Pin) Timing
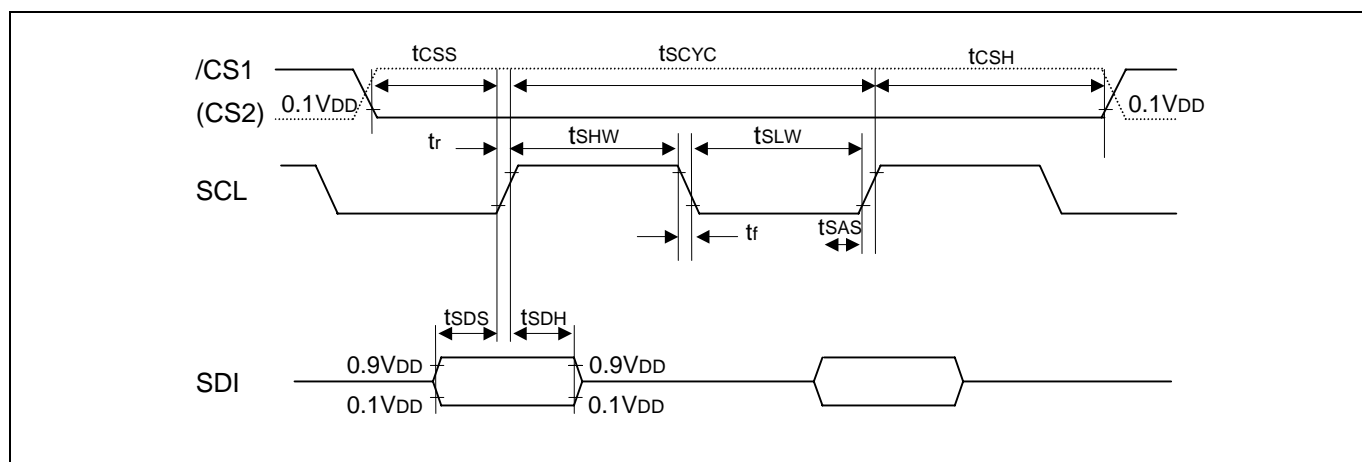
Figure 27.Serial Interface (3 Pin) Timing Diagram

Table 8.Serial Data Interface Timing

(V$_{DD3}$ = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	t$_{SCYC}$		TBD	ns
SCL High Pulse Width	SCL	t$_{SHW}$		TBD	ns
SCL Low Pulse Width	SCL	t$_{SLW}$		TBD	ns
SDI Setup time	SDI	t$_{SDS}$		TBD	ns
SDI Hold time	SDI	t$_{SDH}$		TBD	ns
Chip Select Setup time	CS1B (CS2)	t$_{CSS}$		TBD	ns
Chip Select Hold time	CS1B (CS2)	t$_{CSH}$		TBD	ns

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Reset Input Timing
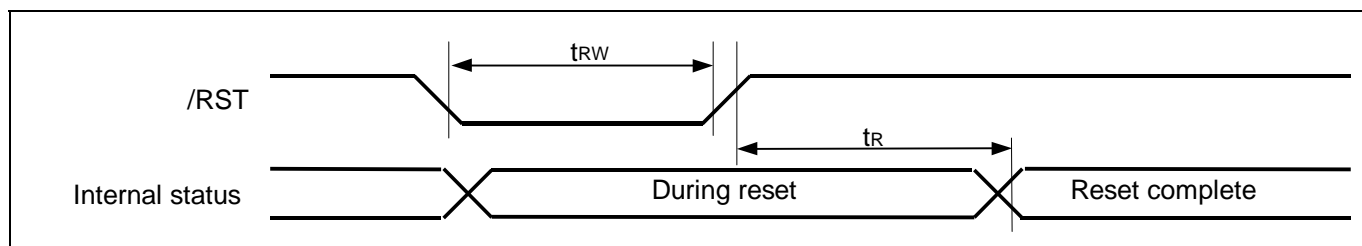
Figure 28.Reset Input Timing Diagram

Table 9.AC Characteristics (Reset mode)

(V$_{DD3}$ = 1.65 ~ 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RSTB	T$_{RW}$		1000	-	ns
Reset time	-	t$_R$		-	1000	ns

SYSTEM APPlication DIAgram

Internal Power Mode
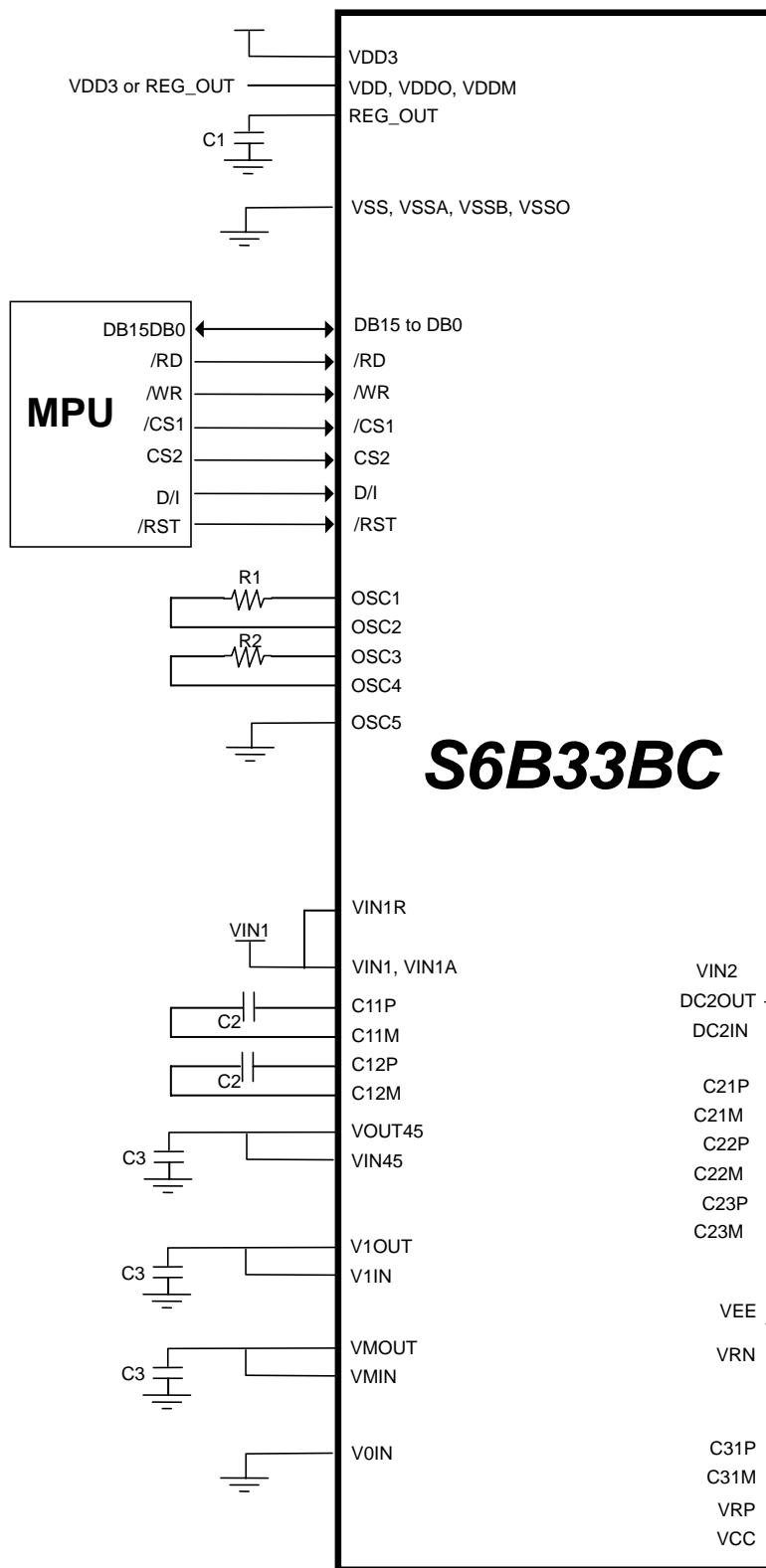
External Component

Name	Device
R1,R2	Resistors
C1,C2,C3	Capacitors
D1	Schottky barrier diode
Rd	Discharge Resistor

Values of external Components

Item	Capacitance
C1	1.0 to 4.7µF
C2	1.0 to 2.2µF
C3	1.0 to 2.2µF
D1	Vforward = Max. 0.3V at 1mA Vreverse = Min. 15V
Rd	Typ. 1M ohm

Note : Employing Rd is recommended when abnormal
l display occurs in recovery sequence after detaching battery.
(It depends on module or panel characteristics.)

Maximum rating voltage of capacitors

Item	Maximum rating voltage
REG_OUT to VSS	3V
VOUT45 to VSS	11V
C11P to C11M	6V
C12P to C12M	6V
VMOUT to VSS	3V
DC2OUT to VSS	5V
V1OUT to VSS	6V
C21P to C21M	5V
C22P to C22M	10V
C23P to C23M	13V
C24P to C24M	13V
VSS to VRN	13V
C31P to C31M	17V
VRP to VSS	18V

MPU

S6B33BC
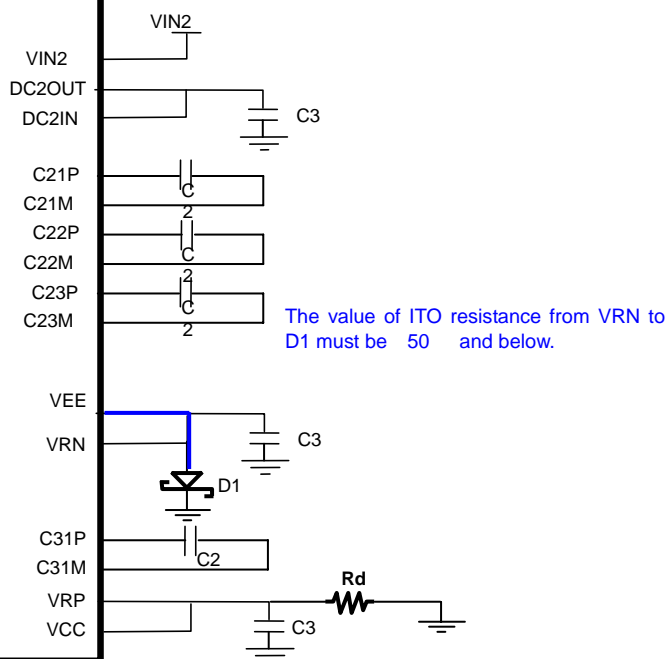
The value of ITO resistance from VRN to
D1 must be 50   and below.

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External Power Mode
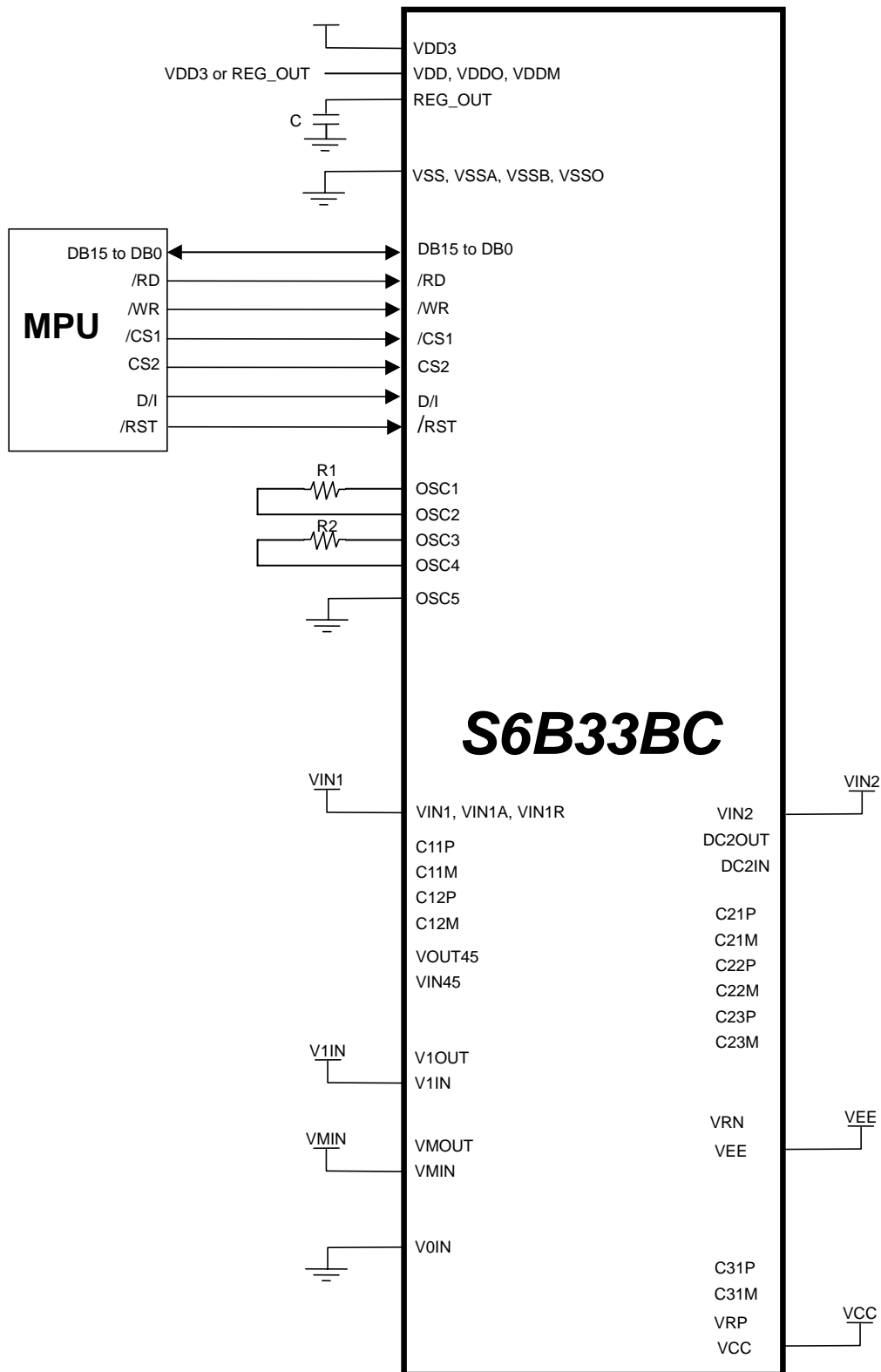
OTP calibration mode

SEQUENCE FOR SETTING THE MODIFIED ELECTRONIC VOLUME

- Next figure is a Block Diagram of Sequence for Setting the Modified Electronic Volume.
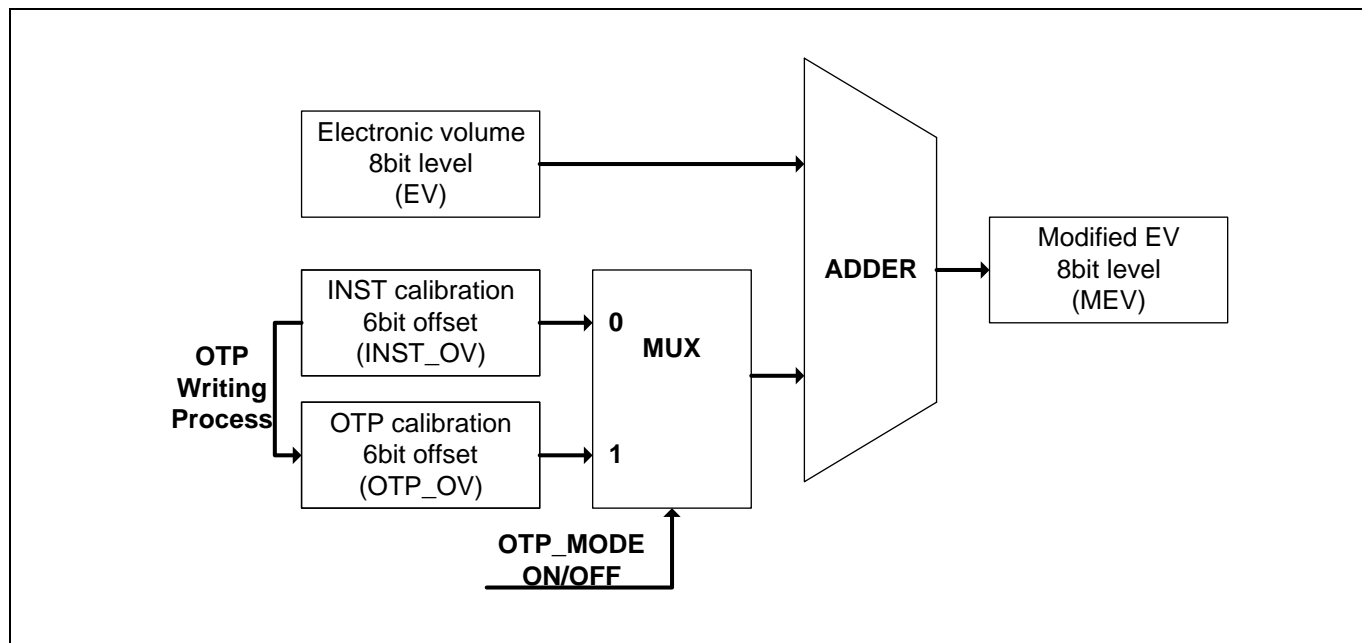

Figure 29. Sequence for Setting the Modified Electronic Volume

Initially, OTP cell is not programmed and has 6'b00000 value. When the external reset is applied, OTP mode is On. MEV is EV + OTP_OV. Since OTP_OV is 6'b00000, MEV is EV. For V1OUT calibration The instruction "OTP mode off" is executed, and then MEV is EV + OV and user can adjust MEV value using the instruction "Set offset volume register". When MEV overflows or underflows, MEV will be saturated. Repeat this step until end of the calibration. If V1OUT calibration is suitable, OTP writing process is executed, and then OTP cell is programmed and OTP_OV is programmed with OV. Finally, V1OUT calibration process is finished. Again, when the external reset is applied, OTP mode is ON. MEV is EV + OTP_OV. Accordingly MEV is the EV that has always the offset with OTP_OV value. However, if programmed OTP_OV is unlike, the instruction "OTP mode off" can be executed and then MEV will be EV + OV. Accordingly OV can be adjusted with instructions although OTP cell is programmed.

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EPROM CELL STRUCTURE

OTP (One Time Programmable) has been implemented on the S6B33B3. The EPROM stores the offset volume for V1OUT calibration after the device has been assembled and calibrated on a LCD module. For OTP programming, OTPD pin and OTPG pin are used. These pins should be available to on the module glass by ITO.

The OTP block of the S6B33B3 consists of 7 bits. 1 bit is used for OTP mode protection bit (OPRT), and 6 bits are used for V1OUT calibration (OV5~OV0). OPRT can be read or written automatically in this LSI.

EPROM block

MSB						LSB
OPRT	OV5	OV4	OV3	OV2	OV1	OV0

Description

OPRT : The Offset Volume(OV) can be written to EPROM cells only when OPRT bit = '0'

OV5~OV0 : The OV is used for calibrating the V1OUT voltage as an offset to the EV register value.

V1OUT CALIBRATION FLOW

V1OUT may be calibrated with OTP in the following order.(ex : EV = 32, OV=-3)

STEP	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1.											Apply external reset (OTP data read)
2.	0	0	0	0	1	0	1	0	1	0 or 1	Set contrast control 1 or 2 by using instruction (EV = 32)
	0	0	0	0	1	0	0	0	0	0	
3.	0	0	1	1	1	0	1	0	1	0	OTP mode off by using the instruction
4.	0	0	1	1	1	0	1	1	0	1	Set offset volume by using the instruction (OV = -3)
	0	0	0	0	1	1	1	1	0	1	
5											Repeat STEP 4. Until the end of the calibration
6.											Apply programming voltages for OTP programming (OTPG=12.5V,OTPD=12V)
7.	0	0	0	0	1	0	1	1	0	1	Standby on by using the instruction.
8	0	0	1	1	1	0	1	1	1	1	OTP write Enable **(Only available when OPRT= 0)**
9											Apply external reset
10.											Cut off programming voltages for OTP programming (OTPG,OTPD)

After the external reset, the calibrated data are automatically transferred to the 6-bit reference voltage control register.

*Step 6, 7, 8, 9 are OTP_WRITING PROCESS.

*OTP_WRITING PROCESS is available when OPRT is zero (if OPRT = 1, OTP cell could not be programmed).
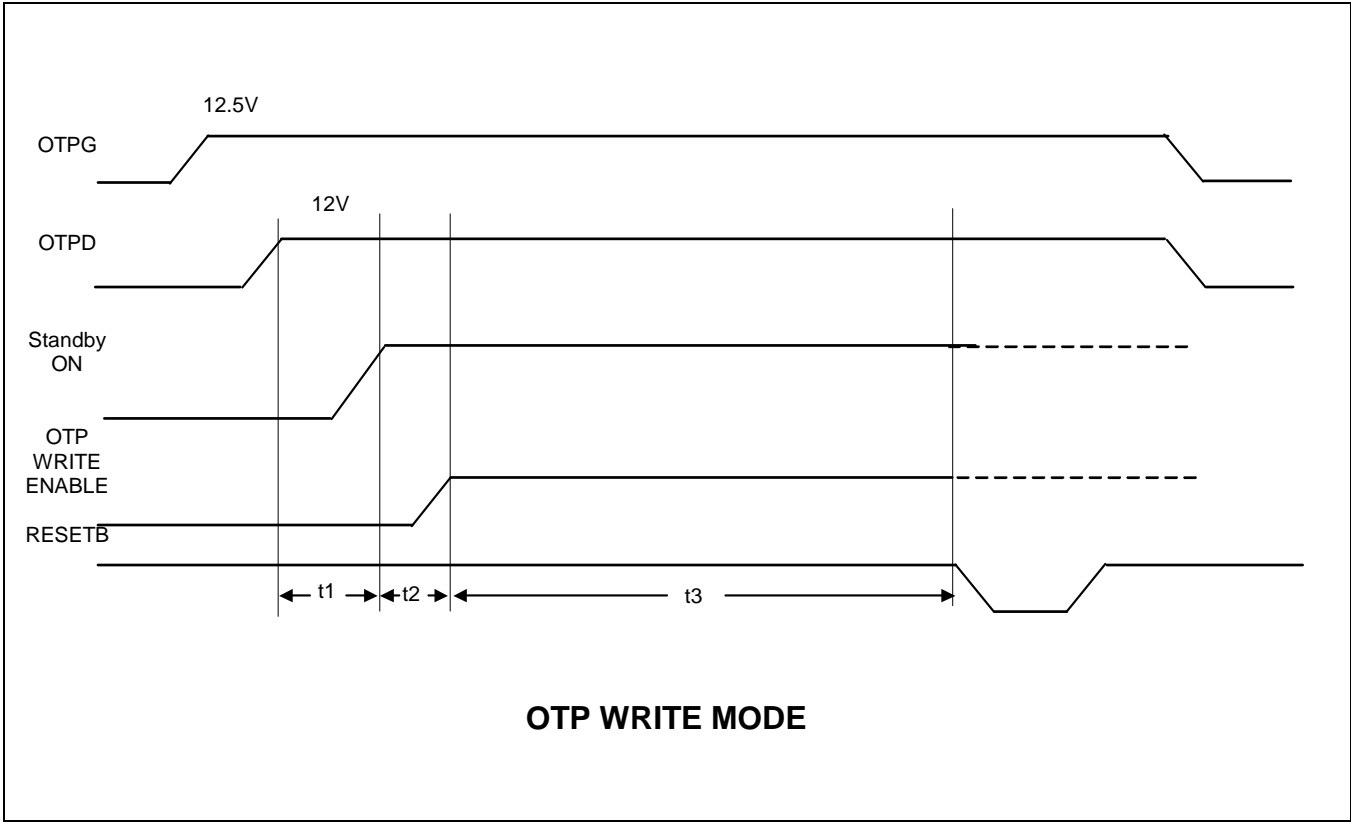
VOLTAGES AND WAVEFORMS FOR OTP PROGRAMMING

Figure 30. Voltages and waveforms for OTP programming (OTP Writing Process)

Specific timings (t1~t3)

Timing	Min	Max
t1,t2	100uS	-
t3	100mS	300mS

OTPG/D Voltage Tolerance

Item	Min	Typ	Max	Unit	Remarks
Tolerance of OTPG	12.4	12.5	12.6	V	±100mV
Tolerance of OTPD	11.9	12.0	12.1	V	±100mV

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Revision history

<table>
<tr><td colspan="4" align="center">S6B33BC Specification Revision History</td></tr>
<tr><td align="center">Version</td><td align="center">Content</td><td align="center">Author</td><td align="center">Date</td></tr>
<tr><td align="center">0.0</td><td>Original</td><td>D.C.Park</td><td>Jan.31. 2005</td></tr>
<tr><td align="center">0.1</td><td>1. Add pad configuration.

2. The range of power (VDD, VDD3) is modified.
  - Without internal regulator
  VDD : 1.8 ± 0.15 [V] (Typical : 1.8V) → VDD : 1.65 to 1.95 [V]
  VDD3: 1.8 to 3.3 [V] → VDD3: 1.65 to 3.3 [V]
  - Add the pin description of VDD3. (Page 12,26)
  VDD3 is more than VDD.</td><td>D.C.Park</td><td>Apr.1. 2005</td></tr>
<tr><td align="center">0.2</td><td>1. OTP writing time is modified from 50ms~1000ms to 100ms~300ms.
  (Page 67)
2. The interval time between set various registers and ram data and display on is modified from 300ms to 100ms. (Page 86)</td><td>D.C.Park</td><td>Apr.21. 2005</td></tr>
<tr><td align="center">0.3</td><td>1. Change Operating Voltage Range (VDD, VDD3) in Features (Page 1)
2. Change pad size of 1~16, 170~701 in Table 1.S6B33BCX Pad Dimensions (Page 4)
3. Change VDD3, VDD range in Figure 21 Regulator Application (page 26)
4. Change voltage name in power on/off sequence. (page 68, 70)
  VIN1/VIN1R/VIN1 → VIN1/VIN1R/VIN1A
5. Change VDD3 comment in Operating Voltage (page 71)
6. Change VDD3 comment in DC Characteristics (1) (page72~73)</td><td>D.C.Park</td><td>Jun.2. 2005</td></tr>
</table>