2020 DCS Lab 01

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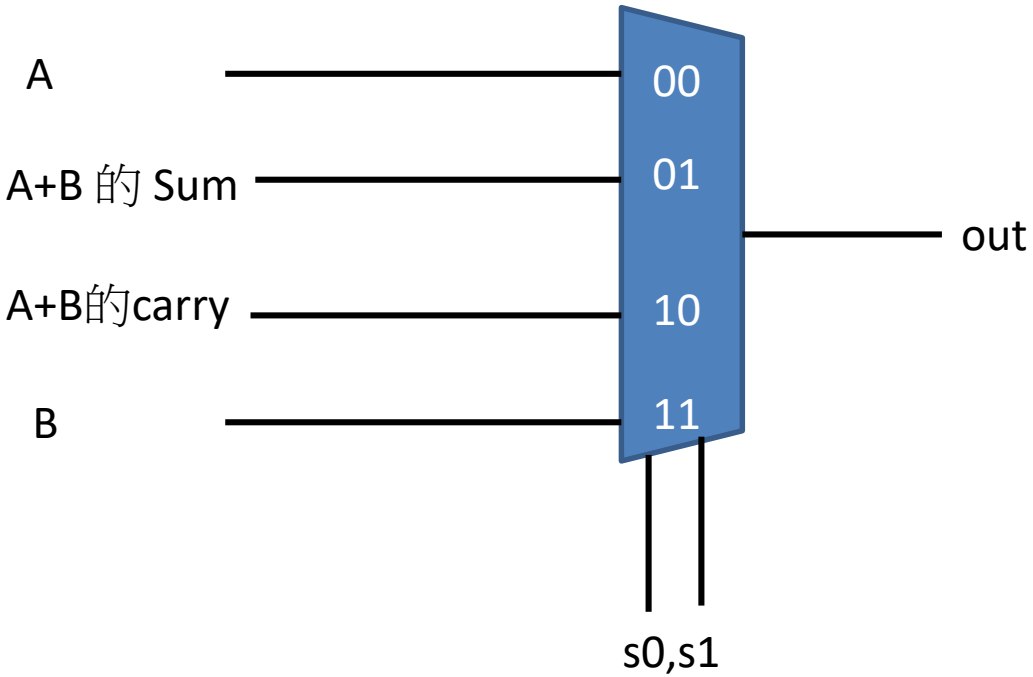
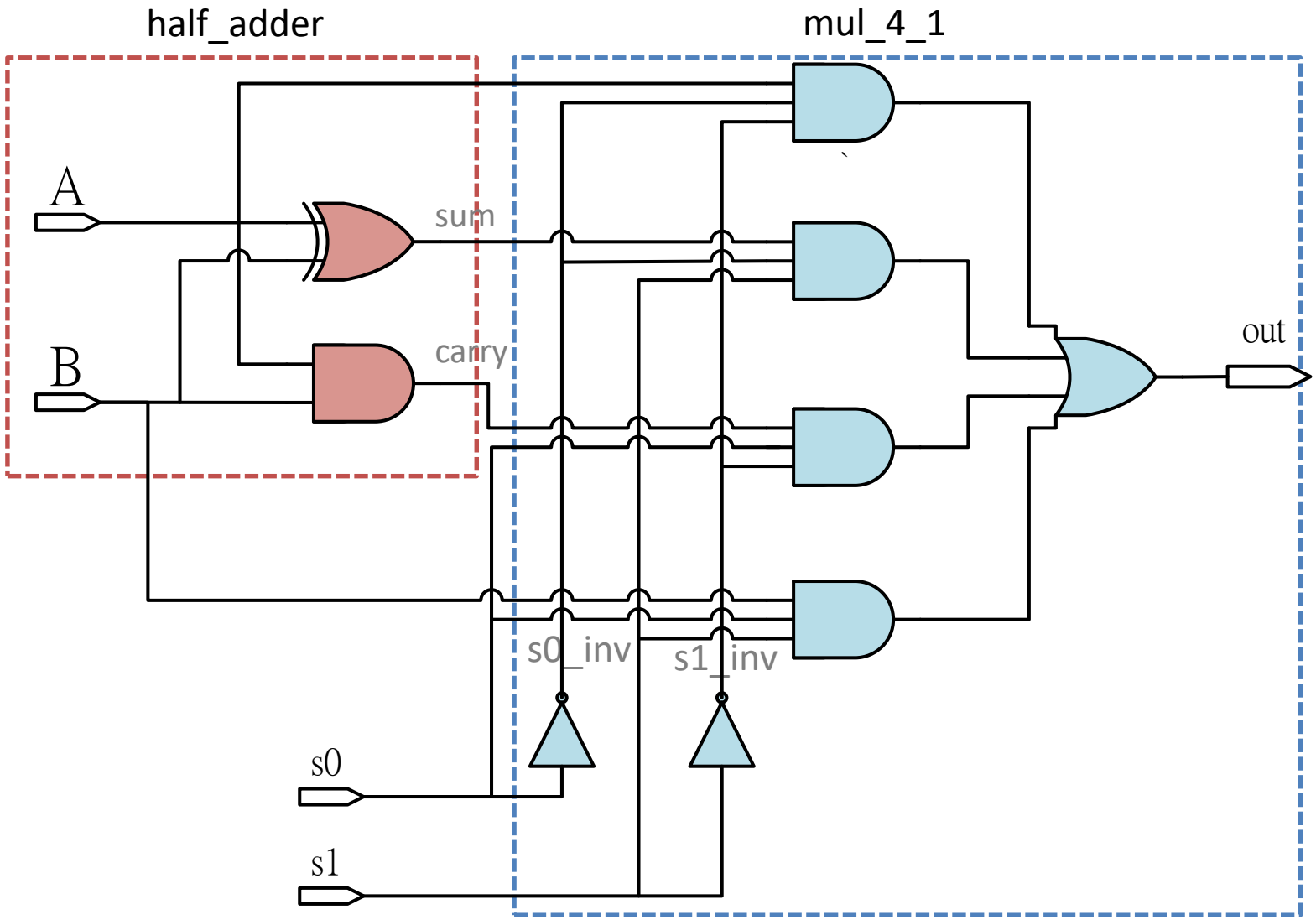
Lab01

- Gate level
- 使用以下gate去完成電路
  - buf(out,a,b)
  - not(out,a)
  - and(out,a,b,c)　(3 input or 2 input)
  - xor(out,a,b)
  - or(out,a,b)
- 可照助教提示切module或自行改寫
- tar –xvf ~dcsta01/Lab01.tar
  - 請在server上使用以上指令載下此次LAB

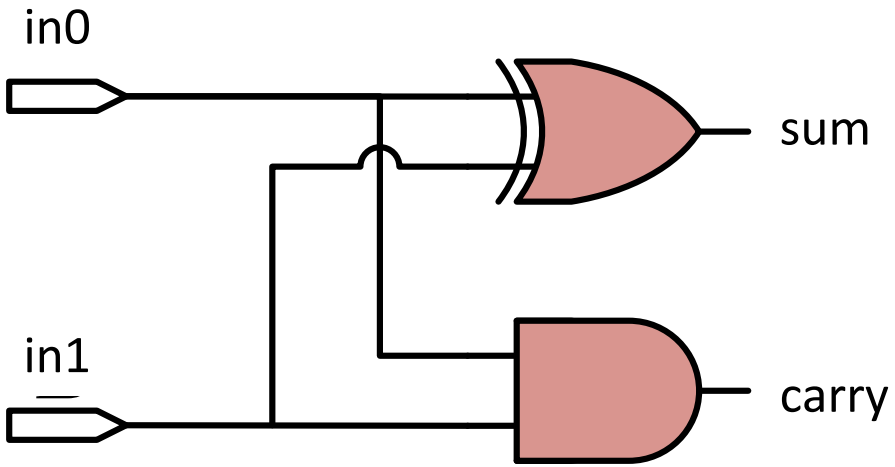
Lab01



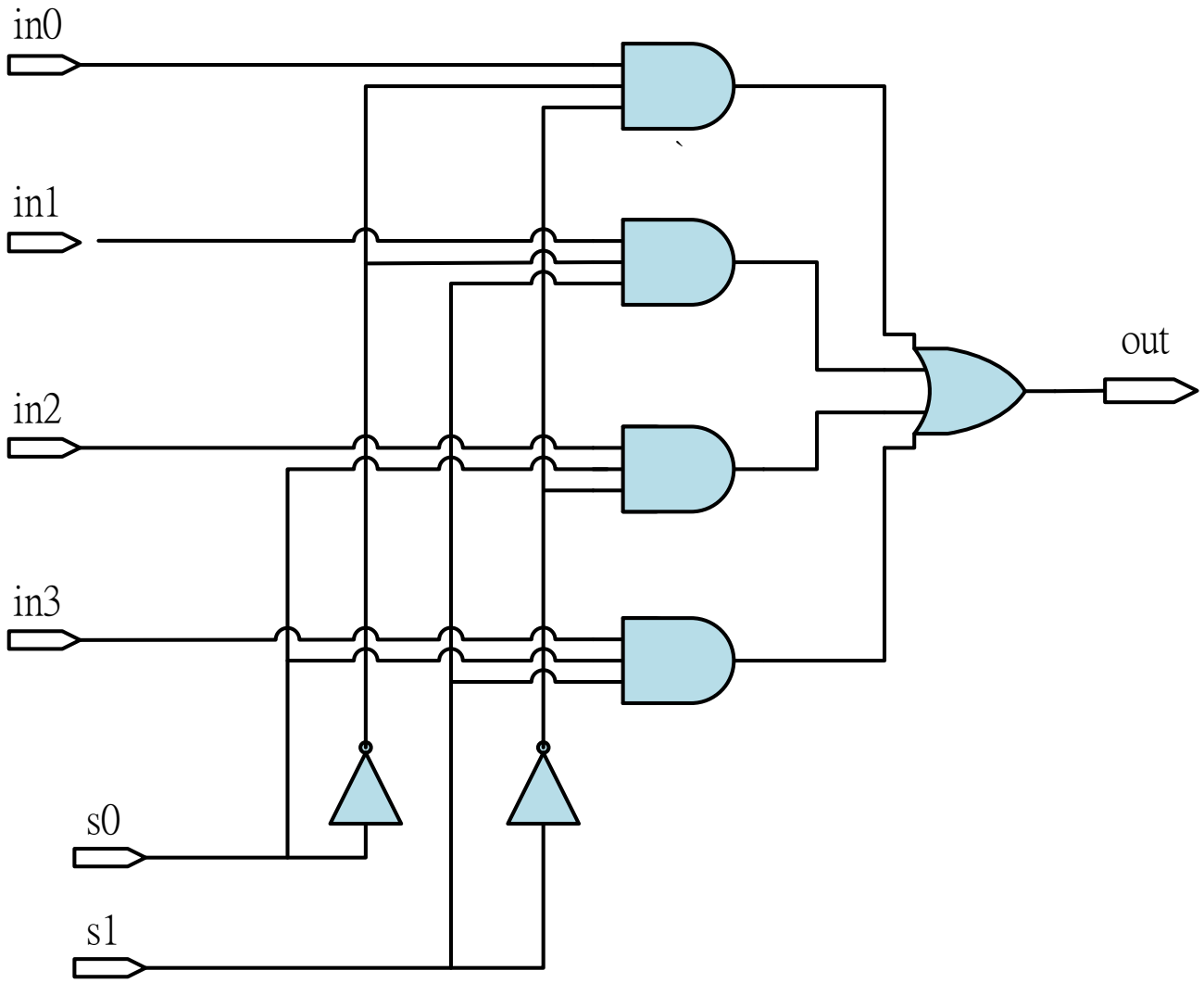
Lab01



half_adder



mul_4_1



Port

Input Signal	Bit Width	Definition
A,B,s0,s1	1	如第三頁圖

Output Signal	Bit Width	Definition
out	1	如第三頁圖

E3 rule

- 請使用system Verilog
- 使用09上傳