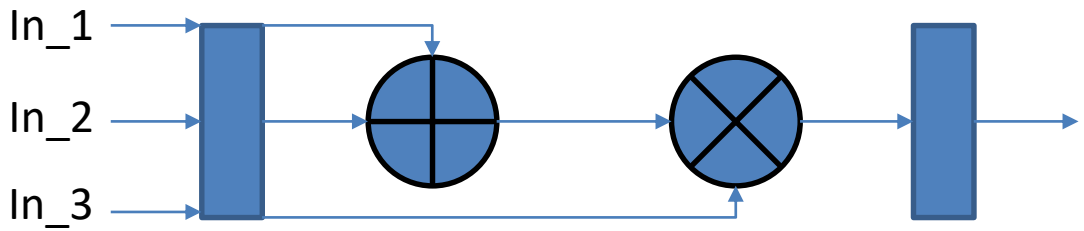
2021 DCS Lab 09

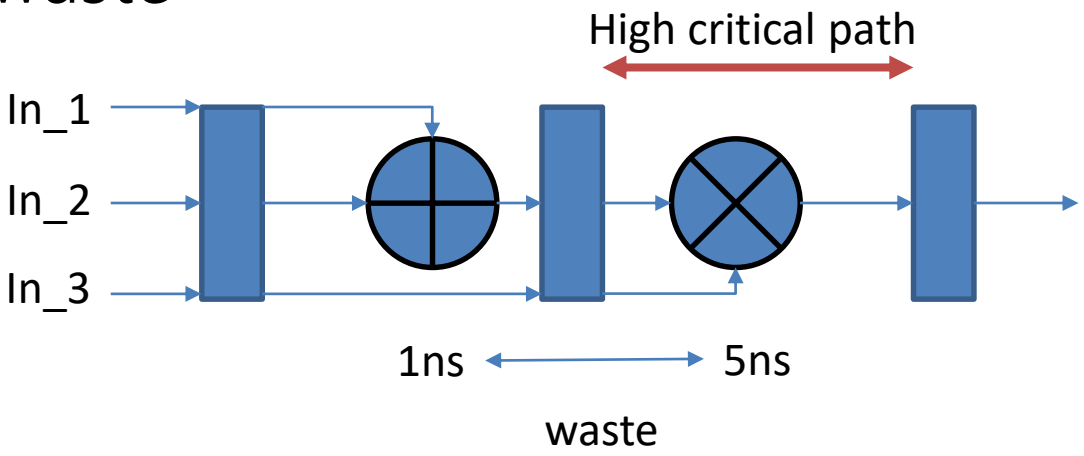
Unbalanced pipeline

Pipeline

- No pipeline, long critical path

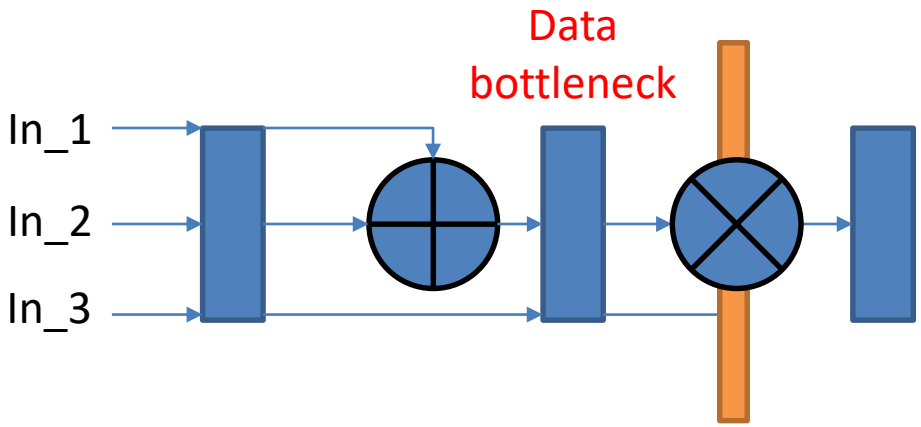


- Balanced pipeline, need higher clock period and waste



Unbalanced pipeline

- Unbalanced pipeline, more complex, higher area, lower clock period.



Pipeline Multiplier

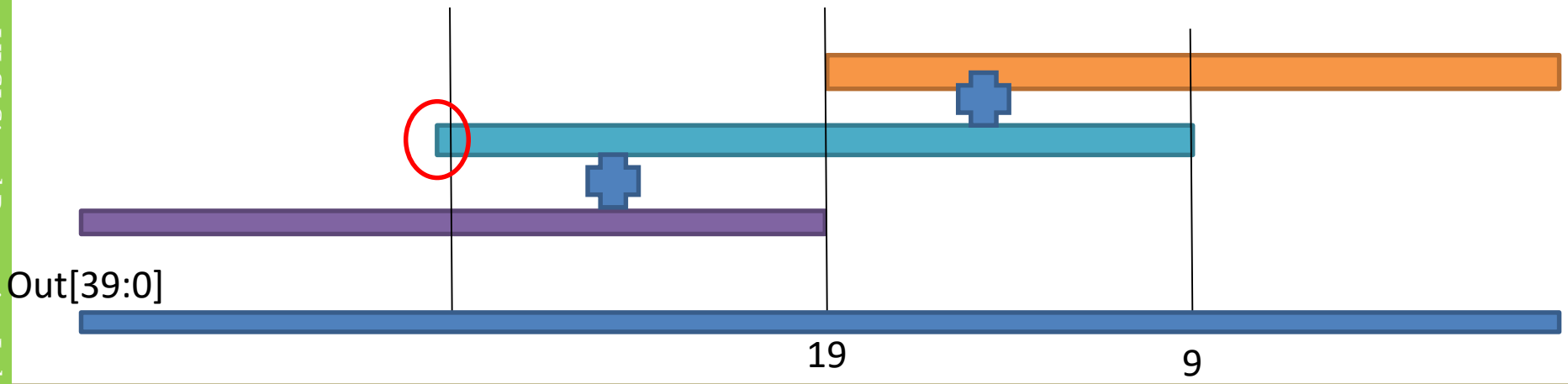
Fast to slow, solution (Reference: Ch 10 p23)

1. Stall
2. Split pipeline
3. Parallel copies
4. FIFO

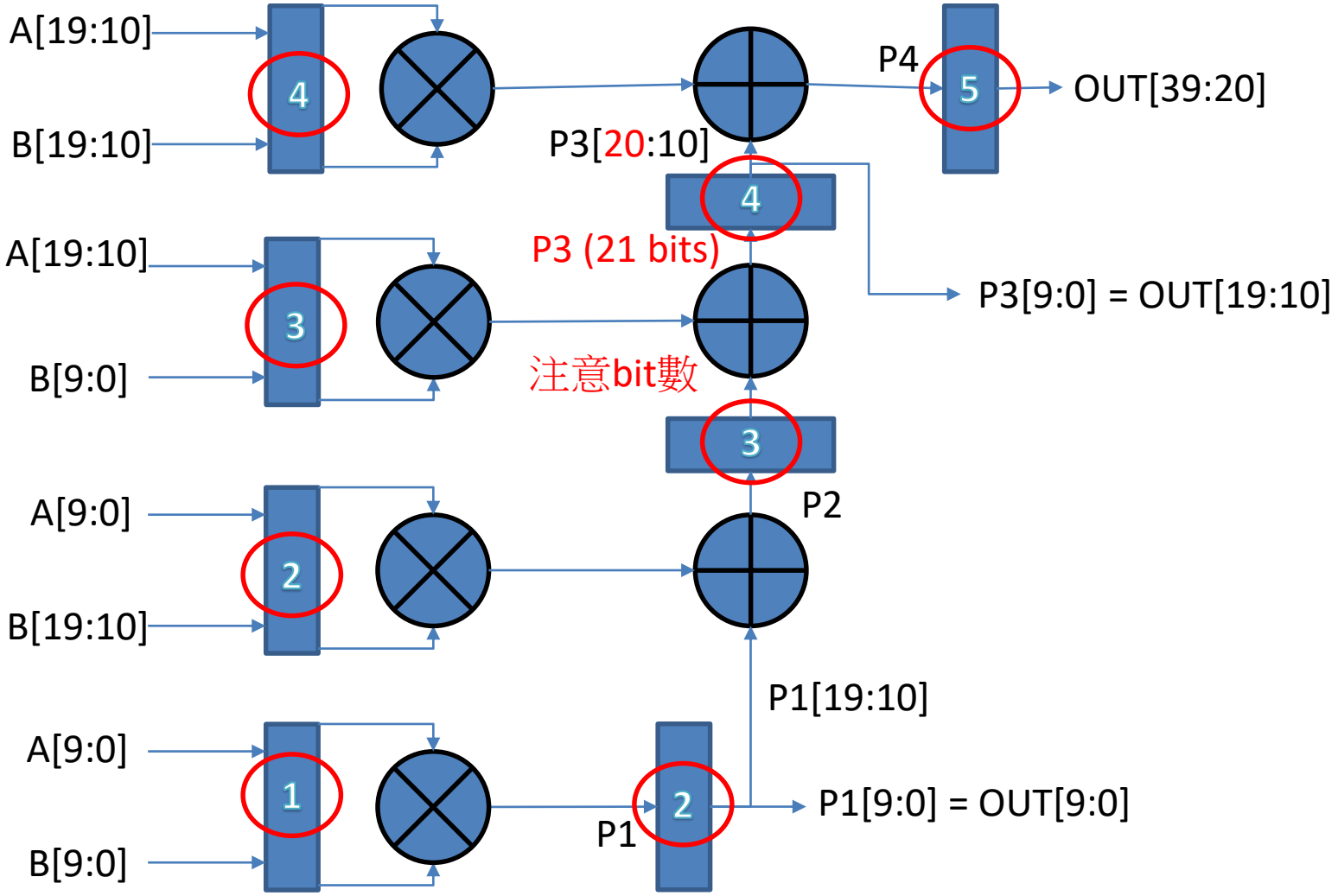
You need to design

- $Out = (in\_1 + in\_2) \times (in\_3 + in\_4)$
  - In_1, in_2, in_3, in_4: 19 bits
  - Out: 40 bits
- Pipeline Multiplier
  - A[19:0] x B[19:0]
    = (A[19:10] x 2^10 +A[9:0]) x (B[19:10] x 2^10 +B[9:0])
    = A[19:10] x B[19:10] x2^20 +(A[19:10] x B[9:0] + A[9:0] x B[19:10])x2^10 + A[9:0] x B[9:0]

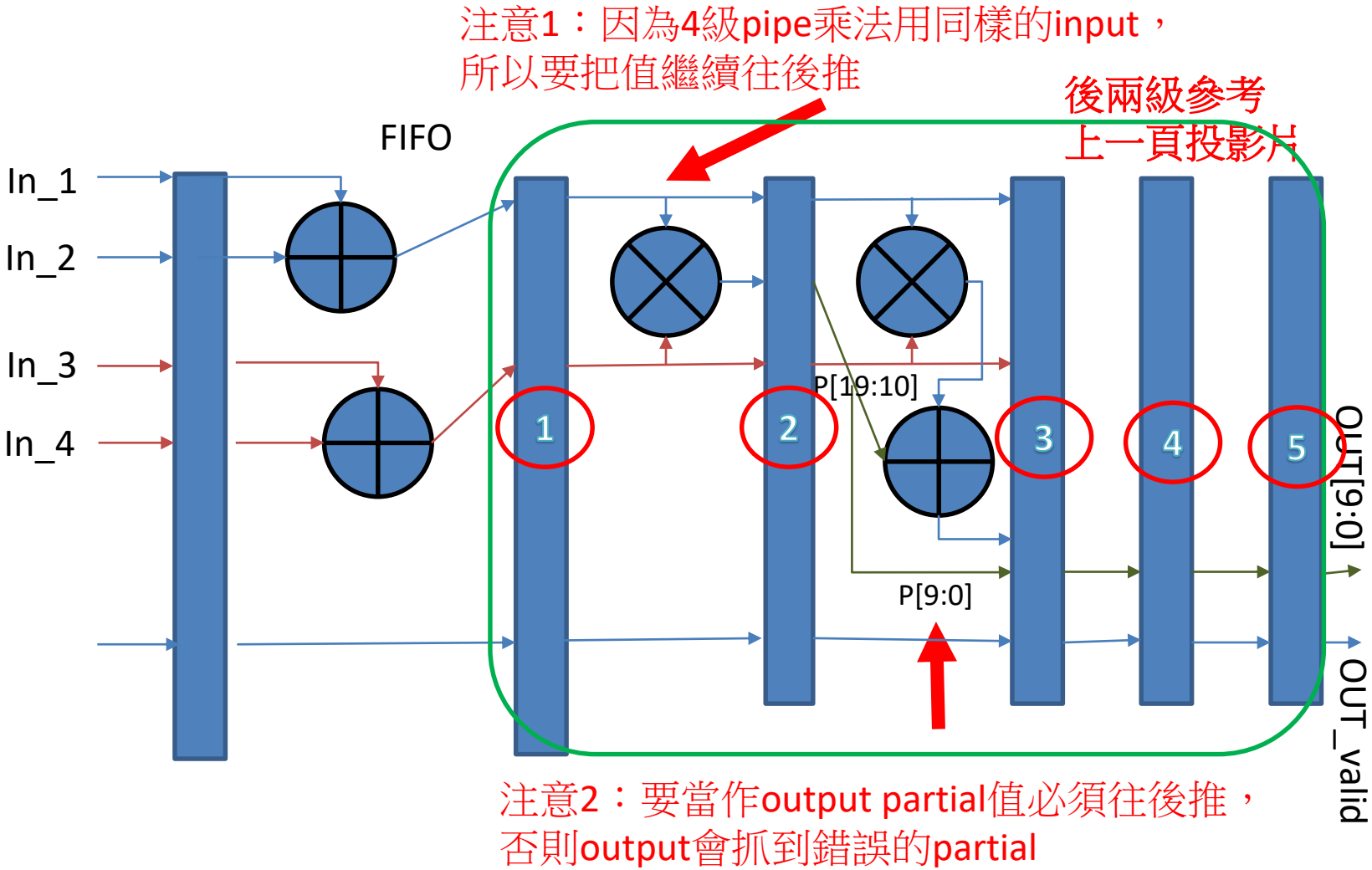
注意bit數



Pipeline Multiplier



建議架構


注意1：因為4級pipe乘法用同樣的input，
所以要把值繼續往後推
後兩級參考
上一頁投影片
FIFO
In_1
In_2
In_3
In_4
1
2
3
4
5
P[19:10]
P[9:0]
OUT[9:0]
OUT_valid
注意2：要當作output partial值必須往後推，
否則output會抓到錯誤的partial

adv_pipeline.sv

Input Signal	Bit Width	Definition
clk	1	Clock
rst_n	1	Asynchronous active-low reset
In_1	9	為連續資料，in_valid = 1時，同時給予四筆data
In_2	9	
In_3	9	
In_4	9	
in_valid	1	當此訊號拉起時給in資料。

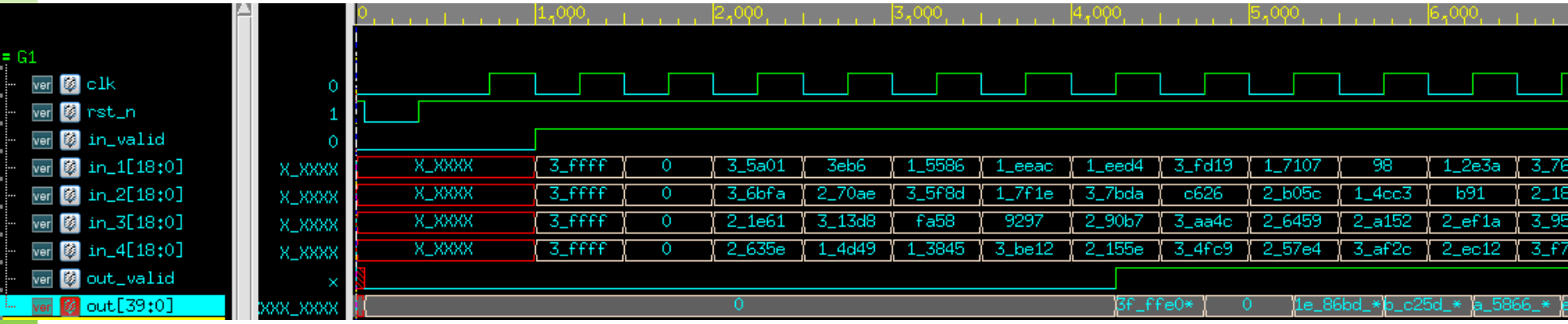
Output Signal	Bit Width	Definition
out_valid	1	Out_valid可為不連續資料，當此訊號拉起時，testbench依照input data順序檢查。
Out	40	Out_valid=1時，輸出一筆40bits資料

Spec

- 可以使用各種方式balance pipeline，不需照建議架構寫design。
- output檢查順序不得更改。
- 所有output必須非同步負準位reset。
- 01_RTL 需要PASS。
- 02_SYN不能有error跟latches。
- 02_SYN，clock period = 3.7ns，timing slack必須為MET。
- 注意1：使用建議架構較為輕鬆，請注意設計中的bit數。
- 注意2：乘法器critical path非常長，如不使用pipeline timing可能不會met。
- 注意3：數字非常大，不容易靠肉眼debug，請想清楚撰寫。

Output & Waveform

- Waveform



Command

- tar -xvf ~dcsta01/Lab09.tar
- Upload
  - cd 09_upload
  - ./01_upload
  - ./02_download demoX