



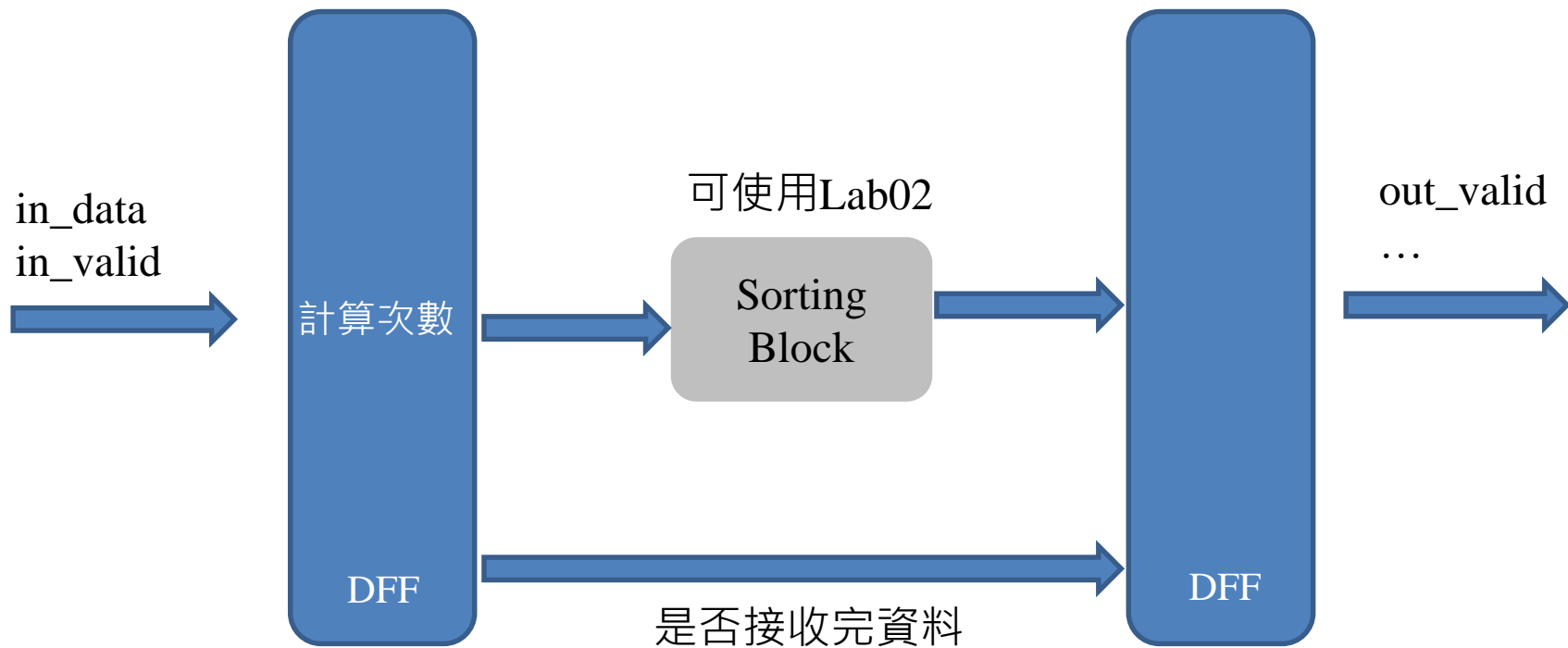
DCS Lab04

隋建德 郭書宏 許仲緯

Histogram

- 連續輸入100個數字，範圍0~3
- 計算100個數字內有幾個0,1,2,3
- 將四個計算的結果做排序(可用Lab02)，由小至大
- Ex: 輸入數字: 0,1,3,1,2,.....
 - 有10個0,11個1,8個2,7個3
 - 輸出 7,8,10,11

參考架構 (Histogram)



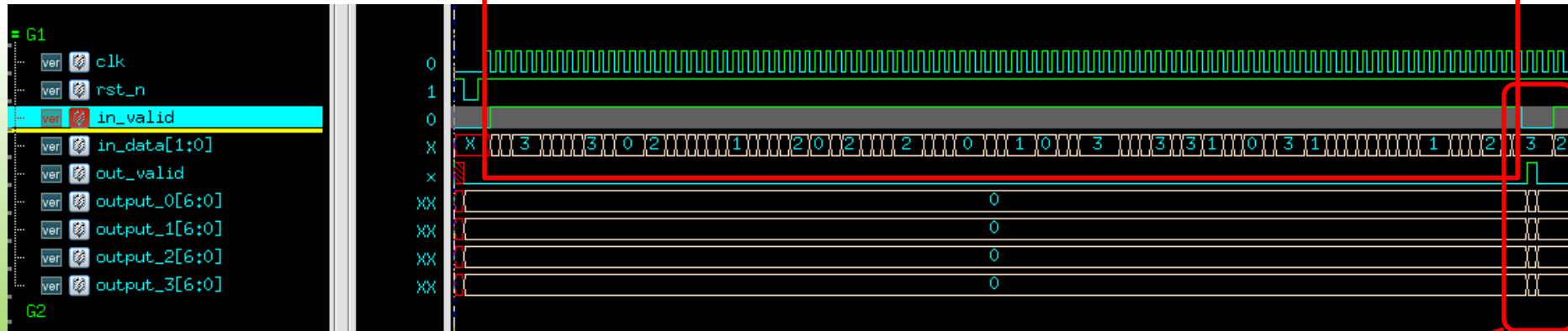
Histogram

Input Signal	Bit Width	Definition
clk	1	Clock
rst_n	1	Asynchronous active-low reset
in_data	2	隨機的數字
in_valid	1	當此訊號拉起時，代表in_data有意義

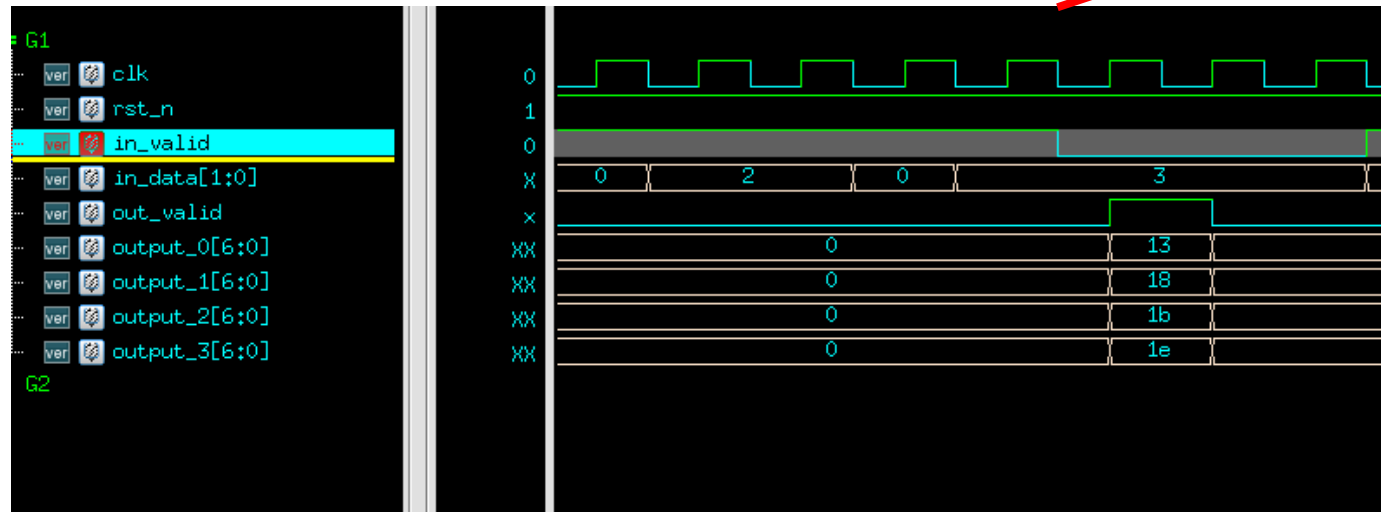
Output Signal	Bit Width	Definition
out_valid	1	當此訊號拉起時，testbench開始檢查。 Out_valid必須在in_valid降下之後的 10cycle之前拉起。並且只能high1cycle
output_0	7	排序後最小值
output_1	7	排序後第二小值
output_2	7	排序後第二大值
output_3	7	排序後最大值

波形

接收100筆資料



需在10cycle內輸出結果



Command

- `tar -xvf ~dcsta01/Lab04.tar`
- `cd Lab04/01_RTL/`
- `cd ../02_SYN/`
 - 檢查latch error MET

Upload

- `cd ../09_UPLOAD/`
- `./01_upload` (上傳code)
- `./02_download [argument]` (下載上傳結果)
 - `[argument] = demo1 or demo2`
 - 檢查是否上傳成功&正確

```
linux01 [Lab02/09_UPLOAD]% ./01_upload
```

```
module Sort(  
    // Input signals
```

```
endmodule
```

```
-----  
The 1st demo deadline is Thu Mar 18 16:25:00 CST 2021 ,  
It is Fri Mar 12 18:15:48 CST 2021 now!  
It will upload to demo1.  
It will overwrite your file if you have uploaded before.
```

```
Is this the file you want to upload?(y/n):y  
Upload done!
```

```
linux01 [Lab02/09_UPLOAD]%
```

```
linux01 [Lab02/09_UPLOAD]% ./02_download demo1  
Download done!
```