Topic A2

Pipelined Architectures

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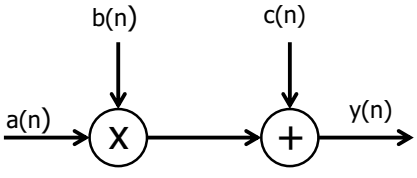
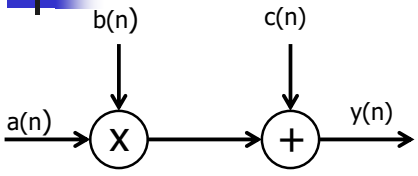
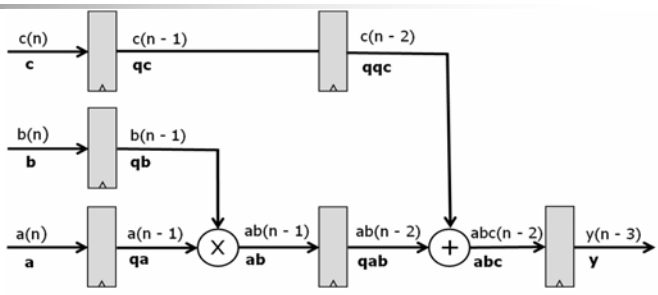
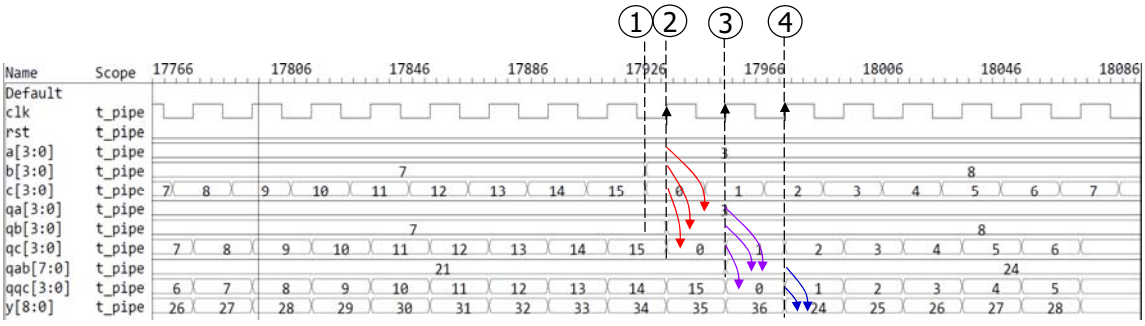
Data Path



Pipelined Architectures







Pipelined Arch.

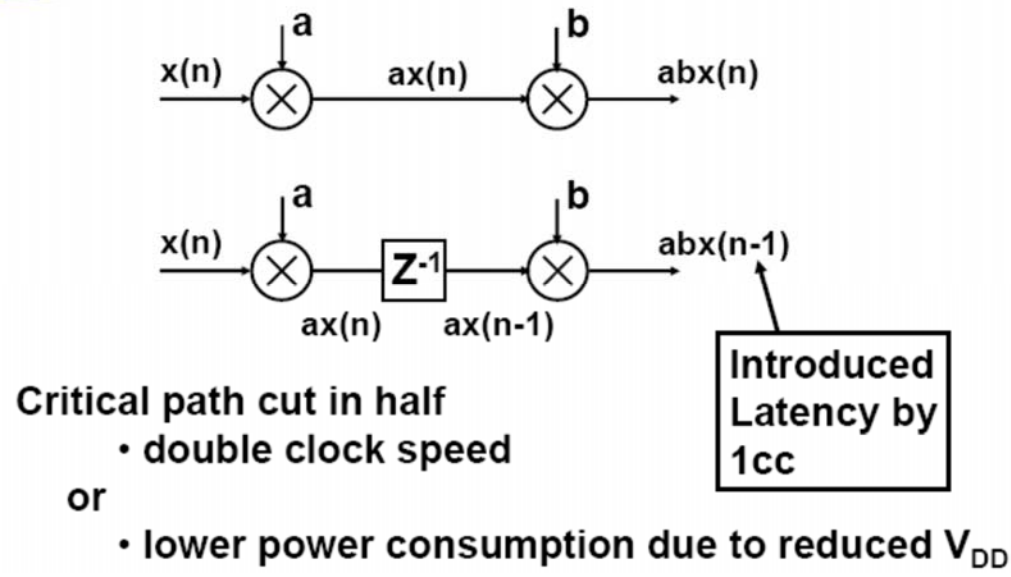
```
module pipe_v3 (clk, rst, y, a, b, c);
input clk, rst, a, b, c;
output y;
reg [8:0] abc, y;
reg [7:0] qab, ab;
reg [3:0] qa, qb, qc, qqc;
wire [3:0] a, b, c;

// assign #18 ab = a * b;
// assign #12 abc = u + v;

always @ (qa or qb or qab or qqc)
begin
   ab =  qa * qb;
   abc = qab + qqc;
end

always @ (posedge clk or posedge rst)
if (rst)
   begin
      qa = 0;
      qb = 0;
      qc = 0;
      qqc = 0;
      qab = 0;
      y = 0;
   end
else
   begin
      qa <= a;
      qb <= b;
      qc <= c;
      qab <= ab;
      qqc <= qc;
      y <= abc;
   end
endmodule
```

1

```
`include "pipe_v3.v";
module t_pipe_v3;

reg  clk, rst;
wire [8:0] y;
reg [3:0] a, b, c;
integer k;

pipe_v3 uut (clk, rst, y, a, b, c);

initial
begin
   rst <= 0;          // rst <= 0;        <------- time = 0
   #5 rst = 1;        // rst <= #5   1;   <------- time = 5
   #26;               // rst <= #31  0;   <------- time = 31
   rst = 0;           // clk <= 0;        <------- time = 0
   clk <= 0;
end

always
   #10 clk = ~clk;

initial
begin
   {a, b, c} = 0;
   #13;
   for (k = 0; k < 4096; k = k + 1)
   begin
      {a, b, c} = k;
      #20;
   end
end
initial #40960 $finish;
endmodule
```

2

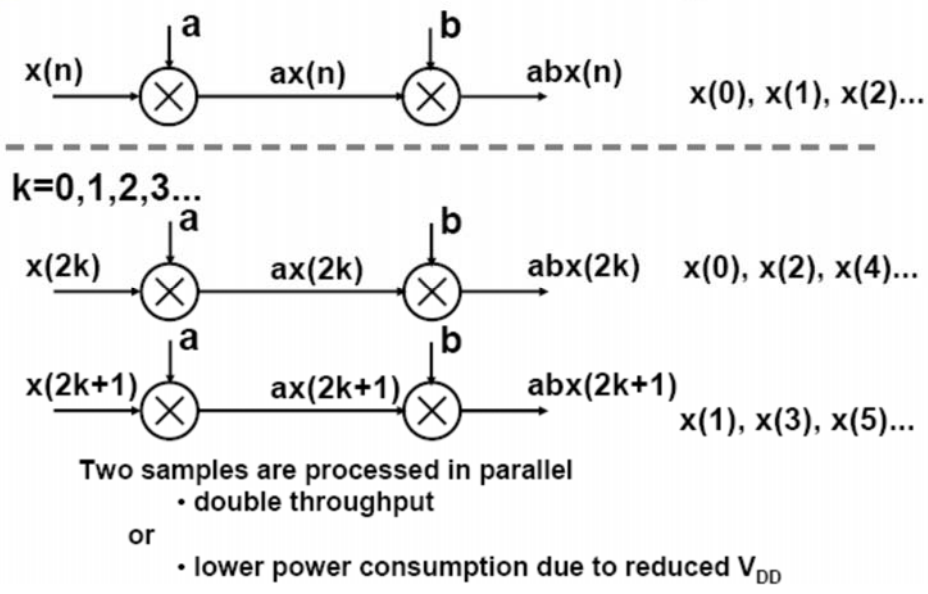
Pipelining



Critical path cut in half
- double clock speed

or
- lower power consumption due to reduced V_{DD}

Parallel Processing



Two samples are processed in parallel
- double throughput

or
- lower power consumption due to reduced V_{DD}