

2021 DCS Lab 07

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Pattern

- 這次Lab寫pattern去測錯誤的design,找到其錯誤
- 這次Lab只需要寫00_TESTBED/pattern.sv
- lab07_1.sv代表第一個spec錯誤的design,依此類推。lab07.sv 是正確的design。
- lab07_x.sv & lab07.sv 都不要動到
- 可以參考之前幾次的pattern和講義

lab06.sv

Input Signal	Bit Width	Definition
clk	1	5 ns Clock for 1 cycle
rst_n	1	Asynchronous reset when reset negedge, all output should be zero
in_number	4	連續給4個數字。方便之後說明,分別用 in_1、in_2、in_3跟in_4代表
mode	2	幾種運算模式,請看下一頁
in_valid	1	in_valid high when giving number

Output Signal	Bit Width	Definition
out_valid	1	High for 1 cycle
out_result	7	High for 1 cycle,計算後的結果,如下頁 所示

mode

需先將input四個數值(in_1~in_4)進行排序由小至大,假設以下經過排序後sort_1最小, sort_4最大

Input signal :mode		
0	out_number = sort_1 + sort_2	
1	out_number sort_2 – sort_1	
2	out_number = sort_4 - sort_3	
3	out_number = sort_1 - sort_4	

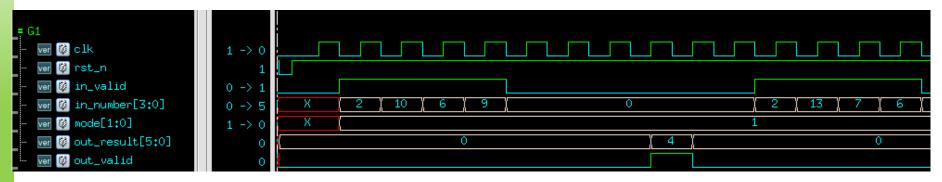
Specifications

- Top module name : lab07 (File name: lab07.sv)
- Spec1: reset後output signal要歸零
- Spec2:計算完吐完值後1cycle, out_valid要歸零 (out_valid只維持1cycle)
- Spec3: 100cycle內要計算完成(out_valid為high)
- Spec4: function要對(前一頁的公式會有錯要檢查出來)

• 註:請用random多跑幾組去檢測(建議100以上)

Output & Waveform

Waveform



Command

- tar -xvf ~dcsta01/Lab07.tar
- ./01_run_spec1 : run for check spec1(should display SPEC1 Fail)
- ./01_run_spec2 : run for check spec2(should display SPEC2 Fail)
- ./01_run_spec3 : run for check spec3(should display SPEC3 Fail)
- ./01_run_spec4 : run for check spec4(should display SPEC4 Fail)
- ./01_run : run for right design(should display Congratulation)
- You should Pass all spec!

Command

• 請參考pattern.sv裡這段,需要各自秀出 SPEC1.2.3.4等資訊,以免助教demo時抓不到

Command

- tar -xvf ~dcsta01/Lab07.tar
- Upload
 - cd 09_upload
 - ./01_upload
 - ./02_download demoX