

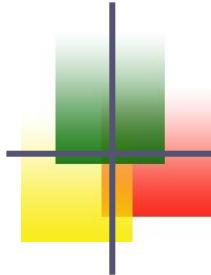


*System On Chip*

教育部商管學程系統晶片應用課程

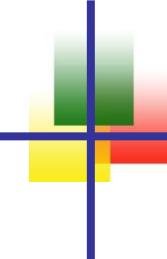
# *Introduction to SoC and Its Applications*

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*Fundamental of SoC and Semiconductor Process*

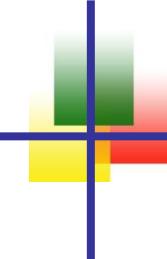




# Outline

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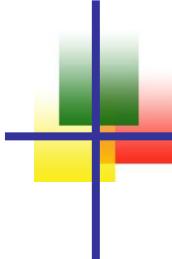
- **Introduction to Integrated Circuits**
- **IC Evolution**
- **Device Fabrication**
- **Conclusion**



# Outline

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- **Introduction to Integrated Circuits**
- **IC Evolution**
- **Device Fabrication**
- **Conclusion**



# Chip Everywhere!

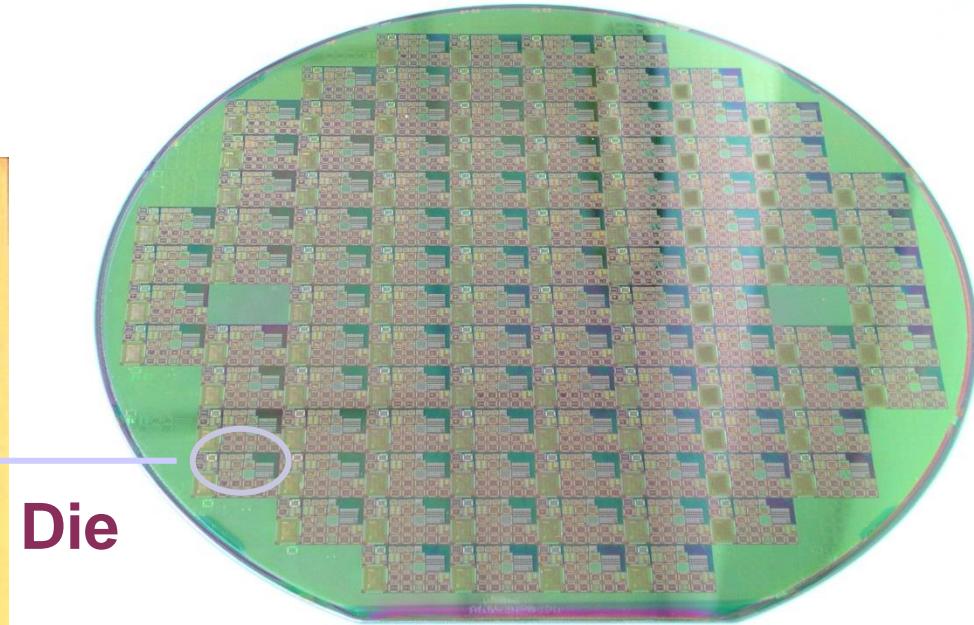
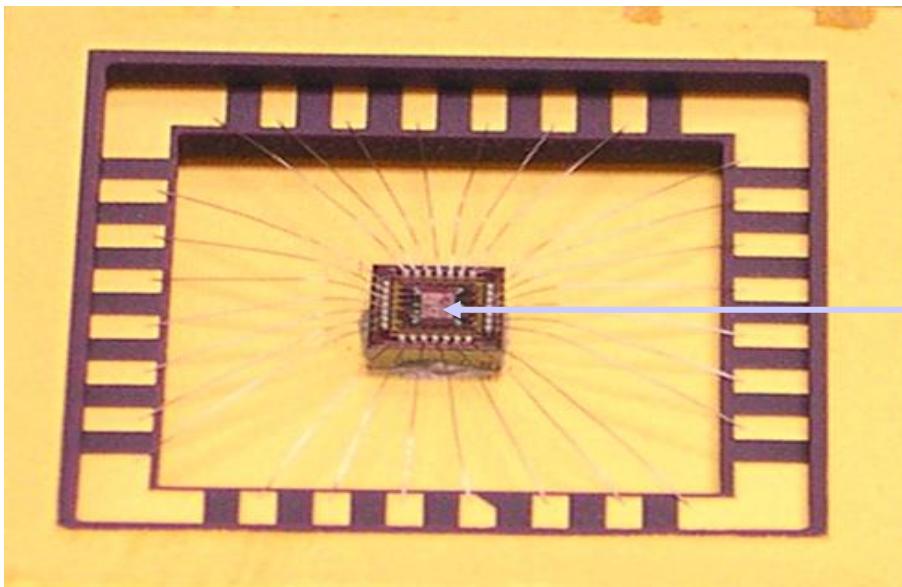
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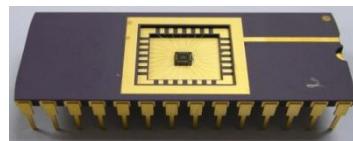
# Wafer & Die & Packaging

Wafer

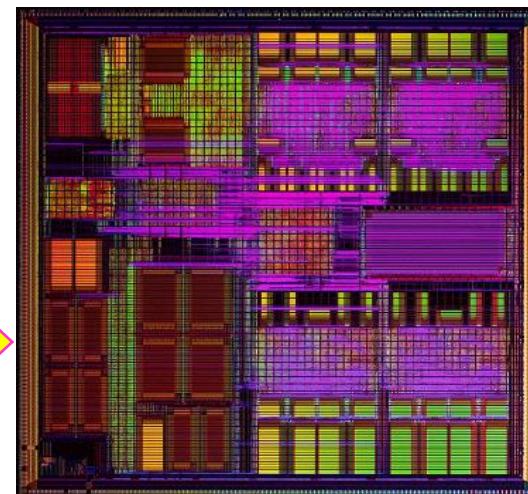
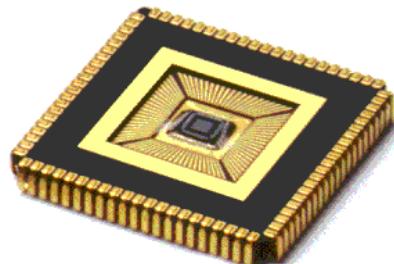
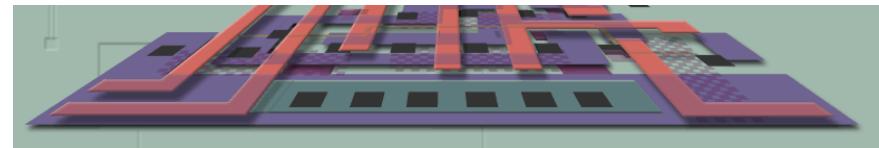
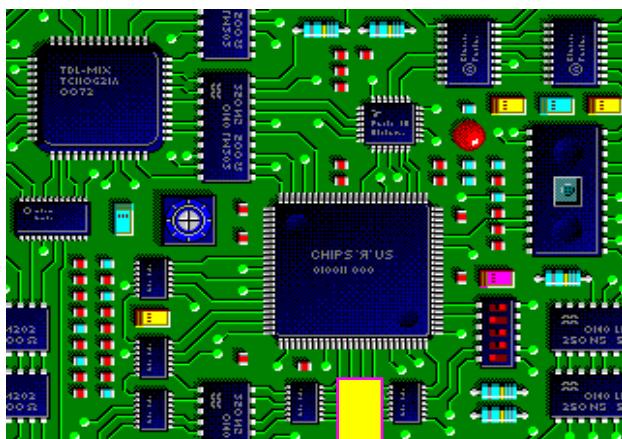
Assembly/Packaging



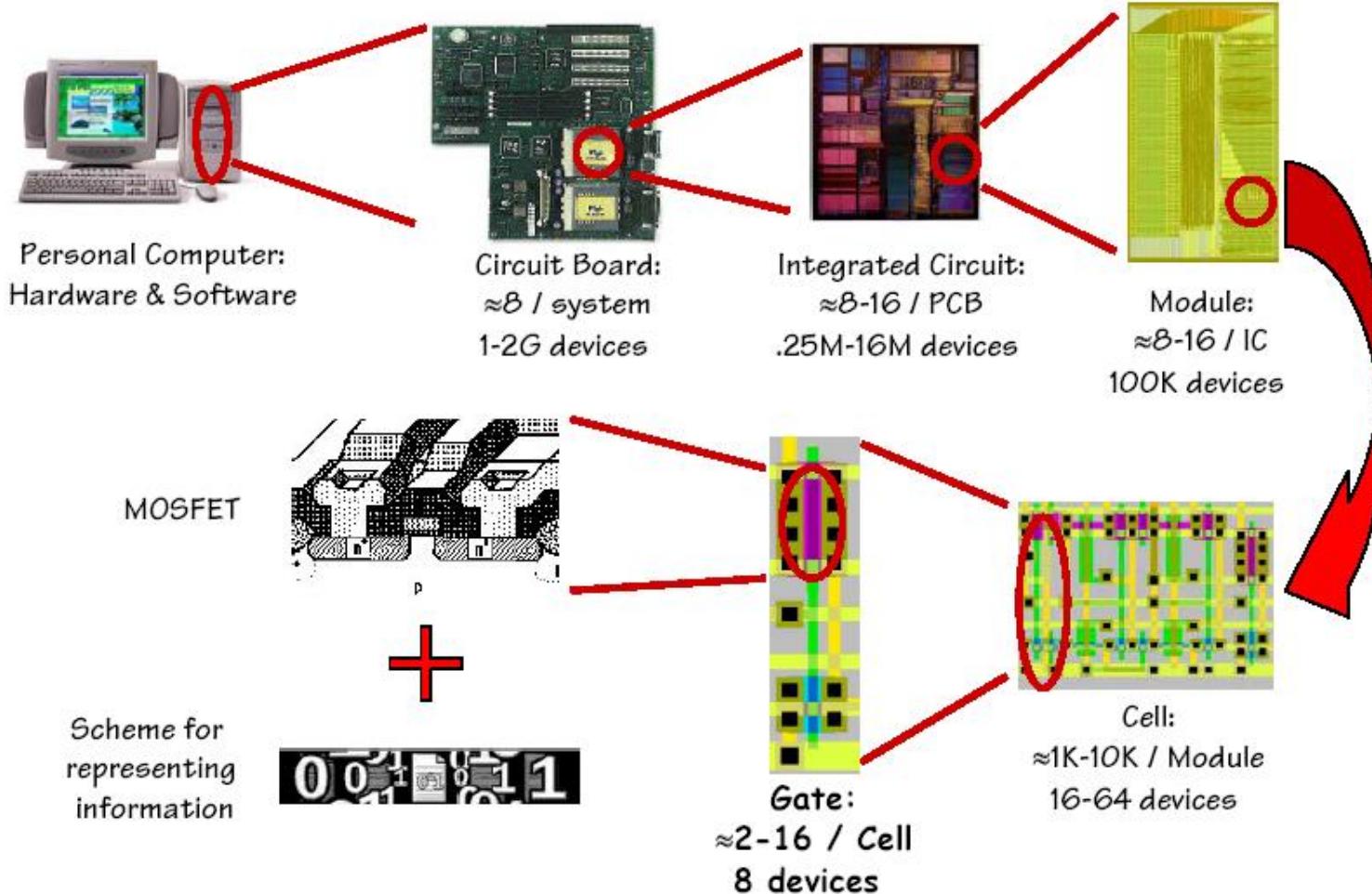
Die

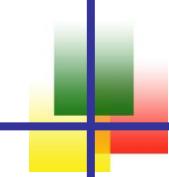


# Integrated Circuits (ICs)



# Modern System Engineering





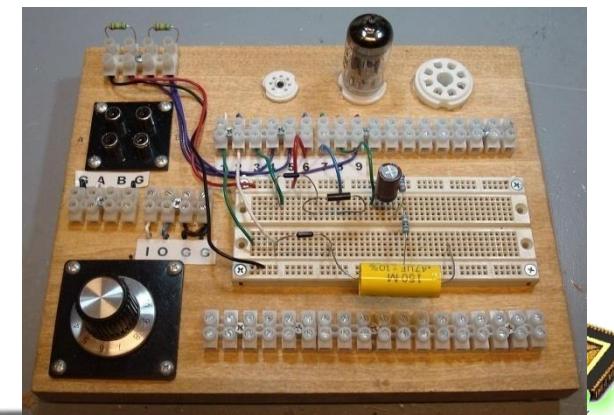
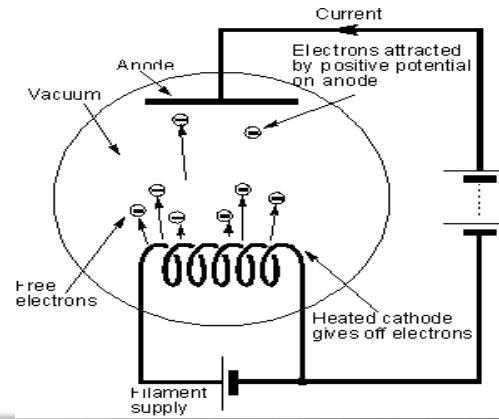
# Transistor Evolution

## ■ 1<sup>st</sup> Generation: Vacuum Tube, 1946~1954

- In 1946, University of Pennsylvania, USA, manufactured the first computer (ENIAC) with vacuum tubes. It shares 18,000 vacuum tubes, weighs about 30 tons, is 15.24 meters long, 9 meters wide, and 2 meters high. It takes about two classrooms to fit.

## ■ 2<sup>nd</sup> Generation: Transistor, 1954

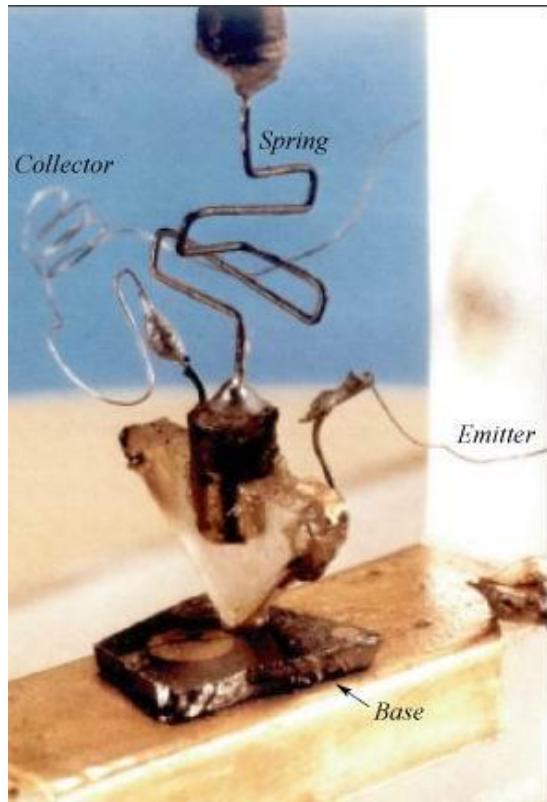
- The transistor was invented in 1948, and in 1954. Bell Labs in the United States completed a computer based on transistors. This kind of computer is only one twentieth the size of a vacuum tube



# The First Transistor

## ■ The First transistor , AT&T Bell Labs, 1947

- Point connect transistor
- Semiconductor- Ge

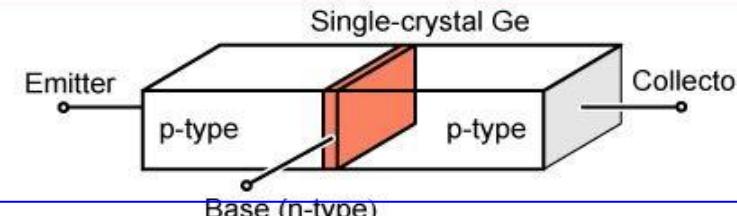
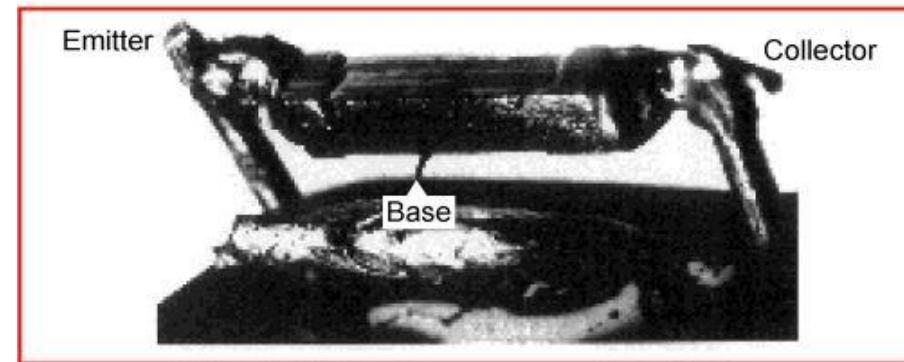
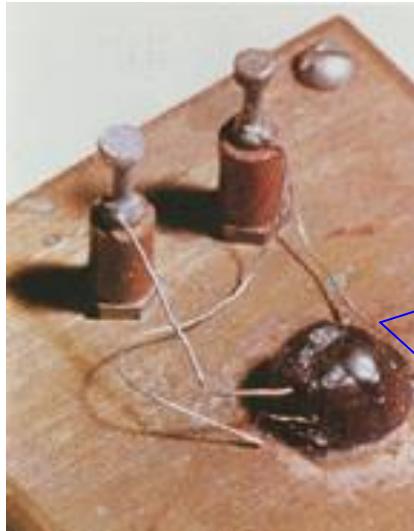


# The First Junction Transistor



## The first transistor with diffused pn junction(junction transistor)

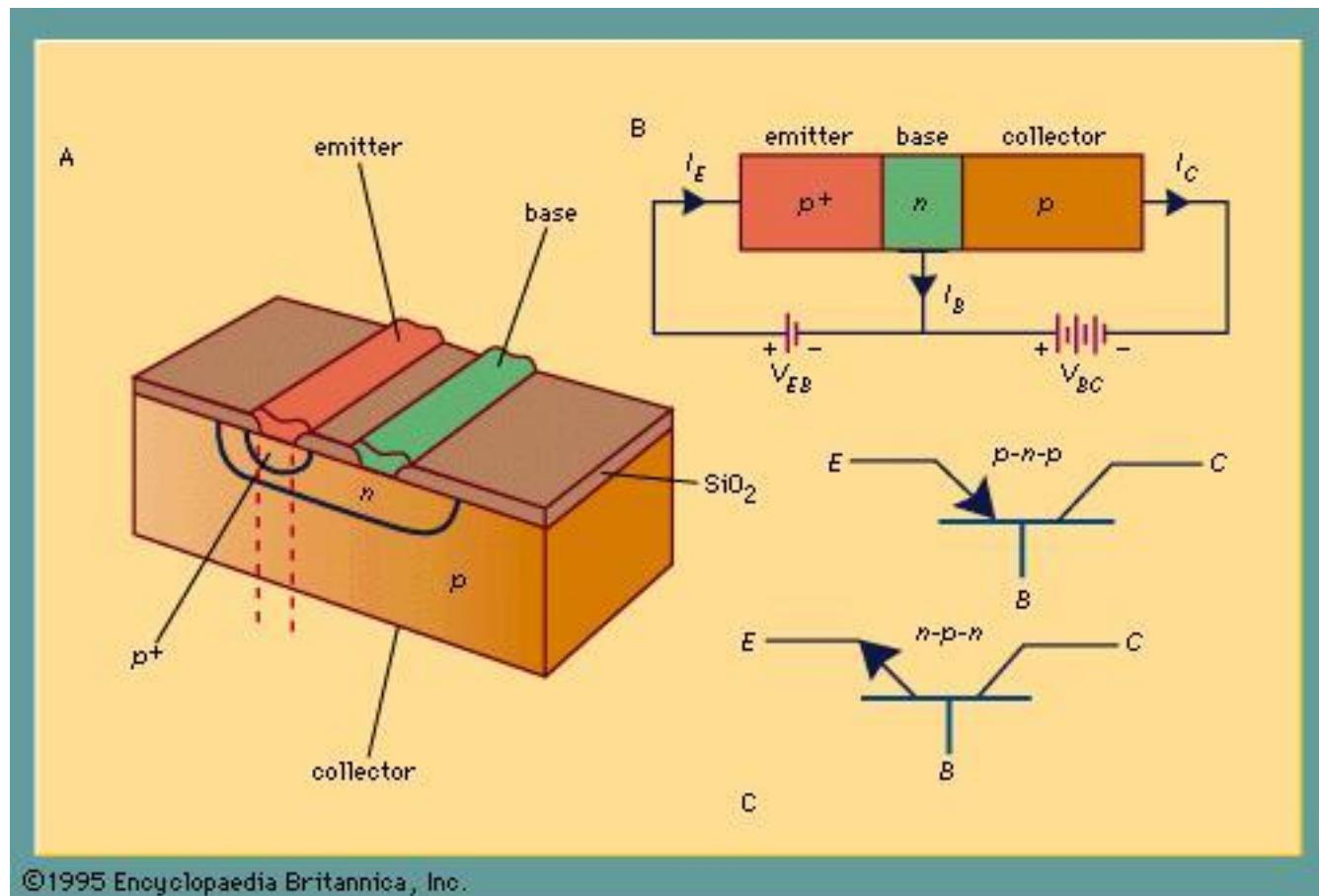
- William Shockley, Bell Lab, 1949
- Semiconductor substrate silicon
- N-type (silicon diffused with pentavalent atoms)
- P-type (silicon diffused with trivalent atoms)
- NPN or PNP with emitter/base/collector





# Bipolar Transistor

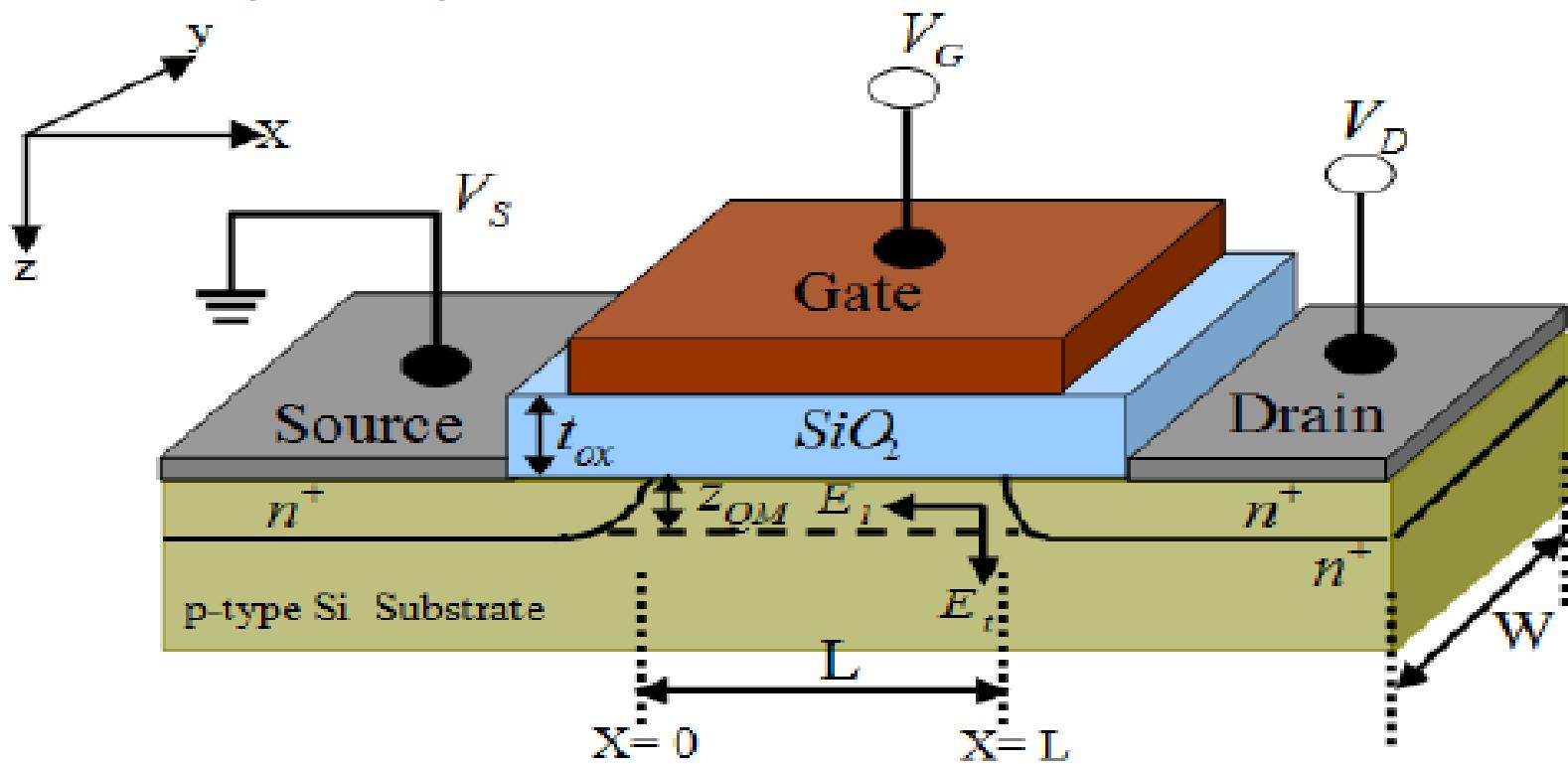
- Type of transistor that relies on the contact of two types of semiconductor for its operation



# MOS(Metal-Oxide-Semiconductor)FET(Field-Effect-Transistor)

## MOSFET Transistor structure

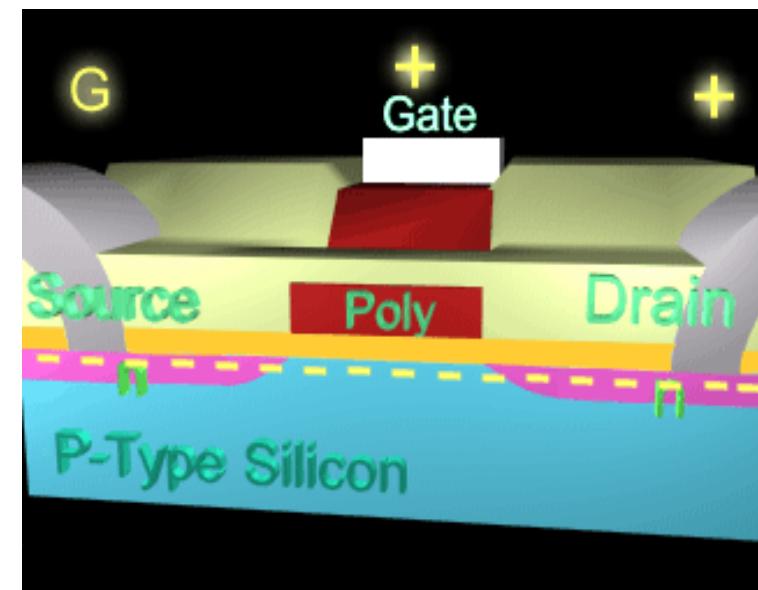
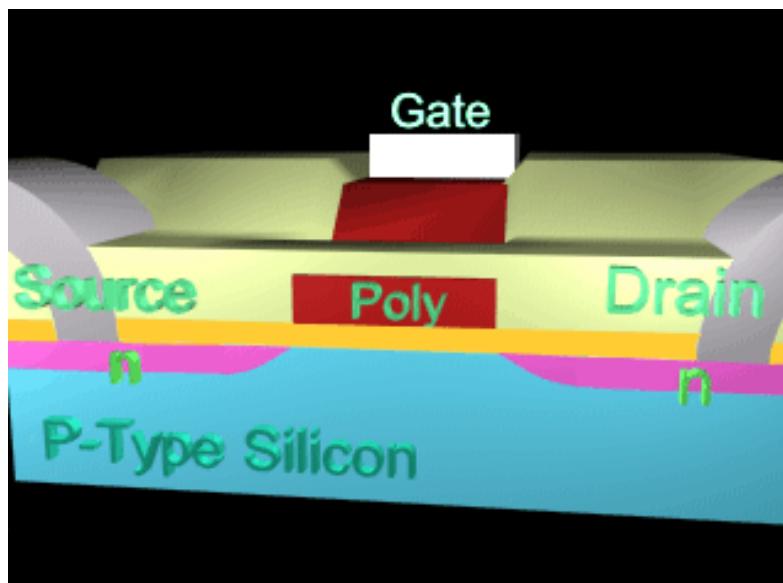
- Drain/Gate/Source
- NMOS (Drain/Source are n-type/substrate are p-type)
- PMOS (Drain/Source are p-type/substrate are n-type)
- L: gate length

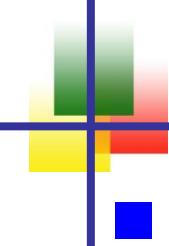


# N-channel Metal-Oxide-Semiconductor

## NMOS/PMOS (CMOS-complementary contains NMOS/PMOS)

- Gate – polysilicon
- Source, Drain – n-type
- Substrate – p-type
- Carrier – electrons

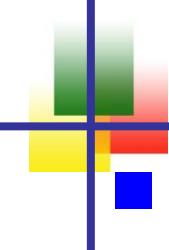




# Transistor Evolution(cont.)

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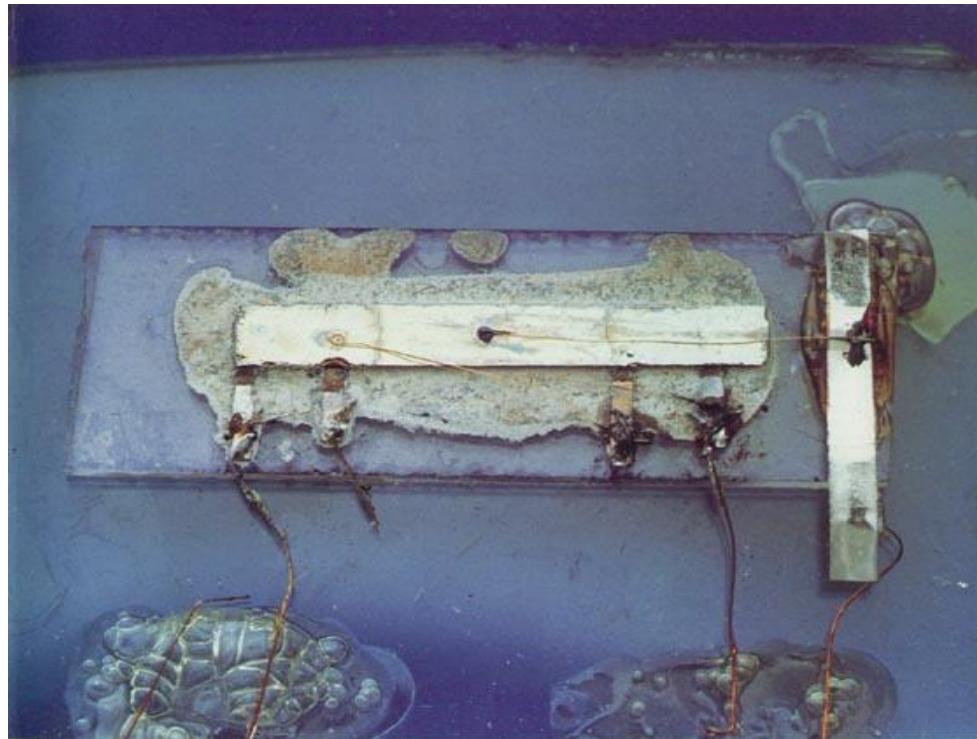
- **3<sup>rd</sup> Generation : Integrated Circuits, or IC, 1964**
  - Put several transistors on top of the same substrate (die)
  - Texas Instrument
- **4<sup>th</sup> Generation : Very Large Scale Integrated Circuits (VLSI)**
  - With more than ten thousand transistors on one die is called VLSI
- **5<sup>th</sup> Generation: System on a Chip, SoC**
  - Nanometer transistors with Hardware/Software integration



# The First Integrated Circuit (IC)

## ■ First IC

- Made by Jack Kilby of Texas Instrument in 1958
- 5 integrated components



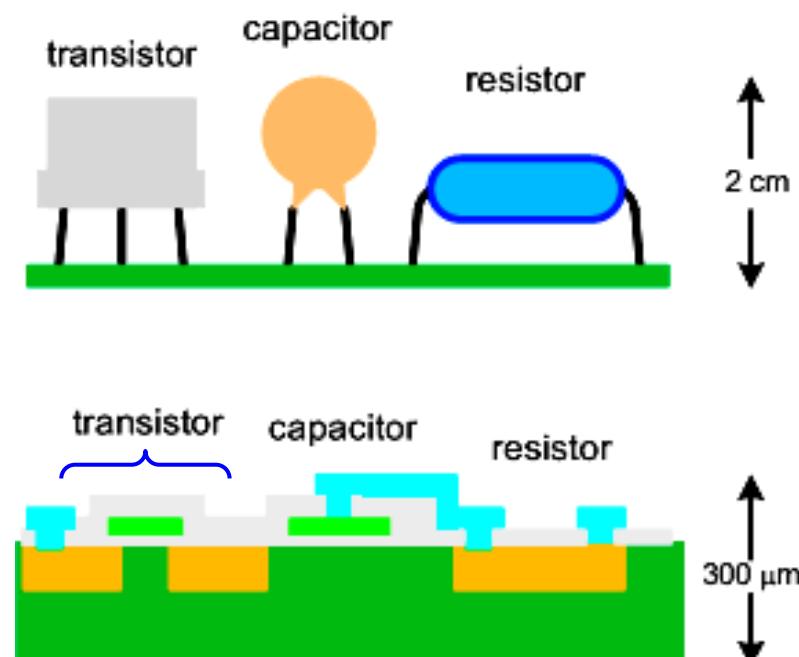
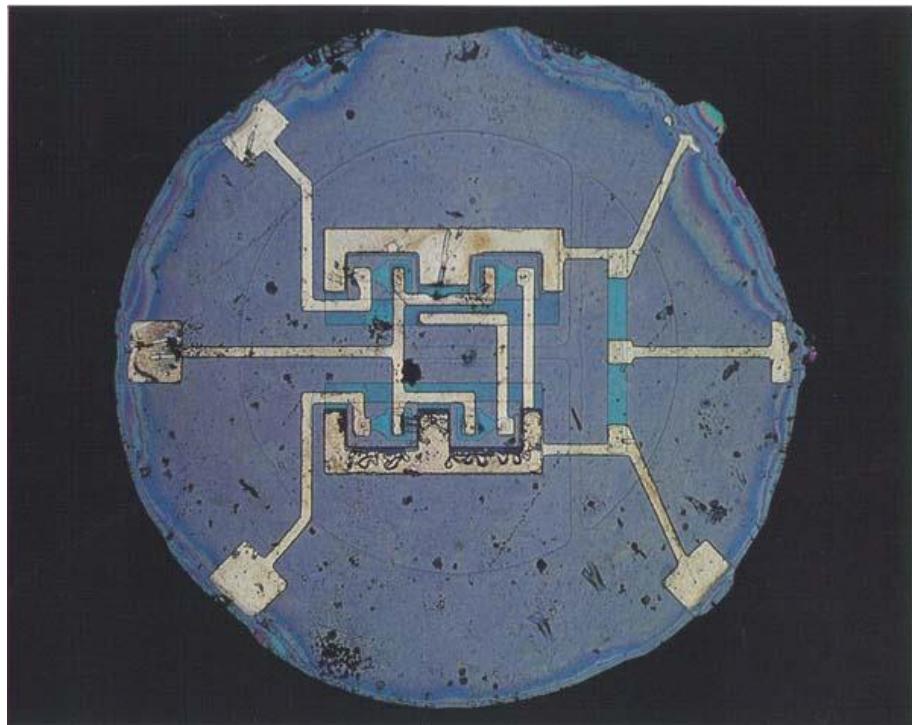
Source:<http://smithsonianchips.si.edu/augarten/i6.htm>



# The First Planar IC

## ■ Planar Technology Invented

- Made by Robert Noyce of Fairchild Camera in 1961



Source:<http://smithsonianchips.si.edu/augarten/i10.htm>



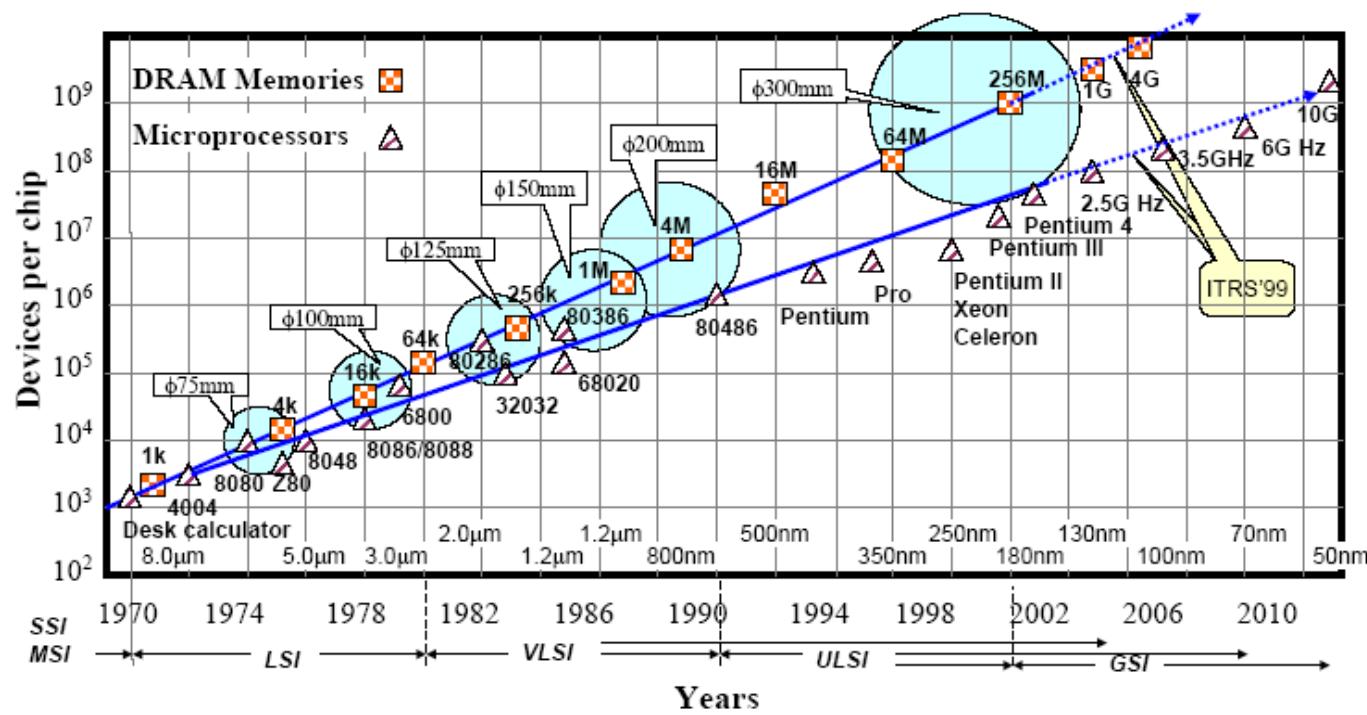
# Outline

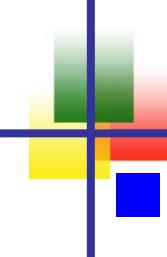
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- **Introduction to Integrated Circuits**
- **IC Evolution**
- **Device Fabrication**
- **Conclusion**

# Moore's Law and Technology Scaling

■ “...the performance of an IC, including the number components on it, doubles every 18-24 month with the chip price...” —Gordon Moore 1960





# Types of IC

---

## ■ **SSI (Small-Scaled Integrated Circuits)**

- Tens of components (1970s)

## ■ **MSI (Medium-Scaled IC)**

- Hundreds of components

## ■ **LSI (Large-Scaled IC)**

- Thousands of components (1980s)

## ■ **VLSI (Very Large Scaled IC)**

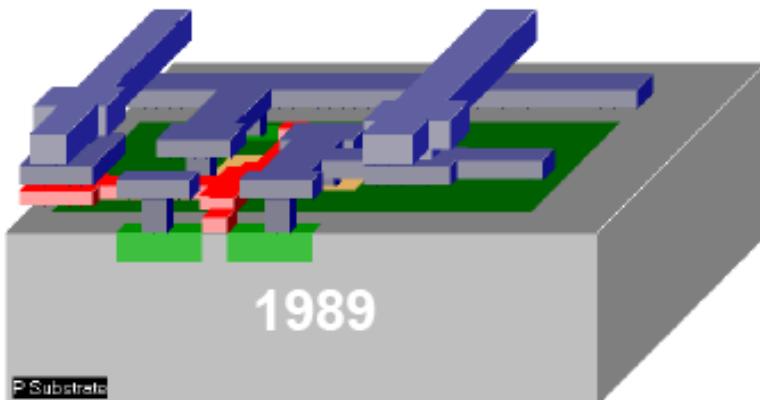
- Tens thousands of components (1990s)

## ■ **SoC (System on a Chip)**

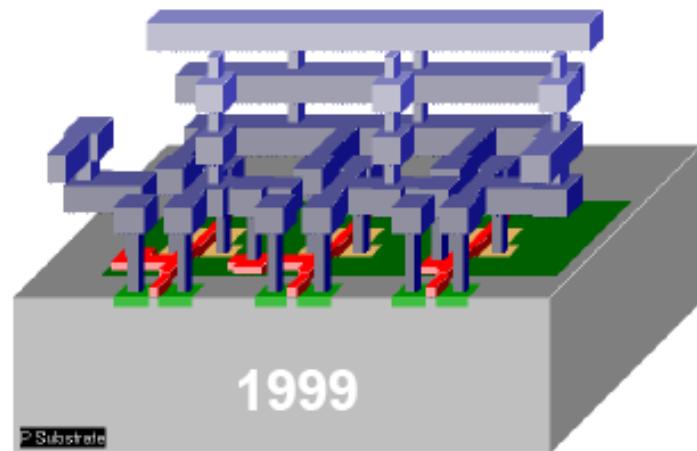
- Millions of components (2000s)

- 1 components =10 gates

# Changes in Real ICs



0.8 $\mu$ m CMOS



0.18 $\mu$ m CMOS

Technology:	0.8 $\mu$ m	0.18 $\mu$ m	0.07 $\mu$ m
# of Metal layers:	2~3	6	8-9
G.W. Aspect ratio (t/w):	~0.8	~1.8	~2.7
Wire length(m/chip):	~130	~1,480	~10,000

**Interconnects Start to Dominates Cost and Performance**  
**Interconnect starts to be main design constraints**

Source: L.-R. Zheng, KTH

# More Moore (Technology scaling)

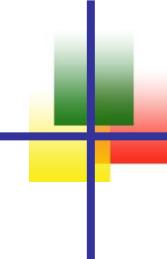
- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1994
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2019 (TSMC commercial 5nm technology)
- 3 nm – ~2022

When will it end?

Transistor size shrink by half every 18 month

Technology naming by the gate length of the transistor

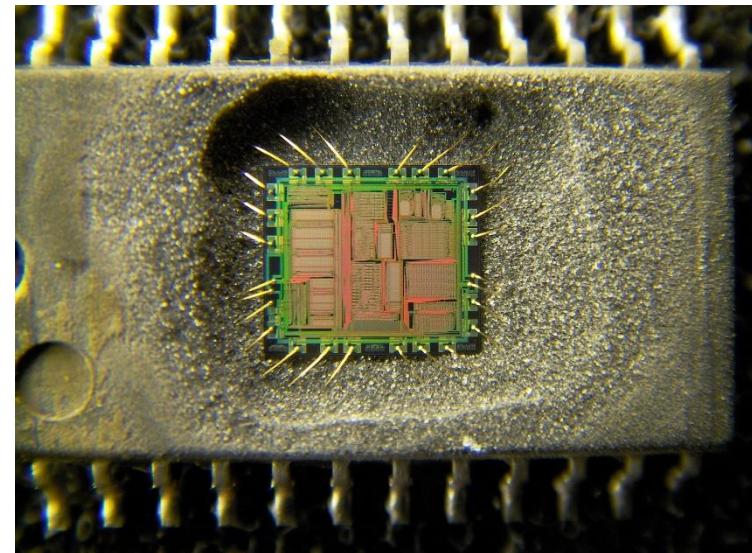
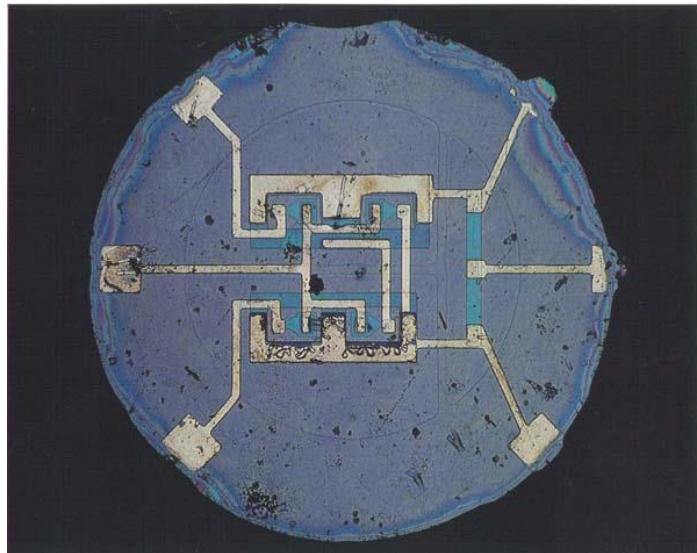
The diameter of an **atom** ranges from about 0.1 to 0.5 nanometers

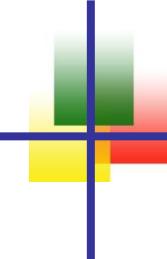


# Moore's Law and Technology Scaling

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- *Shrink transistor size*
- *Gate length from 2um to 5nm/3nm/2nm)*





# Outline

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- **Introduction to Integrated Circuits**
- **IC Evolution**
- **Device Fabrication**
  - Oxidation
  - Lithography
  - Ion Implantation
  - Diffusion
- **Conclusion**



# **Device Fabrication Technology**

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About  $10^{20}$  transistors (or 10 billion for every person in the world) are manufactured every year.

VLSI (Very Large Scale Integration)

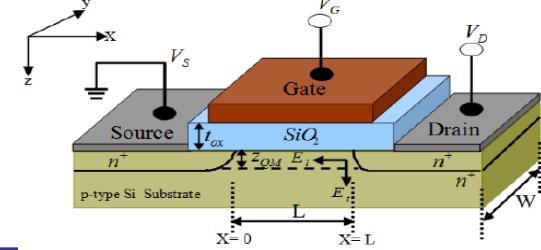
ULSI (Ultra Large Scale Integration)

GSI (Giga-Scale Integration)

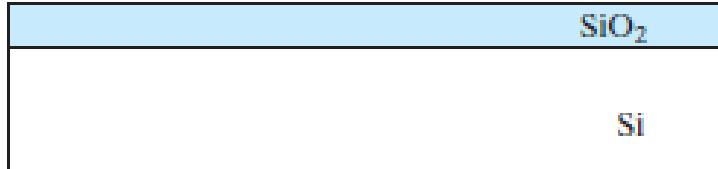
Variations of this versatile technology are used for

- ✓ flat-panel displays,
- ✓ micro-electro-mechanical systems (*MEMS*), and
- ✓ chips for DNA screening...

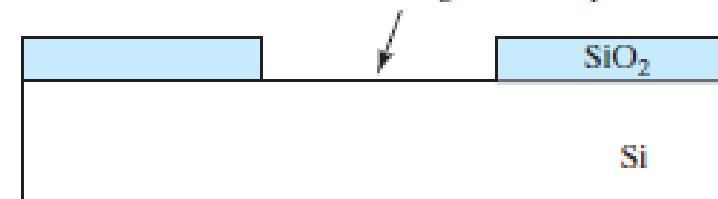
# Semiconductor Process



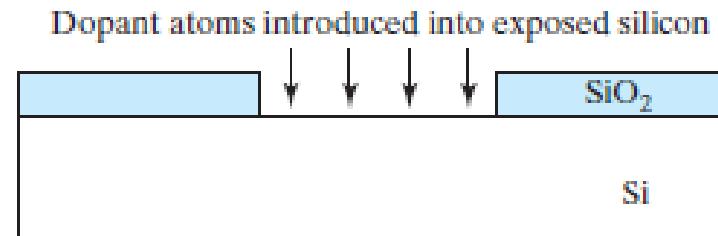
Oxidation



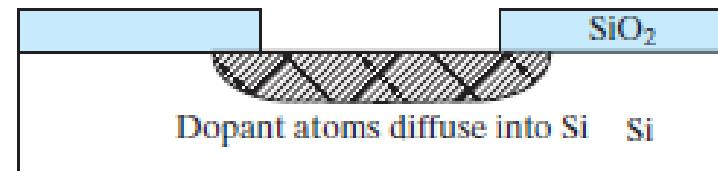
Lithography &  
Etching



Ion Implantation



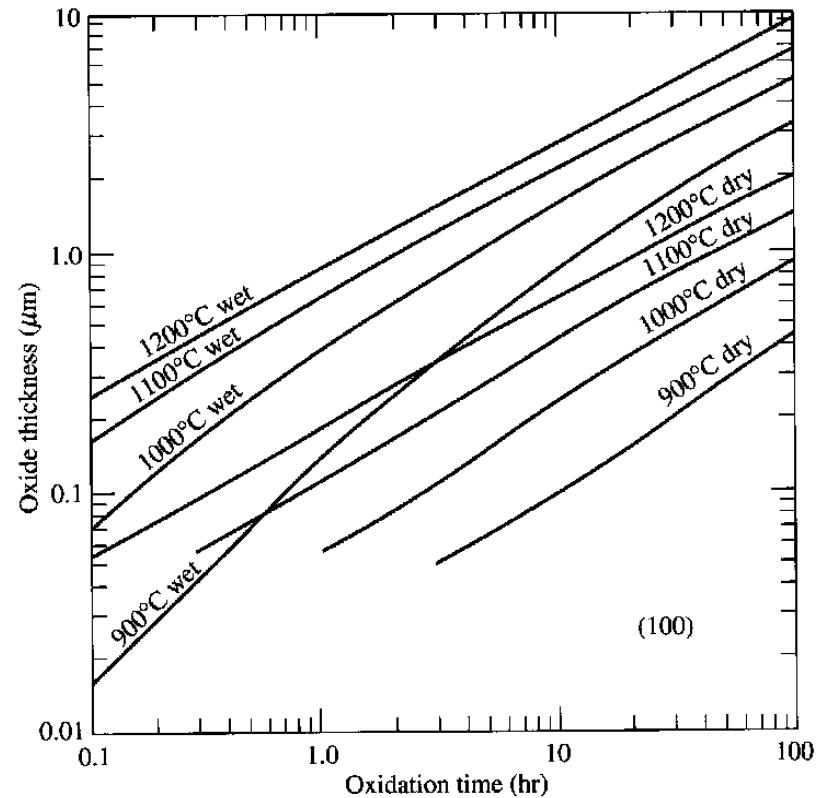
Annealing &  
Diffusion



# Oxidation of Silicon

Dry Oxidation :  $\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2$

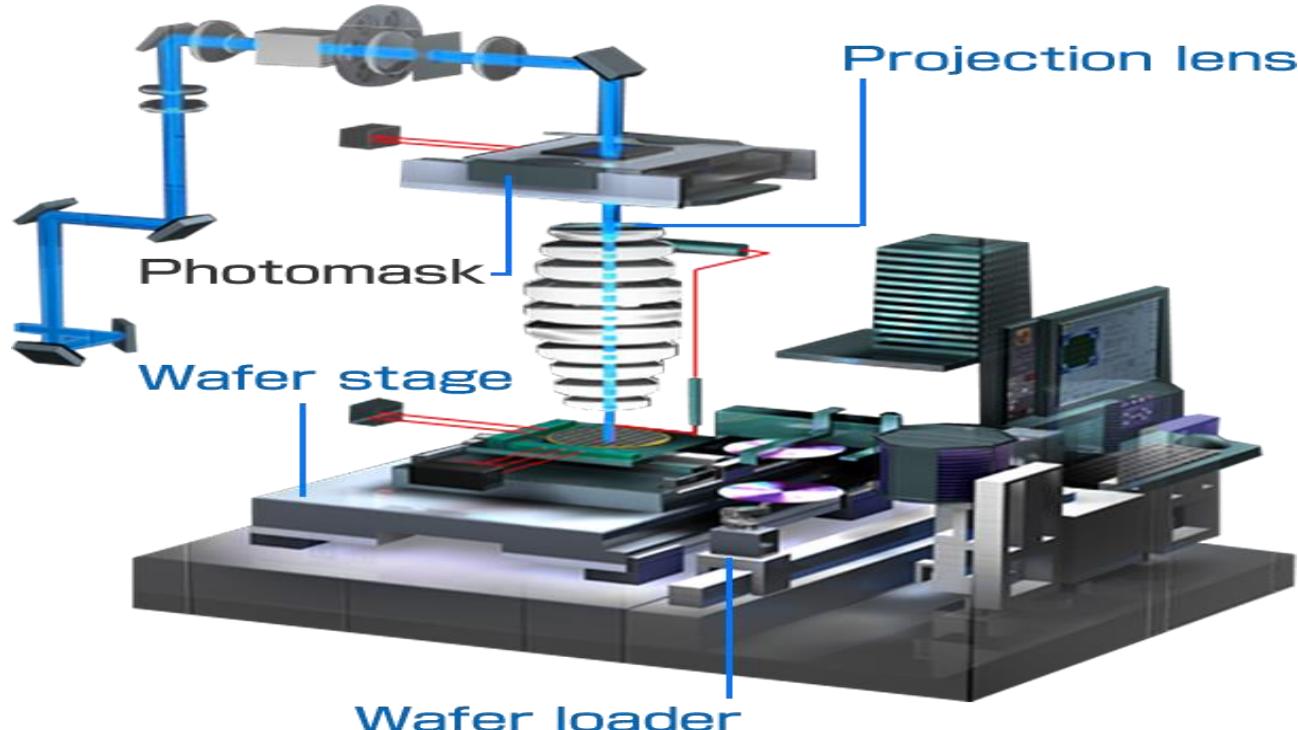
Wet Oxidation :  $\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2$



# Lithography

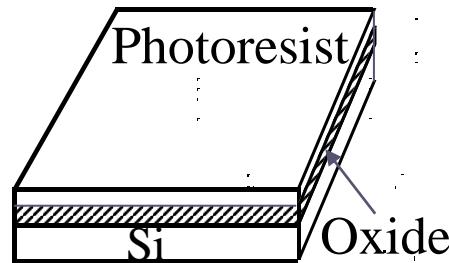
## A semiconductor lithography system

- a process to reduce highly complex circuit patterns
- drawn on a photomask of a large glass plate
- Using ultra-high-performance lenses
- exposed onto a silicon substrate known as a wafer.

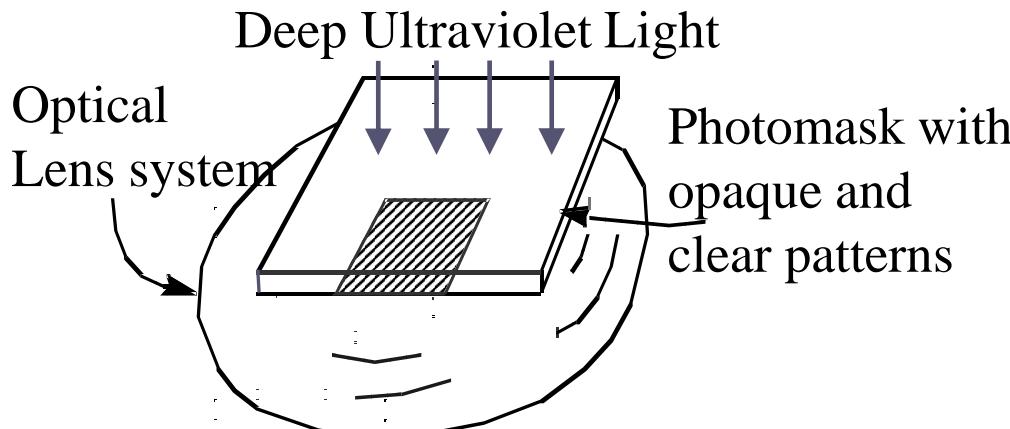


# Lithography Process

(a) Resist Coating



(b) Exposure

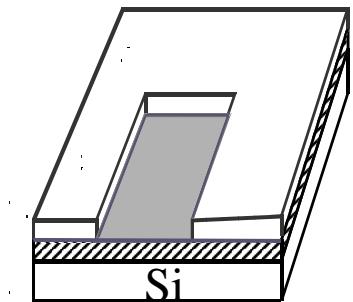
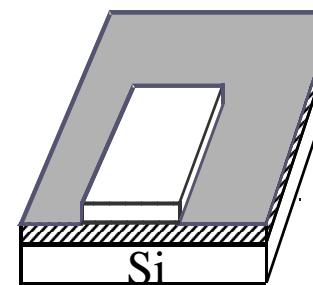


Modern Semiconductor Devices for Integrated Circuits (C. Hu)

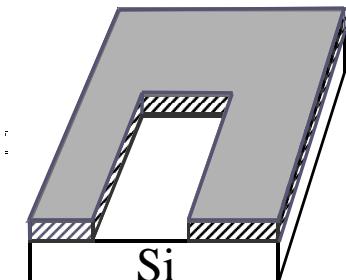
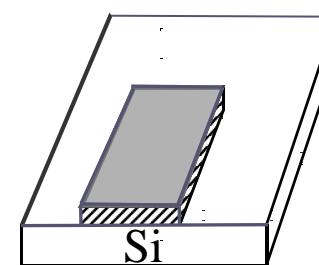
(c) Development

Positive resist

Negative resist



(d) Etching and Resist Strip





# Lithography Resolution

## Photolithography Resolution Limit, $R$

$R \geq k\lambda$  due to optical diffraction

- Wavelength  $\lambda$  needs to be minimized. (248 nm, 193 nm, 157 nm?)
- $k (<1)$  can be reduced

- Large aperture, high quality lens

- Immersive lithography

- EUV

- Phase-shift mask, etc.

- Lithography is difficult and expensive. There can be 40 lithography steps in an IC process.

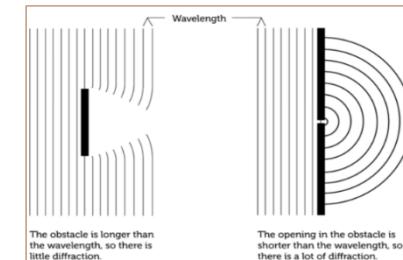


Figure 1.24

diffraction



# **Pattern Transfer–Etching**

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## ■ **Wet Etching**

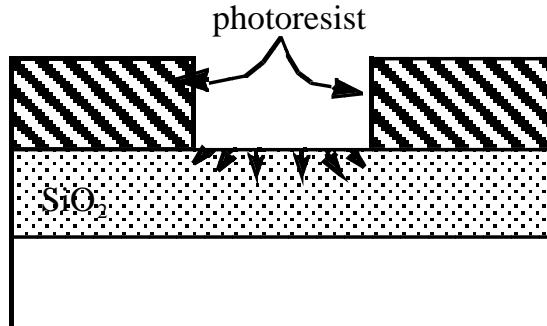
- material removal process that uses liquid chemicals or etchants to remove materials from a wafer.

## ■ **Dry Etching**

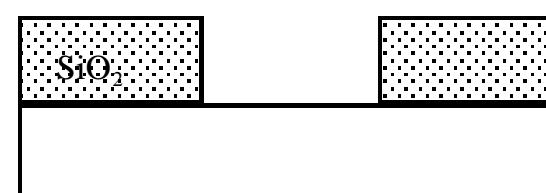
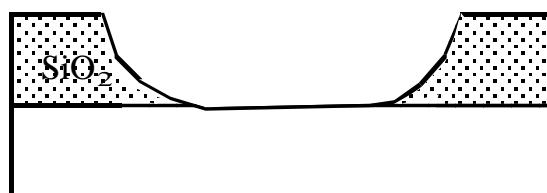
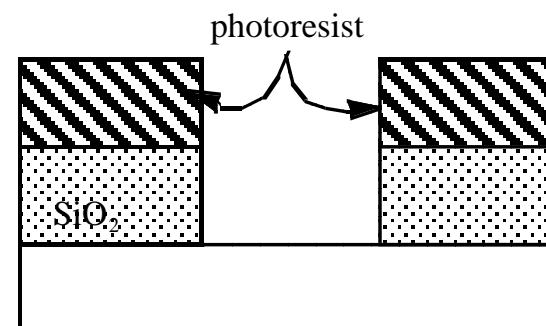
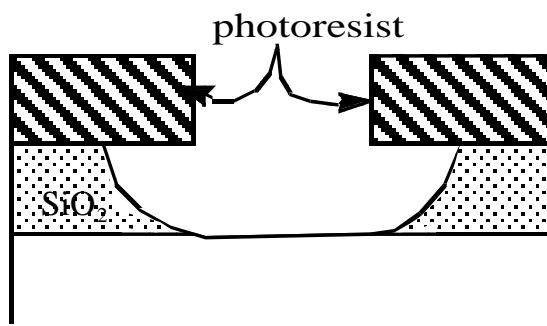
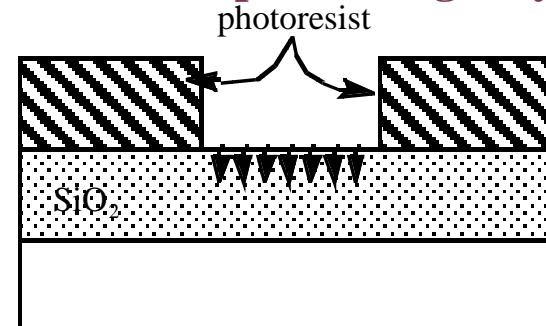
- material removal process by exposing the material to a bombardment of ions

# Pattern Transfer–Etching

Isotropic etching(wet)



Anisotropic etching (dry)



Modern Semiconductor Devices for Integrated Circuits (C. Hu)



# **Pattern Transfer–Etching**

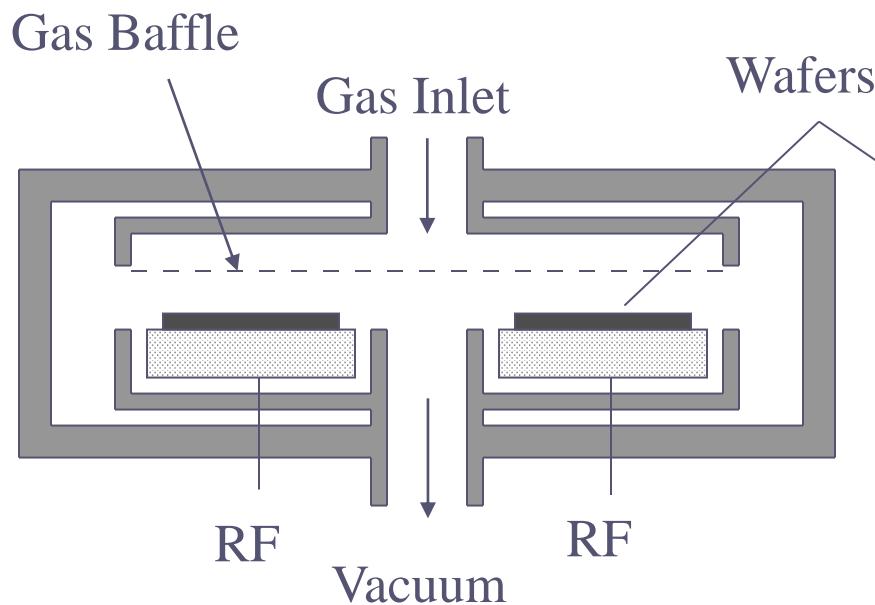
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*Dry Etching (also known as Plasma Etching, or Reactive-Ion Etching) is anisotropic.*

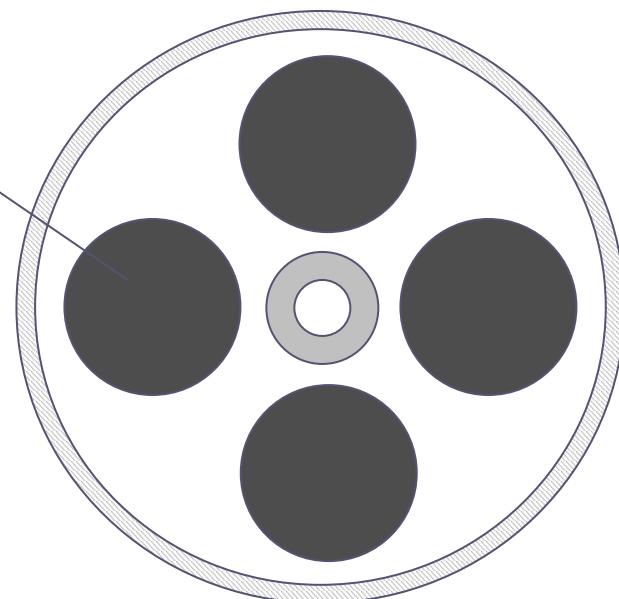
- Silicon and its compounds can be etched by plasmas containing F.
- Aluminum can be etched by Cl.
- Some concerns :
  - Selectivity and End-Point Detection
  - Plasma Process-Induced Damage or Wafer Charging Damage

# **Pattern Transfer–Etching**

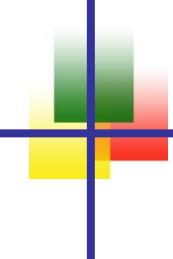
## *Reactive-Ion Etching Systems*



Cross-section View

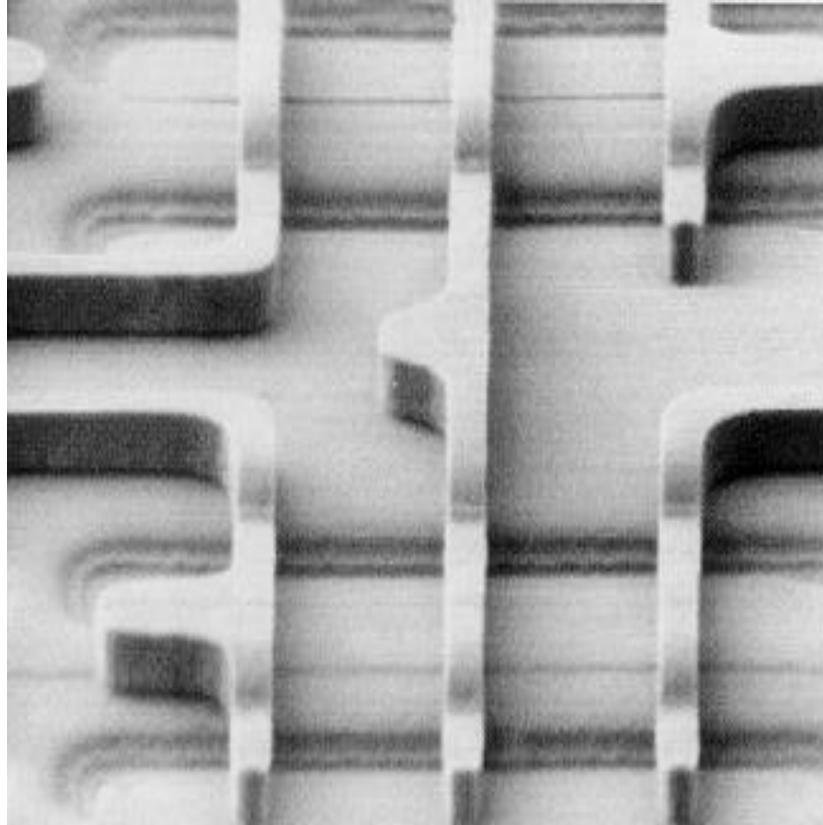


Top View



# ***Pattern Transfer–Etching***

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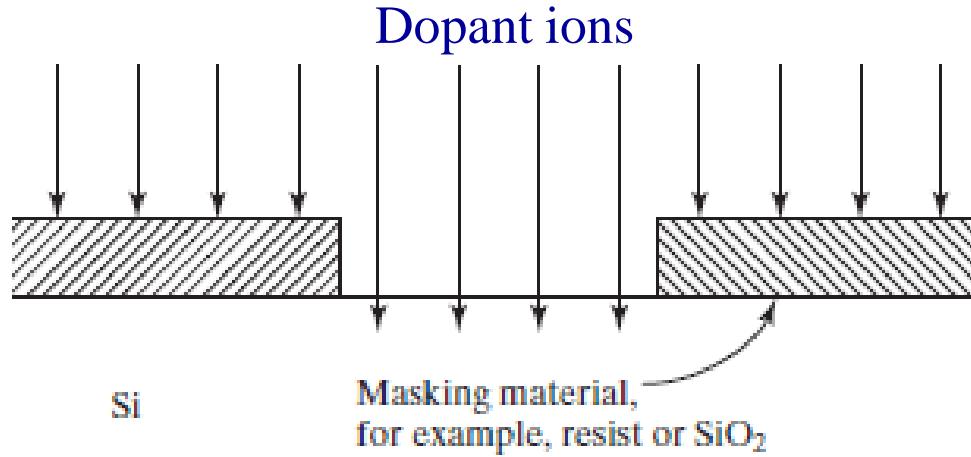
*Scanning electron microscope view of a plasma-etched  
0.16  $\mu\text{m}$  pattern in polycrystalline silicon film.*

Modern Semiconductor Devices for Integrated Circuits (C. Hu)



# Doping Ion Implantation

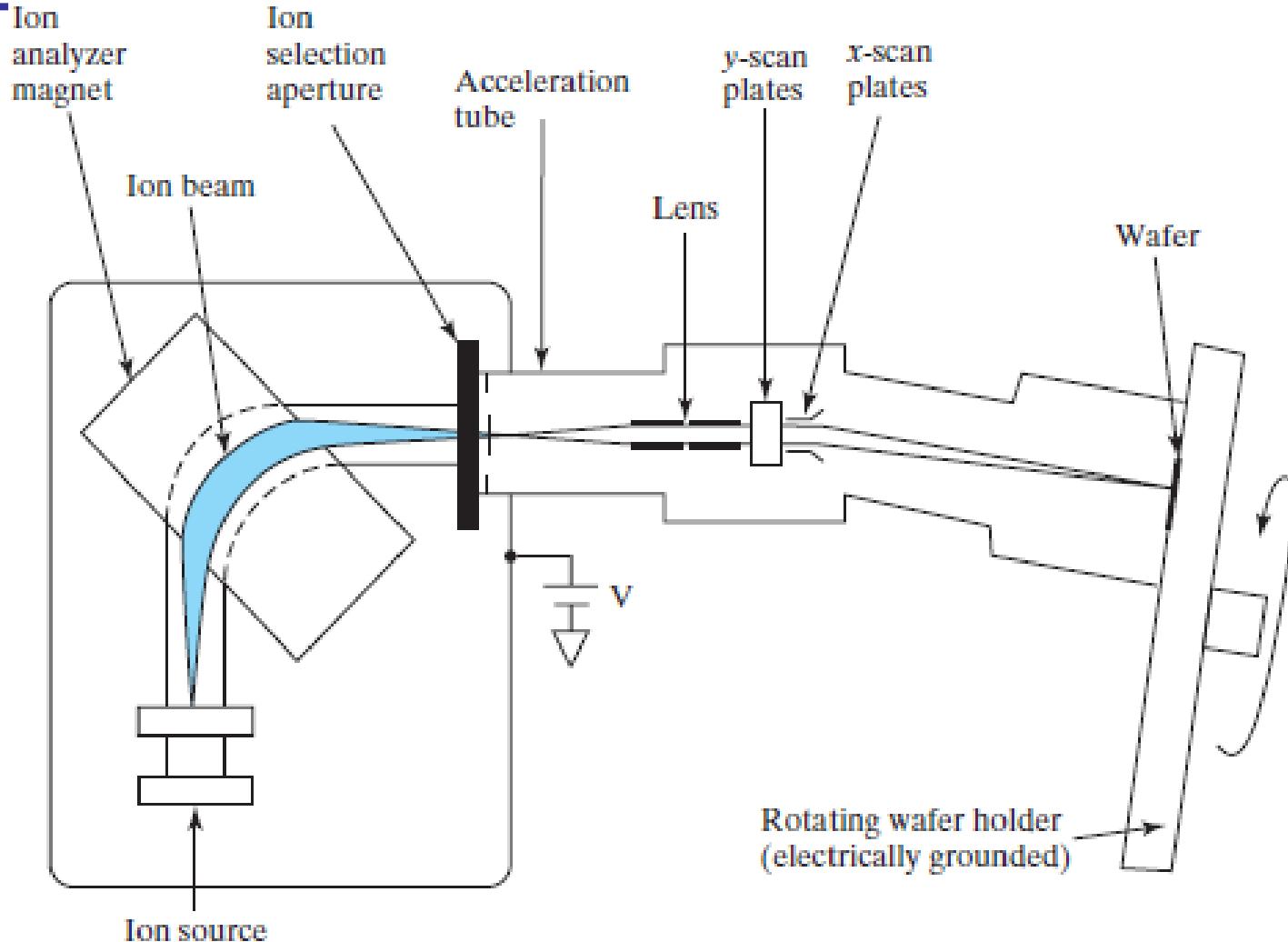
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- 
- The dominant doping method
  - Excellent control of **dose** ( $\text{cm}^{-2}$ )
  - Good control of implant depth with energy (KeV to MeV)
  - Repairing crystal damage and dopant activation requires annealing, which can cause dopant diffusion and loss of depth control.

# Ion Implantation

## *Schematic of an Ion Implanter*



Modern Semiconductor Devices for Integrated Circuits (C. Hu)



# *Dopant Diffusion*

---

## *Shallow Junction and Rapid Thermal Annealing*

- After ion implantation, thermal annealing is required.
- Furnace annealing takes minutes and causes too much diffusion of dopants for some applications.
- In rapid thermal annealing (RTA), the wafer is heated to high temperature in seconds by a bank of heat lamps.
- RTA
- In flash annealing (100mS) and laser annealing (<1uS), dopant diffusion is practically eliminated.



# Outline

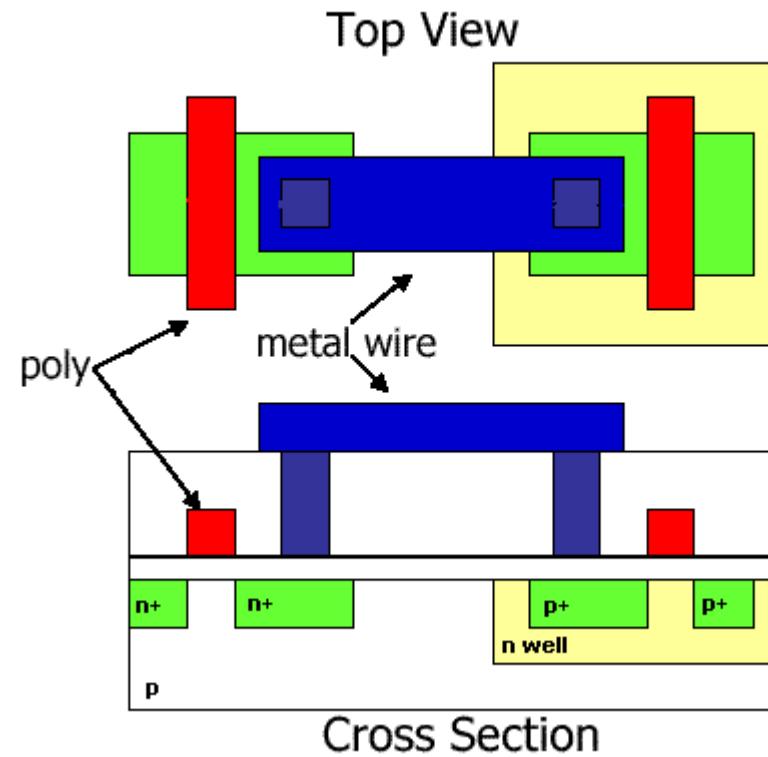
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- **Introduction to Integrated Circuits**
- **IC Evolution**
- **Device Fabrication**
  - Polysilicon
  - Isolation
  - Via
  - Metal
- **Conclusion**

# *Process after Doping*

- Polysilicon-silicon nitride Si<sub>3</sub>N<sub>4</sub>
- Isolation layer

- Metal
- Via



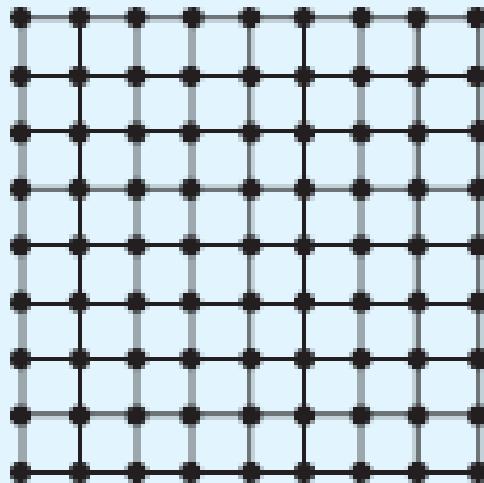
Modern Semiconductor Devices for Integrated Circuits (C. Hu)



# *Thin-Film Deposition*

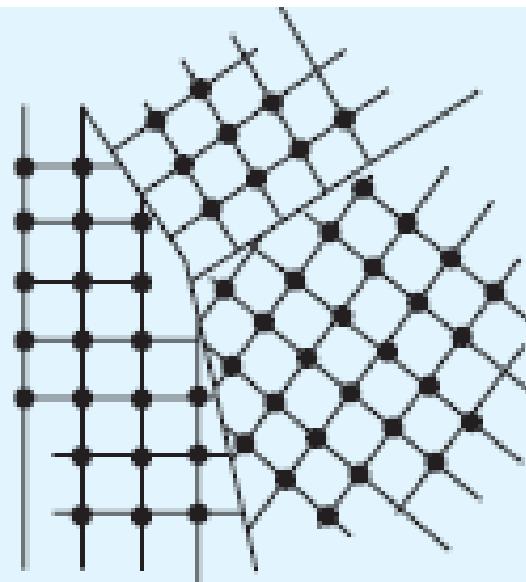
## *Three Kinds of Solid*

Crystalline



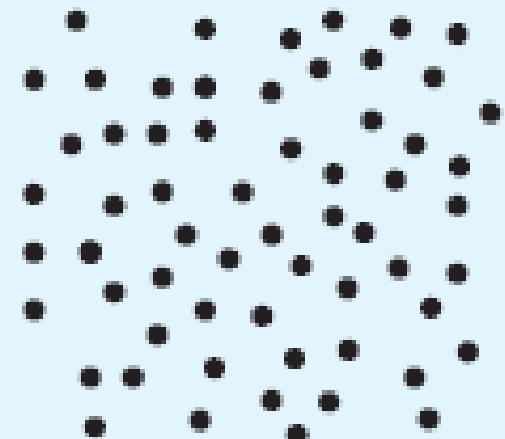
Example:  
Silicon wafer

Polycrystalline



Thin film of Si or metal.

Amorphous

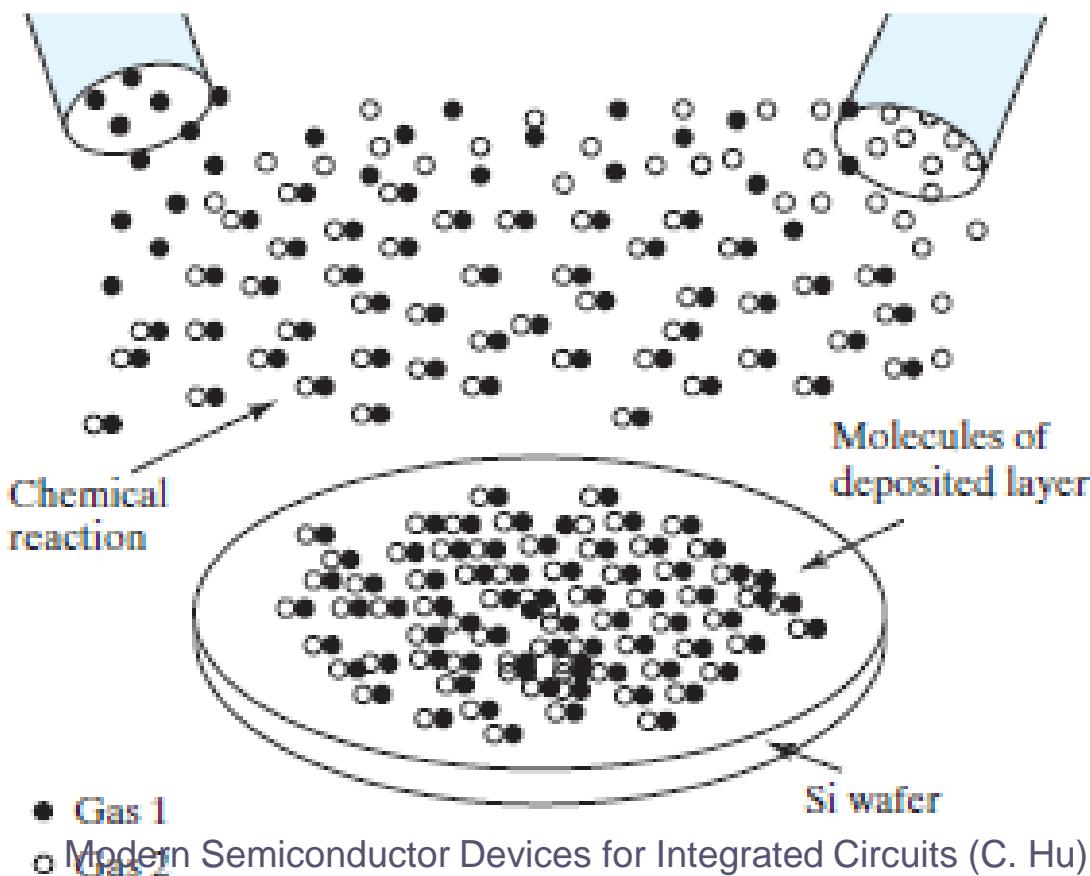


Thin film of  
 $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$ .

# Low Pressure Chemical Vapor Deposition (LPCVD)

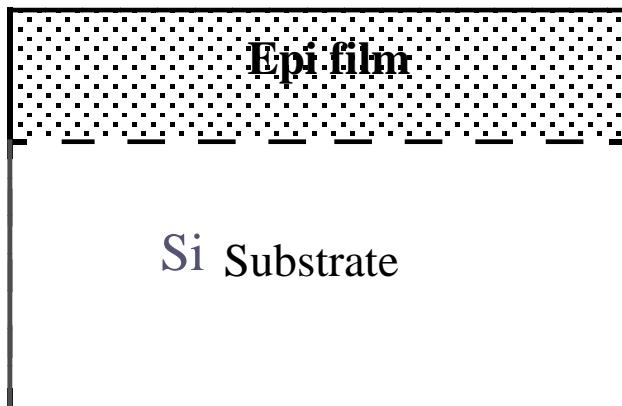
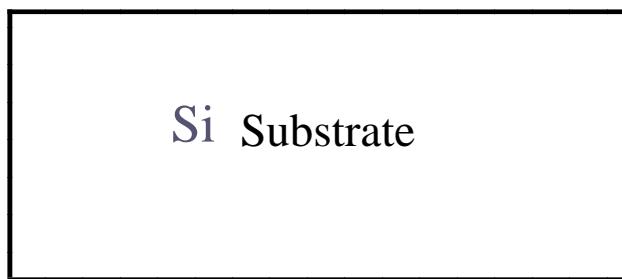
Thin film is formed from gas phase components.

- Polysilicon, Silicon Nitride
- Ex: Polysilicon; chemical decomposition of silane ( $\text{SiH}_4$ ) at high temperatures of 580 to 650 °C.
- $\text{SiH}_4(\text{g}) \rightarrow \text{Si}(\text{s}) + 2 \text{H}_2(\text{g})$  CVD at 500-800°C<sup>[8]</sup>

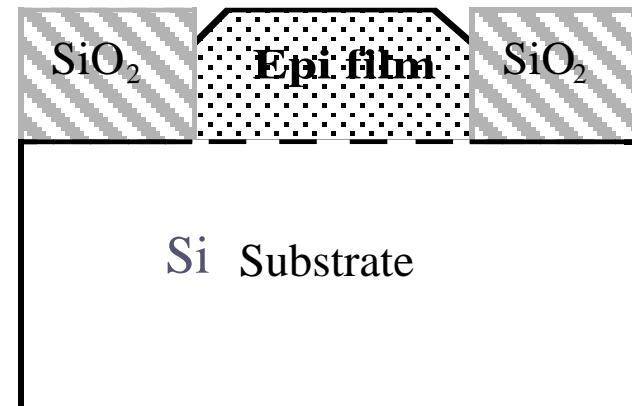
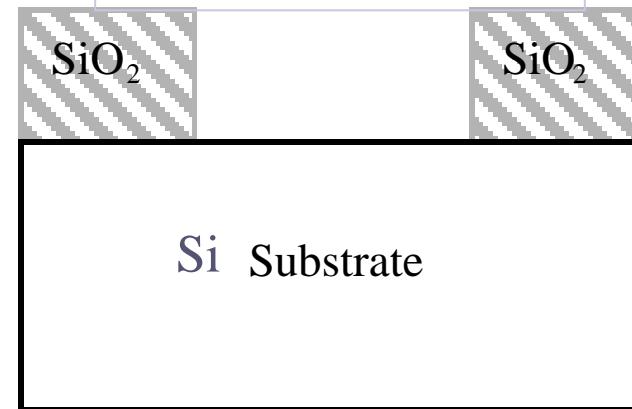


# Epitaxy (*Deposition of Single-Crystalline Film*)

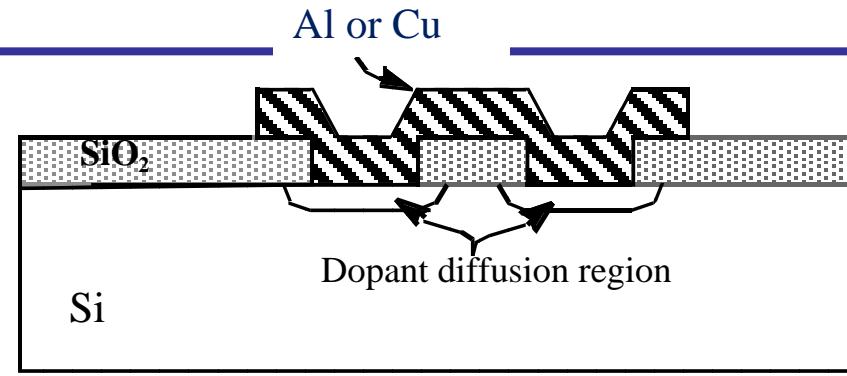
## Epitaxy



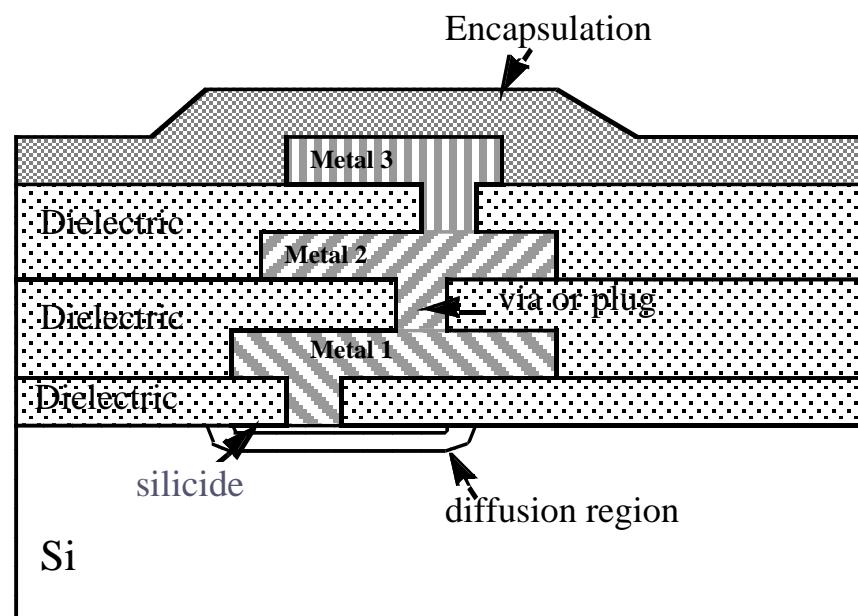
## Selective Epitaxy



# Interconnect – The Back-end Process



(a)

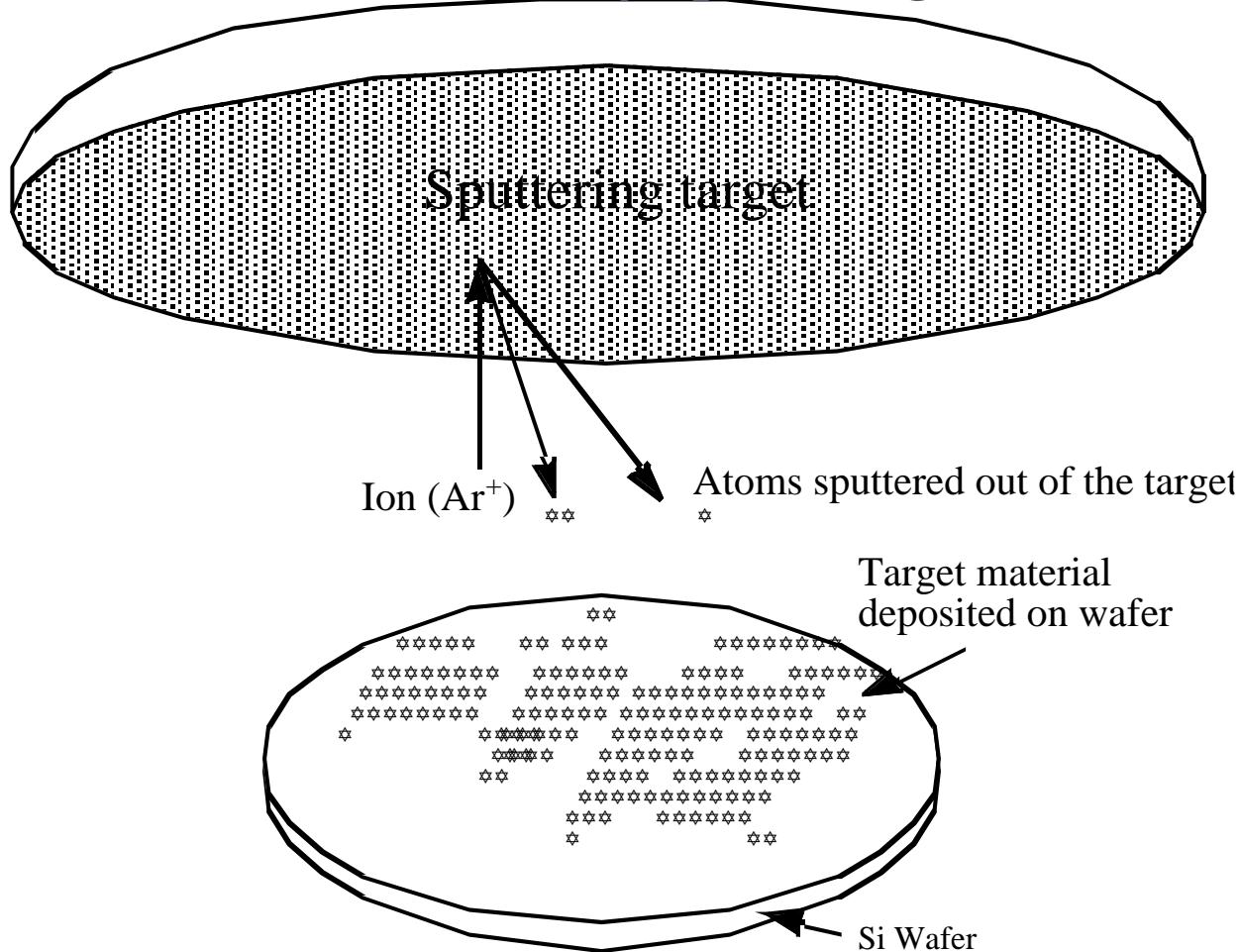


(b)

Modern Semiconductor Devices for Integrated Circuits (C. Hu)

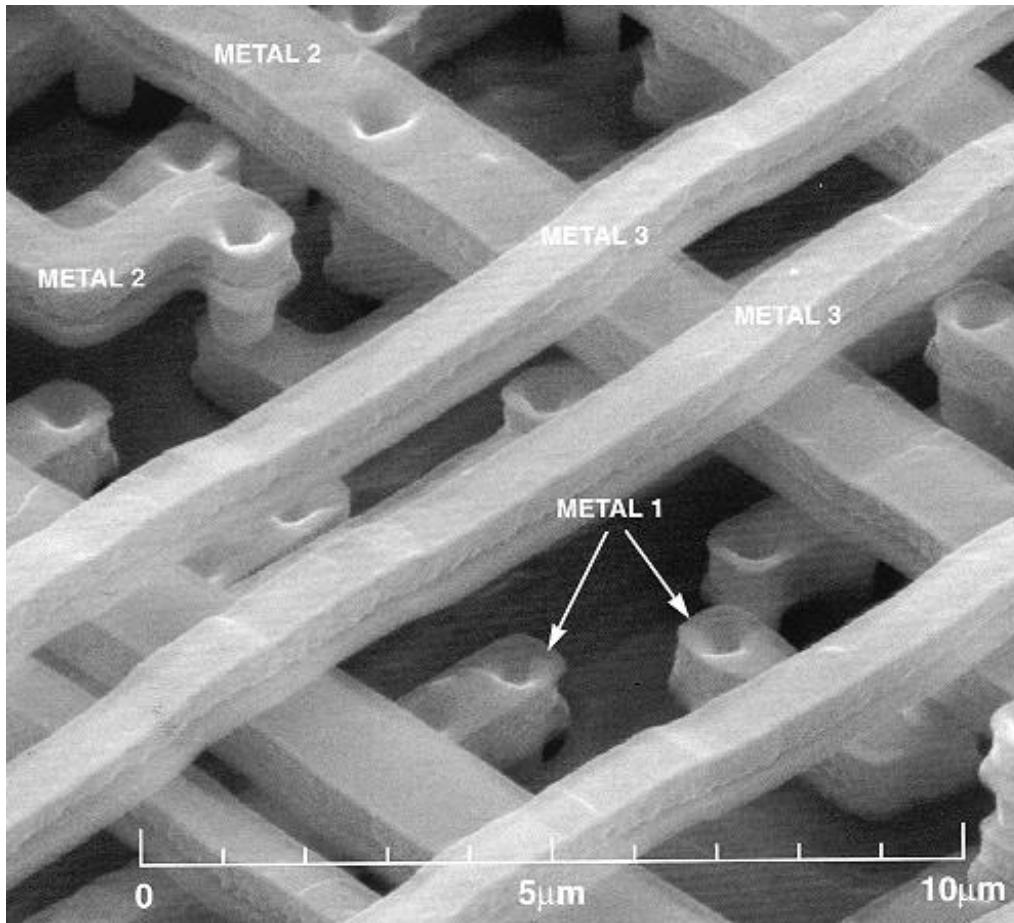
# Metal Formation -Sputtering

## *Schematic Illustration of Sputtering Process*



# *Interconnect – The Back-end Process*

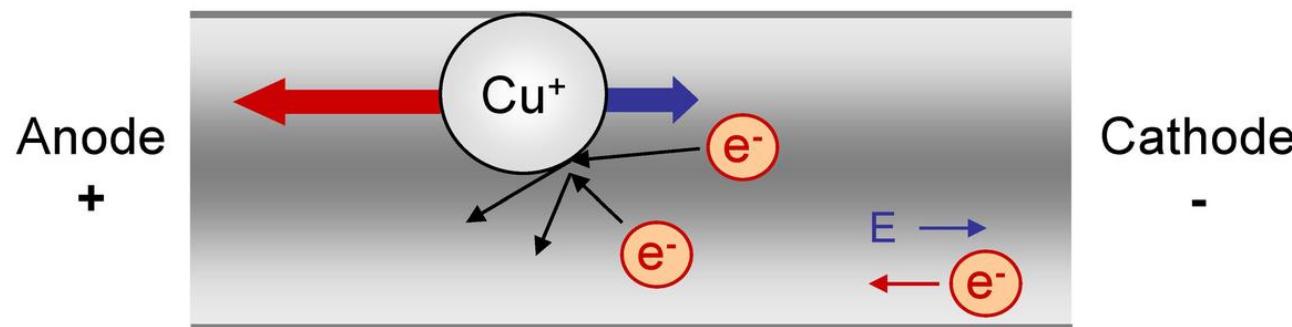
***SEM: Multi-Level Interconnect (after removing the dielectric)***



# Interconnect – The Back-end Process

## Copper Interconnect

- Al interconnect suffers from gap (holes) formation by electromigration.
- Cu has excellent electromigration reliability and 40% lower resistance than Al.



# Periodic Table

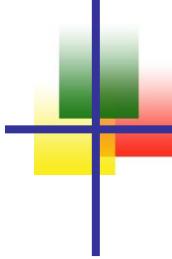


Atomic number  
Symbol  
Atomic weight

Metal  
Semimetal  
Nonmetal

<b>1</b>	<b>H</b> 1.008	<b>2</b>	<b>C</b> 12.01	<b>3</b>	<b>Li</b> 6.941	<b>4</b>	<b>Be</b> 9.012	<b>5</b>	<b>Sc</b> 44.96	<b>6</b>	<b>Ti</b> 47.88	<b>7</b>	<b>V</b> 50.94	<b>8</b>	<b>Cr</b> 52.00	<b>9</b>	<b>Mn</b> 54.94	<b>10</b>	<b>Fe</b> 55.85	<b>11</b>	<b>Co</b> 58.93	<b>12</b>	<b>Ni</b> 58.69	<b>13</b>	<b>Cu</b> 63.55	<b>14</b>	<b>Zn</b> 65.39	<b>15</b>	<b>Ga</b> 69.72	<b>16</b>	<b>Ge</b> 72.61	<b>17</b>	<b>As</b> 74.92	<b>18</b>	<b>Se</b> 78.96	<b>He</b> 19.00
<b>2</b>	<b>Li</b> 6.941	<b>3</b>	<b>Mg</b> 24.31	<b>4</b>	<b>Ca</b> 40.08	<b>5</b>	<b>Sc</b> 44.96	<b>6</b>	<b>Ti</b> 47.88	<b>7</b>	<b>V</b> 50.94	<b>8</b>	<b>Cr</b> 52.00	<b>9</b>	<b>Mn</b> 54.94	<b>10</b>	<b>Fe</b> 55.85	<b>11</b>	<b>Co</b> 58.93	<b>12</b>	<b>Ni</b> 58.69	<b>13</b>	<b>Cu</b> 63.55	<b>14</b>	<b>Zn</b> 65.39	<b>15</b>	<b>Ga</b> 69.72	<b>16</b>	<b>Ge</b> 72.61	<b>17</b>	<b>As</b> 74.92	<b>18</b>	<b>Se</b> 78.96	<b>He</b> 19.00		
<b>3</b>	<b>Na</b> 22.99	<b>4</b>	<b>Mg</b> 24.31	<b>5</b>	<b>K</b> 39.10	<b>6</b>	<b>Ca</b> 40.08	<b>7</b>	<b>Sc</b> 44.96	<b>8</b>	<b>Ti</b> 47.88	<b>9</b>	<b>V</b> 50.94	<b>10</b>	<b>Cr</b> 52.00	<b>11</b>	<b>Mn</b> 54.94	<b>12</b>	<b>Fe</b> 55.85	<b>13</b>	<b>Co</b> 58.93	<b>14</b>	<b>Ni</b> 58.69	<b>15</b>	<b>Cu</b> 63.55	<b>16</b>	<b>Zn</b> 65.39	<b>17</b>	<b>Ga</b> 69.72	<b>18</b>	<b>Ge</b> 72.61	<b>He</b> 19.00				
<b>4</b>	<b>Rb</b> 85.47	<b>5</b>	<b>Sr</b> 87.62	<b>6</b>	<b>Y</b> 88.91	<b>7</b>	<b>Zr</b> 91.22	<b>8</b>	<b>Nb</b> 92.91	<b>9</b>	<b>Mo</b> 95.94	<b>10</b>	<b>Tc</b> 98.91	<b>11</b>	<b>Ru</b> 101.1	<b>12</b>	<b>Rh</b> 102.9	<b>13</b>	<b>Pd</b> 106.4	<b>14</b>	<b>Ag</b> 107.9	<b>15</b>	<b>Cd</b> 112.4	<b>16</b>	<b>In</b> 114.8	<b>17</b>	<b>Sn</b> 118.7	<b>18</b>	<b>Sb</b> 121.8	<b>He</b> 127.6	<b>19</b>	<b>Te</b> 126.9	<b>20</b>	<b>I</b> 131.3		
<b>5</b>	<b>Cs</b> 132.9	<b>6</b>	<b>Ba</b> 137.3	<b>7</b>	<b>Lu</b> 175.0	<b>8</b>	<b>Hf</b> 178.5	<b>9</b>	<b>Ta</b> 180.9	<b>10</b>	<b>W</b> 183.8	<b>11</b>	<b>Re</b> 186.2	<b>12</b>	<b>Os</b> 190.2	<b>13</b>	<b>Ir</b> 192.2	<b>14</b>	<b>Pt</b> 195.1	<b>15</b>	<b>Au</b> 197.0	<b>16</b>	<b>Hg</b> 200.6	<b>17</b>	<b>Tl</b> 204.4	<b>18</b>	<b>Pb</b> 207.2	<b>19</b>	<b>Bi</b> 209.0	<b>20</b>	<b>At</b> 210.0	<b>21</b>	<b>Rn</b> 222.0			
<b>6</b>	<b>Fr</b> 223.0	<b>7</b>	<b>Ra</b> 226.0	<b>8</b>	<b>Lr</b> 262.1	<b>9</b>	<b>Rf</b> 261.1	<b>10</b>	<b>Db</b> 262.1	<b>11</b>	<b>Sg</b> 263.1	<b>12</b>	<b>Bh</b> 264.1	<b>13</b>	<b>Hs</b> 265.1	<b>14</b>	<b>Mt</b> 268	<b>15</b>	<b>Uun</b> 269	<b>16</b>	<b>Uuu</b> 272	<b>17</b>	<b>Uub</b> 277	<b>18</b>	<b>Uut</b> 289	<b>19</b>	<b>Uuq</b> 289	<b>20</b>	<b>Uup</b> 289	<b>21</b>	<b>Uuh</b> 289	<b>22</b>	<b>Uus</b> 289	<b>23</b>	<b>Uuo</b> 293	
<b>6</b> <b>La</b> 138.9 <b>Ce</b> 140.1 <b>Pr</b> 140.9 <b>Nd</b> 144.2 <b>Pm</b> 146.9 <b>Sm</b> 150.4 <b>Eu</b> 152.0 <b>Gd</b> 157.3 <b>Tb</b> 158.9 <b>Dy</b> 162.5 <b>Ho</b> 164.9 <b>Er</b> 167.3 <b>Tm</b> 168.9 <b>Yb</b>  <b>7</b> <b>Ac</b> 227.0 <b>Th</b> 232.0 <b>Pa</b> 231.0 <b>U</b> 236.0 <b>Np</b> 237.0 <b>Pu</b> 244.1 <b>Am</b> 243.1 <b>Cm</b> 247.1 <b>Bk</b> 247.1 <b>Cf</b> 251.1 <b>Dy</b> 252.0 <b>Es</b> 257.1 <b>Fm</b> 258.1 <b>Md</b> 259.1 <b>No</b>																																				

(c)1998  
Kremer Paul

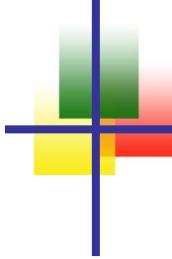


# *Interconnect – The Back-end Process*

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## *Planarization*

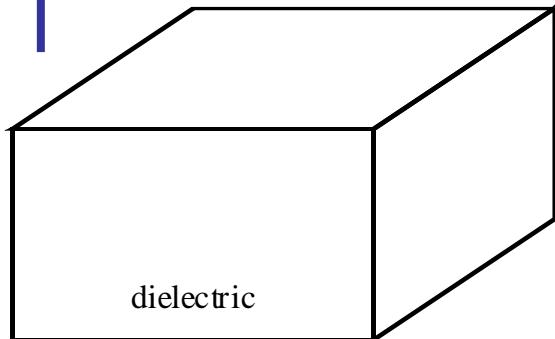
- A flat surface is highly desirable for subsequent lithography and etching.
- CMP (Chemical-Mechanical Polishing) is used to planarize each layer of dielectric in the interconnect system. Also used in the front-end process.



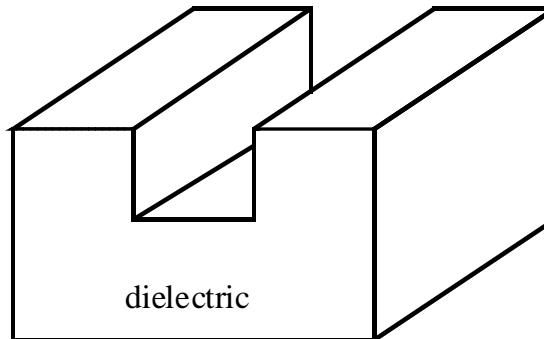
# *Interconnect – The Back-end Process*

## *Copper Damascene Process*

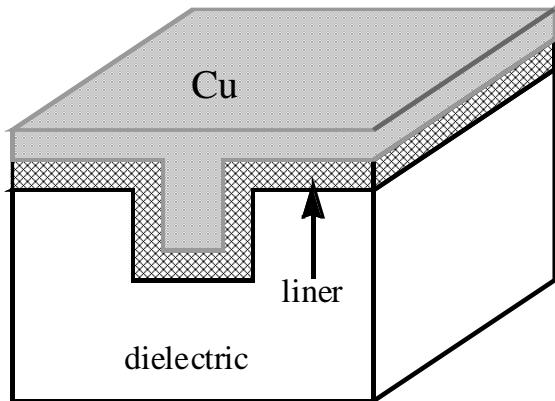
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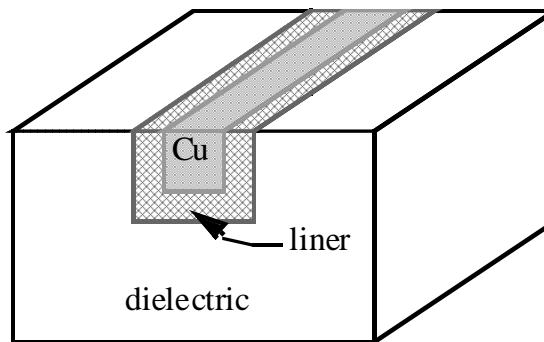
(a)



(b)



(c)



(d)

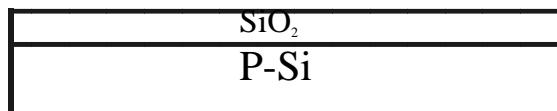
- Chemical-Mechanical Polishing (CMP) removes unwanted materials.
- Barrier liner prevents Cu diffusion.

# Summary—A Device Fabrication Example

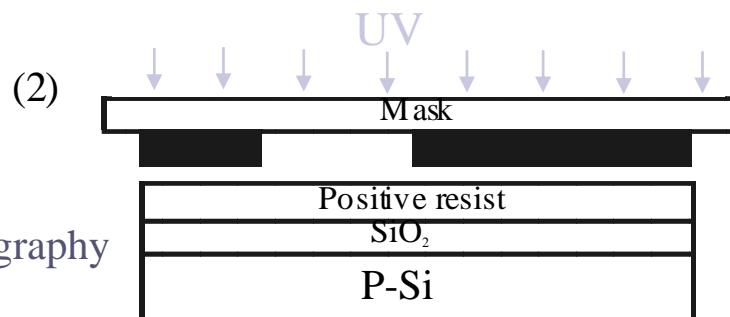
Wafer (0)



(1) Oxidation



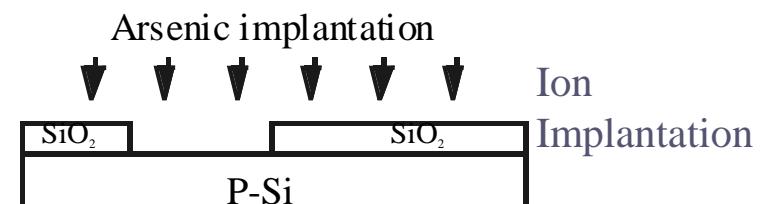
Lithography



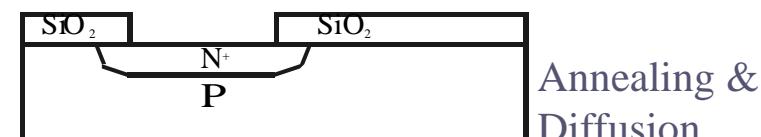
(3) Etching



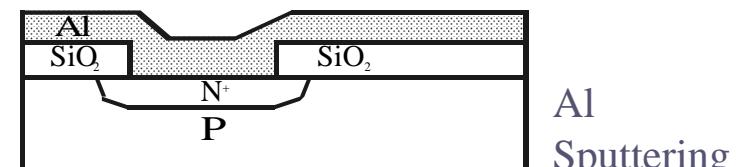
(4)



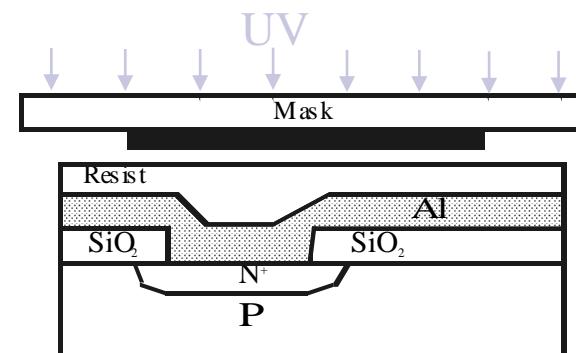
(5)



(6)



(7)

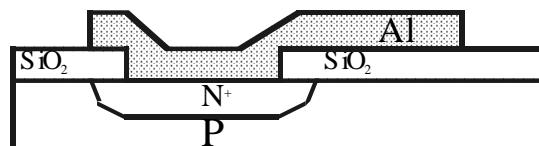


Lithography

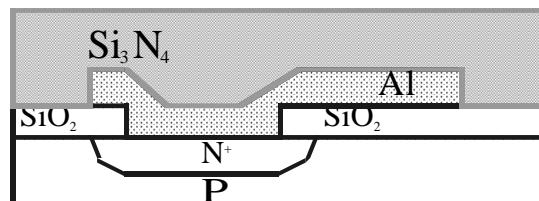
Modern Semiconductor Devices for Integrated Circuits (C. Hu)

# Summary—A Device Fabrication Example

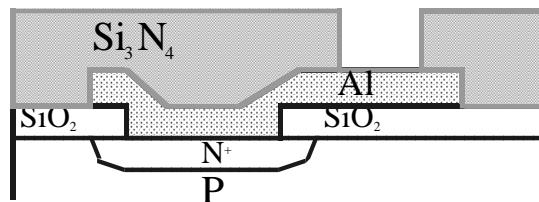
Metal etching  
(8)



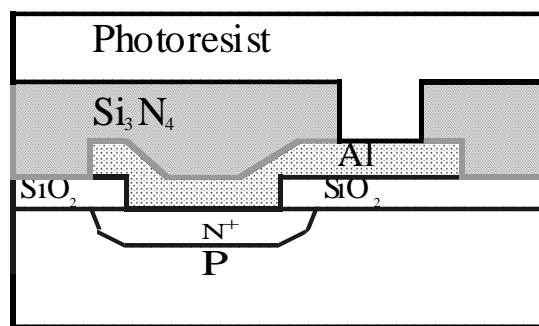
CVD nitride deposition  
(9)



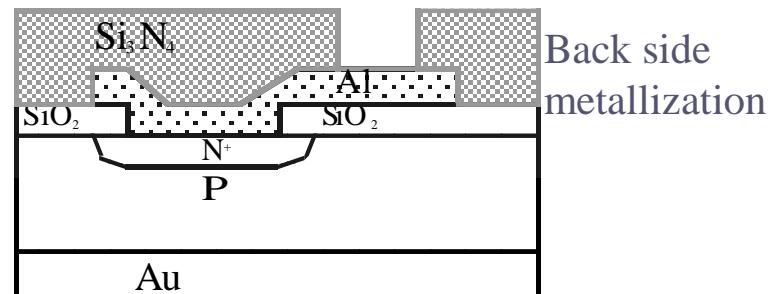
Lithography and etching  
(10)



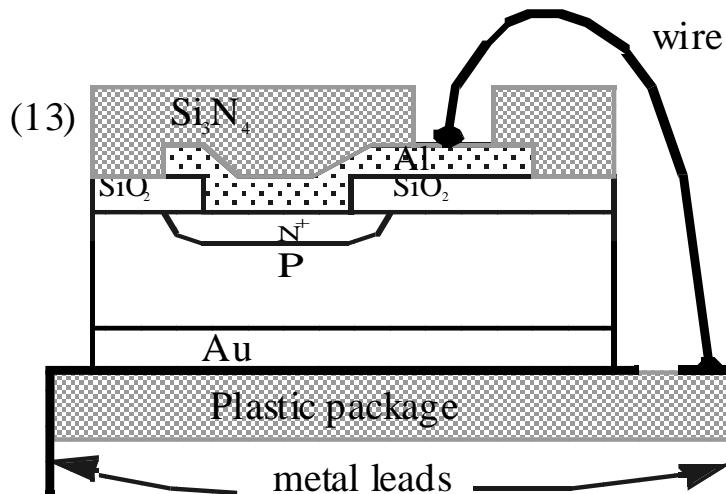
Back Side milling  
(11)



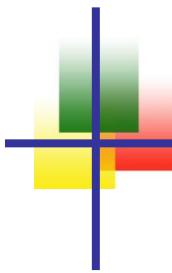
(12)



(13)



Dicing, wire bonding,  
and packaging

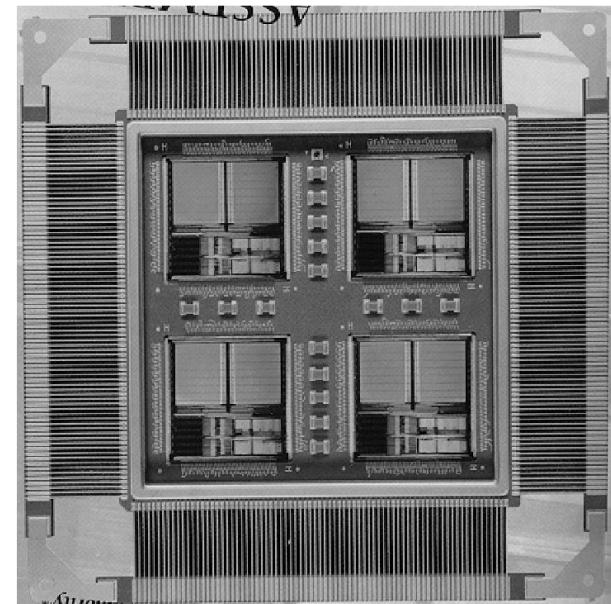


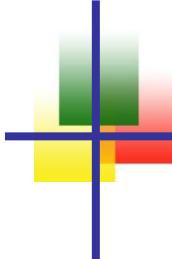
# Testing, Assembly, and Qualification

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## *Testing, Assembly, and Qualification*

- Wafer acceptance test
- Die sorting
- Wafer sawing or laser cutting
- Packaging
- Flip-chip solder bump technology
- Multi-chip modules
- Burn-in
- Final test
- Qualification
- TSMC manufacture





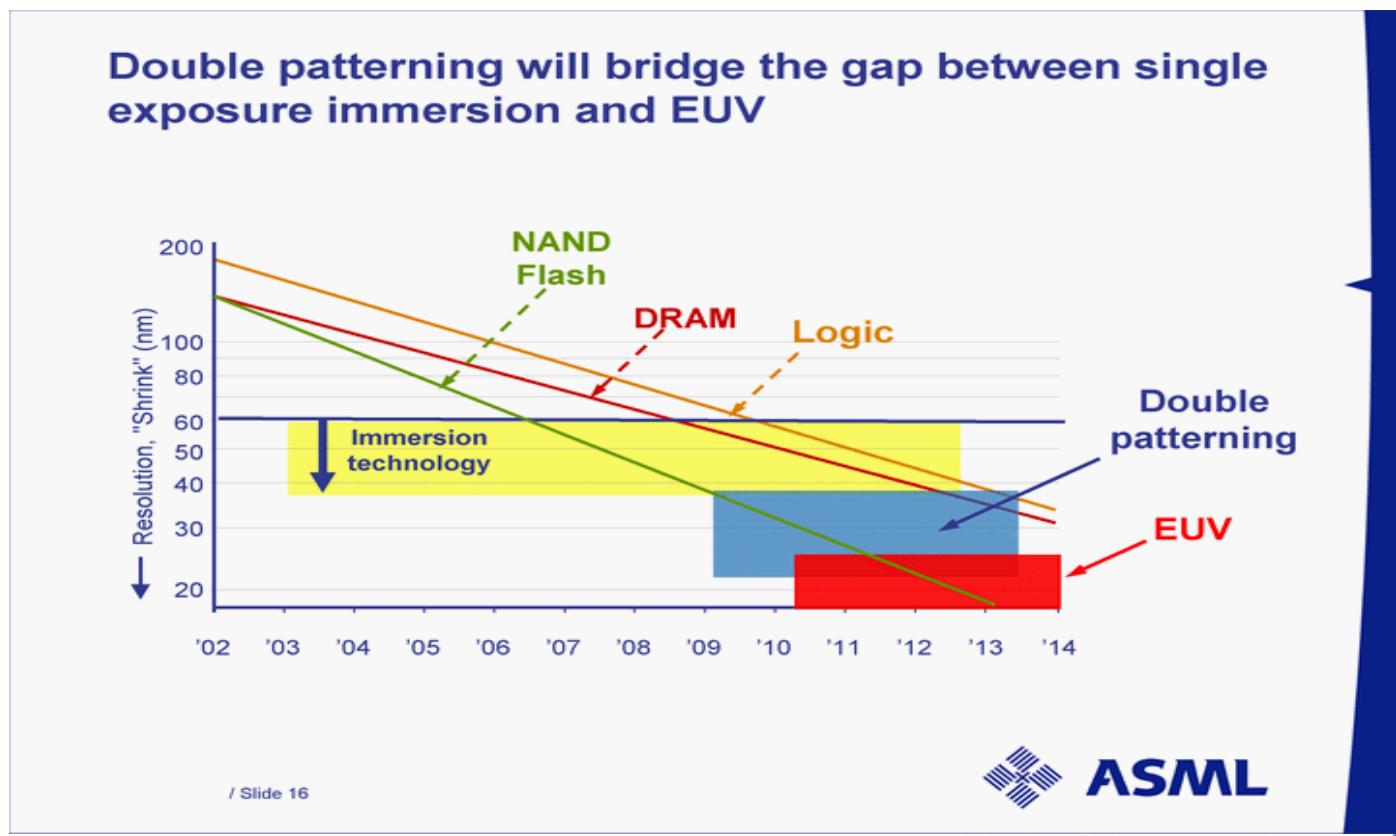
# Semiconductor Process

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Semiconductor process

# 製程技術演進與預測 (Lithography)

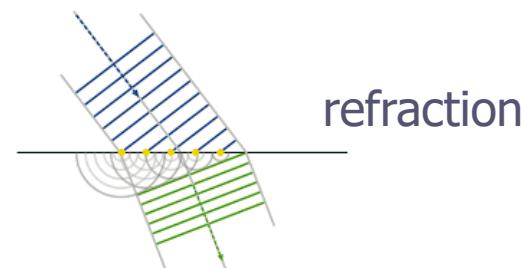
ASML: Netherlands Company provides lithography systems for semiconductor  
Industries using extreme ultraviolet (EUV) at 13.5nm technology



# *Wet/ Immersion Lithography*

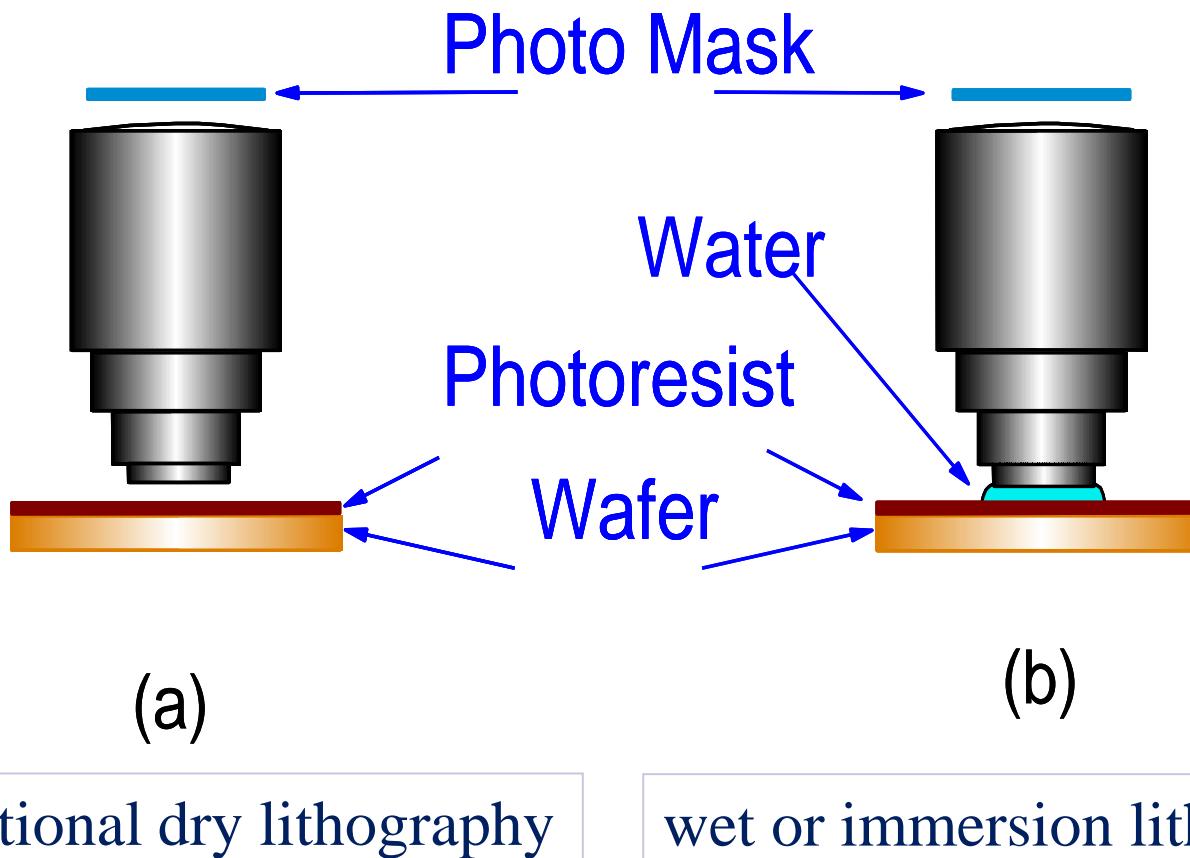
## ■ Immersion lithography

- liquid medium between the final lens and the wafer surface
- liquid medium refractive index greater than one
- Resolution increased by a factor of refractive index
- Water is most used with refractive index 1.44
- IBM and AMD use immersion lithography at 65nm and 45nm nodes



Modern Semiconductor Devices for Integrated Circuits (C. Hu)

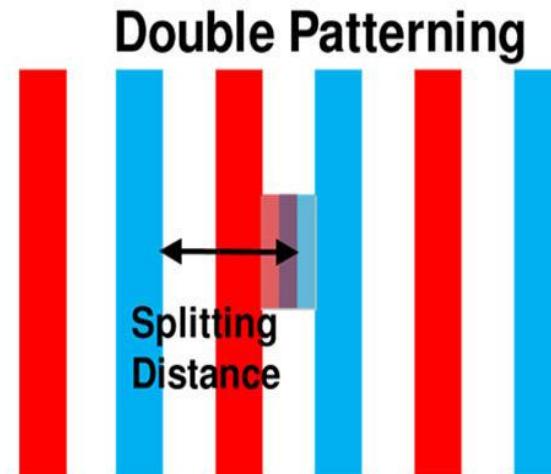
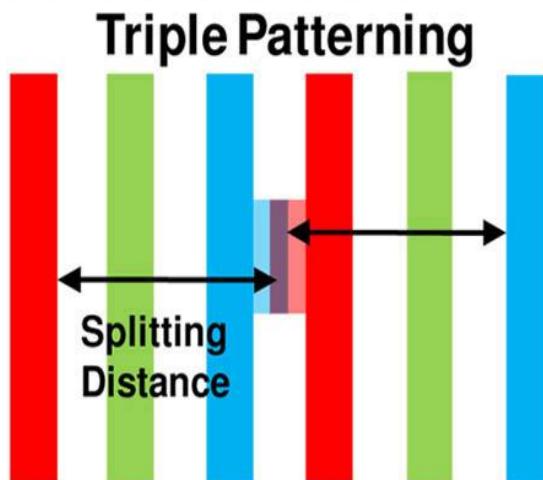
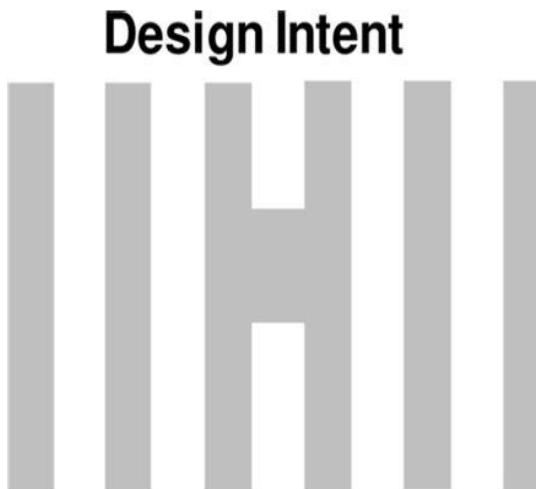
# Wet Lithography

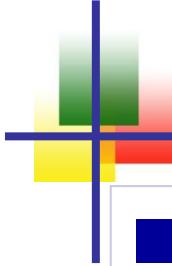


conventional dry lithography

wet or immersion lithography

# Double Patterning





# ***Extreme ultraviolet (EUV) Lithography***

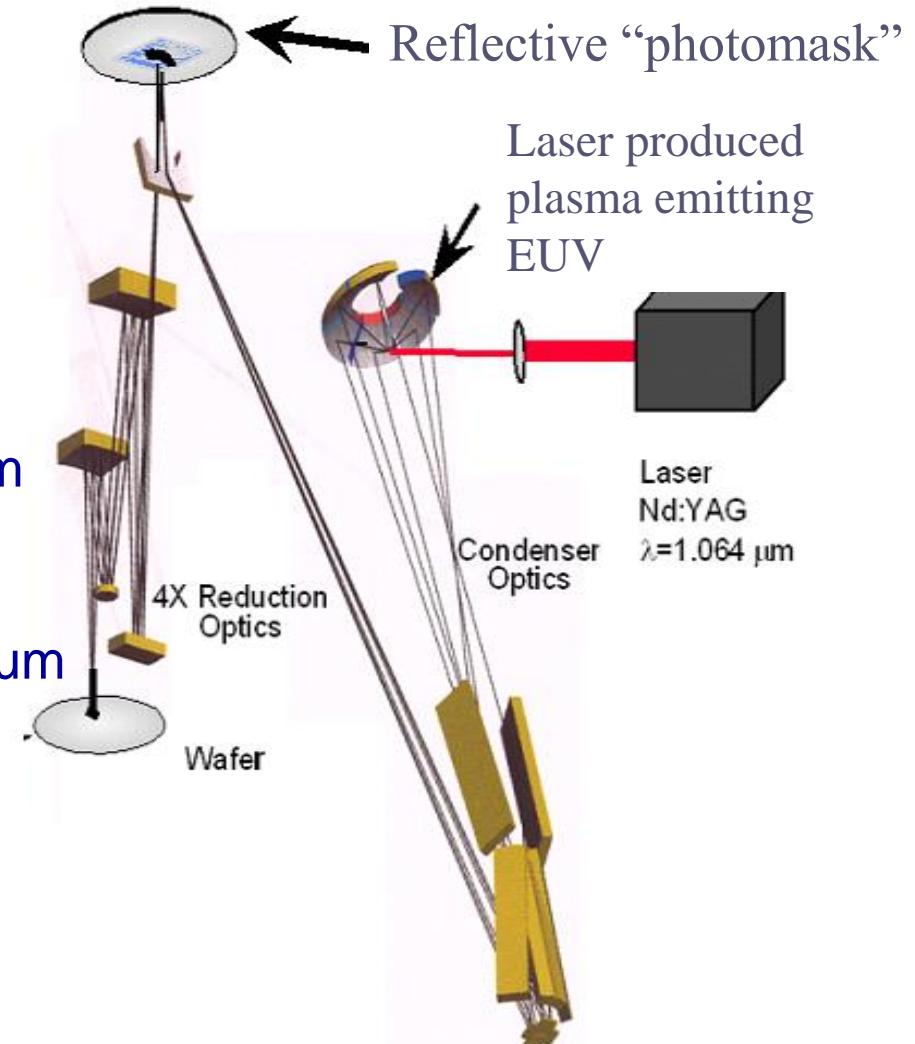
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## ■ Extreme ultraviolet lithography

- With light wavelength 13.5nm
- EUV light source uses a high power laser to create a plasma.
- Emit a short wavelength light inside a vacuum chamber.
- Several multilayer mirrors in the chamber to reflect light via interlayer interference.
- Start to use in 7nm process

# Extreme UV Lithography (13.5 nm wavelength)

- No suitable lens material at this wavelength.
- Optics is based on mirrors with nm flatness.
- **Nd:YAG** (neodymium-doped yttrium aluminium garnet; Nd:Y<sub>3</sub>Al<sub>5</sub>O<sub>12</sub>) is a crystal that is used as a lasing medium for solid-state lasers.



# Semiconductor Process Evolution

Node=size reduction, HP=high performance(deliver twice gate density)

## Customer lithography roadmap by sector

YEAR	DRAM	NAND	MPU	LOGIC
	Node = HP [nm]	Node = HP [nm]	Node / HP [nm]	Node / HP [nm]
2007	65	55	45 / 80	
2008	55	42		45 / 70
2009	52	35	32 / 60	40 / 70
2010	45	28		32 / 50
2011	38	22	22 / 40	28 / 50
2012	32	20		
2013	28	18	15 / 30	22 / 35 DPT
2014	25	15		
2015	22	12	11 / 22	15/30

Single exposure

Double patterning  
ie., Spacer

Double patterning  
LELE

EUV

EUV INSERTION TIME FAVORED BY DESIGN LIMITATIONS, COST AND PROCESS CONTROL REQUIREMENTS OF DOUBLE PATTERNING, MAKING EUV PROCESS OF CHOICE WHEN ACHIEVING ITS COST TARGETS

Source: ASML Marketing (4/10)

/ Slide 20

Public



# Semiconductor Process Evolution

ITRS-International Technology Roadmap for Semiconductor

Node	2014	2015	2016	2017	2018
22/20 nm	 				
16/14 nm FinFET			  		
10 nm			  		
7 nm				 	

# Semiconductor Process Evolution

ITRS-International Technology Roadmap for Semiconductor

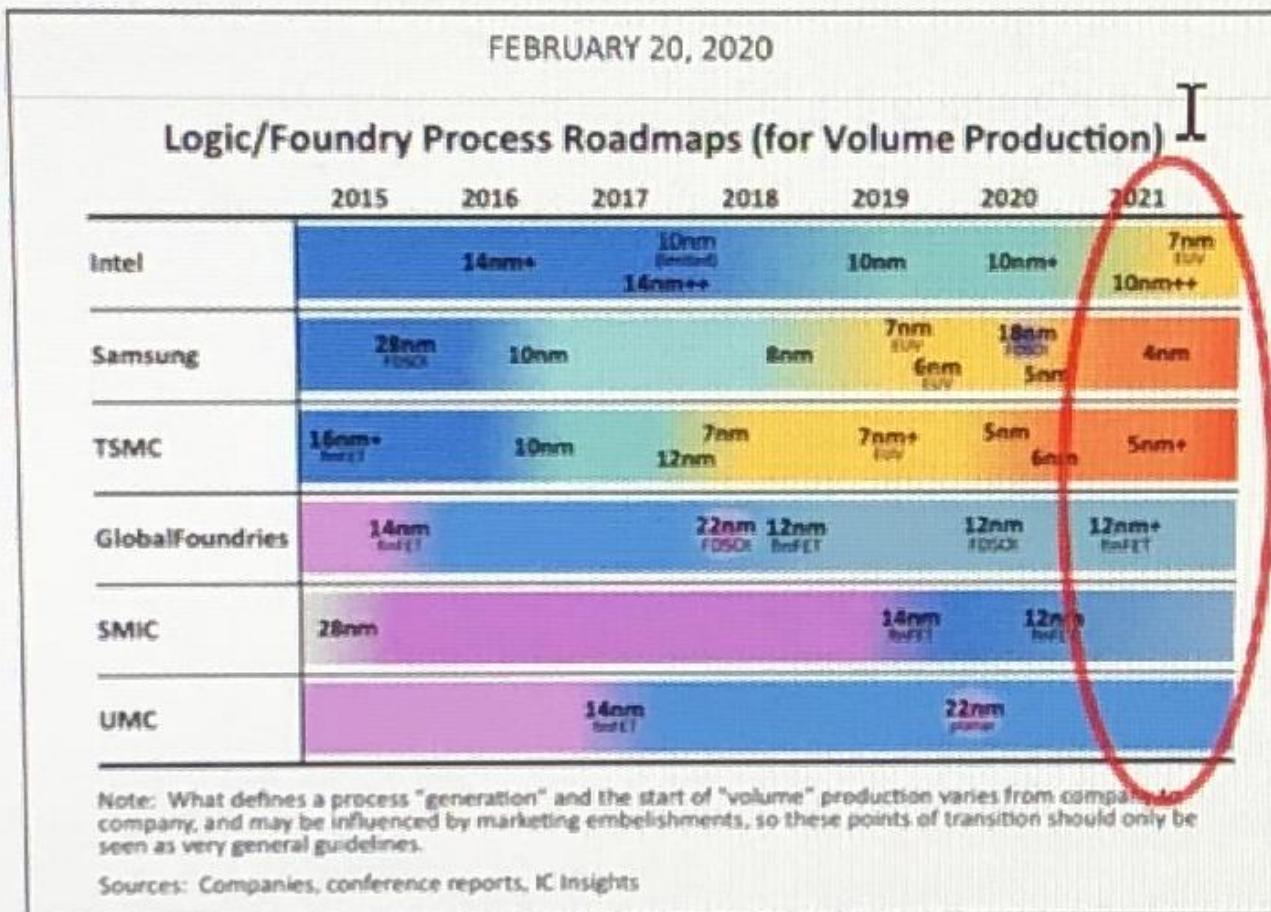
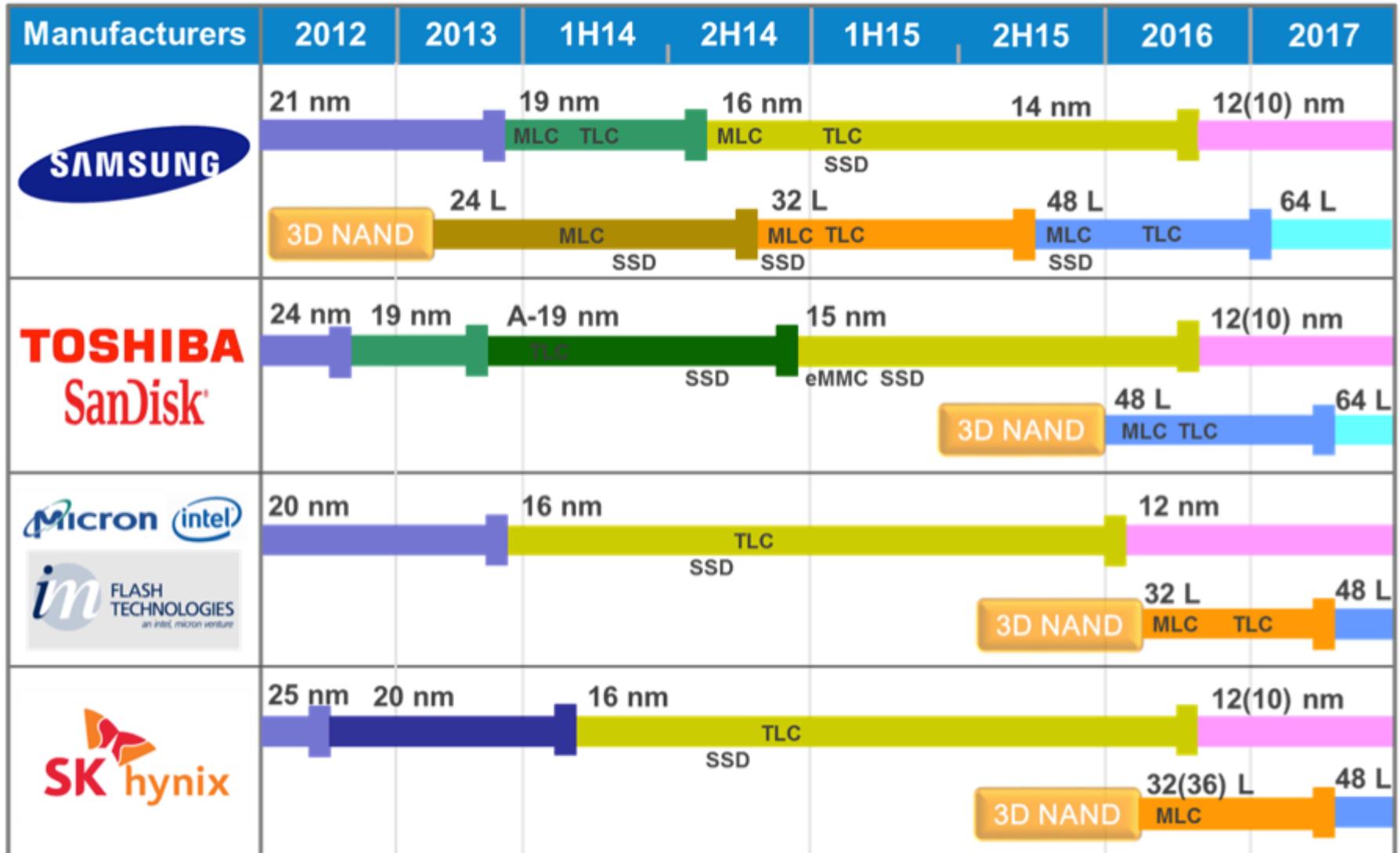


Figure ES6

Industry unrealistic node nomenclature

# NAND Expectation By SRC Roadmap



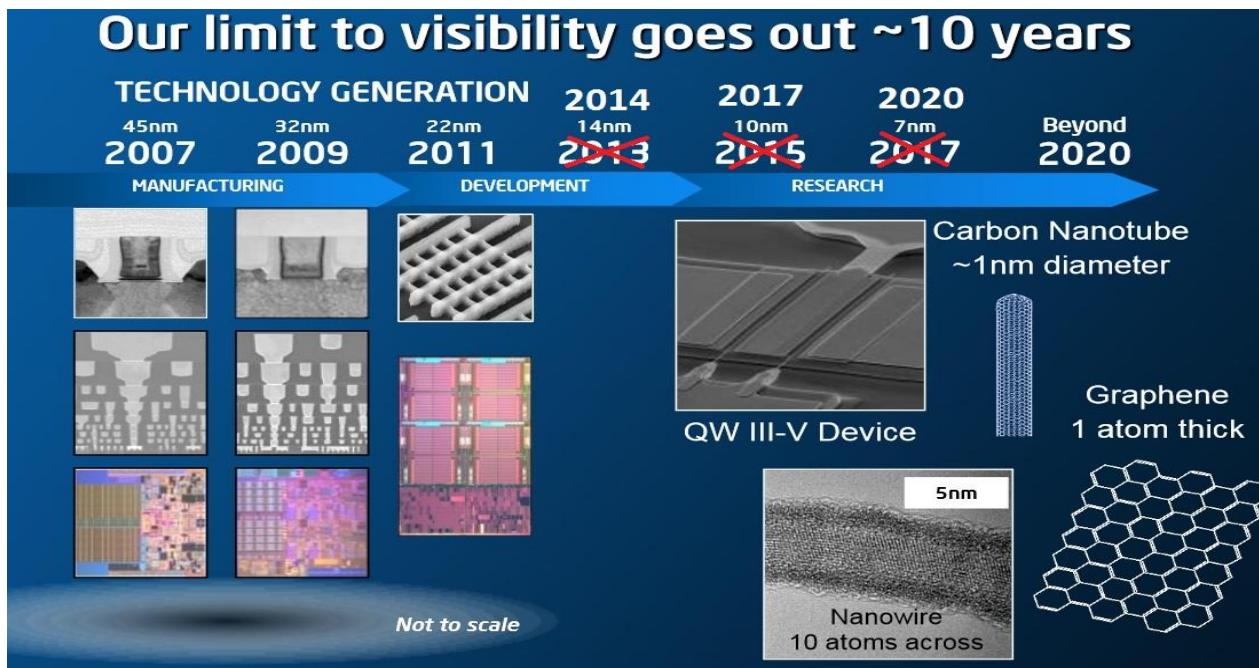
MLC=Multi-level cell/2 bit/cell(4 states) TLC-triple level cell(3 bit/cell)8 states  
 3D Nand 24L (24 layers)



# Nanotransistor Scaling

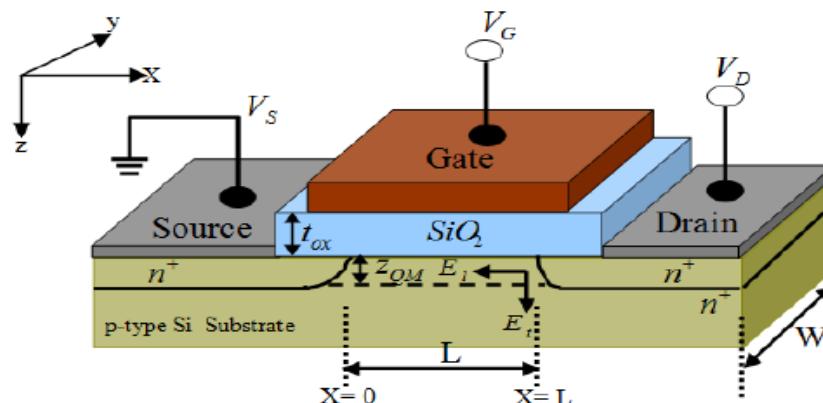
## ■ Scaling

- Gate length
- Supply voltage decreases (e.g. .25um -> 2.5 V, 90nm-> 1V)
- Threshold voltage decreases
- Thinnness of Dielectric ( $\text{SiO}_2$ ) below gate decreases



# Pros of Nanotransistor Scaling

- More Moore targets bringing PPAC value for node scaling every 2–3 years:
  - (P)erformance: >15% more operating frequency at scaled supply voltage (frequency increases, voltage decreases)
  - (P)ower: >35% less energy per switching at a given performance
  - (A)rea: >35% less chip area footprint
  - (C)ost: <30% more wafer cost – 20% less die cost for scaled die.

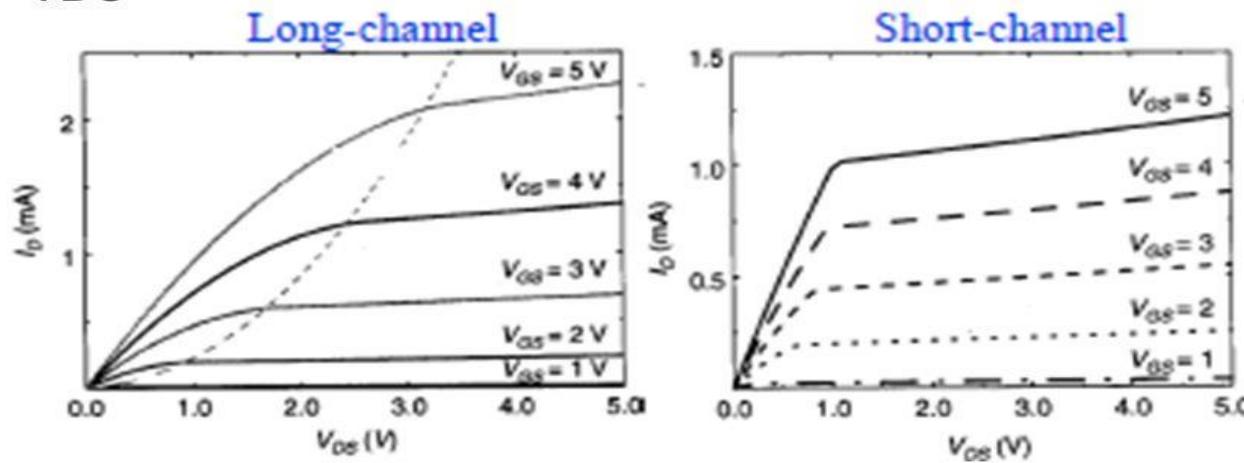


# Cons of Nanotransistor

## ■ Short channel effect

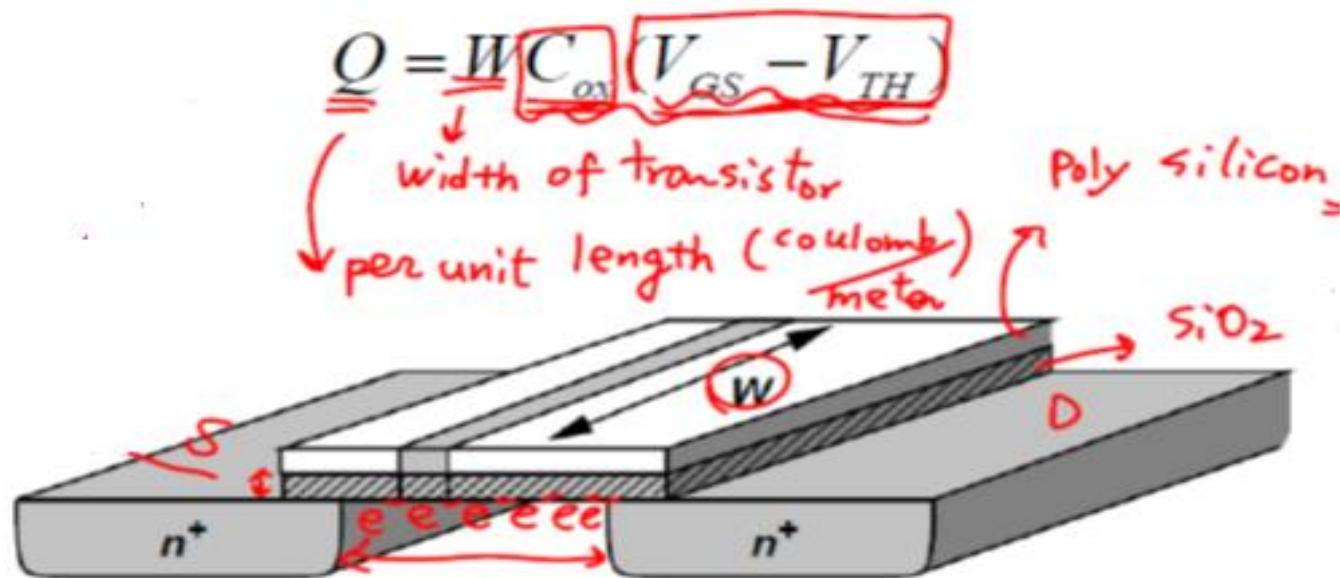
### Short-channel and long channel comparison

- Linear dependence on  $V_{GS}$  in short-channel device
- Short-channel device has  $\sim 40\%$  less current at high  $V_{DS}$



# Current Characteristics

- The gate/Oxide/semiconductor can be viewed as a capacitor
- The charge accumulated at the channel is proportional to the area of the capacitor
- For drift current, the relation between the mobile charge density and current can be expressed

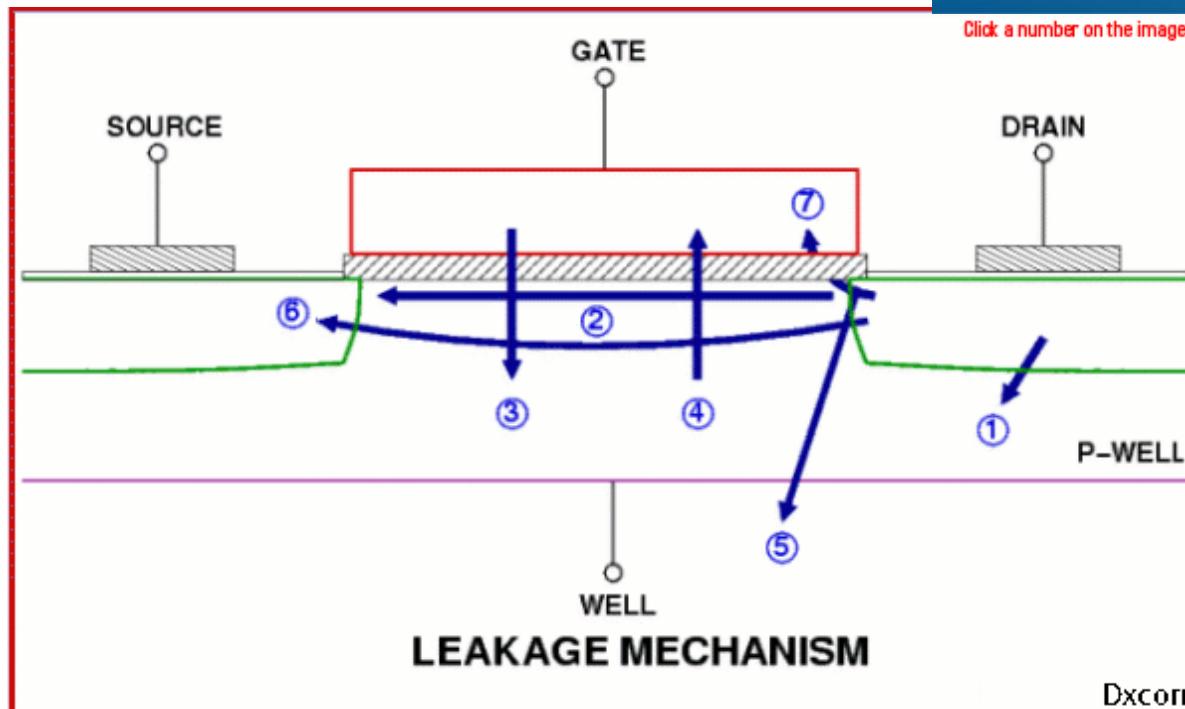
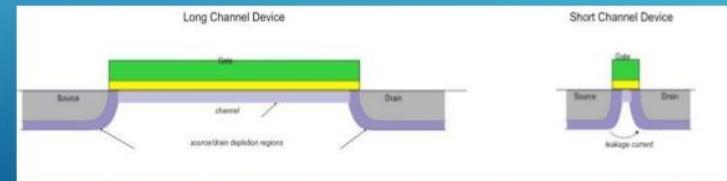


# Cons of Nanotransistor

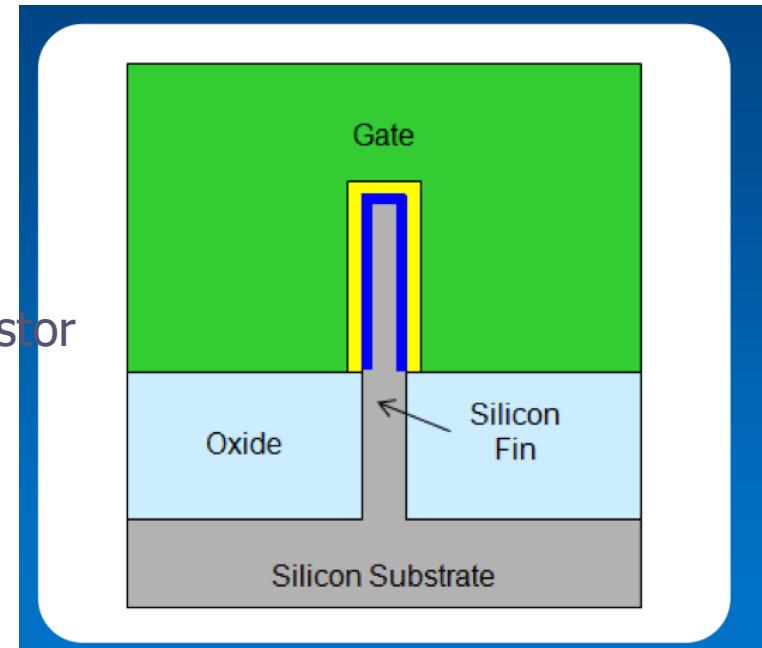
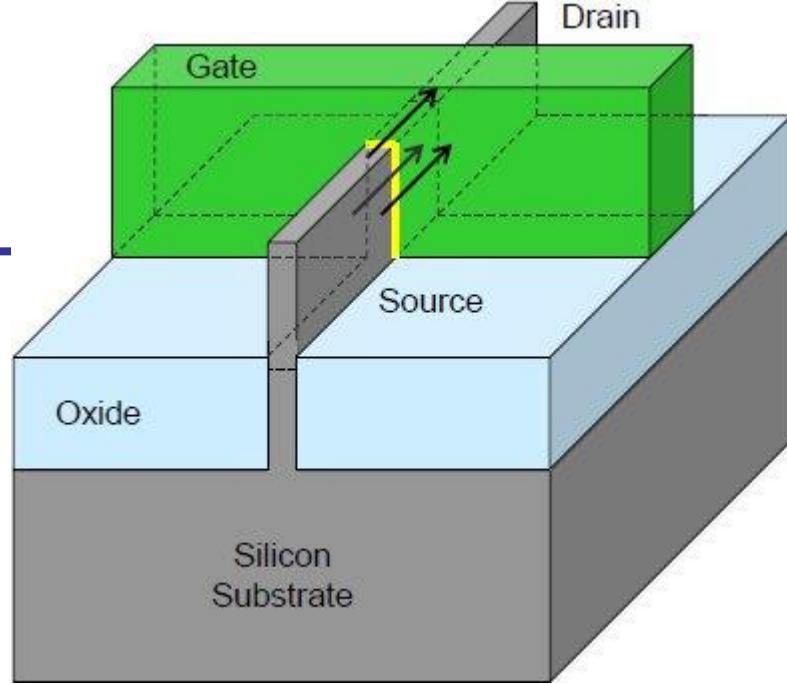
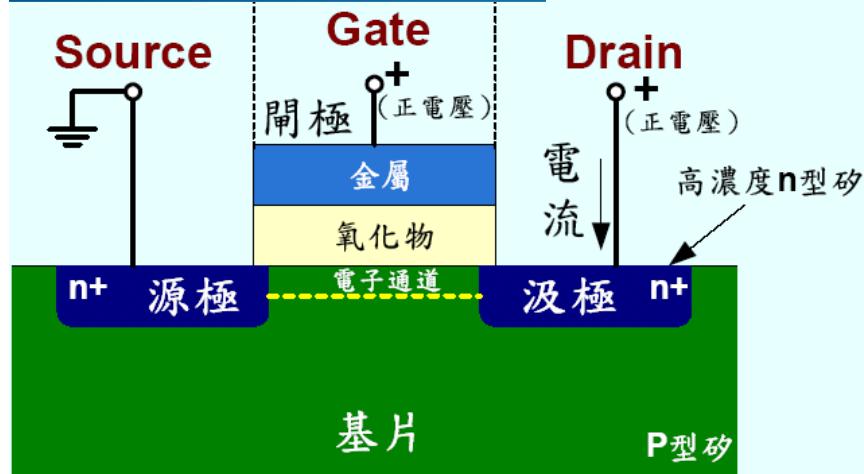
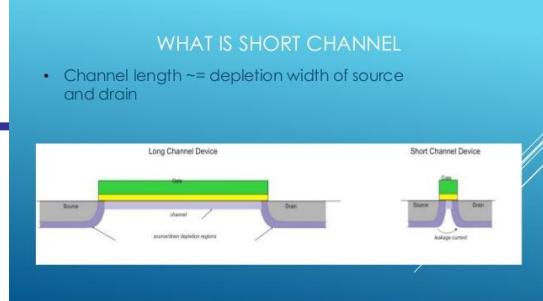
When the size of transistor decreases, the percentage of Leakage currents increases

## WHAT IS SHORT CHANNEL

- Channel length  $\sim$  depletion width of source and drain



# FinFET (10nm)



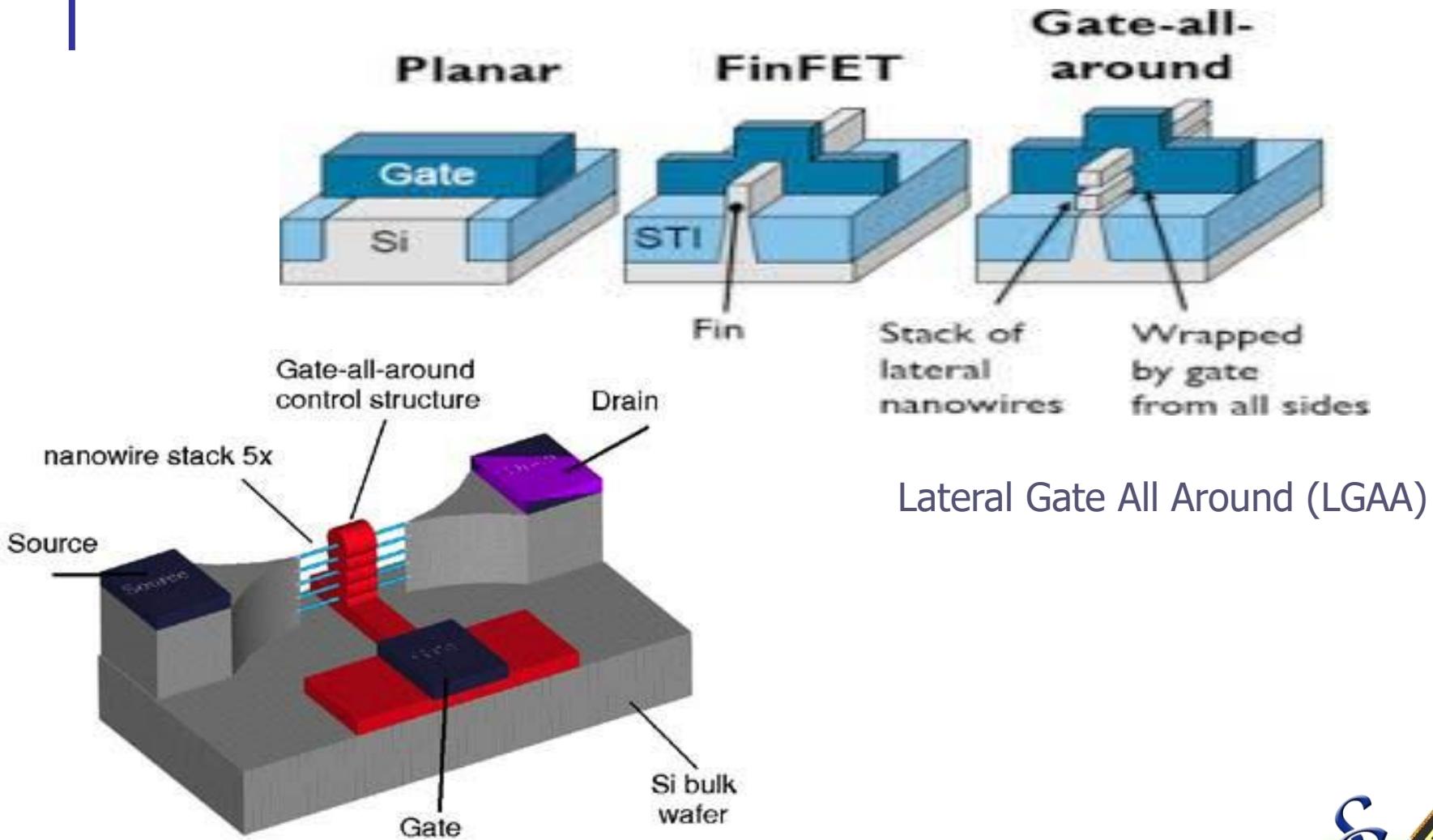
-Increases contact area by lifting the substrate above the planar surface of Transistor

1. Increase gate voltage control
2. Decrease leakage currents
3. Decrease dynamic power dissipation
4. Dynamic power is the power dissipated during transistor transition(0->1 or 1->0)

Left:traditional MOSFET, right:FinFET

# Gate\_All\_around FET(GAAFET 5nm)

## MOSFET/FINFET/GAAFET

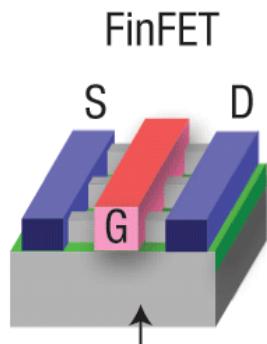


# Devices Evolution

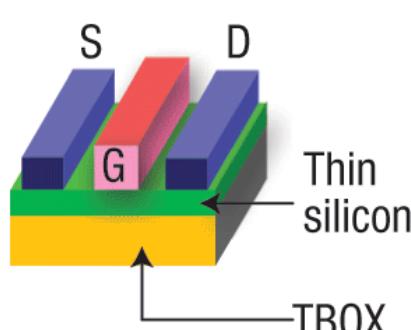
## MOSFET/FINFET/GAAFET/3DVLSI

2017

10 nm equiv.



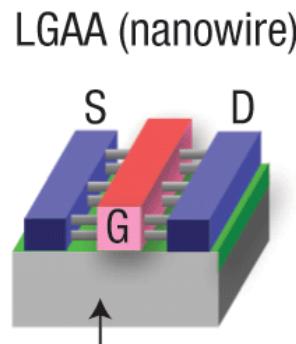
FinFET



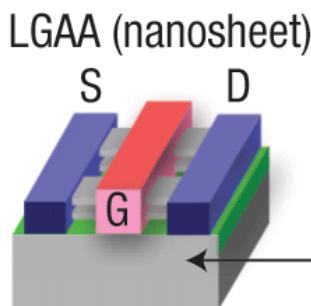
FDSOI

2019

7 nm equiv.



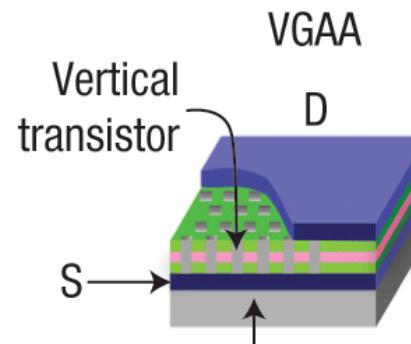
LGAA (nanowire)



LGAA (nanosheet)

2021

5 nm equiv.

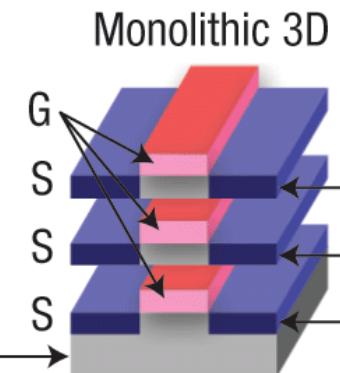


Vertical  
transistor

VGAA

2024–2033

3–1 nm equiv.



Monolithic 3D

Fully Depleted Silicon On Insulator (FD-SOI)

# FD-SOI

- Fully Depleted Silicon On Insulator (FD-SOI) (STMicroelectronics/Global Foundry)

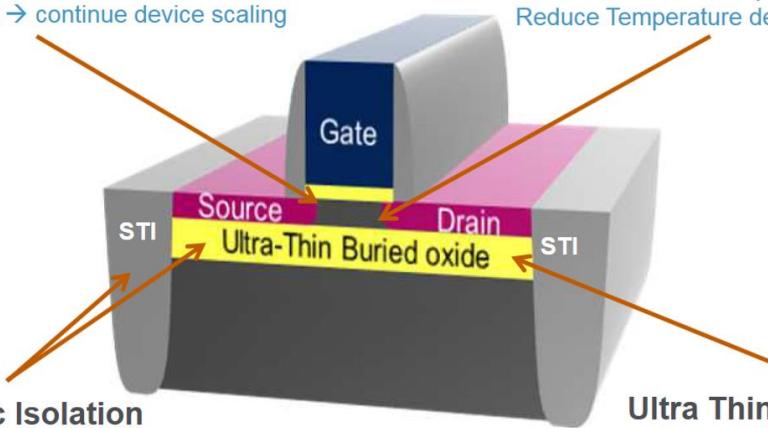


## Ultra-Thin BODY

Excellent Electrostatic Control of the channel  
Low SCE, DIBL  $\rightarrow$  Low  $V_t$  @ High  $V_D$   
Gate length shrink  $\rightarrow$  continue device scaling

## Undoped Channel & no Pocket

Less  $V_t$  variability & SRAM  $V_{min}$  improved  
Lower Power Consumption  
Reduce Temperature dependency & no RDF



## Total Dielectric Isolation

Lower SD capacitances & Lower SD Leakage  
Less Sensitive to Temperature  
Higher power efficiency

## Ultra Thin BOX

Body Biasing (BB)  $\rightarrow$  FBB & RBB  
Speed boost due to BB  
GP Implantation  $\rightarrow$   $V_t$  adjustment

# More Moore

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
<i>Logic industry "Node Range" Labeling (nm)</i>	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
<i>IDM-Foundry node labeling</i>	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
<i>Logic device structure options</i>	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA 3DVLSI	VGAA, LGAA 3DVLSI
<i>Logic device mainstream device</i>	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
<b>DEVICE STRUCTURES</b>							
<b>LOGIC DEVICE GROUND RULES</b>							
MPU/SoC Metal <sub>x</sub> ½ Pitch (nm) [1,2]	<b>18.0</b>	<b>14.0</b>	<b>12.0</b>	<b>10.5</b>	<b>7.0</b>	<b>7.0</b>	<b>7.0</b>
MPU/SoC Metal <sub>y</sub> 1 ½ Pitch (nm)	<b>18.0</b>	<b>14.0</b>	<b>12.0</b>	<b>10.5</b>	<b>7.0</b>	<b>7.0</b>	<b>7.0</b>
Contacted poly half pitch (nm)	<b>27.0</b>	<b>24.0</b>	<b>21.0</b>	<b>18.0</b>	<b>16.0</b>	<b>16.0</b>	<b>16.0</b>
<i>L<sub>g</sub> : Physical Gate Length for HP Logic (nm) [3]</i>	<b>20</b>	<b>18</b>	<b>16</b>	<b>14</b>	<b>12</b>	<b>12</b>	<b>12</b>
<i>L<sub>g</sub> : Physical Gate Length for LP Logic (nm)</i>	<b>22</b>	<b>20</b>	<b>18</b>	<b>16</b>	<b>14</b>	<b>14</b>	<b>14</b>
Channel overlap ratio - two-sided	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>
Spacer width (nm)	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>5</b>	<b>6</b>	<b>6</b>
Contact CD (nm) - finFET, LGAA	<b>18</b>	<b>16</b>	<b>14</b>	<b>12</b>	<b>10</b>		
Contact CD (nm) - VGAA						<b>12</b>	<b>12</b>
<i>Device architecture key ground rules</i>							
FinFET Fin Half-pitch (nm)	<b>16.0</b>	<b>14.0</b>					
FinFET Fin Width (nm)	<b>8.0</b>	<b>7.0</b>					
FinFET Fin Height (nm)	<b>45</b>	<b>50</b>					
Footprint drive efficiency - finFET	<b>3.06</b>	<b>3.82</b>					
Lateral GAA lateral half-pitch (nm)			<b>12.0</b>	<b>10.5</b>	<b>9.0</b>		
Lateral GAA vertical half-pitch (nm)			<b>8.0</b>	<b>8.0</b>	<b>8.0</b>		
Lateral GAA (nanosheet) thickness (nm)			<b>5.0</b>	<b>5.0</b>	<b>5.0</b>		
Lateral GAA (nanosheet) minimum width (nm)			<b>7.0</b>	<b>7.0</b>	<b>6.0</b>		
Number of vertically stacked nanosheets			<b>3</b>	<b>4</b>	<b>5</b>		
Device height (nm)			<b>47</b>	<b>63</b>	<b>79</b>		
Footprint drive efficiency - lateral GAA			<b>3.00</b>	<b>4.57</b>	<b>6.11</b>		
Vertical GAA lateral half-pitch (nm)						<b>7.0</b>	<b>7.0</b>
Vertical GAA width (nm)						<b>6.0</b>	<b>6.0</b>
Contact-gate enclosure (nm)						<b>2.0</b>	<b>2.0</b>
Footprint drive efficiency - vertical GAA						<b>1.7</b>	<b>1.7</b>
Device effective width (nm)	<b>98.0</b>	<b>107.0</b>	<b>72.0</b>	<b>96.0</b>	<b>110.0</b>	<b>24.0</b>	<b>24.0</b>
Device lateral half-pitch (nm)	<b>16.0</b>	<b>14.0</b>	<b>12.0</b>	<b>10.5</b>	<b>9.0</b>	<b>7.0</b>	<b>7.0</b>
Device height (nm)	<b>45.0</b>	<b>50.0</b>	<b>47.0</b>	<b>63.0</b>	<b>79.0</b>	<b>24.0</b>	<b>24.0</b>
Minimum device width (fin, nanosheet) or diameter (nm)	<b>8.0</b>	<b>7.0</b>	<b>7.0</b>	<b>7.0</b>	<b>6.0</b>	<b>6.0</b>	<b>6.0</b>

<https://www.hpcwire.com/2019/07/24/ieee-releases-expansive-2018-roadmap-for-devices-and-systems/>



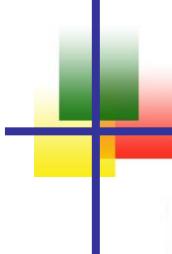
# Semiconductor Process Evolution

## IRDS-International Roadmap for Devices and Systems

Table ES2     Overall Roadmap Technology Characteristics

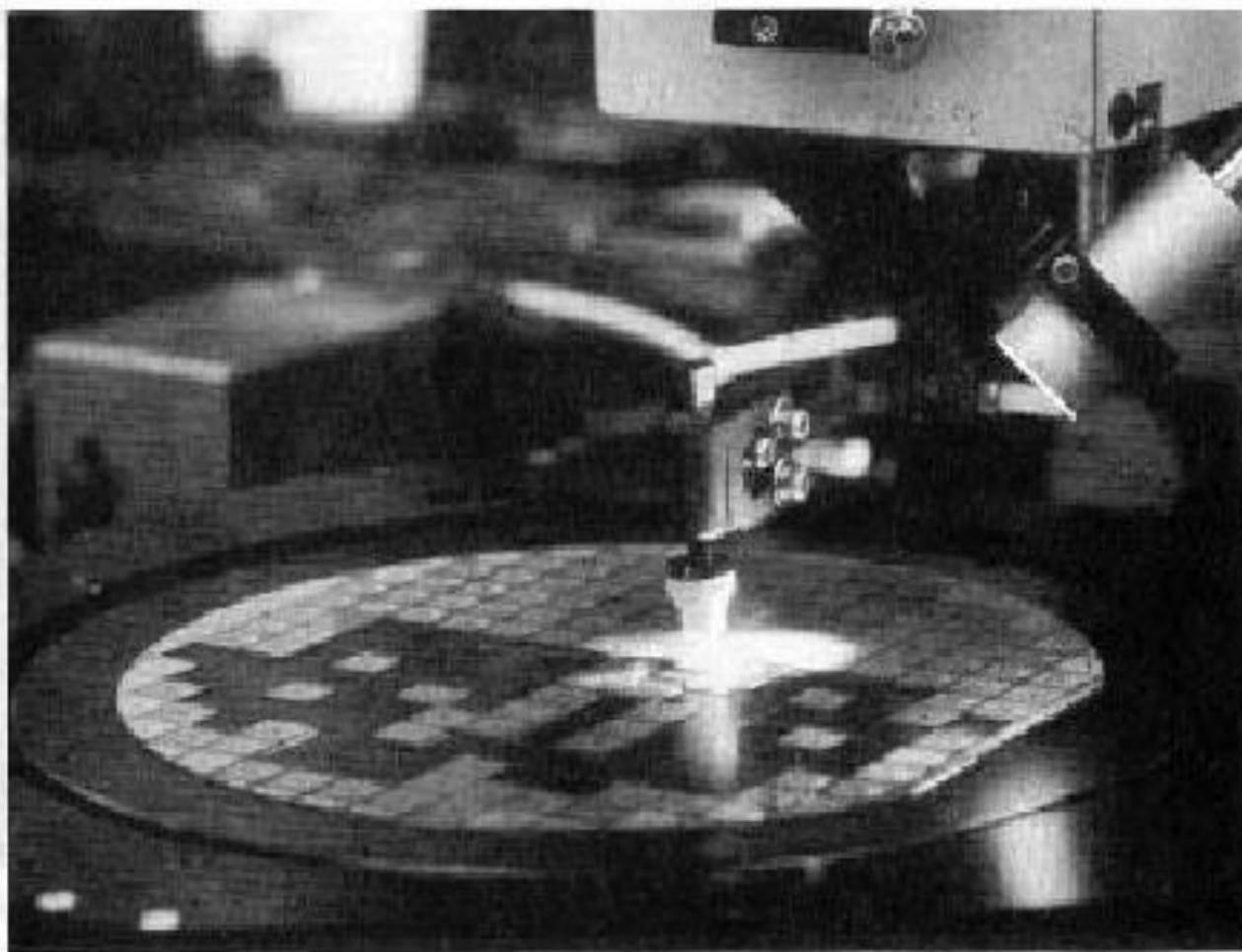
2017 IRDS Executive Summary - ORTC							
YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
Logic device technology naming	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14 T2	P32M14 T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA, 3DVLSI	VGAA, LGAA, 3DVLSI
LOGIC CELL AND FUNCTIONAL FABRIC TARGETS							
Average cell width scaling factor	1.00	0.90	0.90	0.90	0.90	0.90	0.90
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx $\frac{1}{2}$ Pitch (nm) [1,2]	18	14	12	10.5	7.0	7.0	7.0
Physical gate length for HP Logic (nm) [3]	20	18	16	14	12	12	12
Lateral GAA (nanosheet) Minimum Width (nm)			7.0	7.0	6.0		
Minimum Device Width (fin, nanosheet) or Diameter (nm)	8	7.0	7.0	7.0	6.0	6.0	6.0
LOGIC DEVICE Electrical							
Vdd (V)	0.75	0.70	0.65	0.65	0.65	0.60	0.55
DRAM TECHNOLOGY							
DRAM $\frac{1}{2}$ Pitch (nm) [1]	18	17.5	17	14	11	8.4	7.7
DRAM cell size factor: $aF^2$ [11]	6	6	4	4	4	4	4
DRAM bits/1chip target	8G	8G	16G	16G	32G	32G	32G
NAND Flash							
Flash $\frac{1}{2}$ Pitch (nm) (un-contacted Poly)(F) (2D) [1]	15.0	15.0	15.0	15.0	15.0	15.0	15.0
Flash Product Highest Density (independent of 2D or 3D)	512G	1T	1T	1.5T	3T	4T	4T+
Flash 3D Maximum Number of Memory Layers [6]	64	96	128	192	384	512	>512





# Sawing a Wafer into Chips

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# Snapshot



## ■ 300mm wafer and Pentium 4™

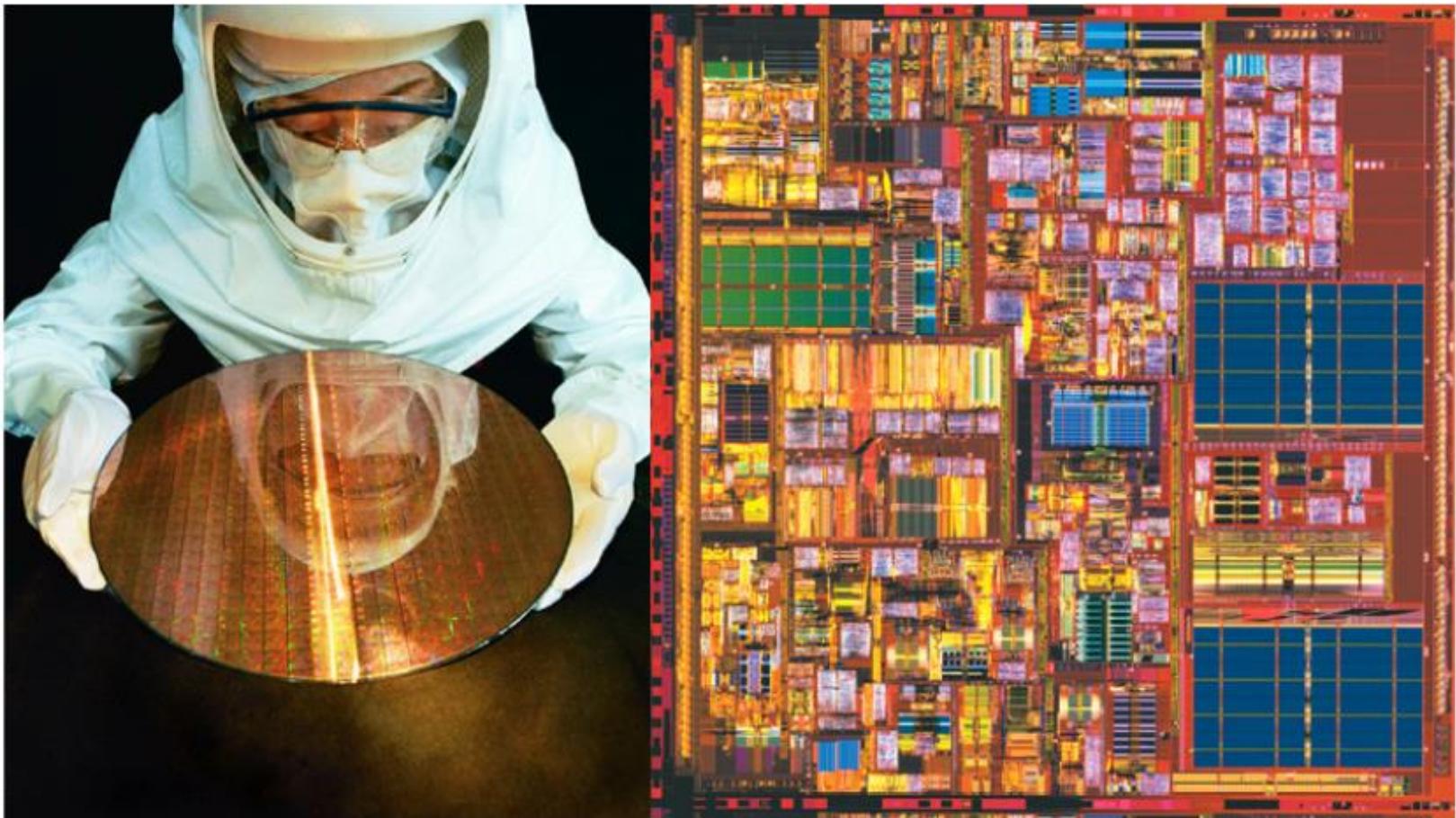
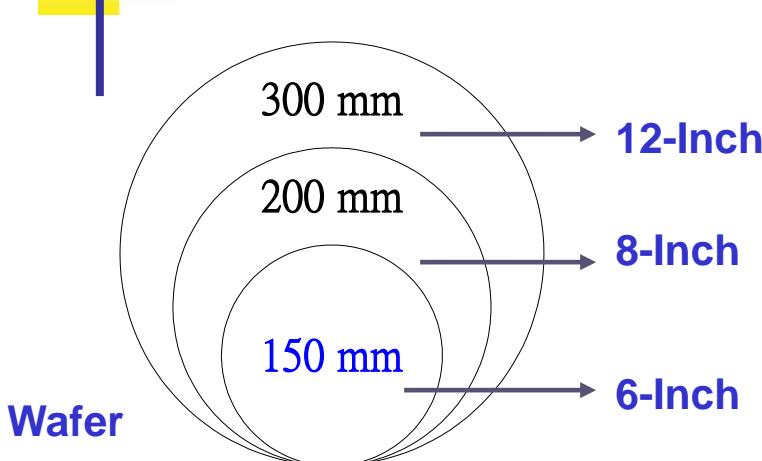


Photo courtesy of Intel

# Feature Technology and Size

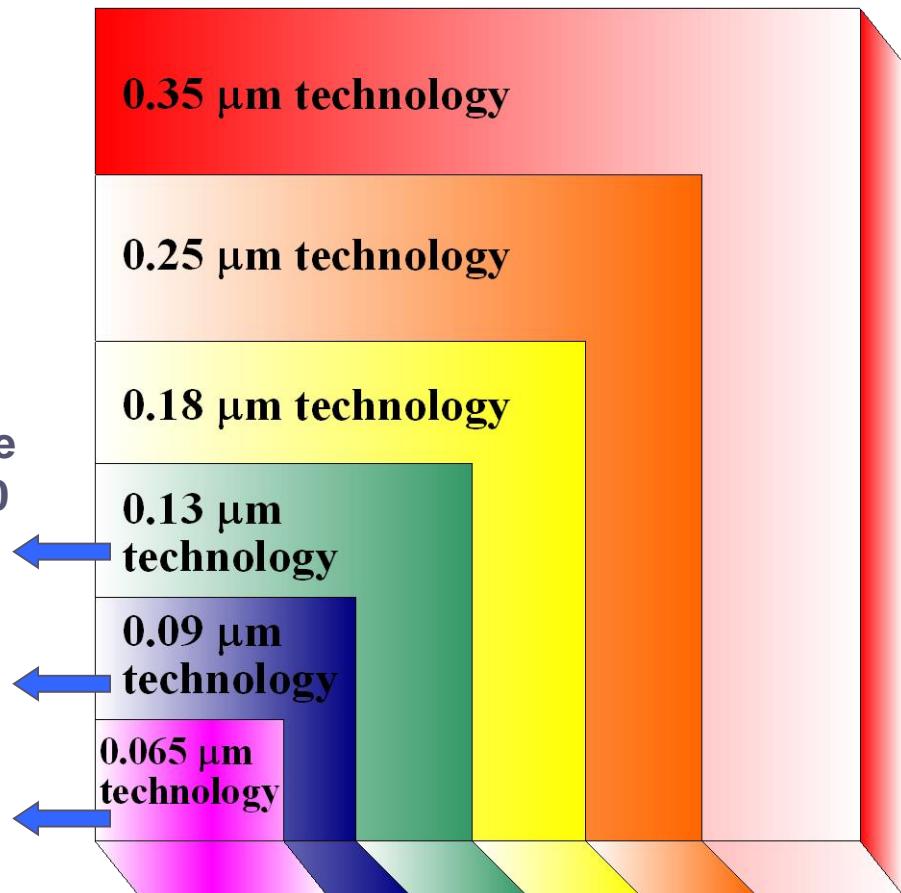


When compared to the **0.18-micron** process, the new **0.13-micron** process results in less than 60 percent the die size and nearly 70 percent improvement in performance

The **90-nm** process is manufactured on 300mm wafers

NEC devices low-k film for second-generation  
**65-nm** process

Most recent technology  
45nm/22nm/16nm/10nm/7nm/5nm



# Top Semiconductor Fab

- Top ten semiconductor fab. Revenue comparison at 2019

Figure: Top Ten Foundries in 1Q19, Ranked

(Million USD)

Rank	Company Name	1Q18 Revenue	1Q19 Revenue (E)	1Q19 Market Share (%)	1Q19 Revenue Growth YoY (%)
1	TSMC	8,547	7,028	48.1%	-17.8%
2	Samsung	3,253	2,785	19.1%	-14.4%
3	GlobalFoundries	1,513	1,234	8.4%	-18.4%
4	UMC	1,292	1,058	7.2%	-18.1%
5	SMIC	831	654	4.5%	-21.3%
6	Tower Semiconductor	313	310	2.1%	-0.9%
7	Powerchip Semiconductor	341	251	1.7%	-26.4%
8	VIS	221	225	1.5%	1.6%
9	Hua Hong Semiconductor	210	220	1.5%	4.7%
10	Dongbu Hi-Tek	131	132	0.9%	1.1%

Note:

1. Samsung's revenue include those from its System LSI and Foundry Business
2. GlobalFoundries' revenue include that of its IBM Business
3. Only foundry revenue was included for Powerchip Semiconductor

Source: TrendForce, Mar. 2019

# Top Semiconductor Fab

## Top ten semiconductor fab. Revenue comparison at 2021

Table 1: Ranking of Global Top 10 Foundries by Revenue, 1Q21 (Unit: Million USD)

Ranking	Company	Revenue			Market Share	
		1Q21	4Q20	QoQ	1Q21	4Q20
1	TSMC	12,902	12,696	2%	55%	54%
2	Samsung	4,108	4,177	-2%	17%	18%
3	UMC	1,677	1,591	5%	7%	7%
4	GlobalFoundries	1,301	1,552	-16%	5%	7%
5	SMIC	1,104	981	12%	5%	4%
6	PSMC	388	340	14%	2%	1%
7	Tower	347	345	1%	1%	1%
8	VIS	327	306	7%	1%	1%
9	HHGrace	305	280	9%	1%	1%
10	HLMC	295	300	-2%	1%	1%
Top 10 Total		22,753	22,569	1%	96%	96%

Notes:

1. 4Q20 USD\$1:KRW\$1,118; USD\$1:TWD\$28.5

2. 1Q21 USD\$1:KRW\$1,115; USD\$1:TWD\$28.1

3. Samsung's revenue includes the revenues from its System LSI unit and foundry business.

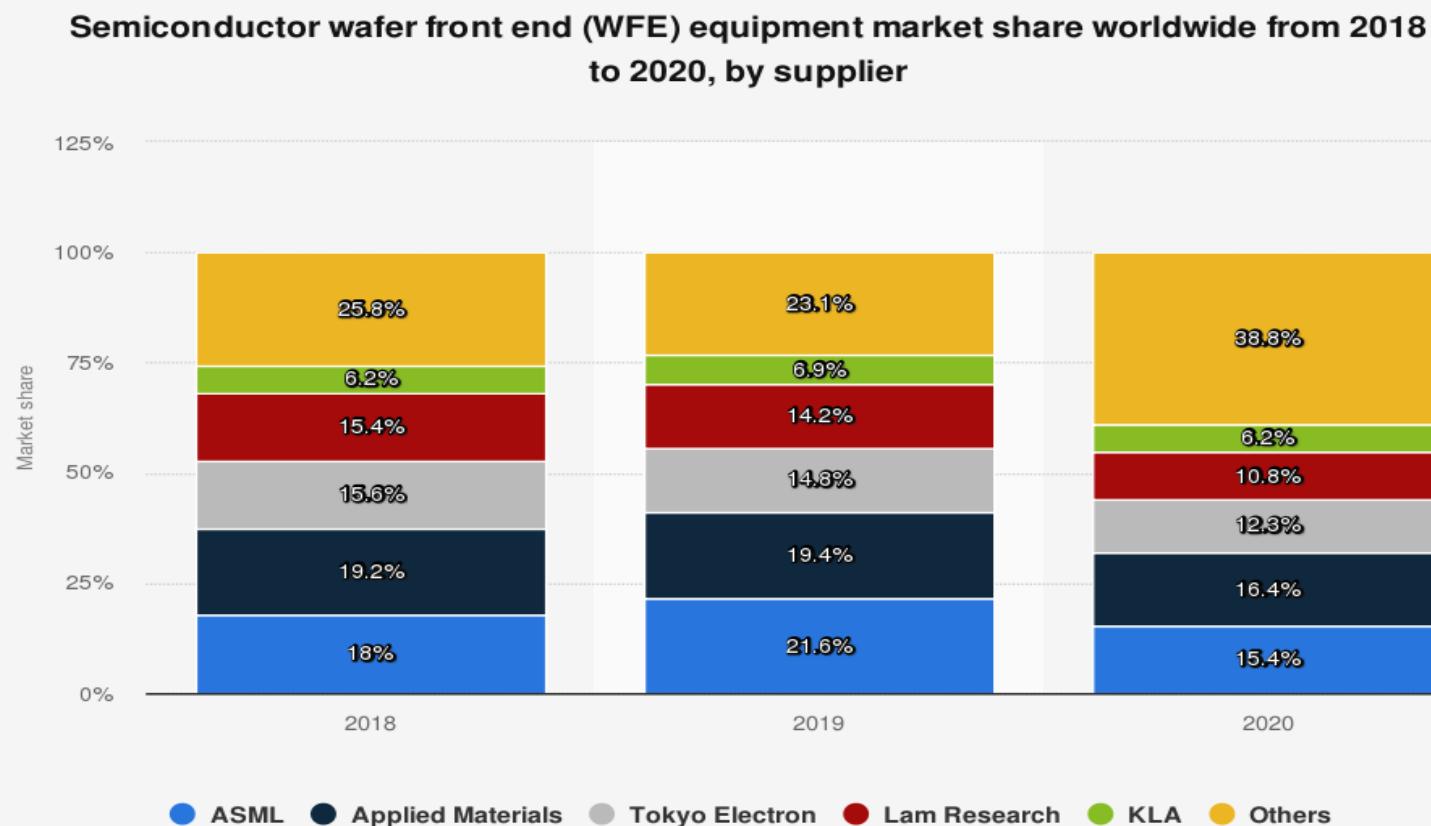
4. PSMC's revenue derives from its foundry services only.

5. HLMC's revenue include the revenues from Shanghai Huali Microelectronics Corporation and Shanghai Huali Integrated Circuit Corporation.

Source: TrendForce, May 2021

# Top Semiconductor Equipment

## Top ten semiconductor Equipment comparisons at 2020



### Sources

The Information Network; Seeking Alpha; SemiWiki  
© Statista 2021

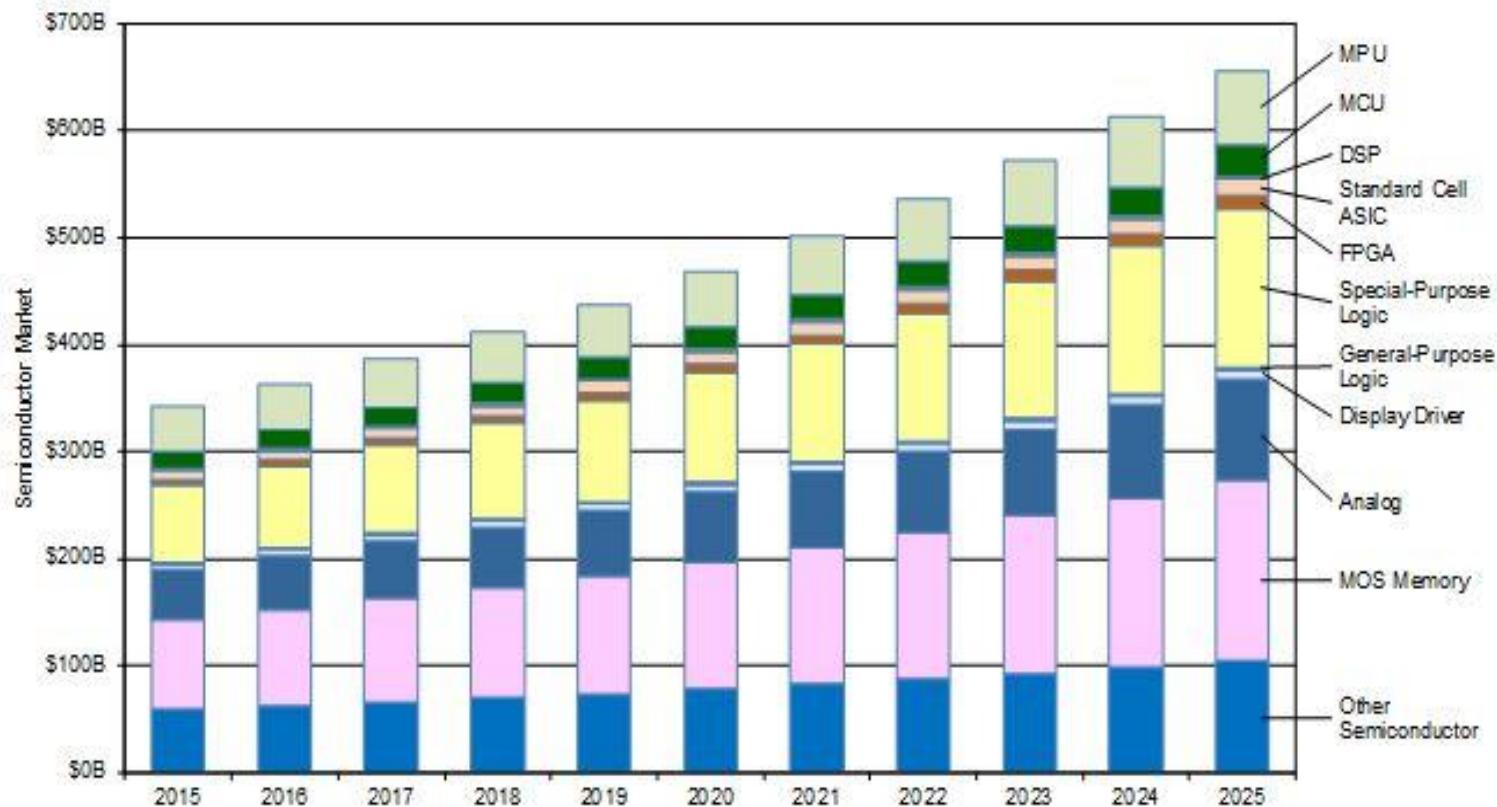
### Additional Information:

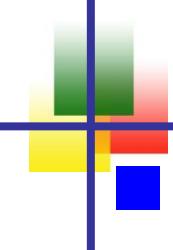
Worldwide; The Information Network; 2018 to 2020



# Semiconductor Industries

- Global semiconductor industry market outlook
  - Special purpose logic such as IoT
  - IoT applications include controllers, wireless connectivity, and embedded nonvolatile memory.





# Wide Bandgap Semiconductor

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## ■ SiC and GaN

- Bandgap energy for Si and GaAs is 1.12ev and 1.43 ev
  - Bandgap energy for SiC and GaN is 3.2ev and 3.4 ev
  - It is more difficult for SiC and GaN to change from insulator to conductor under high temperature and pressure compared with Si and GaAS
  - High performance and stability under high frequency and temperature
  - Applications
    - Electrical car charging/ Base stations
    - High voltage such 400V or 800V
- <https://technews.tw/2021/09/22/wide-band-gap-gan-sic/>

# Wide Bandgap Semiconductor

■ SiC

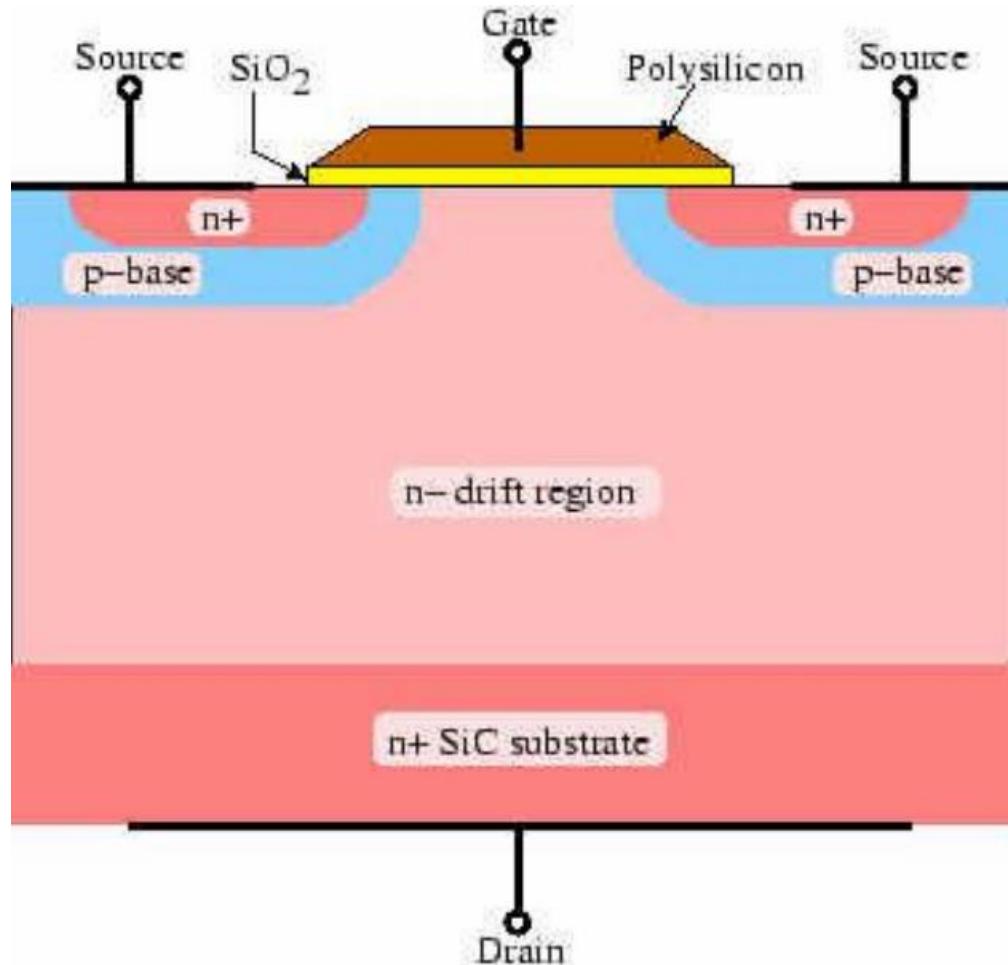
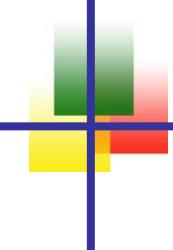


Figure 1: Vertical DMOS SiC MOSFET



# Reference

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