Introduction to System-on-Chip and its Applications

Computer System-on-Chip

Ching Te Chiu

Outline

- **Background**
- **Computer**
  - ➔ Definition
  - ➔ Functions
- **Architecture**
  - ➔ Basic components in computer
- **CISC vs RISC**
- **CPU**
  - ➔ Intel 486
  - ➔ Intel Pentium
  - ➔ Intel Core i7
- **Intel Microarchitecture Evolution**

Introduction

- **Computer**
  - ➔ Computer is also called “electronic calculator”. It was originally used to do calculations or statistics. However, after years of improvements, computer can not only accept user input, but also calculate or analyze according to logical judgment, and finally memorize the result or output according to a certain format.
  - ➔ Functions:
    - ➲ Input/Output Data
    - ➲ Data Processing
    - ➲ Data Storage

Introduction

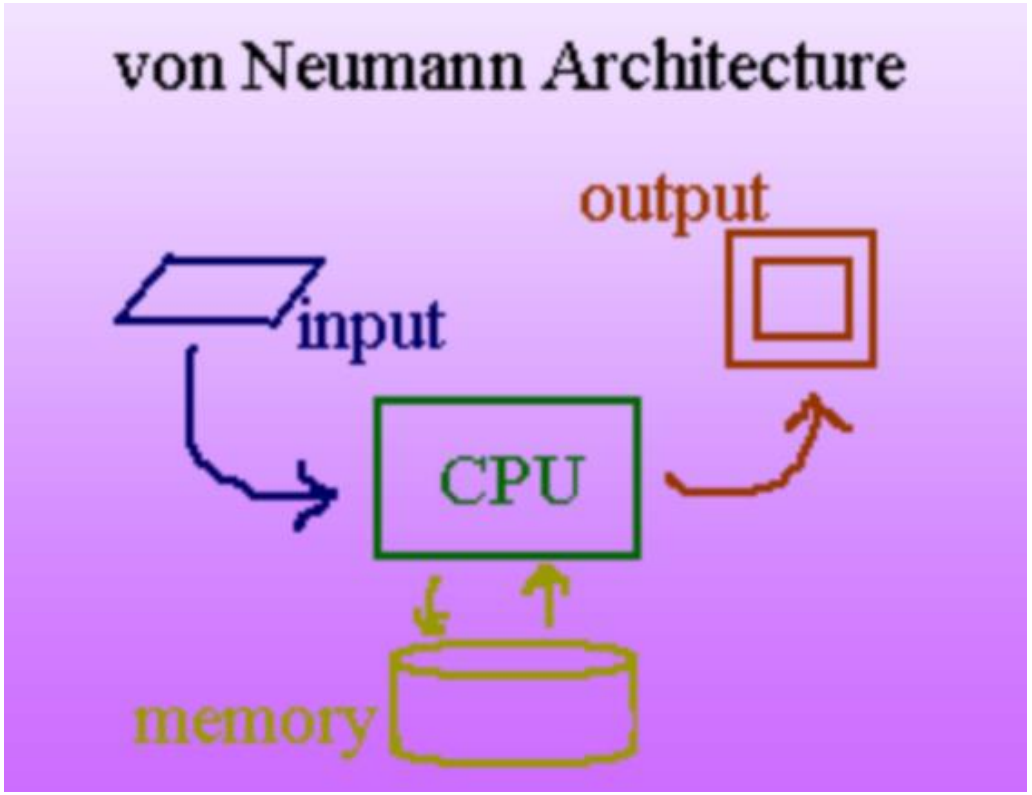
- **Computer**
  - ➔ Computer is composed of hardware and software.
    - ➲ Hardware : Every components which you can see in computer
      - ⇨ CPU、Memory、Keyboard、Screen、Printer and so on.
    - ➲ Software : Software is an umbrella term for a variety of program
      - ⇨ Application software : Inventory system、payroll system
      - ⇨ System software : Operating System、compiler、loader、link and so on.
- **Applications**
  - ➔ Scientific calculations
  - ➔ Database Systems

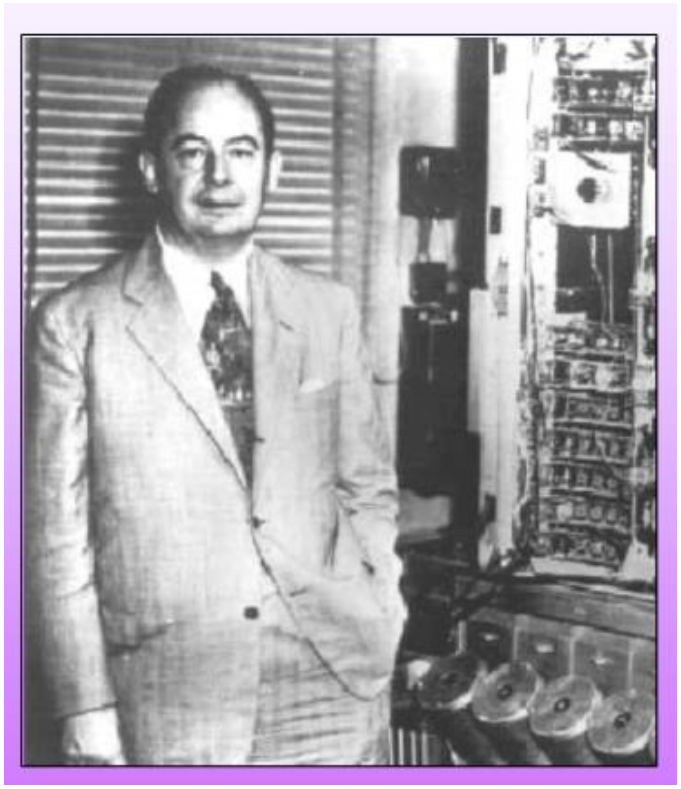
Computer category

- **Super Computer**
  - ➔ The most powerful, but also the most expensive. Execute tera (10^{12}) instructions per second.
  - ➔ Mainstream applications: stock analysis, car design, movie special effects.
  - ➔ Specific applications: Worldwide weather forecasting and weapon development.
- **Mainframe**
  - ➔ A few giga (10^{9}) instructions are processed every second with hundreds of millions of characters.
  - ➔ Mainstream applications: Airlines, government financial audit units, aircraft design companies.
- **Microcomputer**
  - ➔ Personal Computer (PC)、notebook computer
- **Embedded Computer**
  - ➔ Cellphone, personal digital assistant (PDA), and information appliance

范紐曼(Von Neumann) Architecture

- The person who first proposed the concept of memory.





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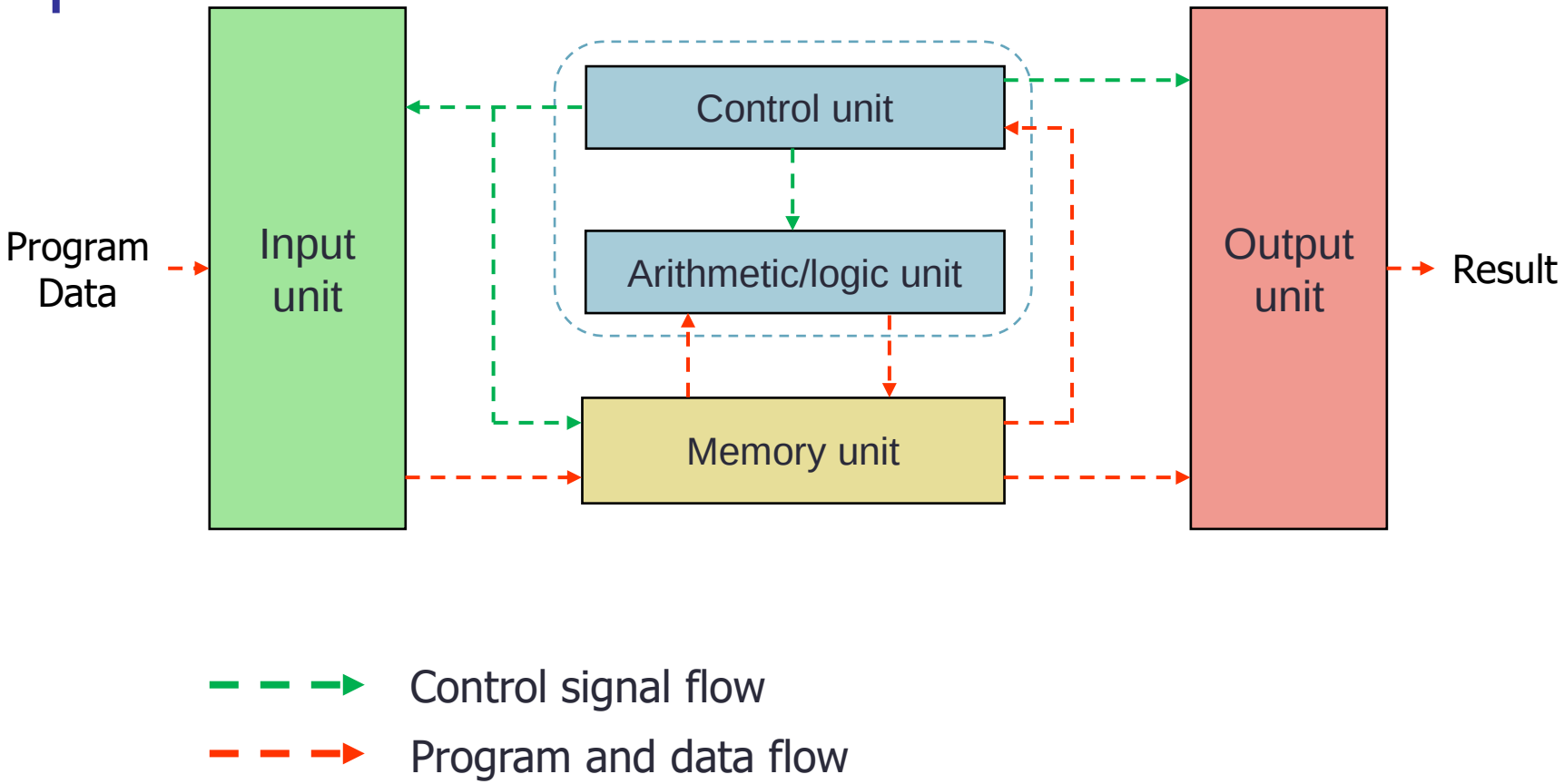
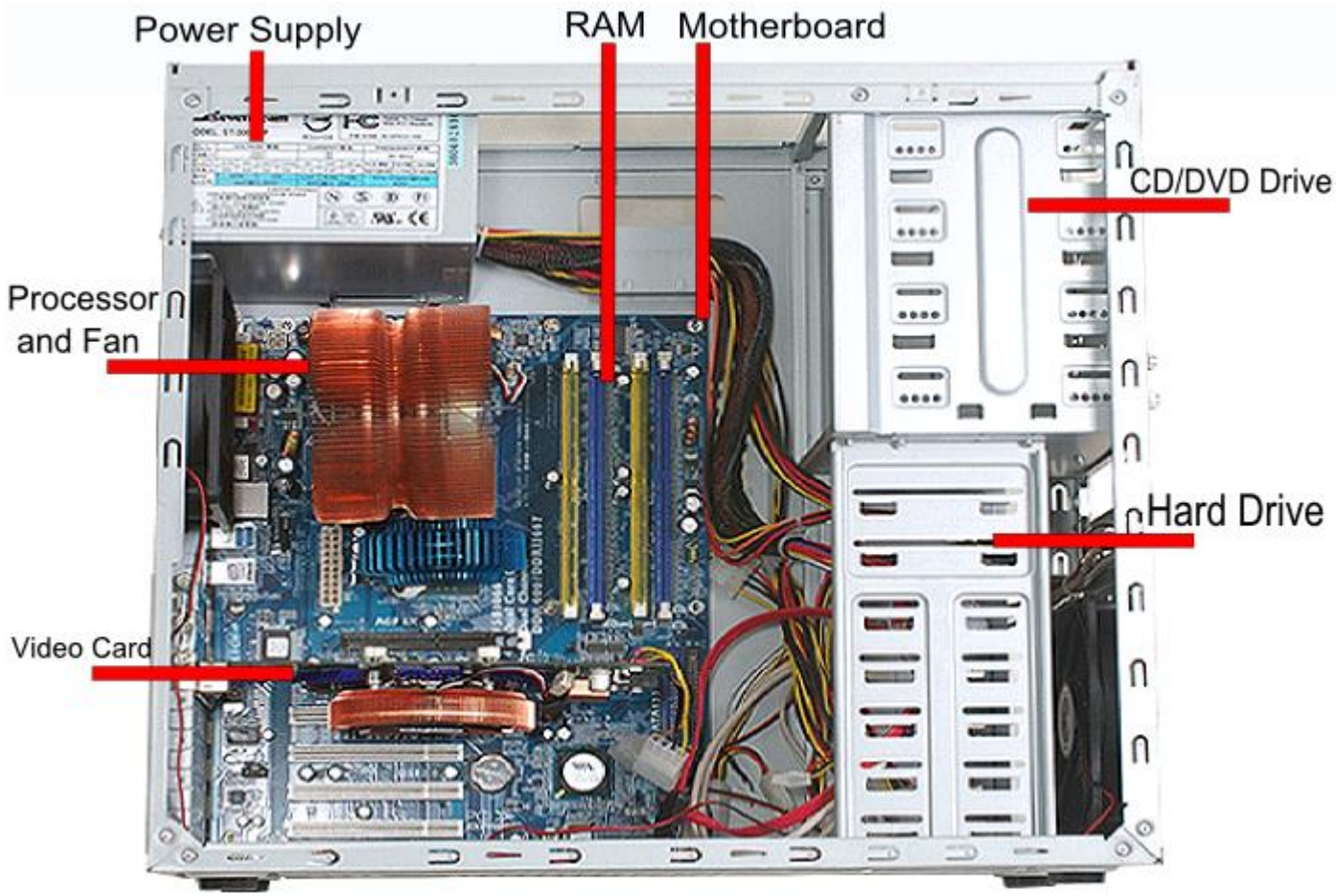
Computer Architecture

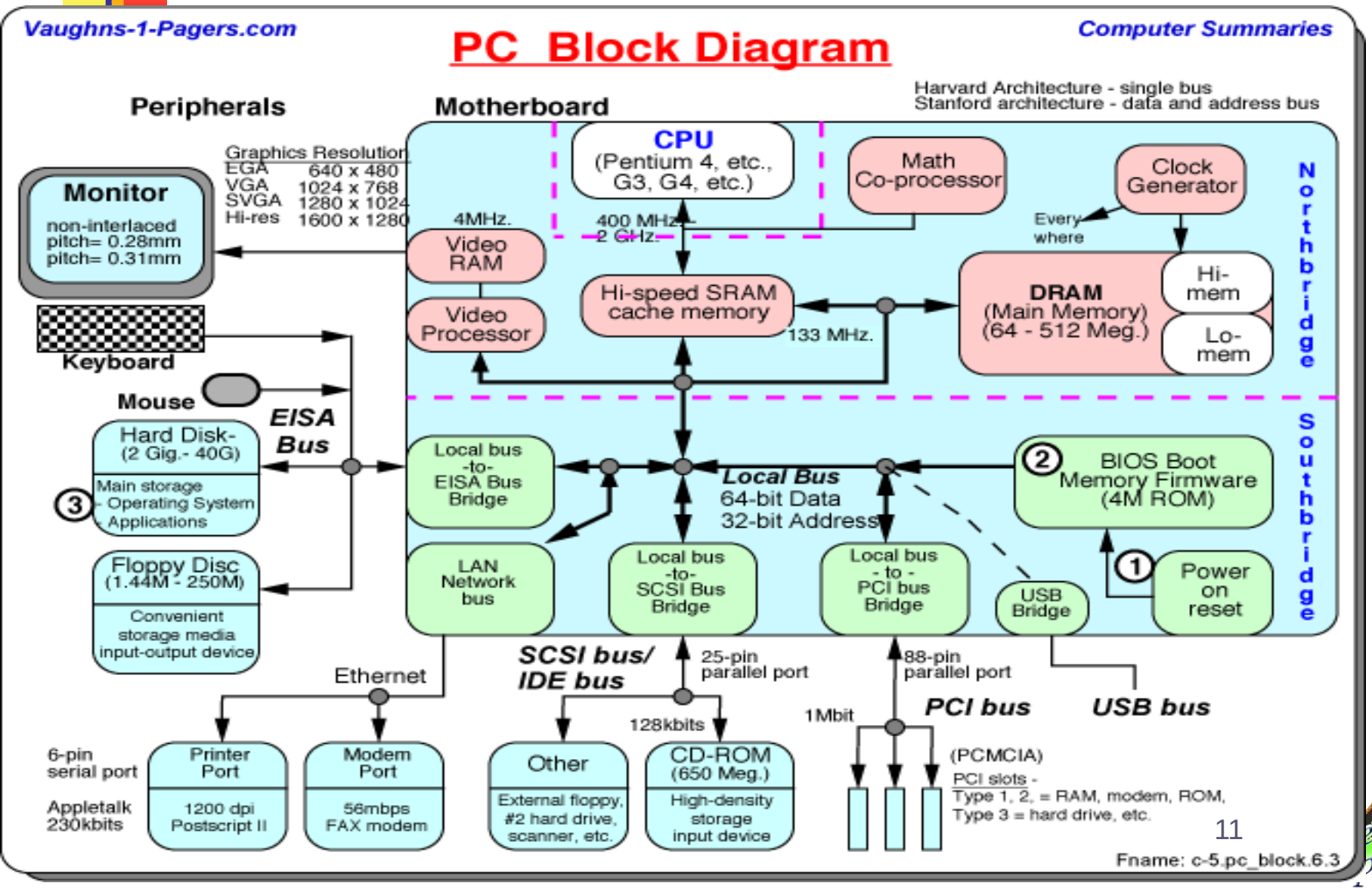


Overall System Architecture of Computer

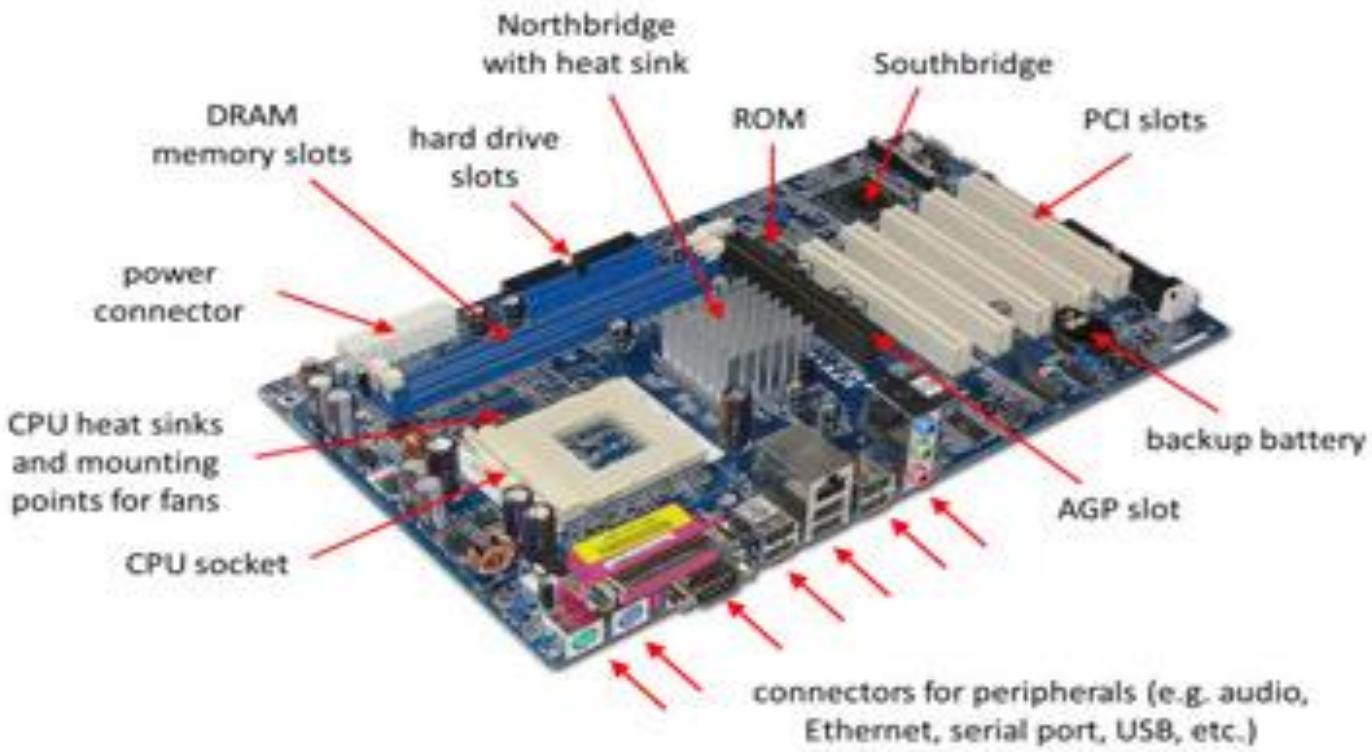
Overall System Architecture of Computer



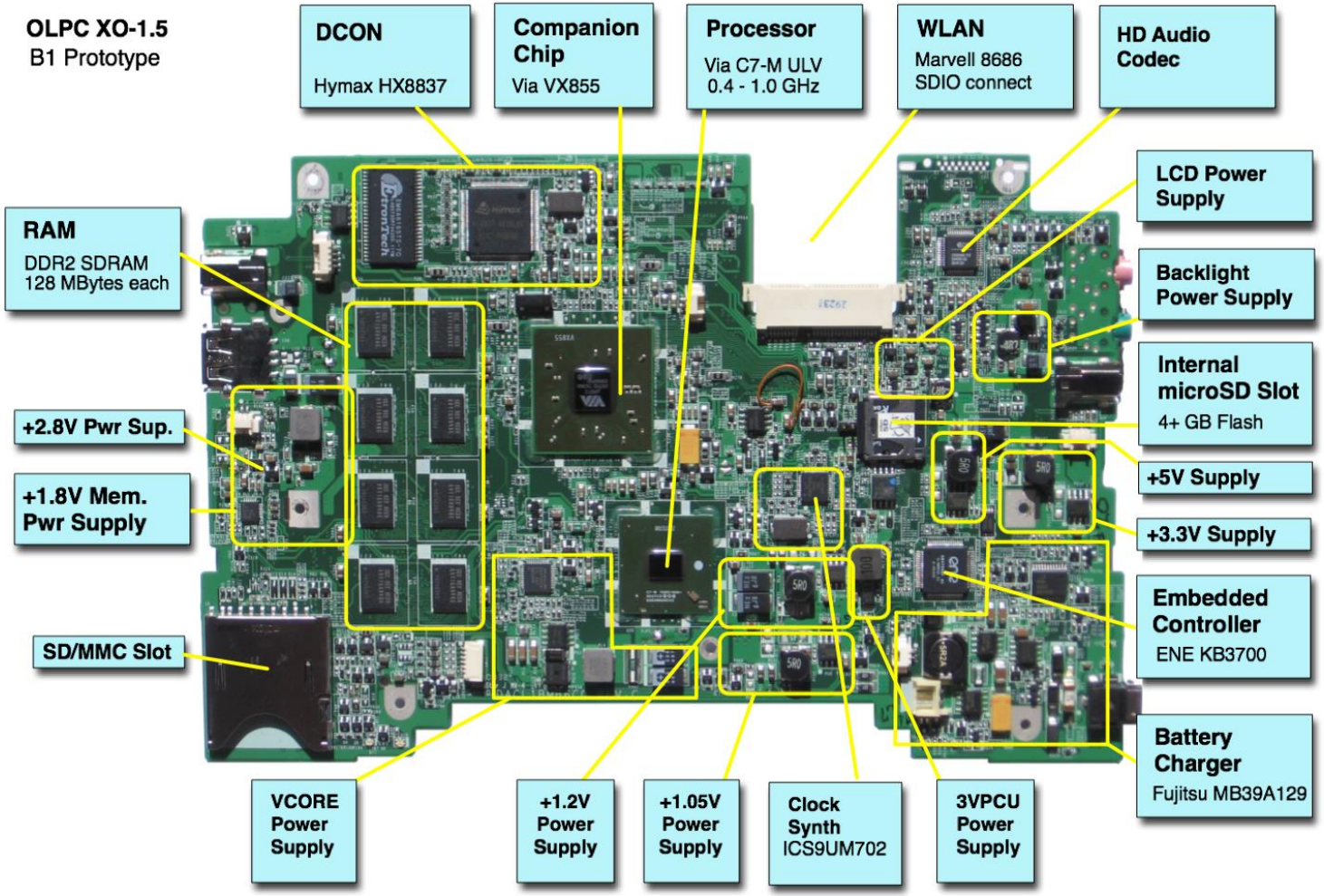
PC Motherboard Block Diagram



Motherboard of PC



Notebook Motherboard



Basic PC Components

- **CPU (Central Processing Unit)**
  - ➔ It reads the list of instructions and runs (*executes*) each one in order.
  - ➔ Clock rate around gigahertz (GHz)。
- **Random Access Memory, RAM**
  - ➔ DDR4 SDRAM is the mainstream of current memory
  - ➔ (DDR5 debut 2021) DDR5-6000 (2 x 16GB)
  - ➔ Generally equipped with 512MB or even 8GB.
- **Hard Disk Drive, HDD (250GB-20TB)**
  - ➔ Capacity: The unit capacity of HDD has been increased to several tera bytes.
  - ➔ Rotation speed: Refers to the speed of the internal motor of the hard disk, the unit is RPM (rotation per minute). The faster the speed, the faster the hard disk read /write speed.
  - ➔ 7200 RPM HDD will deliver a read/write speed of 80-160MB/s.
- **Solid-state disk（SSD)(120GB-30TB)**
  - ➔ SSD-512GB(2018), 1TB(2019), Seagate SSD 26TB (2022)
  - ➔ Typical SSD will deliver read/write speed of between 200 MB/s to 550 MB/s.

Basic PC Components

- **High-speed USB (Universal Serial Bus) port**
  - ➔ USB 1.0 can reach up to 12M bps,
  - ➔ USB 2.0 can reach 480M bps,
  - ➔ USB 3.0 up to 5Gbps
  - ➔ It has the advantages of high transmission rate, support for hot plugging and plug and play.
- **Mother Board**
  - ➔ Input/output devices, CPU, memory, storage devices, etc.

Features / Version	USB 3.2 Gen 1	USB 3.2 Gen 2	USB 3.2 Gen 2x2	USB 4.0
Speed	Super Speed	Super Speed+	Super Speed+	Super Speed+
Bandwidth	5 Gbps	10 Gbps	20 Gbps	40 Gbps
Encoding	8b/10b	128b/132b	128b/132b	128b/132b
Release	2009	2014	2017	2019

Central Processing Unit (CPU)

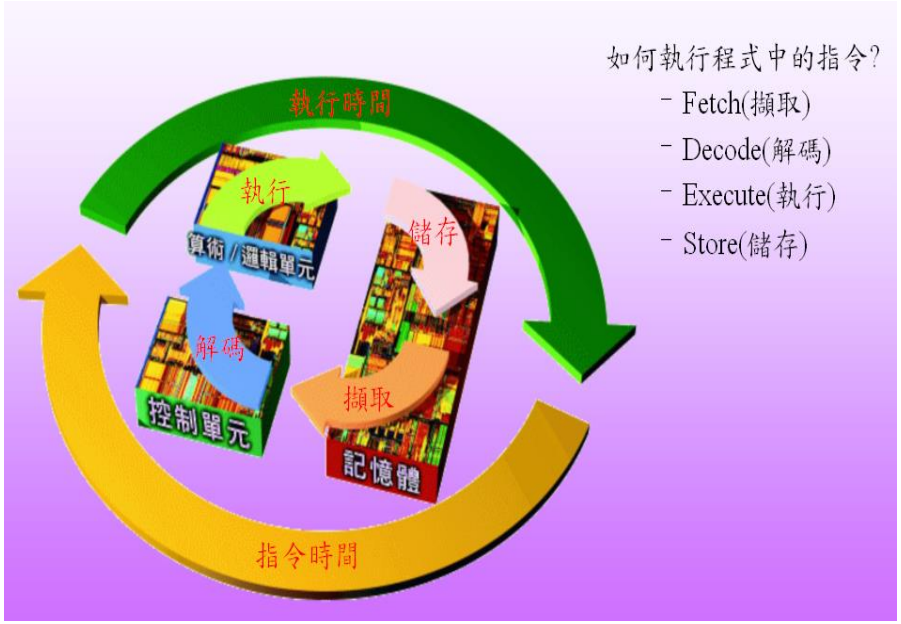
- **Brain of Computer**
- **General Processor**
  - ➔ Carry out the instructions of a computer program
  - ➔ Performs the basic arithmetical and logical functions
  - ➔ Input/output operations of a computer system
  - ➔ Complicated instructions such as editing an image file or creating 3D animation

Basic unit in CPU

- **Arithmetic logic unit, ALU**
  - ➔ Add, subtract, multiply, divide and compare, select, judge and other operations.
- **Control unit, CU**
  - ➔ Decoding function of instructions in the translation program
  - ➔ Coordinate and control all components to execute the instructions to make the computer automatically process data.
- **Register**
  - ➔ Temporarily store data, such as accumulators used to store calculations. Its function is similar to memory.
- **Cache unit**
  - ➔ Store the program or data currently being processed and the capacity is in MB.

Machine Cycle in CPU

- **Execute an instruction includes four steps**
  - ➔ Fetch
  - ➔ Decode
  - ➔ Execute
  - ➔ Store



Early processors

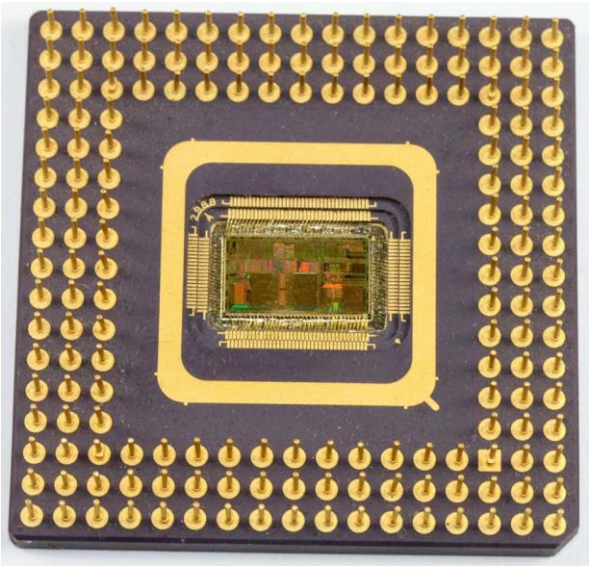
- Intel 4004
- 4-bit CPU
- Clock 0.74 MHZ
- US $1425.00 at launch
- 2300 transistors
- Around 1971

Intel 8088

- First Time IBM used CPU from outside
- 29,000 transistors
- 8 Bit CPU
- 5-10 MHZ clock speed

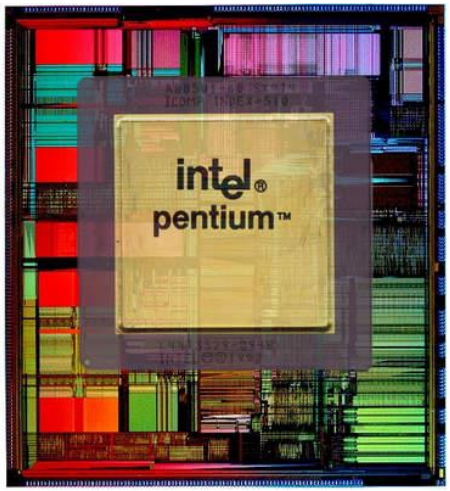
Intel 486

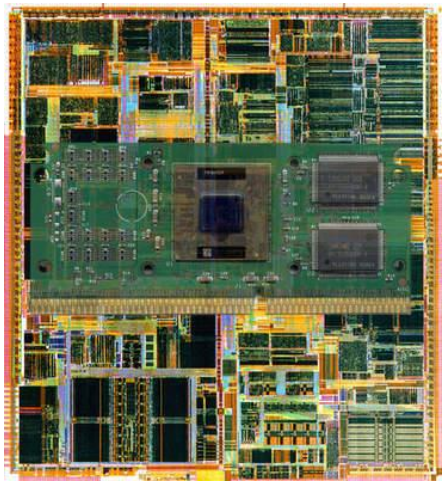
- First CPU to support GUI, not just command line inputs.
- First CPU with a FPU (Floating Point Unit)
- 16-100MHZ clock rate
- 1.2 Million transistors

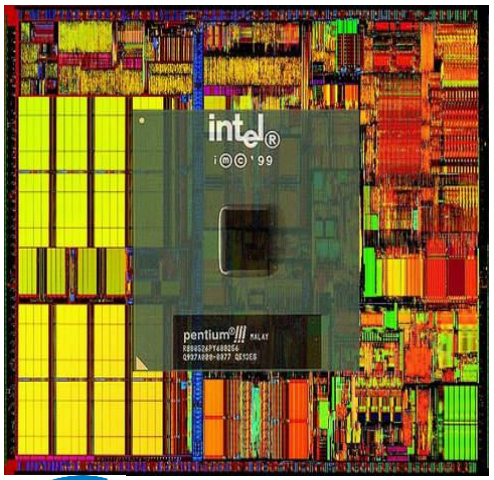


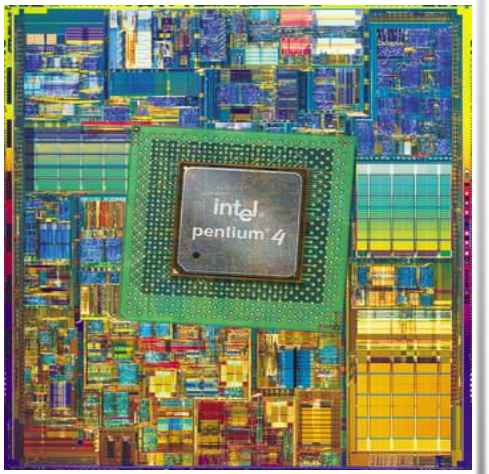
Pentium Series

- Consolidation of Intel's brand image
- Hyperthreading (Execute two treads in parallel in one CPU)
- NetBurst (Hyper pipelined/trace cache technology to boost clock rate)
- 32 Bit CPU









Intel Microprocessor

微處理器	出廠年	操作頻率	電晶體數目	暫存器	資料匯流排寬度	位址空間	快取記憶器
8086	1978	8 MHz	29 k	16 GP	16	1 MB	
286	1982	12.5 MHz	134 k	16 GP	16	16 MB	
386 DX	1985	20 MHz	275 k	32 GP	32	4 GB	
486 DX	1989	25 MHz	1.2 M	32 GP, 80 FPU	32	4 GB	L1:8 kB
Pentium	1993	60 MHz	3.1 M	32 GP, 80 FPU	64	4 GB	L1:16 kB
Pentium Pro	1995	200 MHz	5.5 M	32 GP, 80 FPU	64	64 GB	L1: 16 kB L2: 256/512 kB
Pentium II	1997	266 MHz	7 M	32 GP, 80 FPU, 64 MMX	64	64 GB	L1: 32 kB L2: 256/512 kB
Pentium III	1999	500 MHz	8.2 M	32 GP, 80 FPU 64 MMX, 128 XMM	64	64 GB	L1: 32 kB L2: 512 kB

Intel x86 Microprocessors

- A series of CPUs featuring the advance of VLSI design and technology

uP	Date of introduction	# transistors	Feature size (microns)
80286	02/82	134,000	1.5
80386	10/85	275,000	1.5
80486	04/89	1,200,000	1.0
Pentium	03/93	3,100,000	0.8
Pentium Pro	11/95	5,500,000	0.6
Pentium II	10/98	7,500,000	0.25
Pentium III	01/99	106 mm^2	0.18
Pentium IV	11/20	217 mm^2	0.18

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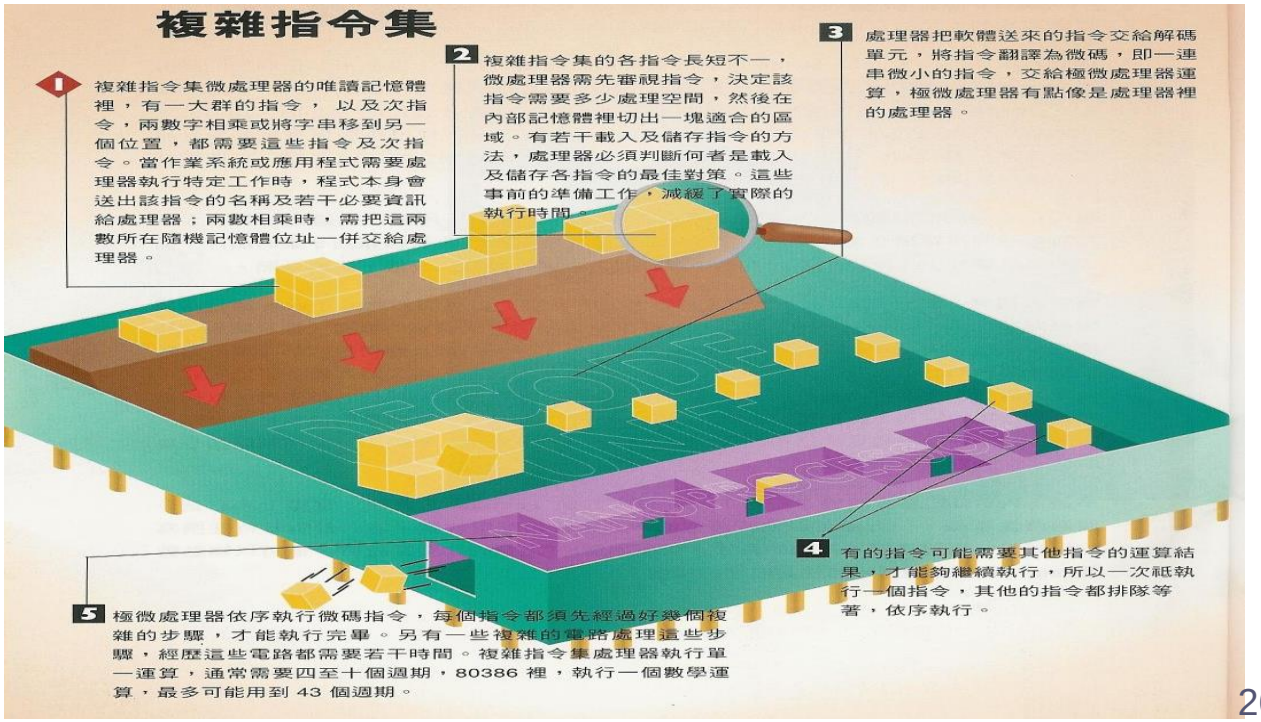
Complex Instruction Set Computer (CISC)

- **computer** in which single **instructions** can execute several low-level operations (such as a load from memory, an arithmetic operation, and a memory store)
- capable of multi-step operations or addressing modes within **single instructions**.

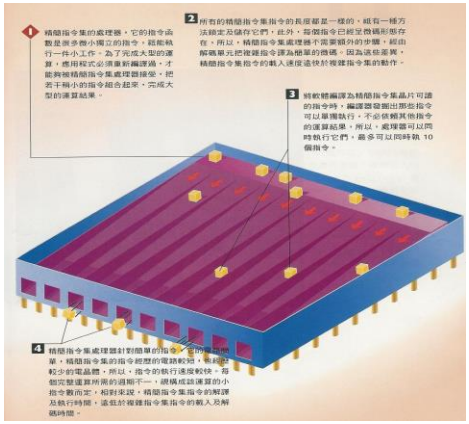


CISC

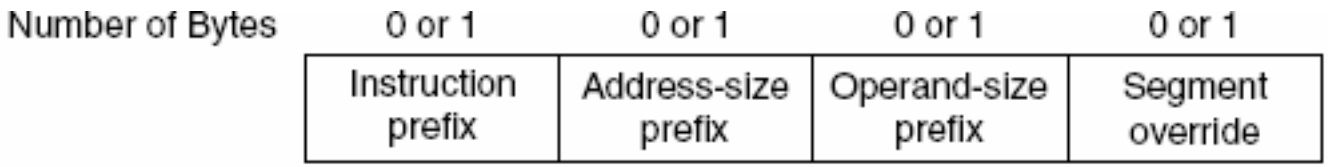
- **Microprogram**
  - ➔ A series of simple instructions is called a microprogram
  - ➔ In the CISC structure, some complicated instructions are decomposed into a series of relatively simple instructions (microprogram) for execution
  - ➔ Microprograms are usually written by engineers during the design phase,
  - ➔ Microprograms are usually invisible to ordinary programmers and cannot be modified.
  - ➔ Example: microprogram sequencer for a control memory

Reduced instruction set computer(RISC)

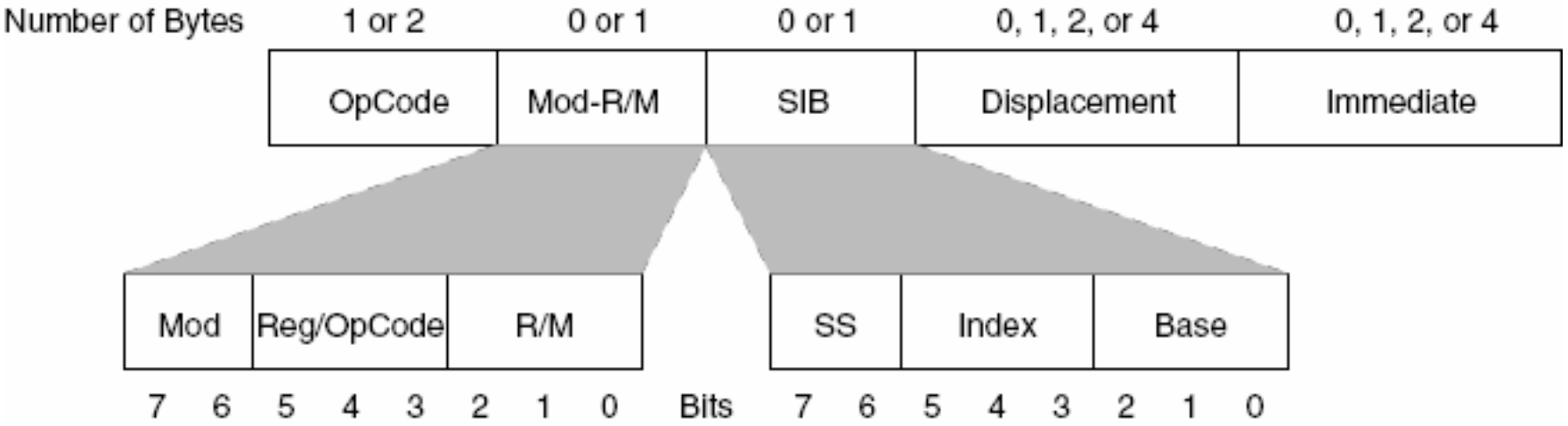
- **Reduced instruction set computer**
  - ➔ There are relatively few instruction types and address modes.
  - ➔ It has a fixed and very simple instruction decoding format.
  - ➔ Fast single cycle instruction operation time.
  - ➔ The control unit is hardwired, not microprogrammed.
  - ➔ The actions on the memory are restricted, and the main actions are the storage and retrieval of instructions.
  - ➔ Large number of registers.
  - ➔ Use compilers to optimize the performance of the object code.



X86 CICS Instruction Format

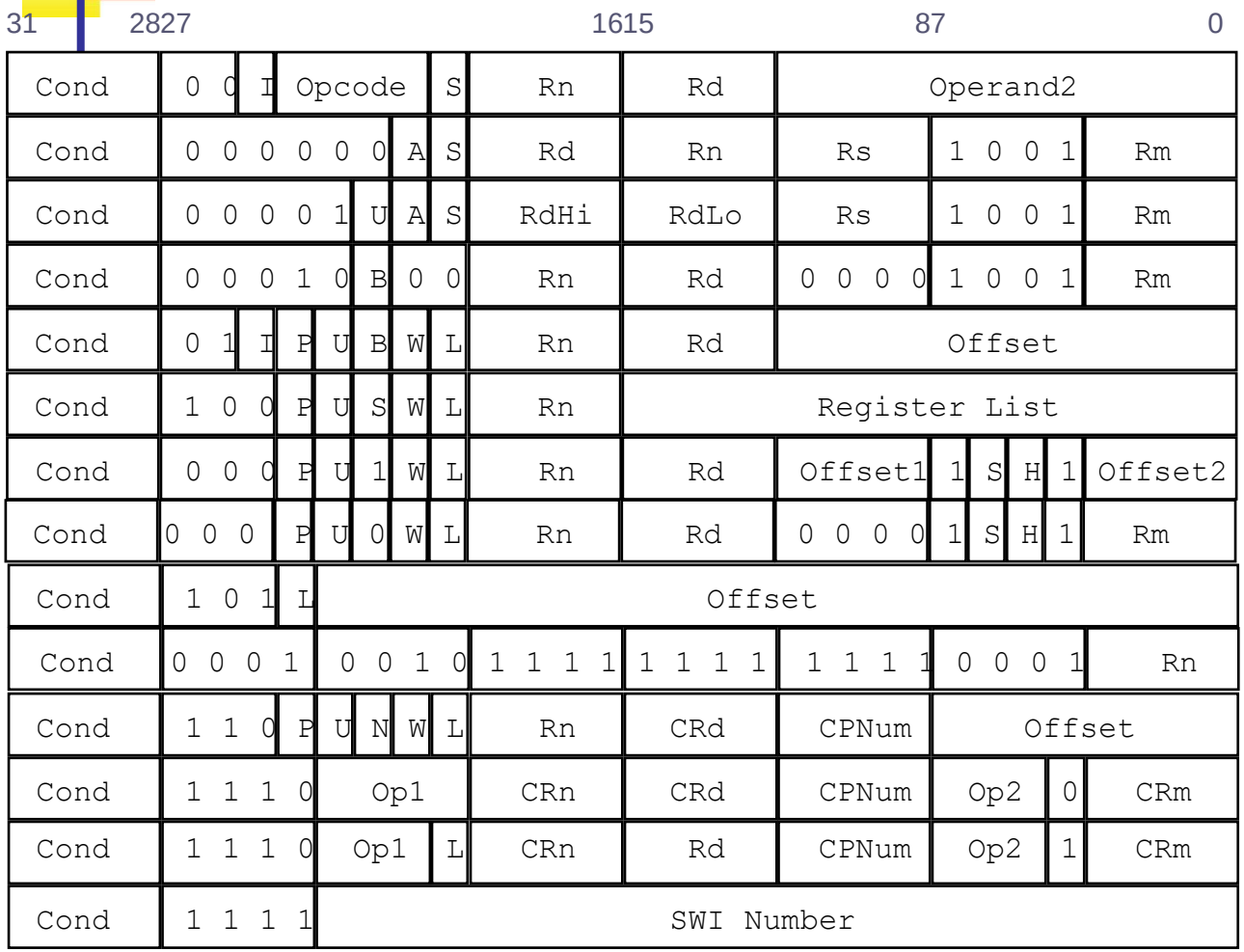


(a) Optional instruction prefixes



(b) General instruction format

ARM RICS Instruction Set Format



Instruction type

Data processing / PSR Transfer

Multiply

Long Multiply **(v3M / v4 only)**

Swap

Load/Store Byte/Word

Load/Store Multiple

Halfword transfer : Immediate offset **(v4 only)**

Halfword transfer: Register offset **(v4 only)**

Branch

Branch Exchange **(v4T only)**

Coprocessor data transfer

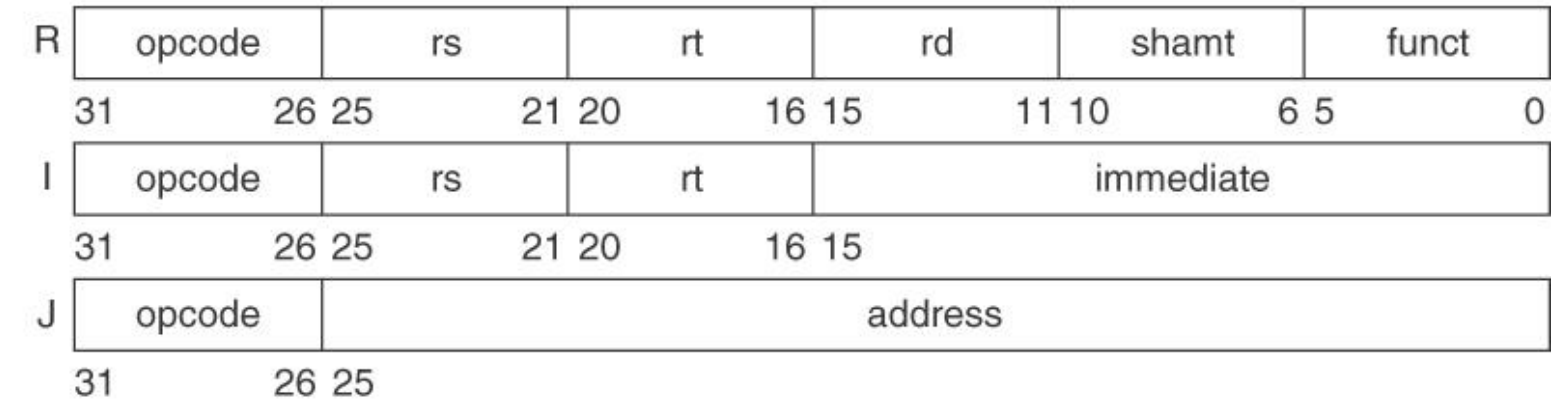
Coprocessor data operation

Coprocessor register transfer

Software interrupt

MIPS64 RICS Instruction Format

Basic instruction formats



Floating-point instruction formats

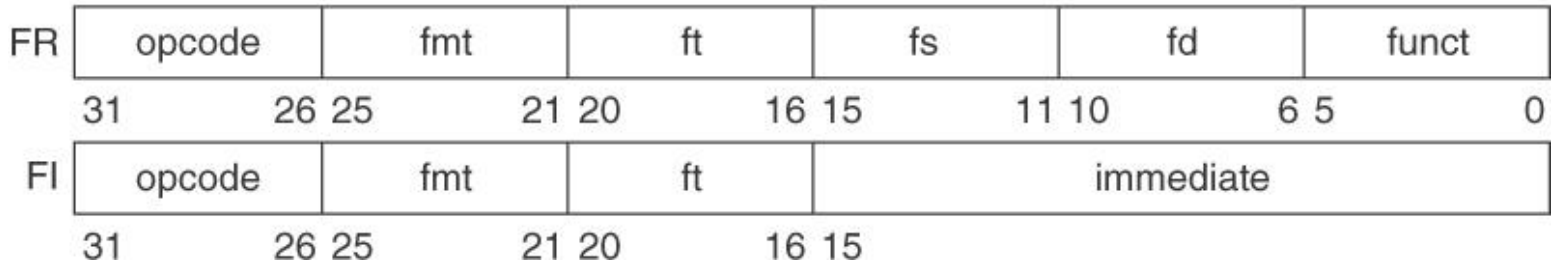


Figure 1.6 MIPS64 instruction set architecture formats. All instructions are 32 bits long.

- The R format is for integer register-to-register operations, such as DADDU, DSUBU, and so on.
- The I format is for data transfers, branches, and immediate instructions, such as LD, SD, BEQZ, and DADDIs.
- The J format is for jumps,
- the FR format for floating-point operations,
- FI format for floating-point branches.

RISC vs CISC Instruction Set

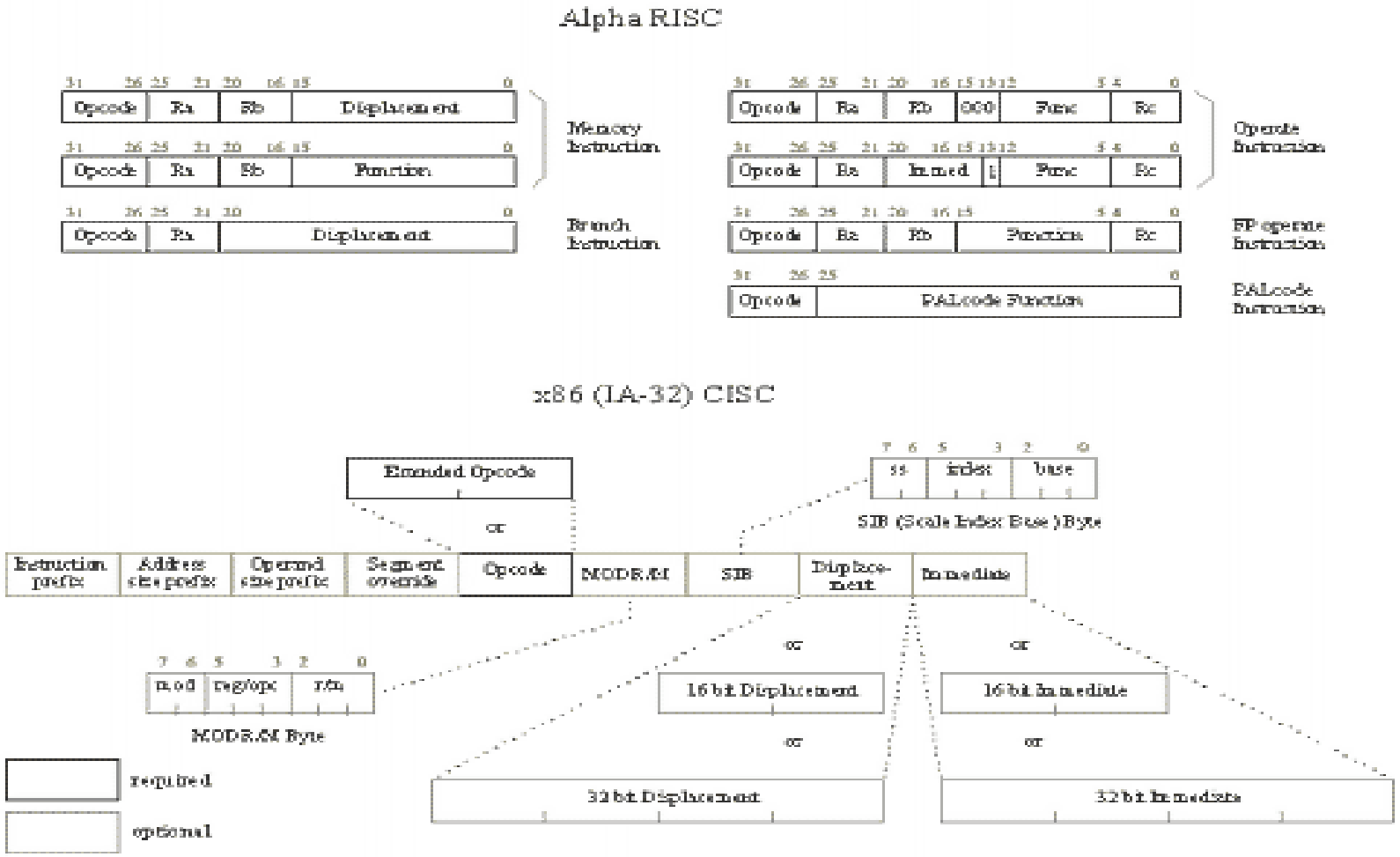


Figure 1 Instruction Encoding of Representative RISC and CISC

RISC vs. CISC Performance

- Execution of instructions
  - ➔ The format of the CISC instruction varies in length, and the number of cycles when executed is not uniform.
  - ➔ RISC structure is just the opposite, so it is suitable for the design of pipeline processing architecture.
- Formation of instructions
  - ➔ CISC adopts the design of micro-instruction code control unit because of the complicated instructions
  - ➔ 90% of RISC instructions are directly completed by the hardware
  - ➔ RISC is shorter than CISC in instruction execution time.
- RISC is simpler in design than CISC.
- In terms of performance, RISC still has the advantage.
- Due to the simplified instructions, the application code becomes larger and RISC requires a larger program memory space.

CISC and RISC Comparison

	CISC	RISC
1	Complex instructions taking multiple cycles	Simple instructions taking 1 cycle
2	Any instruction may reference memory	Only LOADS/STORES reference memory
3	Not pipelined or less pipelined	Highly piplined
4	Instructions interpreted by the microprogram	Instructions executed by the hardware
5	Variable format instructions	Fixed format instructions
6	Many instructions and modes	Few instructions and modes
7	Complexity in the microprogram	Complexity is in the compiler
8	Single register set	Multiple register sets

Source:
www.egr.msu.edu/classes/ece482/Teams/97fall/xdesign2/arm/andy.doc

Intel CPU

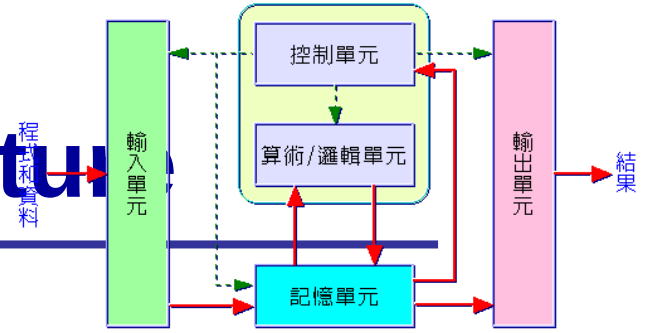
- **Intel Compatibility**
  - ➔ Each new generation of Intel architecture microprocessor is a **superset of its predecessors**.
  - ➔ Provide not only **backward compatibility** to older chips and older software, but also add **new or enhanced features**.
- **Advantages**
  - ➔ Reuse hardware
  - ➔ Reuse software
  - ➔ Reduce developers time

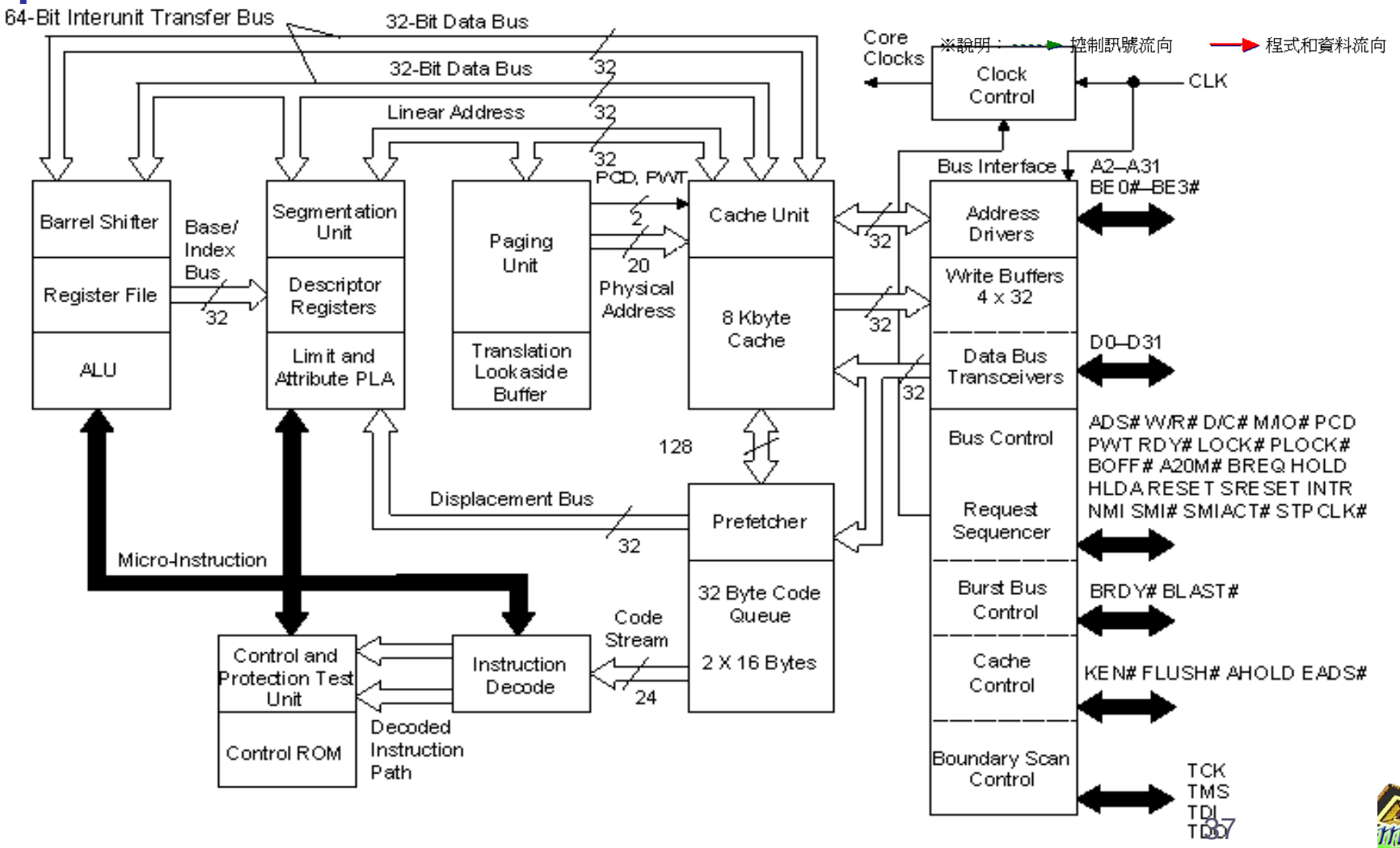
Intel 486 CPU Specification

Intel486™ DX MICROPROCESSOR

- Binary Compatible with Large Software Base
  - MS-DOS*, OS/2**, Windows*
  - UNIX*** System V/386
  - iRMX®, iRMK Kernels
- High Integration Enables On-Chip
  - 8 Kbyte Code and Data Cache
  - Floating Point Unit
  - Paged, Virtual Memory Management
- Easy To Use
  - Built-In Self Test
  - Hardware Debugging Support
  - Intel Software Support
  - Extensive Third Party Software Support
- IEEE 1149.1 Boundary Scan Compatibility
  - Available on 50 MHz Version Only
- Upgradable to Intel OverDrive™ Processor
- 168-Pin Grid Array Package
- High Performance Design
  - RISC Integer Core with Frequent Instructions Executing in One Clock
  - 25 MHz, 33 MHz, and 50 MHz Clock
  - 80, 106, 160 Mbyte/sec Burst Bus
  - CHMOS IV and CHMOS V Process Technology
  - Dynamic Bus Sizing for 8-, 16-, and 32-Bit Busses
- Complete 32-Bit Architecture
  - Address and Data Busses
  - Registers
  - 8-, 16- and 32-Bit Data Types
- Multiprocessor Support
  - Multiprocessor Instructions
  - Cache Consistency Protocols
  - Support for Second Level Cache

Intel 486 CPU Architectur





CPU BUS

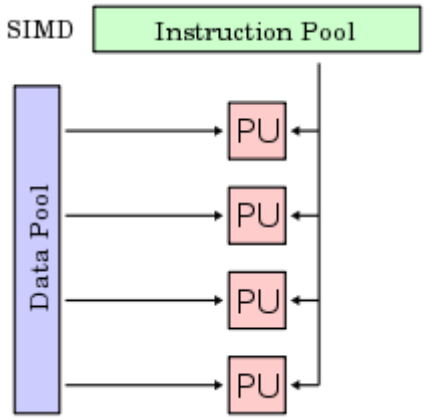
- **Address Bus**
  - ➔ Transmitting the address of the data to be accessed by the CPU.
  - ➔ Determine how much the memory capacity. N address lines can have a memory space of 2 to the N-th power, and its address is 0 to 2^N - 1.
  - ➔ Unidirectional transmission
- **Data Bus**
  - ➔ Transmitting the data to be accessed by the CPU.
  - ➔ The number of lines represents the word of the CPU, the basic unit of data that the CPU can access at a time.
  - ➔ It is often called an N-bit CPU, which means that the CPU has N data lines.
  - ➔ Bidirectional transmission
- **Control Bus**
  - ➔ Responsible for transmitting the control signal sent by the CPU.
  - ➔ Unidirectional transmission

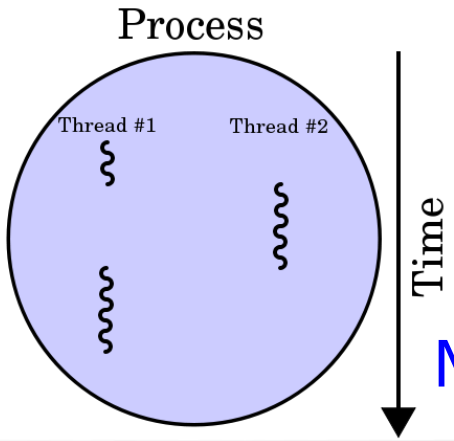
Intel Pentium CPU Features

- Multimedia extensions (**MMX technology**),
- **Intel SSE** (Stream SIMD Extension)
  - SIMD instructions increase performance for the same operations on multiple data objects.
  - Typical applications are digital signal processing and graphics processing
- **FPUs**

Other features:

Encryption/Decryption
Power management
Multilevel caches
Multithreading

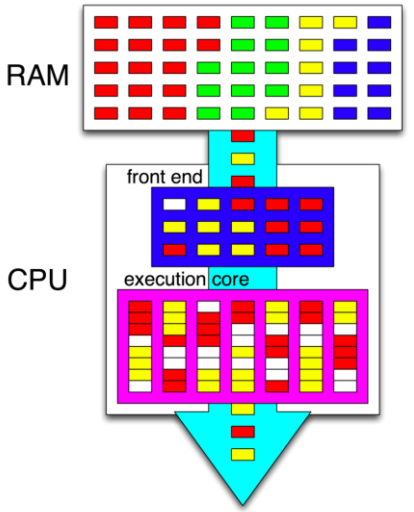




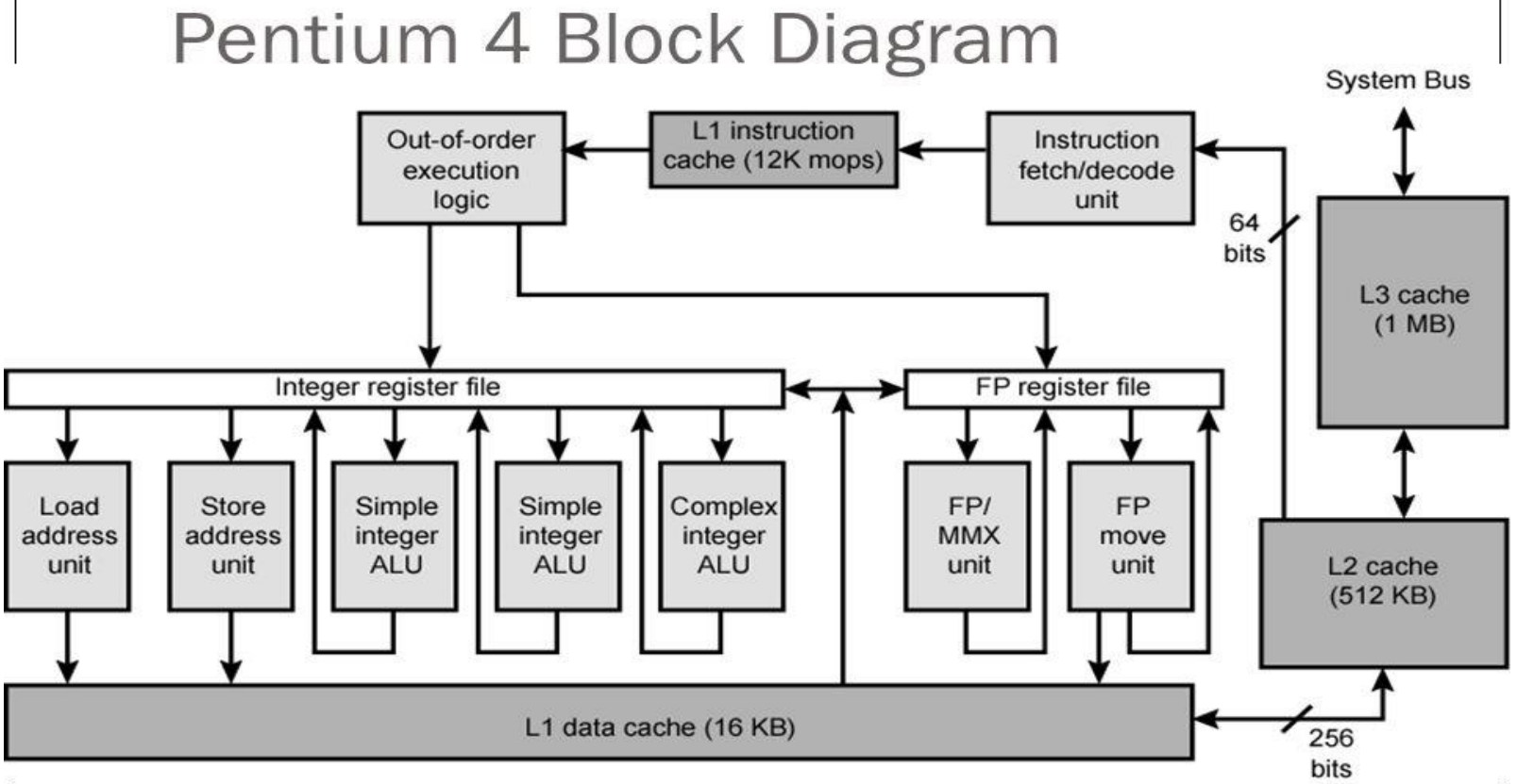
Multithreading

Next Generation Core Family

- Hyper-Threading (HT)
- single **processor** to handle two independent sets of instructions at the same time.
- **HT** Technology converts a single physical **processor** into two virtual **processors**
  - ➔ implementation used to improve parallelization of computations (doing multiple tasks at once)
  - ➔ Instructions are fetched from RAM
  - ➔ (differently colored boxes for four different programs),
  - ➔ execution core capable of executing instructions
  - ➔ from two different programs
  - ➔ during the same clock cycle



Pentium function block



Intel CPU Evolution

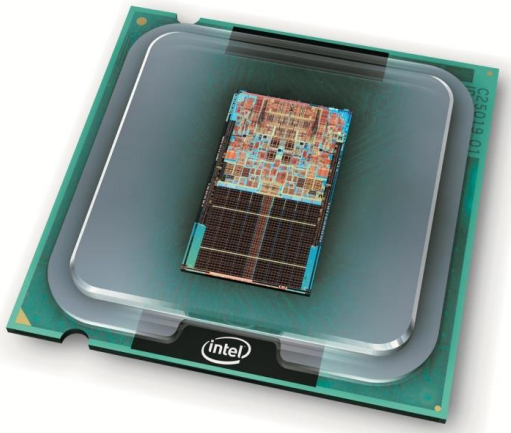
Multi-core: more than one CPU core in a die

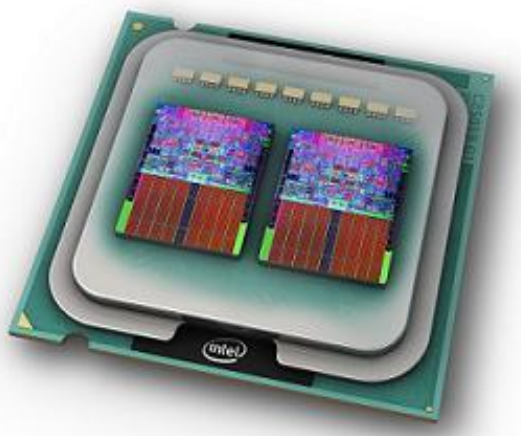
TDP: **Thermal Design Power**(Prescott, Smithfield-90nm)

Year	Architecture	CPU	Core Count	TDP	Clock Speed (MHz)
2004	Prescott	Pentium 570J	1+HT	115	3800
2005	Smithfield	Pentium 840 EE	2+HT	130	3200
2006	Kentsfield	C2E QX6800	4	130	2930
2007	Yorkfield	C2E QX9650	4	130	3000
2008	Nehalem	Core i7-965	4+HT	130	3200 / 3460
2009	Nehalem	Core i7-975	4+HT	130	3360 / 3600
2010	Westmere	Core i7-980X	6+HT	130	3360 / 3600
2011	Sandy Bridge-E	Core i7-3960X	6+HT	130	3300 / 3900
2012	Ivy Bridge	Core i7-3770K	4+HT	77	3500 / 3900
2013	Ivy Bridge	Core i7-4960X	6+HT	130	3600 / 4000
2014	Haswell	Core i7-4790K	4+HT	88	4000 / 4400
2015	Skylake	Core i7-6700K	4+HT	91	4000 / 4200

Core 2 Series

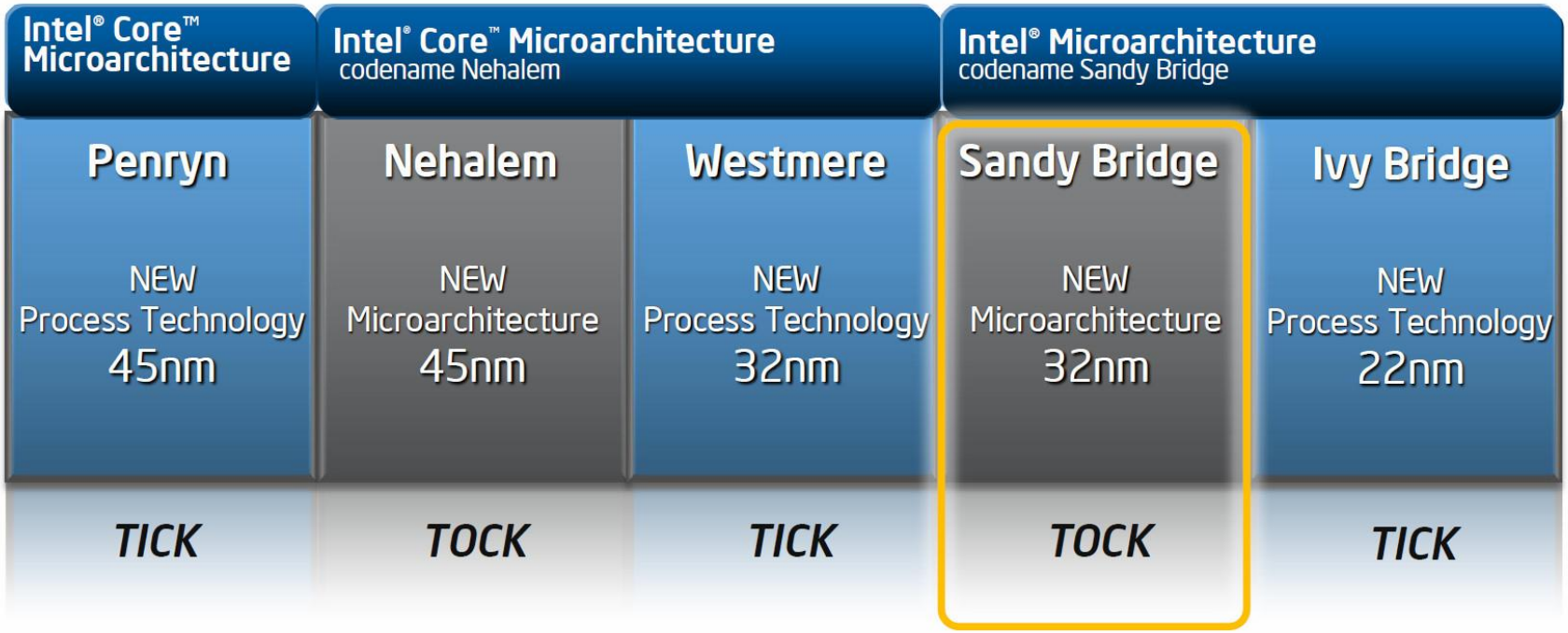
- High performance induces high power issues
- Prescott/Smithfield have high TDP
- Energy efficiency is lower than AMD CPU
- Centrino –platformization (integrate low power CPU, chipset and Wi-Fi) for notebook intel's successful return to King of CPUs





Architecture/Process Tick Tock

- Tick Tock strategy – increase performance
- Tick: mature microarchitecture on new process
- Tock: mature process on new microarchitecture

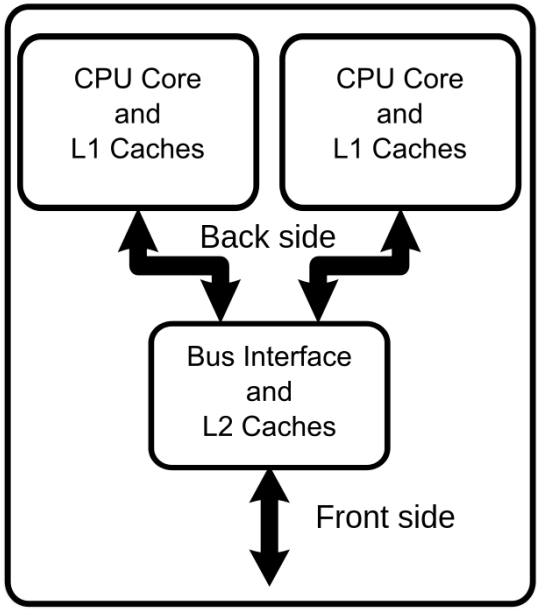


Knight's Corner

- High Performance Computing: over 1 TeraFlops operations

Hardware trend

- Multi-core to many-core:
  - ➔ from dual-, quad-, eight-core to tens or even hundreds of cores.
- Heterogeneous:
  - ➔ special purpose processors cores in addition to general purpose cores for higher efficiency in processing multimedia, recognition and networking applications
- Energy-efficiency:
  - ➔ focus on performance-per-watt
  - ➔ with advanced fine-grain or ultra fine-grain power management
  - ➔ Dynamic voltage frequency scaling (DVFS)
- Multiple Cache



Multi-core and Multi-threaded

- A multi-core microprocessor
  - ➔ one that combines two or more independent processors into a single package, often a single integrated circuit (IC).
  - ➔ multi-core microprocessors allow a computing device to exhibit some form of thread-level parallelism (TLP)

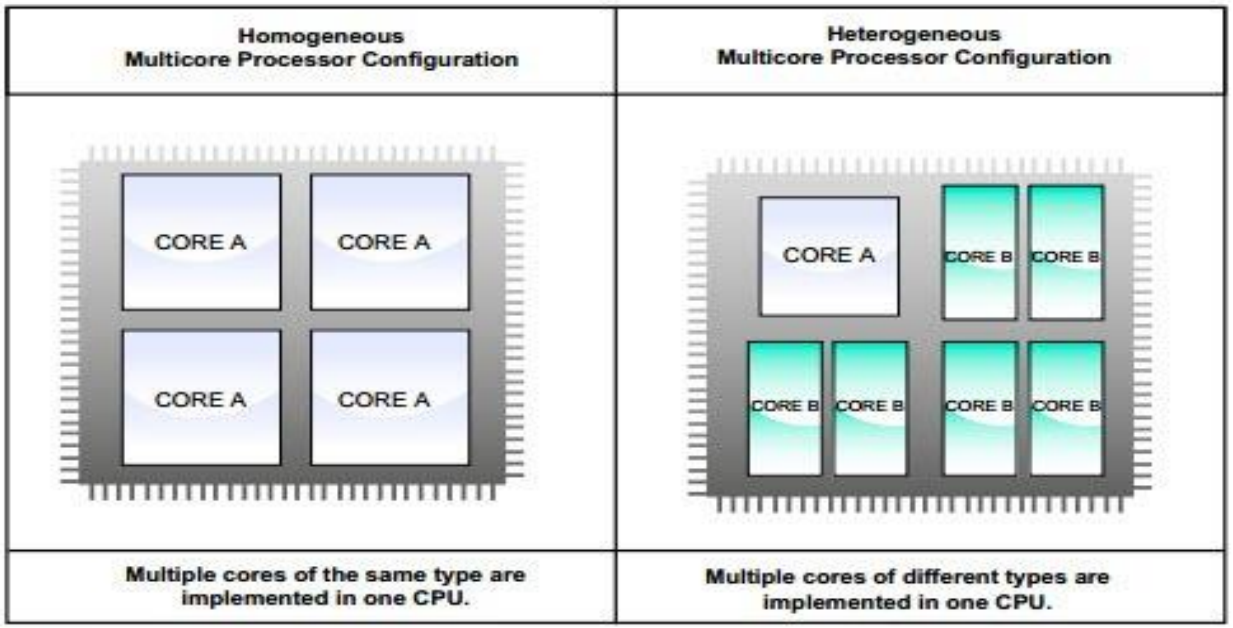
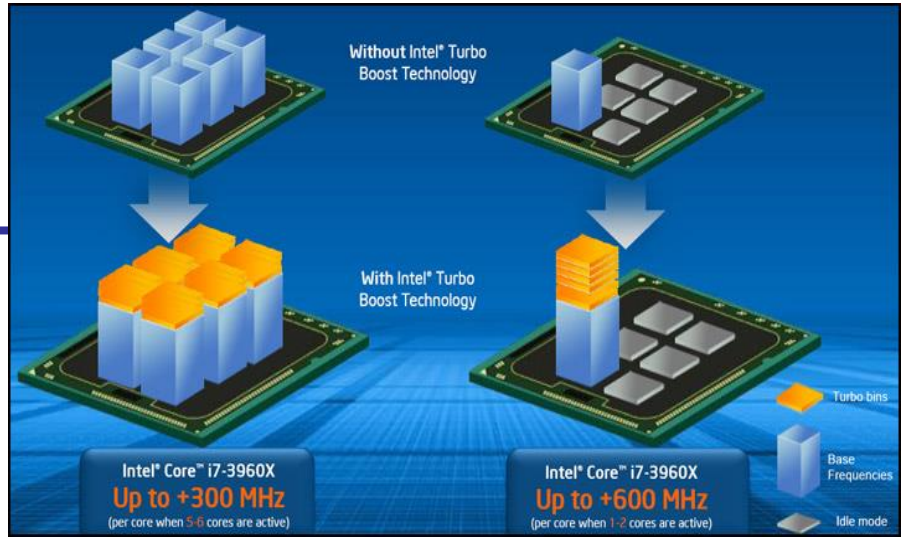


FIGURE 5.13

A sketch diagram for both homogeneous (symmetric) and heterogeneous (asymmetric) multicore processors

Intel Core i7 CPU



- High computation power
- High Speed
- Turbo Boost Technology
  - ➔ Detect the voltage of the processor,
  - ➔ Speed up the clock rate of the running processing core if it is lower than the rated limit
  - ➔ Frequency increases occur in increments of
    - ➲ 133 MHz for Nehalem processors
    - ➲ 100 MHz for Sandy Bridge, Ivy Bridge, Haswell and Skylake processors.
- Fantastic entertainment and gaming
- Seamless 4K Ultra HD, and 360 video

Intel Core i7 Microprocessors

- **A series of CPUs featuring the advance of VLSI design and technology**

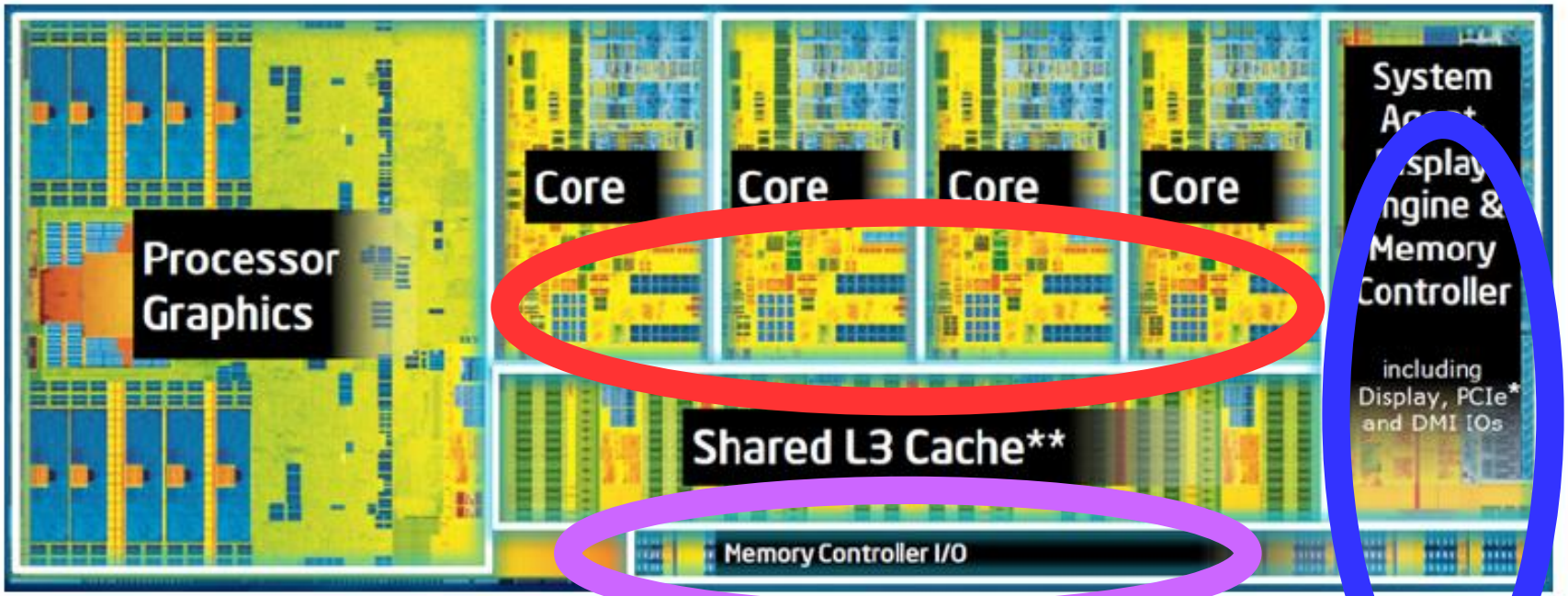
Core i7	Bloomfield Lynnfield Gulftown Sandy Bridge Sandy Bridge-E Sandy Bridge-E Ivy Bridge Haswell Ivy Bridge-E Ivy Bridge-E Haswell-E Broadwell Skylake Kaby lake-7700K	4 (core number) 4 6 4 6 4 4 4 4 6 6 4 4 4/8	45 nm 45 nm 32 nm 32 nm 32 nm 32 nm 22 nm 22 nm 22 nm 22 nm 22 nm 14 nm 14 nm(Sept/2015) 14nm

Intel microprocessor

Codename (main article)	Brand name (list)	Cores	L3 Cache	GPU Model	Socket	TDP	Process	I/O Bus	Release Date
Broadwell-DT (Desktop)[49]	Core i7-5775C	4	6 MB	Iris 6200	LGA 1150	65 W	14 nm	Direct Media Interface, Integrated GPU	June 2015
	Core i7-5775R								
Broadwell-U (Mobile)	Core i7-5xx7U	2	4 MB	Iris 6100	BGA 1168	28 W	14 nm	Direct Media Interface Integrated GPU	January 2015
	Core i7-5x50U			HD 6000		15 W			
	Core 7i-5x00U			HD 5500					

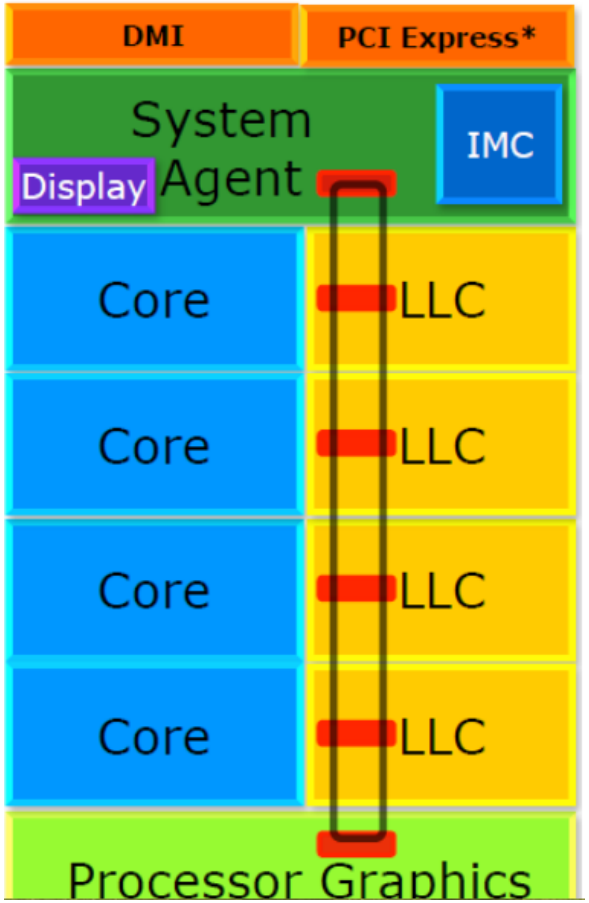
Intel Core i7 Processor

- Four independent CPU cores.
- Integrated L1, L2 and L3 caches.
- Memory controller



The Relations between CPU & Caches

- CPU each has caches :L1,L2
- Shared caches : L3
- DRAM controller:
  - Responsible for cache coherence.
- Memory controller:
  - DRAM refresh via BIOS to support multiple speed.
- Graphics Process
- PCI Express
  - Responsible for cache coherence.
- DMI (Direct Media Interface)



Intel i7 floorplan

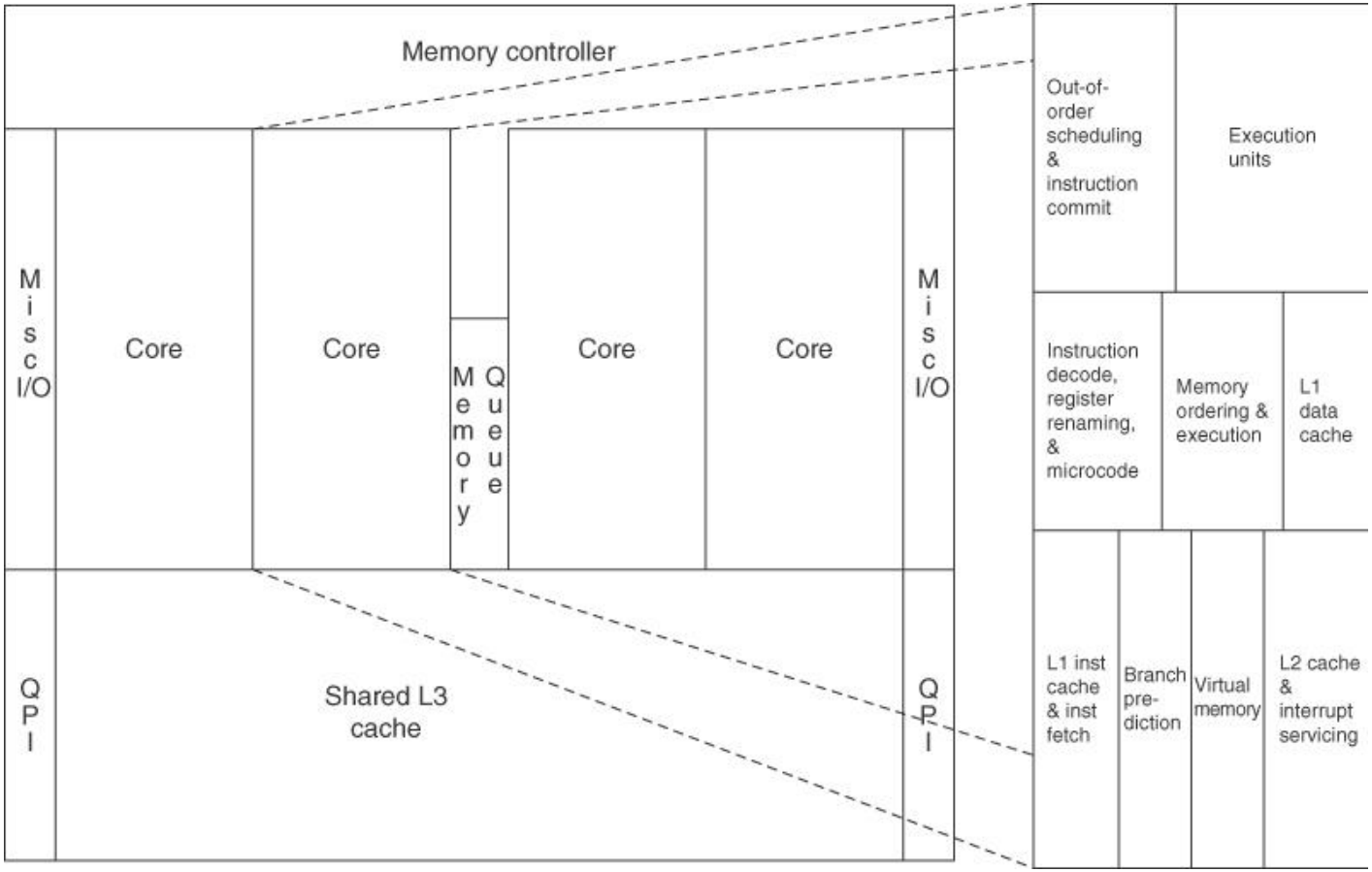


Figure 1.14 Floorplan of Core i7 die in Figure 1.13 on left with close-up of floorplan of second core on right.

Intel i7

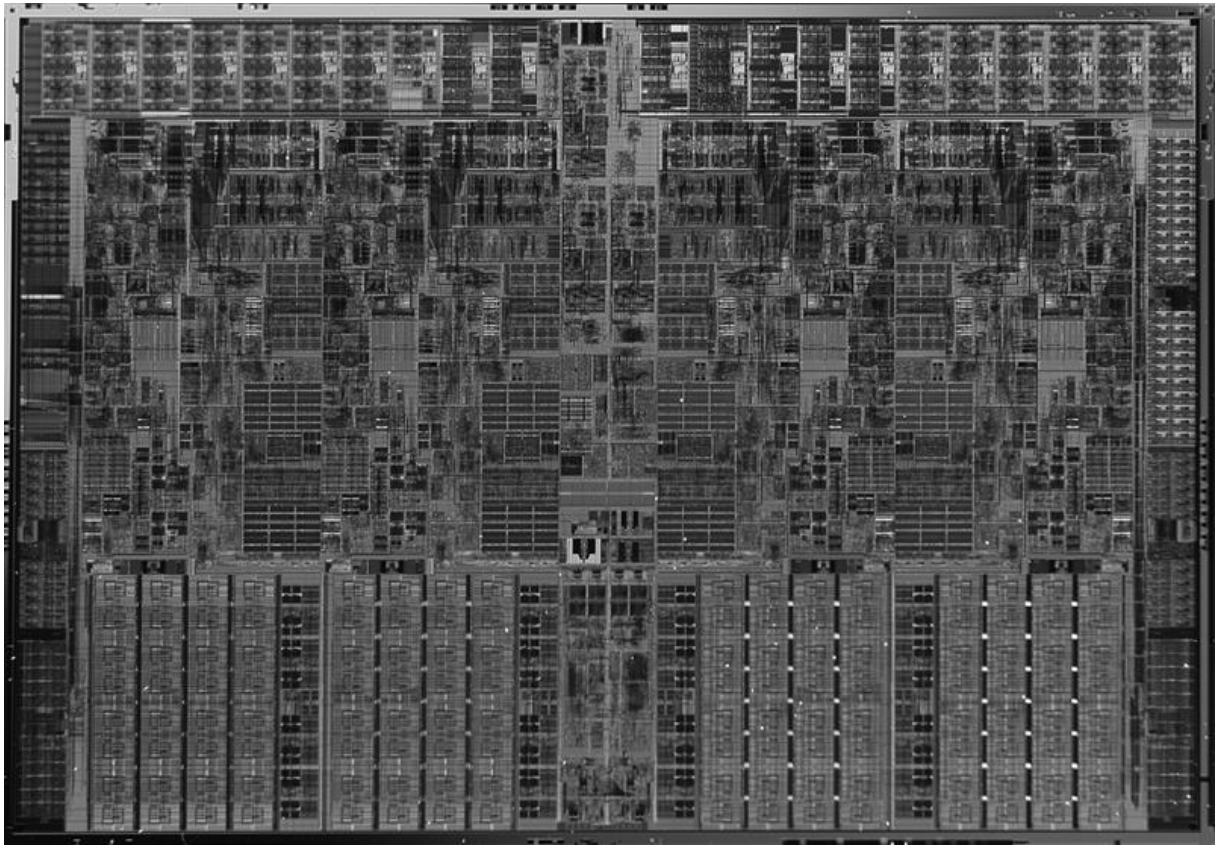
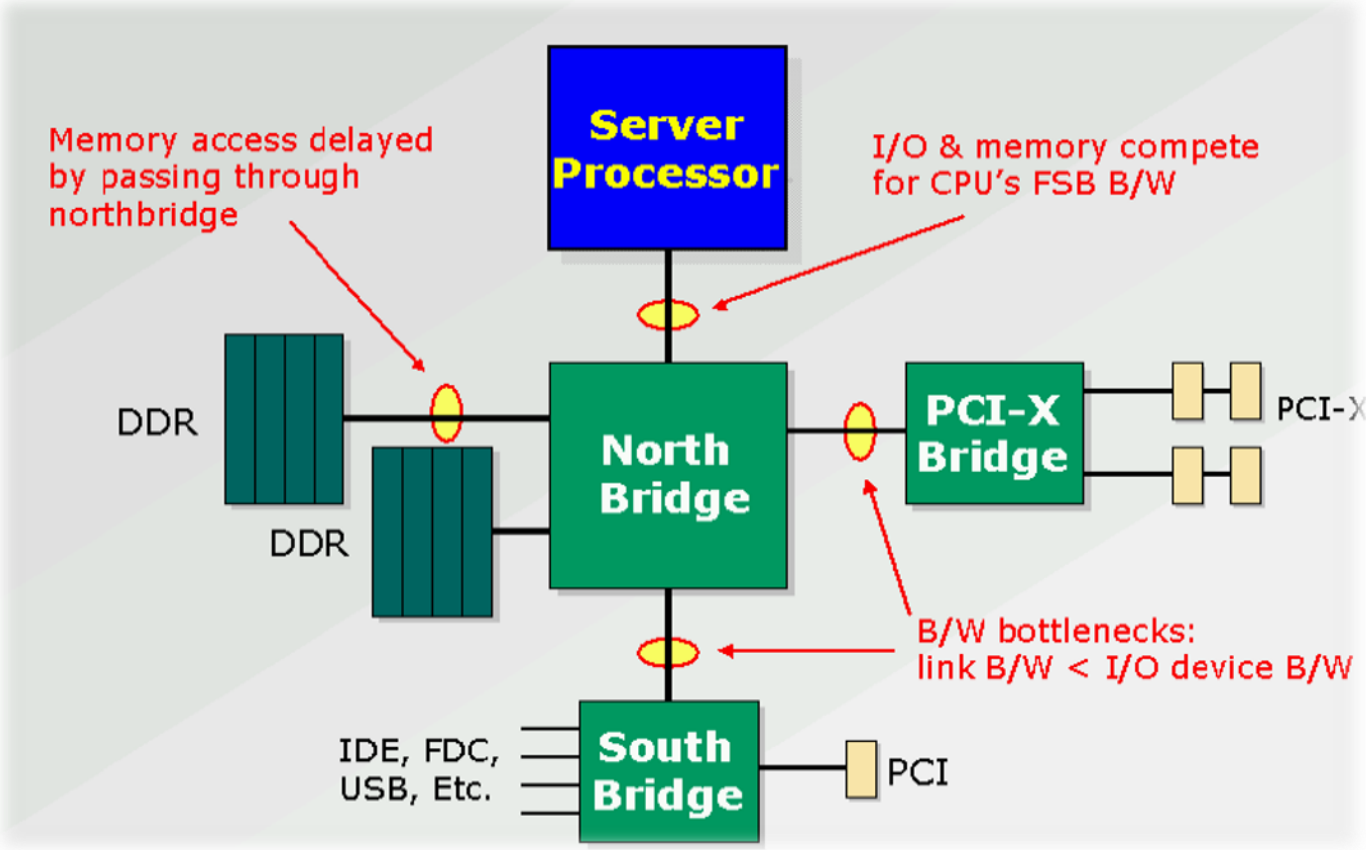


Figure 1.13 Photograph of an Intel Core i7 microprocessor die The dimensions are 18.9 mm by 13.6 mm (257 mm2) in a 45 nm process. (Courtesy Intel.)

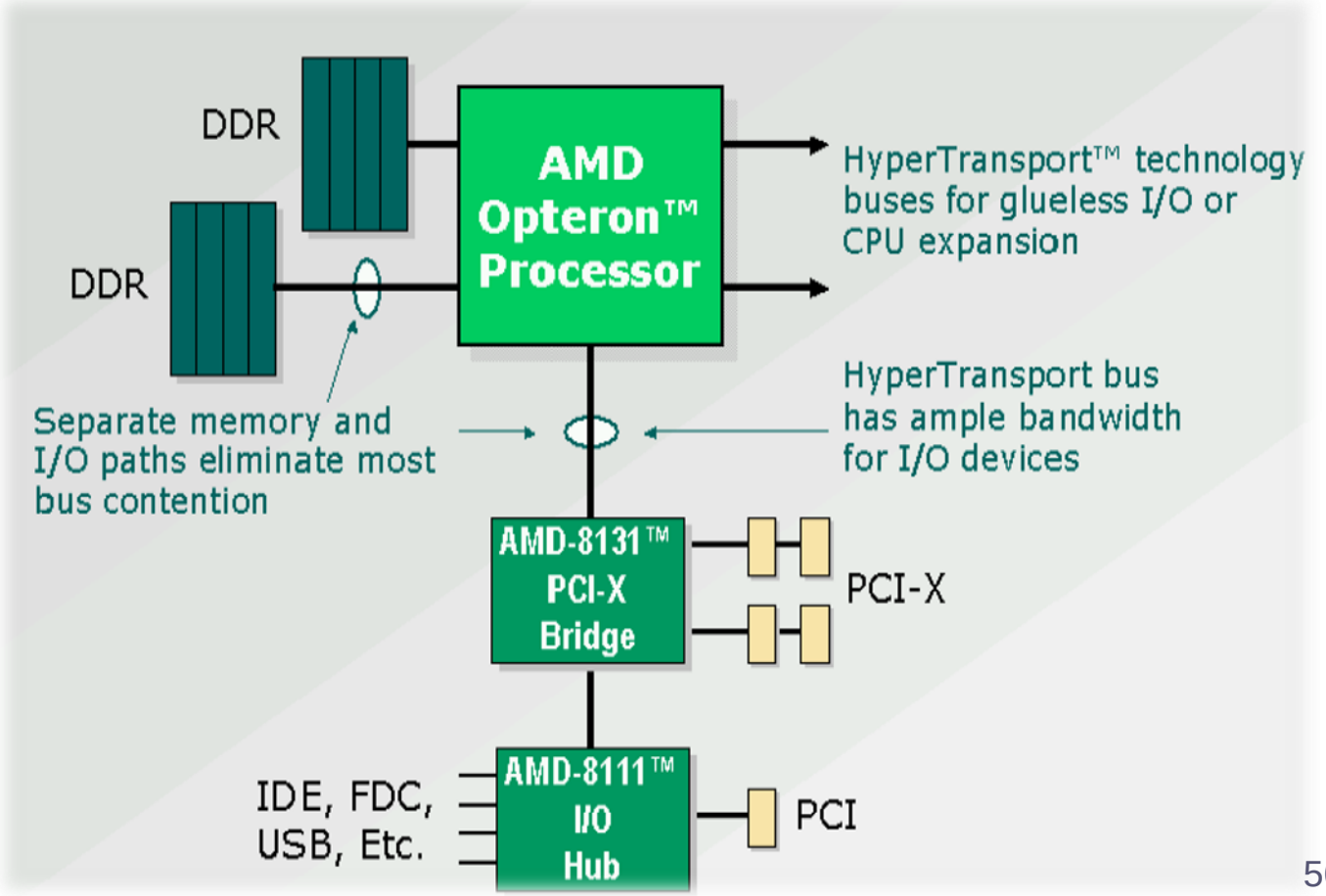
Architecture Implementation

- Three major components (early):
  - Processor chip,
  - MCH (Memory Controller Hub, North bridge),
  - ICH (I/O Controller Hub, South bridge)



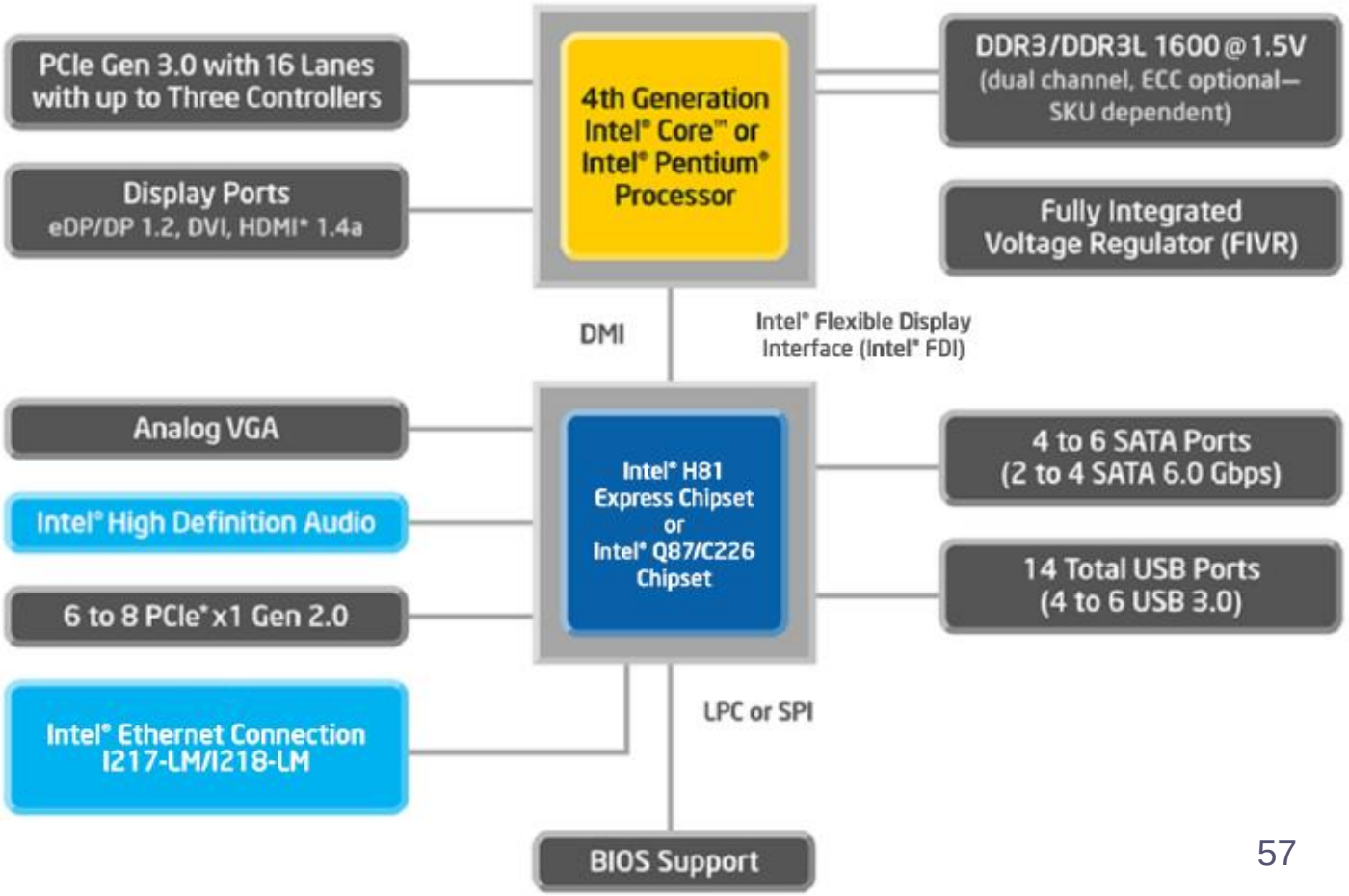
Architecture Implementation

AMD Opteron series

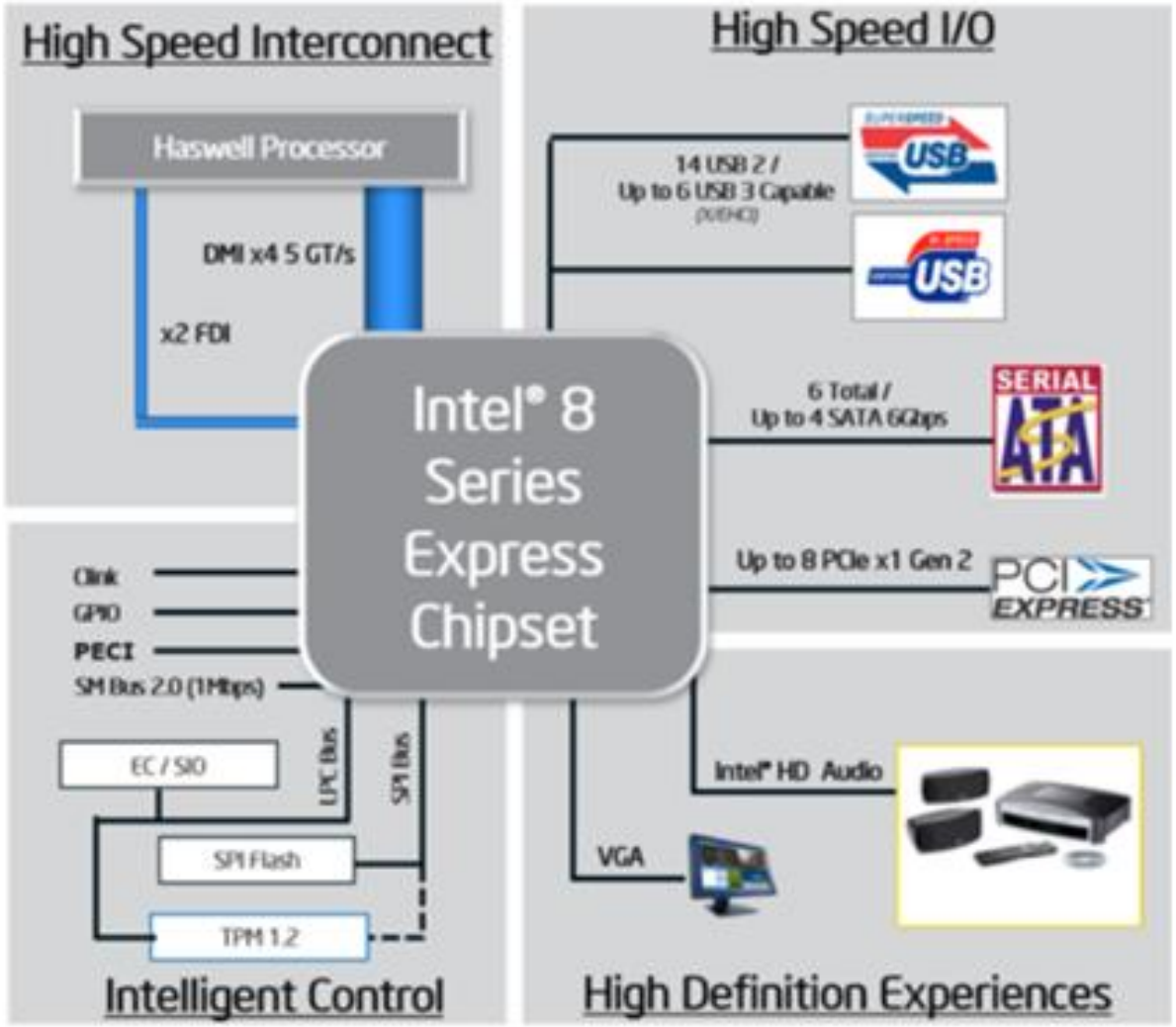


Intel Core i7 processor Hardware Platform

- Two major components (today):
  - Microprocessor chip
  - PCH (Platform controller hub)



Platform Controller Hub (PCH)



Compatibility Peripherals

The PCH contains

- **Two 82C37 DMA controllers**
  - DMA(Direct Memory Access)， The main function is to directly access the memory without going through the CPU.
  - Using DMA has two great benefits for CPU
    - Increased CPU usage efficiency
    - Faster than using CPU to manipulate memory
- **Two ISA-compatible 82C59 interrupt controllers**
  - The interrupt controller is the bridge of interrupt processing between the CPU and the peripheral device. The interrupt request sent by the peripheral device needs to be processed by the interrupt controller.
  - In the past : Two 82C59 controllers can support 15 interrupt sources.
  - Now : Two ISA-compatible 82C59 interrupt controllers can support over 15 interrupt sources.

ISA: Interrupt storage area

DMI (Direct Media Interface)

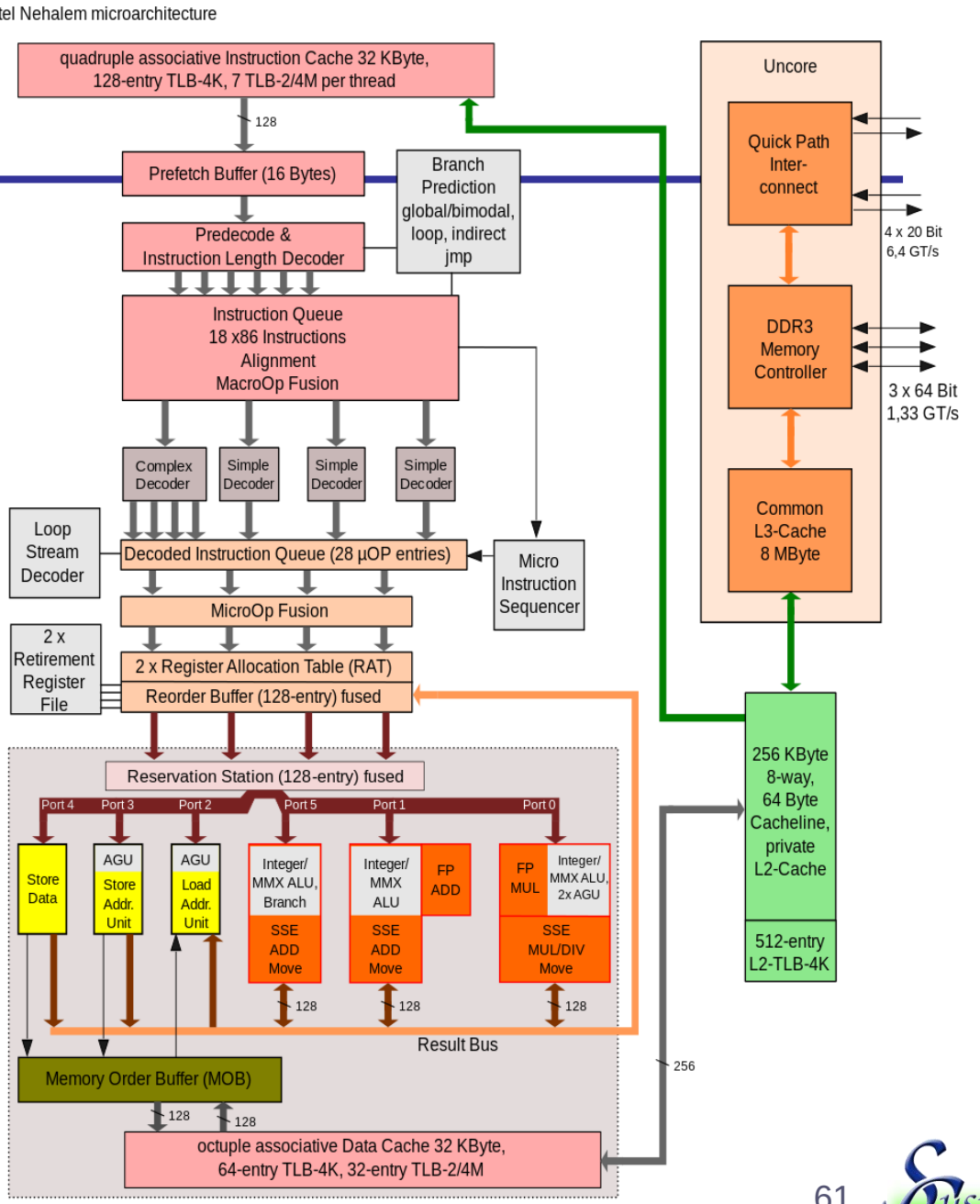
- Early:
  - Only support the communication between processor and I/O .
- Today:
  - Link between Intel Core i7 processor and its companion chip. (point to point with 2GB/s)
- High-Compatibility.
- QPI (Quick Path Interconnect) Replace FSB (front side Bus) – used to connect processor to I/O Hub

QPI:

- Support high transportation of processor and I/O,
- Links processor and external memory (point to point)

QPI

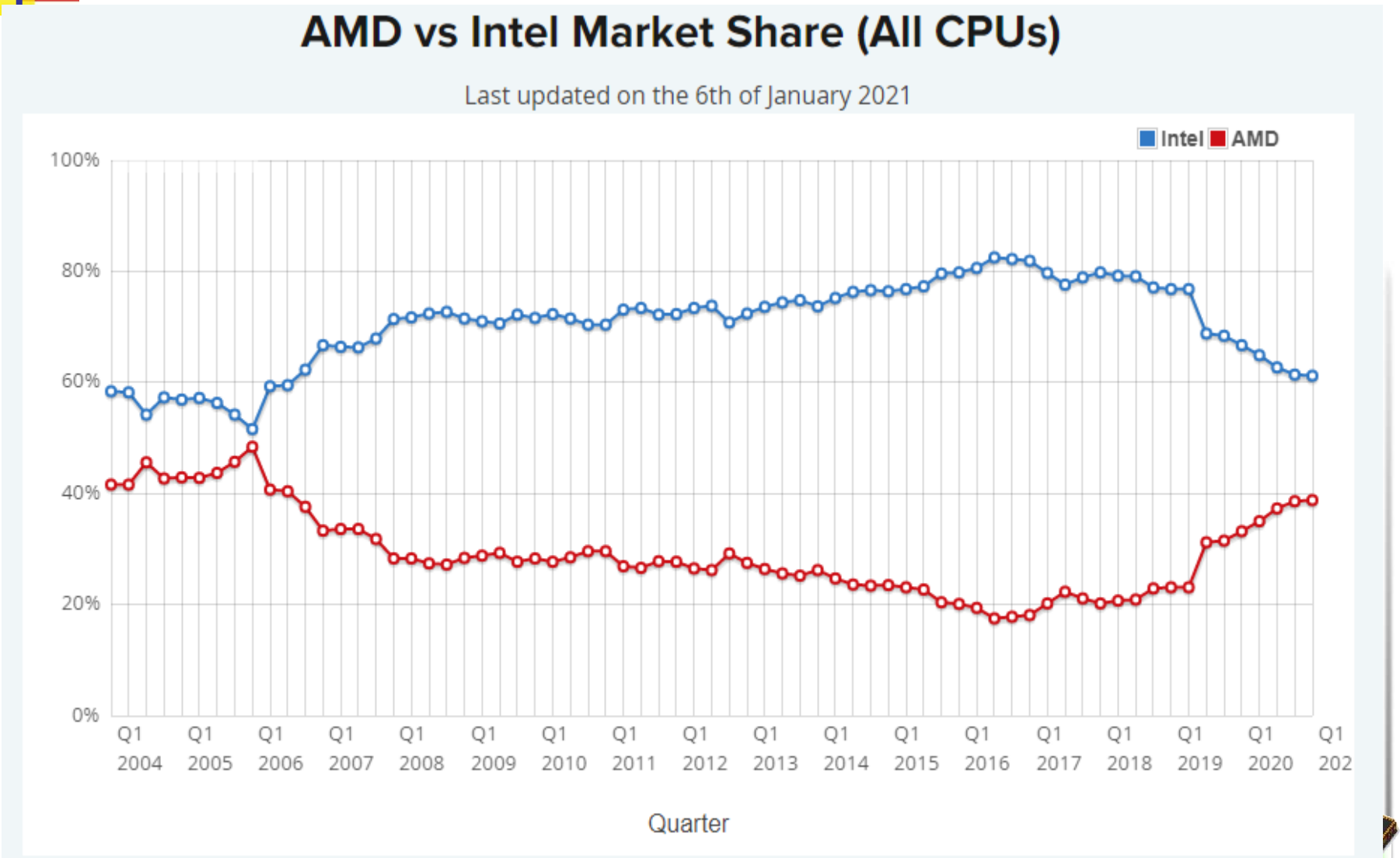
- QPI (Quick Path Interconnect) module – used to connect processor to I/O Hub



PCI-E (Peripheral Component Interconnect Express)

- **PCI**
  - A standardized way of exchanging data between computer components
  - External GPU, storage devices, cluster interconnect
- **PCI-E:**
  - The existing PCI programming concepts and communication standards are used.
  - The existing PCI system can be converted to PCI-E only by modifying the physical layer without modifying the software.
  - PCI-E has a faster rate to replace almost all existing internal bus (including AGP (accelerated graphic port and PCI)

CPU Market Survey



Intel Porter's 5 Forces Analysis

- **Substitute Products**
  - ➔ AMD, VIA, processors using x86.
- **Bargaining Power of Suppliers**
  - ➔ Design and Manufacture are all controlled within Intel.
  - ➔ Monopoly of Market leads to near 0 power for PC suppliers.
- **Threat of New Competition**
  - ➔ x86 market unlikely
  - ➔ ARM

Intel Porter's 5 Forces Analysis

- **Bargaining Power of Customers**
  - ➔ Household brand, thus preference.
- **Intensity of Rivalry**
  - ➔ So far not a lot…
  - ➔ Perhaps in the Future Mobile Market
  - ➔ Intel VS ARM, Qualcomm, Samsung, nVidia…etc

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Porter's 5 forces?

Intel S.W.O.T. Analysis

- **Strengths**
  - ➔ Father of Processors
  - ➔ Market Leading Manufacturing Process
  - ➔ Strong market position and brand Image
- **Weakness**
  - ➔ Lack of Presence in the Mobile Market
  - ➔ High retail price
- **Opportunities**
  - ➔ Mobile Market
  - ➔ Advancements in Technologies
  - ➔ Product and Market Penetration in existing Markets
- **Tread**
  - ➔ Changing customer preferences and loyalty
  - ➔ RISC CPUs slowly taking up x86 Market Share
  - ➔ TSMC, Samsung, Global Foundries catching up

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