Introduction to System-On-Chip and its Applications

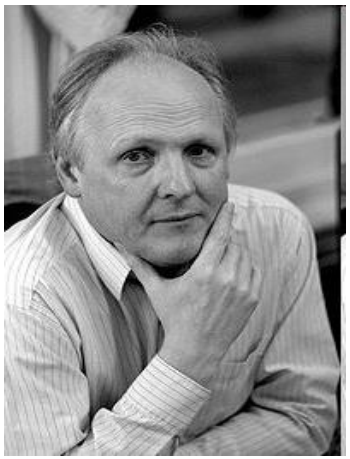
ARM Processors and Architectures

Outline

- ARM Mircoprocessor Applications
- ARM Architecture Overview
- Embedded applications
- Smart phone applications
- PC applications
- ARMv7-AR Architecture
  - ARM System Design

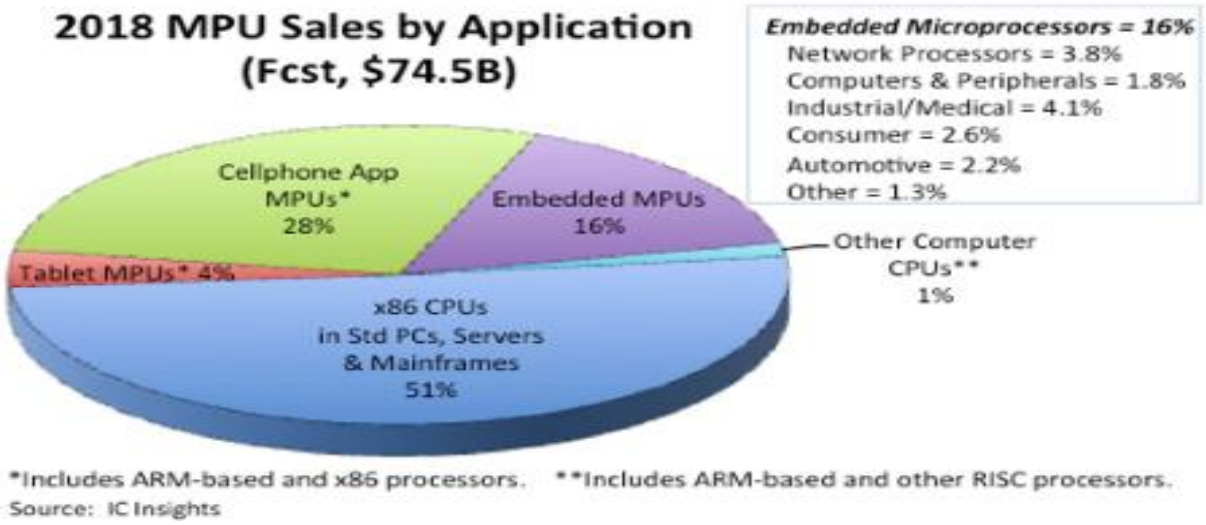
ARM Company History

- **A**dvanced **R**ISC **M**achines (ARM)
- 1985 Acorn Computer Group developed the world's first commercial RISC processor(developed by the team led by Steve Furber and Sophie)
- ARM founded in November 1990
- Company headquarters in Cambridge, UK
  - Processor design centers in Cambridge, Austin
  - Sales, support, and engineering offices all over the world



ARM Company History

- Best known for its range of RISC processor cores designs
  - Other products – fabric IP, software tools, models, cell libraries –
  - Help partners develop and ship ARM-based SoCs
- ARM does *not* manufacture silicon
- SoftBank completes $31 billion acquisition of ARM at Sep. 2016
- Nvidia acquire ARM for $40 Billion from Softbank at Sep. 2021
- Nvidia terminated the bid for ARM at Feb. 2022



Where is ARM???

- ARM is everywhere. 25 Billion ARM-based Chips in 2020

7.9 Billion ARM-Based Chips in 2011


Recon Goggles
Heads Up Display

LiveScribe
Smartpen


WiFi
Routers


Braun
Coffee Machine


Asus
Eepad Transformer


Bernina 830
Sewing Machine


Western Digital
My Passport disk drives


Bluetooth


di A8 (2012)
nfotainment

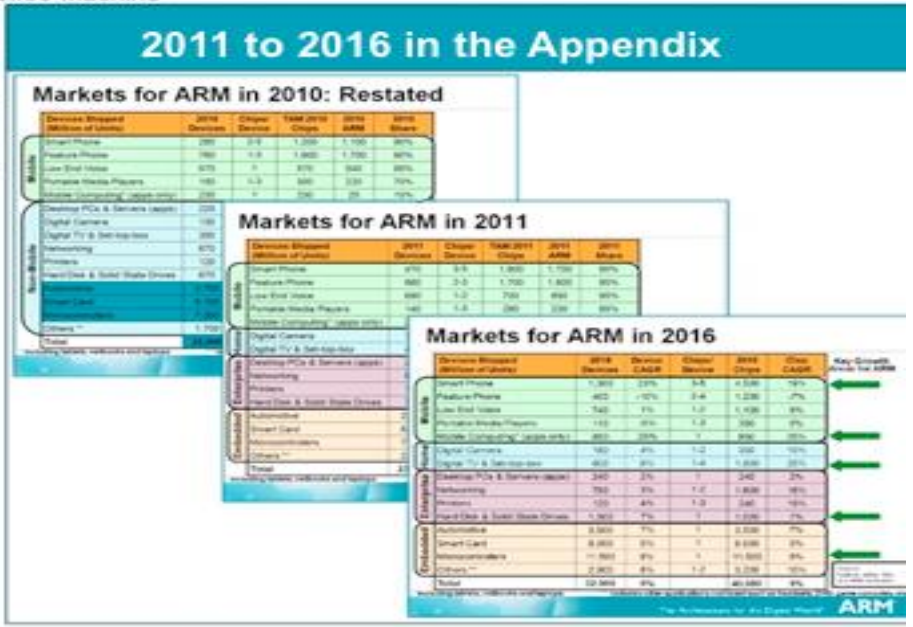

Steelseries
Sensei Mouse


HP Photosmart Printer


Embedded Labs
Industrial Network Server

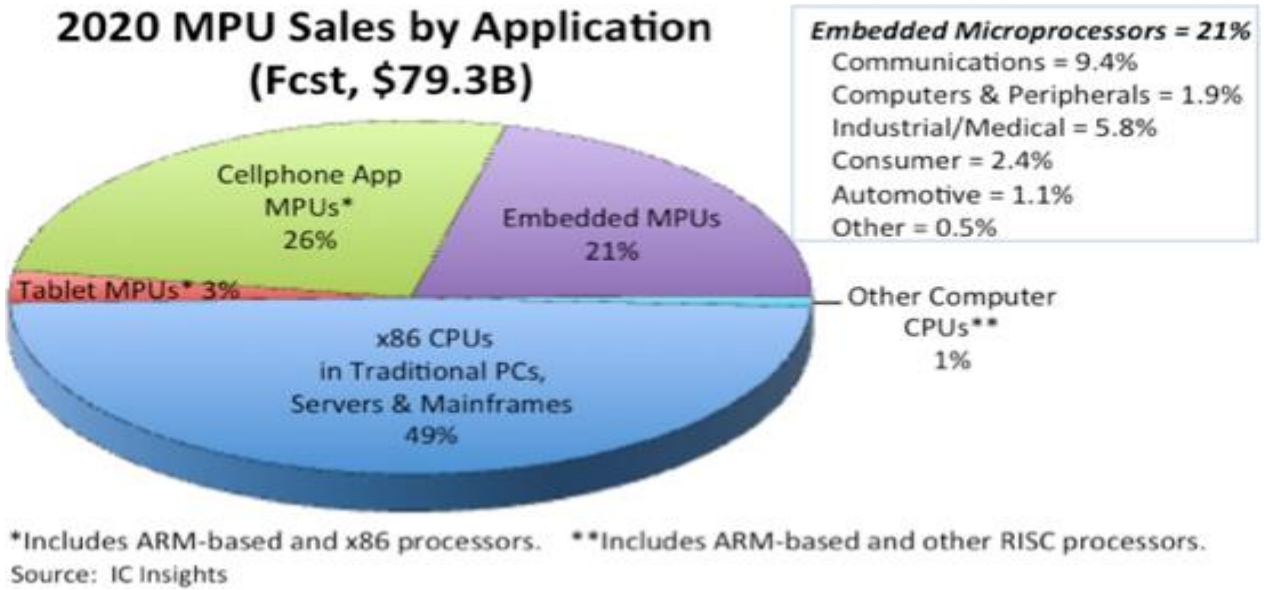

Verifone
Cash Terminal


HTC
Sensation



ARM Applications

- PC, Mainframes, servers
- Cellphone
- Embedded Mircoprocessor



Markets for ARM in 2016

	Devices Shipped (Million of Units)	2016 Devices	Device CAGR	Chips/ Device	2016 Chips	Chip CAGR	Key Growth Areas for ARM
Mobile	Smart Phone	1,300	23%	3-5	4,500	19%	←
	Feature Phone	400	-10%	2-4	1,200	-7%	
	Low End Voice	740	1%	1-2	1,100	9%	
	Portable Media Players	110	-5%	1-3	350	5%	
	Mobile Computing* (apps only)	850	25%	1	850	25%	←
Home							
							←
Enterprise	Desktop PCs & Servers (apps)	240	2%	1	240	2%	
	Networking	790	3%	1-2	1,600	16%	
	Printers	120	4%	1-3	240	19%	
	Hard Disk & Solid State Drives	1,000	7%	1	1,000	7%	←
Embedded	Automotive	3,500	7%	1	3,500	7%	
	Smart Card	8,000	5%	1	8,000	5%	
	Microcontrollers	11,500	8%	1	11,500	8%	←
	Others **	2,900	8%	1-2	3,200	10%	
	Total	**32,000**	**6%**		**40,000**	**9%**	

Source: Gartner, InStat, SIA, and ARM estimates

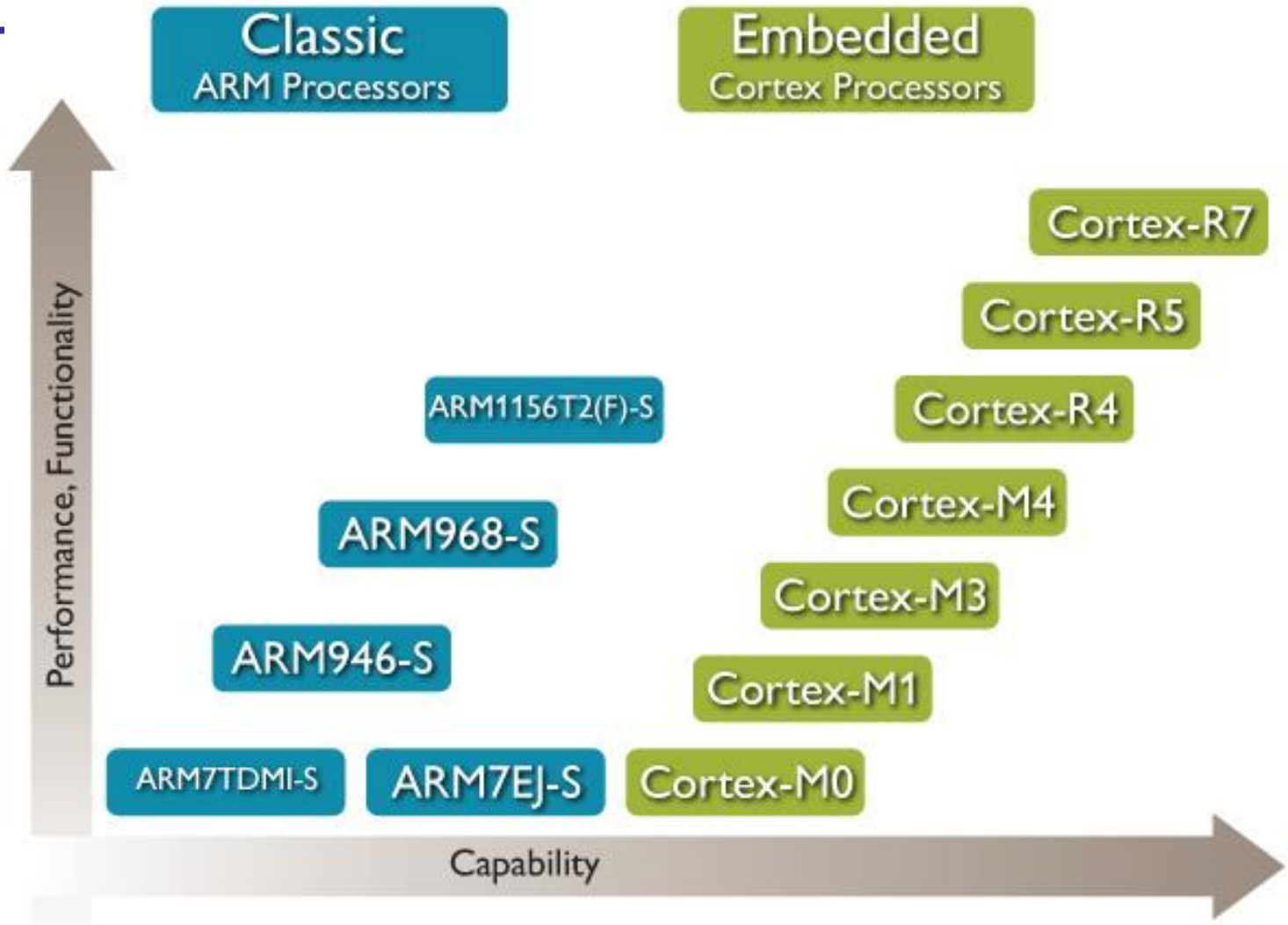
* Including tablets, netbooks and laptops

** Includes other applications not listed such as headsets, DVD, game consoles, etc

ARM Classic and Cortex Cores

- Classic –for computer applications
- Cortex -Very wide range of scalable performance options
  - Cortex-M
    - microcontroller cores for a wide range of embedded applications
  - Cortex-R
    - high-performance cores for real-time applications
  - Cortex-A
    - application processor cores for a performance-intensive systems

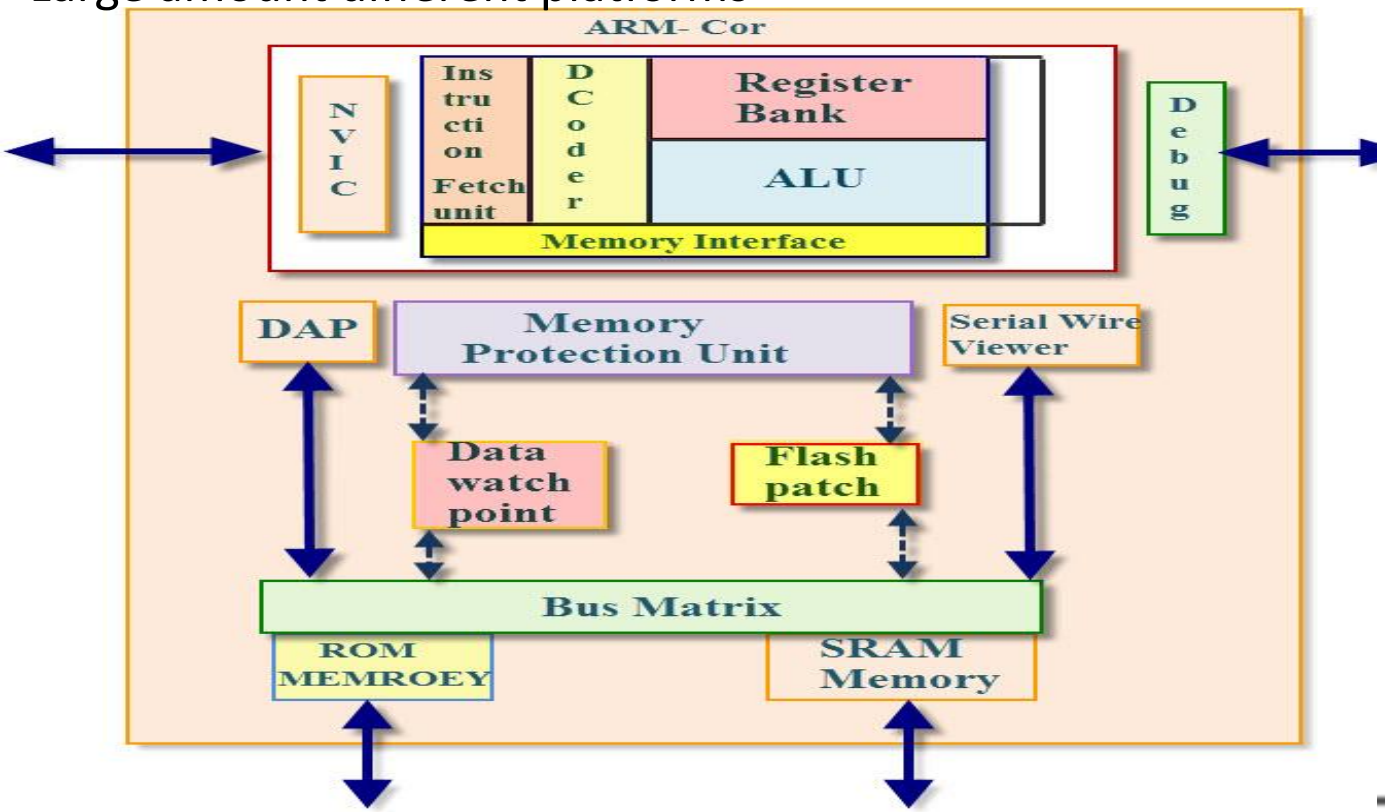
Embedded Processors



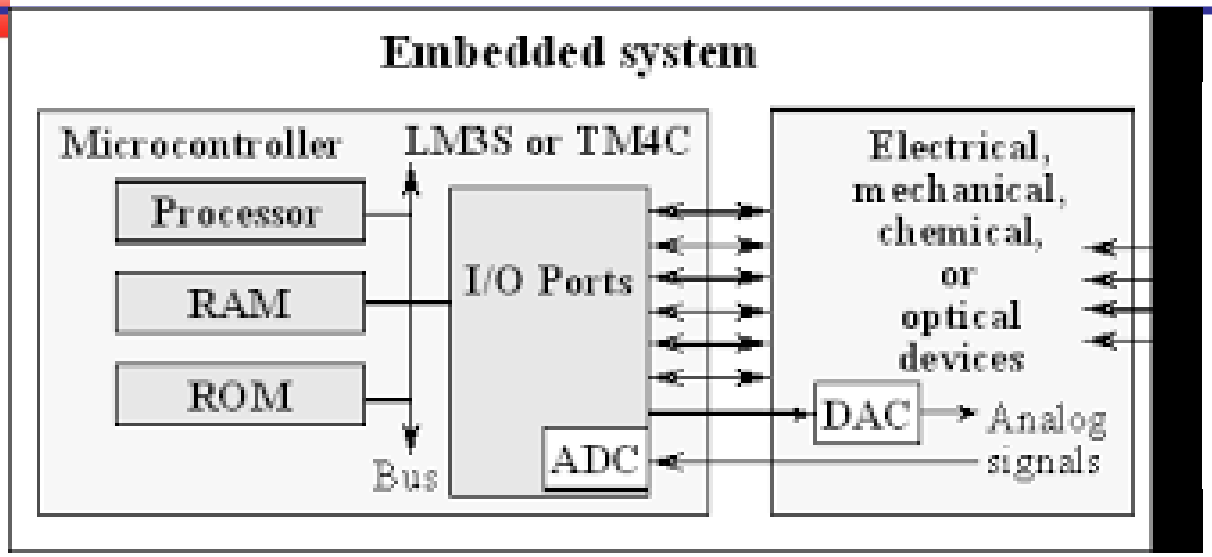
Embedded System Requirements

Microprocessor-based computer hardware system with software that is designed to perform a dedicated function

- Simple calculation
- Small size memory
- Large amount different platforms



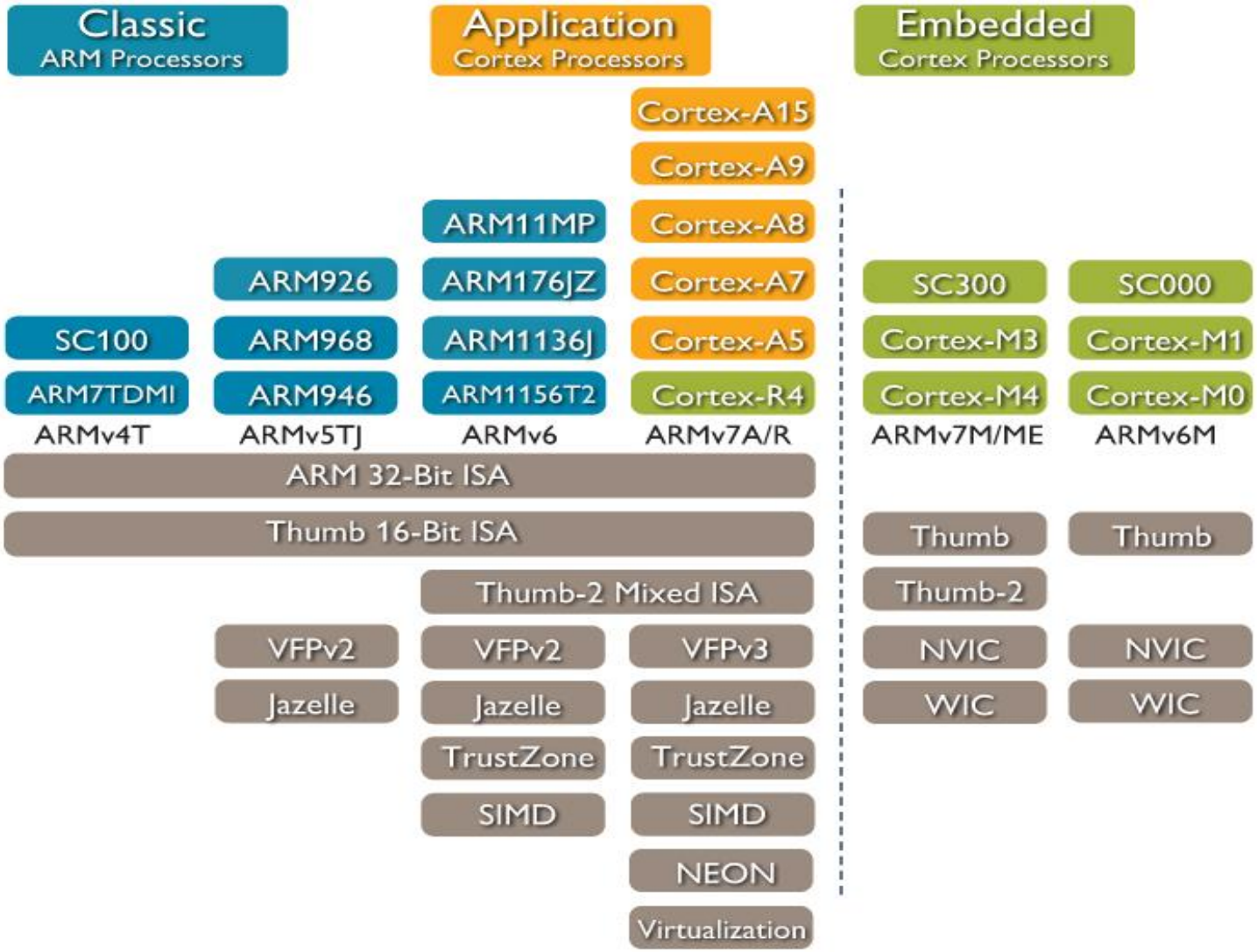
Embedded System with ARM core



arm
CORTEX®-M4

Nested vectored interrupt controller		Wake-up interrupt controller	
CPU Armv7-M			
Memory protection unit		DSP	FPU
3x AHB-Lite	ITM trace	Data watchpoint	JTAG
	ETM trace	Breakpoint unit	Serial wire

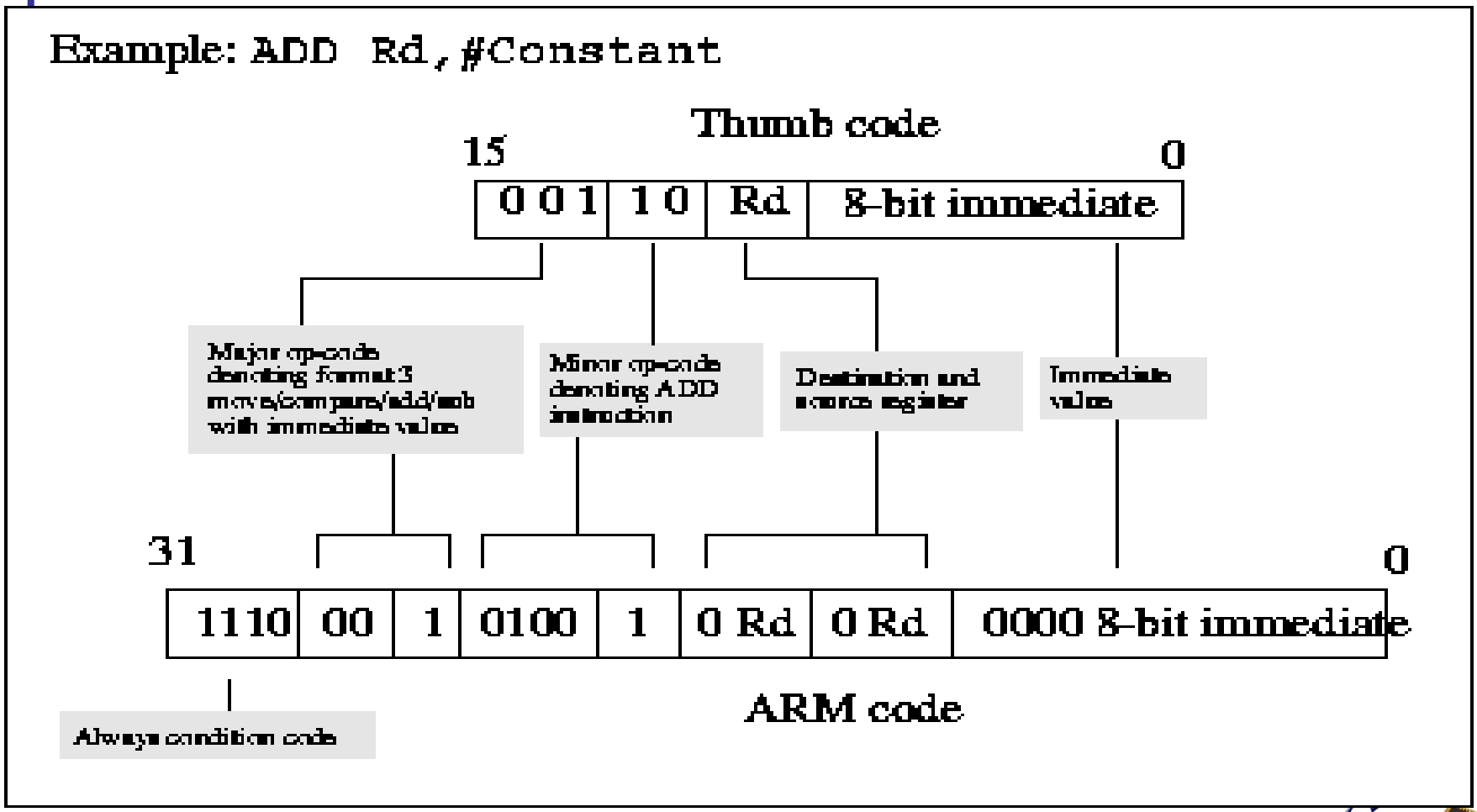
Which architecture is ARM processor?



Thumb 16-bit ISA

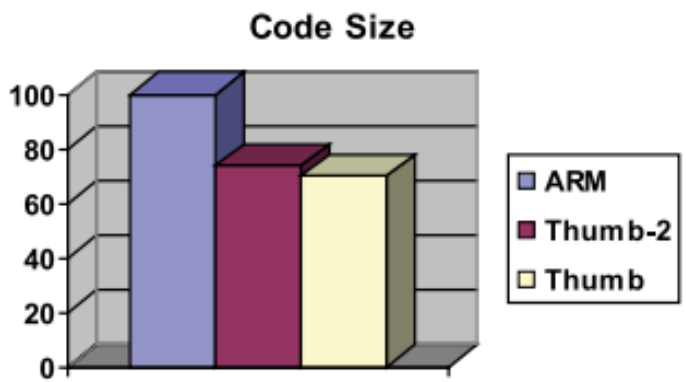
- Why
  - Limited instruction memory in embedded system
  - Code density
  - Smaller size instruction to do the same job
- What is thumb?
  - ISA (Instruction Set Architecture)
  - 16-bit
  - Independent of 32-bit ARM instructions
- Thumb
  - Improve compiled code-density
  - Processors since the ARM7TDMI have featured the **Thumb** Instruction set state

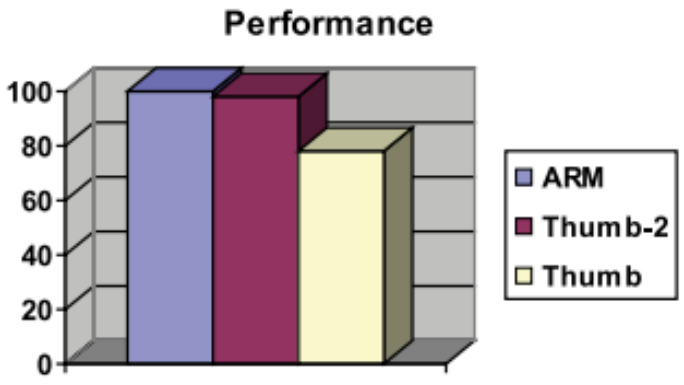
Comparison of ARM and Thumb ISA



Thumb/Thumb-2 Technology

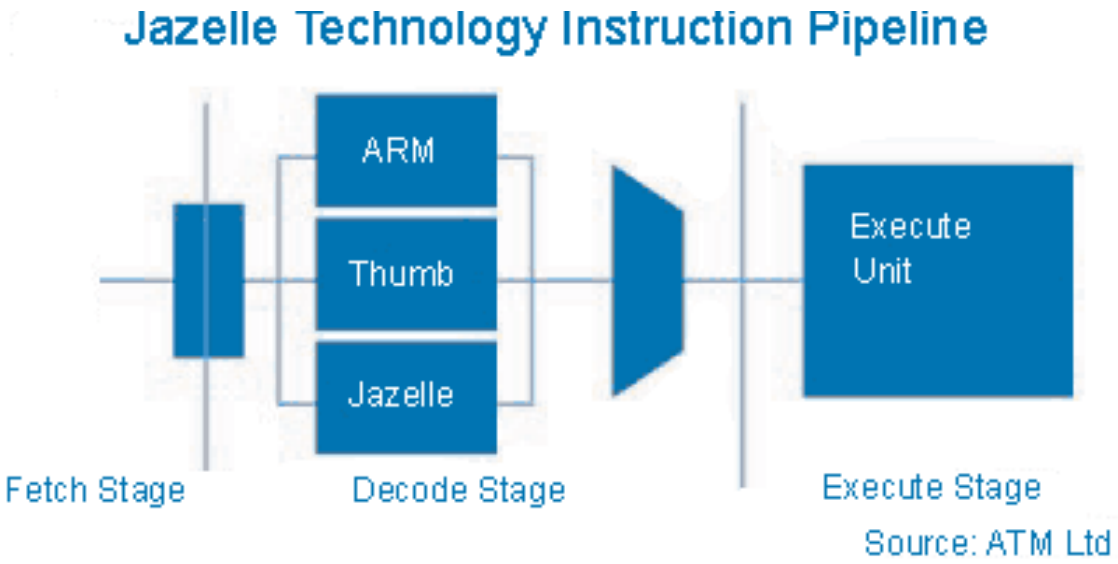
- Thumb-2 ISA
  - A superset of the Thumb instruction set
  - **32-bit** instructions that are intermixed with the 16-bit instructions/without Thumb state
  - Covers almost all the functionality of the ARM instruction set
  - Thumb-2 technology made its debut in the ARM1156 core
- ThumbEE (Thumb Execution Environment)
  - For Limbo, Java, C#, Perl and Python





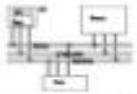
Jazelle

- Jazelle
  - Java Bytecode is the instruction set of the Java virtual machine
  - Java byte code suitable for different hardware platforms
  - Jazelle DBX (Direct Bytecode eXecution)
    - ARM1025EJ-S
    - **Execute Java bytecode in hardware** as **a third execution state** alongside the existing ARM and Thumb modes.



ARM/Thumb/Jazelle

Instruction sets



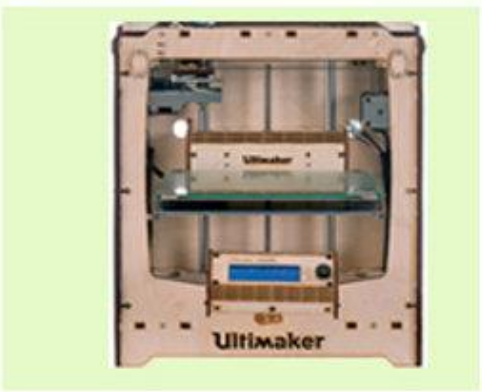
- ARM/Thumb/Jazelle

	ARM (*cpsr* $T = 0$)	Thumb (*cpsr* $T = 1$)
Instruction size	32-bit	16-bit
Core instructions	58	30
Conditional execution[a]	most	only branch instructions
Data processing instructions	access to barrel shifter and ALU	separate barrel shifter and ALU instructions
Program status register	read-write in privileged mode	no direct access
Register usage	15 general-purpose registers +*pc*	8 general-purpose registers +7 high registers +*pc*

	Jazelle (*cpsr* $T = 0, J = 1$)
Instruction size	8-bit
Core instructions	Over 60% of the Java bytecodes are implemented in hardware; the rest of the codes are implemented in software.

Enterprise System-Real time applications

Robot arm - detects object distance/position (complex computation)
- control robot movement (real time requirement)



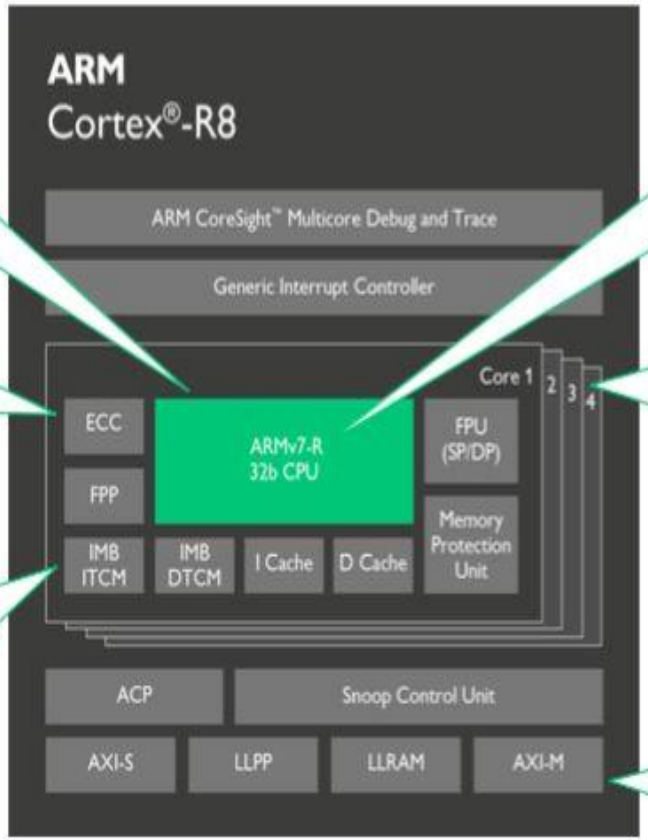
Enterprise System ARM Architecture

Cortex-R8: Advanced Real-Time, High-Performance

Leading edge performance
- Quad cores with superscalar out-of-order execution
- Advanced 11-stage pipeline

Reliability support
- Enhanced fault detection and control – MPU, ECC, DCLS

Rapid responsiveness
- Large Tightly-Coupled Memory up to 2 MB per core
- Predictable low-latency access
- Hard real-time determinism



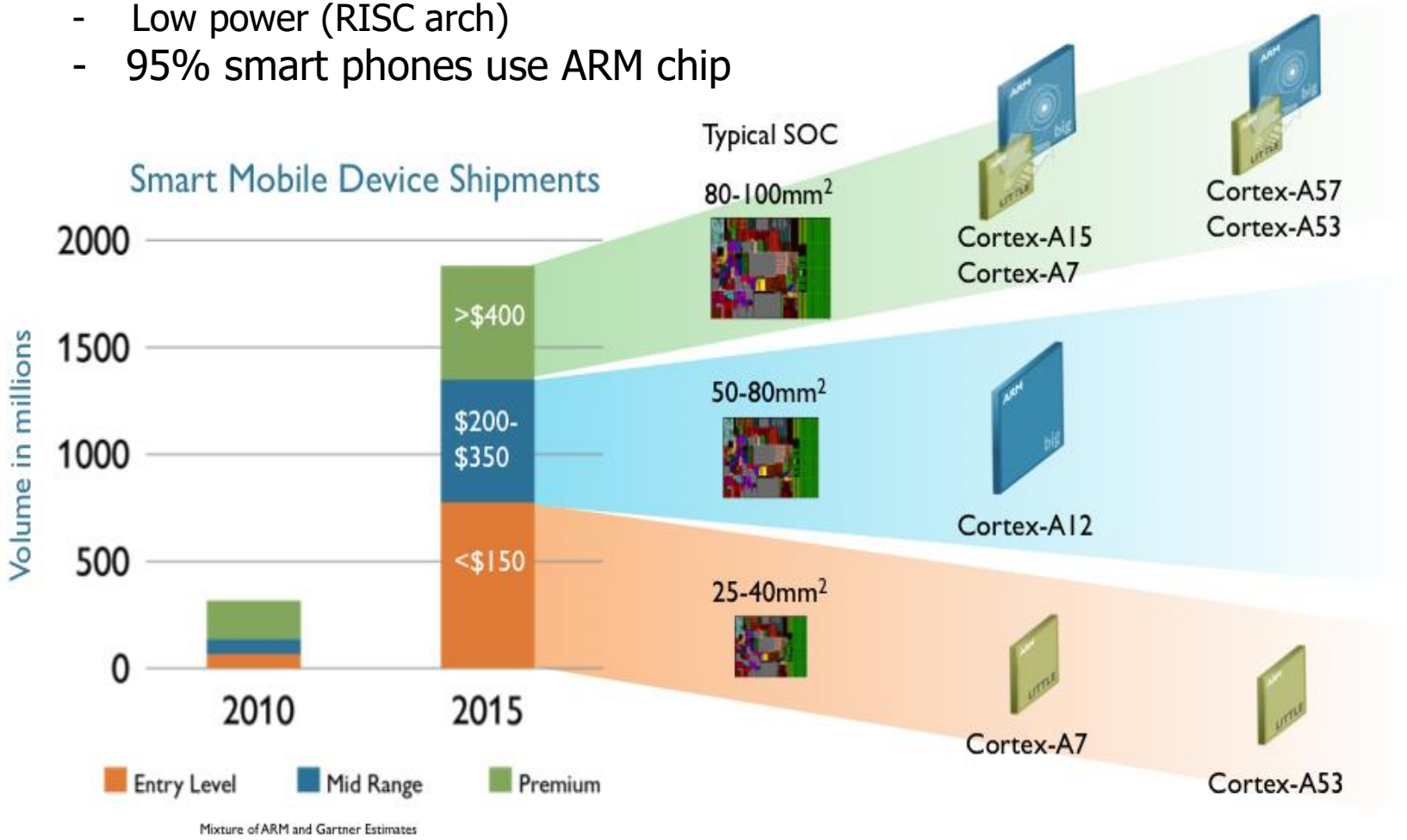
Software compatibility
- Modem software and system level design and simulation assets built around ARMv7-R

Scalability
- Option from one to four cores
- Exploit workload parallelism
- Power down individual cores according to workload

Extensibility
- Rich set of interface ports
- Coherent integration with closely coupled accelerators

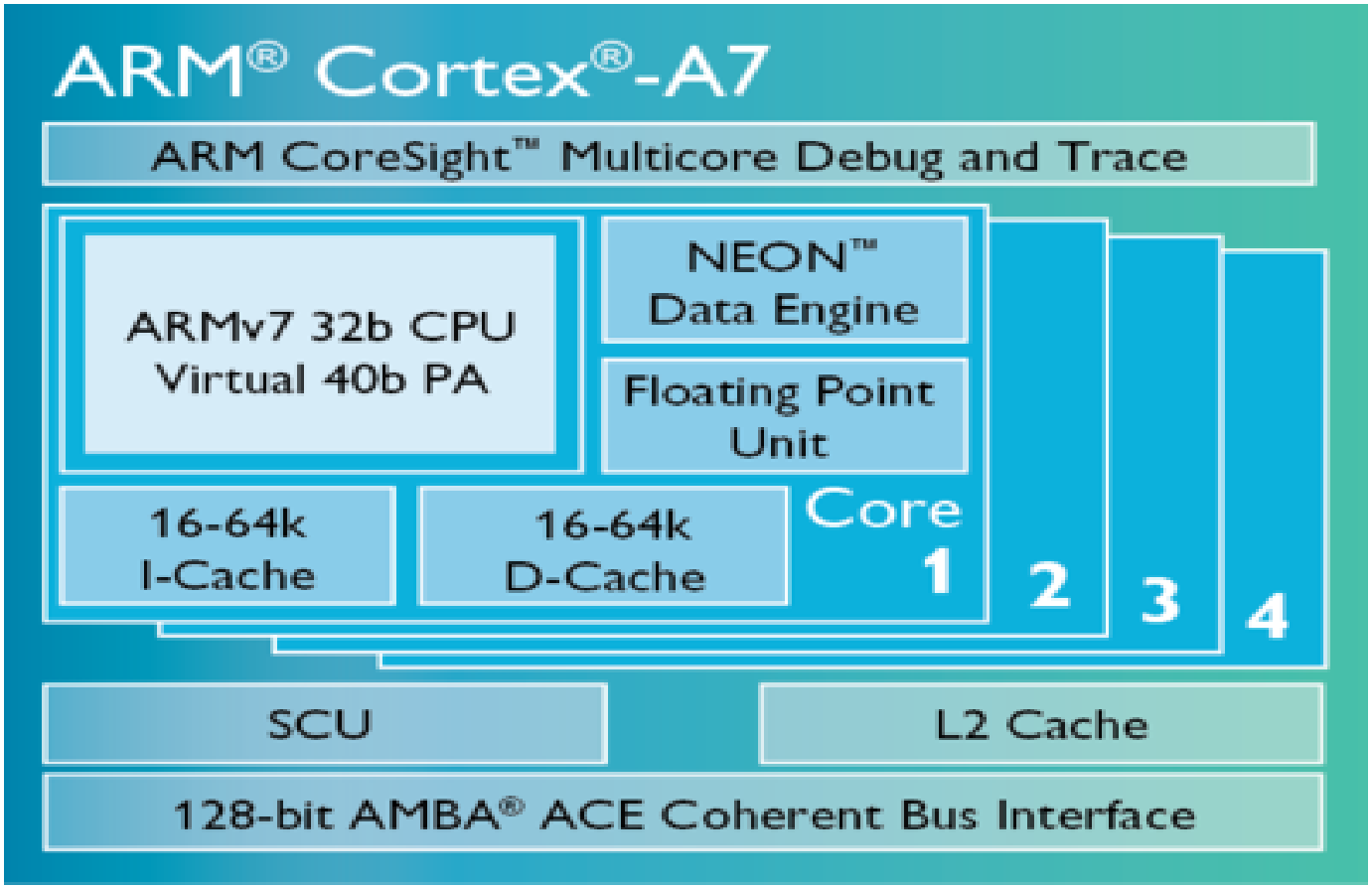
Mobile -Applications

- Multi-tasking (Multimedia/texting/voice call –heterogeneous core)
- Multimedia (NEON)
- Low power (RISC arch)
- 95% smart phones use ARM chip



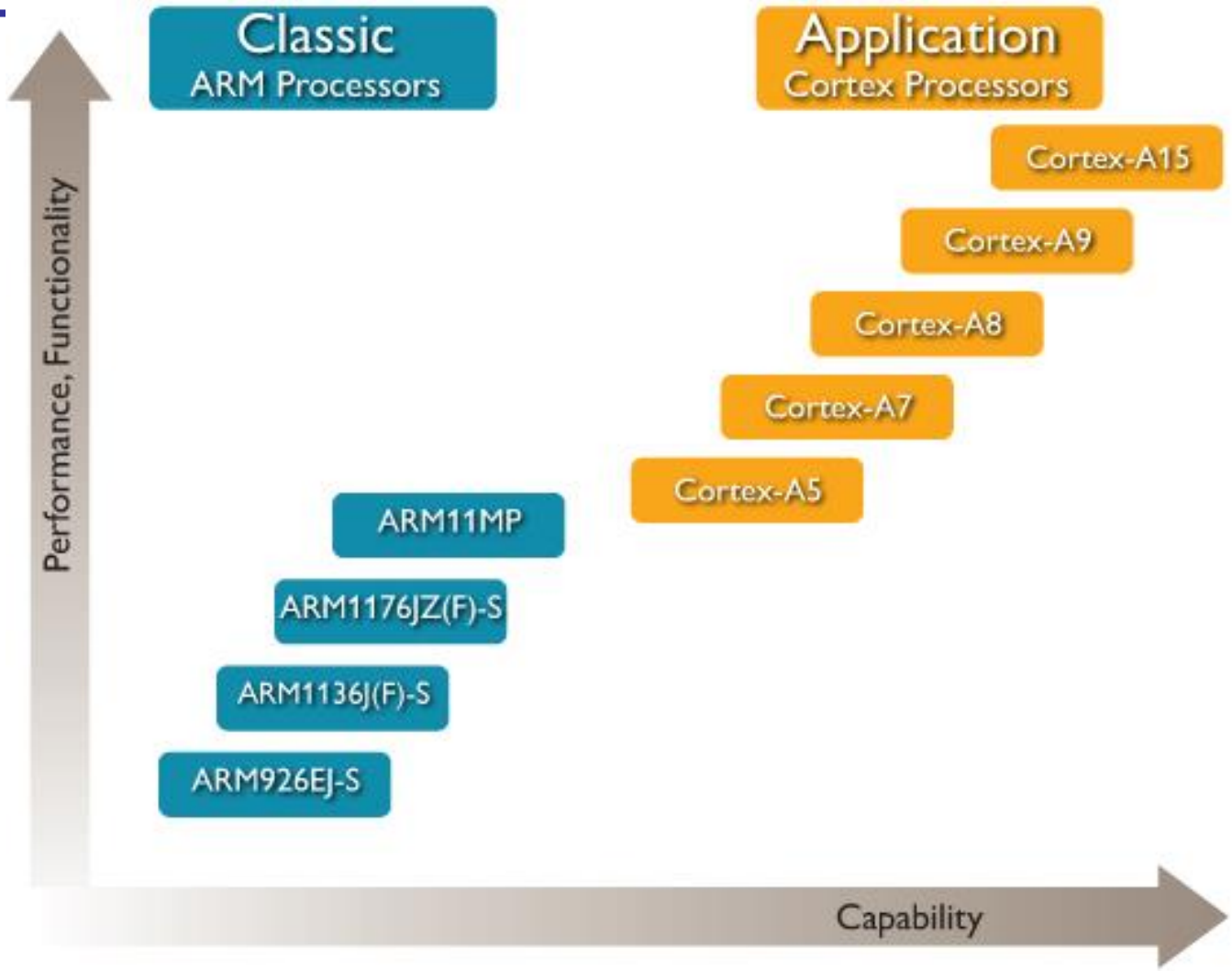
Mobile System ARM Architecture

- Cortex A7-Multicore architecture with NEON Data engine



https://www.phytec.eu/cn-in-product/som/cortex-a7/

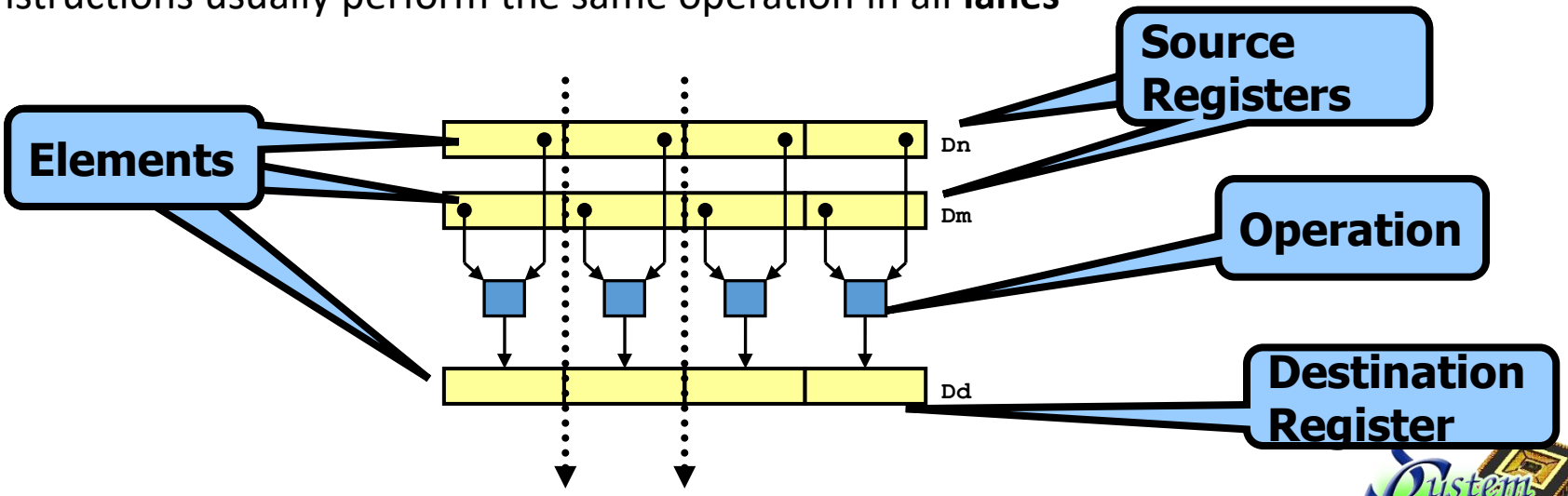
Application Processors



What is NEON?

- NEON is a **wide** SIMD data processing architecture
  - Extension of the ARM instruction set (v7-A)
  - 32 x 64-bit wide registers (can also be used as 16 x 128-bit wide registers)

- NEON instructions perform “Packed SIMD” processing
  - Registers are considered as **vectors** of **elements** of the same data type
  - Data types available: signed/unsigned 8-bit, 16-bit, 32-bit, 64-bit, single prec. float
  - Instructions usually perform the same operation in all **lanes**



NEON

- Advanced SIMD (NEON)
  - A combined 64- and 128-bit single instruction multiple data (SIMD) instruction set
  - Provides standardized acceleration for media and signal processing applications
  - NEON
    - can execute MP3 audio decoding on CPUs running at 10 MHz
    - can run the GSM AMR (Adaptive Multi-Rate) speech codec at no more than 13 MHz

Data Sizes and Instruction Sets

- ARM is a 32-bit load / store RISC architecture
  - The only memory accesses allowed are loads and stores
  - Most internal registers are 32 bits wide
  - Most instructions execute in a single cycle
- When used in relation to ARM cores
  - **Halfword** means 16 bits (two bytes)
  - **Word** means 32 bits (four bytes)
  - **Doubleword** means 64 bits (eight bytes)
- ARM cores implement two basic instruction sets
  - **ARM** instruction set – instructions are all 32 bits long
  - **Thumb** instruction set – instructions are a mix of 16 and 32 bits
    - **Thumb-2** technology added many extra 32- and 16-bit instructions to the original 16-bit Thumb instruction set
- Depending on the core, may also implement other instruction sets
  - **VFP** instruction set – 32 bit (vector) floating point instructions
  - **NEON** instruction set – 32 bit SIMD instructions
  - **Jazelle-DBX** - provides acceleration for Java VMs (with additional software support)
  - **Jazelle-RCT**(Runtime Compilation Target)- based on ThumbEE mode and supports ahead-of-time(AOT) and just-in-time (JIT) compilation with Java and other execution environments. - provides support for interpreted languages

Architecture ARMv7 (32-bit ISA) profiles

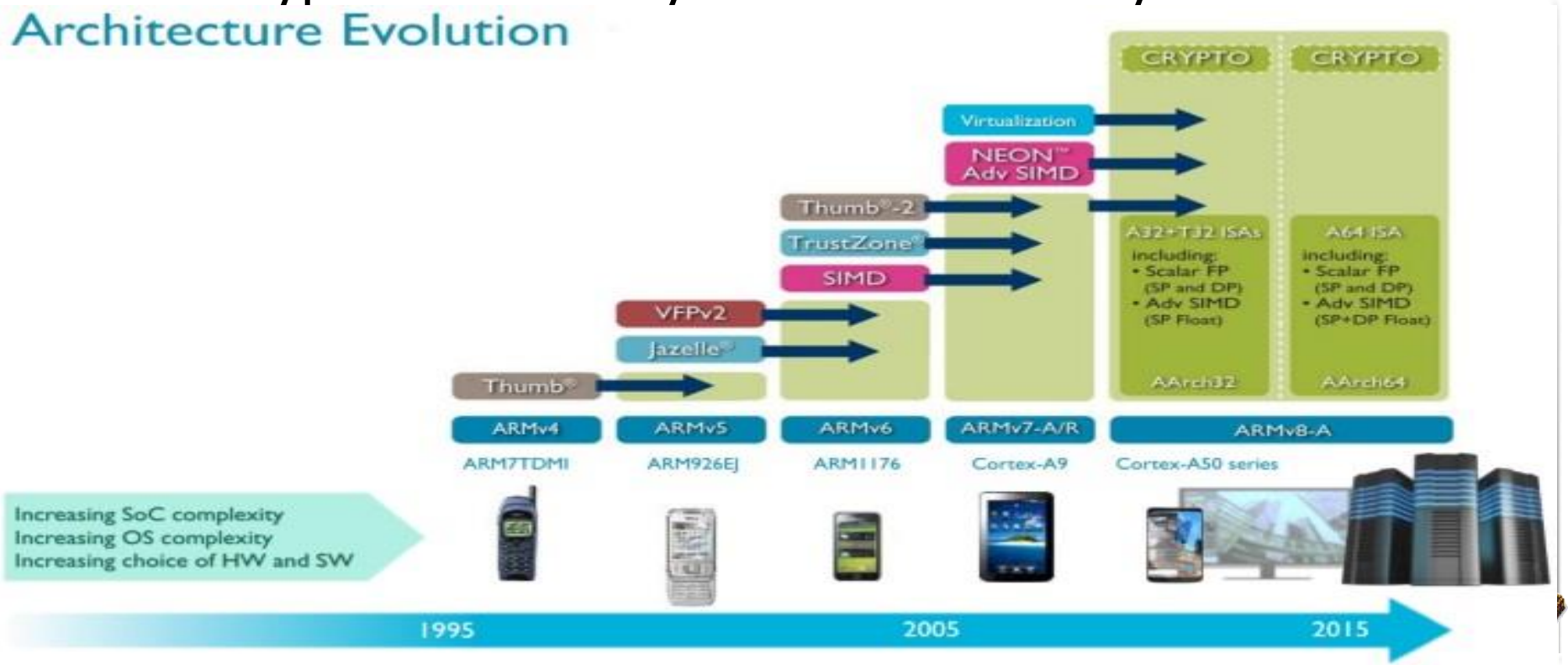
- Application profile (ARMv7-A)
  - Memory management support (MMU)
  - Highest performance at low power
    - Influenced by multi-tasking OS system requirements
  - Trust Zone –to isolate security components in a system by separating physical system into two virtual system: one for rich operating system the other for secure operation system
  - Jazelle-RCT for a safe, extensible system
  - e.g. Cortex-A5, Cortex-A9

- Real-time profile (ARMv7-R)
  - Protected memory (MPU)
  - Low latency and predictability 'real-time' needs
  - Evolutionary path for traditional embedded business
  - e.g. Cortex-R4

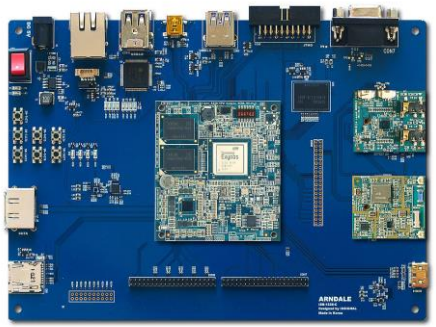
- Microcontroller profile (ARMv7-M, ARMv7E-M, ARMv6-M)
  - Lowest gate count entry point
  - Deterministic and predictable behavior a key priority
  - Deeply embedded use
  - e.g. Cortex-M3

ARMv8-A (for high end smart phones/ PC)

- 64-bit/32-bit ARM CPU
  - Compatible with ARMv7-A/R
  - Adv. SIMD (4x128b or 2x128b)
  - Crypto for security such as AES encrytion



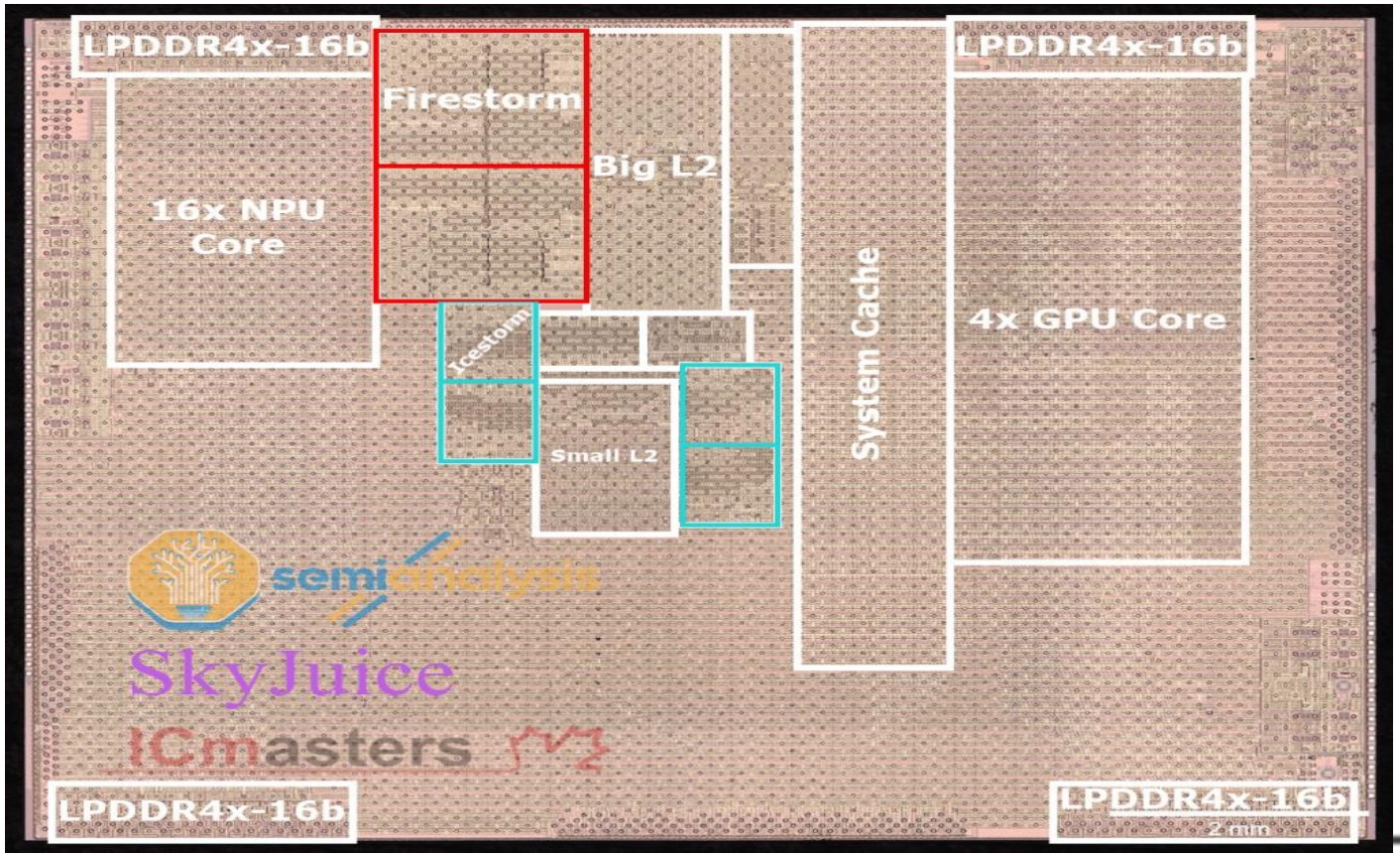
High End Smart phone



- Cortex-A32../Firestorm/Icestorm
  - Decode (2-wide,..8-wide(firestorm), 6-wide(icestorm)
  - Pipeline depth (8-16)
  - 3~12-stage out-of-order pipeline

Apple A14 Bionic ARMv8.5-A

- **Apple A14 Bionic** is a 64-bit ARMv8.5-A[5] system on a chip (SoC)
- iPhone 12 / iPad
- Two Firestorm (Armv8.5-A) CPU (red box)
- Four Icestorm (Armv8.5-A) CPU (green box)



Apple M1 Max Chip

M1 Max

- Apple M1 Max (announces Oct. 18/2021)
  - Eight performance cores
    - 192 KB of L1 instruction cache and
    - 128 KB of L1 data cache and share a 12 MB L2 cache
  - Two efficiency cores
    - 128 KB L1 instruction
    - cache, 64 KB L1 data cache, and a shared 4 MB L2 cache.
  - 24 to 32 GPU cores
    - 16MB System Level shared Cache
  - 16 Neural Engine cores
  - 64GB unified RAM with 400GB/s memory bandwidth
  - 57 billion transistor
  - Support 7 streams 8K videos

Conclusion

- ARM is a trend.
  - An ARM ecosystem have been created
  - ARM is seen everywhere in our daily life.

Reference

- http://www.arm.com/
- http://www.androidauthority.com/intel-readying-serious-contender-for-use-in-android-devices-in-2012-39524/
- http://www-cs-faculty.stanford.edu/~eroberts/courses/soco/projects/2000-01/risc/risccisc/
- http://news.cnyes.com/content/20110826/KDYNZBJB0O23I.shtml
- http://www.technolog.msnbc.msn.com/technology/technolog/china-overtakes-us-largest-smartphone-market-118874
- http://www.dazeinfo.com/2011/12/15/global-smartphone-penetration-2011/
- http://en.wikipedia.org/wiki/Porter_five_forces_analysis
- http://gigaom.com/mobile/arm-vs-intel-just-starting-or-already-over/
- http://tech.hexun.com.tw/2011-10-07/133967251.html
- http://www.eetimes.com/electronics-news/4234459/ARM-customers
- http://www.heyrick.co.uk/assembler/riscvcisc.html
- http://zh.wikipedia.org/wiki/ARM%E6%9E%B6%E6%A7%8B