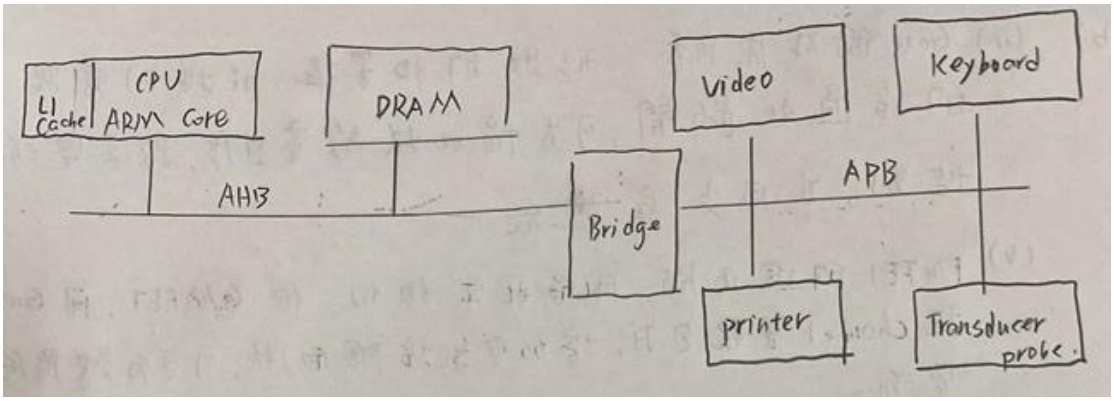
Introduction to System-on-Chip and its Applications

Test 1 11/14/2022

1. Leakage current is a big problem in nano technology node.
   (a) (2%) Which of the following can be used to reduce leakage current (i) low-k dielectric (ii) FinFET (iii) Silicon on Insulator (SOI) (iv) immersive lithography (v) Gate All Around FET
   (ii) (v)
   (b) (2%) For the selected items in (a), explain their function principle to reduce leakage
   在 FinFET 的架構中，gate 做成類似魚鰭的叉狀 3D 架構，可於電路的兩側控制電路的接通與斷開。
   這種設計可以大幅加快充放電速度，改善電路控制並減少漏電流，也可以大幅縮短電晶體的 gate length。
2. (4%)(a)What are the two building components to build SOC rapidly? Describe their definitions.
   IP, Platform
   (4%) (b) List one example for each the building components in (a).
   IP: USB
   Platform: AMBA
   (2%) Describe the difficulty of integrating the DRAM with the CMOS logic in semiconductor process.
   從 DRAM 的結構上可以發現，其組成元件有電容的存在。困難的地方在於，電容的製程當中，必須要從晶圓表面上向下挖溝擴大表面積，以增加電容量。這與邏輯電路由晶圓表面向上堆砌恰好相反，使其整合的技術困難。
3. Given the following components of an ultrasonic medical image system,
   (a) Video output interface
   (b) Microcontroller CPU architecture
   (c) Support DDR III DRAM
   (d) L1 Cache
   (e) printer
   (f) keyboard
   (g) Transducer probe

   (2%) (i) Which of the microcontroller will be preferred? (b1) intel i7 (b2) ARM.v4M (b3) intel i9 (b4) ARM.v4R
   (b4)

(4%) (ii) Draw a SOC platform of the required module components based on the requirement item number with different kind of on-chip bus (AMBA based) that contains the required module components. (要把 a-g 畫進去)



4. (2%)(a) For the application of weather forecast simulations, which of the following CPU are preferred? (i) intel 8-core sandy bridge CPU (ii) ARM.v5R (iii) ARM.v6A (iv) Nvidia GK 110

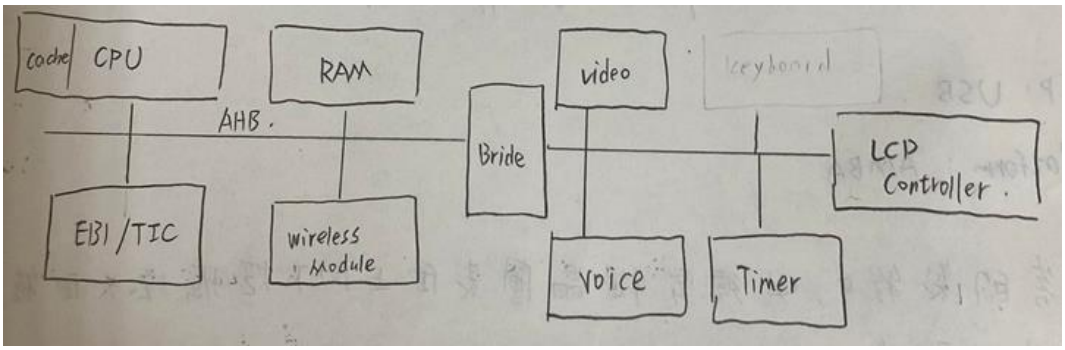
   (i)

   (2%) (b) which of the following L1 cache capacity is preferred (i) 4kB (ii) 1MB (iii) 512KB (iV) 1GB

   (iii) 64KB per core.

   64*8 = 512KB

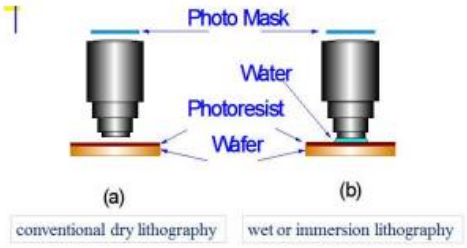
   (4%) (ii) Draw a SOC platform of including CPU, cache, and other required components with different kind of on-chip bus (AMBA based) that contains the required module components.



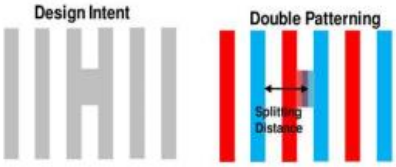
5. For the three technologies, immersion technology, double patterning, and extreme Ultraviolet, used in the lithography under submicron to reduce the transistor dimension,

   (a) (3%) Describe the operating principles for these three technologies.

Immersion lithography: The liquid medium that has a refractive index greater than one is between the final lens and the wafer surface.

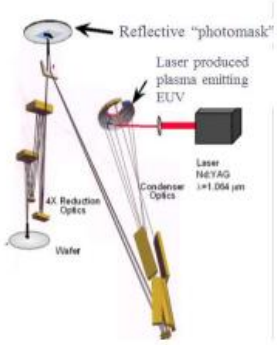


Double pattering lithography:一種將會佈局分割為兩個或多個以上各別光罩的技術，如Pitch Splitting(或稱Litho-Etch-Litho-Etch, LELE)，將原始繪製的多邊形切割為多塊並縫合在一起的不同方式，以提供更多的分解選項。



Extreme UV Lithography (13nm wavelength)

Extreme Ultraviolet lithography: It works by burning intense beams of ultraviolet light that are reflected from a circuit design pattern into a silicon wafer.

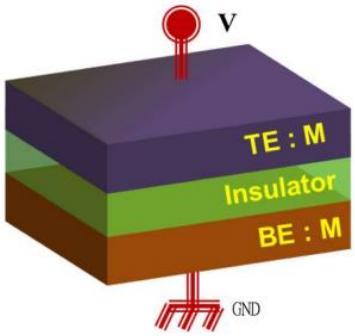


(b) (3%) Using a table to show their pros and cons of these three technologies.

Techniques	Immersion	Double Patterning	Extreme Ultraviolet
Advantages	- Blurriness is reduced. - Enhance the resolution.	- Enhance the feature density.	- Offer higher resolution.
Disadvantages	- Tolerance in wafer topography flatness is reduced compared to the corresponding "dry" tool at the same resolution.	- Design restrictions. - High cost. - Alignment issues.	-Price is expensive.

6. (4%) Draw a diagram to describe the principle of storing bit in the following memory: (a) Resistive RAM (b) Floating Gate Flash (c) Harddisk Drive.

(a) 利用上下兩層金屬電極中夾的一層特別的絕緣材料(過渡金屬氧化物)，絕緣材料的電阻值會隨著所加偏壓改變而產生不同的電阻值，利用電阻改變儲存資料。



(b)

當我們應用 FN 穿隧的原理來操作浮動閘極元件，於閘極施加正電壓，則會使源極(Drain)的電子穿過穿隧氧化層(Tunnelling Oxide)到達浮動閘極(Floating Gate)，若此時停止施加電壓，則電子將會被侷限在穿隧氧化層和控制氧化層之間的位能井內。相反地，於閘極施加負電壓，則會將浮動閘及內的電子趕回源極去。

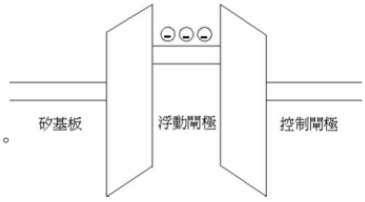
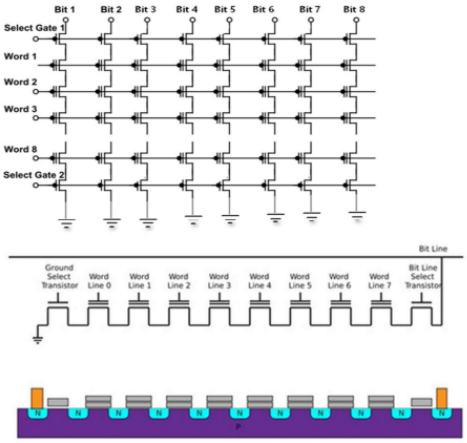
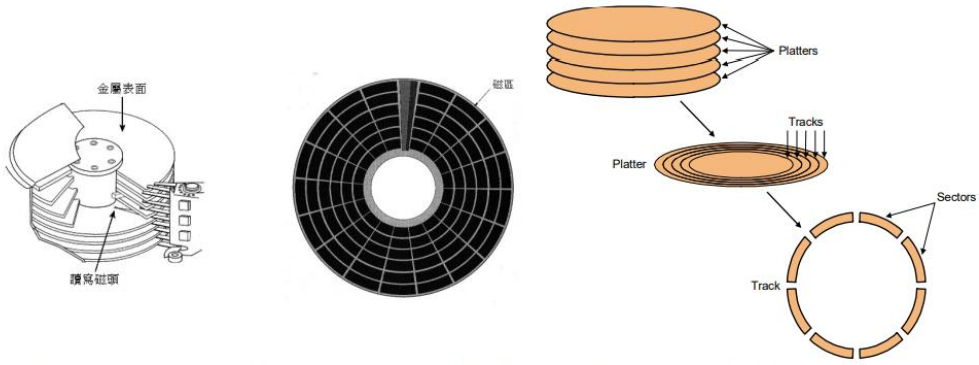


圖 1-11 電子侷限在二氧化矽位能井中。



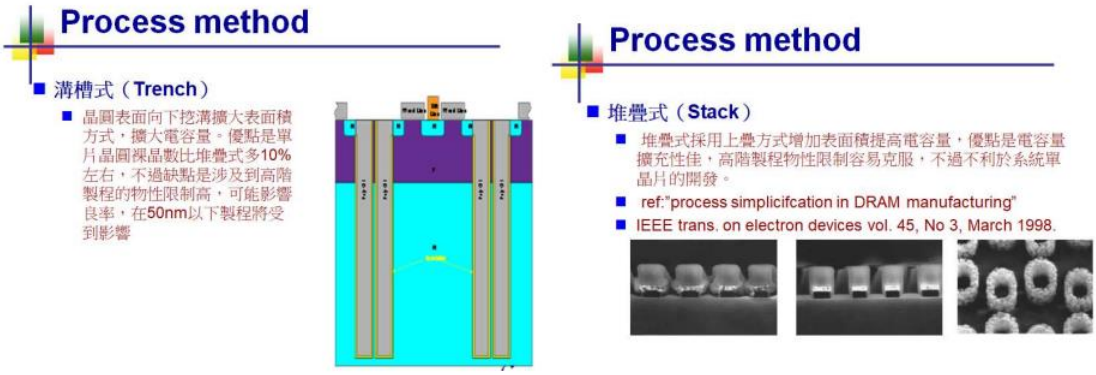
由左圖可見每個Bit Line下的基本存儲單元是串聯的，NAND讀取數據的單位是Page，當需要讀取某個Page時，FLASH 控制器就不在這個Page的Word Line施加電壓，
而對其他所有Page的Word Line施加電壓（電壓值不能改變Floating Gate中電荷數量），
讓這些Page的所有基本存儲單元的D和S導通，而我們要讀取的Page的基本存儲單元的D和S的導通/關斷狀態則取決於Floating Gate是否有電荷，
有電荷時，Bit Line讀出 ‘0’，無電荷Bit Line讀出 ‘1’，實現了Page數據的讀出，可見NAND無法實現位讀取（即Random Access），進程代碼也就無法在NAND上運行。

(c)



- 一堆同圓心軸的金屬碟，它們已經被磁化的了。所有的資料都是記錄在這些光滑的金屬碟表面之上
- 每個金屬磁片通常都有兩面，每一面都有其各自的讀寫磁頭(Head)一個
- 金屬磁碟旋轉，磁頭不移動的在表面相對所畫出來的一圈，可以說是一個磁軌(Track)。
- 那麼從圓心向外以一定距離進行量度，將所有表面上的相同圓周的磁軌從上到下疊起來，抽象地看就是一個磁柱(Cylinder)了。
- 由圓心開始，在同一表面上分別畫出無數條半徑，然後每兩條半徑所分割的磁軌，我們稱為磁區(Sector)。每一磁區"通常"會可攜帶 512byte(0.5KB)的資料
- Magnetic polarity to present data pattern

7. (a) (2%) Which of the following memory are suitable for storing MP3 data?
   (i) DRAM (ii) NOR Flash (iii) NAND Flash (iv) ROM
   (iii)
   (b) (4%) For the answer in (a), describe the memory structure and why the structure is suitable for the application.
   因為此架構具備 high speed serial access(音樂通常存取 serial access)的特性然後價格便宜
   (c) (2%) What is disadvantage of the answer in (a)?
   Slow random access
   (d) (2%) What kind of approach can be used to release the problem in (c)? Describe its operation principle.
   寫入用 NOR,讀取用 NAND
8. (2%) Which of the following are hard IPs in a SOC? (a) RTL DSP core (b) technology specific JTAG (c) gate level ARM (d) polygon level JPEG.
   (b)(d)
9. (4%) Describe the pro and con of stack and trench semiconductor process. Schemes for DRAM.



10. (a) (2%) Which of the following memory is suitable for IoT device? (a) NOR Flash (b) NAND Flash (c) RRAM (d) MRAM

    (a)(b)(c)(d)

    (b) (4%) For the answer in (a), describe the operation principle and the reason for this application.

    (a)(b) 有 high speed serial access, 價格便宜

    (c)讀寫速度快

    (d)讀寫速度很快，且是 nonvolatile

11. (4%) List the advantages and disadvantages of the CISC and RISC processors in terms of instruction type, instruction execution time, hardware complexity, addressing mode and compiled object code complexity.

	CISC	RISC
1	Complex instructions taking multiple cycles	Simple instructions taking 1 cycle
2	Any instruction may reference memory	Only LOADS/STORES reference memory
3	Not pipelined or less pipelined	Highly piplined
4	Instructions interpreted by the microprogram	Instructions executed by the hardware
5	Variable format instructions	Fixed format instructions
6	Many instructions and modes	Few instructions and modes
7	Complexity in the microprogram	Complexity is in the compiler
8	Single register set	Multiple register sets

    (2%) Which of the following methods can be used to increase operation per second for intel single core CPU? (a) Stream SIMD (b) Hyper Threading (c) turbo boost (d) ring interconnect

    (a)(b)(c)

12. (4%) Describe the operation principle of (i) Channel Hot Electron, (ii) FN tunneling in Flash to inject and erase electrons to floating gate.

    (2%) Describe the operation principle on how to read the store data as one or zero

from floating gate transistor.

- (1)
  - (i)通道熱電子編程(Channel Hot Electron，CHE)』，該方法通過對控制閘施加高電壓，使傳導電子在電場的作用下突破絕緣體的屏障進入到浮閘內部，反之亦然，以此來完成寫入或者抹除動作。
  - (ii)『Fowler-Nordheim(FN)隧道效應法』，它是直接在絕緣層兩側施加高電壓形成高強度電場，幫助電子穿越氧化層通道進出浮閘

- (2)

The logical "0" or "1" is sensed by
whether a current through the transistor
when an intermediate voltage is on the CG.
Once the FG is charged->
increasing the threshold voltage (VT1) of the cell.
A higher voltage(VT2) on the CG to make the channel conductive.
At read, an intermediate voltage between the threshold voltages (VT1 & VT2) is applied to the CG.
If conducts, then 0 is stored.
If unconducts, then 1 is stored

13. (4%) Describe what kind of technology and its function principle used in intel core to solve the problem of data transfer bottleneck between CPU and main memory.

    Cache.

    利用 cache 將常用 data 放在 cpu, 減少外部記憶體存取。

14. (4%) Describe the operation principle of SRAM based in-memory computing.

    SRAM 有 high-performance multimedia 與 low-power consumption 特性, simple read 造就 fast access, 可以讓 cpu 在做運算時，直接在 SRAM 裡面運算即可。

15. (2%) (a) Provide the reason that the SSD controller and the NAND Flash does not in a single SOC?

    SSD controller: 負責 read/ write.

    NAND Falsh: 負責 store.

    資料經過 controller 之後才會寫入 NAND 保存。

    (2%) (b) Provide the reason that the CPU and the DRAM does not fabricate in a single SOC?

    CPU 是屬於 logic，與 DRAM 製成不一樣。

16. (4%)(a) Which of the following ARM ISA is suitable for smart card applications?

    (i) thumb ISA (ii) jazelle ISA (iii) VFP (iv) NEON

    (b) describe the operation principle and the reason for this application.

    有寫出合理原因都可以

17. (4%) (a) Which of the following ARM architecture is suitable for high end smart phone applications? (i) ARMv4.M (ii) ARMv5.R (iii) ARMv6.A (iv) ARMv7.A

    (iv)

    (b) describe the main functions in this architecture and the reason for this application.

Low-cost, power-efficiency.

18. (2%) (a) What are three reasons that GPU is more suitable for data training in machine learning applications?
    High bandwidth, Parallels, Faster memory access from cache.
19. (2%) Which of the technology used in Nvidia GPU to increase the data bandwidth transfer between DRAM and GPU (i) HBM2 (high bandwidth memory) (ii) silicon interposer (iii) unified memory architecture (iv) NVLink
    (i)

20. (2%) Which of the technology used in Nvidia GPU so that the memory bandwidth from GPU to registers/L1 Cache is much faster than that of CICS CPU? (i) structural sparsity (ii) tensor core (iii) Multi-Instance GPU (MIG) (iv) HBM2
    (ii)
21. (2%) (a) Which of the following emerging memory is more likely to be market faster (i) RRAM (ii) PCM (iii) MRAM (iv)SSTMRAM (b) describe the reason for each item in the list.
    有寫出合理就可以