Introduction to System-on-Chip
Individual Project Report:

Optical Interconnect

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1. Introduction

1.1 VCSEL introduction

VCSELs are widely used in optical interface like high-speed optical communications, sensing, autonomous vehicles, data storage, next generation computing, etc.

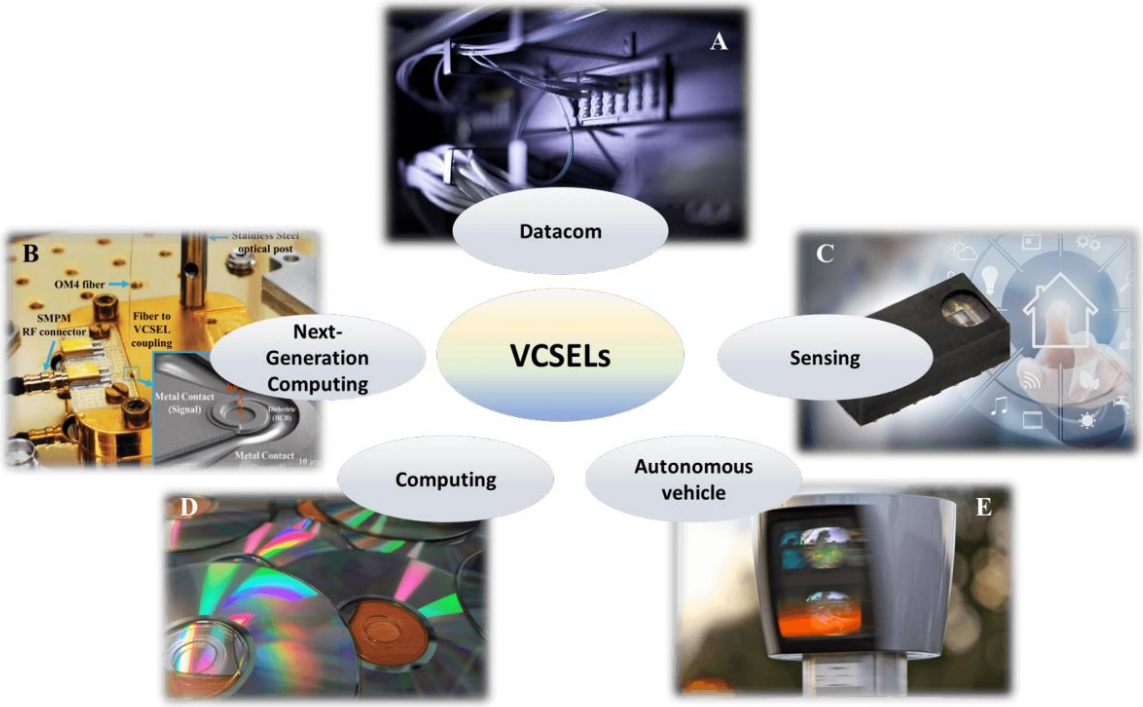


Fig. 1.1

1.2 Data center traffic issue

According to Cisco Global Cloud Index 2016-2021, data center traffic increases approximately 25% per year. In this chart we also can find out that over 70% traffic remains within data center. Therefore, how to speed up transmission rate within a low power

consumption is the main challenge we have to face.

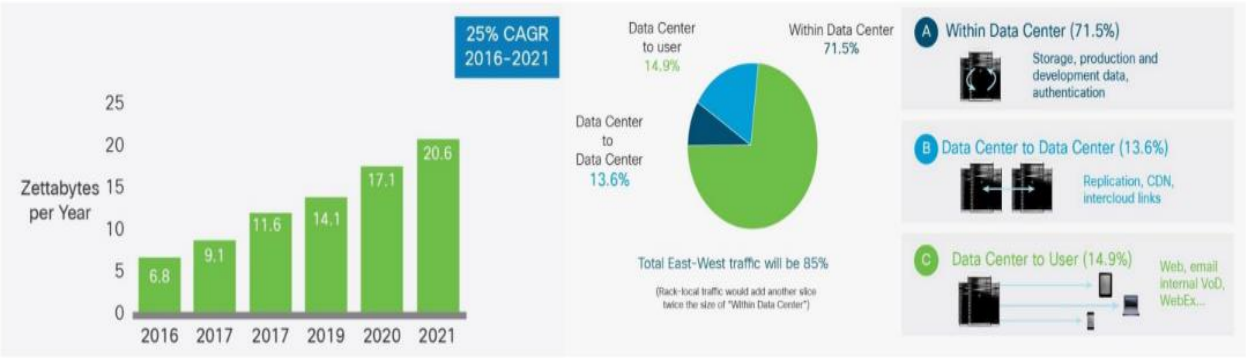
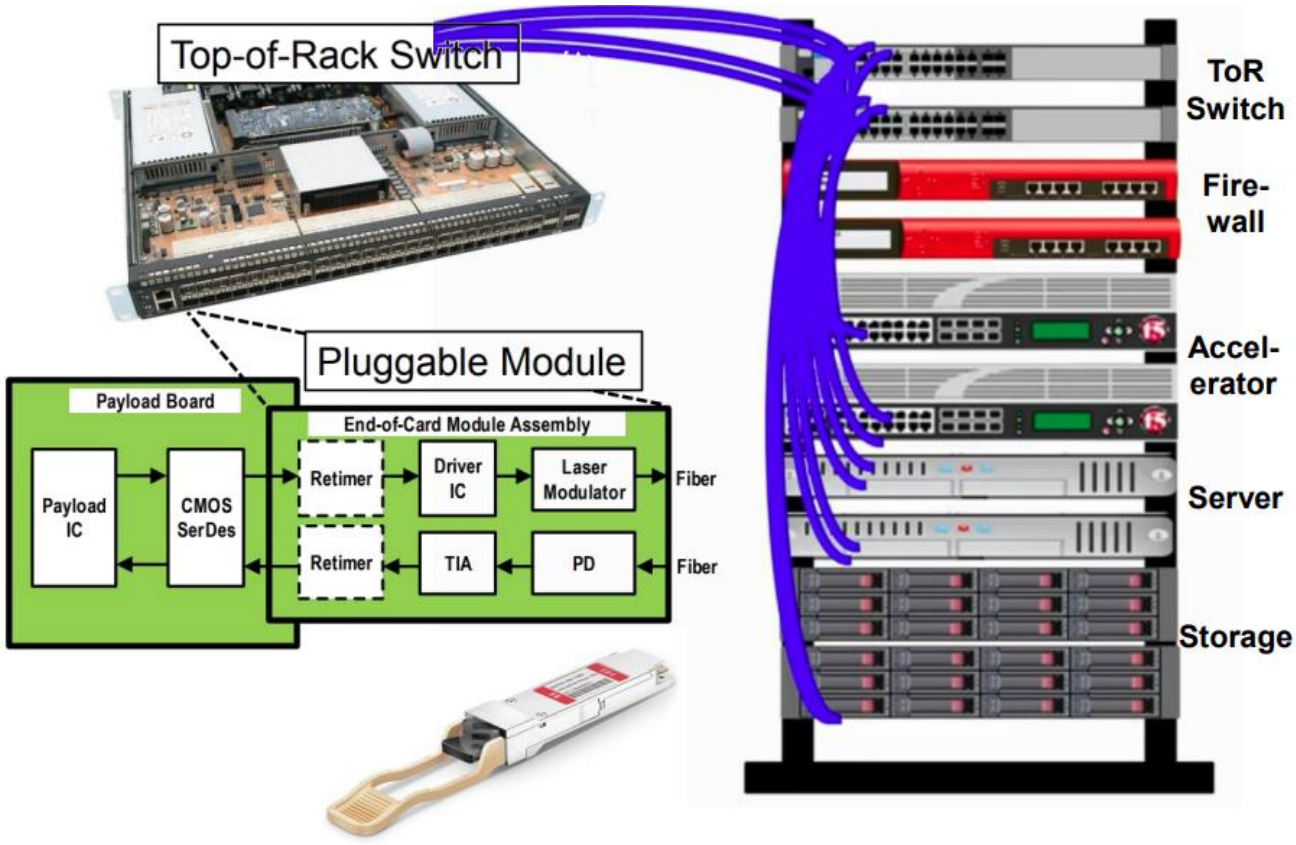


Fig. 1.2

1.3 General data center architecture

The picture below shows the architecture of Top-of-Rack (ToR) switch in the data center.



The data center is composed of several racks as shown in the figure

above. In each rack, a ToR switch is designed at the top of the rack to handle the data reception and transfer between components in order to transfer data between the various functional components.

1.4 IEEE optical transmission standard

Among various types of optical components, VCSEL-based optical links provide a solution for the high-speed short reach links and cost reduction. Meanwhile, according to the standard optical transmission specifications published by IEEE in 2017, each channel needs to achieve 56Gb/s or 56GBd/s to meet the requirement.

IEEE P802.3bs™/D3.0						
Optical 400Gb/s						
Item	**Name**	**Count**	**Ch.**	**Distance**	**Speed**	**Mod.**
1	400GBASE-SR16	16	MM	0.5-100m	26.5625GBd	NRZ
2	400GBASE-DR16	4	SM	2m to 500m	53.125GBd	PAM4
3	400GBASE-FR16	8	SM	2m to 2km	26.5625GBd	PAM4
4	400GBASE-LR16	8	SM	2m to 2km	26.5625GBd	PAM4
Optical 200Gb/s						
Item	**Name**	**Count**	**Ch.**	**Distance**	**Speed**	**Mod.**
1	200GBASE-DR16	4	SM	2m to 500m	26.5625GBd	PAM4
2	200GBASE-FR16	4	SM	2m to 2km	26.5625GBd	PAM4
3	200GBASE-LR16	4	SM	2m to 2km	26.5625GBd	PAM4

Fig. 1.3

2. Wireline Communication Technology

2.1 General wireline communication architecture

Fig. 2.1 shows the functions of wireline communication technology. The transmitter (TX) can transmit the signal through “channel”. The channel can carry the signal from transmitter to receiver, but it will impair the transmitted signal at the small time. There are various types of channel including coaxial, fiber, backplane trace for wireline, and free-space, multi-path reflection for wireless.

Fig. 2.1

2.2 Serial vs. Parallel

In wireline communication technology we transfer the data links from parallel to serial like Fig. 2.2

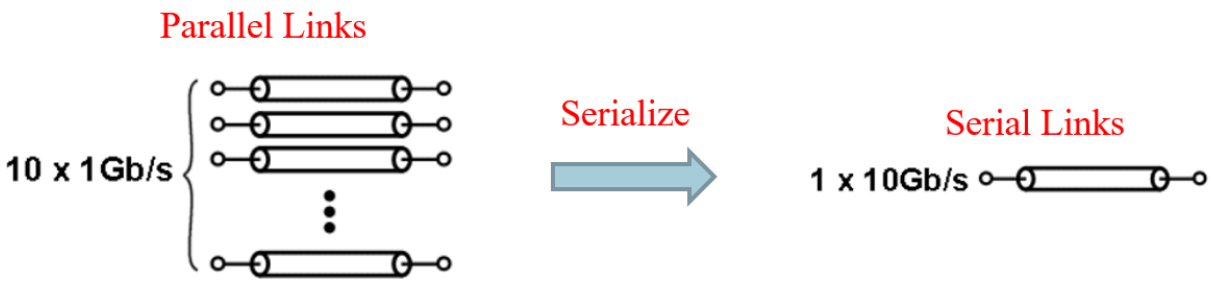


Fig. 2.2

There are three main reasons why we use this method to send high-speed data. The first reason is that the more channels there are, the higher the cost will be. The cost is due to the production cost of the channel and the power consumption generated by the channel. Second, the less the number of channels we can reduce the area of the interconnections. Third, synchronization for data in parallel links is difficult. But as a result of using serial links to transfer data is the cost of higher channel loss (increased bandwidth) and complicated circuit design.

2.3 Architecture of SerDes

Following (Fig. 2.3) is a general architecture of a serializer /deserializer (SerDes). In general, low-speed, sub-rate data inputs are presented at the input ports in parallel. They are retimed and serialized into higher speed data streams by a multiplexer (MUX). A phase-locked loop (PLL) provides clocks with different frequencies

and phases for the retimers and selectors in the MUX. An output driver is used to deliver data to the channel. For optical applications, laser drivers are employed to emitted laser into the fiber, which may introduce distortion, dispersion, and other nonidealities. High frequency signal power tends to be attenuated more severely in the channel, so the transmitter usually includes a pre-emphasis device to neutralize the effect.

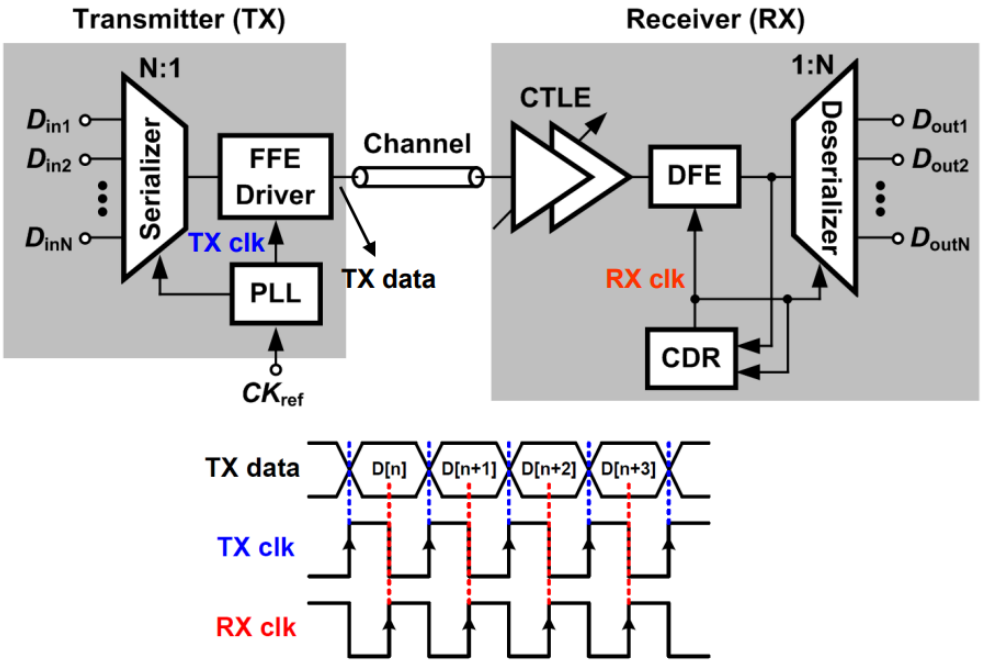
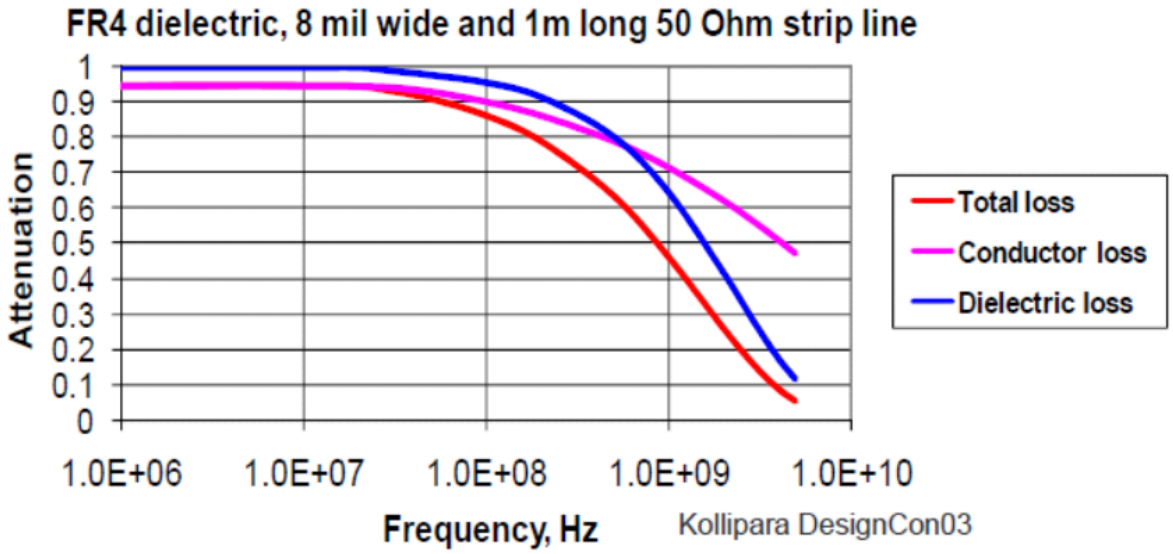


Fig. 2.3

2.4 Channel loss

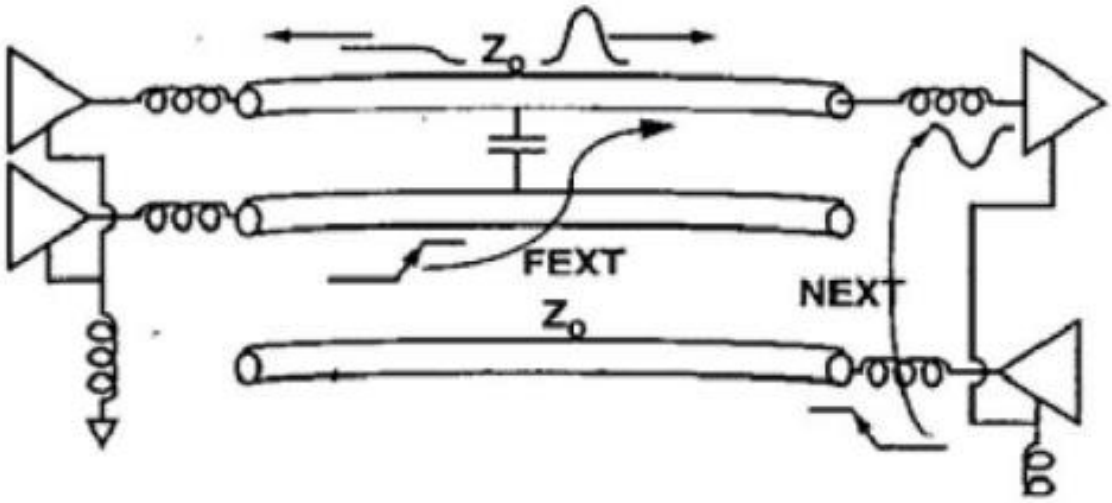
A typical channel, taking FR4 channel for example, suffers from skin effect loss, dielectric loss, crosstalk, and other nonidealities, we need to introduce more complicated equalizing technology in

receiver to recover data when the data rate is high, which will result in higher power consumption. And that is the reason why the optical channel is favorite to use in data center.



- Skin Effect Loss ∝ √ F
- Dielectric Loss ∝ F

Fig. 2.4



■ “Near-end” xtalk: NEXT (reverse wave)
■ “Far-end” xtalk: FEXT (forward wave)

Fig. 2.5

2.5 Eye diagram

By folding transmitter output data every two bit periods and overlapping the waveform, we obtain an eye diagram. The widest opening of the “eye” is named eye opening. Similarly, eye closure is defined as 1−eye-opening. Also known as inter symbol interference (ISI), the eye closure is indeed caused by incomplete pulses.

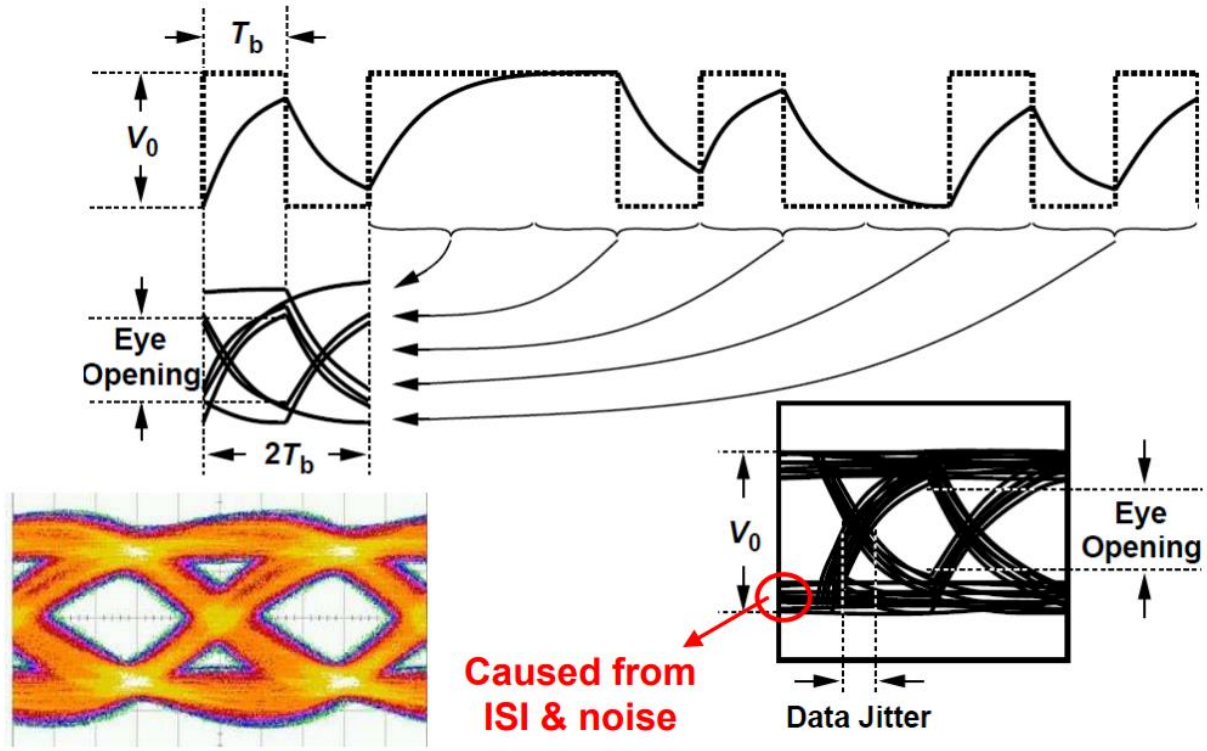


Fig. 2.6

3. Characteristics of Modern High-Speed VCSELs

3.1 VCSEL cross section

A VCSEL is actually heterostructure laser diode with active region covered by distributed Bragg reflectors (DBRs) on top and bottom. As shown in Fig. 3.1, light comes out in the direction perpendicular to the surface, facilitating 20 array realization. The easy in-wafer testing and circular beam makes VCSEL superior to its edge emitting counterpart.

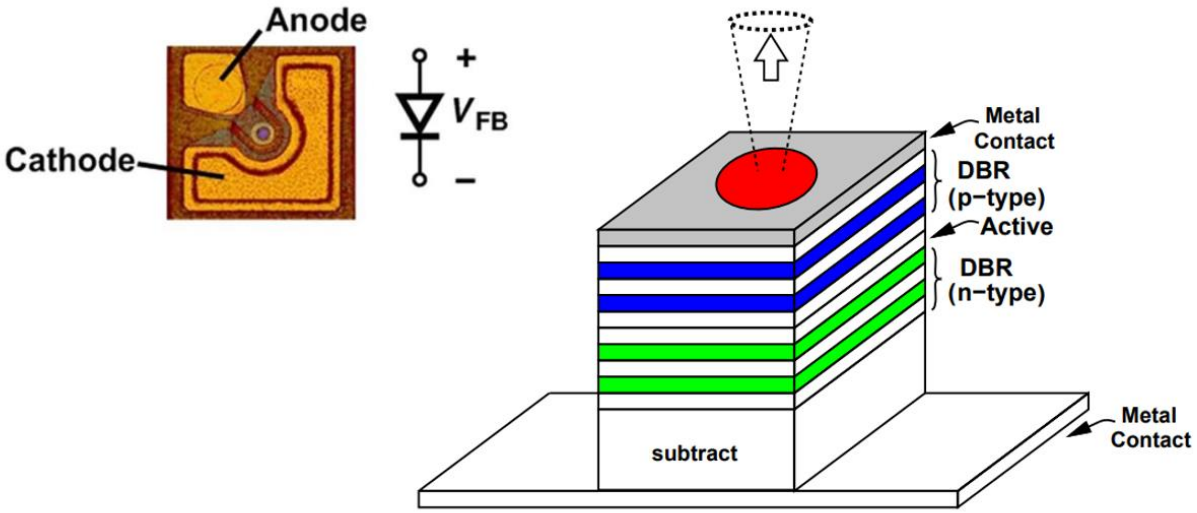


Fig. 3.1

3.2 VCSEL DC characteristic

For communications using a VCSEL, the data is modulated in the power emitted by the VCSEL. This can be controlled by the current

injected into the laser. There are two critical DC characteristic curves which are taken into consideration when modulating a VCSEL. They are the V-I and P-I curves.

The V-I characteristics give us the differential resistance of the VCSEL which helps us determine the voltage drop expected for different modulation currents. This is an important parameter as the driver bias point needs to be designed keeping in mind that the transistors don't go out of saturation in case of a large voltage drop across the VCSEL.

The P-I characteristics are shown in below. This is the most important curve for modulating the VCSEL. From the curve, the approximate DC response of the VCSEL output power is given by

$$P_{out} = \eta \times (\mathrm{I}_{VCSEL} - \mathrm{I}_{TH})$$

Here, η is the slope efficiency of the VCSEL and I_{TH} is the threshold value of the injected current. The VCSEL is turned ON when the injected current is more than the threshold current.

3.3 VCSEL AC characteristic

Just like any laser, the VCSEL optical response depends on the electron density N and the photon density Np in the laser cavity

volume V. Light is the result of the interactions between these densities and can be estimated by solving the following coupled differential equations, also called the rate equations.

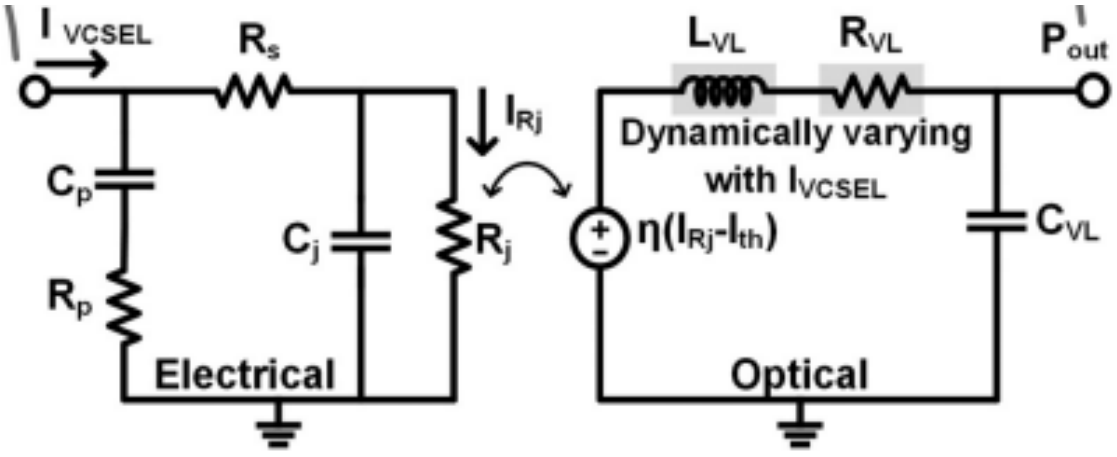
$$\frac{dN}{dt} = \frac{I_{VCSEL}}{qV} - \frac{N}{\tau_{sp}} - GNN_p$$

$$\frac{dN_p}{dt} = GNN_p + \beta_{sp}\frac{N}{\tau_{sp}} - \frac{N_p}{\tau_p}$$

$$P_O = N_p h v V v_g$$

Here, h is the Plank's constant, v is the frequency of emitted light and v_g is the light group velocity.

Combining the rate equations above and taking the Laplace transform, we can form it as a second-order low-pass filter. By using it we can construct an ideal model as Fig. 3.2 to simulate VCSEL nonlinearity characteristics.



■ Mayank Raj, JSSC ’16

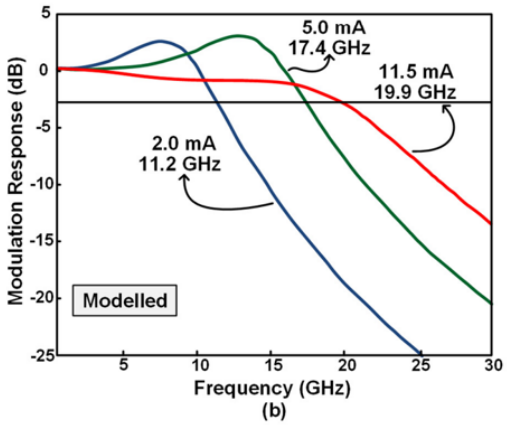


Fig. 3.2

4. VCSEL Transmitter Architecture

4.1 Transmitter architecture

The overall circuit architecture shown in Fig. 4.1.

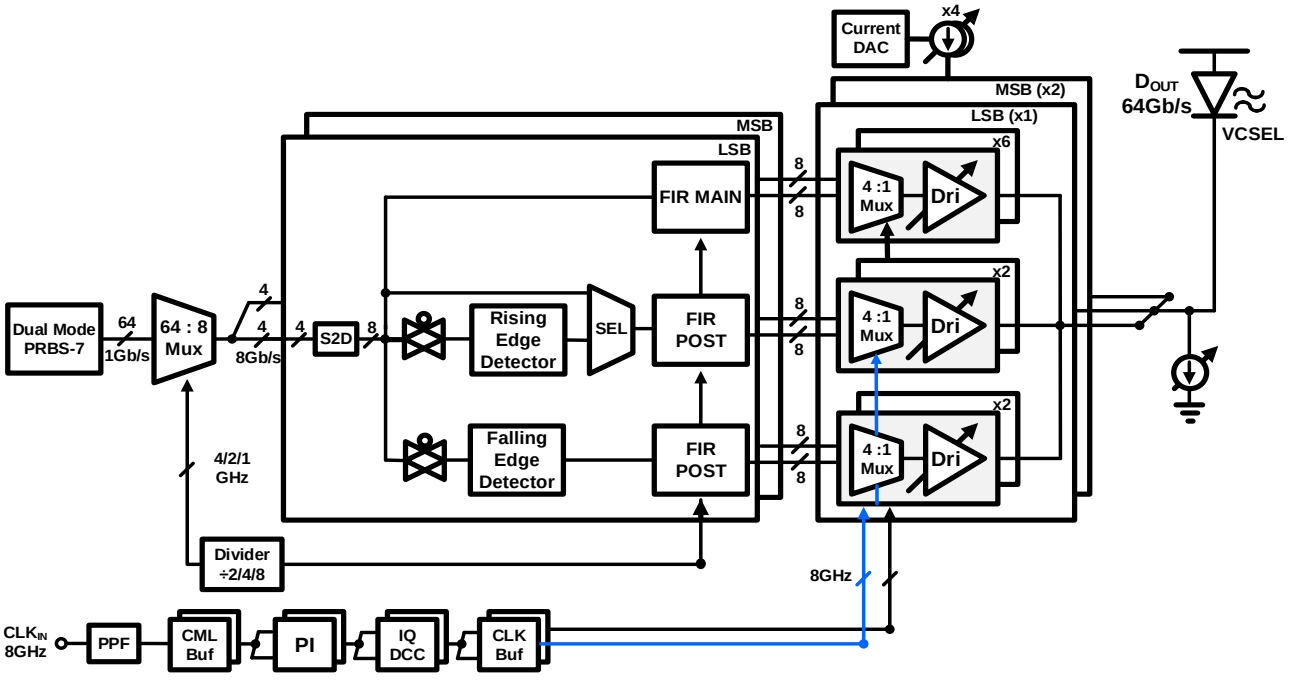


Fig. 4.1

First of all, the PRBS generates various data sequence at low speed, and transmits to the next 64:8 mux and get synthesized into higher speed data. Secondly, the tree structure circuit consisting of 3 stages of 2:1 mux is chosen as the 64:8 mux to synchronize the phase of data and clock effectively. The following circuits are quarter-rate edge pulse detectors which generates pulses at each rising and falling edge transition to compensate the unexpected behavior of VCSEL. Each rising and falling data will be sent to three corresponding feed-forward equalizers (FFE) and be serialized to highest speed data. The modulation output is shown as Fig. 4.2. and Fig. 4.3

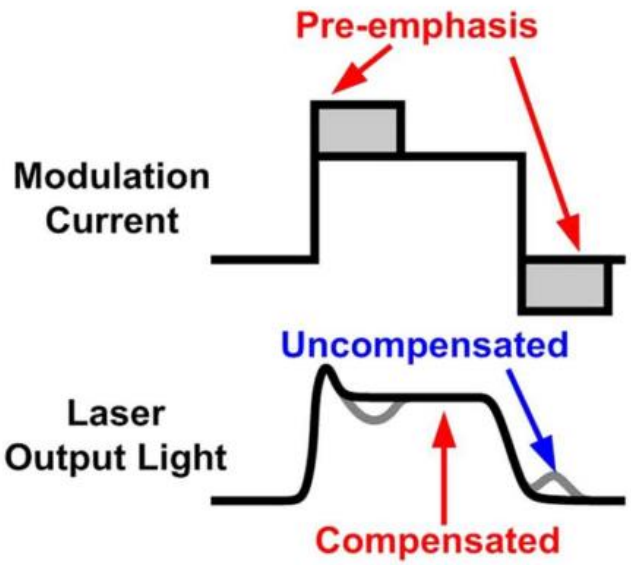


Fig. 4.2

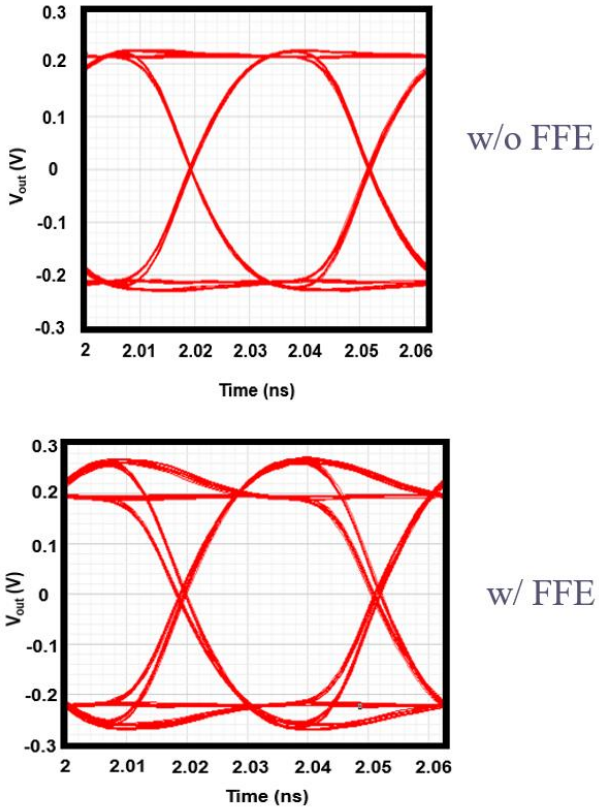


Fig. 4.3

Thirdly, a nonlinear and asymmetric FFE is specifically designed to generate a wide phase of post cursors from 0.5UI delay to 2UI delay by tuning the phase interpolator in order to alleviate the nonlinearity of VCSELs and the intersymbol interference (ISI). Finally, the data will be synthesized to 32Gb/s and transmitted to the current mode driver to driver the VCSEL.

5. Industry Analysis

5.1 VCSEL market forecast

The VCSEL market will rise at a compound annual growth rate (CAGR) of 18.3% from more than $1bn in 2020 to $2.7bn in 2025 (Fig. 5.1).

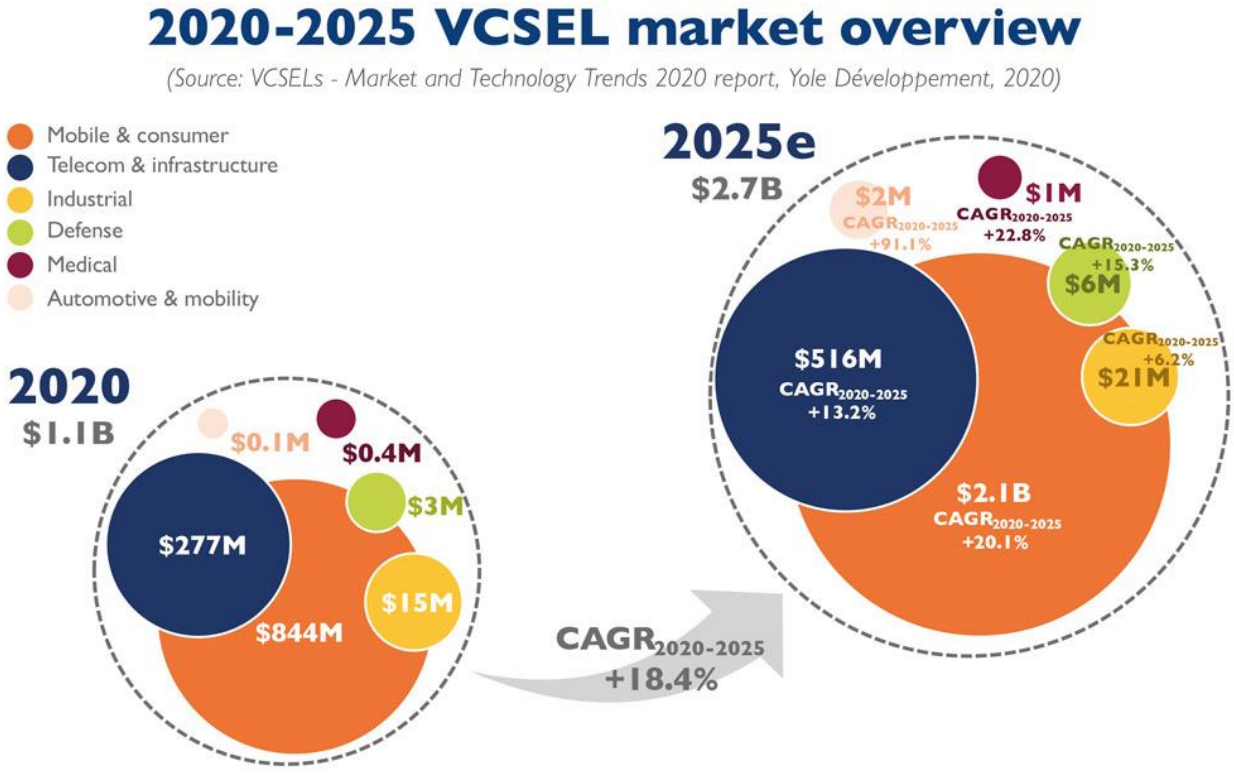


Fig. 5.1

From Fig. 5.1, we can find out that telecom and infrastructure applications (mainly data center) are expected to generate revenue of $277m in 2020 and should reach $516m in 2025 at a CAGR of 13.2%.

5.2 Porter’s five forces analysis

5.1.1 Bargaining power of customers

- High switching cost
- High product differentiation
- Low bargaining power of customers

5.1.2 Bargaining power of suppliers

- High bargaining power for optical component and foundry suppliers
- Low bargaining power for PCB suppliers

5.1.3 Competitive rivalry

- High market concentration
- High product differentiation
- High competitive rivalry

5.1.4 Threat of substitutes

- No substitute
- Market still has room to go

5.1.5 Threat of new entrants

- High entry costs
- Large market growth
- Still has the threat of new entrants

5.3 SWOT

5.2.1 Strengths

- Low cost of processing
- Low power consumption in Tx and Rx circuit
- Less signal degradation

5.2.2 Weakness

- Low power output of VCSELs
- Limited distance
- Nonlinearity

5.2.3 Opportunities

- Achieving high modulation bandwidth at small current
- Increase optical output power

5.2.4 Threats

- New interconnection technology

6. Conclusion

The growth of bandwidth requirements have pushed the traditionally electrical wireline interconnects within data center and computing system to limits. To overcome the shortcomings of electrical

channels, several receiver and transmitter equalization techniques have been used. However, these compensation techniques consume considerable power and die area, and, as a result, current high-speed I/O link designs are increasingly becoming power and channel-limited.

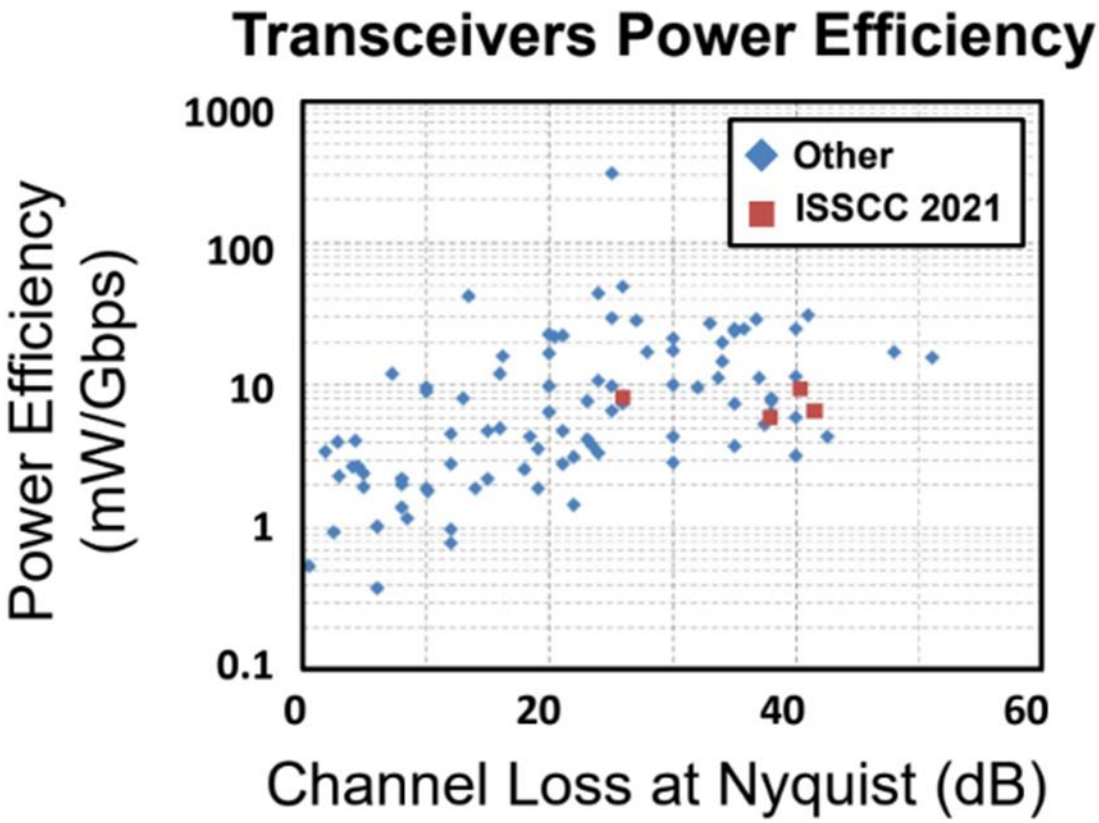


Fig 6.1

A possible solution to this problem is to use optical interconnects. Optical channels, unlike their electrical counterparts, have negligible frequency-dependent loss. This provides the opportunity for optical link designs to fully utilize higher data-rates available through CMOS

technology scaling, without excessive equalization complexity.

7. References

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