Introduction to SoC and Its Applications

SoC Design

Outline

- IC Industry Segments
- IC Design Flow
- Conquer SoC Design Complexity
- What is the Intellectual Property?
- Platform-based Design Methodology
- Conclusion

IC Industry Segments

- **IC design**
  - Designs of layouts, circuits, logic gates, architectures, or behaviors
- **IC fabrication**
  - Process technology of fabricating transistors in chips (UMC, TSMC)
- **IC testing**
  - Design for testability
- **IC packaging**
  - Assembly dies into a supporting case to prevent physical damages
- **CAD (Computer-Aided Design)**
  - All the related EDA (electronic design automation) tools during IC designs

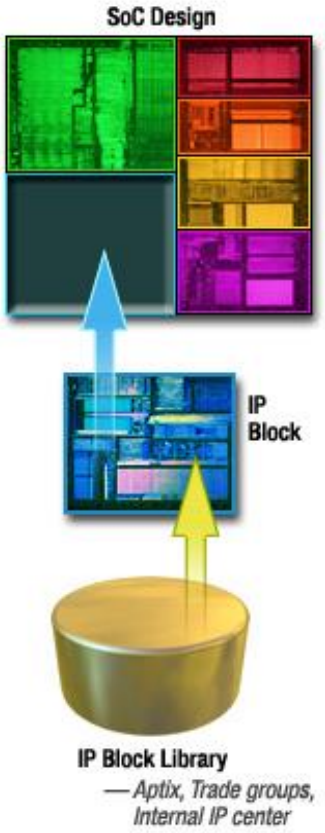
SoC: System on Chip

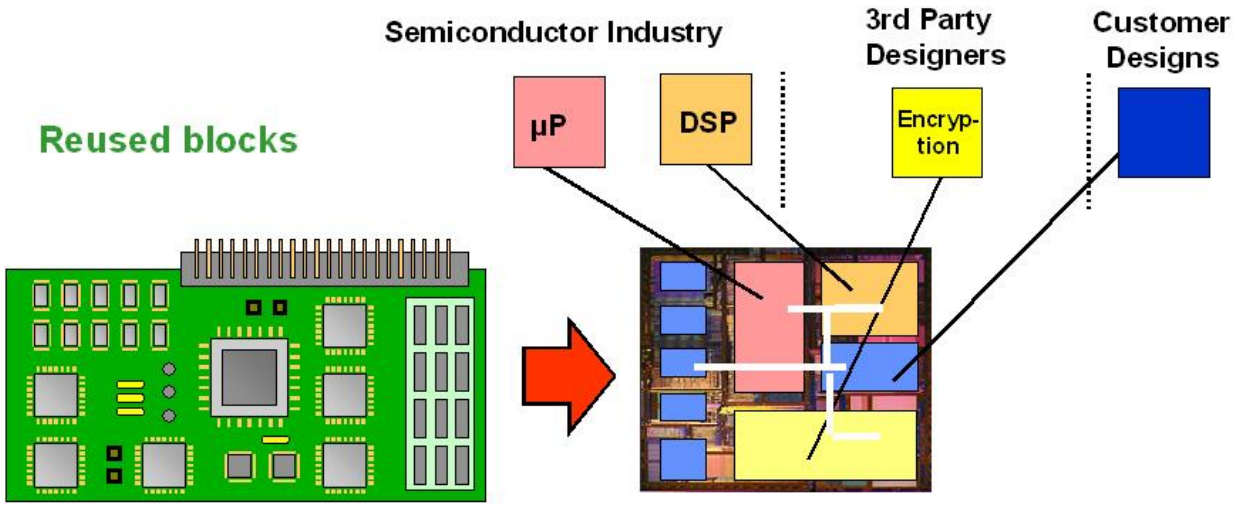
- **System**

  A collection of all kinds of components and/or subsystems that are appropriately interconnected to perform the specified functions for end users.

- **A SoC design is a "product creation process" which**
  - Starts at identifying the end-user needs (or system)
    - Hardware
    - Software
  - Ends at delivering a product with enough functional satisfaction to overcome the payment from the end-user

What is SoC in your mind?





Definition: integration of a complete system onto a single IC

SoC Applications

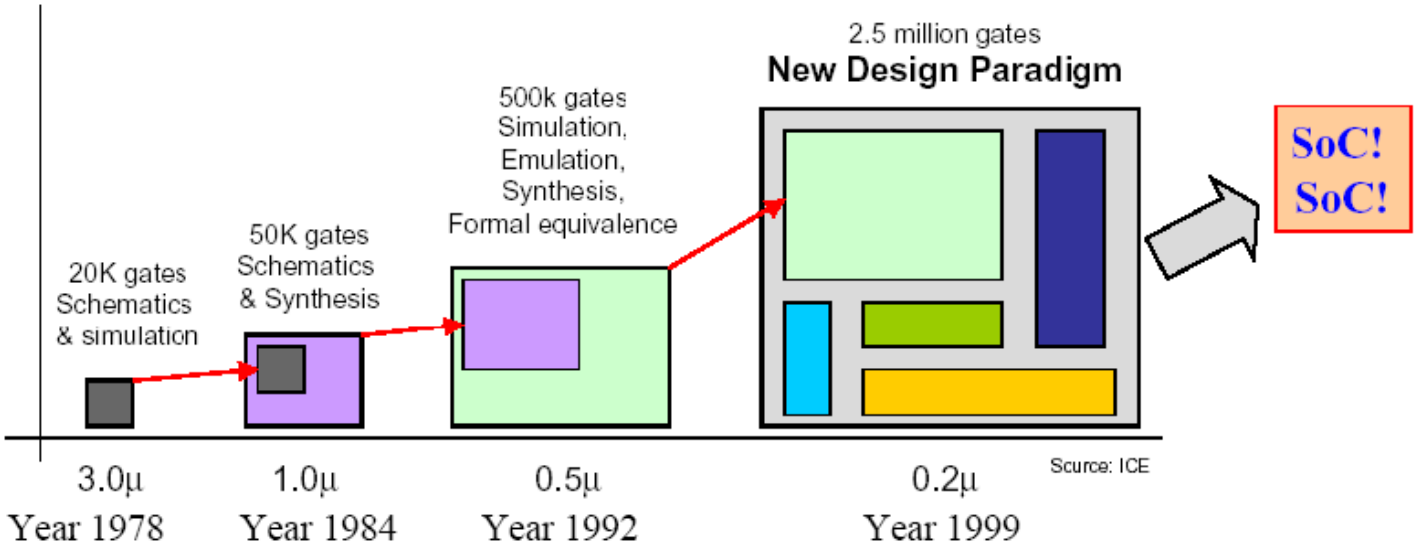
- **Microprocessors or microcontroller**
  - Pentium, ARM, DSP processors
- **Memory**
  - DRAM, SRAM, ROM, flash
- **Special purpose processors**
  - Audio, image or video compression
    - Image: JPEG, JPEG2000
    - Video: MPEG 1, 2, 4, 7, H.264/MPEG-4 AVC, HEVC(high efficiency video coding (video compression)
    - Audio: MP3, AC3, …
  - Communication (wire or wireless)
- **Information Appliance (IA) –Smart phones/Personal Digital Assistants(PDA)**
- **BioChip**

Why Nanometer Transistors?

- Performance increases on a single chip
- Power decreases
- Area decreases
- Cost reduces
- Higher speed, higher frequency

Evolution of Microelectronics

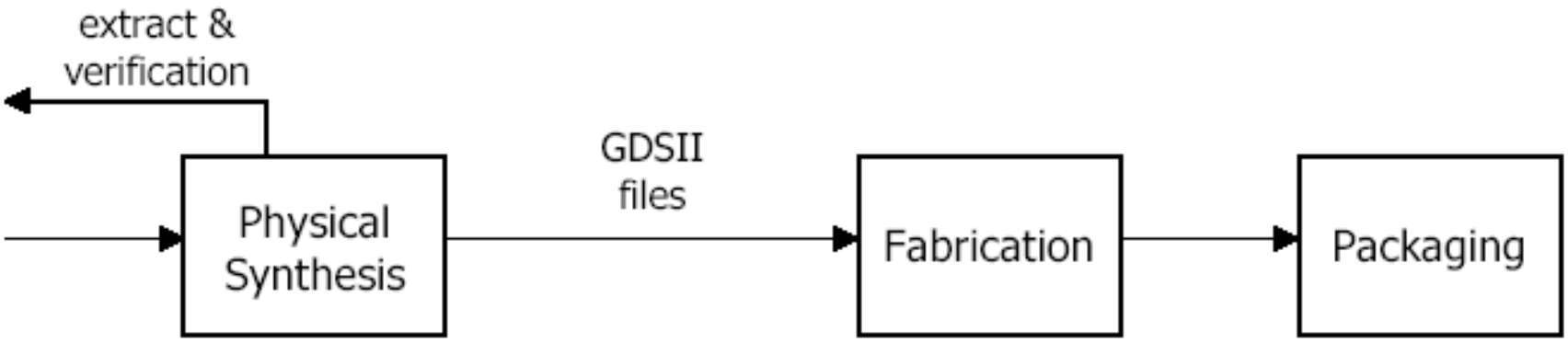
- **Today's Silicon process technology**
  - 0.13μm CMOS, 90nm, 65nm, 45nm, 22nm, 10nm, 7nm, 5nm
  - ~100 M of devices, 3GHz internal clock
- **Yesterday's chips are today's function blocks**

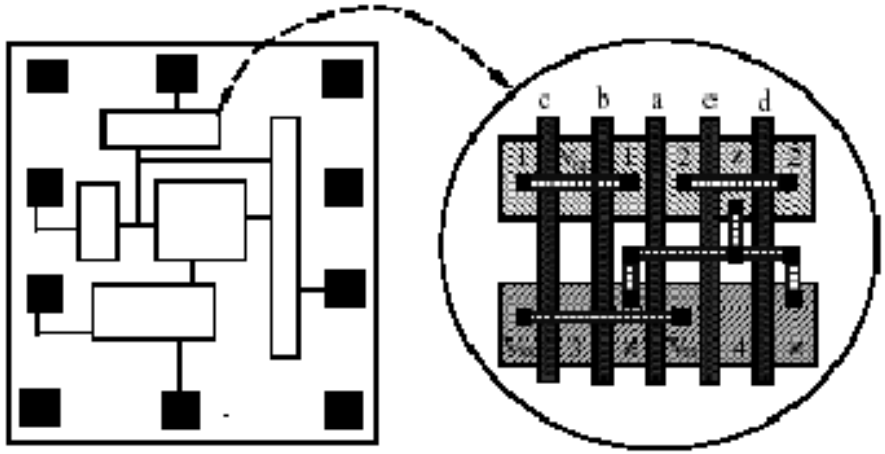


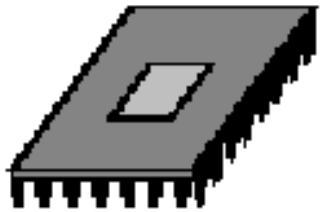
Challenges of Nanometer Transistors and SoC

- **Fabrication**
  - Uniform control of nano wires
  - Mass production with high yield rate
  - Device structure
  - Expensive Equipments
- **Design**
  - More IC complexity, Lower voltage, Higher frequency (> 10G Hz)
  - EDA tool support
  - Device leakage current problem
  - Interconnection wire delay
  - Shorter design time
- **IC Systems**
  - SoC
  - Embedded Software
  - Cross Domain Applications

IC Design and Fabrication

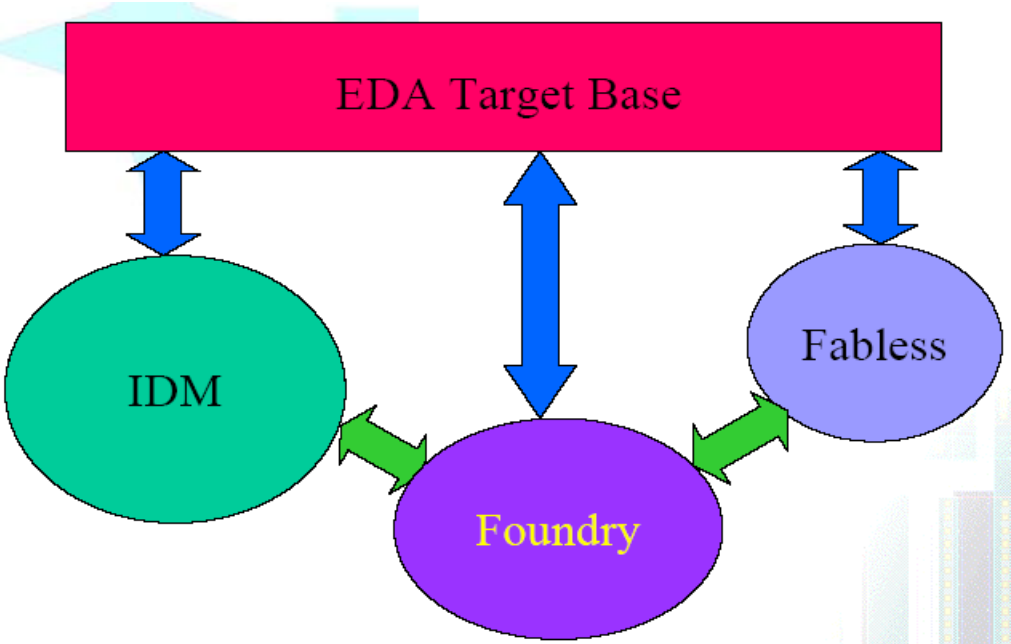






IC Industry Segments in Taiwan

- Integrated Device Manufacturers (IDM)
- Foundries
- Fabless Semiconductor Companies
- EDA Vendors (Synopsys acquire springsoft), Cadence



System Development Flow

Applications

Specifications

傳輸距離： 100 m
功率消耗：2 W
功能：影像傳輸、
語音傳輸
螢　幕：176 x 220 pixel
65535 色
1.8 吋 TFT
其他

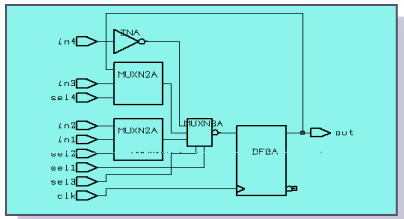
System Design

Hardware:
CPU,
RAM, I/O…

Software:
C,C++

Component Design

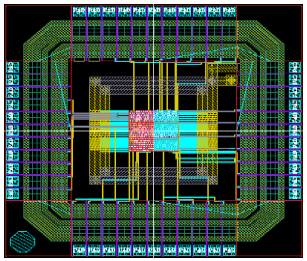
```
always @(posedge clk)
begin
  if (sel1) begin
     out=in1;
  else
     out=in2;
  end
end
```



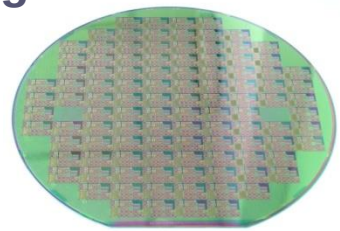
Synthesis

Placement & Routing

Layout

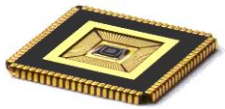


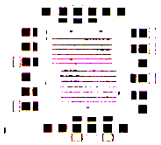
Fabrication



Testing

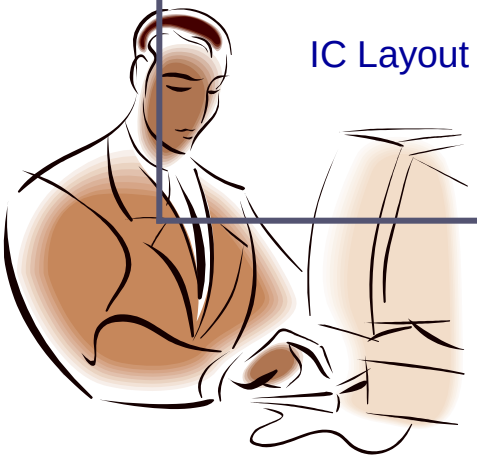
Marketing





IC Designers

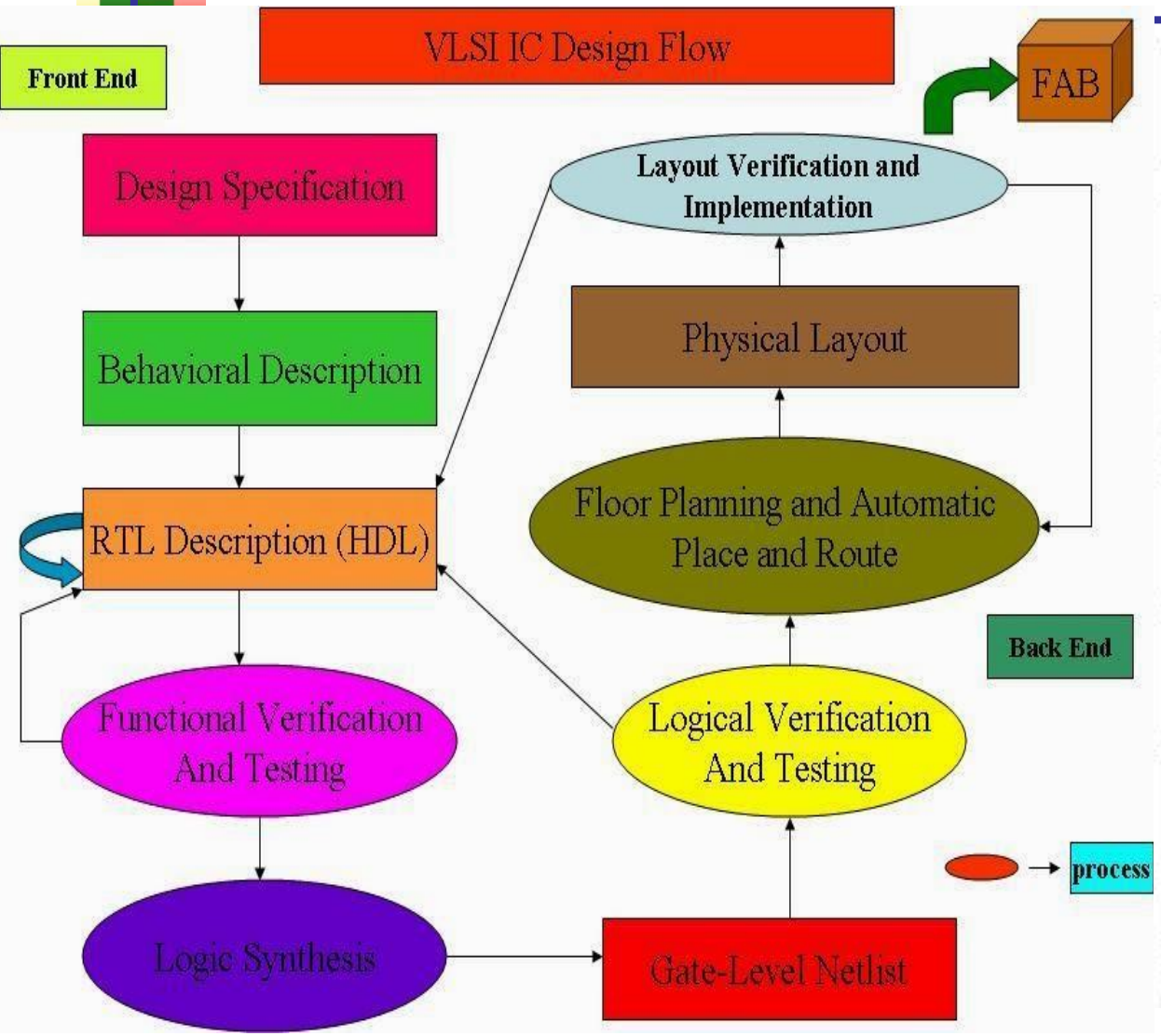
Who	What to do
System Design Engineer ASIC Design Engineer IP Design Engineer Circuit Design Engineer CAD Engineer Test Engineer	Specification Definition Behavioral Design and Simulation Register Transfer Level (RTL) Design, Simulation and Testing Gate/Switch/Circuit Level Design, Simulation and Testing
IC Layout Engineer	Physical Layout Layout Verification Post-layout Verification (Simulation)

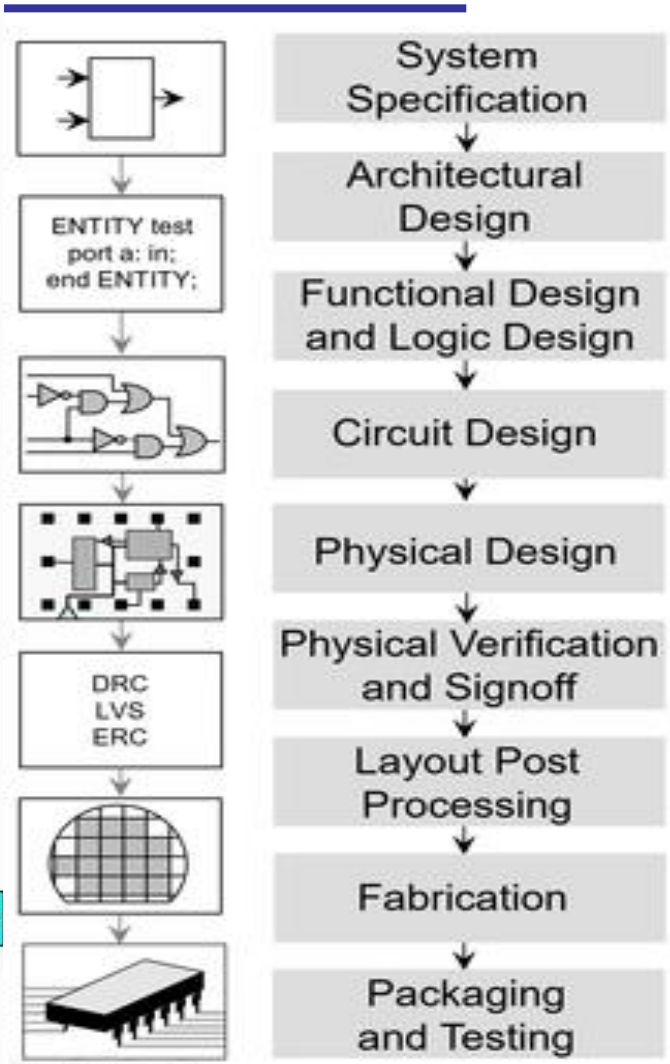


Outline

- IC Industry Segments
- IC Design Flow
- Conquer SoC Design Complexity
- What is the Intellectual Property?
- Platform-based Design Methodology
- Conclusion

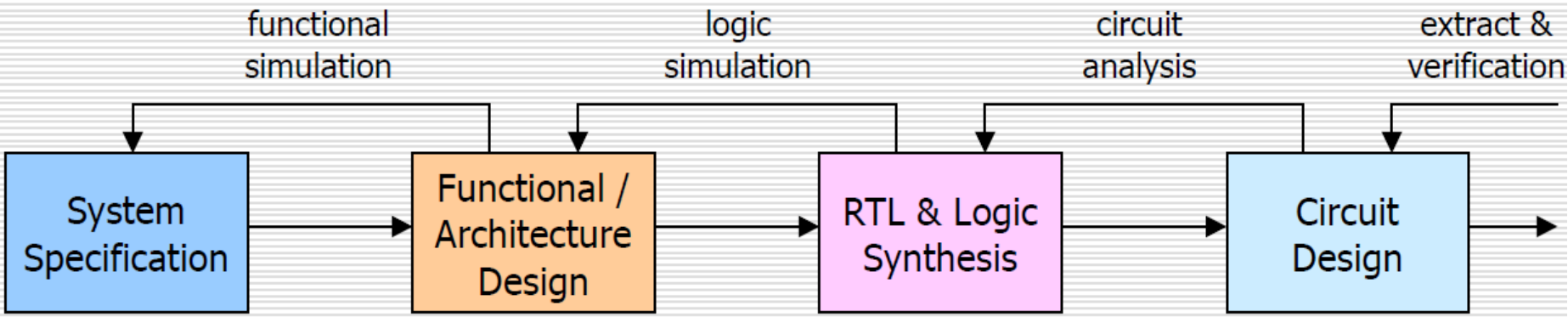
IC Design Flow

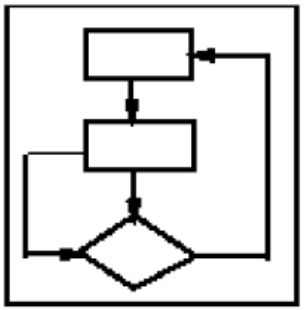




HDL-Based Design Flow

Typical HDL-Based Design Flow

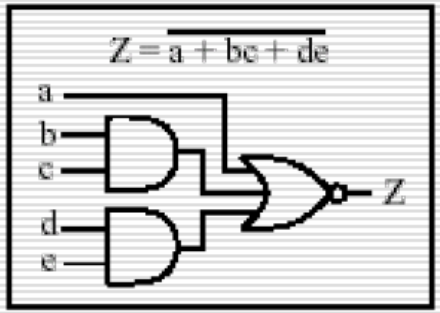




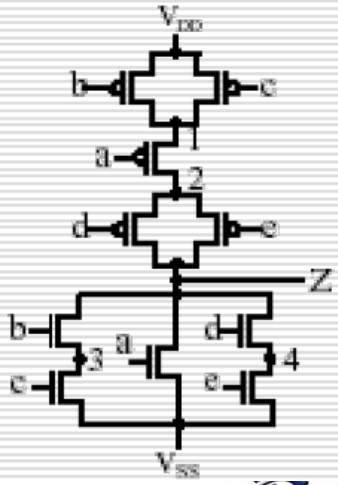
behavior representation

```
module fz(a,b,c,d,e,Z);
input a,b,c,d;
output Z;
assign Z =
  ~(a|(b&C)|(d&e));
endmodule
```

HDL description



gate-level representation



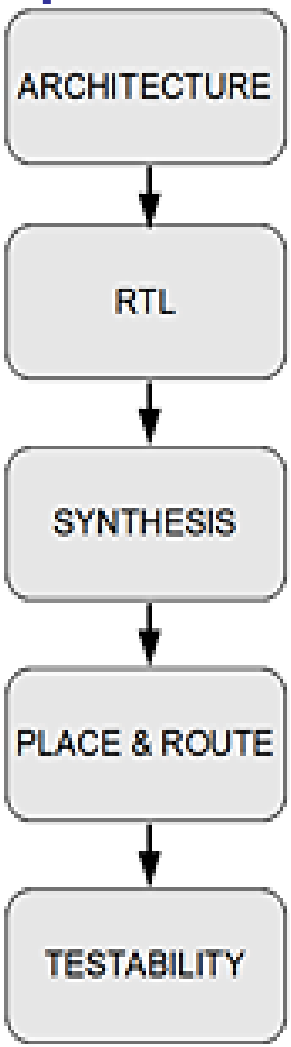
RTL Code Example

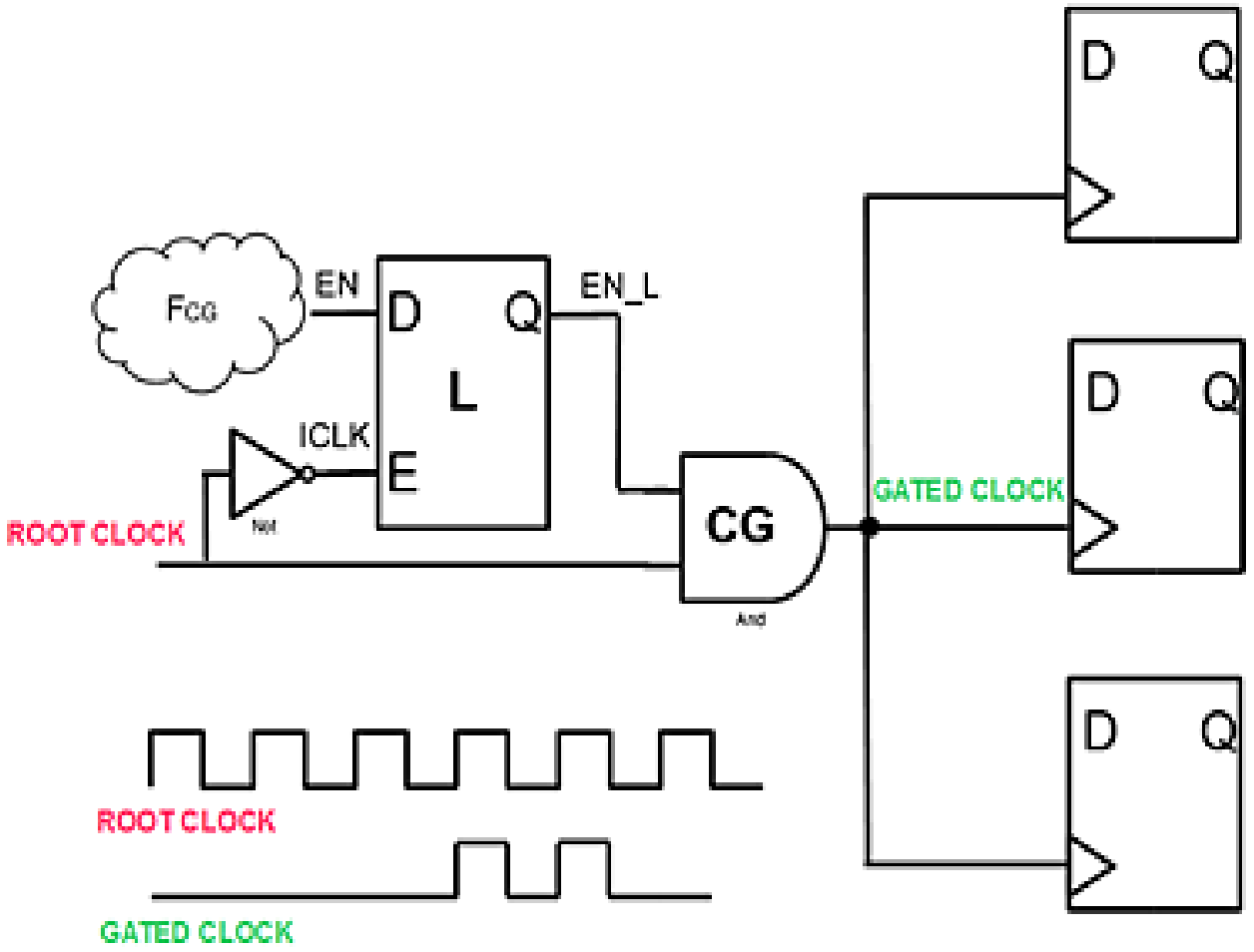
```
always @(posedge clk or negedge rst)
  if (!rst)
    bcd_counter <= #1 4'b0000;
  else
    bcd_counter <= #1 bcd_counter + 1; // binary counter
end

//convert binary to gray code
assign gray_code = { bcd_counter[3] ,
                     bcd_counter[3] ^ bcd_counter[2],
                     bcd_counter[2] ^ bcd_counter[1],
                     bcd_counter[1] ^ bcd_counter[0]}
```

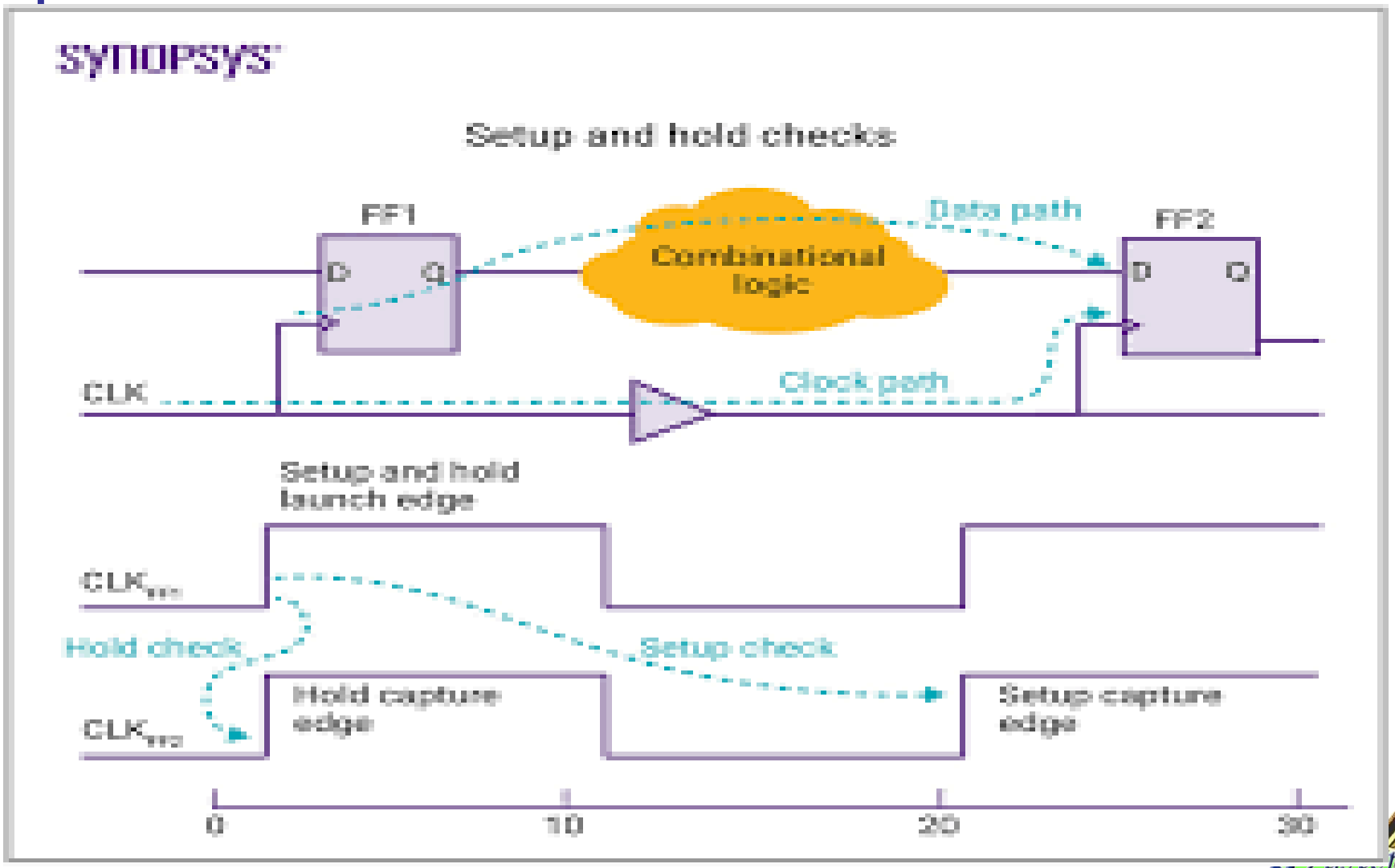
Verilog code to convert BCD to Gray Code *(Ex. 16)*

Synthesis example

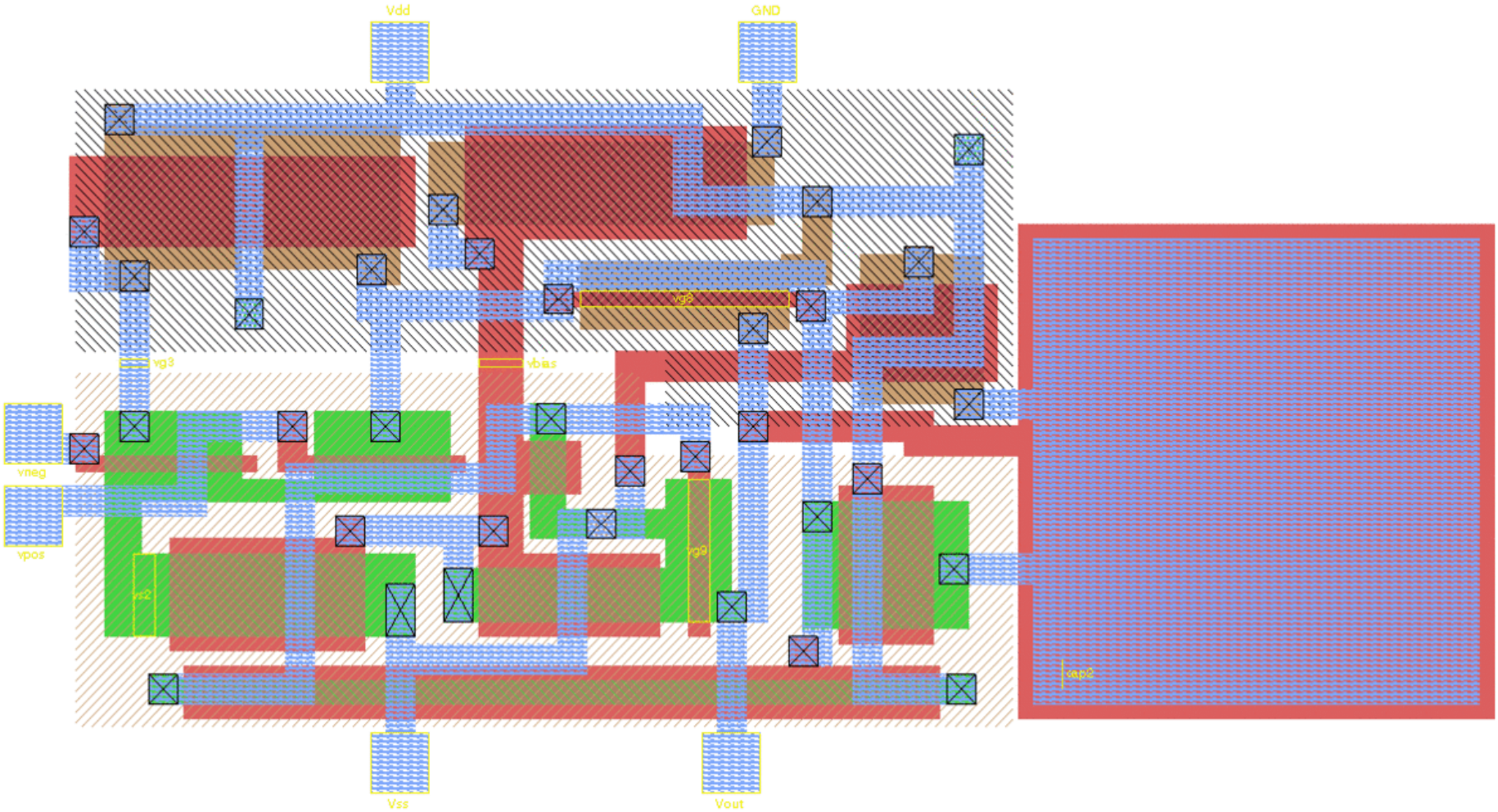




Static Timing Analysis (STA)

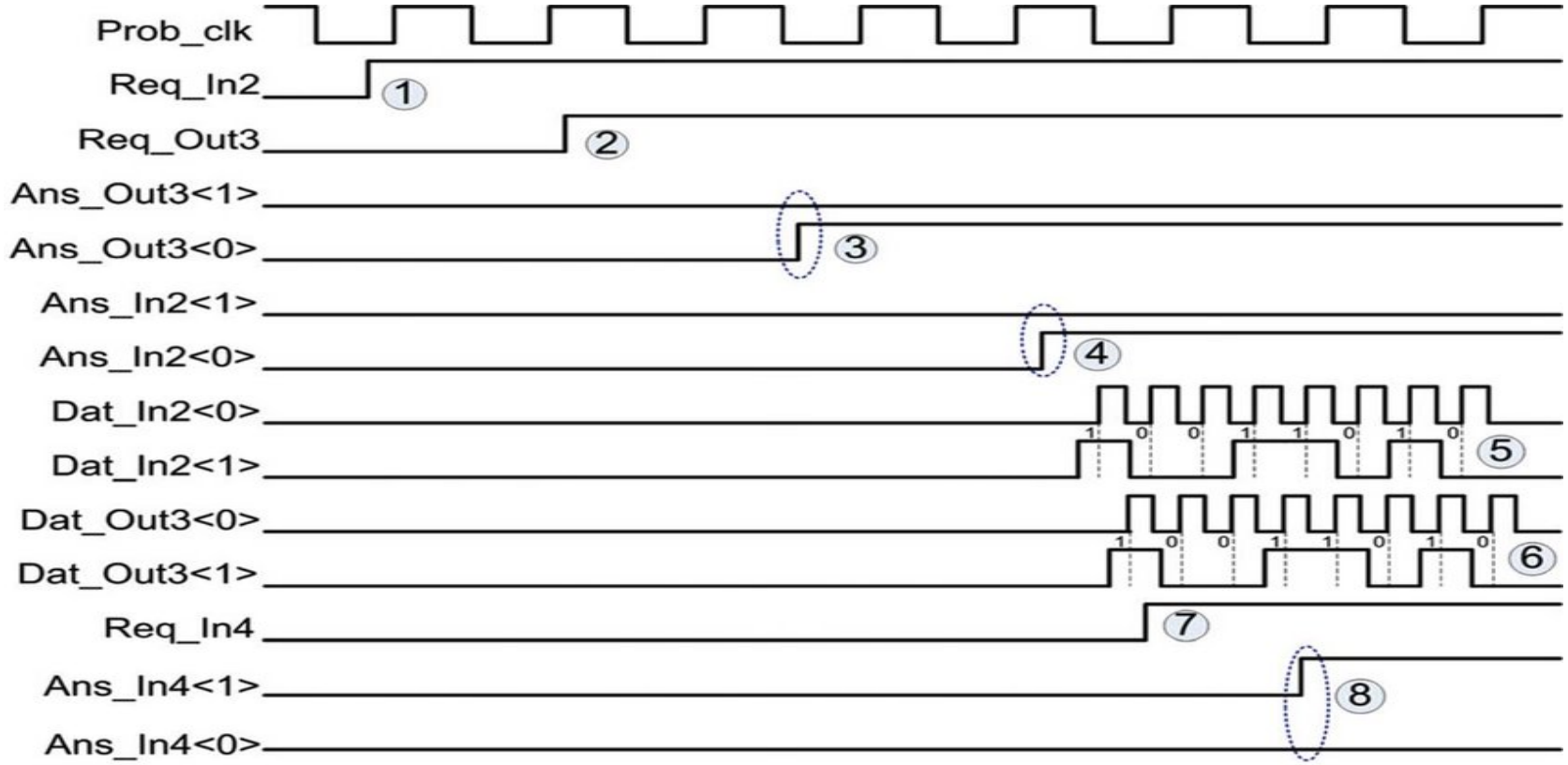


Place and Route Example



Post Layout Simulation Example

- Adding parasitic resistance/capacitance/inductance, device modeling

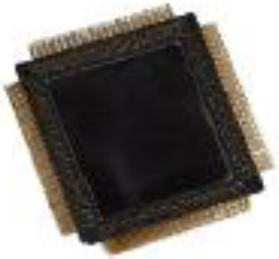


① Request (or incomming probe) arrives at In2
② Request is fowarded to idle Out3
③ ACK arrives at Out3 from downstream switch
④ ACK is sent to upstream switch
⑤ - ⑥ Data wave-pipelined from Dat_In2 to Dat_Out3
⑦ Request Circuit arrives at In4
⑧ Out3 is busy, "Network-Blocked" is sent to upstream switch to force backtracking

Outline

- IC Industry Segments
- IC Design Flow
- Conquer SoC Design Complexity
- What is the Intellectual Property?
- Platform-based Design Methodology
- Conclusion

SOC is industry trend



Today

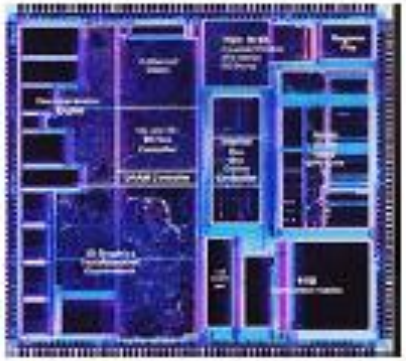
Assembly

ASIC/ASSP Application specific standard product

System-Board

Tomorrow

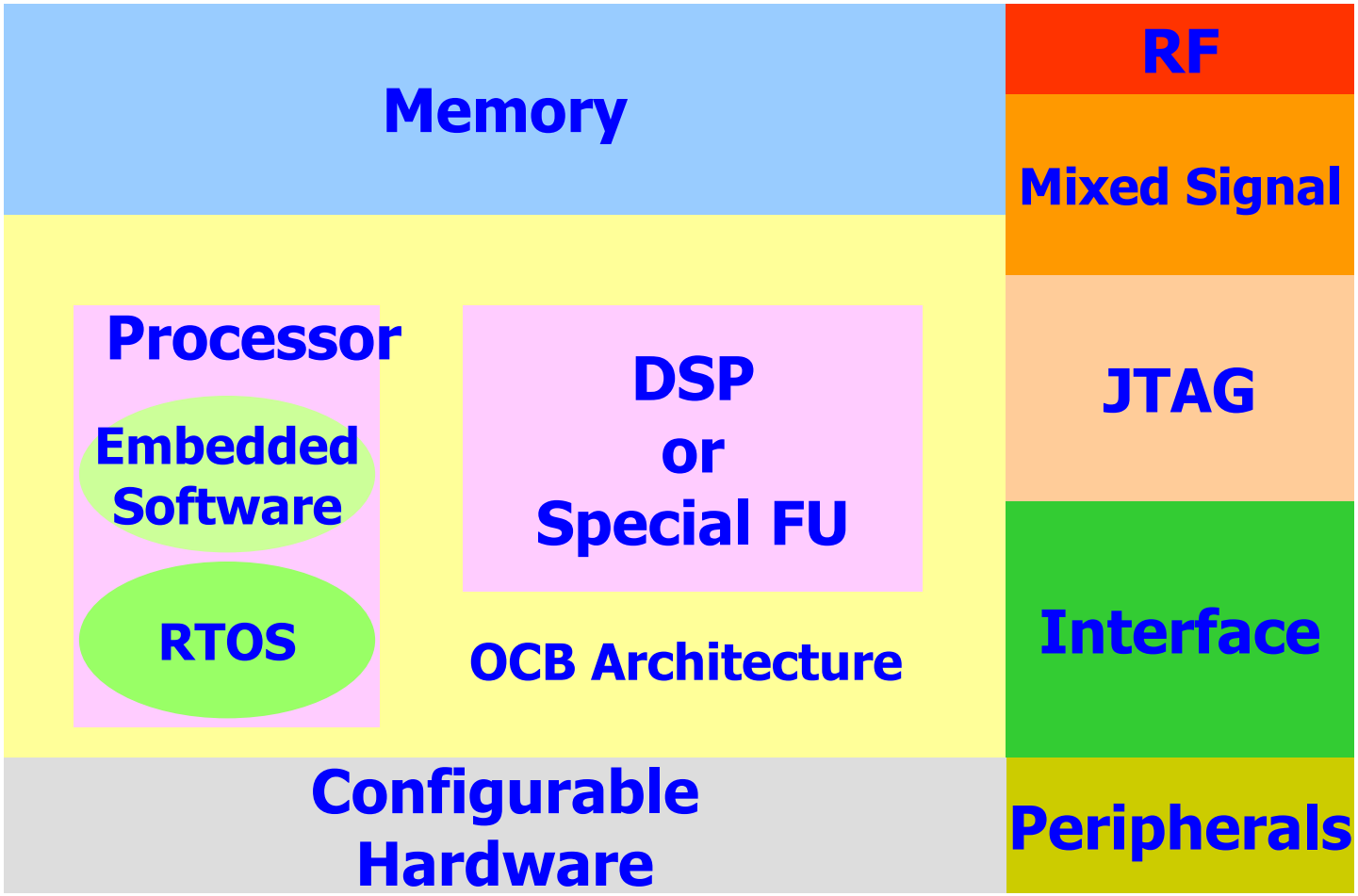
Integration



IP/System-Board

SOC

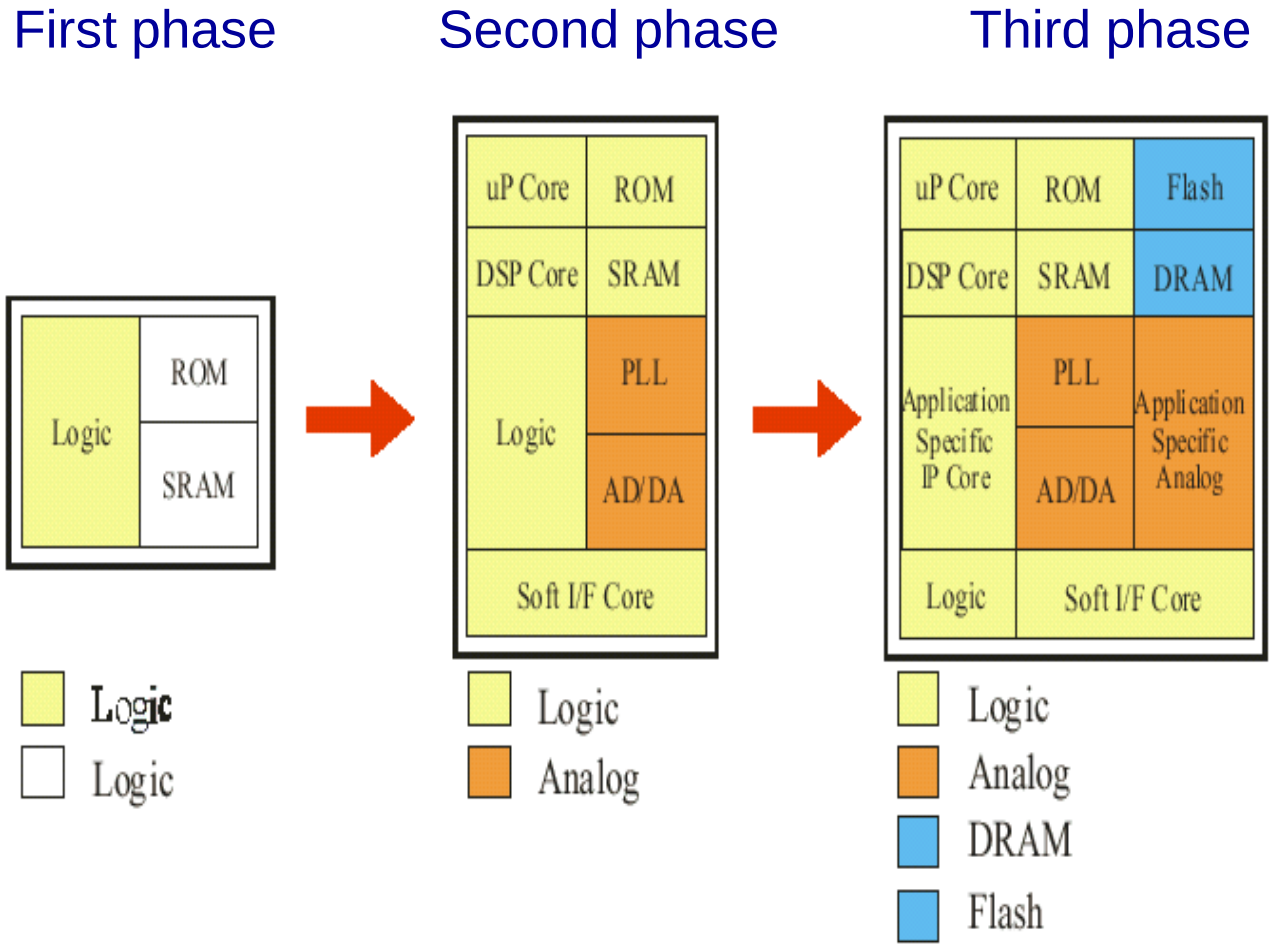
SoC Architecture



Joint Test Action Group (JTAG)

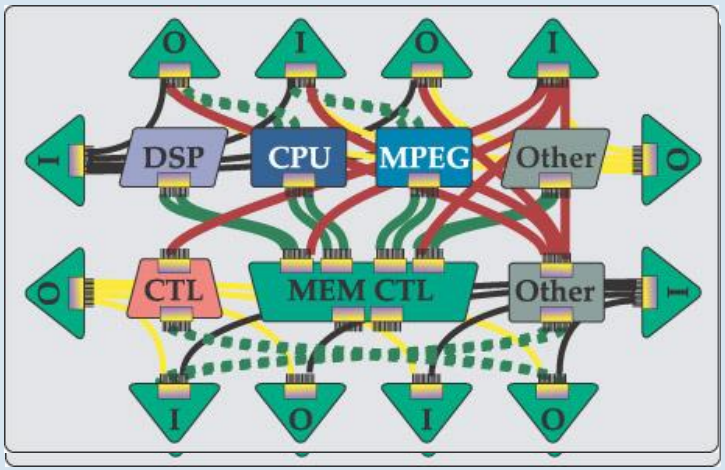
On Chip Bus (OCB)

SoC On-Chip Module Evolution



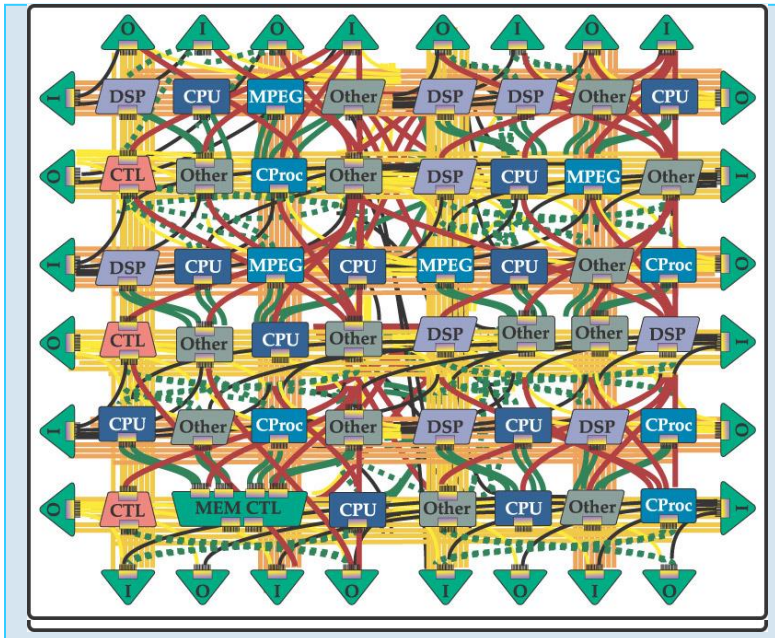
SOC Complexity / Abstraction

Yesterday



- Processor-centric (1 or 2)
- Simple I/O
- Manageable Complexity

Today



- Many processing units
- Large amount of I/O
- Overwhelming Complexity!

Source: EI-SONICS

Conquer the SoC Design Complexity

- **Use a known real entity**
  - A pre-designed component (Intellectual Property (IP), Virtual Component (VC) reuse)
  - A platform (architecture reuse)
- **Partition**
  - Based on functionality
  - Hardware and software
- **Modeling**
  - At different level
  - Consistent and accurate

Outline

- IC Industry Segments
- IC Design Flow
- Conquer SoC Design Complexity
- What is the Intellectual Property?
- Platform-based Design Methodology
- Conclusion

What is IP?

- **Intellectual Property (IP)**
  - Intellectual Property means products, technology, software, etc. that have been protected through patents, copyrights, or trade secrets.
- **Virtual Component (VC)**
  - A block that meets the Virtual Socket Interface Specification (VSIA) and is used as a component in the Virtual Socket design environment. Virtual Components can be of three forms — Soft, Firm, or Hard.
  - Also named mega function, macro block, reusable component

Buzz words or Slogans

- **SOC (System-On-a-Chip)**
  - Integration of all HW and SW components of a system on a single chip
  - Embedded microprocessor cores, embedded real-time OS (RTOS), embedded memory, …
- **SIP (Silicon Intellectual Property)**
  - A complete HW component ready for integration in SOC
  - Similar to a subroutines (functional call) in software program
- **ASIC (Application Specific Integrated IC)**
  - Design for special functions (i.e. Video decoder, USB 3.0)
- **Programmable IC**
  - Design for general purpose (i.e. CPU, ARM)

Types of IP – based on Functionally

- **Foundation IP – Cell, MegaCell**
  - Standard Cell
    - Core Cells –(Combinational cells/Sequential cells)
    - I/O cells –Input/Output/Power/gound
    - Hard Macro Cells – RAM/ROM/Register/Hard IP
- **Star IP – ARM (low power)**
- **Niche IP – JPEG, MPEGII, TV, Filter**
- **Standard IP – USB, IEEE1394, ADC, DAC**
- **……..**

IP Sources

- Legacy IP
  - from previous IC
- New IP
  - specifically designed for reuse
- Licensed IP
  - from IP vendors

IP, VC, PE, FU, …

- **Pre-designed component Components**
  - PE – Processor Element
  - FU – Functional Unit
  - Memory controller
  - Interrupt controller
  - Power management controller
  - Internal memories
  - Bridges
  - Caches
  - Other functional units

Types of IP

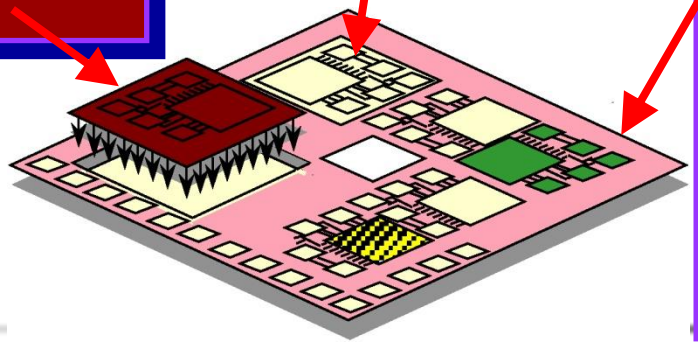
- IP realization:
  - Hard IP
  - Firm IP
  - Soft IP

Firm IP:

- gate level or synthesizable RT level data
- Some technology and/or physical constraints
- some flexibility on form & function
- Predictable size and speed

Hard IP:
("physical")

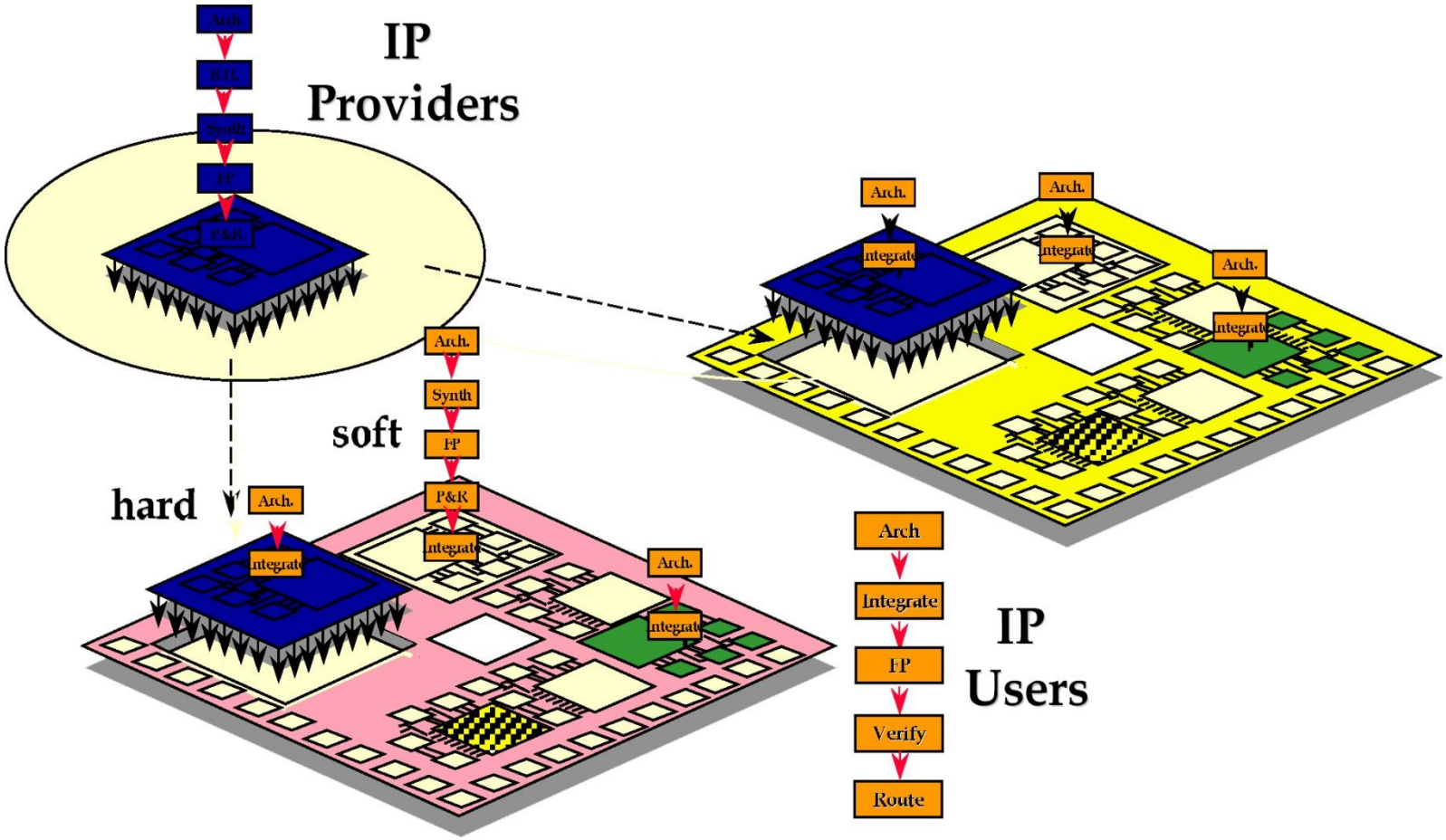
- Polygon level data
- Technology specific
- Fixed form & function
- Well characterized



Soft IP: ("Core")

- RT level or above
- Technology portable
- Flexible form & function
- Estimated size and speed

Core(IP)-Based Design



Criteria in Selecting IP's

- Processor IP selection criteria
  - Power, performance, area, cost
  - Flexibility
  - Hardness (hard IP vs. soft IP)
  - Available system software
  - Development environment
  - Simulation model
  - Support library
  - Support OS
  - Inter-operability with other IP's

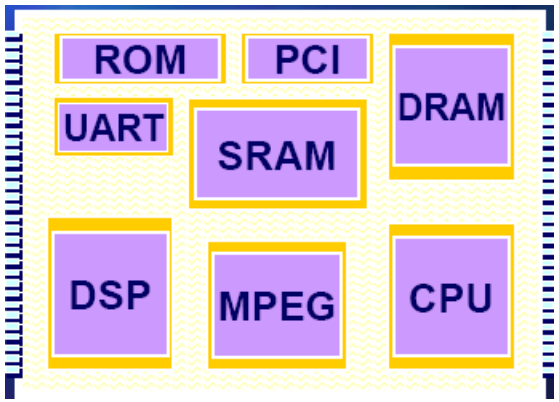
Differences in Design Between IC and IP

- **Limitation of IC design**
  - Number of I/O pin
  - Design and Implement all the functionality in the silicon
- **Hard IP**
  - No limitation on number of I/O pin
  - Provide multiple level abstract model
  - Design and Implement all the functionality in the layout
- **Soft IP**
  - No limitation on number of I/O pin
  - Parameterized IP Design: design all the functionality in HDL code but implement desired parts in the silicon
  - IP compiler/Generator: select what you want !!
  - More high level auxiliary tools to verify design
  - More difficult in chip-level verification

SoC and SIP

- System-on-Chip (SoC)
- Semiconductor Intellectual Property (SIP)
  - Also known as cores, virtual components (VCs)
  - Memory, processors, DSPs, I/O, peripheral

- SoC = ∑ IPs ?



Outline

- IC Industry Segments
- IC Design Flow
- Conquer SoC Design Complexity
- What is the Intellectual Property?
- SOC Design Considerations
- Platform-based Design Methodology
- Conclusion

SoC Design Considerations

- Architecture strategy
- Synthesis and backend strategy
- Integration strategy
- Design-for-test strategy
- Verification and Validation strategy
  - Verification –checking the products meets the design spec
  - Validation-checking the products meets the users' need

Architecture Strategy

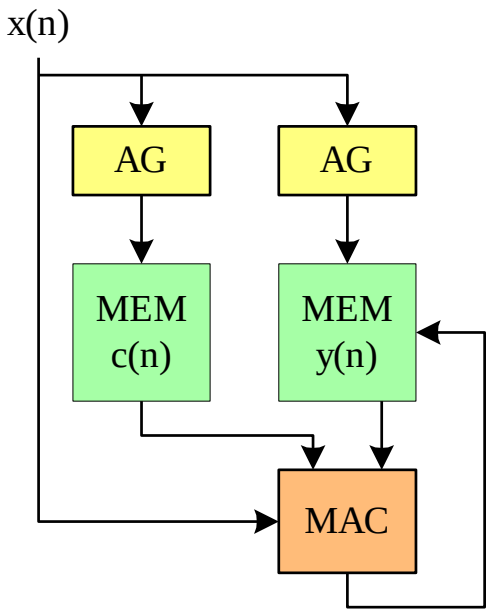
- **Reusable IPs (configurable)**
  - Central processing core
  - DSP cores
  - On chip bus
  - Easy plug-and-play IPs
  - I/O, peripherals
- **Platform-based design methodology**
  - Parameterization
  - Function partition

Why Configurable?

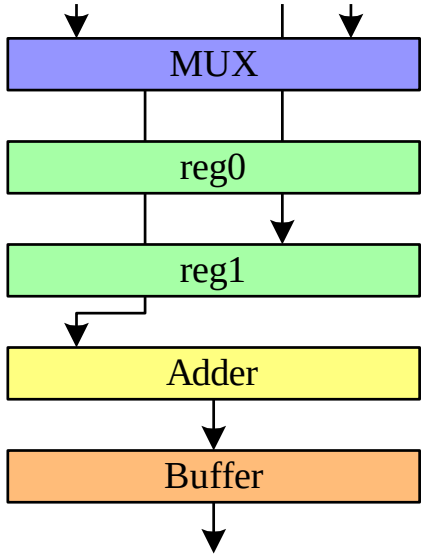
- **Reusable IP methodology**
  - Parameterization/Configurable
- **All IPs are typically customized to meet specific SoC specification**
- **Software upgradability**
- **Short product cycles**
- **E.g. External memory controller supports**
  - memory types (sync. Or async.)
  - Sizes,
  - Widths,
  - Banks,
  - Etc.

PE Granularity

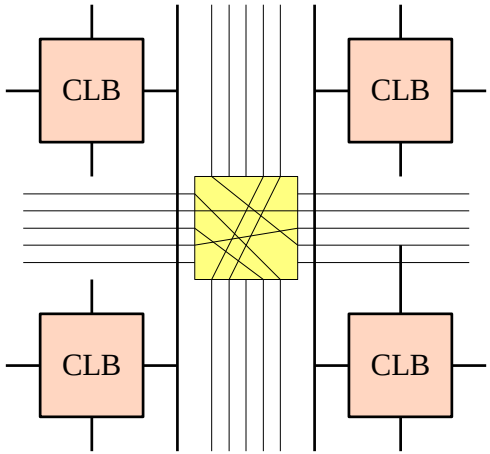
- Smallest unit of the reconfigurable fabric that can be reprogrammed
- tradeoffs between flexibility and reconfiguration overhead



Reconfigurable Dataflow



Reconfigurable Datapath

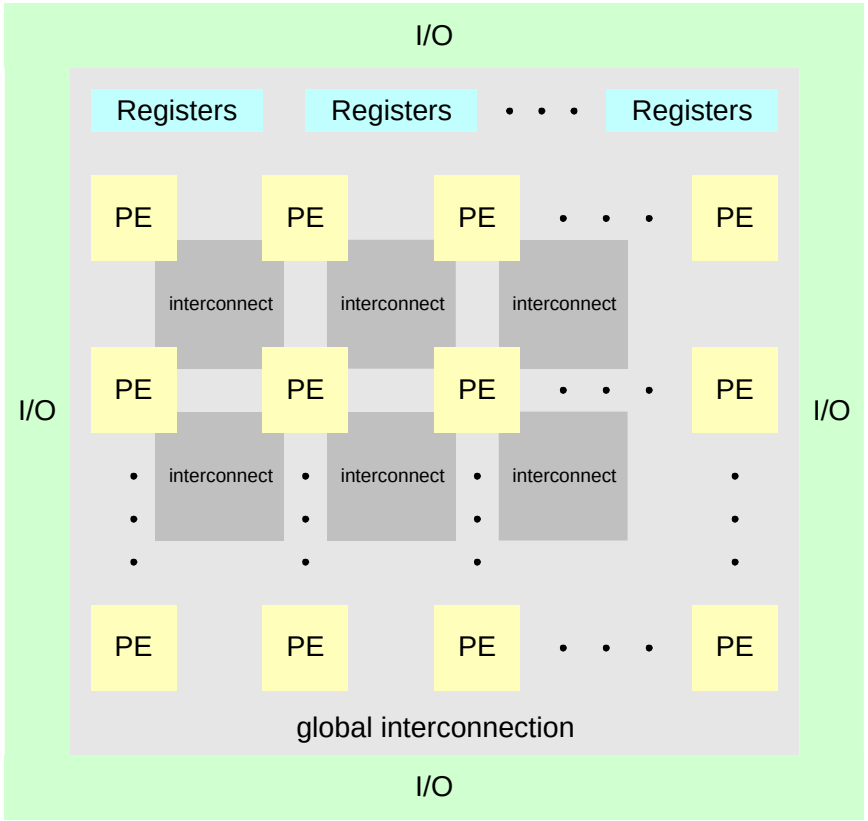


Reconfigurable Logic

General-Purpose Metamer

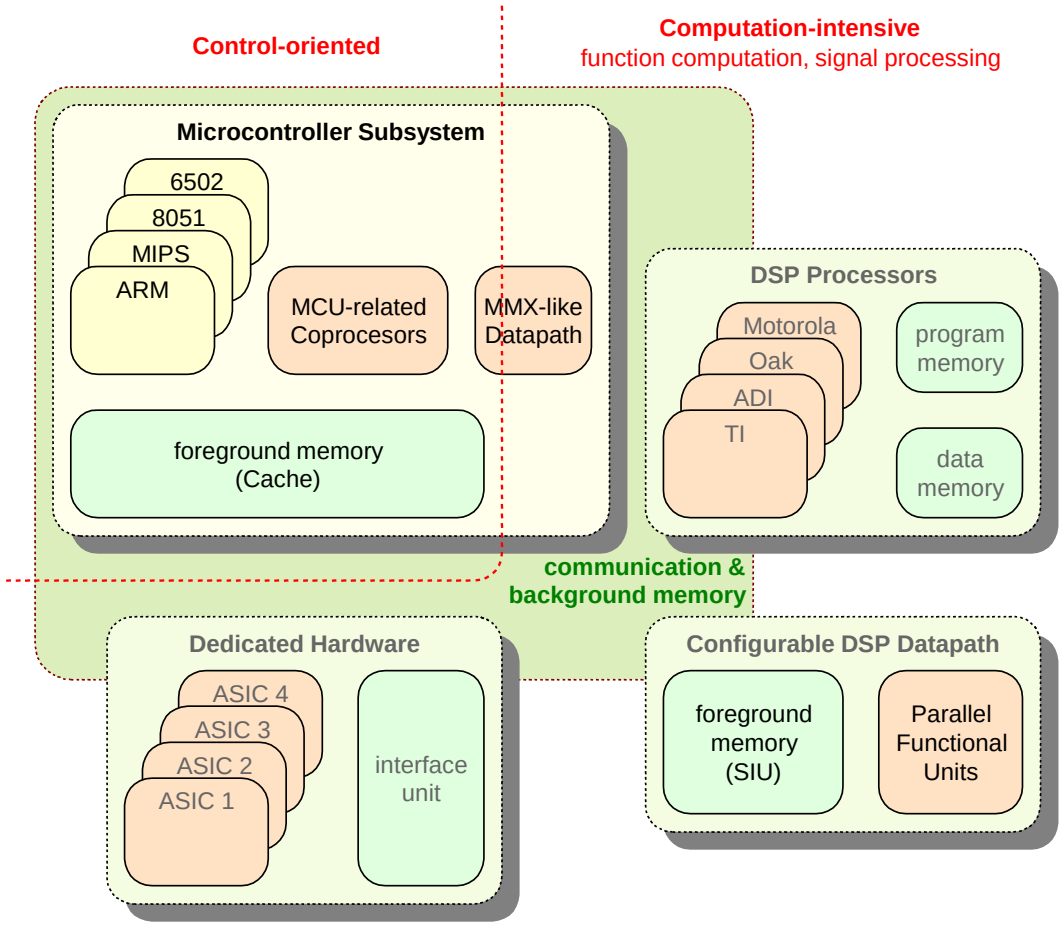
- Function partition
- PE granularity

  (usually imply # of functionalities)
- Interconnection routability
  - neighbor (1-D) / mesh (2-D)
  - crossbar
  - bus
- Initialization mechanism
- Configuration overhead
- Metamer—colors have similar visual effect but different spectral composition



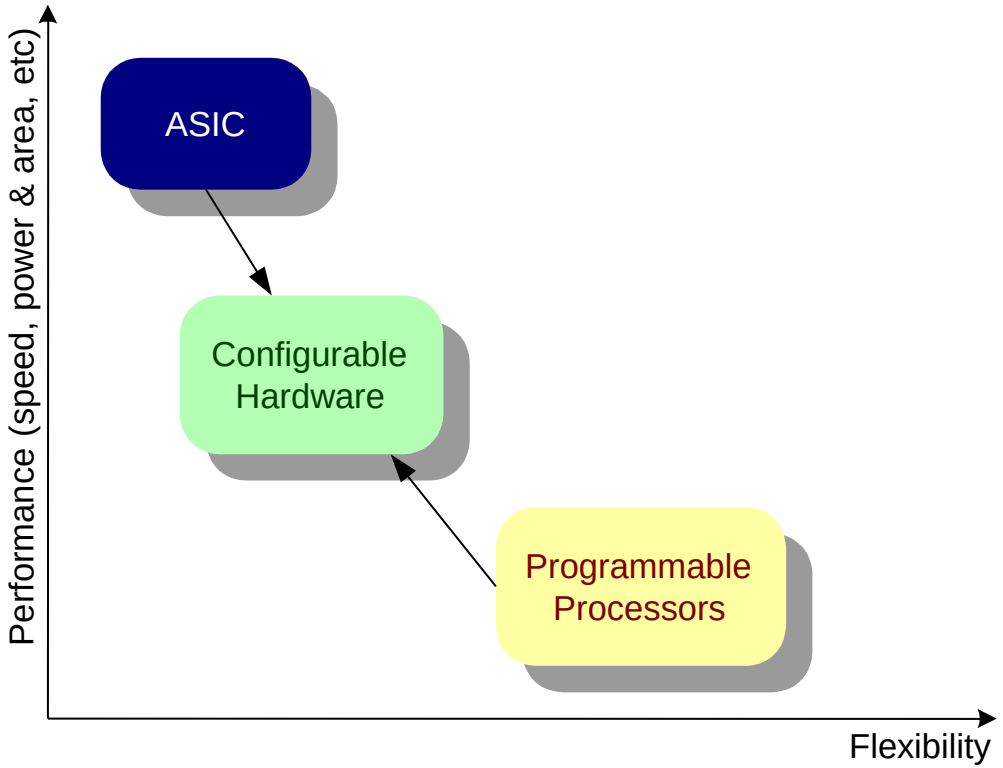
Alternative Computing Subsystem

- **Function partition**
- Control-dominated subsystem
  - controls & coordinates system tasks
  - performs ***reactive*** tasks
  - (e.g. user interface)
- Data-dominated subsystem
  - regular & predictable ***transformational*** tasks
  - well-defined DSP kernels with high parallelism



Remark: Silicon Pendulum

- *standardization*
  - flexibility
  - time to market
  - cost effectiveness
- *customization*
  - performance
  - differentiation
  - value addition



SoC: A Finer View

- **SoC = ∫ (IPs + Platform)**

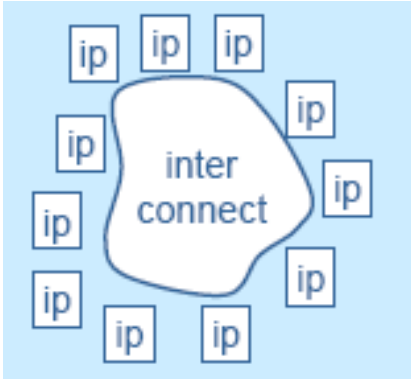
- **Platform, or Semiconductor Infrastructure IP**

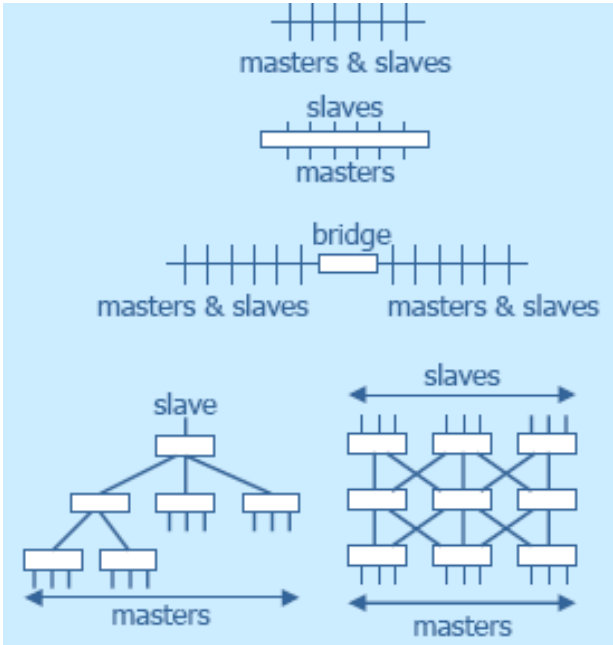
-A platform **is a suite of reusable parts (IP) of many system designs connected in a limited spectrum of applications**

  - Interconnect/Inter-block communication
  - Performance optimization
  - Test
  - Diagnosis
  - Repair
  - Power management
  - …

On-Chip-Bus, OCB

- **Requirements**
  - Have to connect many local IPs
    - Heterogeneous traffic
    - Scalable capability
    - QoS
- **Types**
  - Wire (zero hop)
  - Bus (single hop)
  - Switch, router (multi-hop)
  - Circuit-switched
  - Packet-switched

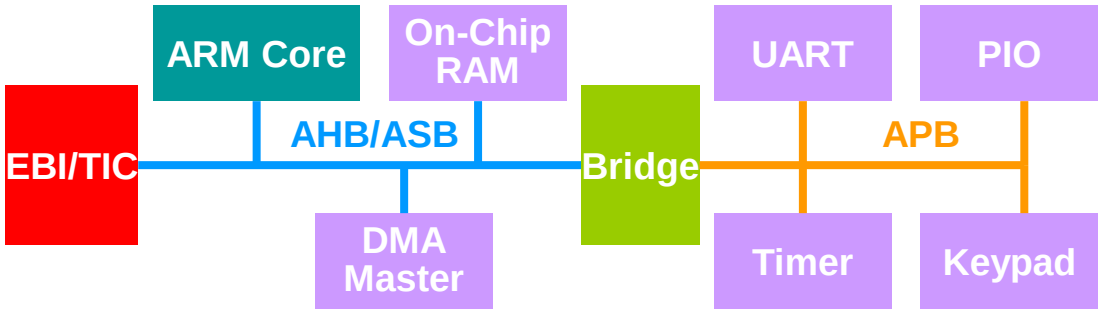




Source: Philips

Example: ARM OCB - AMBA

- Advanced Microcontroller Bus Architecture (AMBA)
- AMBA 2.0 specifies
  - the Advanced High-performance Bus (AHB)
  - the Advanced System Bus (ASB)
  - the Advanced Peripheral Bus (APB)
  - test methodology



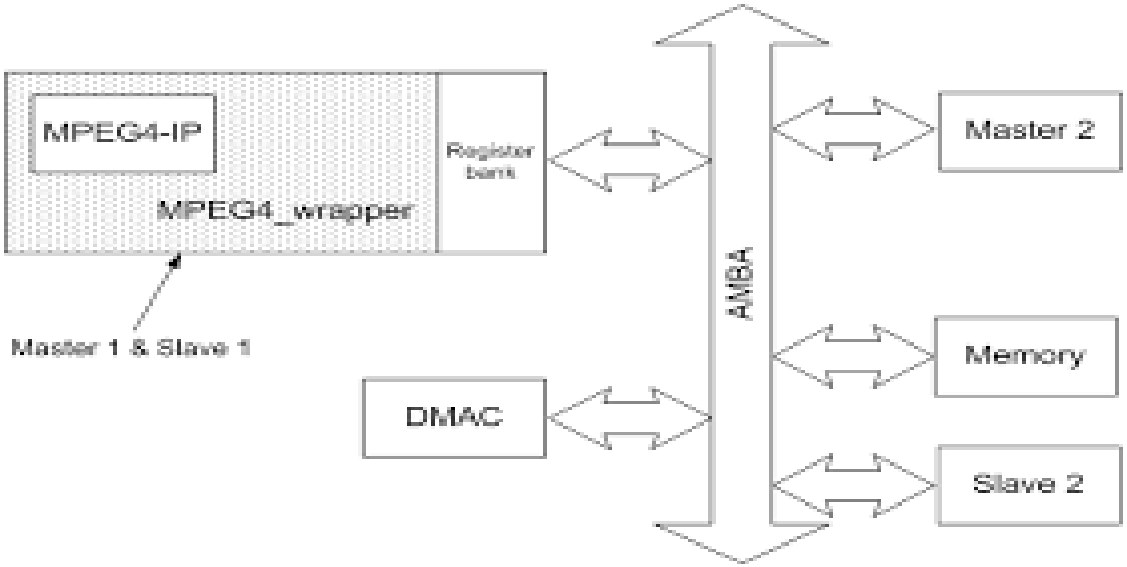
A typical AMBA system

AMBA Bus Types

- the Advanced High-performance Bus (AHB)
  - Connecting high frequency system modules such as processors, on-chip memories, off-chip external memories for high performance backbone bus. Bus width up to 1024 bit
- the Advanced System Bus (ASB)
  - an alternative system bus suitable for use where the high-performance features of AHB are not required. Bus width ~32b
- the Advanced Peripheral Bus (APB)
  - for minimal power consumption and reduced interface complexity to support peripheral functions

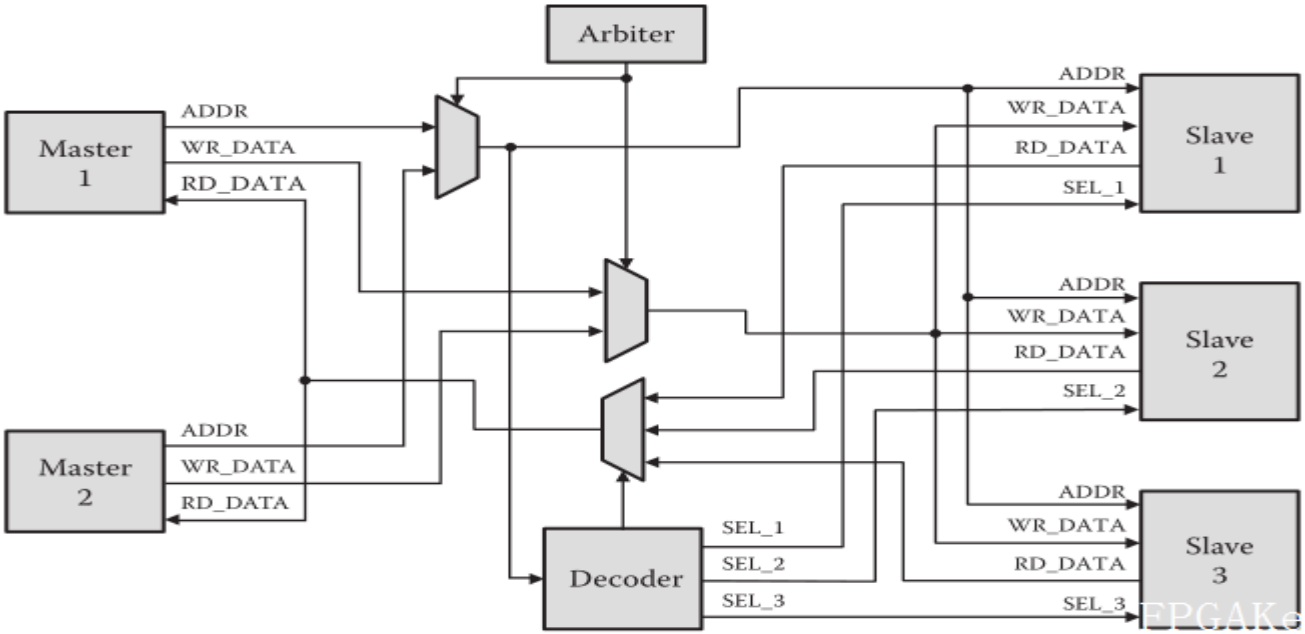
AMBA AHB Wrapper Design

- MPEG4 in AMBA design
  - MPEG2 IP is a master
  - Register Bank is a slave
  - Wrapper contains one master and one slave



AMBA AHB Bus Interconnect

- AHB Interconnect
  - central multiplexor interconnection scheme
  - masters drive out the address and control signals
  - arbiter determines which master has its address and control signals routed to all of the slaves.
  - central decoder is also required to control the read data and response signal multiplexor,

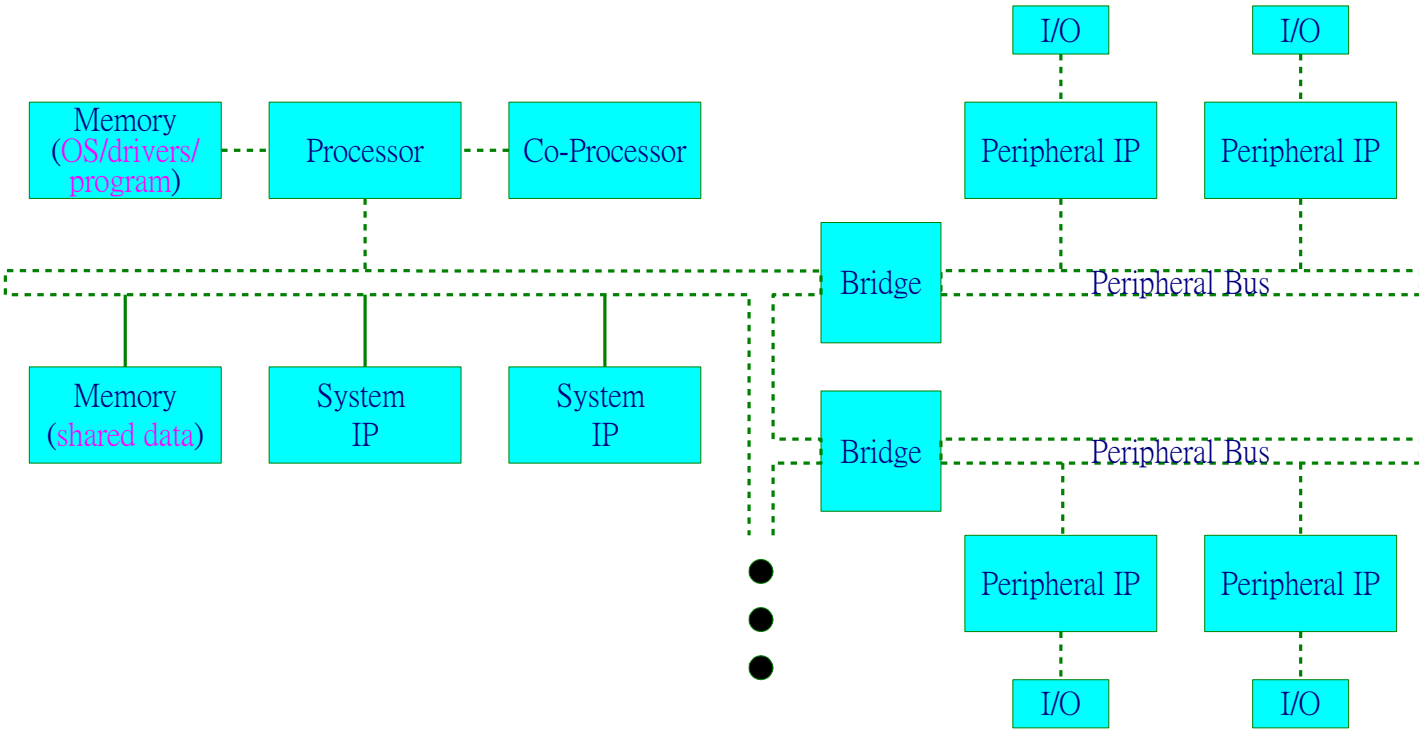


Virtual Component Interface (VCI)

- **What is VCI**
  - A request-response protocol, contents and coding, for the transfer of requests and responses
- **Why VCI**
  - Other IP blocks not available ‘wrapped’ to the on-chip communications may work with IP wrappers. VSI Alliance VCI is the best choice to start with for an adaptation layer
- **VCI specifies**
  - Thee levels of protocol
    - Advanced VCI (AVCI),
    - Basic VCI (BVCI), and
    - Peripheral VCI (PVCI)
  - Transaction language

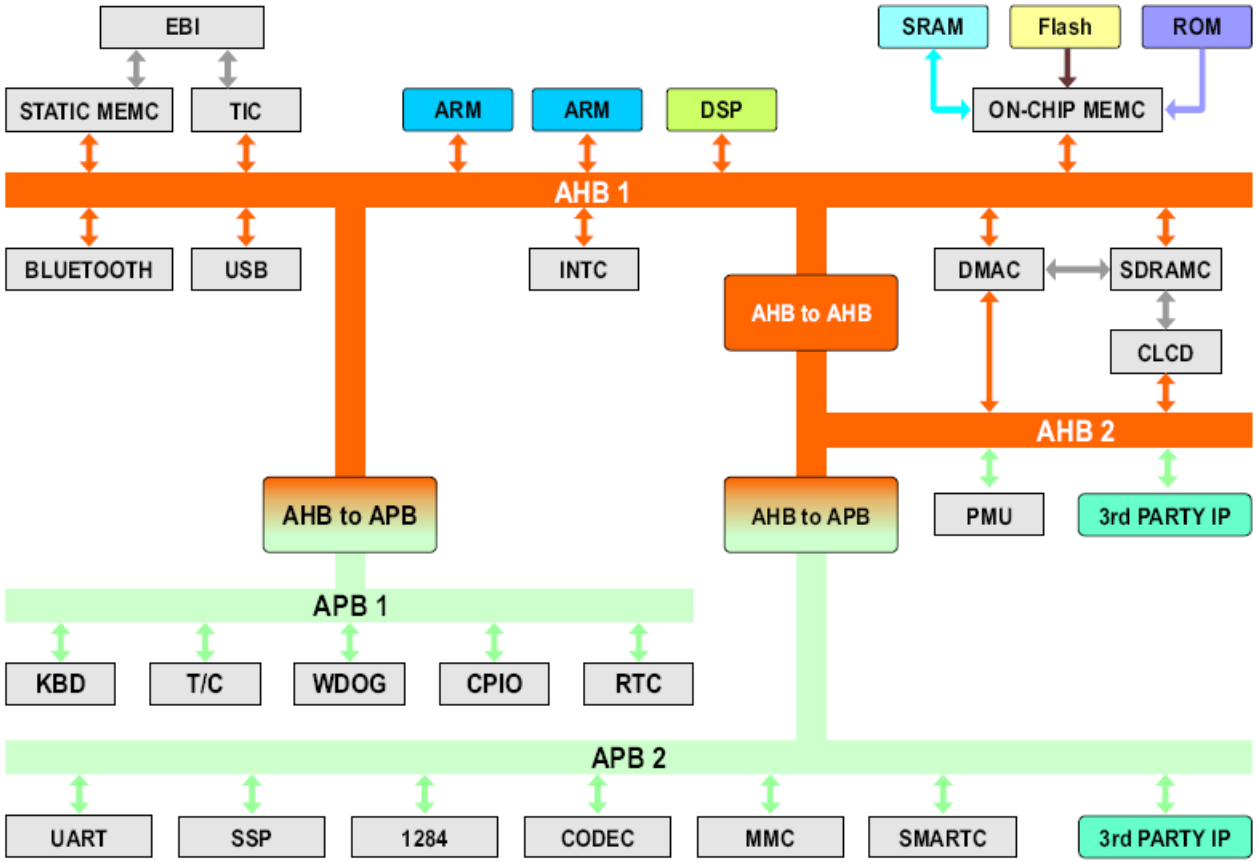
Platform

- A platform **is a suite of reusable parts (IP) of many system designs connected in a limited spectrum of applications**



Source: SOC Design Overview /MOE, R.O.C.

Platform Example

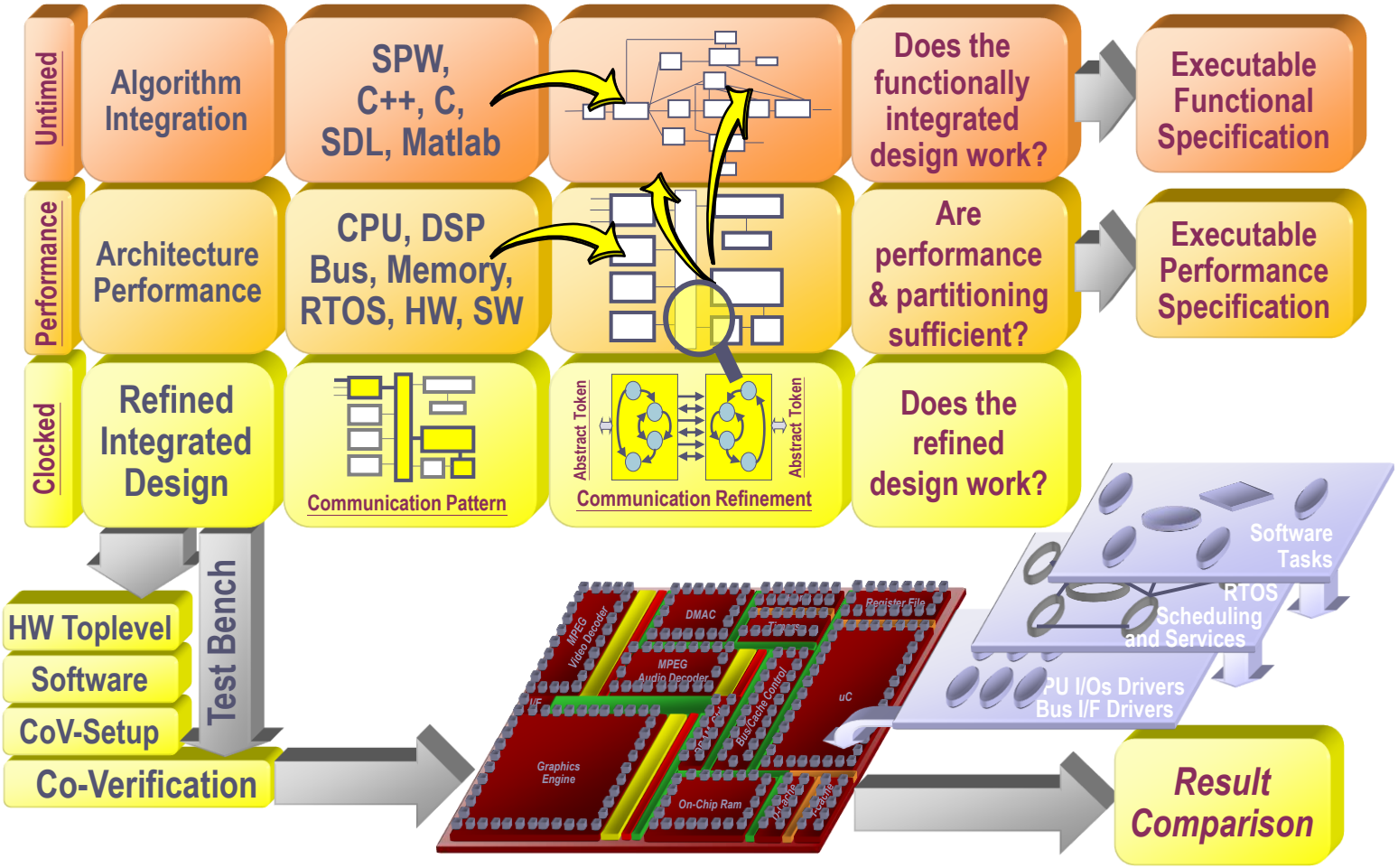


Wipro's ARM-based SoC-RapTor Platform

Benefits of Platform-based Design

- **Simplify backbone design:**
  - A platform provides an architecture reference which is proved to be a applicable architecture.
  - Simple modification is enough to be suitable to similar systems.
- **Save repetitive design time:**
  - Existing IPs for the platform can be adopted to accelerate the build up time.
  - Based on existing platform ease the replace of custom design.
- **Ease the verification:**
  - The environment provided by a platform helps to verify the custom modification in each step.
- **Early evaluation:**
  - A virtual prototyping provides early system performance data and H/S partitioning information.

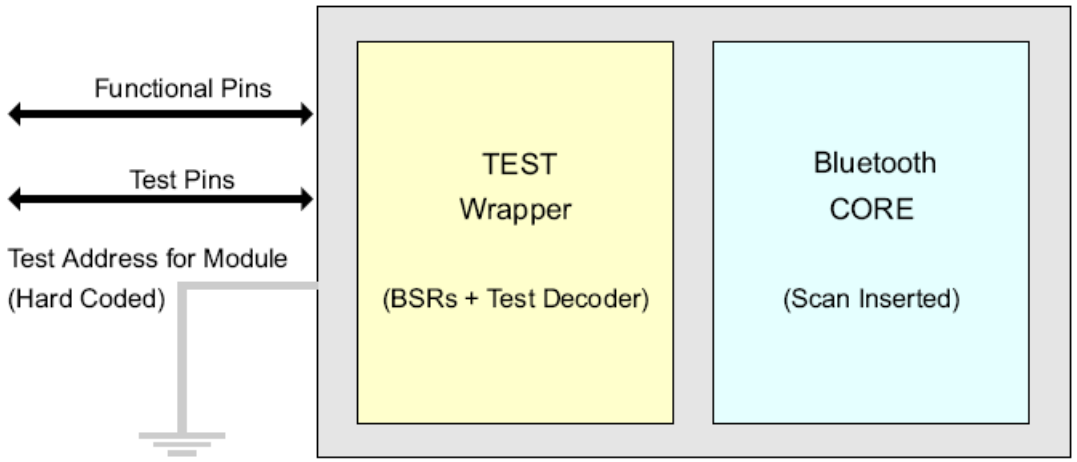
Hardware, Software and Testbench Export



Source: Cadence

Design for Test (DFT) Strategy

- DFT is usually implemented using a full scan, muxed flip-flop of scan insertion.
- For embedded memories, Built in Self-test (BIST) and Module Test are best used.

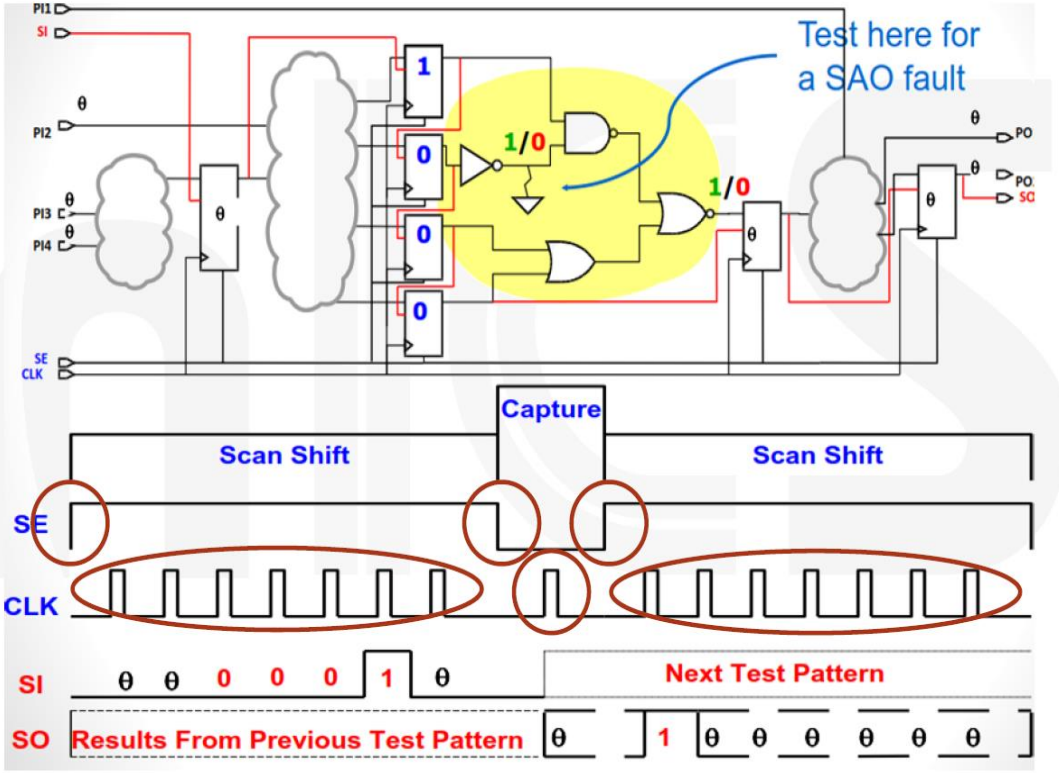


Design for Test (DFT) Strategy

- DFT is usually implemented using a full scan, muxed flip-flop of scan insertion.

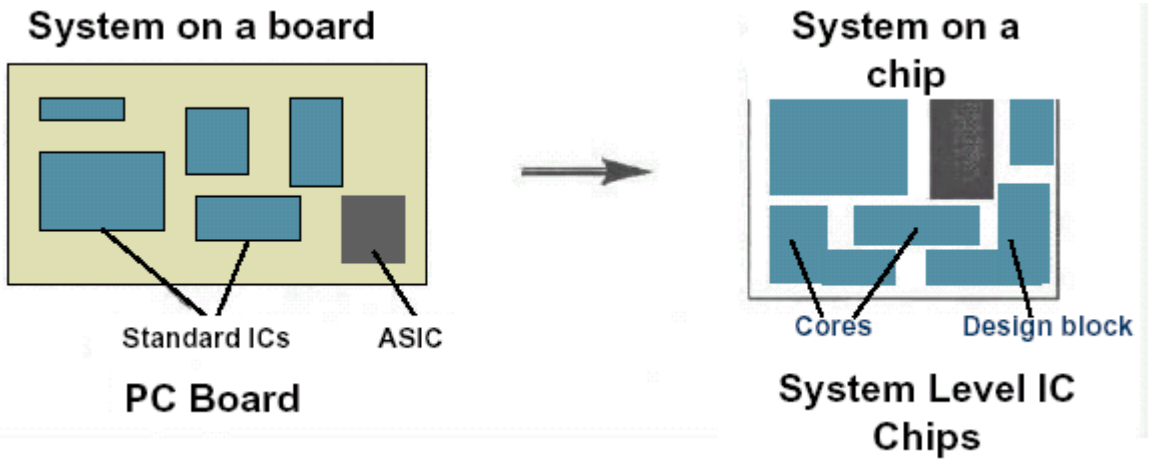
Scan Testing Protocol

- Enable scan (SE=1)
- Shift in state vector
- Disable scan (SE=0)
- Toggle Clock to exercise fault ("Capture")
- Enable scan (SE=1)
- Shift out result vector



Benefits of Using SoC

- Reduce overall system cost
- Increase performance
- Lower power consumption
- Reduce size



SoC - New Design Era

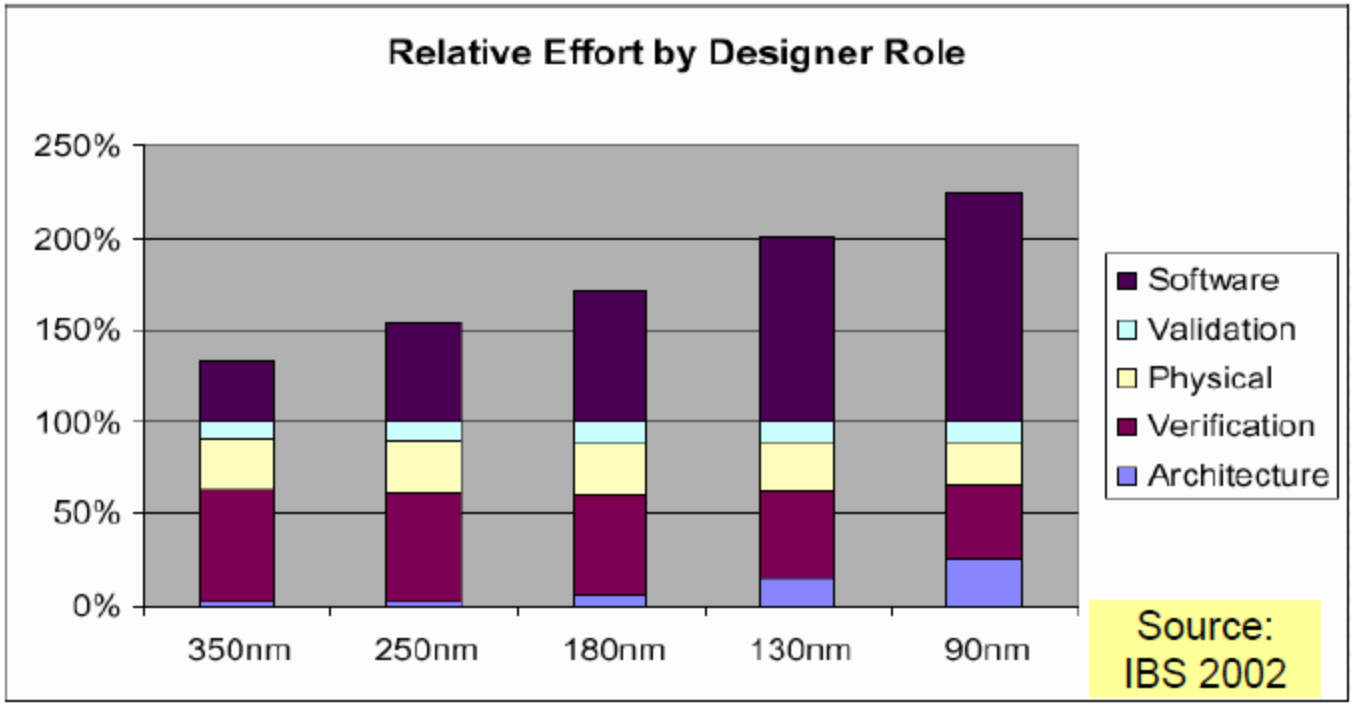
New design consideration

- Design methodology ◂ Platform-based design ▸
- Functionality implementation
  - Personal reuse
  - In-house reuse
  - IP reuse
  - Architecture reuse
  - Parameterized and blockwise design
  - IP Compiler/Generator

Reuse without redesign

- Multi-level design descriptions
- Physical design consideration/constraint

SoC Design + Rising Complexity

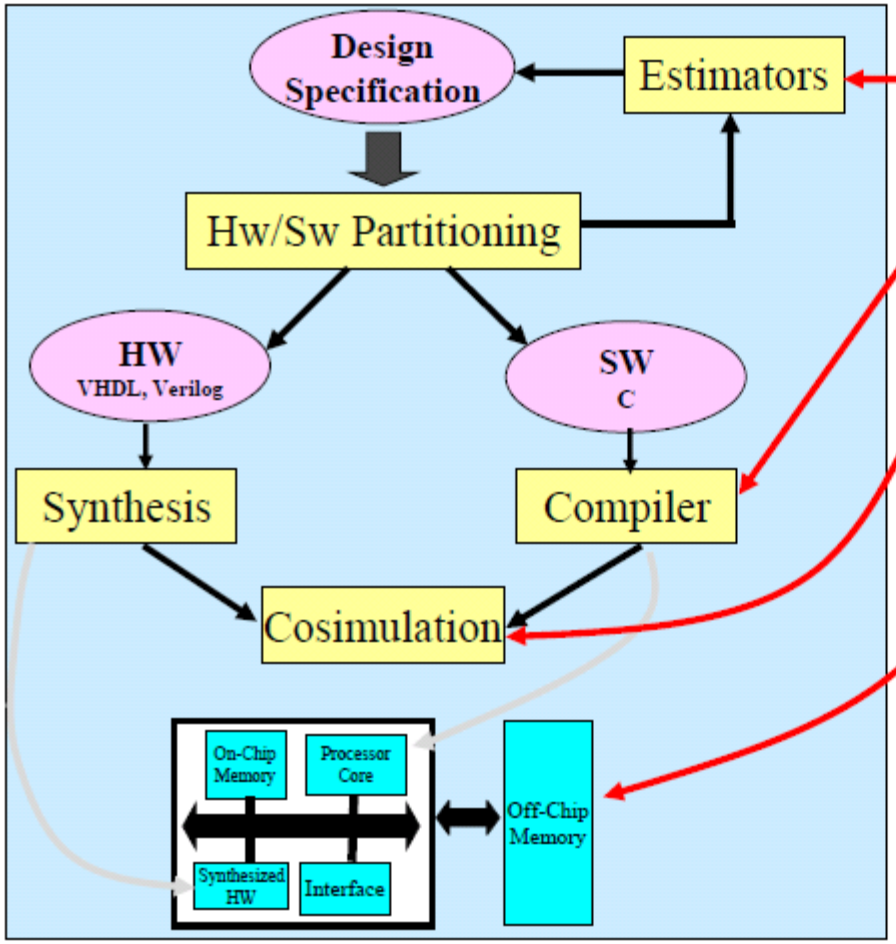


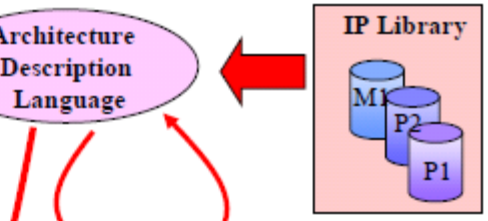
* Software costs overtake total hardware costs at 130nm
* Architecture effort overtakes physical design at 90nm

Key Trends: Embedded S/W content in SOC is way up

- eS/W: Current application complexity
  - Set-top box: >1 million lines of code
  - Digital audio processing: >1 million lines of code
  - Recordable DVD: Over 100 person-years effort
  - Hard-disk drive: Over 100 person-years effort
- In multimedia systems
  - S/W cost (licenses) 6X larger than H/W chip cost
  - eS/W uses 50% to 80% of design resources
- eS/W now an essential part of SoC products

SoC HW/SW Co-design





- Rapid design space exploration
- Quality tool-kit generation
- Design reuse

SoC Current Status

- Time-to-market pressure
- ASIC/ASSP (Application specific standard product) ratio: 80/20 in 2000, but 50/50 now
- In-house ASIC design is down, replaced by off-the-shelf, programmable ASSP

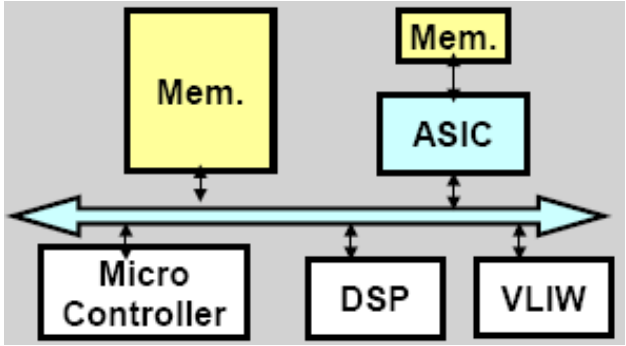
- Number embedded processors in SoC rising:
  - ST: recordable DVD 5
  - Hughes: set-top box 7
  - Agere: Wireless base station 8
  - ST: HDTV platform 8
  - Latest mobile handsets 10
  - NEC: Image processor 128
  - ST: NPU >150

Next Generation SoC Objectives

- **Flexibility**

  -softer systems:eFPGA. eSOC, eProcessors, combined with standard H/W IP

- **Fast Platform Implemenation**
  - Use of synthesizable, off-shelf IP
  - Scalable SoC interconnect
  - Trend towards standarized platform
  - Need clear programming model



Top Semiconductor Companies

- Top ten semiconductor companies Revenue

1H20 Top 10 Semiconductor Sales Leaders ($M, Including Foundries)

1H20 Rank	1H19 Rank	Company	Headquarters	1Q20 Total IC	1Q20 Total O-S-D	1Q20 Total Semi	2Q20 Total IC	2Q20 Total O-S-D	2Q20 Total Semi	2Q20/1Q20 % Change	1H20 Total Semi	1H19 Total Semi	1H20/1H19 % Change
1	1	Intel	U.S.	19,508	0	19,508	19,443	0	19,443	0%	38,951	32,038	22%
2	2	Samsung	South Korea	13,939	858	14,797	14,078	875	14,953	1%	29,750	26,671	12%
3	3	TSMC (1)	Taiwan	10,319	0	10,319	10,398	0	10,398	1%	20,717	14,845	40%
4	4	SK Hynix	South Korea	5,829	210	6,039	6,848	212	7,060	17%	13,099	11,558	13%
5	5	Micron	U.S.	5,004	0	5,004	5,620	0	5,620	12%	10,624	10,175	4%
6	6	Broadcom Inc. (2)	U.S.	3,671	408	4,079	3,625	405	4,030	-1%	8,109	8,346	-3%
7	7	Qualcomm (2)	U.S.	4,050	0	4,050	3,807	0	3,807	-6%	7,857	7,289	8%
8	10	Nvidia (2)	U.S.	3,073	0	3,073	3,452	0	3,452	12%	6,525	4,674	40%
9	8	TI	U.S.	2,974	190	3,164	2,890	187	3,077	-3%	6,241	6,884	-9%
10	16	HiSilicon (2)	China	2,670	0	2,670	2,550	0	2,550	-4%	5,220	3,500	49%
—	—	Top-10 Total		71,037	1,666	72,703	72,711	1,679	74,390	2%	147,093	125,980	17%

(1) Foundry (2) Fabless

Source: Company reports, IC Insights' *Strategic Reviews* database

Semiconductor optoelectronic, sensor, and discrete (O-S-D) sales

Top Semiconductor Companies

- Top ten semiconductor companies Revenue

2Q21 Top 10 Semiconductor Sales Leaders ($M, Including Foundries)

2Q21 Rank	1Q21 Rank	Company	Headquarters	1Q21 Total IC	1Q21 Total O-S-D	1Q21 Total Semi	2Q21 Total IC	2Q21 Total O-S-D	2Q21 Total Semi	2Q21/1Q21 % Change
1	2	Samsung	South Korea	16,152	920	17,072	19,262	1,035	20,297	19%
2	1	Intel	U.S.	18,676	0	18,676	19,304	0	19,304	3%
3	3	TSMC (1)	Taiwan	12,911	0	12,911	13,315	0	13,315	3%
4	4	SK Hynix	South Korea	7,270	358	7,628	8,762	451	9,213	21%
5	5	Micron	U.S.	6,629	0	6,629	7,681	0	7,681	16%
6	6	Qualcomm (2)	U.S.	6,281	0	6,281	6,472	0	6,472	3%
7	8	Nvidia (2)	U.S.	4,842	0	4,842	5,540	0	5,540	14%
8	7	Broadcom Inc. (2)	U.S.	4,364	485	4,849	4,400	490	4,890	1%
9	10	MediaTek (2)	Taiwan	3,849	0	3,849	4,496	0	4,496	17%
10	9	TI	U.S.	3,793	235	4,028	4,030	269	4,299	7%
—	—	Top-10 Total		84,767	1,998	86,765	93,262	2,245	95,507	10%

(1) Foundry (2) Fabless

Source: Company reports, IC Insights' *Strategic Reviews* database

Top Fabless Companies

- Top ten fabless companies Revenue

Table: 2019 Revenue Ranking of Top 10 IC Design Companies (Unit: Million USD)

Ranking	Company	2019 Revenue	2018 Revenue	YoY
1	Broadcom	17,246	18,547	-7.0%
2	Qualcomm	14,518	16,370	-11.3%
3	NVIDIA	10,125	11,163	-9.3%
4	MediaTek	7,962	7,882	1.0%
5	AMD	6,731	6,475	4.0%
6	Xilinx	3,234	2,868	12.8%
7	Marvell	2,708	2,823	-4.1%
8	Novatek	2,085	1,813	15.0%
9	Realtek	1,965	1,518	29.4%
10	Dialog	1,421	1,442	-1.5%
Top 10 Total		**67,995**	**70,901**	**-4.1%**

Notes:

1. This table shows only the top 10 IC design companies with publicly disclosed earnings
2. Broadcom's revenue includes its semiconductor business only
3. Qualcomm's revenue includes its QCT business only and not QTL
4. NVIDIA's revenue excludes its OEM/IP businesses

Source: TrendForce, Mar. 2020

Top Fabless Companies

- Top ten fabless companies Revenue

Table 1: Revenue Ranking of Top 10 IC Design Companies, 2Q21 (Unit: Million USD)

Rank	Company	2Q21 Revenue	2Q20 Revenue	YoY Growth
1	Qualcomm	6,472	3,807	70.0%
2	Nvidia	5,843	3,461	68.8%
3	Broadcom	4,954	4,155	19.2%
4	MediaTek	4,489	2,259	98.8%
5	AMD	3,850	1,932	99.3%
6	Novatek	1,219	622	96.0%
7	Marvell	995	716	38.9%
8	Xilinx	879	727	20.9%
9	Realtek	834	579	44.0%
10	Dialog	318	302	5.1%
Top 10 Total		29,852	18,560	60.8%

Notes:
1. This table shows only the top 10 IC design companies with publicly disclosed earnings.
2. Nvidia's revenue excludes its OEM/IP businesses.
3. Qualcomm's revenue includes its QCT business only; Broadcom's revenue includes its semiconductor business only.
4. 2Q21 USD:TWD = 1:27.99; 2Q20 USD:TWD = 1:29.93
Source: TrendForce, Sep. 2021

Reference

- **http://vada.skku.ac.kr/ClassInfo/system_level_design/**
- “System Modeling – Model of Computation and their Applications,” Axel Jantsch LECS, Royal Institute of Technology, Stockholm, Sweden Jan, 2004.
- “Winning the SoC Revolution-Experiences in Real Design,” Grant Martin & Henry Chang, Cadence Labs, KAP, Jun, 2003.
- “Reuse Methodology Manual,” Michael Keating & Pierre Bricaud, KAP, 2003.
- “System Design and Methodology: Modeling and Design of Embedded Systems,” Petru Eles, Linkopings Univ., Sweden
- “Embedded Systems Design,” Frank Vahid, Tony Givargis, John Wiley & Sons, Inc., 2002.
- “Memory Issues in Embedded Systems-on-Chip,” Preeti Ranjan Panda, (Synopsys, Inc.) Nikil Dutt,(Univ. of Cal/Irvine), Alexandru Nicolau(Univ. of Cal/Irvine), KAP 1999.