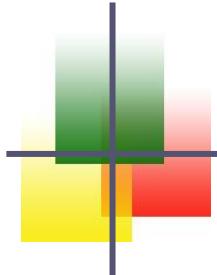




*System On Chip*

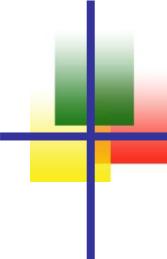
教育部商管學程系統晶片應用課程

## *Introduction to System-on-Chip and its Applications*



High Speed Interface  
for Various Applications





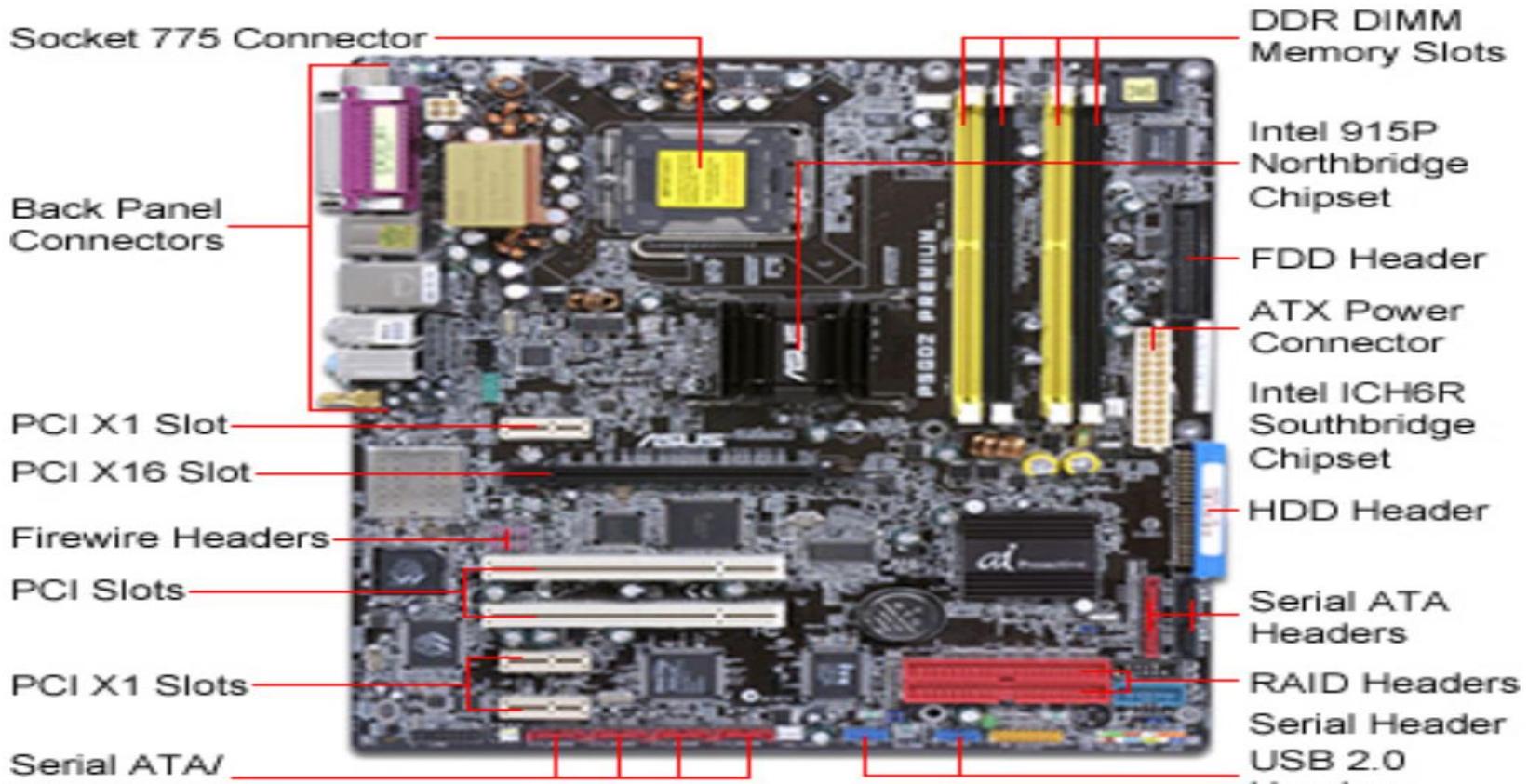
# Outline

---

- Overview
- Interconnect Basics
  - Definition
  - Functions
- Applications
  - Personal Computer
  - Home Entertainment
- Conclusions

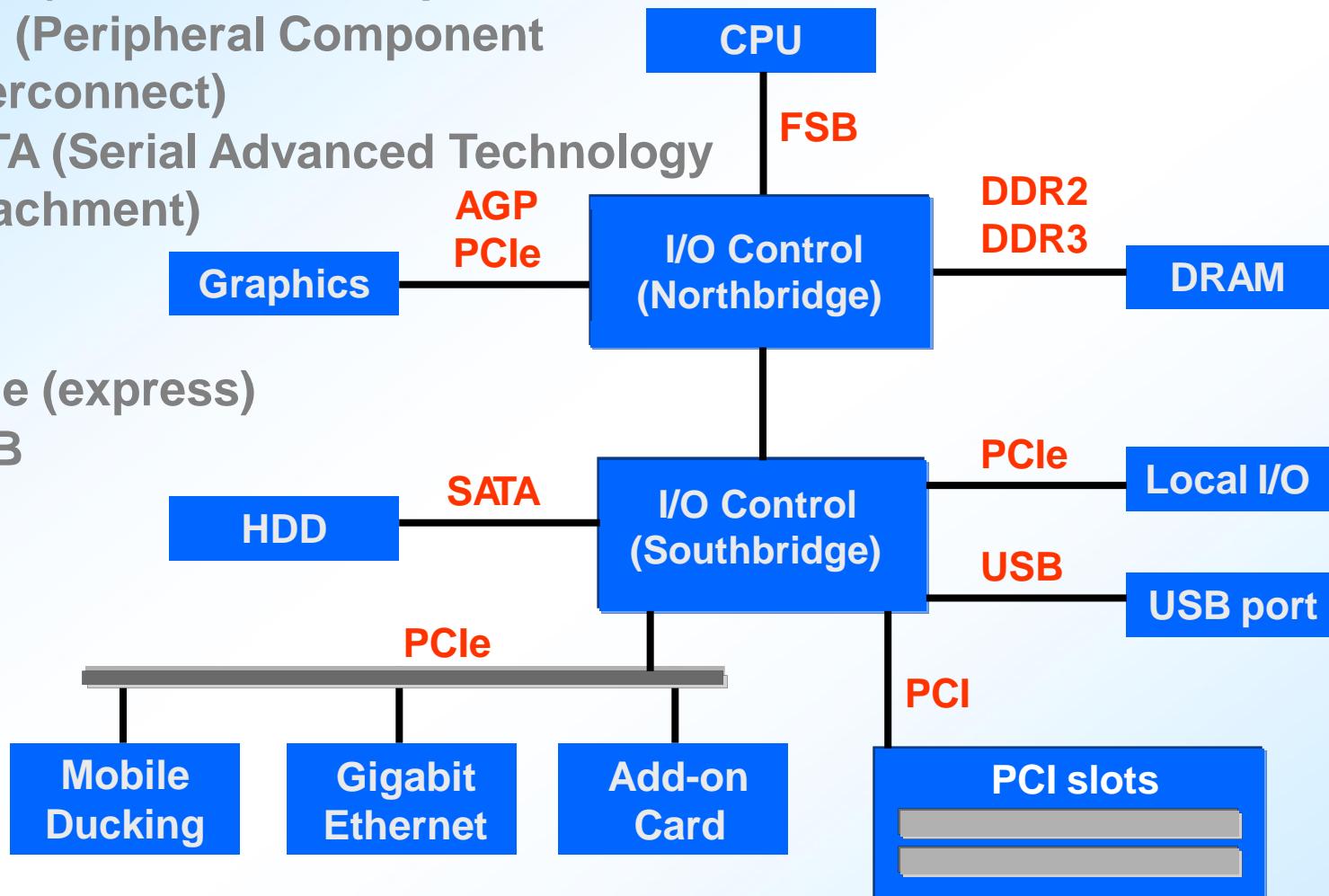
# PC motherboard Interconnect

- DDR slots –DRAM
- SATA slots –HDD (hard disk drive) /SSD
- PCI-E – graphic card
- HDMI – Monitor/Projector
- USB –flash memory



# Applications \_Personal computer

- FSB (Front Side Bus)
- AGP (Accelerated Graphics Port)
- PCI (Peripheral Component Interconnect)
- SATA (Serial Advanced Technology Attachment)

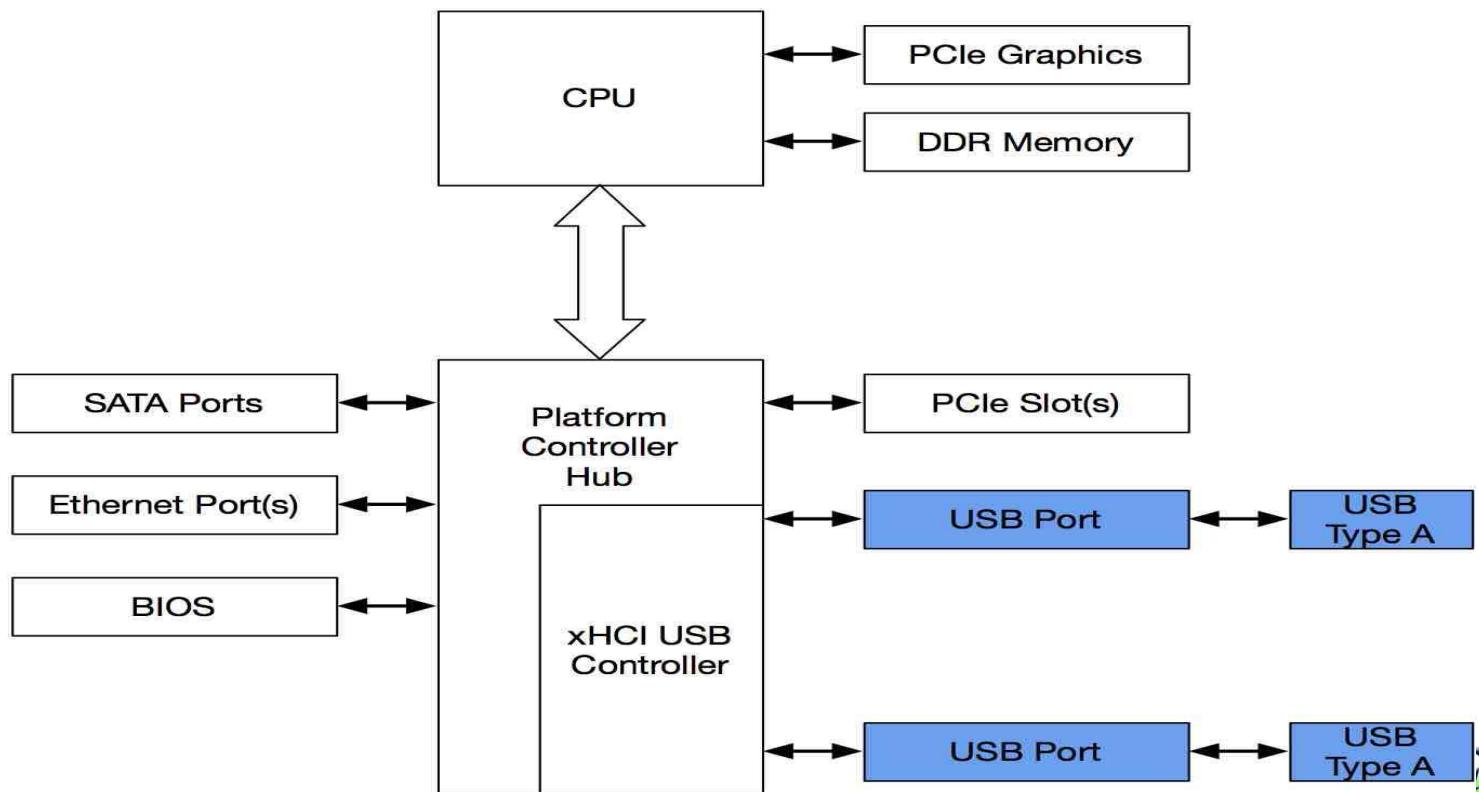


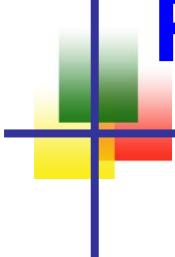
# CPU Interconnect Architecture

■ Parallel Bus: DDR slots –DRAM

■ Serial line:

- SATA slots –HDD (hard disk drive) /SSD
- PCI-E – graphic card /HDMI
- USB –flash memory





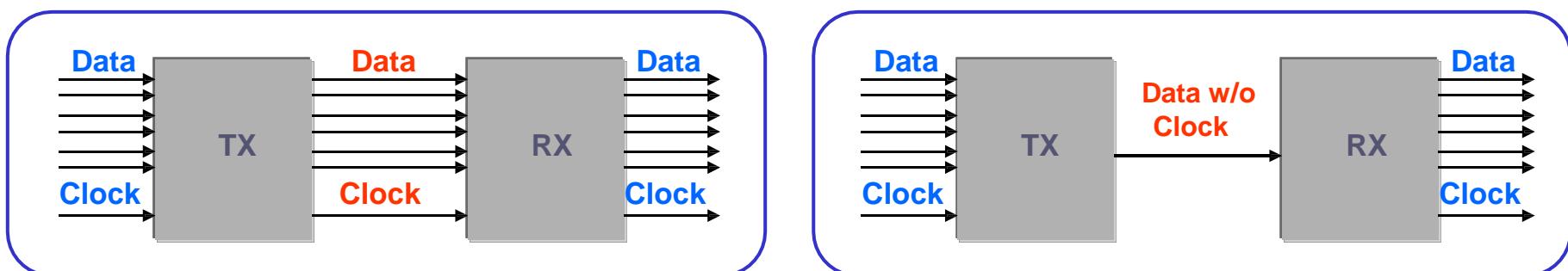
# Parallel vs Serial



## Parallel vs. Serial

- Familiar and quickly implemented
- Fast reaction time
- No Link layer required
- Source synchronous clock required
- Skew between data lines

- Much higher speed
- No skew : Longer distance
- Clock embedded in data
- Reduction of signal line counts
- Heavy Link layer

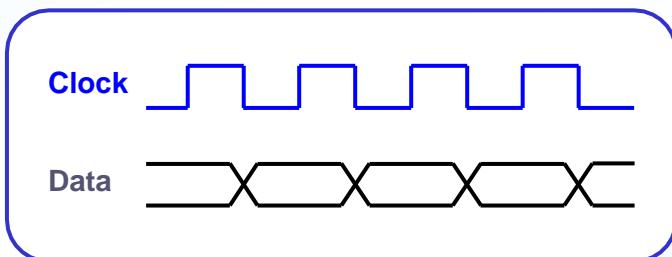


# Explicit vs Embedded clock



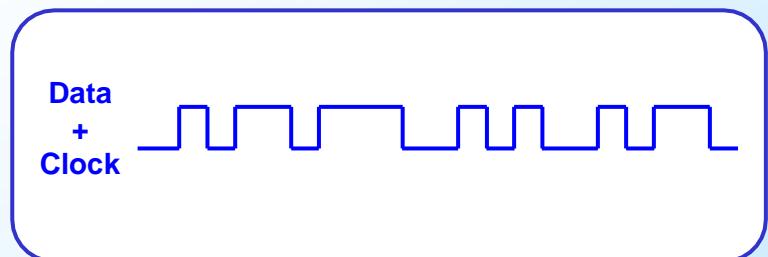
## Explicit Clock

- Intuitive
- Setup/Hold window check
- Clock Skew to data
- Easy Physical layer design
- Ex) LVDS



## vs. Embedded Clock

- Implicit
- Eye diagram check
- Free from skew problem
- Routing flexibility
- Extra encoding required (ex, 8b10b)
- Clock Recovery circuit required
- Ex) DisplayPort

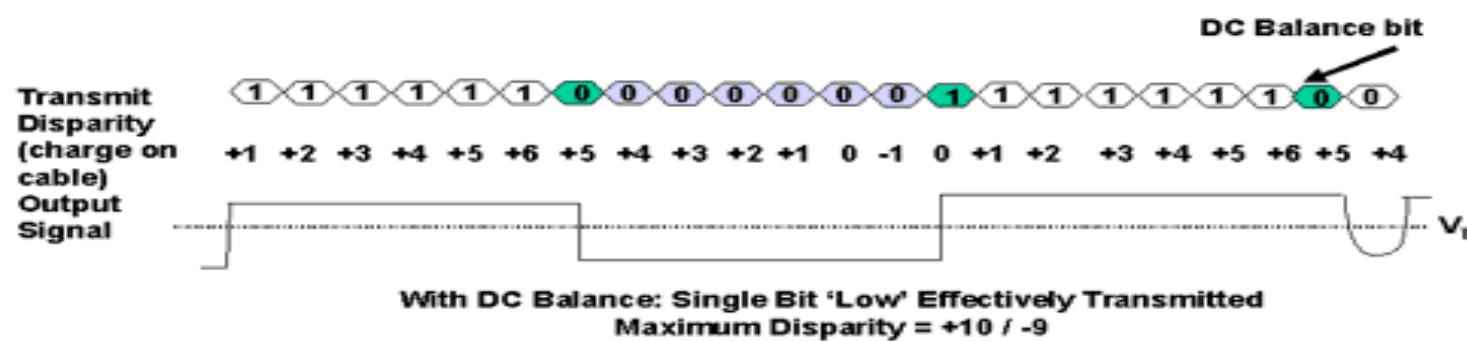
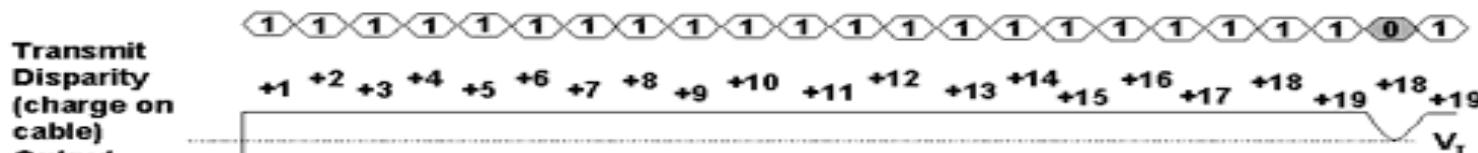


# DC-Balance Embedded Clock Coding

## ■ 8b/10b coding

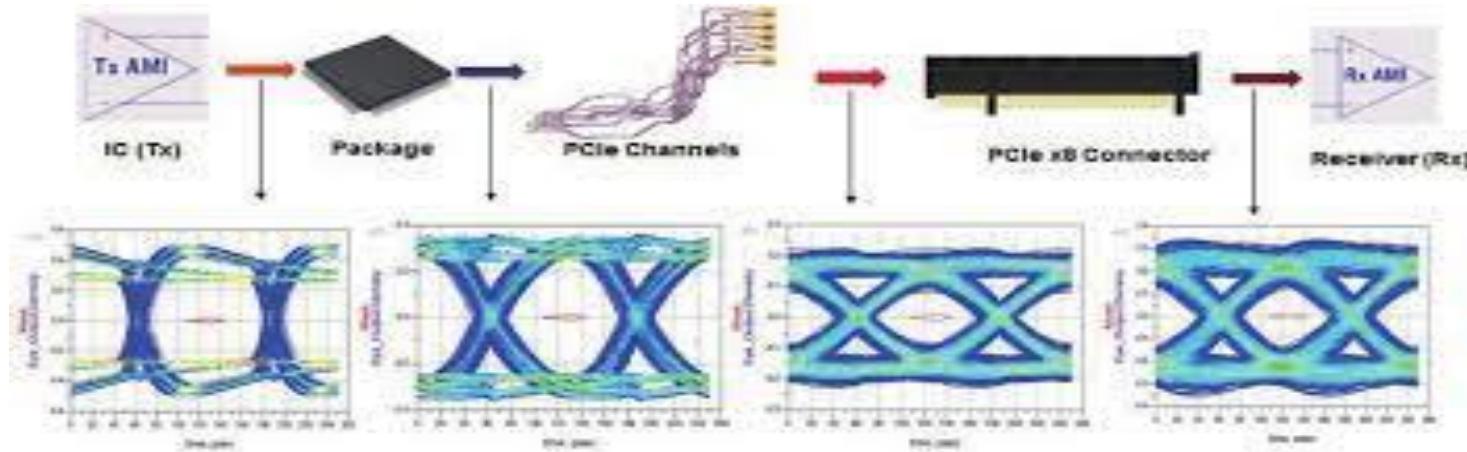
- maps 8-bit words to 10-bit symbols
- achieve DC-balance and Clock recovery
- Not more than 5 ones or zeros in a row
- Count of ones and zero difference is less than 2 in 20 bits

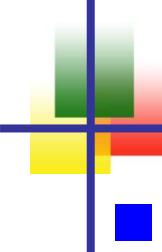
## ■ 128b/130b



# Speed Limiting Factors

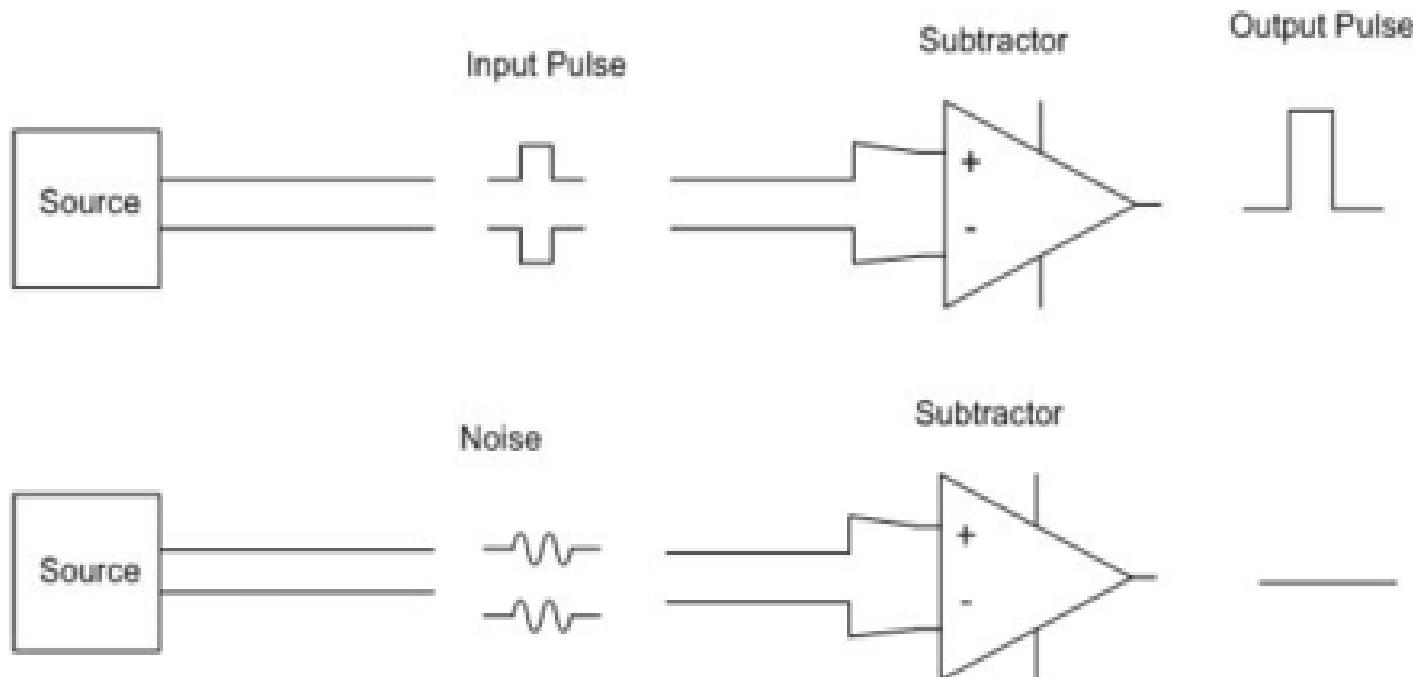
- Capacitive Loading from pad and lead frame
- **Reflection** from Transmission Line Discontinuity
- **Insertion loss**: attenuation from Dielectric Loss at high frequency (PCIe 5.0 at 32GT/s, total channel insertion loss budget is 36dB)
- **Crosstalk** caused by adjacent signal line
- Timing Skew between parallel signals
- Simultaneous Switching Noise (SSN)
- Inter-Symbol Interference (ISI)





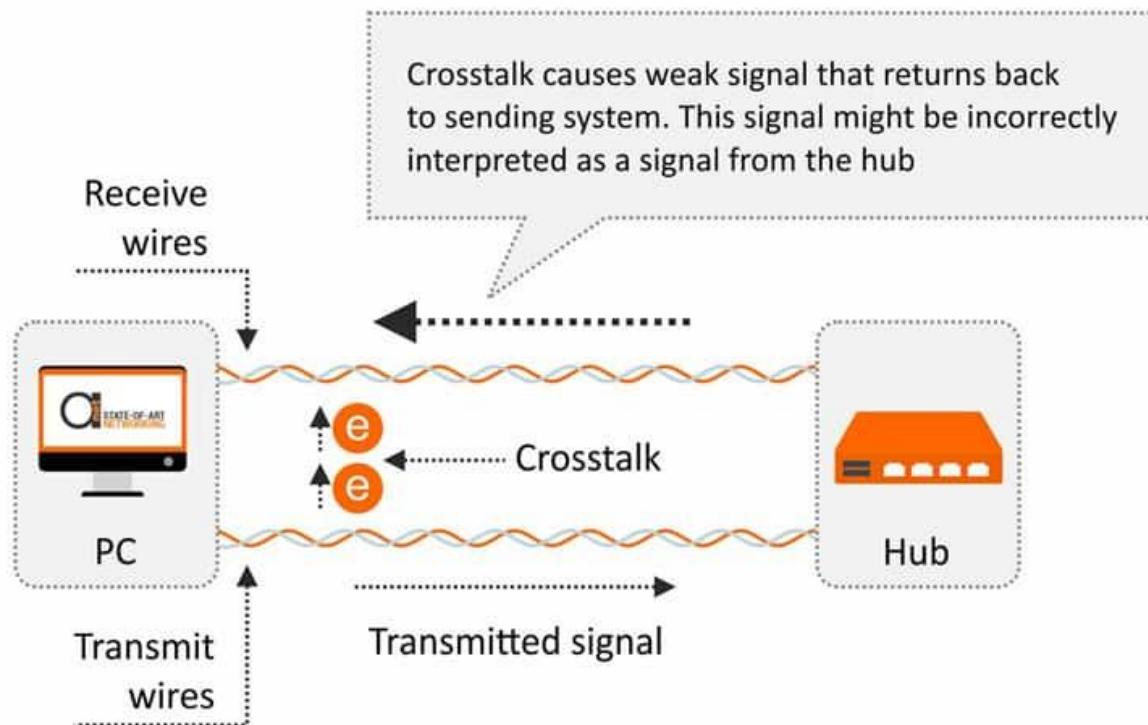
# Differential Signaling

- Differential analog signaling –reduce noise
- Two opposite signals to represent one bit



# Crosstalk caused by adjacent signal line

- Two parallel wires
- Signals couples from one wire to the other
- Generate incorrect signals



# Inter-Symbol Interference (ISI)

## Intersymbol Interference

- If the rectangular multilevel pulses are filtered improperly as they pass through a communications system, they will spread in time, and the pulse for each symbol may be smeared into adjacent time slots and cause **Intersymbol Interference**.

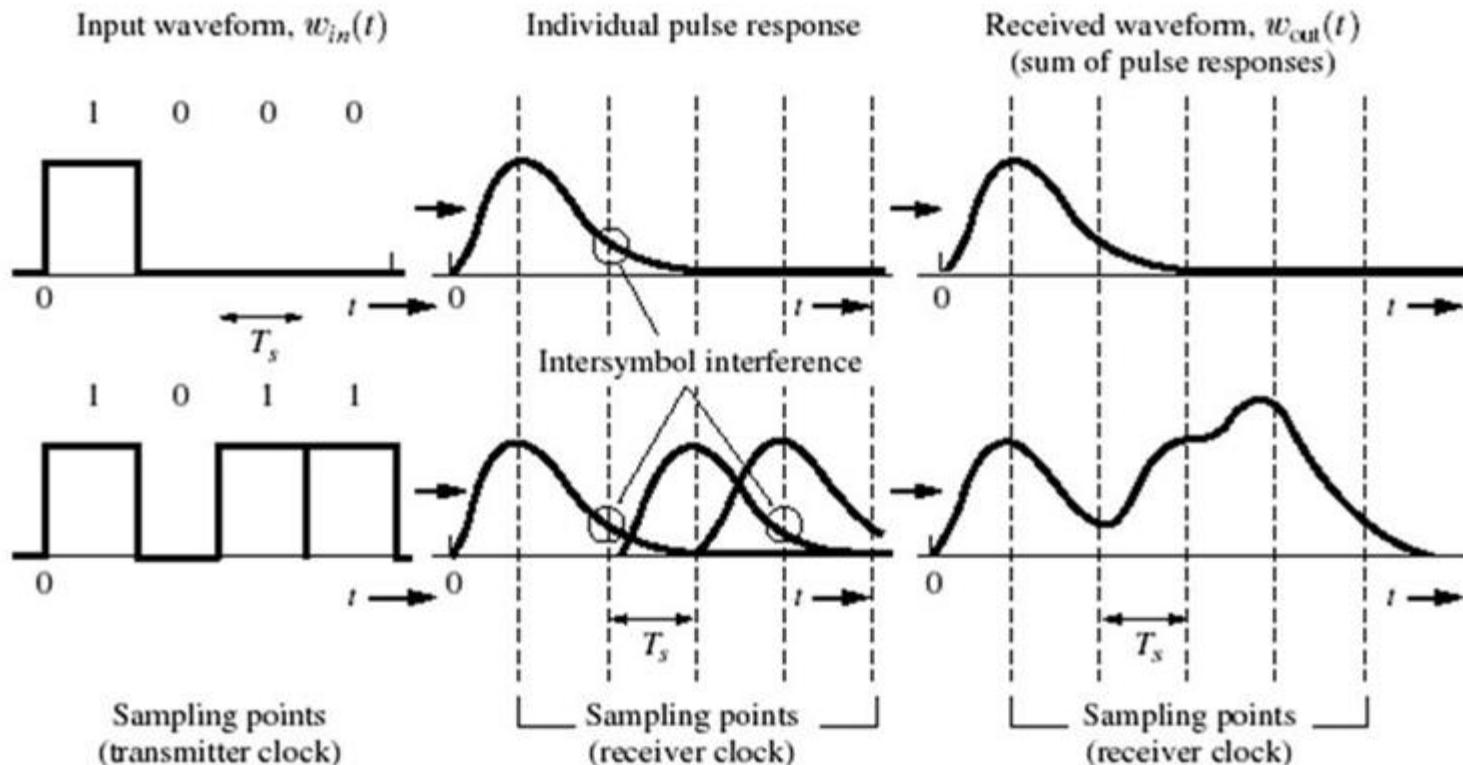
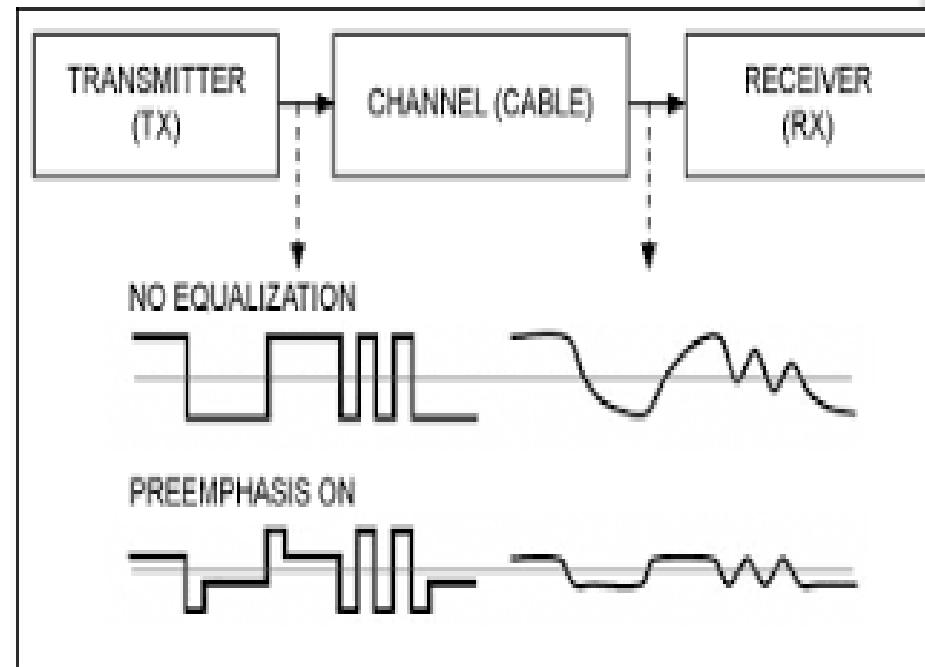
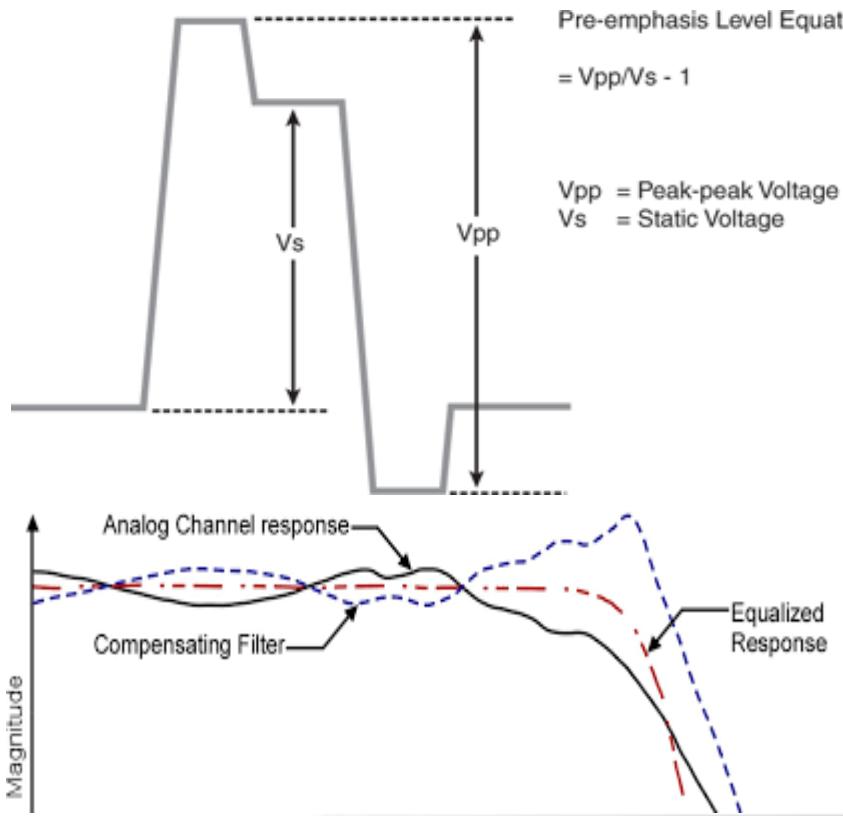


Figure 3–23 Examples of ISI on received pulses in a binary communication system.

# Pre-emphasis and Equalization

- Pre-emphasis is a way to boost only the signal's high-frequency components, while leaving the low-frequency components in their original state
- Equalization-Overcome the high-frequency signal losses of the transmission medium or inter-symbol interference



# Increases Data Rate-Challenges

- Loss

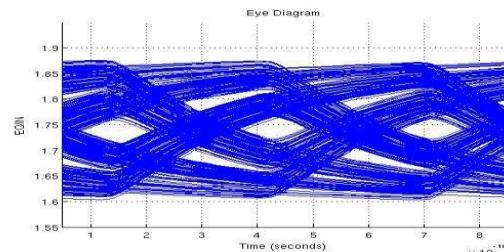
- Pre-emphasis and Equalization
- Equalization implemented by finite impulse filter (FIR)

- Jitter

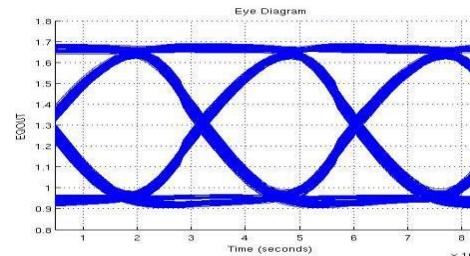
- Clock data recovery (CDR)

- Cross talk/Reflection

- Decision feedback equalizer



Before Equalization

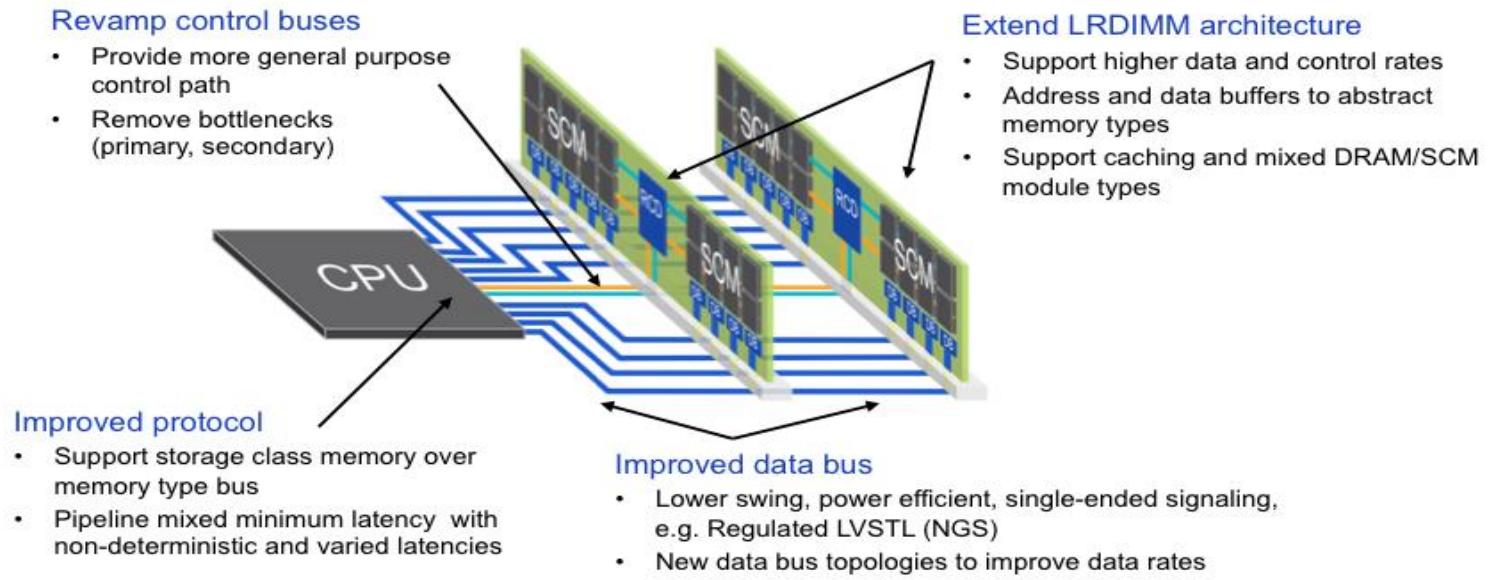


After Equalization

# DRAM to CPU Interconnect

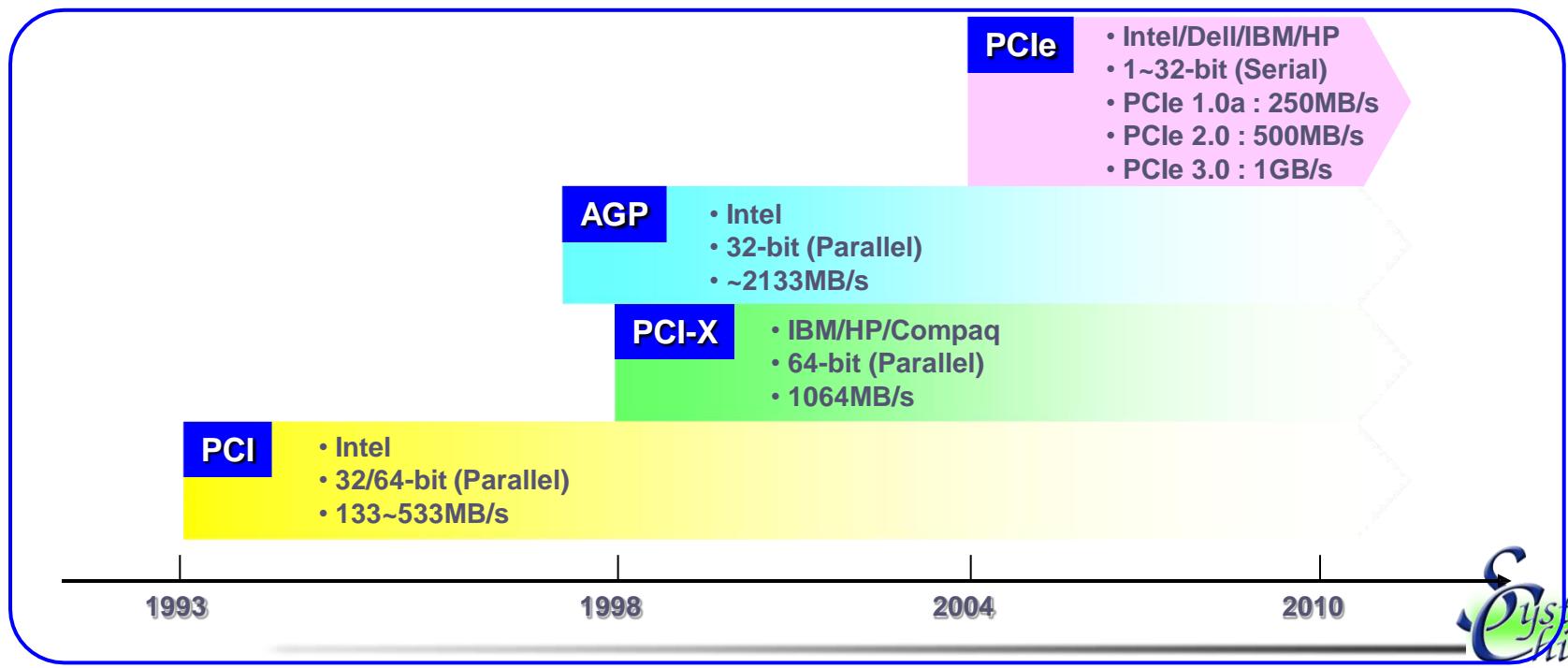
- Off Chip – parallel data bus/ control bus
  - LRDIMM (load reduce dual inline memory module)
  - SCM (storage class memory) : 3D Xpoint, ReRAM (resistive RAM)
- On Chip – HBM (high bandwidth memory)

## DDR5 Potential Directions



# PCI-E (Peripheral Component Interconnect Express )

- PCIe (Peripheral Component Interconnect Express),
  - high-speed serial computer expansion bus standard
    - common motherboard interface for personal computers' **graphics cards, hard drives, SSDs, Wi-Fi and Ethernet hardware connections**
    - computer expansion bus standard, designed to replace the older PCI, PCI-X and AGP (accelerated graphics port) bus standards



# PCIe SPEC Evolution

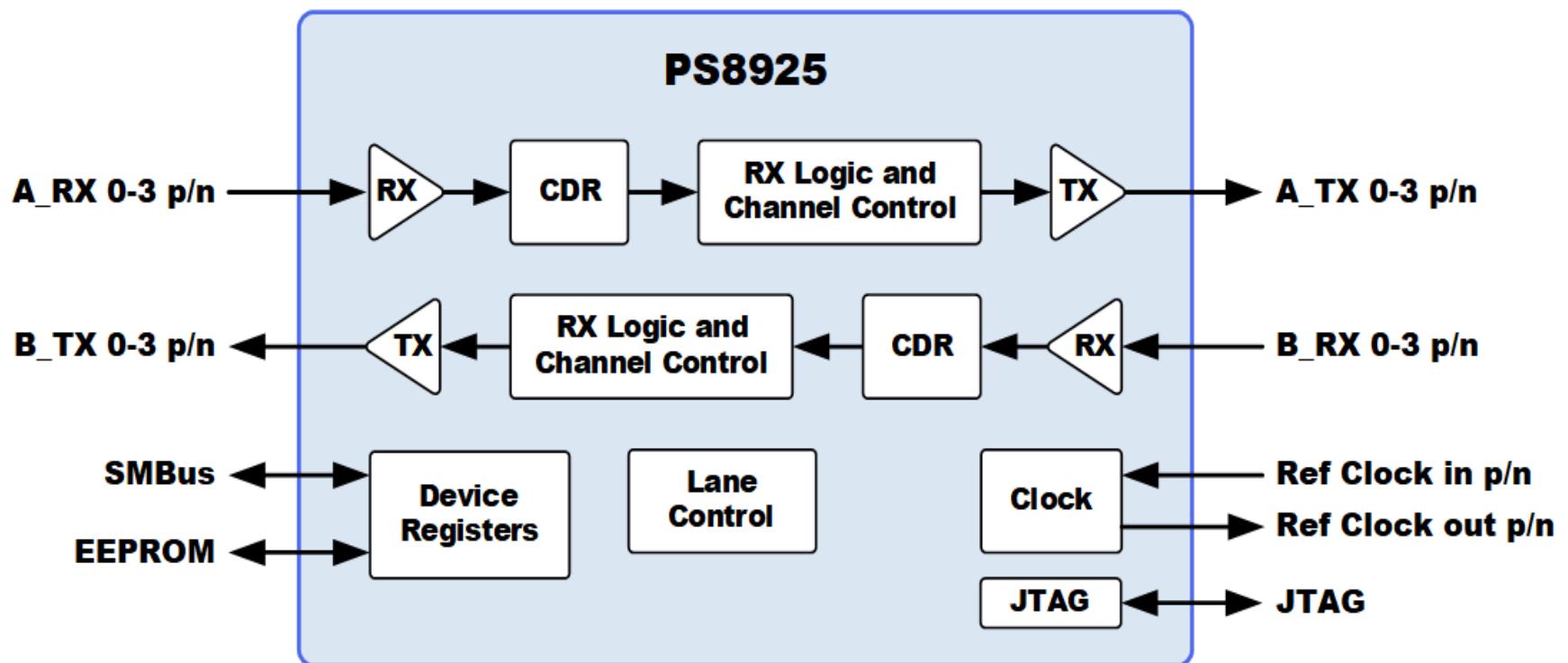
- higher maximum bandwidth, lower I/O pin count and better performance-scaling, more detailed error detection and reporting, and hot-plugging

	RAW BIT RATE	LINK BW	BW/ LANE/WAY	TOTAL BW X16	PCI Express Example Connectors
PCIe 1.x	2.5GT/s	2Gb/s	250MB/s	8GB/s	<b>x1</b> <b>BANDWIDTH</b> Single direction: 2.5 Gbps/200 MBps Dual Directions: 5 Gbps/400 MBps
PCIe 2.x	5.0GT/s	4Gb/s	500MB/s	16GB/s	<b>x4</b> <b>BANDWIDTH</b> Single direction: 10 Gbps/800 MBps Dual Directions: 20 Gbps/1.6 GBps
PCIe 3.x	8.0GT/s	8Gb/s	~1GB/s	~32GB/s	<b>x8</b> <b>BANDWIDTH</b> Single direction: 20 Gbps/1.6 GBps Dual Directions: 40 Gbps/3.2 GBps
PCIe 4.0	16GT/s	16Gb/s	~2GB/s	~64GB/s	<b>x16</b> <b>BANDWIDTH</b> Single direction: 40 Gbps/3.2 GBps Dual Directions: 80 Gbps/6.4 GBps
PCIe 5.0	32GT/s	32Gb/s	~4GB/s	~128GB/s	<small>Source: IBM</small> <small>©2005 HowStuffWorks</small>

$5\text{GT/s} \times 0.8 = 4\text{Gb/s} = 500\text{MByte/s}$  T:transfer

# PCIE Block Diagram

- Lane control
- Transmitter (TX)/ Receiver (RX)/ CDR/ RX logic/ Channel Control
- Clock

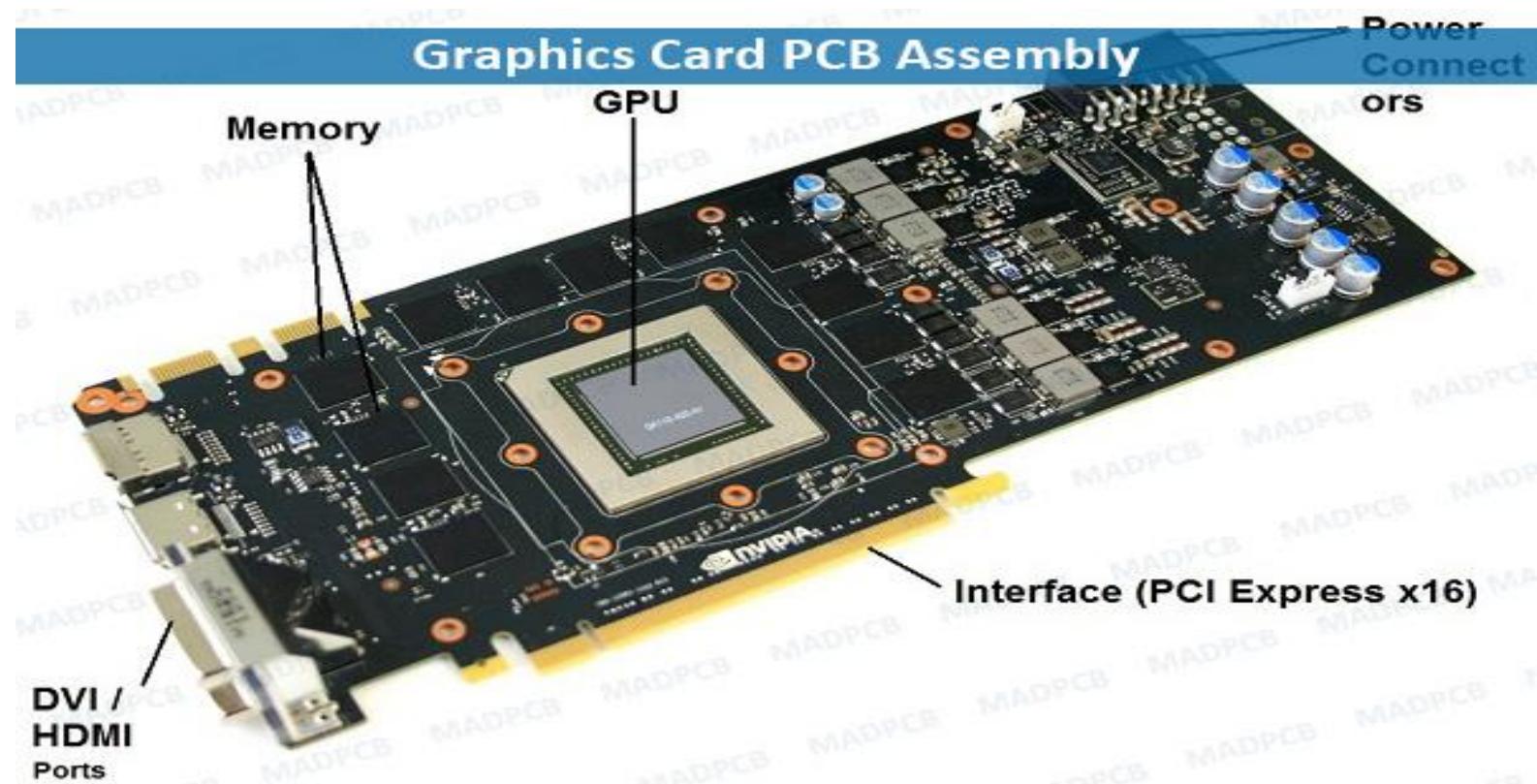


Parade :PS8925 – PCI Express® Gen 4 16Gbps 4-Lane Retime  
(<https://www.paradetech.com/zh-hant/%E7%94%A2%E5%93%81%E4%BB%8B%E7%B4%B9/ps8925/>)



# Video Card Interconnect

- PCI-E : GPU to CPU
- GDDR: GPU
- HDMI : memory to external monitor



# PCIe Applications

## ■ Graphics card



## ■ PCIE solid-state drive



# Memory Interface

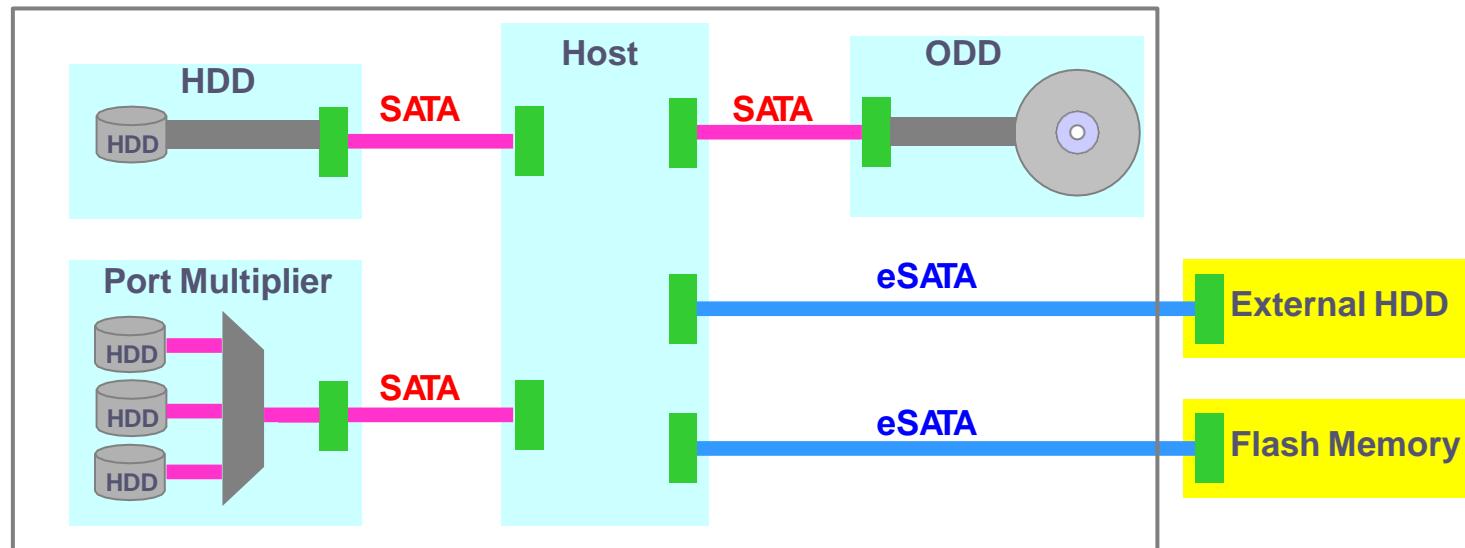
## SATA

(Serial Advanced Technology Attachment)



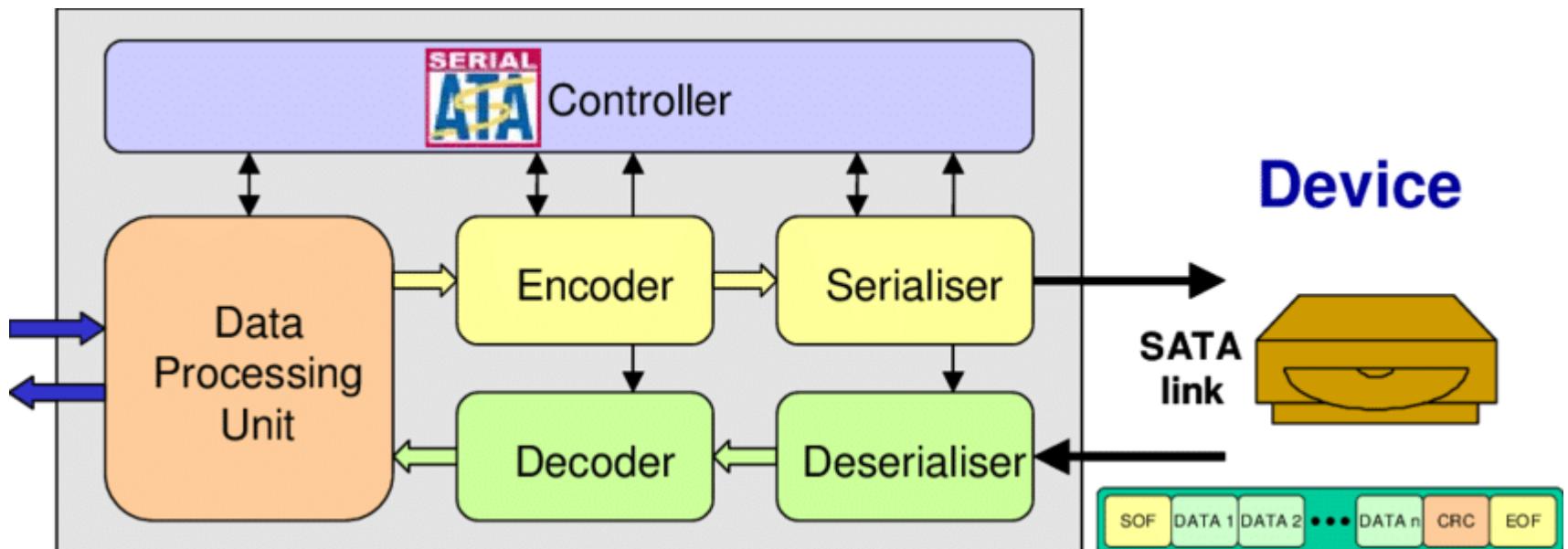
- Computer bus interface for connecting a host bus adapter to mass storage devices HDD, replacing PATA
- Host mode and Device mode supported (“Host Swapping”)

**Variants :** eSATA(External SATA), eSATAp (External SATA with Power), HDD (Hard Disk Drive), ODD (Optical Disk Drive)



# SATA Block Diagram

- Controller
- Data encoder/serializer
- Data decoder/deserializer



# USB (Universal Serial Bus) History

PHILIPS

- Industry standard and protocols for connection, communication and power supply between computers and peripherals

COMPAQ

intel

digital

Microsoft

IBM

NEC

hp

Alcatel-Lucent

NORTEL



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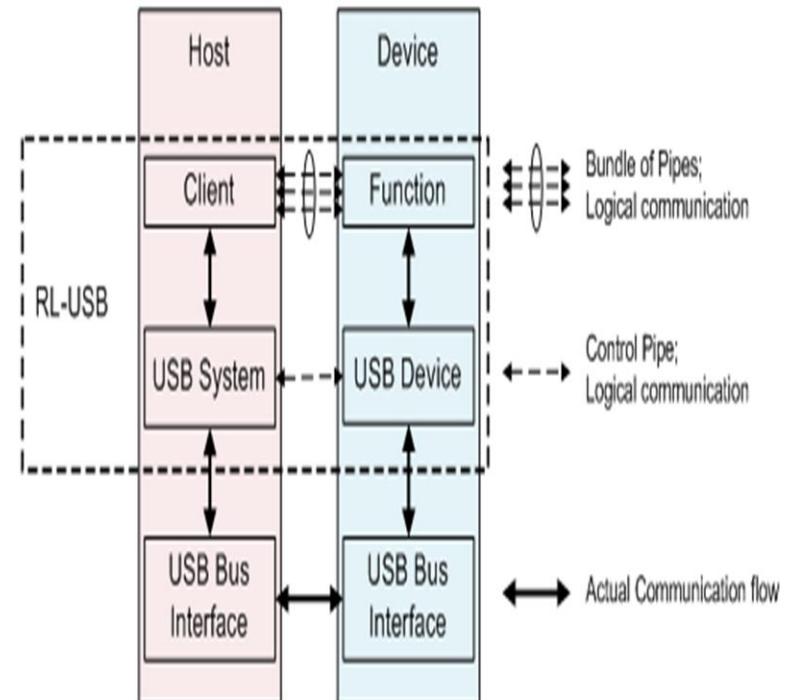
System  
chip on

- USB 1.0 (1996)
  - 1.5 Mbit/s (*Low Speed*)
- USB 1.1 (1998) USB-IF => 4 companies
  - 12 Mbit/s (*Full Speed*)
- USB 2.0 (2000) USB-IF => 7 companies
  - 480 Mbit/s (*High Speed*)
  - Mini-A, Mini-B (2000)
  - USB On-The-Go (2006)
  - Micro USB (2007)
- USB 3.0 (2008~2009)
  - 5 G bit/s (*Super Speed*)
- USB 3.1 (2013)
  - 10 G bit/s (*Super Speed+*)
- USB 3.2 (2017)
  - 20 G bit/s (*Super Speed+ USB dual lane*)
- USB 4 (2019)
  - 40 G bit/s (*2 lanes*)
- USB 4 2.0 (2022)
  - 120 G bit/s

# Architecture

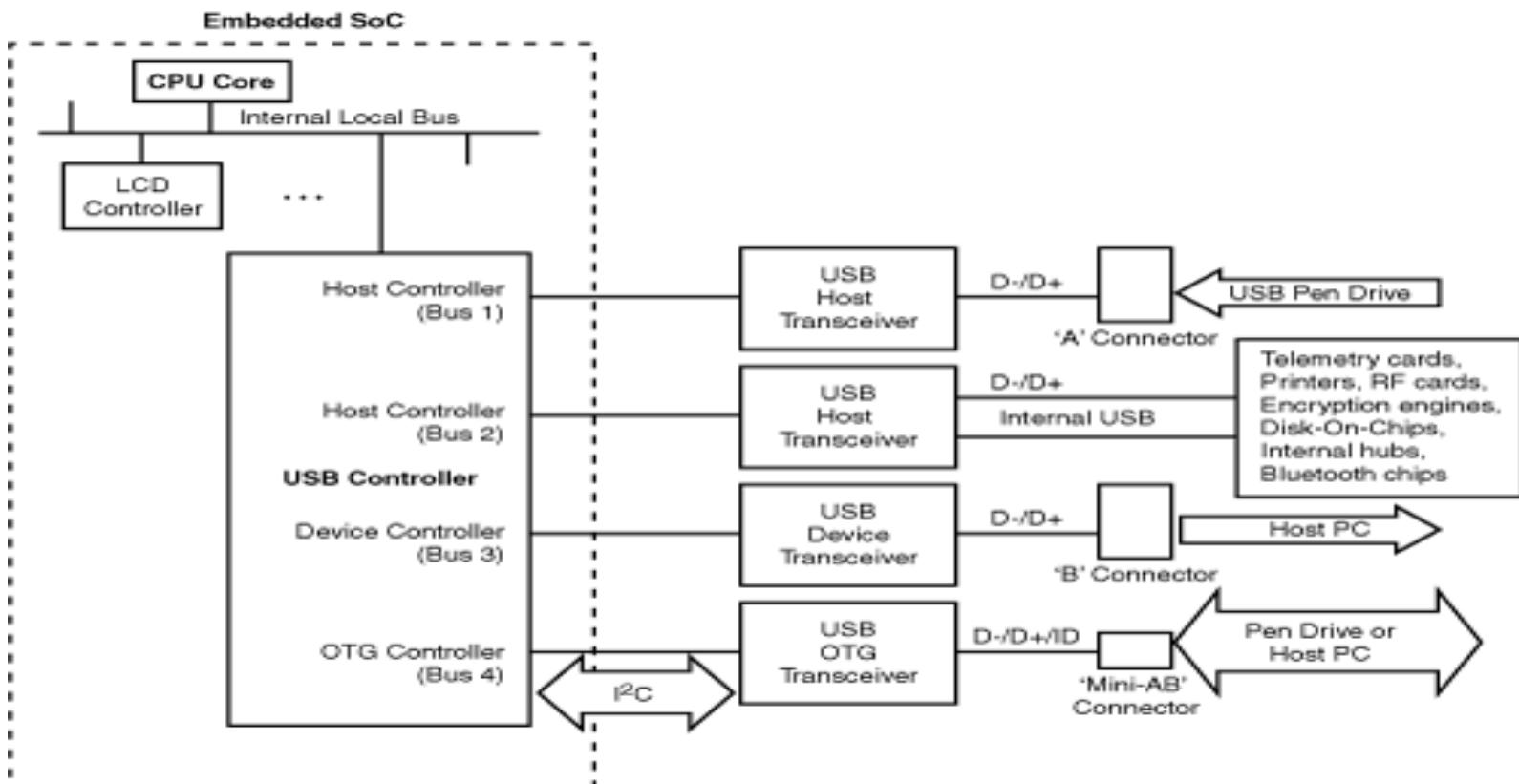
## USB Communication Model

- Polling
- Process
  - Client
  - USB Device
  - USB System
  - USB Bus Interface



# USB Block Diagram

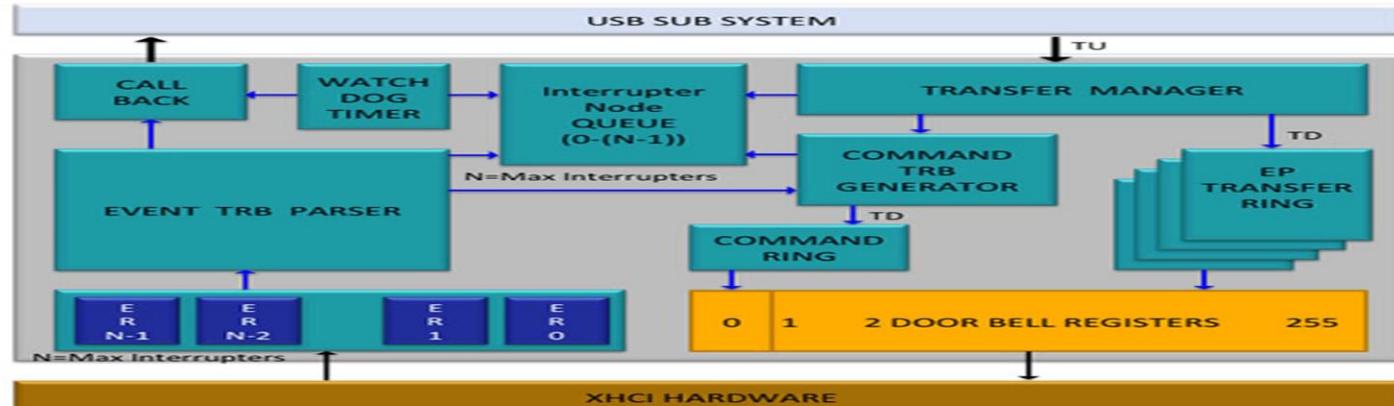
- USB Controller
- Host Transceiver (external/internal)
- Device Transceiver



# Architecture

## ■ USB 3.0

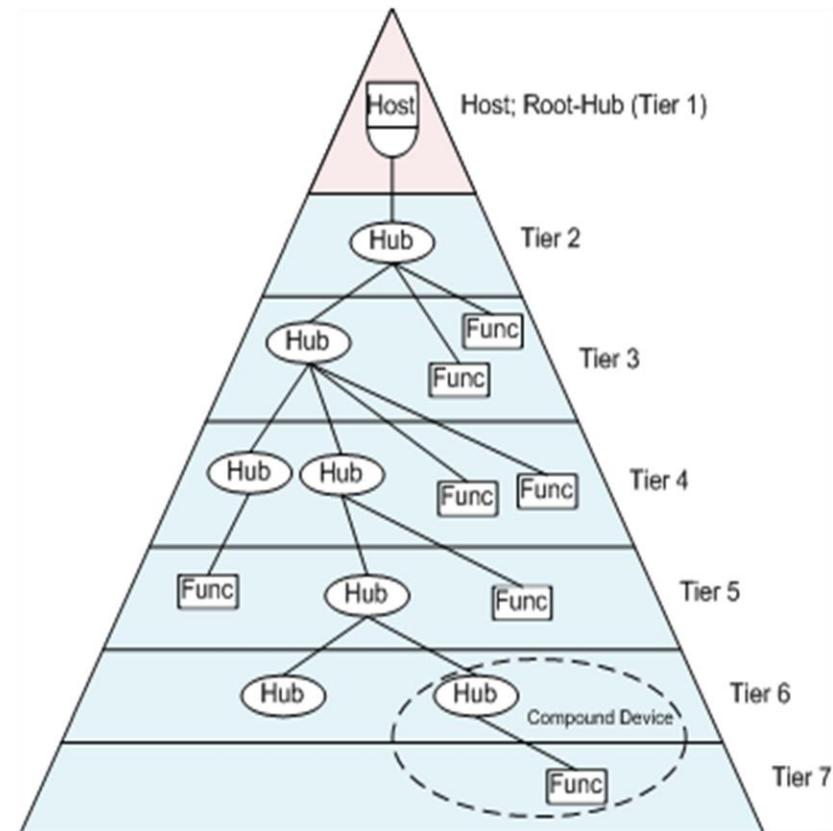
- xHCI (Extensible Host Controller Interface) - 擴展主控制器界面
  - Intel
  - xHCI 0.96 (general)
  - xHCI 1.0 (UASP)
- UASP (USB Attached SCSI Protocol)
  - No need for waiting for other data
  - Improve CPU utilization
  - Reduce data latency
  - Supported by Win8, Mac OS 8 & 9



# Star Network

## USB Serial Bus Architecture

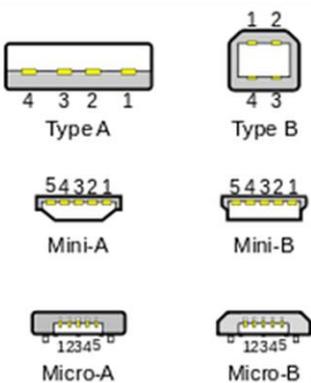
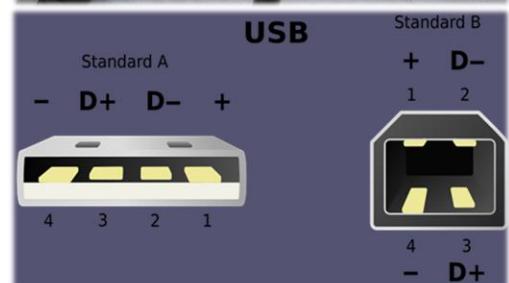
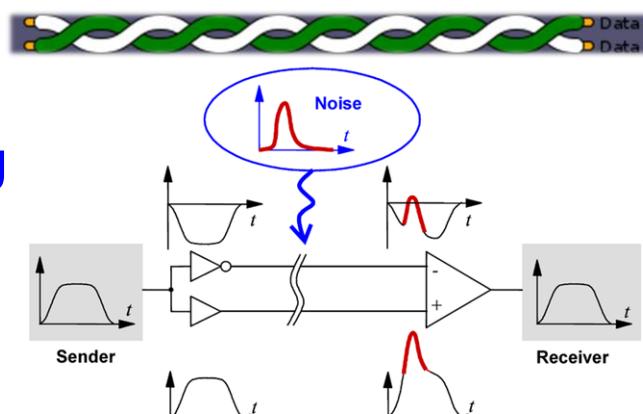
- Tiered Star Network
- 1 Master(Host)
- $\geq 1$  Slaves(Devices)
- Max 127 devices



# USB 2.0

## ■ USB 2.0

- Twisted Pair
- Differential signaling
- Half-duplex



USB 1.x/2.0 mini/micro pinout			
Pin	Name	Wire color	Description
1	V <sub>BUS</sub>	Red	+5 V
2	D-	White	Data-
3	D+	Green	Data+
4	ID	N/A	Permits detection of which end of a cable is plugged in: • "A" connector (host): connected to the signal ground • "B" connector (device): not connected
5	GND	Black	Signal ground

USB 1.x/2.0 standard pinout			
Pin	Name	Cable color	Description
1	V <sub>BUS</sub>	Red (or Orange)	+5 V
2	D-	White (or Gold)	Data -
3	D+	Green	Data +
4	GND	Black (or Blue)	Ground

# USB 3.0

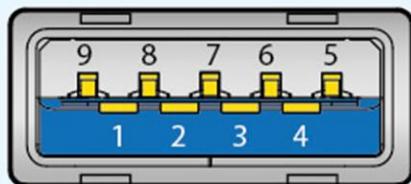
## USB 3.0

### ■ Full-duplex

#### USB 3.0 type A pinout, cable Assembly

Pin	Signal Name	Description
1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
5	StdA_SSRX-	Blue
6	StdA_SSRX+	Yellow
7	GND_DRAIN	GROUND
8	StdA_SSTX-	Purple
9	StdA_SSTX+	Orange
Shell	Shield	Connector Shell

source: www.reviewharddrive.c

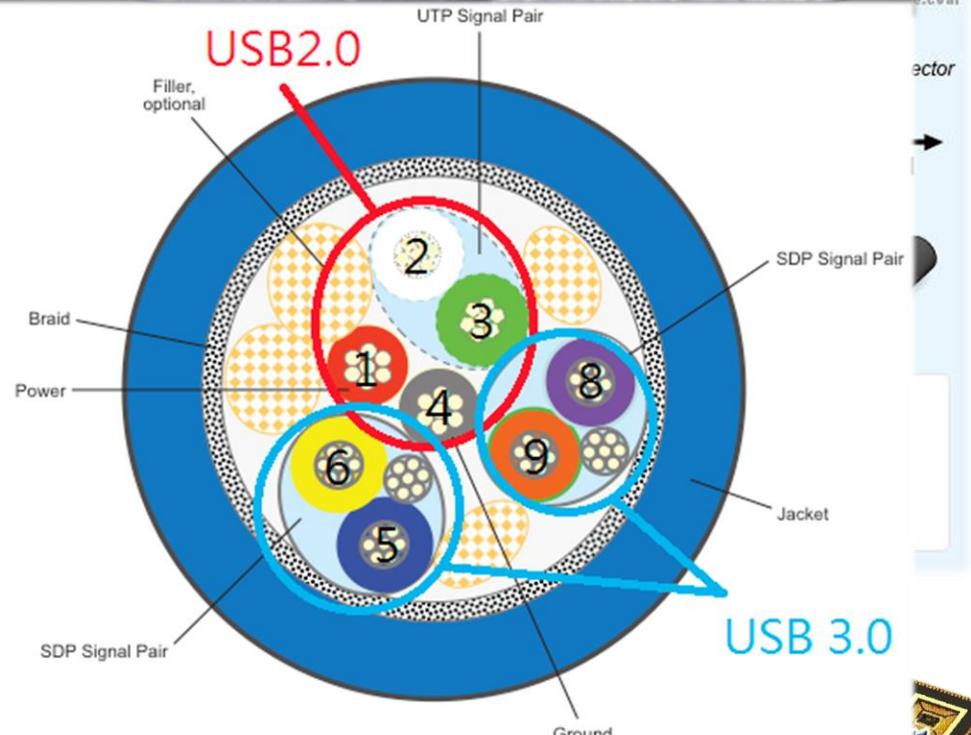
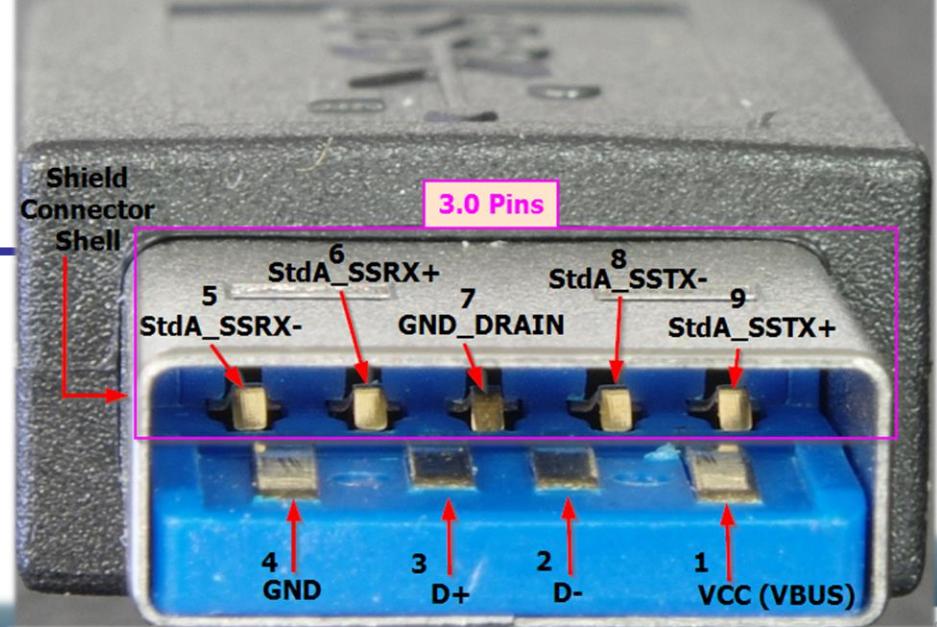


USB 3.0 type A Connector



#### USB 3.0 transfer capability

The high USB 3.0 speed becomes possible due to its full duplex transfer capability in which two lanes are fully reserved for sending the data and the rest of the two lanes are reserved for receiving it.



USB 3.0

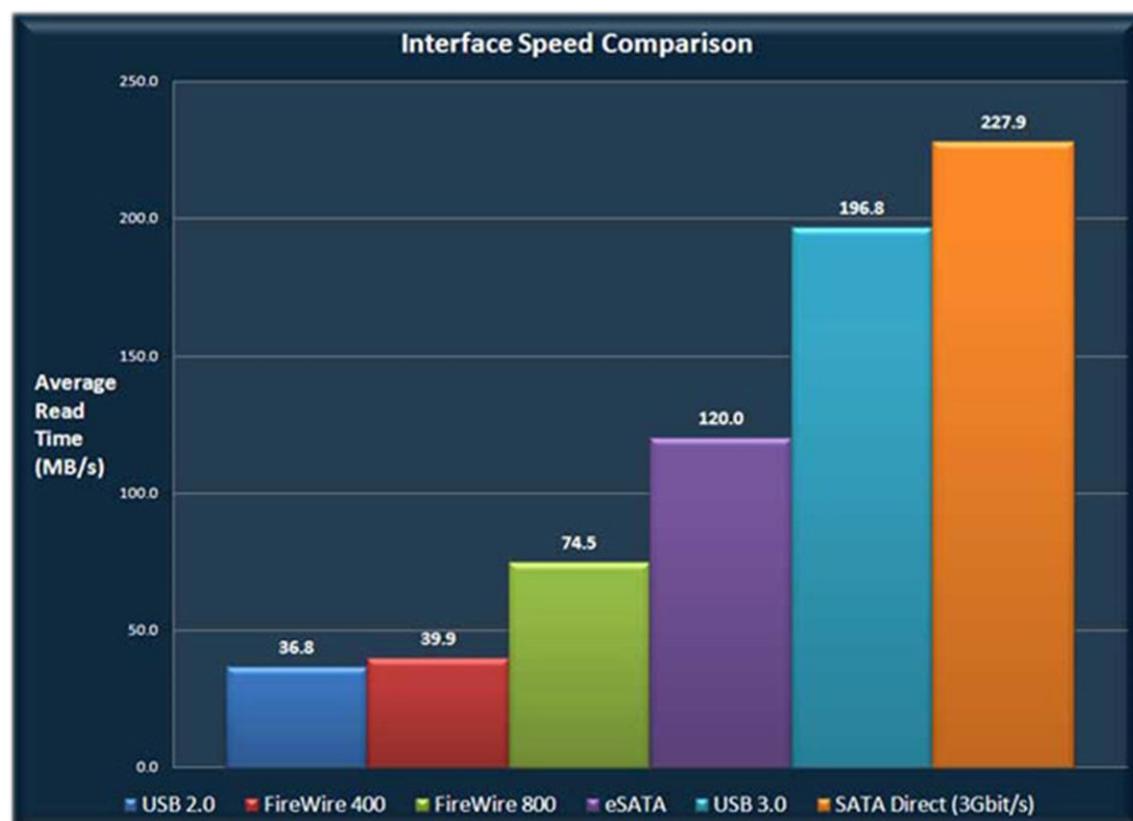
# USB 3.0 Features

## ■ USB

- Generalization
- Plug-and-Play
- Hot Attach & Detach

## ■ USB 3.0

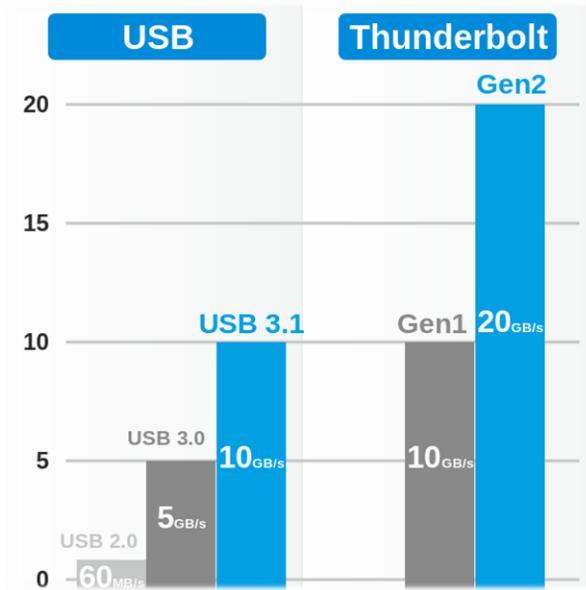
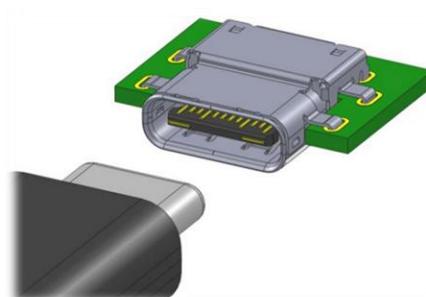
- Power Supply
  - Standby
    - 100mA => 150mA
  - Running
    - 500mA => 900mA
- 4.5~5V
- 4.5W
- Power Management
- Compatibility
- Speed Up



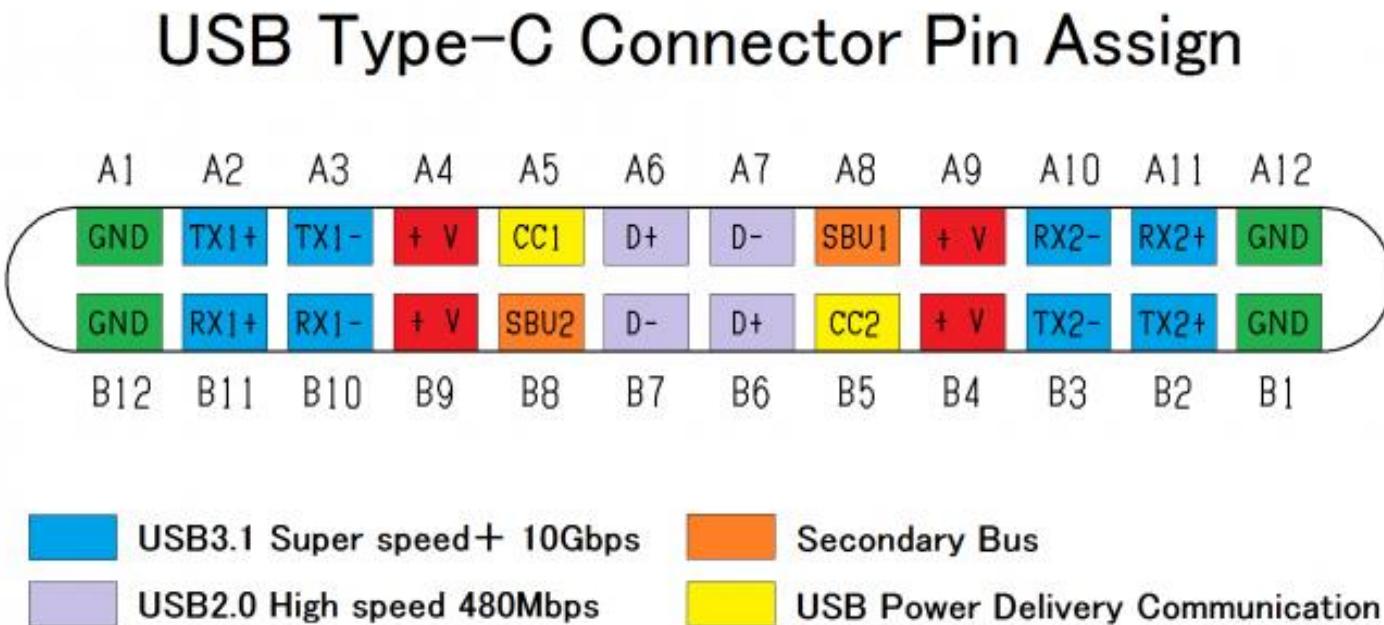
# USB 3.1

## USB 3.1

- 8.3mm x 2.5mm
- Never “Plug” wrongly
- Speed Up (10Gbit/s)
- Support DisplayPort 1.2a
- 5V / 12V / 20V => Max 100W
- Apple use it !!!



# USB 3.1 and Type C Pin assignment



# USB Evolution

USB4 data transfer modes

Marketing name	Logo	Specifications	Old specifications	Dual-lane	Encoding	Nominal speed	
						Gbit/s	GB/s
SuperSpeed USB 5Gbps		USB 3.2 Gen 1x1	USB 3.0, USB 3.1 Gen 1	No	8b/10b	5	0.5
SuperSpeed USB 10Gbps		USB 3.2 Gen 2x1	USB 3.1 Gen 2	No	128b/132b	10	1.2
N/A		USB 3.2 Gen 1x2		Yes	8b/10b	10	1.0
SuperSpeed USB 20Gbps		USB 3.2 Gen 2x2		Yes	128b/132b	20	2.4
N/A		USB4 Gen 2x1		No	64b/66b <sup>[a]</sup>	10	1.2
N/A		USB4 Gen 3x1		No	128b/132b <sup>[a]</sup>	20	2.4
USB4 20Gbps		USB4 Gen 2x2		Yes	64b/66b <sup>[a]</sup>	20	2.4
USB4 40Gbps		USB4 Gen 3x2		Yes	128b/132b <sup>[a]</sup>	40	4.8

# Industry Chain

主端控制晶片 (Host Controller Chip) >>> 主機板、磁碟陣列卡、擴充卡

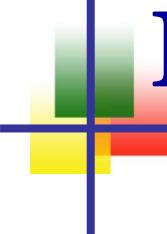
- 睿思(Fresco)、祥碩(ASMedia)、威鋒(Via Labs)、瑞薩電子(Renesas)、  
德州儀器(Ti)

SATA 橋接控制晶片 (SATA Bridge Controller Chip) >>> 外接硬碟盒

- 祥碩(ASMedia)、晶量(Initio)

集線器控制晶片 (Hub Controller Chip) >>> 集線器、硬碟外接座、平板電腦底座、智慧型電視

- 祥碩(ASMedia)、瑞昱(Realtek)、威鋒(Via Labs)
- 創惟(Genesis Logic)、德州儀器(Ti)、瑞薩電子(Renesas)



# Industry Chain

## 轉接驅動晶片 (Re-Driver Chip)

- 祥碩(ASMedia)、德州儀器(Ti)、恩智浦(NXP)、百力達(Pericom)



## 隨身碟控制晶片 (USB Flash Drive Controller Chip) >>> 隨身碟

- 銀燦(Innostor)、群聯(Phison)、慧榮(Silicon Motion)

- 鈺創(Etron)、創惟(Genesis Logic)、擎泰(Skymedi)



## CPU同樣提供USB主控端晶片 功能(Host Controller Chip provided by CPU)



- 英特爾(Intel)、邁爾(Marvell)、德州儀器(Ti)



- 輝達(Nvidia)、高通(Qualcomm)、三星(Samsung)



# Memory Interface Comparison

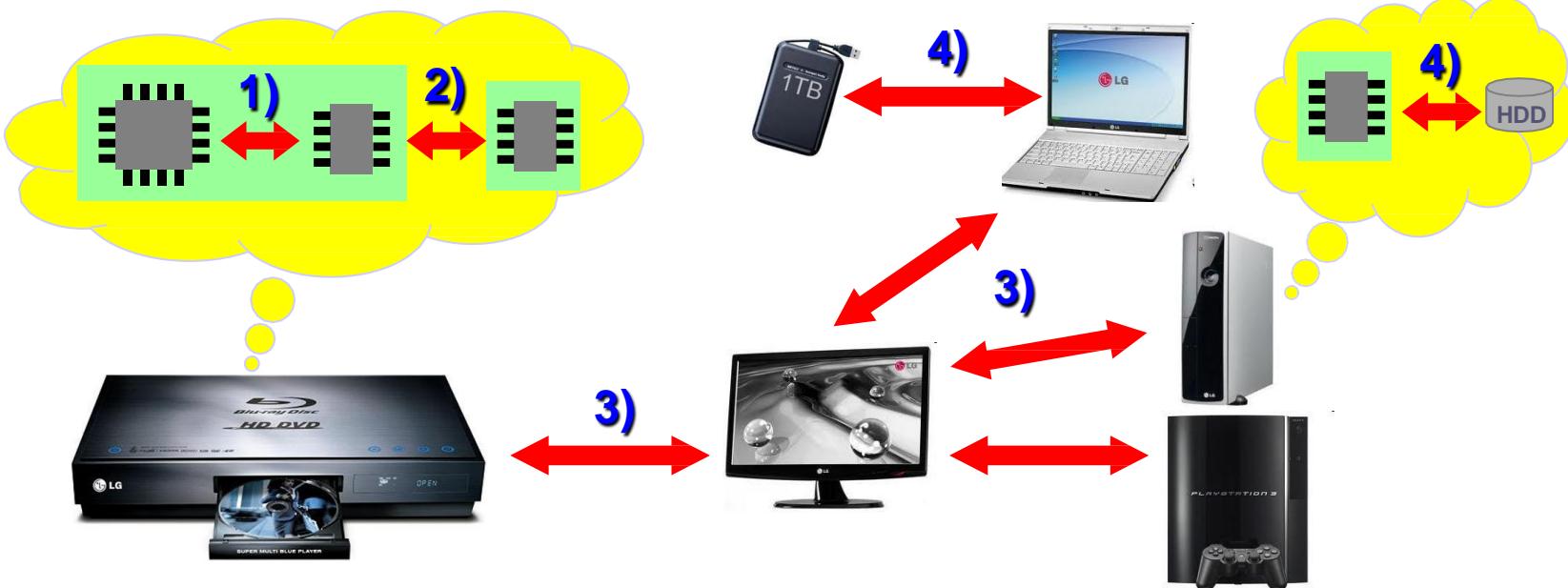
## SATA-IO (SATA International Organization)

	DDR	USB	PCIe	SATA
First version	DDR1	USB1.0	PCIe Gen1	SATA1.0
version	DDR4	USB3.1	PCIe Gen3	SATA3.0
Controlling Authority	JEDEC	USB organization	-	SATA-IO
Bit rate / pair	2133MT(transfer)/s	10Gbps @ super speed	8.0Gbps @ Gen3	6.0Gbps @ Rev3
No. of clock ch.	1pair/8data	No	No	No
No. of data ch.	16, 32	2 pairs	4 pairs (TX) 4 pairs (RX)	1 pair (TX) 1 pair (RX)
Channel coding	No	8b/10b	128b/130b	8b/10b
Major Application	DRAM Interface	Universal	Graphic card interface @ PC	Hard Disk, SSD interface

# High Speed Interface types

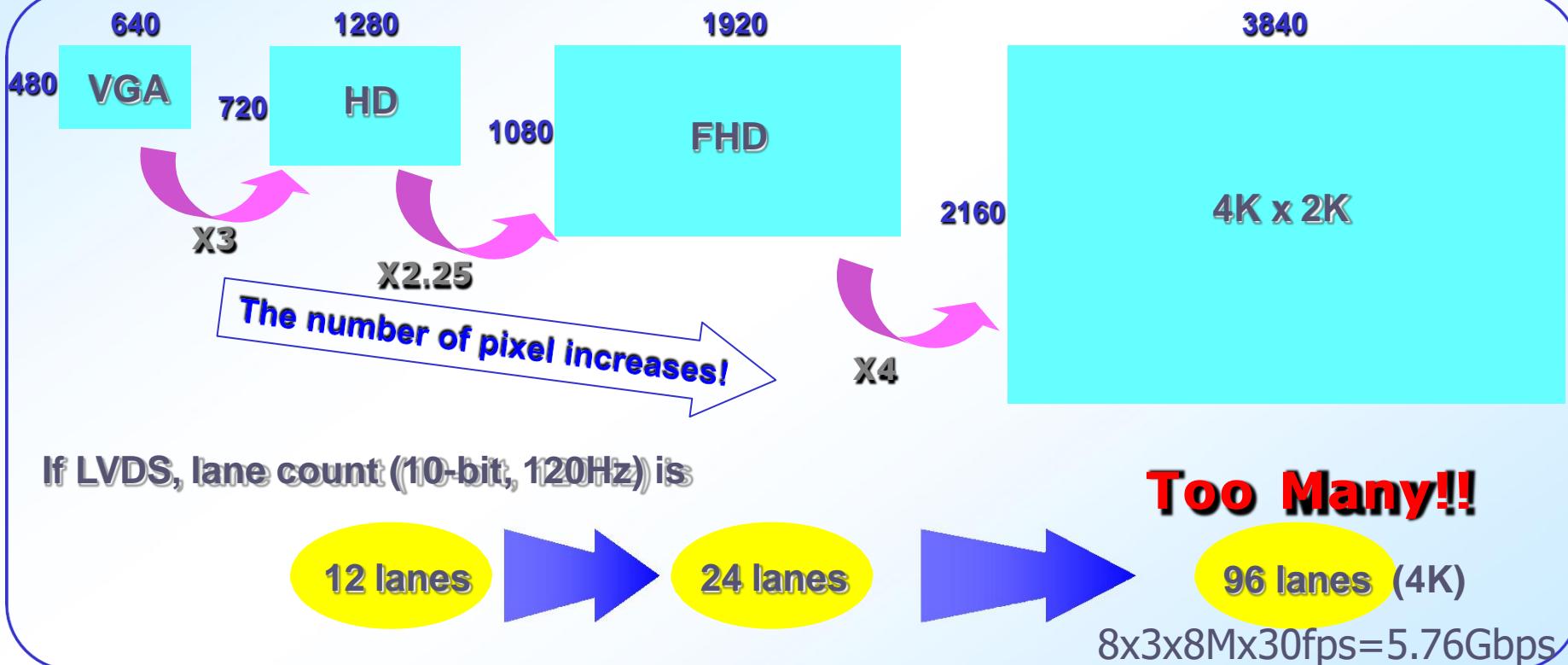
- Current system performance is hampered by Inter-Component Interface rather than Intra-Chip Technology.
  - Chip-to-Chip Interface
  - Board-to-Board Interface
  - Box-to-Box Interface
  - Memory Interface

1) Chip-to-Chip Interface 2) Board-to-Board Interface 3) Box-to-Box Interface 4) MemoryInterface



# Why High Speed Interface-1

- Bigger display and higher resolution drastically increase the pixel data to be transmitted over cables.



If LVDS (Low voltage Differential Signaling) 24bit /20MHz,  
 $5.76\text{Gbps}/24/20\text{M}=12$  pixel/transfer,  $12 \times 24 \times 2 = 576$  pins

1 lane = 2 lines

# Why High Speed Interface-2

## 8K Display Resolution



4K:  $8 \times 3 \times 8 \text{M} \times 30 \text{fps} = 5.76 \text{Gbps}$

8K:  $4 \times 5.76 = 30.04 \text{Gbps}$  (30fps)

8K:  $4 \times 5.76 = 60.08 \text{Gbps}$  (60fps)

# Box-to-Box Interface : HDMI



- • Initial release in 2002; Currently HDMI 2.1 released in 2017
- • Industry de facto standard for Consumer Electronics
- • Networking feature added (LiquidHD)
- • Companion Interface Standard introduced (MHL, SPMT)
- • Needs royalty / licensing fee



HDMI (High-Definition Multimedia Interface), MHL (Mobile High-definition Link),  
SPMT (Serial Port Memory Technology)



# HDMI(High Definition Multimedia Interface)

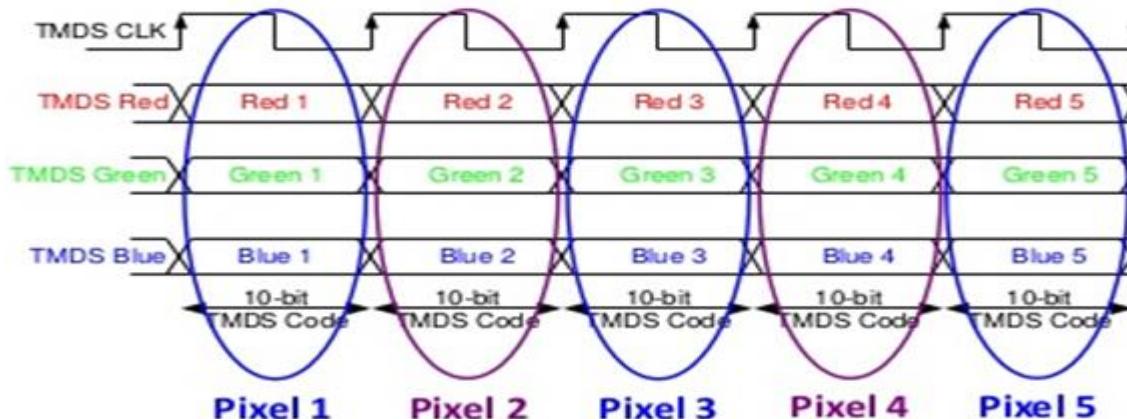
- Proprietary audio/video interface
- Source: Display controller
  - transmitting uncompressed video data and compressed or uncompressed digital audio data
- Destination
  - computer monitor, video projector, digital television, or digital audio device
- Communication channels
  - Transition-minimized differential signaling (TMDS)
    - Transmit video and audio signals
  - Display Data Channel (DDC)
    - I2C bus to learn the video/audio format
  - Consumer Electronics Control (CEC)
    - allow the user to command and control up to 15 CEC-enabled devices

# HDMI-TMDS(Transition-minimized differential signaling (TMDS))

- Interleaves video, audio and auxiliary data

- Three data types

- The video data period
  - the pixels of an active video line are transmitted
- The data island period
  - audio and auxiliary data are transmitted within a series of packets
  - which occurs during the horizontal and vertical blanking intervals)
- The control period
  - between video and data island periods
- TMDS runs at 1/10 of the serial data rate
- 1 TMDS clock is one pixel



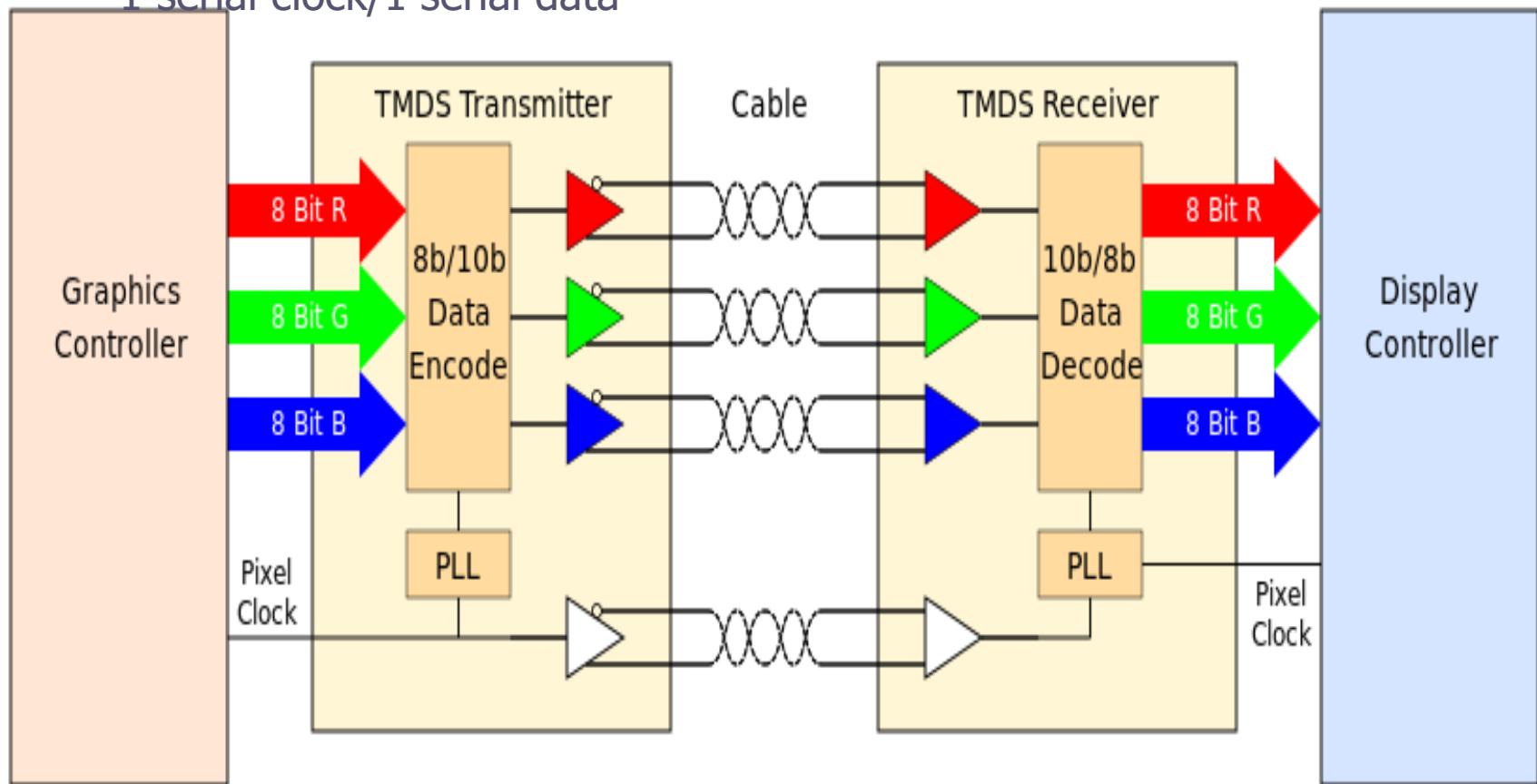
# HDMI-TMDS(Transition-minimized differential signaling (TMDS))

19 pins

3 pair video Lanes for R/G/B

1 pair TMDS clock

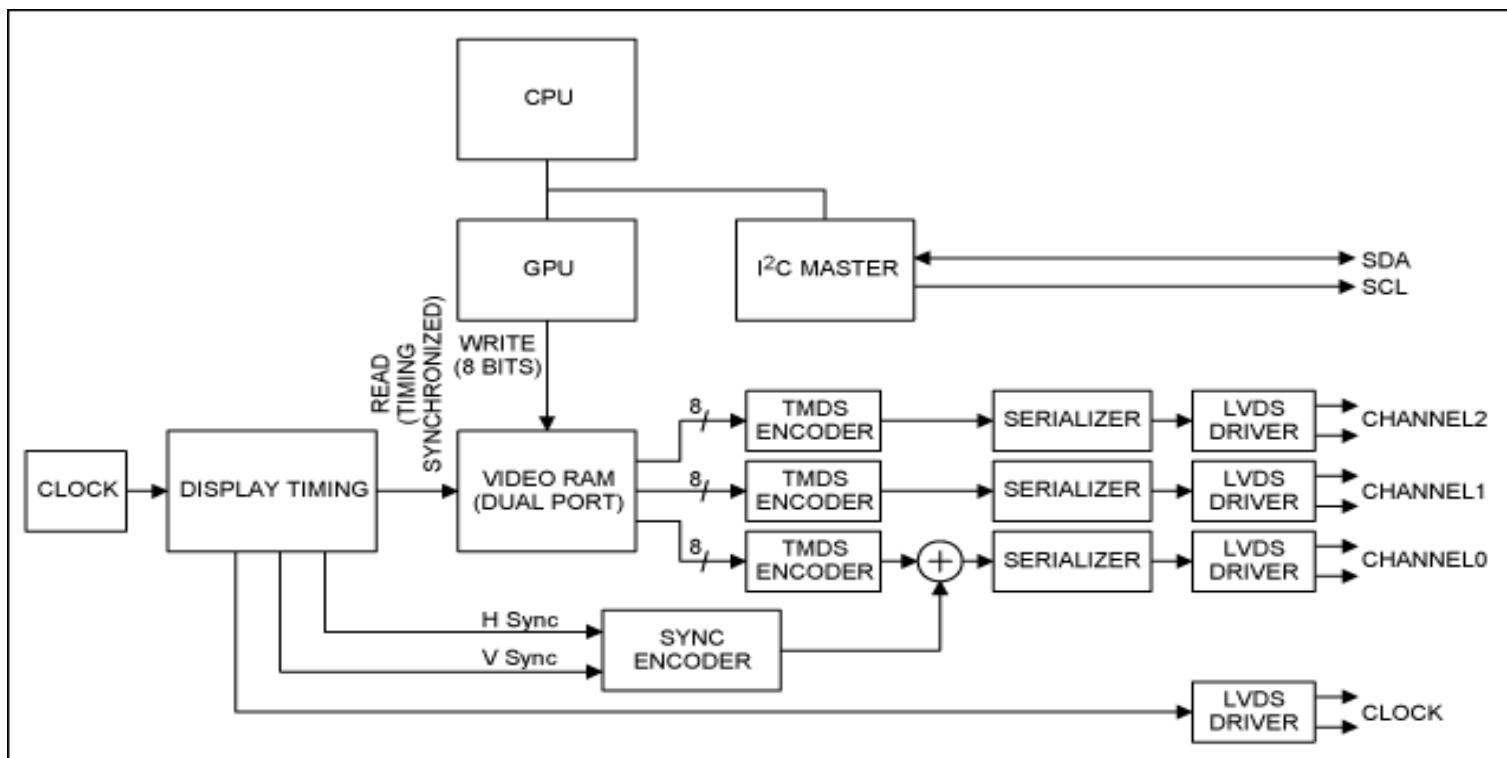
1 serial clock/1 serial data



TMDS傳輸示意圖(以HDMI 1.3為例)

# Video Display Signal and HDMI

CPU send control to GPU  
GPU processing the video display signal;  
Video RAM  
HDMI transmitter



VIDEO DISPLAY SIGNALS AND THE MAX9406 DP-HDMI/DVI LEVEL SHIFTER  
([HTTPS://WWW.MAXIMINTEGRATED.COM/EN/DESIGN/TECHNICAL-DOCUMENTS/APP-NOTES/4/4313.HTML](https://www.maximintegrated.com/en/design/technical-documents/app-notes/4/4313.html))

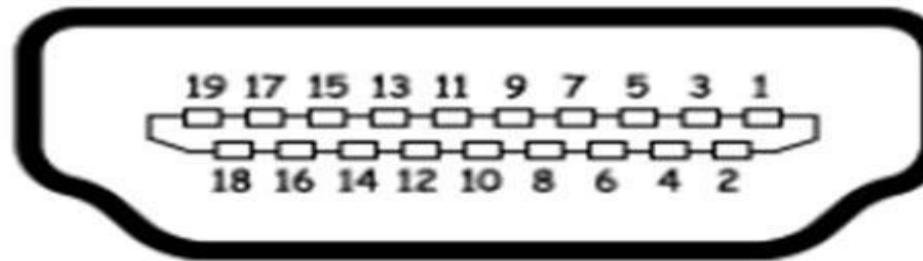
# HDMI-TMDS(Transition-minimized differential signaling (TMDS))

19 pins

3 pair video Lanes for R/G/B

1 pair TMDS clock

1 serial clock/1 serial data



Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		



# HDMI Evolution

HDMI version	1.4	2.0	2.1
Maximum pixel clock rate (MHz)	340	600	5940
Encoding type	8b/10b	8b/10b	16b/18b
Scrambling Present	No	Yes	Yes
Transmission frequency (Variable/Fixed)	Variable	Variable	Fixed
Deep color mode	Yes	Yes	Yes
YCbCr4:2:0-pixel encoding	No	Yes	Yes
Multi-stream audio	No	Yes	Yes
Maximum audio channel	8	32	32
VIC	1-64	65-107	108-219
HDR	No	Static	Dynamic

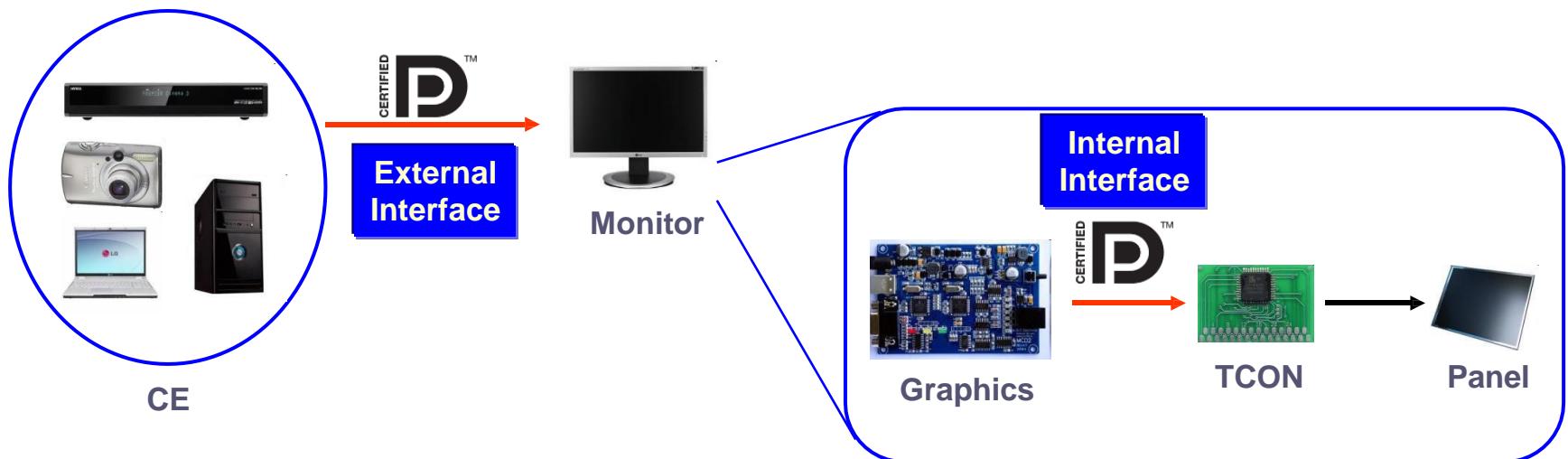
VIC: Video Identification Code (for different resolution,  
i.e. VIC=31 -> 1920x1080p)

# Box-to-Box Interface : DP

## DisplayPort (DP)



- Initial released by VESA in 2006; currently DP 1.2 in 2010
- Intended for both External and Internal interfaces
- Open standard; royalty-free
- Several Derivatives : eDP, iDP, tDP
- PC & Monitor application



VESA (Video Electronics Standards Association),  
eDP (Embedded DP), iDP (Internal DP), tDP (TCON DP)

# DisplayPort

## Function

- connect a video source to a display device such as a computer monitor
- Also carry audio, USB, and other forms of data

## Developed

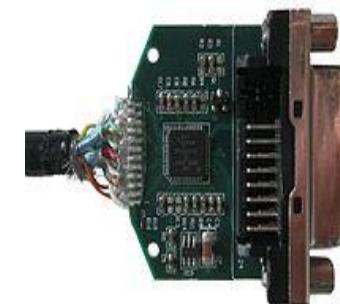
- consortium of PC and chip manufacturers

## Spec

- 20 pins
  - 4 Differential Signal Lanes
  - 1 aux channel lane

## Data Rate

- 1.62, 2.7, 5.4, or 8.1 Gbit/s data rate per lane;
- 1, 2, or 4 lanes; (effective total 5.184, 8.64, 17.28, or 25.92 Gbit/s for 4-lane link);
- 1 Mbit/s or 720 Mbit/s for the auxiliary channel

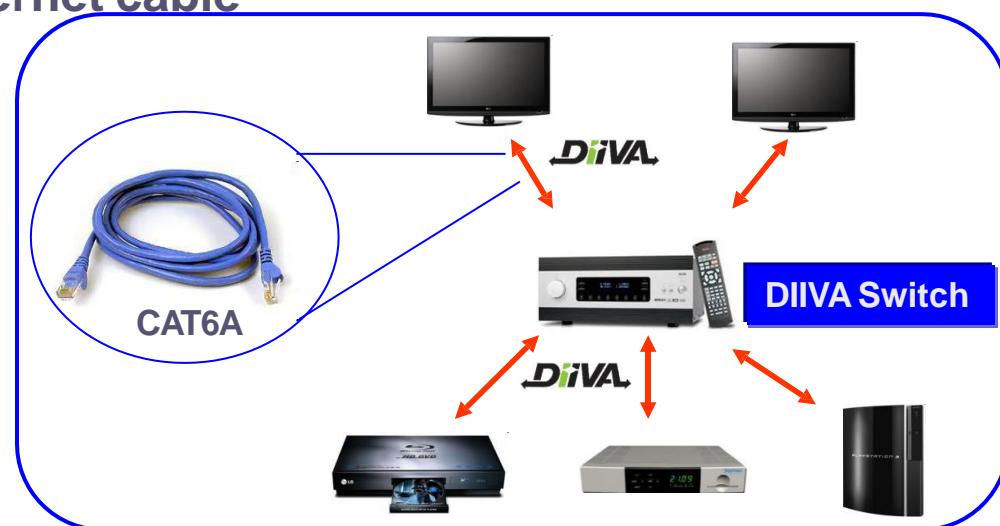
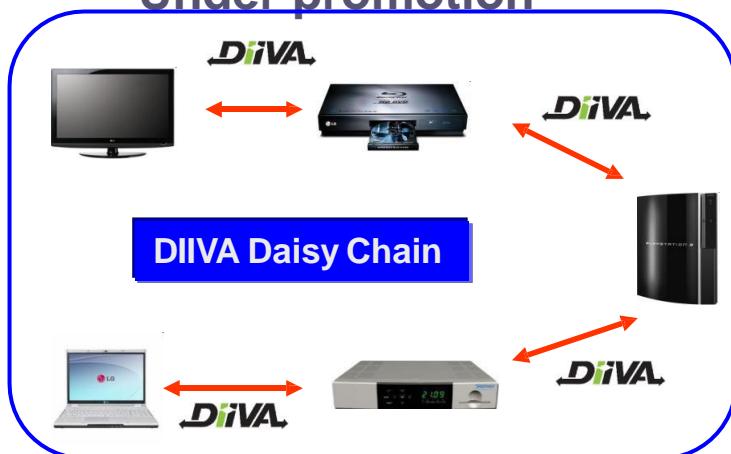


# Box-to-Box Interface : DIIVA

DIIVA (Digital Interactive Interface for Video and Audio),  
DIVA (Digital Interface for Video and Audio)



- Initial released by DIIVA Consortium in 2009
- Originally designed for Home Entertainment Networking
  - : Unification of 3 packet types (Video, Data, Power Control)
- Flexible connection (Daisy Chain or Switch configuration)
- Operating over standard Ethernet cable
- Under promotion



# Box-to-Box Interface Comparison

	HDMI	DisplayPort	DIIVA
First Release	2002/2017	2006	2009
Current version	HDMI 1.4/2.1	DP 1.2	DIIVA 1.0a
Controlling Authority	HDMI LLC	VESA	DIIVA Promoter
Content Protection	HDCP	DPCP / HDCP	HDCP / DTCP-IP
Bit rate / pair	Up to 3.4Gbps/48Gbps	1.62/2.7/5.4Gbps	4.5Gbps
Max. total capacity	10.2Gbps	21.6Gbps	13.5Gbps
No. of clock ch.	1	0	0
No. of video ch.	3	1/2/4	3
AUX channel	DDC	AUX	Hybrid Link
Channel coding	TMDS	8b/10b	8b/10b
Major Application	TV	Monitor	Home Networking
Ethernet	100Mbps	720Mbps	Gigabit
USB	No	Yes	Yes
Remarks			Bidirectional Power Over DIIVA

HDCP , High-Bandwidth Digital Content Protection

DPCP- DisplayPort Content Protection , DDC:direct data channel

Transition Minimized Differential Signaling(TMDS)





# Conclusion

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- As Digital TV becomes the Home Entertainment (HE) Network Hub to interconnect and control the CE equipments, External CE Interface should build and manage the **HE Network**.
- PC interface **keep adopting** clock-embedded serial interface technology, realizing high speed transfer rate and compact design.
- The latest High Speed I/F standards create **new market demand** in the area of Home Entertainment, Display device manufacturing, Mobile device industry, and PC industry.



in the

- LG high speed interface for various applications

<https://www.scribd.com/document/455722908/05-High-Speed-Interface-Various-Applications-LG%EC%A0%84%EC%9E%90-%ED%99%8D%EA%B5%AD%ED%83%9C-%EB%B0%9C%ED%91%9C%EC%9E%90%EB%A3%8C-HS-Interface-V10>