

# Optical interface

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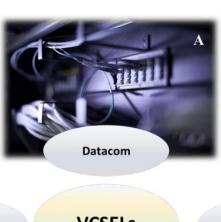


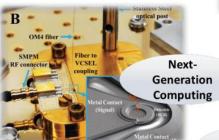
#### **Outline**

- ■Introduction & Background
- ■Wireline Communication Technology
- ■Characteristics of Modern High-Speed VCSELs
- ■VCSEL Transmitter Architecture
- ■Industry Analysis
- **■**Conclusion
- References



#### Introduction





**VCSELs** 







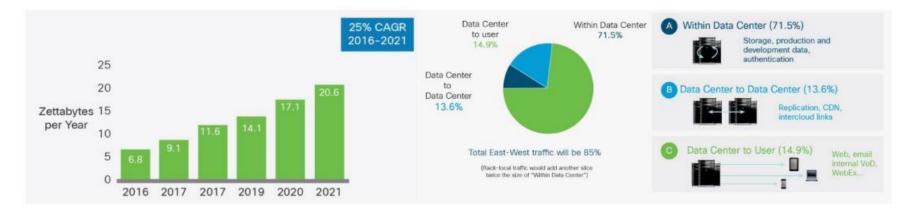
Autonomous







### **Background**



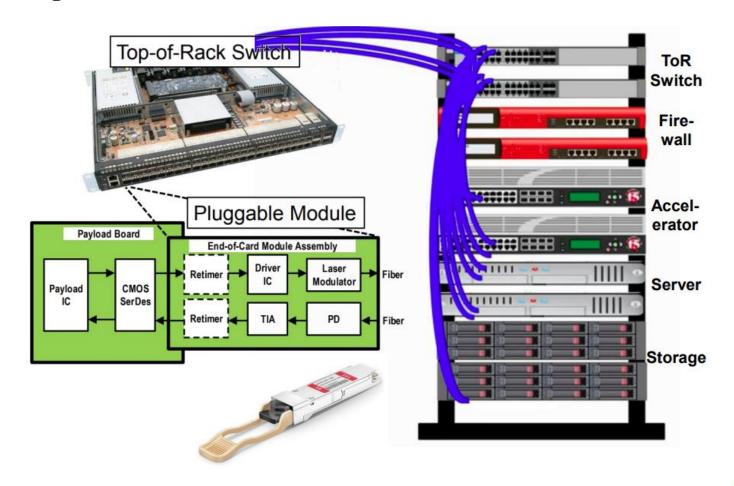
Source: Cisco Global Cloud Index 2016-2021

- Data center traffic increases ~25% per year
- Over 70% traffic remains within data center
- To increase its power efficiency is important



## **Background**

■ Top-of-Rack (ToR) Switch in the Data Center



# **Background**

IEEE P802.3bs <sup>™</sup> /D3.0							
Optical 400Gb/s							
Item	Name	Count	Ch.	Distance	Speed	Mod.	
1	400GBASE-SR16	16	ММ	0.5-100m	26.5625GBd	NRZ	
2	400GBASE-DR16	4	SM	2m to 500m	53.125GBd	PAM4	
3	400GBASE-FR16	8	SM	2m to 2km	26.5625GBd	PAM4	
4	400GBASE-LR16	8	SM	2m to 2km	26.5625GBd	PAM4	
Optical 200Gb/s							
Item	Name	Count	Ch.	Distance	Speed	Mod.	
1	200GBASE-DR16	4	SM	2m to 500m	26.5625GBd	PAM4	
2	200GBASE-FR16	4	SM	2m to 2km	26.5625GBd	PAM4	
3	200GBASE-LR16	4	SM	2m to 2km	26.5625GBd	PAM4	



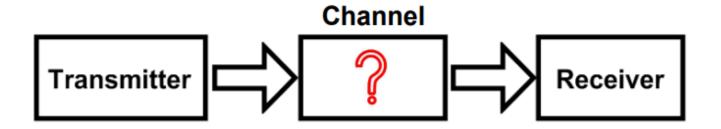


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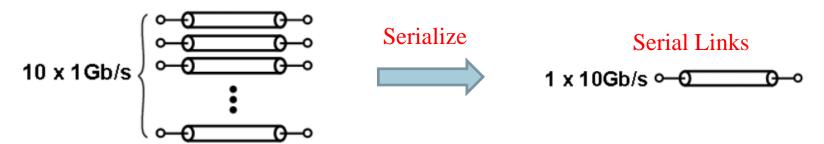


- Transmitter (TX): Transmit the signal through "channel"
- Channel: Impair the transmitted signal
  - ➤ Wireline: Coaxial, Fiber, Backplane trace, etc.
  - ➤ Wireless: Free-space, Multi-path reflection, etc.
- Receiver (RX): Recover the distorted data





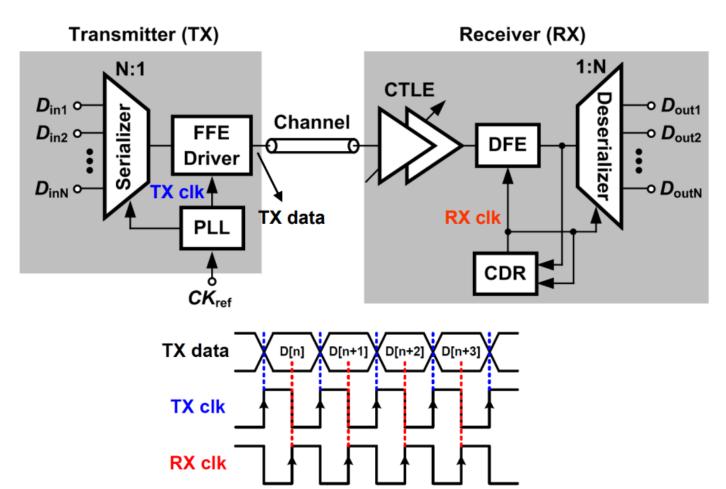
#### Parallel Links



- Channel is expensive
- Reduce the area of the interconnections
- Synchronization for parallel links is difficult
- ➤ Cost of higher channel loss (increased bandwidth) and complicated circuit design





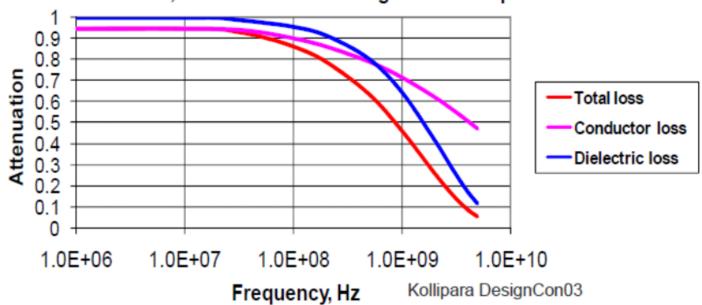






■ Why optical channel?

FR4 dielectric, 8 mil wide and 1m long 50 Ohm strip line

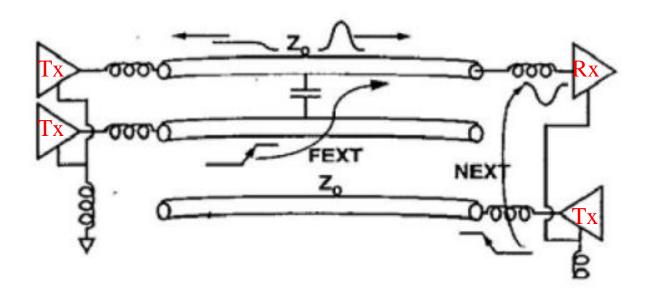


- Skin Effect Loss  $\propto \sqrt{F}$
- Dielectric Loss ∝ F





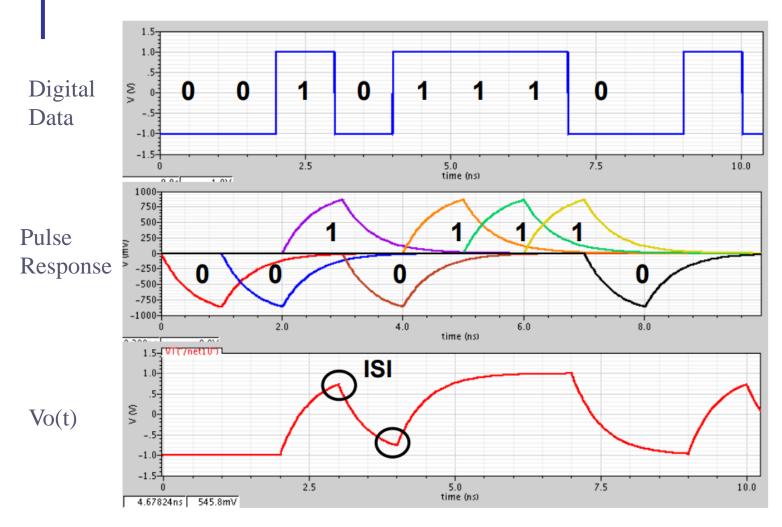
■ Why optical channel?



- "Near-end" xtalk: NEXT (reverse wave)
- "Far-end" xtalk: FEXT (forward wave)



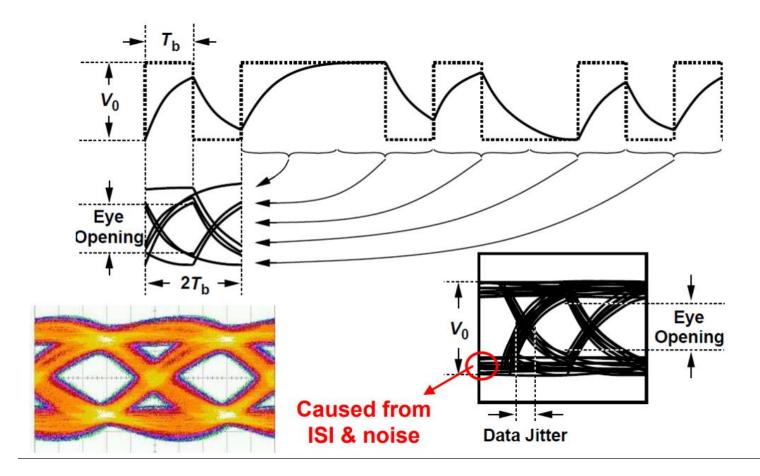








■ Eye diagram



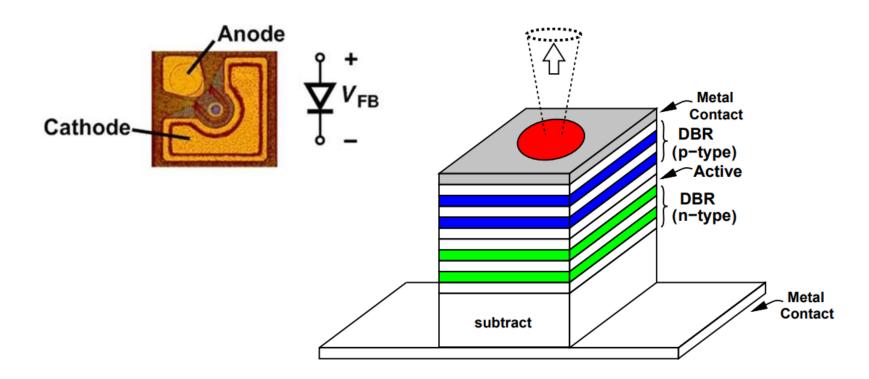


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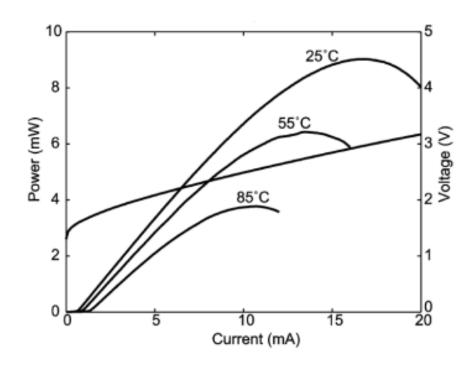








#### DC response



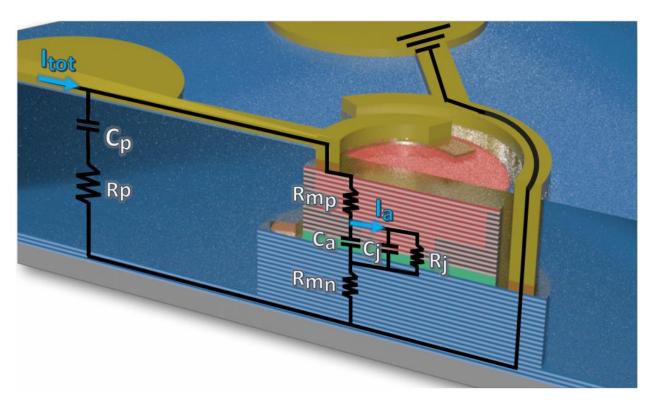
V-I : voltage drop in different modulation current P-I :

$$P_{out} = \eta \times (I_{VCSEL} - I_{TH})$$



AC response

$$H(f) = H_{intrinsic}(f) \cdot H_{electric}(f)$$







■ AC response

Electron density N, photon density Np, laser cavity volume V Rate equations:

$$\frac{dN}{dt} = \frac{I_{VCSEL}}{qV} - \frac{N}{\tau_{sp}} - GNN_p \quad \text{and} \quad$$

$$\frac{dN_p}{dt} = GNN_p + \beta_{sp} \frac{N}{\tau_{sp}} - \frac{N_p}{\tau_p}.$$



■ AC response
Output optical power Po:

$$P_o = N_p h \nu V v_g$$
.

$$\frac{P_o(s)}{I_{VCSEL}(s)} = \frac{h\nu v_g \alpha_m}{q} \times \frac{GN_p}{s^2 + s\left(GN_p + \frac{1}{\tau_{sp}}\right) + \frac{GN_p}{\tau_p}}.$$

$$H(f) = const \times \frac{f_r^2}{f_r^2 + j\left(\frac{f}{2\pi}\right)\gamma - f^2}.$$



■ AC response Resonance frequency:

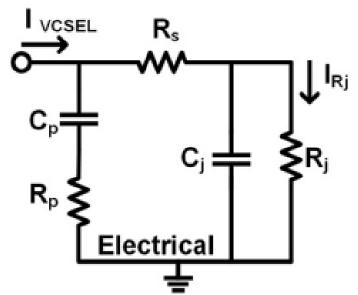
$$f_r = \frac{1}{2\pi} \sqrt{\frac{GN_p}{\tau_p}} \ .$$

$$f_r = D\sqrt{I_{VCSEL} - I_{TH}}$$
.

$$\gamma = K f_r^2 + \gamma_0 \, .$$



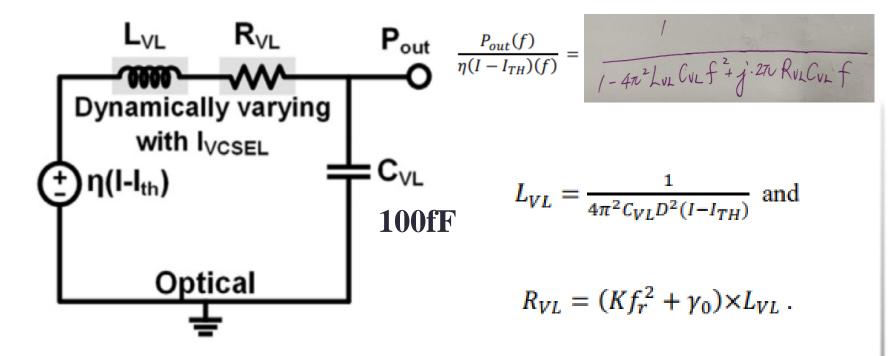




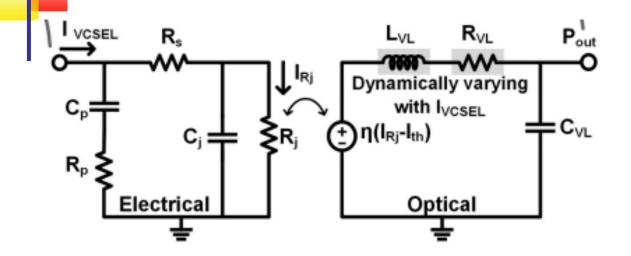
Parameter	Value	
Junction Capacitance (C <sub>j</sub> )	110-117fF	
Junction Resistance (R <sub>j</sub> )	180-150Ω	
DBR Resistance (R <sub>s</sub> )	50Ω	
Pad Capacitance (Cp)	10fF	
Pad Resistance (R <sub>p</sub> )	$1\Omega$	

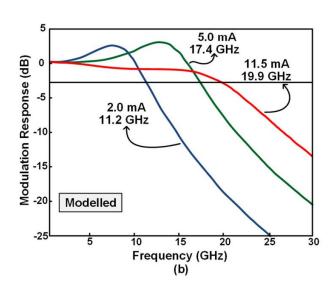






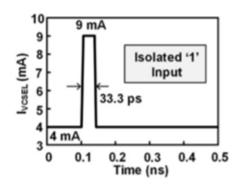


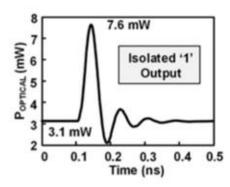


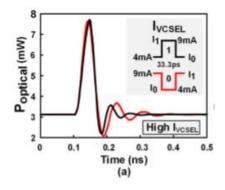


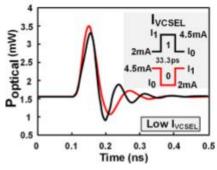


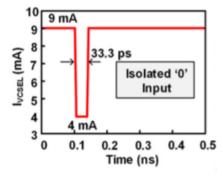


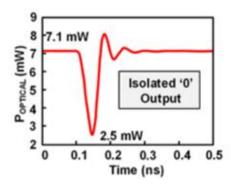


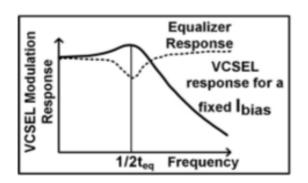
















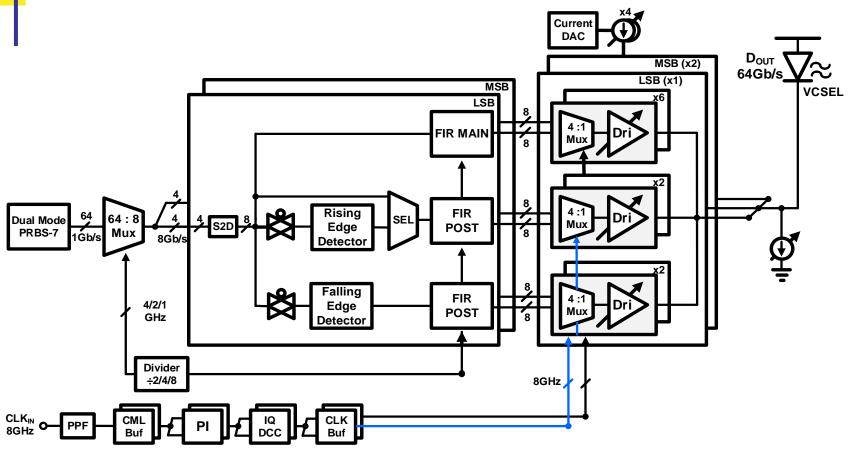
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#### **VCSEL** Transmitter Architecture

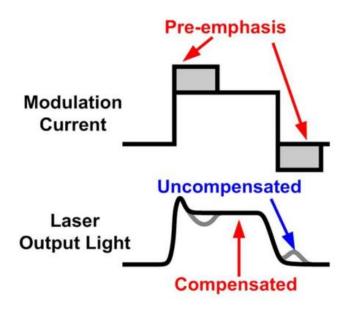


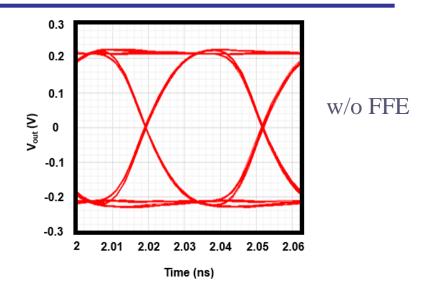


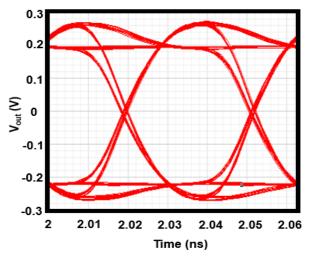


#### **VCSEL** Transmitter Architecture

■ Tx electrical output







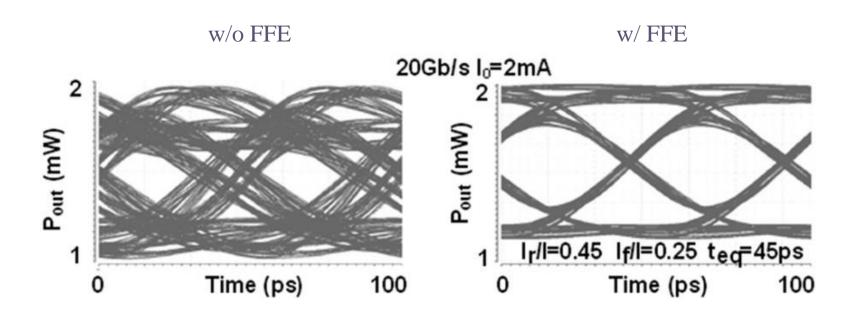
w/FFE





#### VCSEL Transmitter Architecture

■ VCSEL optical output







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### **Industry Analysis**

■ Porter's five forces analysis



Bargaining power of customers

- High switching cost
- High product differentiation
- Low bargaining power of customers



Bargaining power of suppliers

- High bargaining power for optical component and foundry suppliers
- Low bargaining power for PCB suppliers



Competitive rivalry

- High market concentration
- High product differentiation
- High competitive rivalry



Threat of substitutes

- No substitute
- Market still has room to go



Threat of new entrants

- High entry costs
- Large market growth
- Still has the threat of new entrants



### **Industry Analysis**

#### Strengths

- Low cost of processing
- Low power consumption in Tx and Rx circuit
- Less signal degradation

#### Weakness

- Low power output of VCSELs
- Limited distance
- Nonlinearity

#### Opportunities

- Achieving high modulation bandwidth at small current
- Increase optical output power

#### **Threats**

New interconnection technology





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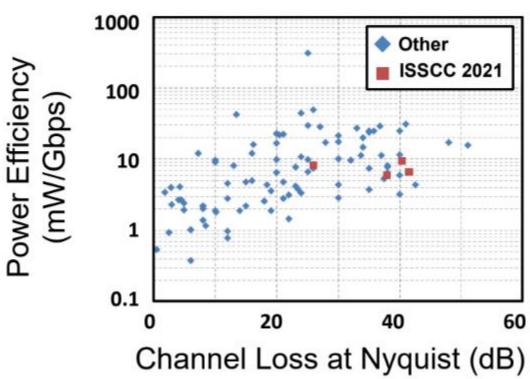
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#### **Conclusion**

#### **Transceivers Power Efficiency**



Source: ISSCC 2021 Wireline Trends





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- M. Ray el al., "A Modelling and Nonlinear Equalization Technique for a 20 Gb/s 0.77 pJ/b VCSEL Transmitter in 32 nm SOI CMOS", May 05, 2016.
- Hao Tien Cheng el al., "Recent Advances in 850 nm VCSELs for High-Speed Interconnects", Feb 13, 2022.
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- Pen-Jui Peng, "Communication Electronics" lecture
- Po-Lin Lee, "A 64Gb/s 4-Level Pulse-Amplitude Modulation Current-mode VCSEL-based transmitter with 2-tap Dual-Mode Adjustable Nonlinear FFE in 40nm CMOS", Jul, 2019.
- ISSCC 2022, SESSION 17, Advanced Wireline Links and Techniques





# Thank you!

