**CS 3339**

**Computer Architecture**

**Fall 2014**

**Homework 2 Problems**

**2.1) Why is binary backwards compatibility so important?**

Backwards compatibility is important because software is more expensive then hardware. If hardware companies want their chip to be bought it needs to be able to run old code faster not force preexisting software to conform to the introduction of new hardware.

**2.2) Why is there no mov (copy one register’s content into another) instruction in the MIPS ISA, i.e., what are the benefits of not implementing this instruction in hardware?**

MIPS attempts to keep their instruction set minimal. The move instruction can be implemented thru

add Rd, Rs, Rt

If a instruction can be implemented though preexisting instructions it is beneficial to hardware because it keeps the complexity of hardware to a minimum.

**2.3) Which of the fields in a MIPS R-type instruction does jr use and how many bits are left unused?**

32 – 6 – 6 – 5 = 15 bits unused.

**2.4) What is the benefit of requiring one of the source registers to also be a destination register (as is the case for many x86 instructions)?**

By allowing one of the source registers to also be a destination it puts more pressure on the limited registers, and allowing one of the operands to be in memory.

**2.5) Compute the address from which the load instruction below reads, the address to which the branch transfers control if taken, and the address that is the target of the jump instruction. All answers should be given in hexadecimal.**

0x80000000: addi $t1, $zero, 1  
0x80000004: lh $t1, 1($t1) 1 + 1 = 0x2 (load addr)  
0x80000008: bne $t1, $zero, 1 0x8000000C + 1\*4 = 0x80000010  
0x8000000C: j 1 ~~0x80000010~~ : 1\*4 = 0x80000004

**2.6) Assume we have two processors A and B whose native ISAs are ISAA and ISAB, respectively. Even if ISAA is quite different from ISAB, it is still possible to emulate ISAA on processor B. Is it also possible for code written in ISAA to run faster in emulated mode on processor B than running natively on processor A? Explain your answer.**

You are able to emulate ISAA on processor B. The code can run faster if processor B. During the process of running the code it will manipulate it to ensure success, so long as it can do so without a reasonable amount of delay it will be successfully faster.

**2.7) The ARM ISA only has 16 registers whereas MIPS has 32. Name two key benefits of only having 16 registers.**

 Requires fewer bits in the instruction word to specify a register number (leaving more bits for other fields);

Secondly Faster register file access

**2.8) Explain how the branch destination address is computed in MIPS.**

Two zero bits are concatenated with the 16-bit immediate field from the instruction word (such that the zeros form the LSBs), the resulting 18-bit value is sign extended to 32 bits and then added to the PC+4.

**2.9) The MIPS ISA has no “bgt a, b, label” (branch greater than) instruction. Provide a sequence of two MIPS assembly instructions that will accomplish the “bgt a, b, label” operation.**

slt $t0, $rs, $rt

bne $t0, $zero, LABEL

**2.10) Name one key advantage of CISC over RISC.**

CISC uses a complex instruction set that puts more emphasis on hardware handling instructions over that of software. By doing so there are fewer instructions than what RISC would implement and therefore shorter programs are produced. The belief is shorter programs allow the hardware to do the work more quickly.