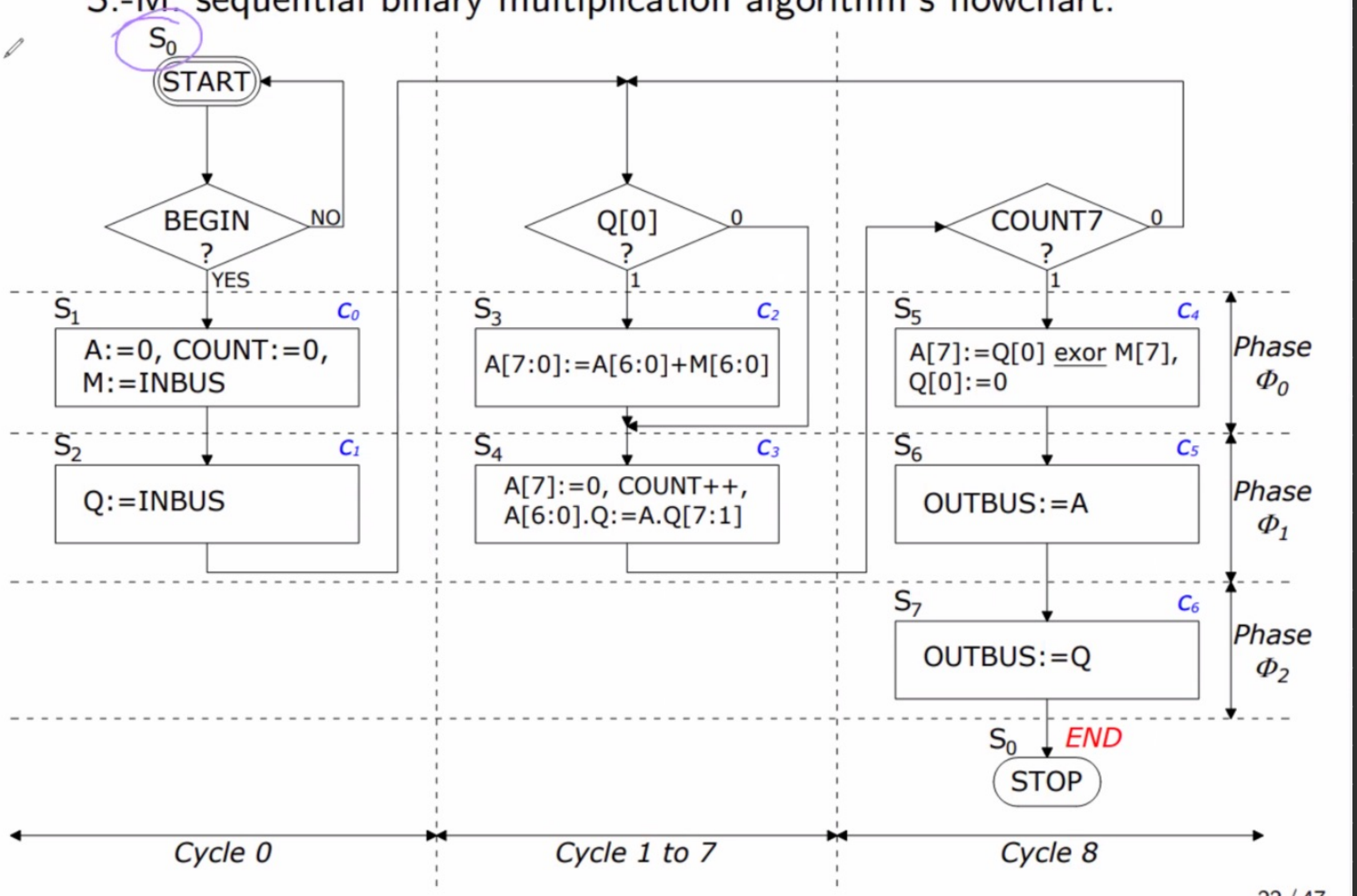
Serial Adder

-> FSM state table

-> Flowchart pt. Control Unit

4.3 - Elements of Control Unit synthesis

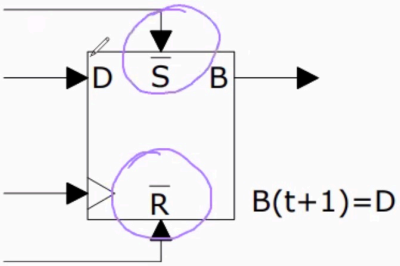
S.-M. sequential binary multiplication algorithm's flowchart:



(A) state table method — Minim — $S \rightarrow 2^n$ — 8 stari → 3 bit.

(B) One Hot — Fiecare stare are un bit "Maxim"

Consider using D type flip flops:



n variabile de stare pt. m stări

$B_n == 1 \rightarrow$ state $= S_n$

$$\Delta_0 = B_0 \cdot \overline{BEGIN} + B_7$$

$$\Delta_1 = B_0 \cdot BEGIN$$

$$\Delta_2 = B_1$$

Excitation Equations

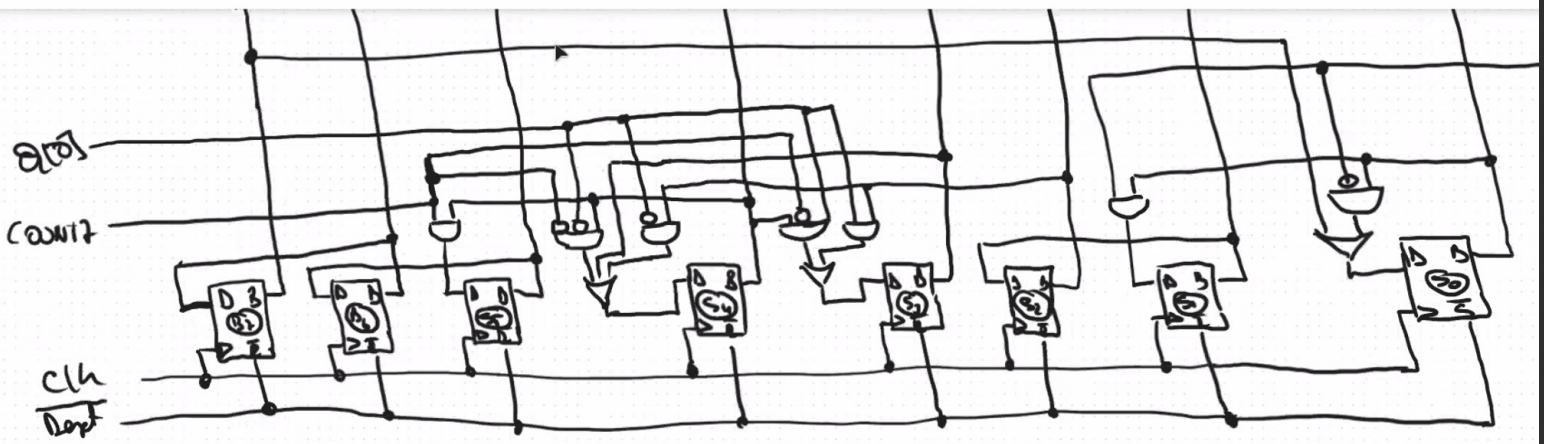
$$\Delta_3 = B_2 \cdot Q[0] + B_4 \cdot \overline{count\,7} \cdot Q[0]$$

$$\Delta_4 = B_2 \cdot \overline{Q[0]} + \Delta_3 + B_4\, \overline{count\,7}\, \overline{Q[0]}$$

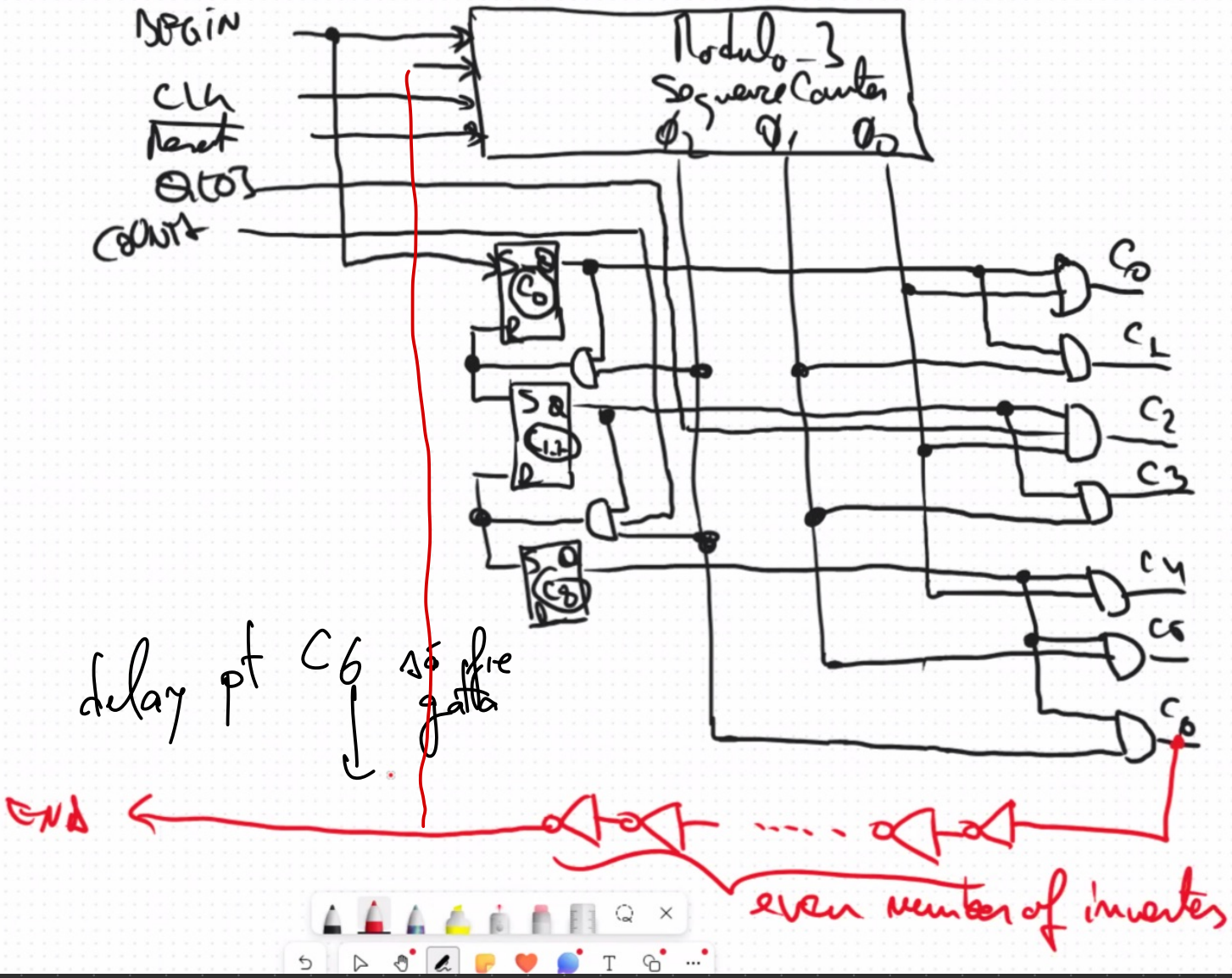
$$\Delta_5 = \Delta_4\, count\,7$$

$$\Delta_6 = B_5$$

$$\Delta_7 = B_6$$



III Sequence Counter



4.3 - Elements of Control Unit synthesis (contd.)

(C): Sequence Counter (continued)