3.3 Write Policies

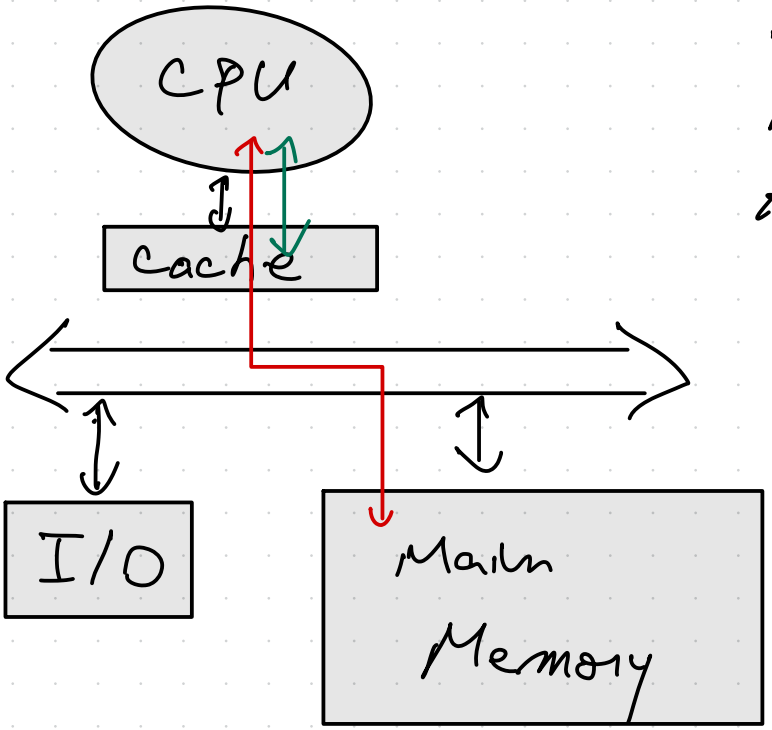
Hit
- WT Write Through – cache + write buffer
- WB Write Back

Miss
- Read → Allocate
- write
  - a write Allocate
  - b write no allocate

3.4. Cache Performance

DMA
Direct
Memory
Access

% BUS Bandwidth



"Nu am fetiș-uri cu Simion

Pilda 1

SIMD

Single Instr. Multiple Data

AVX

CPI ideal = 0.5 c.c

Mem. Access / instr. = 3

Miss Rate = 11%

Miss Penalty = 6 c.c.

CCT = 4 ns

AMAT = ? Avg. Mem. Acc. Time

CPU time = ?

(+)

AMAT = 1. ac. + Miss Rate × Miss Penalty

= 4 ns + 0.11 × $\underbrace{4\text{ns} \times 6\text{cc}}_{24}$

Cache Access → 1 C.C. = **6.64 ns**

CPU time = IC × (CPI ideal + Mem Acc / Instr × Miss Rate × Miss Pen. (cc)) × CCT

= IC × (0.5 + 3 × 0.11 × 6) × 4 ns

≈ 41,92 ns × IC

$$\frac{\text{Performance Cache}}{\text{Perf. Ideal}} = \frac{CPU_{time\ ideal}}{\text{cache}} = \frac{IC \times 34}{IC \times 41.92} =$$

$$= 0.811$$

scade perf. 0.189

Pilda 2

64 kiB cache data

CCT = 20 ns

Mem acc / instr. = 1.3

CPI ideal = 1.5 cc

SA -> clk. degradation of 8.5%

	DM	2-way SA
Miss Rate	3.9%	3%

Miss Penalty = 200 ns

$AMAT_{DM} = 20\ ns + 0.039 \times 200\ ns = 27.8\ ns$

$AMAT_{SA} = 21.7\ ns + 0.03 * 200\ ns = 27.7\ ns$

$CCT_{SA} = \underset{clk.deg}{1.085} \times CCT_{DM} = 1.085 \times 20ns = 21.7\ ns$

$CPU_{time} = IC \times (CPI_{ideal} + Mem.acc/instr \times Miss\ Rate \times Miss\ Pen \times CCT)$

$CPU_{time\ DM} = IC \times (1.5 \times 20\ ns + 1.3 \times 0.039 \times 200\ ns) \times 20\ ns$

$IC \times 40.14\ ns$

$CPU_{time\ SA} = IC \times 40.35\ ns \quad (1.5 \times 21.7 + 1.3 \times 0.03 \times 200) \times 20\ ns$

"Bossul, Sumisul Ti-ului"

HAI SET

Pilda 3

BUS Bandwidth = 10^9 words/sec
BUS width = 2 words
Hit Rate = 90%
1 block = 4 words

10^8 words/sec Proc. ref. rate writes/sec

30% writes
35% dirty blocks
write allocate for a miss a) WB
b) WT

$$\underbrace{10^8 \text{ words/sec}}_{\text{ref-rate}} \times \underbrace{0.1}_{\text{miss rate}} \left(0.7 \times \text{Read MissPen} + 0.3 \times \text{Write MissPen} \right)$$

$$\text{Read Miss Penalty}_{WB} = \underbrace{\frac{\text{Block Size}}{\text{Bus Width}} \times \text{BUS Reads}}_{\text{Allocate}}$$

$$+ \underbrace{0.35}_{\text{dirty blocks}} \times \frac{\text{Block Size}}{\text{Bus Width}} \times \text{BUS Writes}$$

$$= 2 \text{ BUS Reads} + 0.7 \text{ BUS Writes}$$

$$= 2.7 \text{ BUS Accesses}$$

Write Miss Penalty$_{WB}$ = $\underbrace{2 \text{ BUS Reads}}_{\text{Allocate}}$ +

+ $\underbrace{0.7 \text{ BUS Writes}}_{\text{Update}}$ = 2.7 BUS Accesses

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% BUS used = $\frac{10^7 \times 2.7 \text{ (Accesses)}}{10^9 \text{ cycles/sec}}$ = 2.7%

WT $10^6 \times 0.1 \times (0.7 \times \text{Read Miss Pen}^5 + 0.3 \times \underset{\text{Miss Pen}^5}{\text{Write}})$

$+ 10^6 \times \underbrace{0.9}_{\text{hit}} \times \underbrace{0.3}_{\text{writes}} \times \text{Write Hit Penalty}^5$

Read Miss Pen. = $\underbrace{\frac{4}{2} \text{ BUS Reads}}_{\text{Allocate}}$ = 2 BUS Accesses

Write Miss Pen^5 = $\underbrace{\frac{4}{2} \text{ BUS Reads}}_{\text{Allocate}} + \underbrace{1 \text{ BUS Write}}_{\text{MM Write}}$

= 3 BUS Accesses

Write Hit Pen.^{5} = $\underbrace{1 \text{ BUS Acc.}}_{\text{MM Write}}$

$10^7 \times (0.7 \times 2 + 0.3 \times 3) + 10^6 \times 0.9 \times 0.3$

$= 5 \times 10^7$

% BUS used = $\frac{5 \cdot 10^7}{10^9}$ = 5%