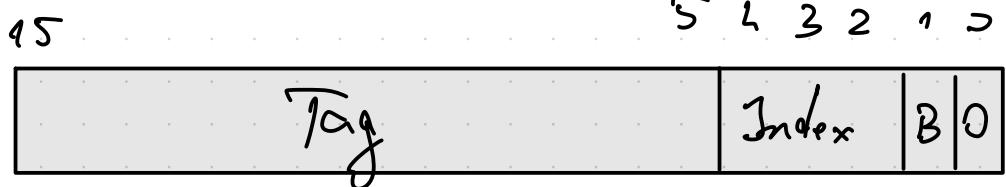


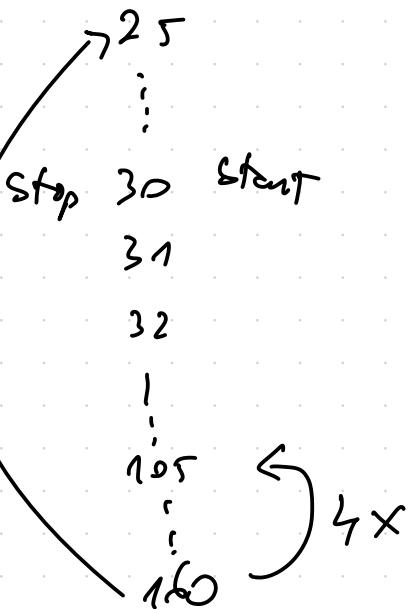
- 4-way SA
- 8 sets = 2^3 Index
- 4 words / block
 2^2 BO

- Size (M_2) = 2^{16} words
- Word addressing
- Cache access time = 2ms
- Miss Penalty = 20ms
- LRU replacement

a) Address format



b) Hit Ratio, Avg. Mem., Access Time



| V | Tat | Date |
|---|-----|---------|
| 0 | 1 | 32 - 35 |
| 1 | 1 | 36 - 39 |
| 2 | 1 | 40 - 43 |
| 3 | 1 | 44 - 47 |
| 4 | 1 | 48 - |
| 5 | 1 | |
| 6 | 1 | 56 - 59 |
| 7 | 1 | 28 - 31 |

| V | Tat | Date |
|---|-----|---------|
| 0 | 1 | 64 - 67 |
| 1 | 1 | |
| 2 | 1 | |
| 3 | 1 | |
| 4 | 1 | |
| 5 | 1 | |
| 6 | 2 | 88 - 91 |
| 7 | 1 | 60 - 63 |

| V | Tat | Date |
|---|-----|-----------|
| 0 | 3 | 76 - 99 |
| 1 | 1 | |
| 2 | 1 | |
| 3 | 1 | |
| 4 | 1 | |
| 5 | 1 | |
| 6 | 3 | 120 - 123 |
| 7 | 1 | 92 - 95 |

| V | Tat | Date |
|---|-----|-----------|
| 0 | 4 | 128 - 131 |
| 1 | 1 | |
| 2 | 1 | |
| 3 | 1 | |
| 4 | 1 | |
| 5 | 1 | |
| 6 | 4 | 952 - 955 |
| 7 | 3 | 924 - 927 |

| | | |
|-----|---|-----|
| 0 | - | 3 |
| 4 | - | 7 |
| 8 | - | 11 |
| 12 | - | 15 |
| 16 | - | 19 |
| 20 | - | 23 |
| 24 | - | 27 |
| 28 | - | 31 |
| 32 | - | 35 |
| 36 | - | 39 |
| 40 | - | 43 |
| 44 | - | 47 |
| 48 | - | 51 |
| 52 | - | 55 |
| 56 | - | 59 |
| 60 | - | 63 |
| 64 | - | 67 |
| 68 | - | 71 |
| 72 | - | 75 |
| 76 | - | 79 |
| 80 | - | 83 |
| 84 | - | 87 |
| 88 | - | 91 |
| 92 | - | 95 |
| 96 | - | 99 |
| 100 | - | 103 |

| | | |
|----|-----|-------|
| 0 | 104 | - 107 |
| 1 | 108 | - 111 |
| 2 | 112 | - 115 |
| 3 | 116 | - 119 |
| 4 | 120 | - 123 |
| 5 | 124 | - 127 |
| 6 | 128 | - 131 |
| 7 | 132 | - 135 |
| 8 | 136 | - 139 |
| 9 | 140 | - 143 |
| 10 | 144 | - 147 |
| 11 | 148 | - 151 |
| 12 | 152 | - 155 |
| 13 | 156 | - 159 |
| 14 | 160 | - 163 |
| 15 | 164 | - 167 |
| 16 | .. | .. |
| 17 | .. | .. |

$$\begin{aligned}
 & 30, 31 \quad 1M \quad 1H \\
 & 32 - 35 \quad 1M \quad 3H \\
 & 36 - 39 \quad 1M \quad 3H \\
 & 40 \quad | \\
 & 43 \quad | \\
 & 48 \quad | \\
 & 52 \quad | \\
 & 56 - 59 \quad — \\
 & (1M) + (1M) \times 31
 \end{aligned}$$

$$\begin{aligned}
 & 39 / 8 = 4 \quad 2.7 \\
 & 156 - 159 \\
 & + (1M) + (3H)
 \end{aligned}$$

| | V | Tag | Data |
|---|---|-----|-----------|
| 0 | n | 5 | 160 - 163 |
| 1 | n | 1 | 36 - 39 |
| 2 | 1 | 1 | 40 - 43 |
| 3 | 1 | 1 | 44 - 47 |
| 4 | 1 | 1 | 48 - |
| 5 | 1 | 1 | |
| 6 | 1 | 1 | 56 - 59 |
| 7 | 1 | 4 | 156 - 159 |

| | V | Tag | Data |
|---|---|-----|---------|
| 0 | n | 2 | 64 - 67 |
| 1 | 1 | 1 | |
| 2 | 1 | 2 | |
| 3 | 1 | 2 | |
| 4 | 1 | 2 | |
| 5 | 1 | 2 | |
| 6 | 1 | 2 | 88 - 91 |
| 7 | 1 | 1 | 60 - 63 |

| | V | Tag | Data |
|---|---|-----|-----------|
| 0 | n | 3 | 76 - 99 |
| 1 | 1 | 1 | |
| 2 | 1 | 2 | |
| 3 | 1 | 2 | |
| 4 | 1 | 2 | |
| 5 | 1 | 2 | |
| 6 | 1 | 3 | 120 - 123 |
| 7 | 1 | 2 | 92 - 95 |

| | V | Tag | Data |
|---|---|-----|-----------|
| 0 | n | 4 | 128 - 131 |
| 1 | 1 | 4 | |
| 2 | 1 | 4 | |
| 3 | 1 | 4 | |
| 4 | 1 | 4 | |
| 5 | 1 | 4 | |
| 6 | 1 | 4 | 952 - 955 |
| 7 | 1 | 3 | 124 - 127 |

| | V | Tag | Data |
|---|---|-----|-----------|
| 0 | 1 | 15 | 160 - 163 |
| 1 | 1 | 1 | 32 - 35 |
| 2 | 1 | 1 | 36 - 39 |
| 3 | 1 | 1 | 40 - 43 |
| 4 | 1 | 1 | 44 - 47 |
| 5 | 1 | 1 | 48 - 51 |
| 6 | 1 | 1 | 52 - 55 |
| 7 | 1 | 4 | 56 - 59 |
| 8 | 1 | 4 | 156 - 159 |
| 9 | 1 | 4 | 28 - 31 |

| | V | Tag | Data |
|---|---|-----|---------|
| 0 | 1 | 2 | 64 - 67 |
| 1 | 1 | 2 | 68 - 71 |
| 2 | 1 | 2 | 72 - 75 |
| 3 | 1 | 2 | 76 - 79 |
| 4 | 1 | 2 | 80 - 83 |
| 5 | 1 | 2 | 84 - 87 |
| 6 | 1 | 2 | 88 - 91 |
| 7 | 1 | 10 | 60 - 63 |

| | V | Tag | Data |
|---|---|-----|-----------|
| 0 | 1 | 3 | 96 - 99 |
| 1 | 1 | 3 | 100 - 103 |
| 2 | 1 | 3 | 104 - 107 |
| 3 | 1 | 3 | 108 - 111 |
| 4 | 1 | 3 | 112 - 115 |
| 5 | 1 | 3 | 116 - 119 |
| 6 | 1 | 3 | 120 - 123 |
| 7 | 1 | 2 | 92 - 95 |

| | V | Tag | Data |
|---|---|-----|-----------|
| 0 | 1 | 4 | 128 - 131 |
| 1 | 1 | 4 | 132 - 135 |
| 2 | 1 | 4 | 136 - 139 |
| 3 | 1 | 4 | 140 - 143 |
| 4 | 1 | 4 | 144 - 147 |
| 5 | 1 | 4 | 148 - 151 |
| 6 | 1 | 4 | 152 - 155 |
| 7 | 1 | 3 | 124 - 127 |

$$\left(\frac{1M}{1H} + \frac{1M}{3H}\right) \times 31 + \left(\frac{1M}{3H} + \frac{1M}{0H}\right) + \left(\frac{0M}{56H}\right) \times 4 + \left(\frac{1M}{2H} + \frac{1M}{2H}\right)$$

$$\text{Hit Ratio} = \frac{325}{361}$$



$$\begin{array}{r} 56 \times \\ 4 \\ \hline 224 + \\ 101 \\ \hline 325 \end{array}$$

36 Misses
325 Hits

361 Accesses

$$\text{Hit Ratio} = 90\% \quad \frac{325}{361}$$

$$\text{Avg. Mem. Access Time} = \text{Acc} \times \text{Hit Rate} + (\text{Acc} + \text{Miss Pen.}) \times \text{Miss Rate}$$

$$= \text{f.ac} \underbrace{(\text{Hit} + \text{Miss Rate})}_{1} + \text{Miss Pen.} \times \text{Miss Rate} =$$

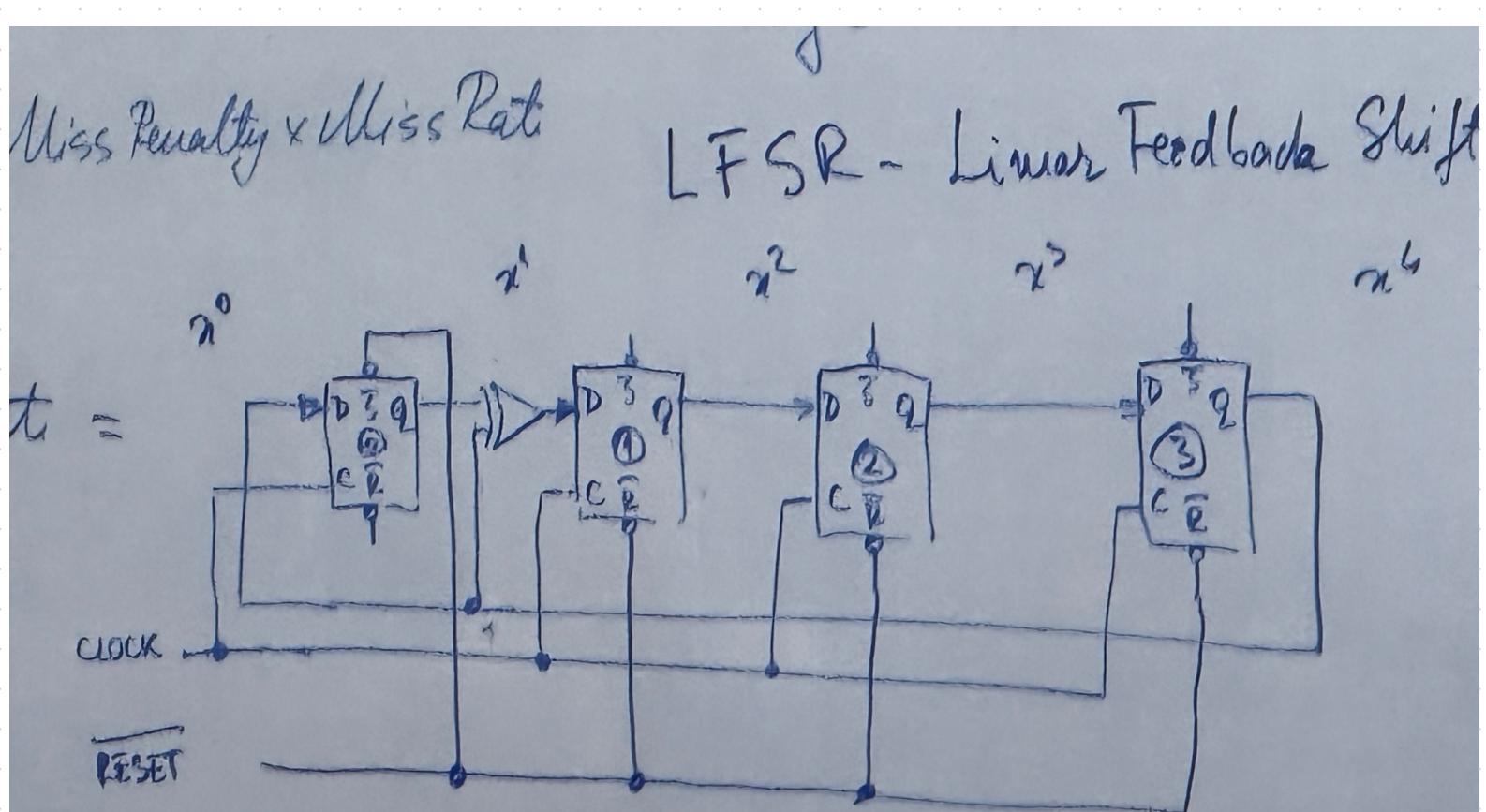
$$= 2 \mu s + 20 \mu s \times 0.1 = \underline{\underline{4 \mu s}}$$

3.2. Replacement Policies

- Only for SA and FA caches

- a) FIFO x
- b) Random
- c) Least Recently Used (LRU)

5) Galois Field Polynomials $G(x) = x^3 + x + 1$
LFSR Linear Feedback Shift Registers



| | D_0 | D_1 | D_2 | D_3 | Decimal |
|----|-------|-------|-------|-------|---------|
| →1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 2 |
| 3 | 0 | 0 | 1 | 0 | 4 |
| 4 | 0 | 0 | 0 | 1 | 8 |
| 5 | 1 | 1 | 0 | 0 | 3 |
| 6 | 0 | 1 | 1 | 0 | 6 |
| 7 | 0 | 0 | 1 | 1 | 12 |
| 8 | 1 | 1 | 0 | 1 | 11 |
| 9 | 1 | 0 | 1 | 0 | 5 |
| 10 | 0 | 1 | 0 | 1 | 10 |
| 11 | 1 | 1 | 1 | 0 | 7 |
| 12 | 0 | 1 | 1 | 1 | - |
| 13 | 1 | 1 | 1 | 1 | 14 |
| 14 | 1 | 0 | 1 | 1 | 15 |
| 15 | 1 | 0 | 0 | 1 | 13 |
| 16 | 1 | 0 | 0 | 0 | 9 |
| 17 | 0 | 1 | 0 | 0 | 1 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |

c) Age Registers

14, 7, 6, 12, 10, 6, 7, 14, 7, 3, 14 (same index)

4-way SA

c) age registers

14, 7, 6, 12, 10, 6, 7, 14, 7, 3, 14 (assumed to have the same index)

4-way SA

| | BANK | | | | AGE | | | |
|---------|------|-----|-----|------|-----|----|----|----|
| | 0 | 1 | 2 | 3 | 0* | 1* | 2* | 3* |
| initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| M 14 | 14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| M 7 | 14 | 7 | 0 | 0 | 1 | 0 | 0 | 0 |
| M 6 | 14 | 7 | 6 | 0 | 2 | 1 | 0 | 0 |
| M 12 | 14 | 7 | 6 | 12 | 3 | 2 | 1 | 0 |
| M 10 | 10 | 7 | 6 | 12 | 0 | 3 | 2 | 1 |
| H 6 | 10 | 7 | (6) | 12 | 1 | 3 | 0 | 2 |
| H 7 | 10 | (7) | 6 | 12 | 2 | 0 | 2 | 1 |
| M 14 | 10 | 7 | 6 | 14 | 3 | 1 | 2 | 0 |
| H 7 | 10 | (7) | 6 | 14 | 3 | 0 | 2 | 1 |
| M 3 | 3 | 7 | 6 | 14 | 0 | 1 | 3 | 2 |
| H 14 | 3 | 7 | 6 | (14) | 1 | 2 | 3 | 0 |

Miss

- replace the LRU
- put the age 0 for replaced block
- increment the ages of the other blocks

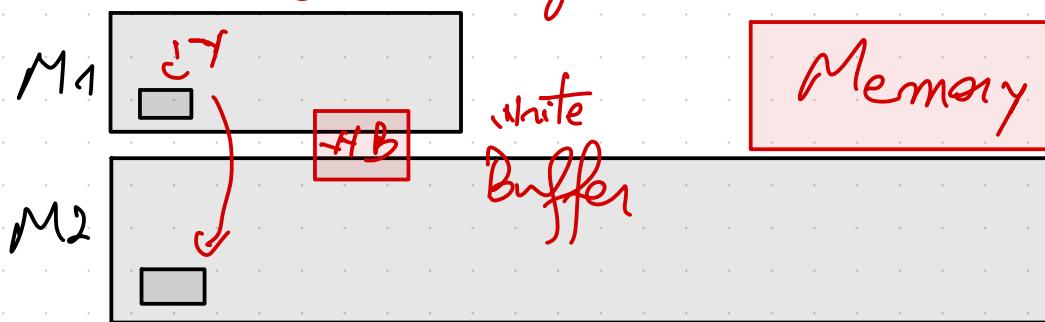
Hit

- put the age 0 for the hit block
- increment the ages that were < than the age of the hit block

3.3. Write Policies

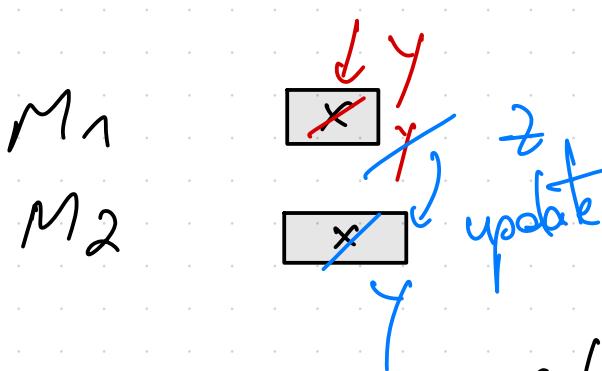
70% of all accesses
are writes

Write Through



Memory Coherence

Write Back



Update M₁ upon replacement

dirty Bit

(dace sa facut @ schimbare care necesita update)

3.4 Cache performance

- Metrics - Miss Rate - access time
- AMAT
- CPU time

Miss Causes \rightarrow Compulsory (cold-start.)
 \Rightarrow bigger block size

↓
Conflict \rightarrow multiple blocks
map at the same location
Capacity \rightarrow higher (SA)
 \downarrow bigger cache size

$$\text{AMAT} = \underbrace{\text{t. ac}}_{T_{\text{time}}} + \text{Miss Rate} \times \underbrace{\text{Miss Penalty}}_{\text{CCT}}$$
$$= (1 + \text{Miss Rate} \times \text{Miss Penalty}) \times \text{CCT}$$

$$\text{CPU}_{\text{time}} = \text{IC} \times \text{CPI} \times \text{cct} \quad \text{for a perfect cache}$$

$$\text{CPU}_{\text{time}} = \text{IC} \times (\text{CPI}_{\text{ideal}} + \frac{\text{Mem. accesses per inst.} \times (\text{Miss Pen.} \times \text{Miss Rate})}{(\text{CC})} \times \text{CCT})$$

"cel mai high, fără o întâia în altă conotație"