

2.4. Computer Performance Equation

Instn. Type	Freq.	CPI	Mosera L/S
ALU	43%	1	
Load	21%	2	
Store	12%	2	
Branch	24%	2	

25% ALU with one operand from the memory

LDR $r_1, [r_2]$

ADD r_3, r_1, r_4

ADD $r_3, [r_2], r_4$

ALU CPI $\rightarrow 2$
Branch CPI $\rightarrow 3$

$$\text{CPU time} = \text{IC} \times \text{CPI} \times \text{CCT} \left(\frac{\text{?}}{\text{CZ}} \right)$$

$$\text{CPI}_{L/S} = 0.43 \times 1 + 0.57 \times 2 = 1.57$$

$$\text{CPU time new} =$$

$$\text{IC}_{\text{new}} = \text{IC}_{L/S} \left(1 - 0.25 \cdot 0.43 \right)$$

$$\text{CPI}_{\text{new}} = 0.43 \cdot (1 - 0.25) \times 1 + 0.43 \cdot (0.25) \times 2$$

" I like to torture manelists "

M. Uddeswar

$$\begin{aligned}
 CPI_{\text{new}} = & \frac{0.43(1-0.25) \times 1 + 0.43 \times 0.25 \times 2}{ALU_1} + \\
 & + \frac{(0.21 - 0.43 \cdot 0.25) \times 2}{\text{Load}} + \frac{0.12 \times 2 + 0.24 \times 3}{\text{Store}} + \frac{0.24 \times 3}{\text{Branch}}
 \end{aligned}$$

$$1 - (0.25 \times 0.43)$$

$$CPU_{\text{time new}} = IC_{L/S} (1 - 0.25 \times 0.43) \times CPI_{\text{new}}$$

$$= IC_{L/S} \cdot 1.7025 \cdot CCT_{L/S}$$

$$CPU_{\text{time L/S}} = IC_{L/S} \cdot 1.57 \cdot CCT_{L/S}$$

BETTER

2.5. Other Metrics

MIPS millions of instr per second

MFLOPS millions of floating point ops. per sec.

$$\text{MIPS} = \frac{\text{IC}}{\text{CPU time} \times 10^6} = \overbrace{f_C \times \text{CFS} \cdot \text{CCT} \cdot 10^6}^{\text{IC}}$$

$$= \frac{\text{Clock Rate}}{\text{CPI} \times 10^6}$$

MIPS inconsistency

- ① varies with the program \Rightarrow depends on the instruction set
- ② can vary inversely with performance

P, Lda - dm Patterson & Hennessy

Optimized Compiler \rightarrow 50% reduction of all ALU

Clock cycle time 20 ns

$$\text{Clock rate} = \frac{1}{20 \times 10^{-9}} =$$

$$\text{CPU time L/S} = \text{IC}_{L/S} \times 1.57 \times 20 \text{ ns}$$

$$= \boxed{\text{IC}_{L/S} \times 31.4 \text{ ns}}$$

$$\text{MIPS}_{L/S} = \frac{50.10^6 \text{ s}^{-1}}{1.57 \cdot 10^9} = \underline{\underline{31.85}}$$

comp. optimisation

$$\text{CPU time CO} = \text{IC}_{CO} \times CPI_{CO} \times 20 \text{ ns}$$

$$\text{IC}_{CO} = \text{IC}_{L/S} (1 - 0.5 \times 0.43)$$

$$\text{CPI}_{CO} = (0.5 \times 0.43 \times 1) \times \cancel{\text{IC}_{L/S}} + (0.57 \times 2) \times \cancel{\text{IC}_{L/S}}$$

$$(1 - 0.5 \times 0.43) \cdot \cancel{\text{IC}_{L/S}}$$

$$\text{CPU time CO} = \text{IC}_{L/S} \times 27.1 \text{ ns}$$

$$\text{MIPS}_{CO} = \frac{50.10^6}{1.726 \cdot 10^9} = \underline{\underline{28.9}}$$

$$\text{Relative MIPS}_x = \frac{\text{Exec. time ref}}{\text{Exec. time}_x} \times \text{MIPS}_{\text{reference}}$$

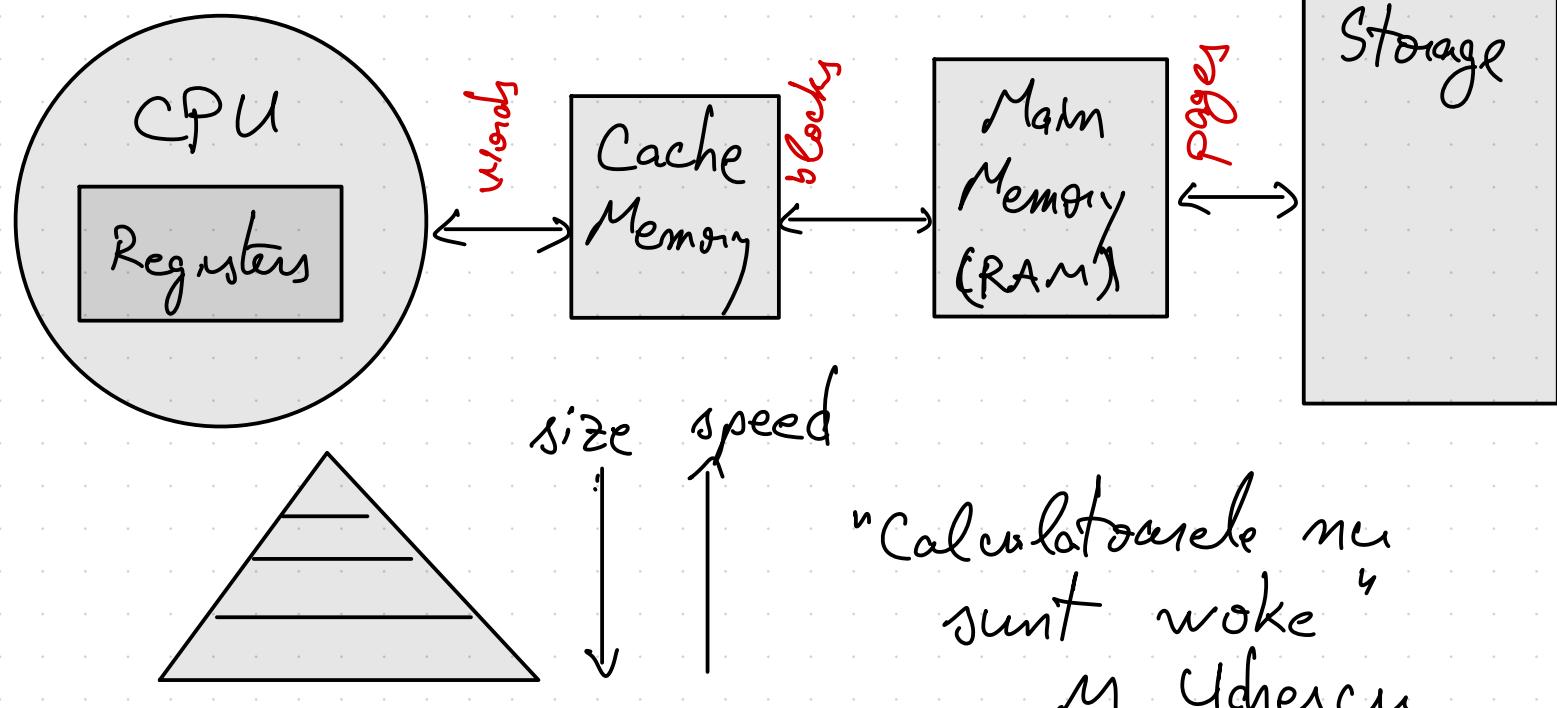
$\sqrt{A} \times 1/11 \rightarrow 1 \text{ MIPS machine}$

MFLOPS

$$\text{MFLOPS} = \frac{\sum C_{FP}}{\text{CPU time} \times 10^6}$$

Chapter 3

Memory Hierarchies



1 Byte \rightarrow 1 B

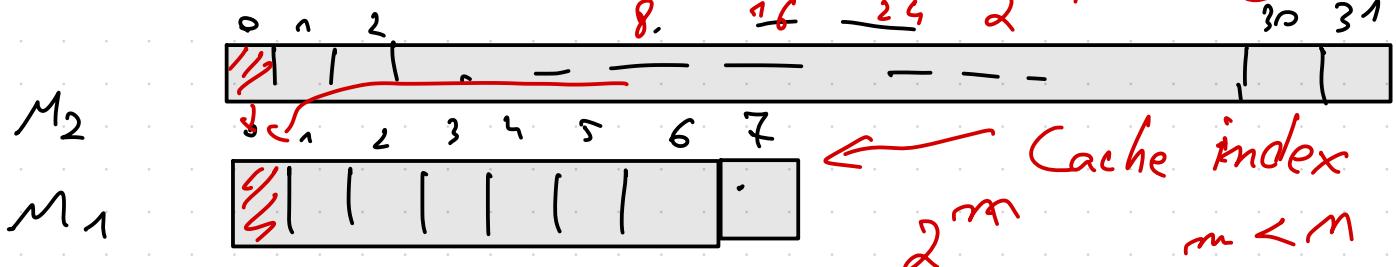
Word \rightarrow 1 or more bytes

3.1 Caches

Size $\begin{cases} \text{split} \\ \text{unified} \end{cases}$

Cache Coherence

3.1.1 Mapping



$$\begin{cases} n = 5 \\ m = 3 \end{cases}$$

$m_2(0), m_2(1), \dots, m_2(i), \dots m_2(2^m - 1)$

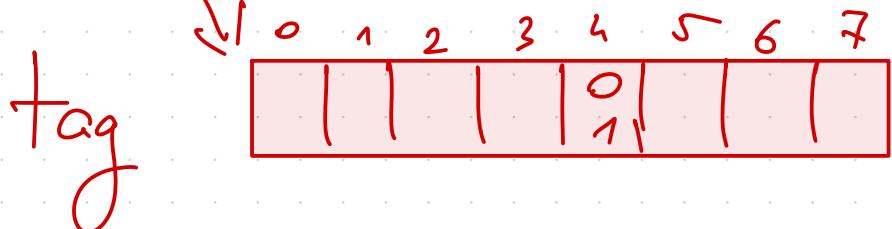
$$j = : \bmod 2^m \quad 0, 8, 16, 24 \rightarrow 0$$

$$j = 0 \bmod 8 = 0 \quad 1, 9, \dots \rightarrow 1$$

$$j = 92 \bmod 8 = 4$$

$\underbrace{}_{\bmod 8}$

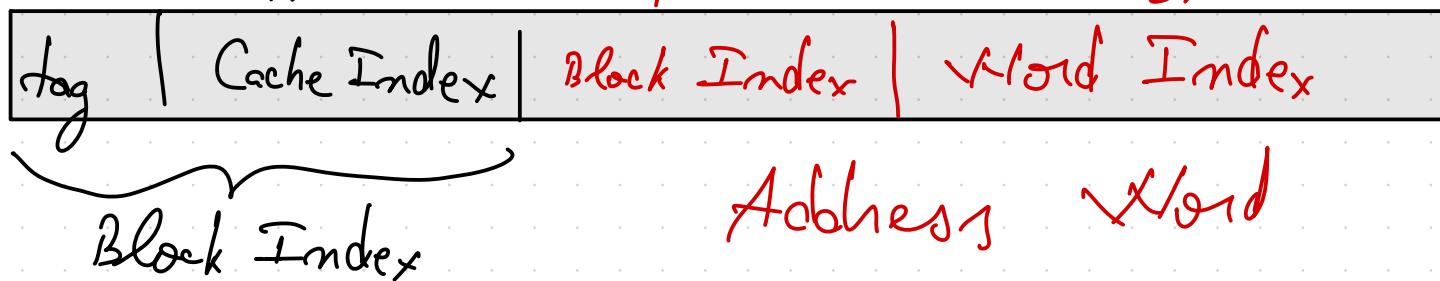
$$12 \quad 01100 \rightarrow 4 \quad \text{concat}(01, 100) = 4$$



$$\text{tag length} = \underline{n - m}$$

<n> <m> <p>

1 word 2^2 bytes
 1 block = 2 words



Example 1

$$\text{Size } (M_2) = 2^{24} \text{ words}$$

$$1 \text{ block} = 4 \text{ words}$$

$$1 \text{ word} = 1 \text{ byte}$$

$$\text{Size } (M_1) = 1 \text{ k block}$$

Address	Code
8192	230
1102	2713
12292	170

