3.4. Cache Performance

L/S Computers

Split cache < data / instructions

Example – 2% L/S insts.

IMR Insts Miss Rate = 8%

dMR data Miss Rate = 10%

Miss Penalty = 25 ns

Clk Rate = 3 GHz

t_{ac} = 1 cc

IC = 1000

a) AMAT = ?

b) CPU_{time} = ?

---

a) $AMAT = t_{ac} + Miss\ Rate \times Miss\ Pen$

$$CCT = \frac{1}{3 \cdot 10^{9}\ s^{-1}} = \frac{10^{-9}}{3}\ s = 0.333\ ns$$

$$Miss\ Pen^{CC} = \left\lceil \frac{25\ ns}{0.333\ ns} \right\rceil = 76\ c.c.$$

$$AMAT = 0.333\ ns + 76\ cc \times 0.333\ ns$$

Misses per Instr. $= \underbrace{1}_{\text{need instr to run anything}} \times \underbrace{0.08}_{IMR} + \underbrace{0.2}_{L/S\ instr} \times \underbrace{0.1}_{Amp}$

||

Mem. Acc per Instr $= \underline{\underline{0.1}}$

× Miss Rate

$$\text{Miss Rate} = \frac{\text{Miss Per Instr}}{\text{Mem Acc per Instr}} = \frac{0.1}{1 + 0.2} = \underline{\underline{0.083}}$$

Miss Rate = 8,33%

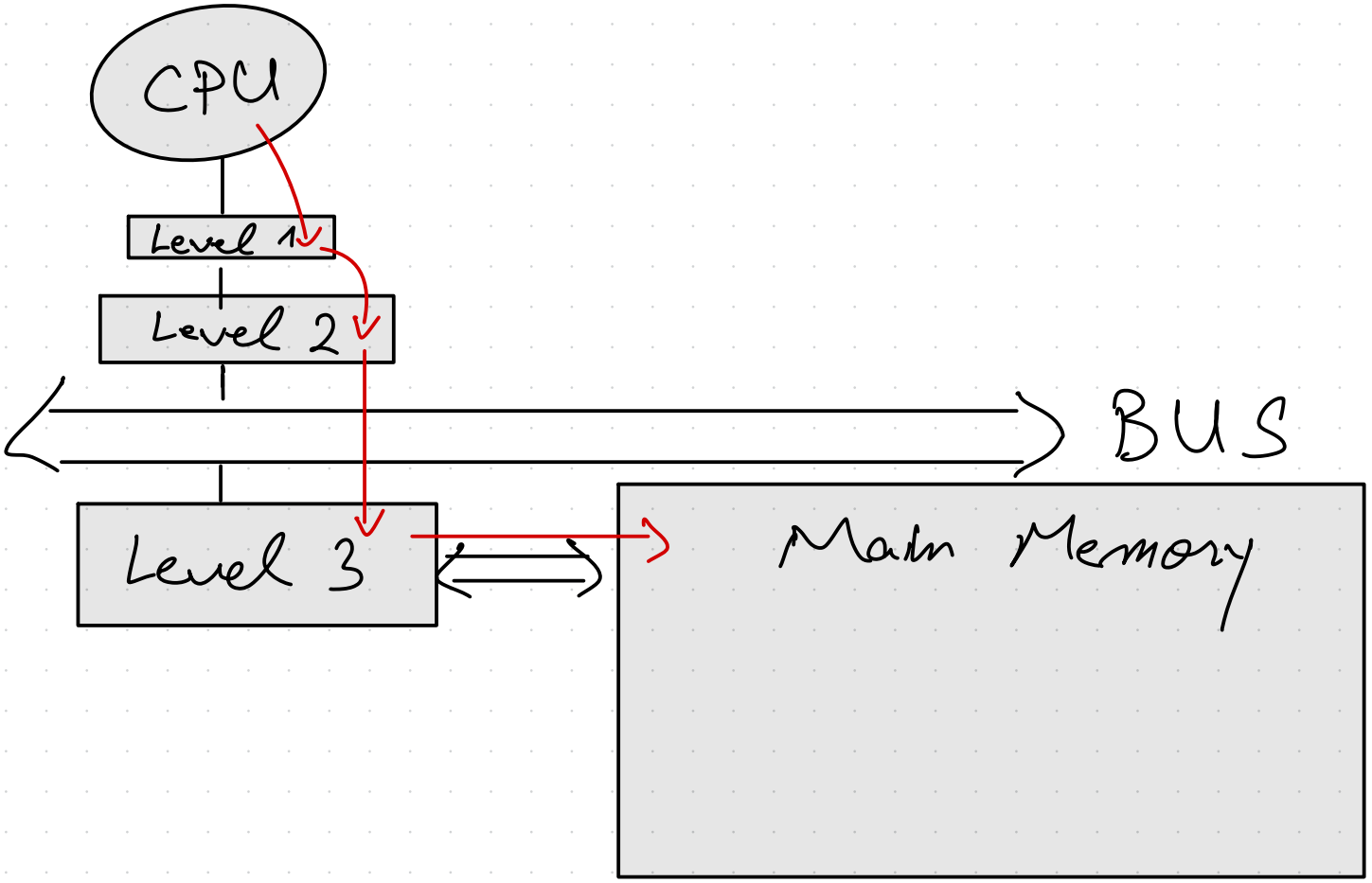
AMAT = 2,434 ns

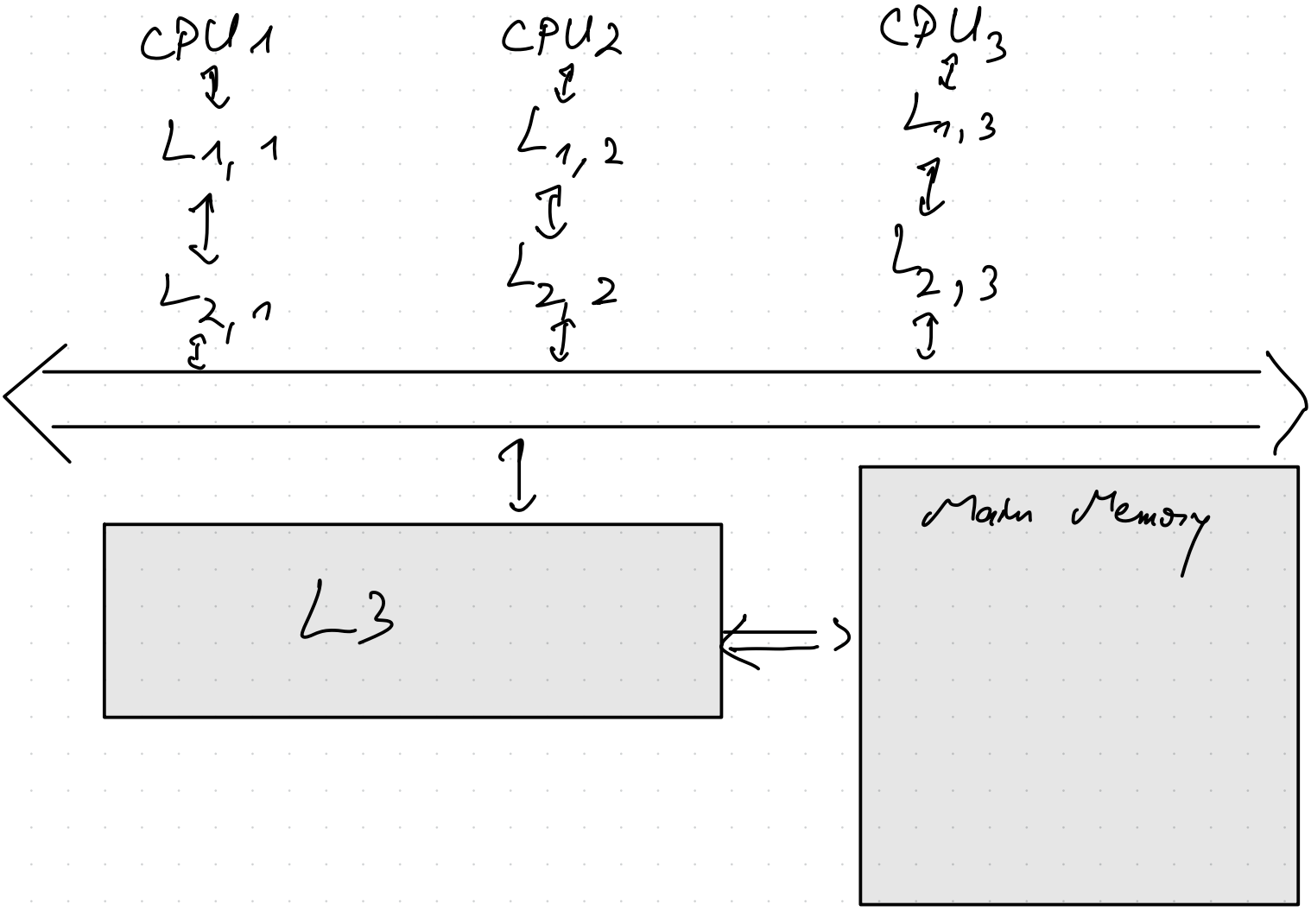
CPI Ideal = 3

$$CPU_{time} = \underbrace{1000}_{IC} \times \left(\underbrace{3}_{CPI_{ideal}\ cc} + \underbrace{0.1}_{Miss/Instr} \times \underbrace{76}_{Miss\ Pen\ cc}\right) \times \underbrace{0.333\ ns}_{CCT}$$

$= 3529.8\ ns = 3.5298\ \mu s$

3.5 Multi-level caches





Example 2

CPI ideal 1 CC

Clk Rate = 4 GHz

Miss Pen. = 100 ns

Miss Rate / Insts = 2% = Mem Acc / Inst × Msg Rate

tac_2 = 5 ns (read / write)

Miss rate / Inst 2 = 0.5%

$$CPU_{time\ 1\text{-}level} = IC \left(1 + 0.02 \times \left\lceil \frac{100\,ns}{0.25\,ns} \right\rceil\right) \times 0.25\,ns$$

(Miss Pen)

$$= IC \times 2.25\,ns$$

$$CPU_{time\ 2\text{-}level} = IC \left(1 + 0.005 \times \left\lceil \frac{100\,ns}{0.25\,ns} \right\rceil + 0.02 \times \left\lceil \frac{5\,ns}{0.25\,ns} \right\rceil\right) \times 0.25\,ns$$

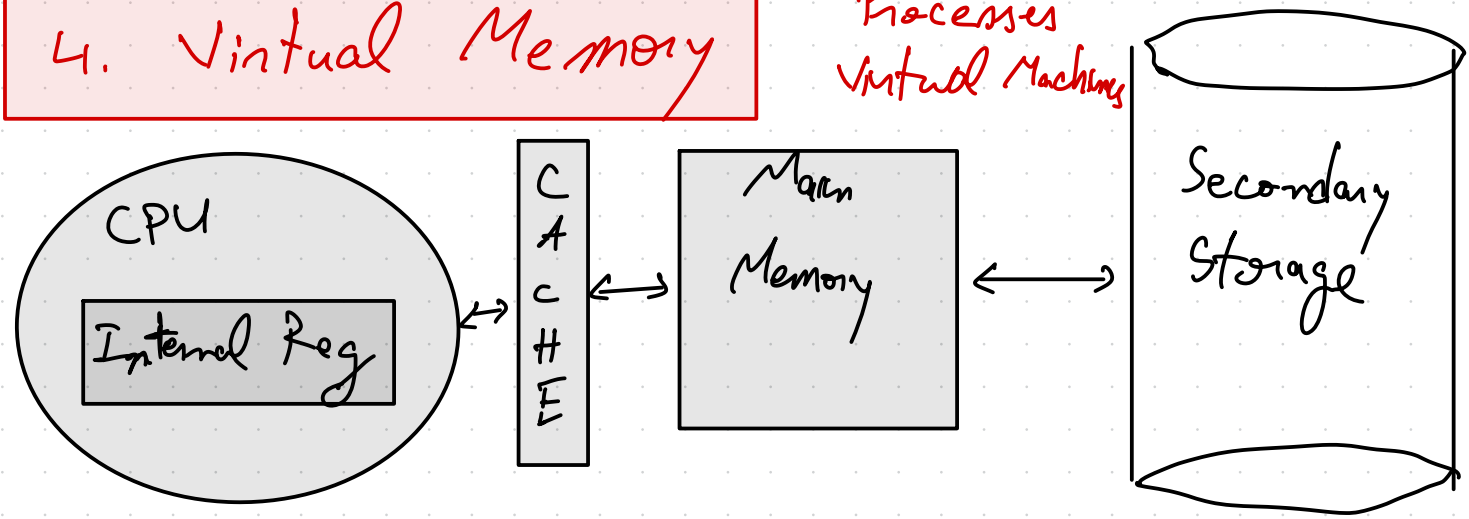
(Miss Pen; tac_2)

$$IC \left(3.4 \times 0.25\,ns\right)$$

$$\frac{\text{Perf level 1}}{2} = \underline{\underline{2.647}}$$

4. Virtual Memory

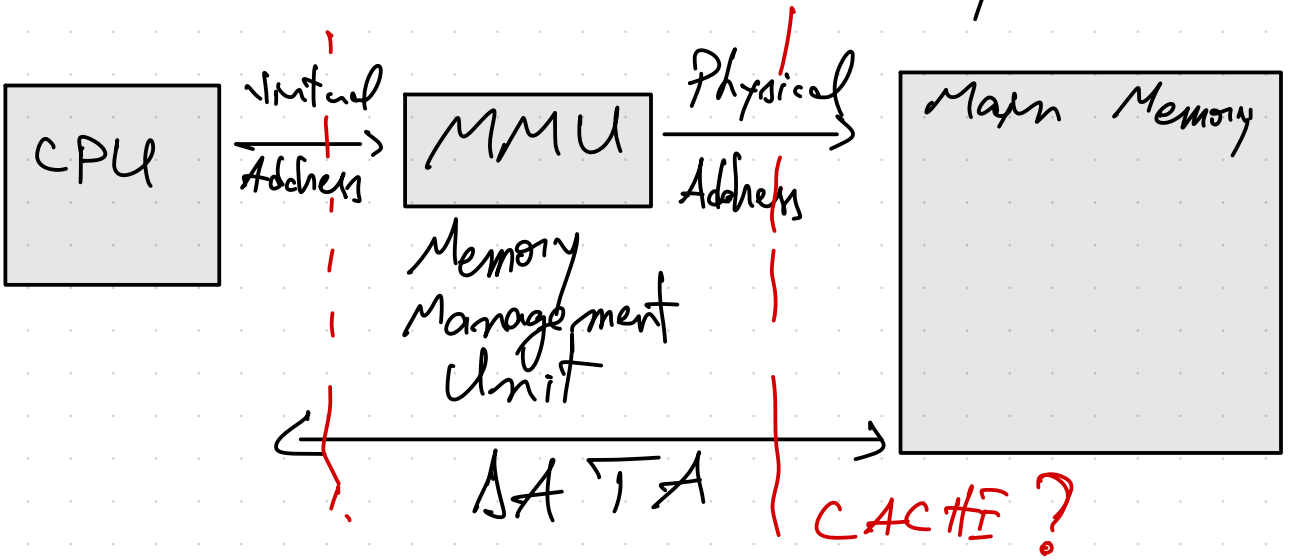
Processes
Virtual Machines



4.1. Motivation

Virtual Memory Space ≥ Physical Mem. Space
(Main Mem.)

Translation
Virtual Address ⟶ Physical Address.

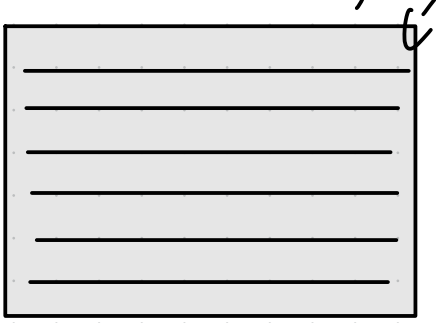


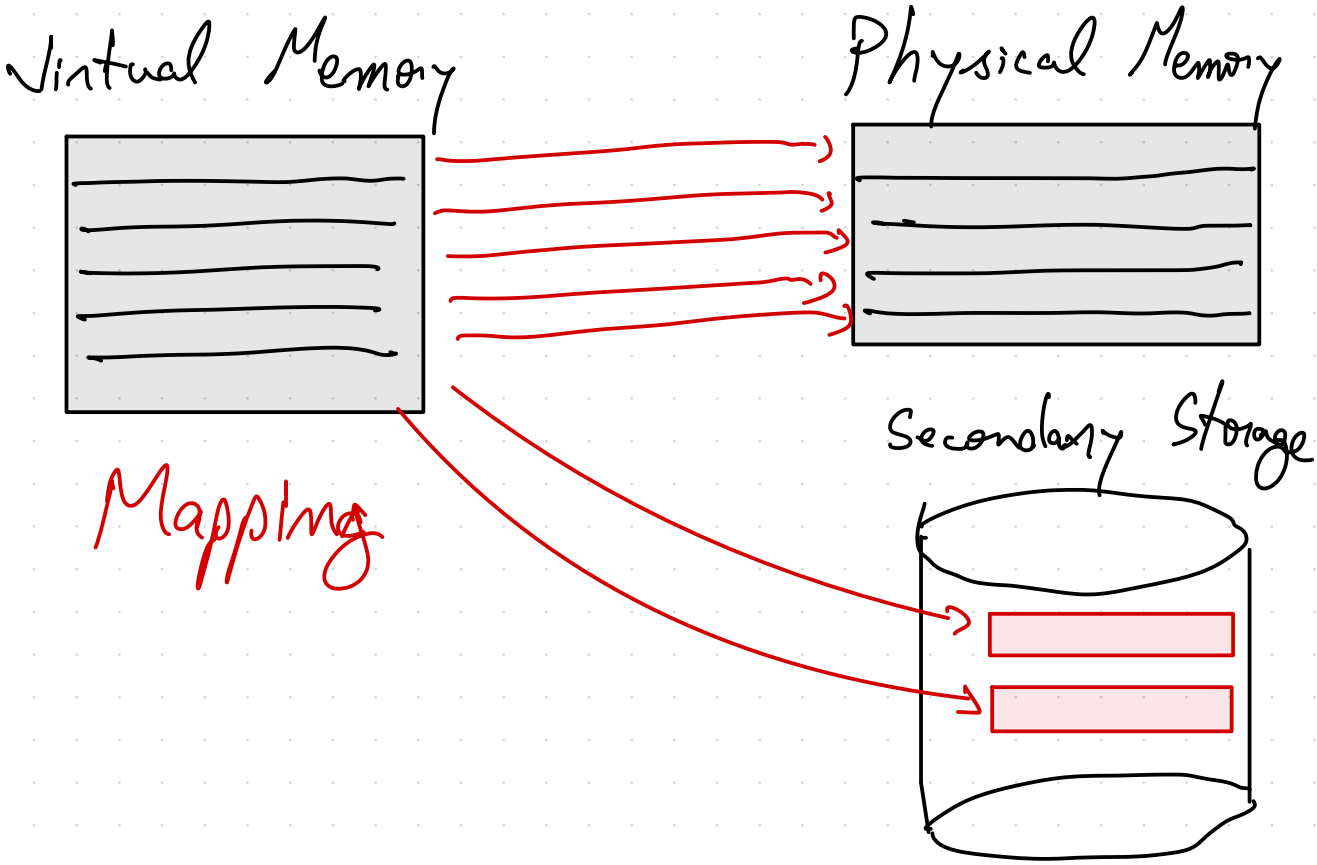
- page (chunk)
- segment

- page → fixed size
- seg. → variable number of pages

"FCSB, Faci Ce Spune Becali"

4.2. Address Translation





Huge Miss Penalty -> page fault

-> need for very low miss rate -> full-associative

-> table -> Page Table

-> fiecare proces are pagina sa

-> write through is out of the question

-> write back

-> Replacement -> software -> teaba SO

Address Mapping -> ARM v 8

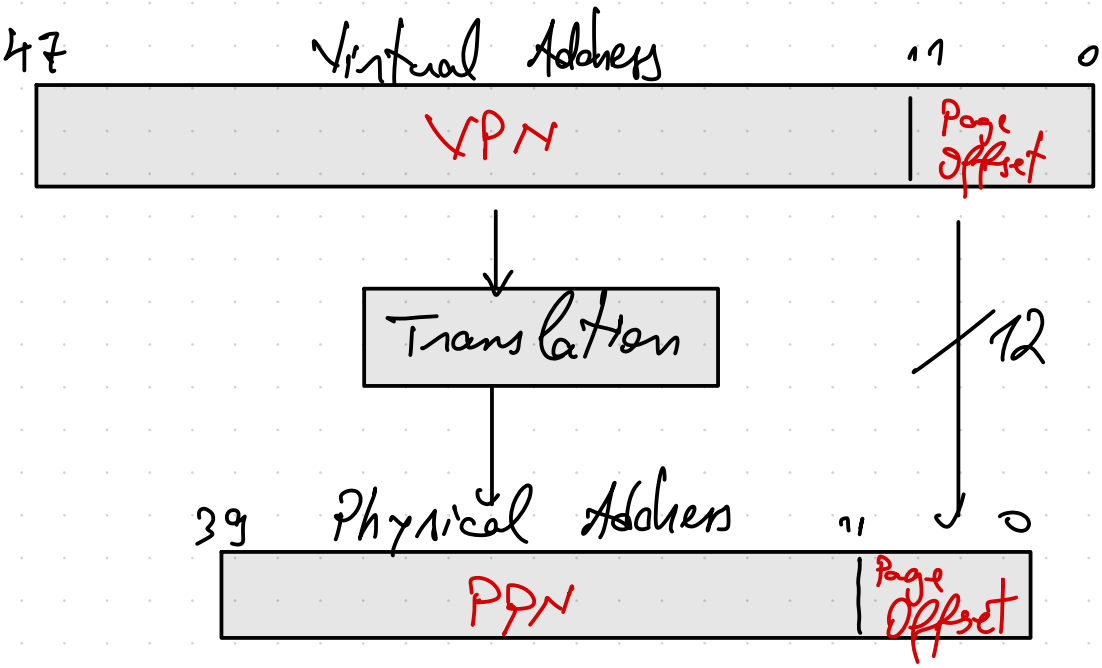
64 bit words

48 bit address

2^{48} bytes $= 2^8 \times 2^{40}$ B $= 2^8$ TiB 256 TiB

2^{40} B = 1 TiB -> Real Address

Page Number



Page Size $= 2^{12}$ B = 4 KiB