

## 1.2 Accelerating multiplication

### 1.2.1 Multiplier performance

Ex.1  $X = 100111010$   
 $X' = \overline{10100111}$

Robertsom  $\rightarrow 5$  OP.

Booth  $\rightarrow 5$  OP.

Ex.2  $X = 11100110$   
 $X' = 00\overline{10101}$

Robertsom  $\rightarrow 5$  OP.

Booth  $\rightarrow 3$  OP.

Ex.3

$X = 010101010$   
 $X' = 1\overline{1111111}$

Robertsom  $\rightarrow 4$  OP.

Booth  $\rightarrow 8$  OP.

Booth encoding

$x_i$	$x_{i-1}$	OP
0	0	0
0	1	1
1	0	$\overline{1}$
1	1	0

### 1.2.2 Modified Booth

- Run of 0s, run of 1s

isolated 0  
isolated 1

$-2^i \cdot y + 2^{i+1} \cdot y = (-1+2) \cdot 2^i \cdot y = 2^i \cdot y$   
 $+2^i \cdot y - 2^{i+1} \cdot y = (1-2) \cdot 2^i \cdot y = -2^i \cdot y$

$x_{i+1}$	$x_i$	R	OP	$R^*$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	$\overline{1}$	1
1	1	0	$\overline{1}$	1
1	1	1	0	1

Ex.1'

$X = 110011101$   
 $X' = \overline{10100101}$   
 $R = 100111000$

MBooth  $\rightarrow 4$  OP

Ex.2'

$X = 1110011$   
 $X' = 00\overline{10101}$   
 $R = 11100110$

MBooth  $\rightarrow 3$  OP

Ex.3'

$X = 101010101$   
 $X' = 01010101$   
 $R = 000000000$

MBooth  $\rightarrow 4$  OP

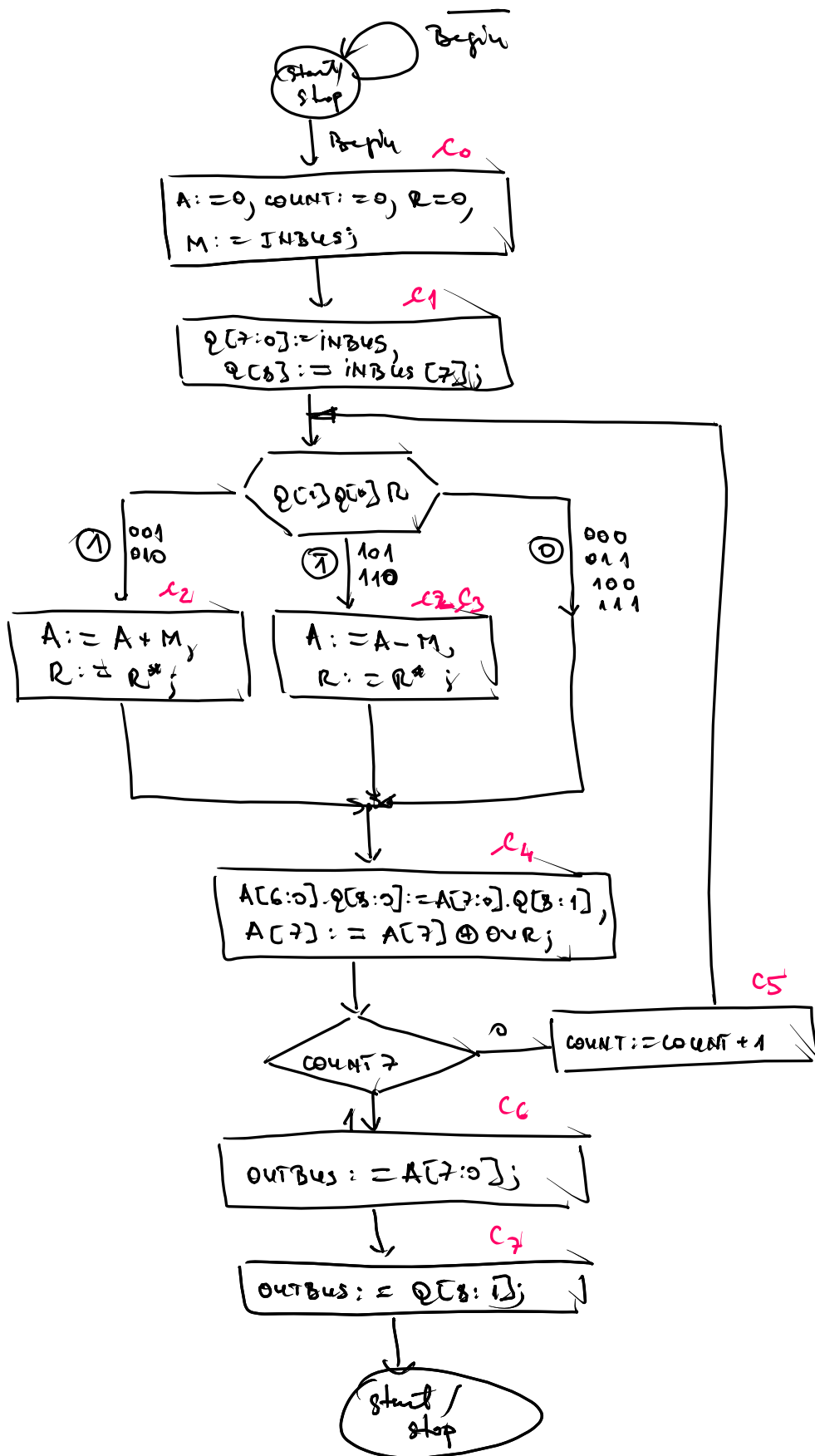
$R^* x_{i+1} x_i$

	00	01	11	10
0	0	0	1	0
1	0	1	1	1

~ ~ ~

$R^* = x_{i+1} \cdot x_i + R \cdot x_i + R \cdot x_{i+1}$

The diagram illustrates a 32-bit parallel adder system. At the top, a 32-bit register 'A' is shown with its output split into two 16-bit segments. The right 16-bit segment is fed into a '3-bit Parallel Adder' block, which also receives an 8-bit carry input 'C<sub>3</sub>'. The adder's output is a 16-bit signal 'Q[15:1]', which is then extended to a 32-bit output bus. A 'Control Unit' block at the bottom receives 'Begin', 'Clock', 'Reset', and 'End' signals. It outputs 'COUNT' and 'COUNT2' signals to a counter and a multiplexer. The counter's output is connected to the 'C<sub>3</sub>' input of the parallel adder. The multiplexer selects between the 'COUNT' signal and the output of the parallel adder to produce the final 32-bit output. The diagram also shows a '3-bit Data Bus' and a '3-bit Data Bus' at the bottom left.



# 1.3 Speeding multiplication with the higher radix

Radix-4

↓

$x_{i+1}$	$x_i$	$x_{i-1}$	OP
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	2
1	0	0	$\bar{2}$
1	0	1	$\bar{1}$
1	1	0	$\bar{1}$
1	1	1	0

$$\rightarrow y \cdot 2^i + 0 = \underline{y \cdot 2^i}$$

$$\rightarrow -y \cdot 2^i + y \cdot 2^{i+1} = y \cdot 2^i$$

$$\rightarrow 0 + y \cdot 2^{i+1} = +2y \cdot 2^i$$

$$\begin{aligned} 1 &\rightarrow +y \\ \bar{1} &\rightarrow -y \\ 2 &\rightarrow +2y \\ \bar{2} &\rightarrow -2y \end{aligned}$$

0 1 0 1 0 1 0 1 0 1 0

$\Rightarrow$  1 1 1 1

4 iterations