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Collegio di Elettronica, Telecomunicazioni e Fisica

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Integrated Systems Architecture

Lab 2: Digital Arithmetic

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Group: 18

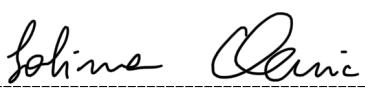
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CHAPTER 1

Digital arithmetic and logic synthesis

1.1 FPU model

1.1.1 Simulation

The FPU has been stimulated with the following operands a and b ; in Table 1.1 is reported the hexadecimal configuration of these numbers.

	a	b		r		
	15	0x4B80	204	0x5A60	3060	0x69FA
	1024	0x6400	204	0x5A60	+∞ (OF=1)	0x7C00
	1024	0x6400	-15	0xCB80	-15360	0xF380
	-15	0xCB80	-204	0xDA60	3060	0x69FA
	-204	0xDA60	1.75	0x3F00	-357	0xDD94
	-1024	0xE400	15	0x4B80	-15360	0xF380
	-30.5	0xCFA0	-7.5	0xC780	228.8	0x5B26
	7.5	0x4780	123	0x57B0	922.5	0x6335
	30.5	0x4FA0	-1.75	0xBF00	-53.4	0xD2AC
	-123	0xD7B0	1.75	0x3F00	-215.3	0xDABA

Table 1.1: Summary of operands and results of multiplications

Figure 1.1 shows a snapshot of the simulation: as it can be observed, stimulating the FPU with the numbers shown in Table 1.1 the results are the expected ones.

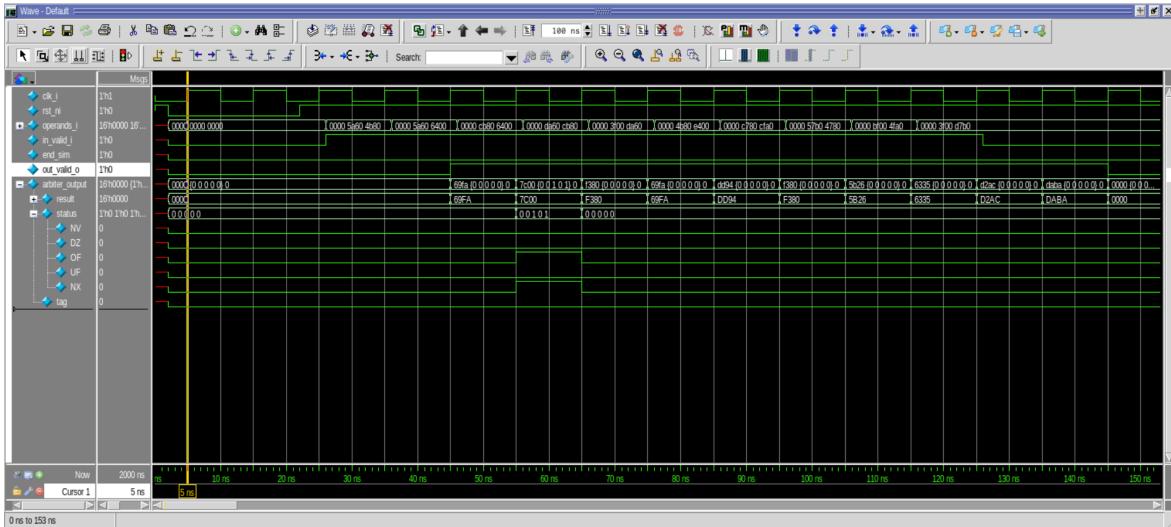


Figure 1.1: Simulation of FPU

1.2 Synthesis strategies

The aim of this section is to compare the results of the synthesis issuing different compile commands and using different implementations.

1.2.1 Synthesis with *compile* command

Table 1.2 shows the maximum frequency achieved and the area occupied. Further details on the reports are listed in appendix 3.1.1.

Clock period	Frequency	Area
3.22 ns	311 MHz	3294.7 μm^2

Table 1.2: Clock period, frequency and area of the architecture synthesized with *compile* command

Figure 1.2 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in table 1.1.

1.2.2 Synthesis issueing *compile* command and then *optimize_registers* command

Table 1.3 shows the maximum frequency achieved and the area occupied. Further details on the reports can be found in appendix 3.1.2.

Clock period	Frequency	Area
2.16 ns	463 MHz	4128.3 μm^2

Table 1.3: Clock period, frequency and area of the architecture synthesized with *compile* command before issueing *optimize_registers* command

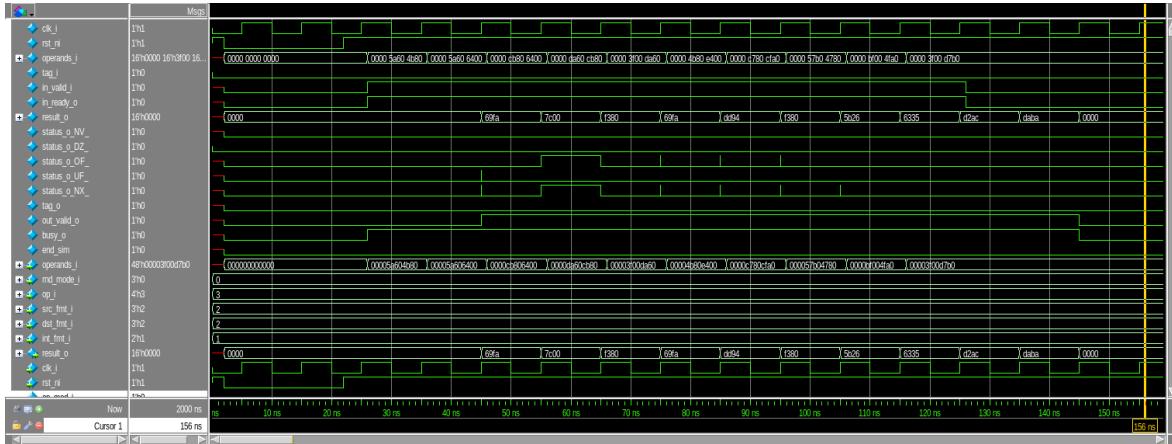


Figure 1.2: Waveform of the architecture synthesized with *compile* command

Figure 1.3 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in table 1.1.

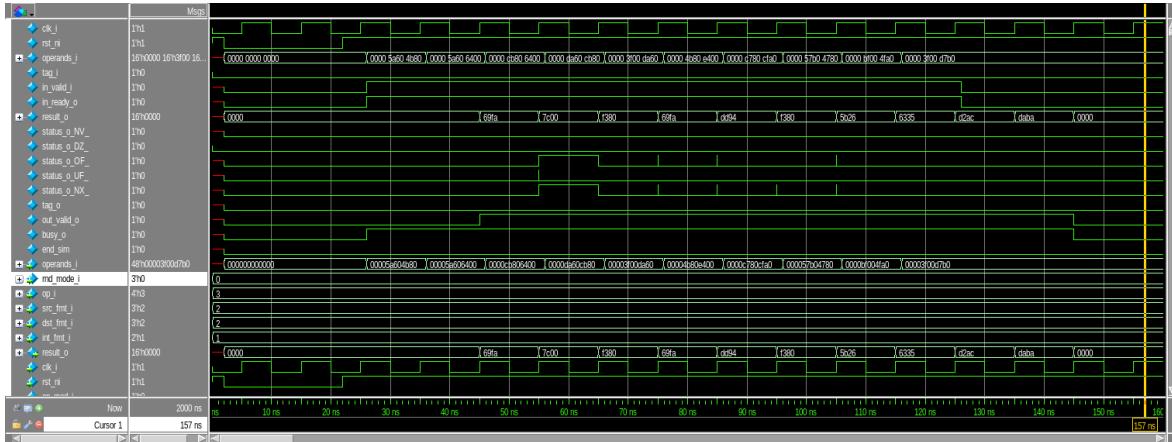


Figure 1.3: Waveform of the architecture synthesized with *compile* command before issuing *optimize_registers* command

1.2.3 Synthesis with *compile_ultra*

Table 1.4 shows the maximum frequency achieved and the area occupied. Further details on the reports can be found in appendix 3.1.3.

Clock period	Frequency	Area
2.43 ns	412 MHz	3861.0 μm^2

Table 1.4: Clock period, frequency and area of the architecture synthesized with *compile_ultra* command

Figure 1.4 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in Table 1.1.

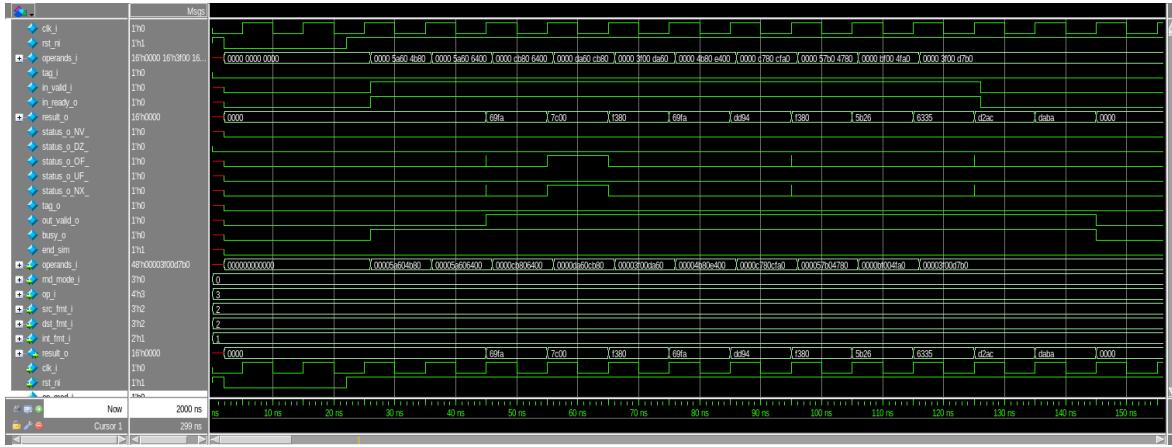


Figure 1.4: Waveform of the architecture synthesized with *compile_ultra* command

1.2.4 Synthesis with *compile* command and CSA architecture

- Before *optimize_registers* command

Table 1.5 shows the maximum frequency achieved and the area occupied. Further details on the reports can be found in appendix 3.1.4, including the *report_resources* which shows that the chosen implementation has been applied.

Clock period	Frequency	Area
2.75 ns	364 MHz	3556.2 μm^2

Table 1.5: Clock period, frequency and area of the architecture synthesized with *compile* command and CSA architecture before *optimize_registers* command

Figure 1.5 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in table 1.1.

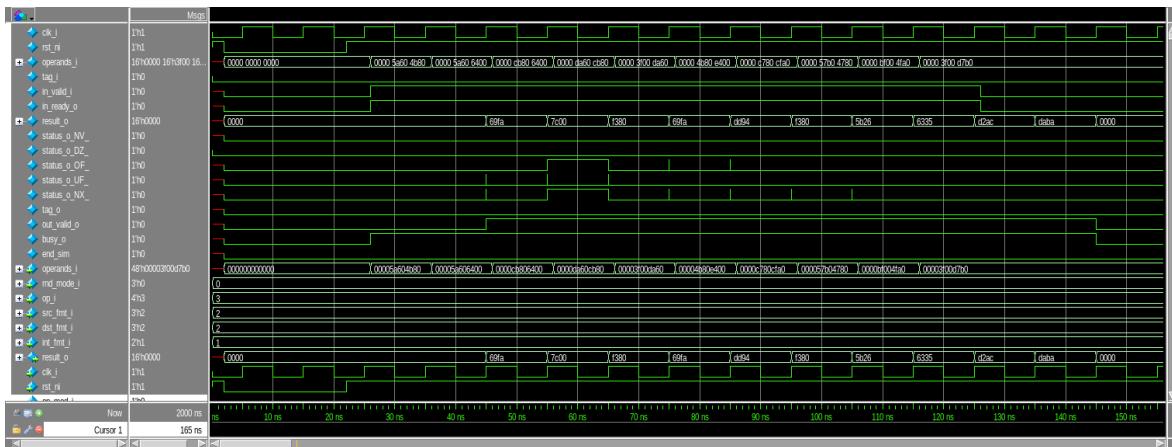


Figure 1.5: Waveform of the architecture synthesized with *compile* command and CSA architecture before *optimize_registers* command

- After *optimize_registers* command

Table 1.6 shows the maximum frequency achieved and the area occupied. Further details on the reports can be found in appendix 3.1.5, including the *report_resources* which shows that the chosen implementation has been applied.

Clock period	Frequency	Area
2.25 ns	444 MHz	4152.3 μm^2

Table 1.6: Clock period, frequency and area of the architecture synthesized with *compile* command and CSA architecture after *optimize_registers* command

Figure 1.6 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in table 1.1.

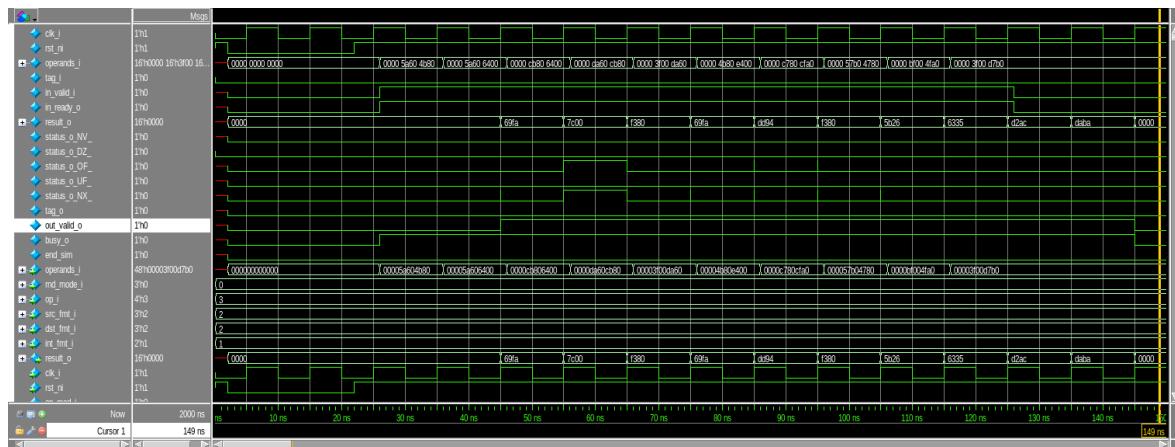


Figure 1.6: Waveform of the architecture synthesized with *compile* command and CSA architecture after *optimize_registers* command

1.2.5 Synthesis with *compile* command and PPARCH architecture

- Before *optimize_registers* command

Table 1.7 shows the maximum frequency achieved and the area occupied. Further details on the reports can be found in appendix 3.1.6, including the *report_resources* which shows that the chosen implementation has been applied.

Clock period	Frequency	Area
2.95 ns	340 MHz	3450.0 μm^2

Table 1.7: Clock period, frequency and area of the architecture synthesized with *compile* command and PPARCH architecture before *optimize_registers* command

Figure 1.7 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in table 1.1.

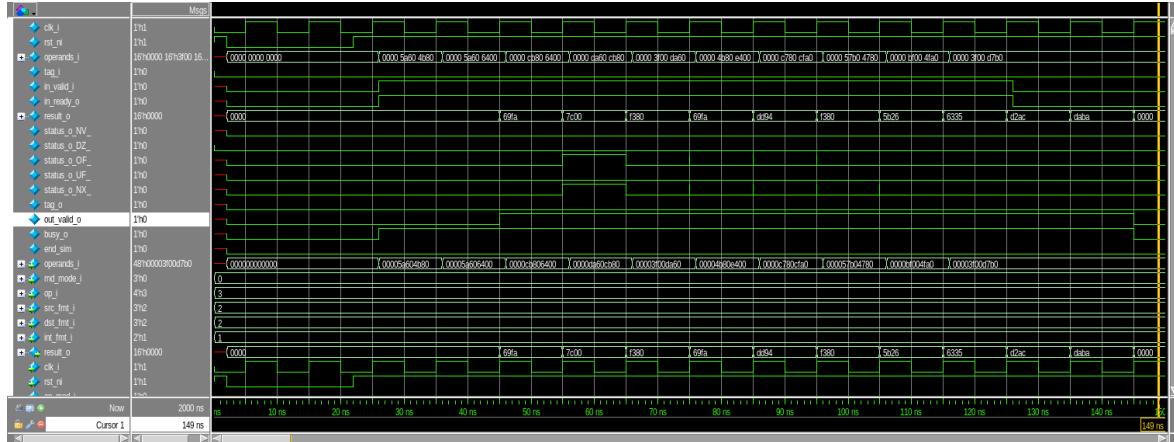


Figure 1.7: Waveform of the architecture synthesized with *compile* command and PPARCH architecture before *optimize_registers* command

- After *optimize_registers* command

Table 1.8 shows the maximum frequency achieved and the area occupied. Further details on the reports can be found in appendix 3.1.7, including the *report_resources* which shows that the chosen implementation has been applied.

Clock period	Frequency	Area
2.16 ns	463 MHz	$4166.6 \mu\text{m}^2$

Table 1.8: Clock period, frequency and area of the architecture synthesized with *compile* command and PPARCH architecture after *optimize_registers* command

Figure 1.8 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in table 1.1.

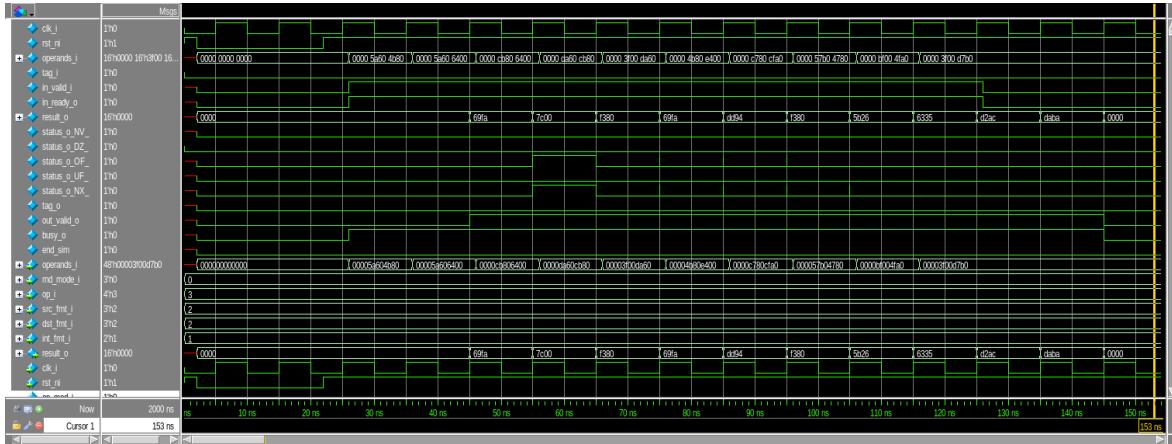


Figure 1.8: Waveform of the architecture synthesized with *compile* command and PPARCH architecture after *optimize_registers* command

1.3 Explanations, comparisons and comments

Table 1.9 shows a summary of the results of all the synthesis performed.

Type of commands issued	Clock period	Frequency	Area
compile	3.22 ns	311 MHz	$3294.7 \mu\text{m}^2$
compile + optimize_registers	2.16 ns	463 MHz	$4166.6 \mu\text{m}^2$
compile_ultra	2.43 ns	412 MHz	$3861.0 \mu\text{m}^2$
compile + CSA arch	2.75 ns	364 MHz	$3556.2 \mu\text{m}^2$
compile + CSA arch + optimize_registers	2.25 ns	444 MHz	$4152.3 \mu\text{m}^2$
compile + PPARCH	2.95 ns	340 MHz	$3450.0 \mu\text{m}^2$
compile + PPARCH + optimize_registers	2.16 ns	463 MHz	$4166.6 \mu\text{m}^2$

Table 1.9: Summary table

The commands used in order to synthesize the different architectures are:

- **compile** which performs synthesis and optimization on the current design;
- **compile_ultra** which is similar to the *compile* command but has tighter constraints for the optimization phase in order to accomplish better quality of results;
- **optimize_registers** which performs retiming of sequential cells, determines the placement of sequential cells in a design to achieve a target clock period and minimizes the number of sequential cells while maintaining that clock period;
- **set_implementation** which allows to use a specified implementation for a cell instance otherwise compile chooses the implementation it considers most appropriate.

The fastest architectures have been synthesized with the commands *optimize_registers* after *compile* and *compile* choosing to use a parallel-prefix implementation and then issuing *optimize_registers*; they occupy the same area.

The worst solution is obtained issuing only *compile*, in fact the frequency is the minimum above all architectures. With *compile_ultra* the area increases by 15.4% with respect to the previous solution and the frequency reached is higher. Without performing the retiming (not issuing *optimize_registers* command), the

CSA implementation of the multiplier allows to reach a better performance in terms of speed compared to the parallel-prefix solution. This happens because with CSA implementation, the number of stages used are lower compared to the amount needed by the parallel prefix one. In the second case, in fact, 4 stages are needed to complete a single addition while in the first case, with 6 stages the multiplication is computed. Applying the *optimization_registers* command, the synthesis with the parallel-prefix architecture has a frequency slightly higher while the area represents the maximum above all architectures analyzed, however the difference between the two is small.

CHAPTER 2

R4-MBE multiplier implementation

In this chapter is described the implementation of a Radix-4 Modified Booth Encoder (R4-MBE) multiplier for unsigned data, designed in **SystemVerilog**. Once it is designed, the component is simulated and it is used as the mantissa multiplier in the floating point unit *fpnew_fma.sv*.

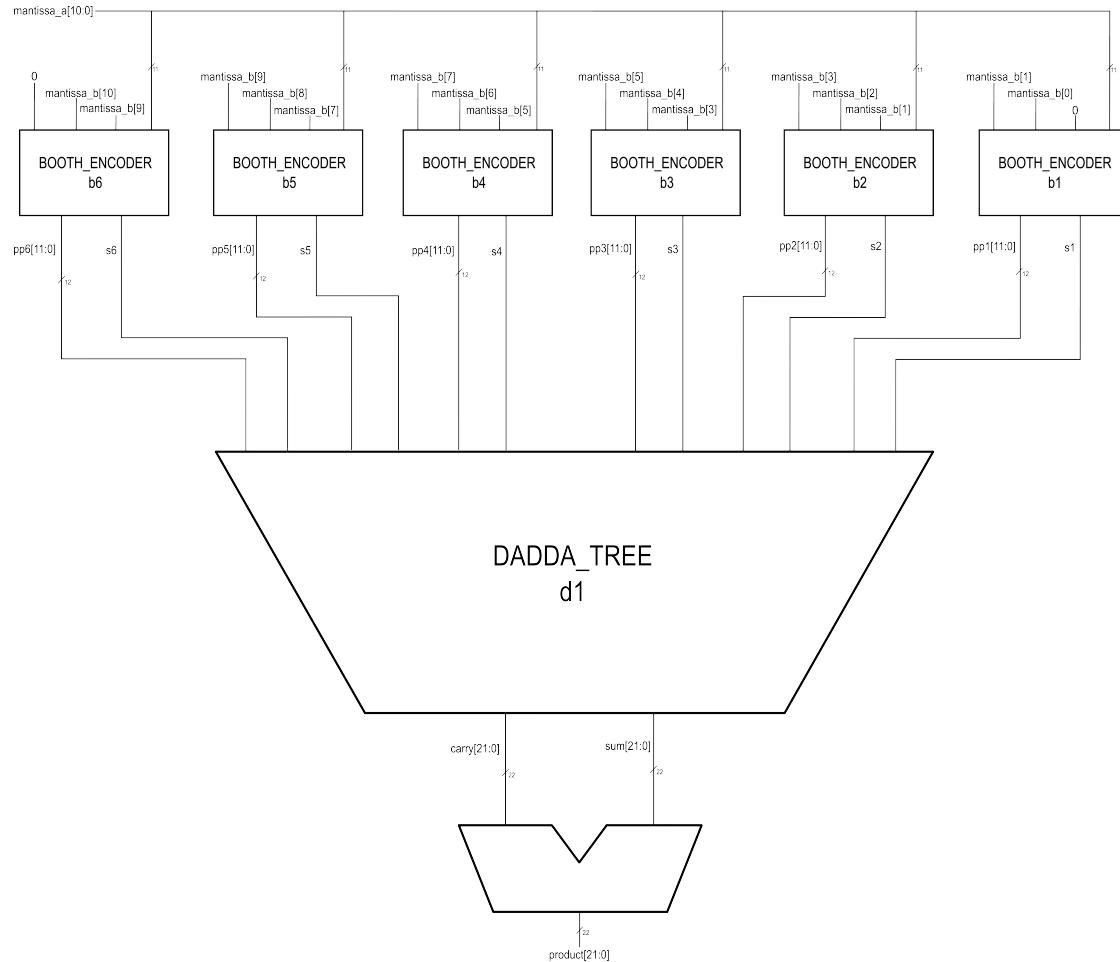


Figure 2.1: R4-MBE multiplier architecture

2.1 Architecture

The R4-MBE architecture is depicted in Figure 2.1.

The architecture is fully combinatorial (this constraint is necessary to be able to include the component as the mantissa multiplier) and, according to the assignment, the modified booth encoding is applied and the Dadda-tree is implemented, simplifying sign extension bits. In Appendix 3.2.3 is reported the SystemVerilog file.

2.1.1 Booth Encoder

The Booth Encoder module is depicted in Figure 2.2.

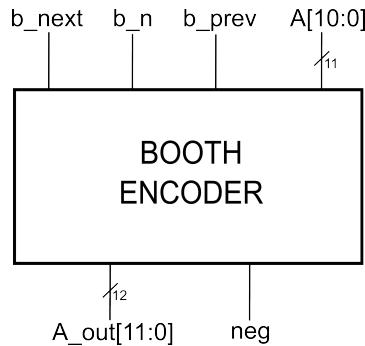


Figure 2.2: Radix-4 Booth Encoder

Since the radix is 4, three consecutive bits are taken, following the encoding technique in Table 2.1; the partial product value is selected in the set $\{0, \pm A, \pm 2A\}$. Absolute value of partial product (A_{out}) and sign bit (neg) are the outputs of this module; in the multiplier architecture the data length is eleven bits, and so six booth encoder modules are placed taking as input 3-bits vector overlapped, as shown in Figure 2.1. Booth encoder description file is reported in Appendix 3.2.1.

b_next	b_n	b_prev	partial product	A_out	neg
0	0	0	0	0	0
0	0	1	A	A	0
0	1	0	A	A	0
0	1	1	2A	2A	0
1	0	0	-2A	2A	1
1	0	1	-A	A	1
1	1	0	-A	A	1
1	1	1	0	0	0

Table 2.1: Radix-4 Booth encoding

The six partial products with the respective sign bits are then summed in a tree of Carry Save Adders, implemented as a Dadda tree.

2.1.2 Dadda tree

Dadda-like tree scheme for 6-operands input with sign extension optimization is shown in Figure 2.3. Starting from six operands, three levels of half and full adders (represented in Figure 2.3 in red and in blue respectively) are necessary to reduce the number to two operands (in carry and sum form), that can be summed together in a final adder taking into account the correct alignment. Sign extension bits are optimized in order to reduce the number of adders, according to the assignment.

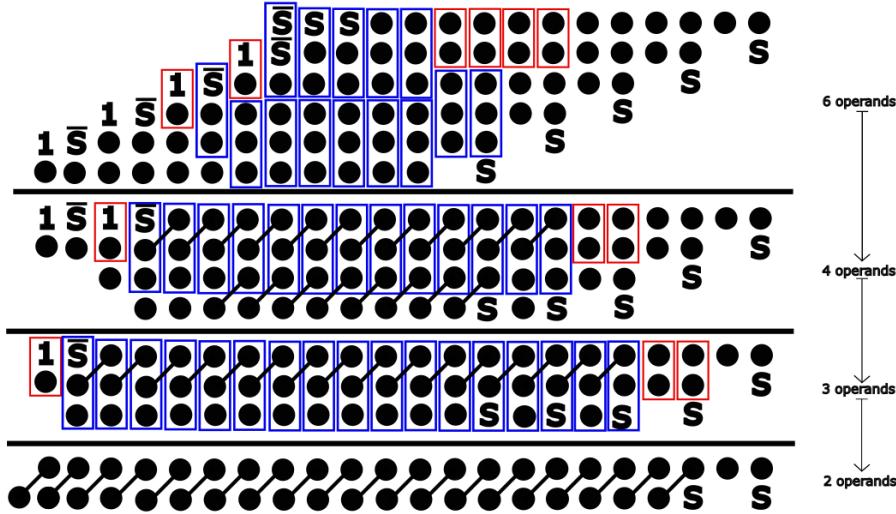


Figure 2.3: Dadda tree scheme

In Figure 2.4 is shown the implementation of this architecture. Since the parallelism of product is 22 bits (11 bits + 11 bits), the same parallelism is used for carry and sum vectors; for this reason the carry bit of 12th half adder is not considered. According to the scheme in Figure 2.3, the alignment of carry and sum is showed in the bottom part of Figure 2.4. In Appendix 3.2.2 is reported the description file.

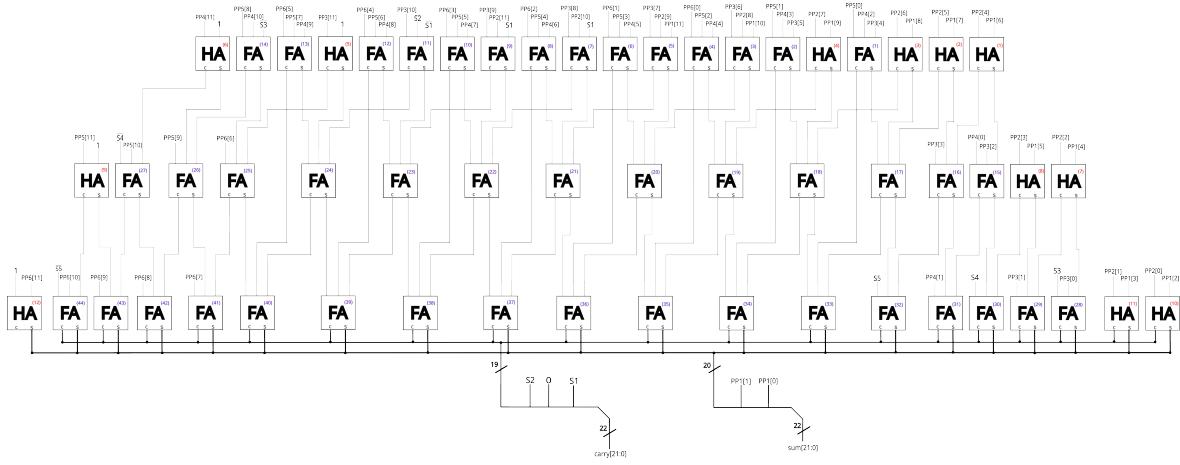


Figure 2.4: Dadda tree implementation

2.2 Simulation

2.2.1 Stand-alone simulation

The multiplier is simulated as a stand-alone component, testing it using random input operands; it works as expected and results are shown below in Figure 2.5 and Figure 2.6.

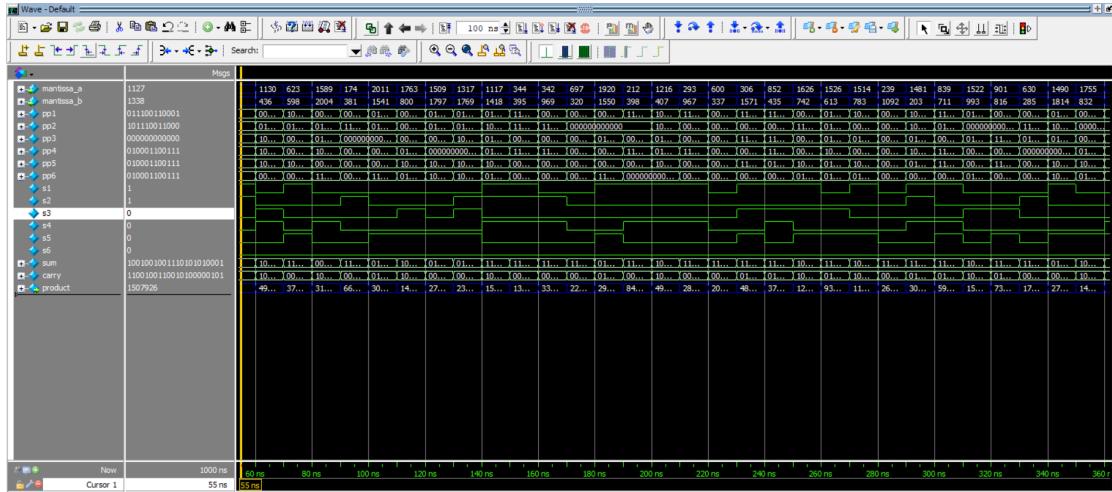


Figure 2.5: Resulting waveforms of stand-alone multiplier simulation

```
Transcript
# Time=100 : RIGHT RESULT! mantissa_a=2011 mantissa_b=1941 product=3090591 expected_product=3090591
# Time=110 : RIGHT RESULT! mantissa_a=1763 mantissa_b= 800 product=1410400 expected_product=1410400
# Time=120 : RIGHT RESULT! mantissa_a=1509 mantissa_b=1797 product=2711673 expected_product=2711673
# Time=130 : RIGHT RESULT! mantissa_a=1317 mantissa_b=1769 product=3229773 expected_product=3229773
# Time=140 : RIGHT RESULT! mantissa_a=1117 mantissa_b=1418 product=1583904 expected_product=1583904
# Time=150 : RIGHT RESULT! mantissa_a= 344 mantissa_b= 395 product= 135880 expected_product= 135880
# Time=160 : RIGHT RESULT! mantissa_a= 342 mantissa_b= 969 product= 331398 expected_product= 331398
# Time=170 : RIGHT RESULT! mantissa_a= 697 mantissa_b= 320 product= 223040 expected_product= 223040
# Time=180 : RIGHT RESULT! mantissa_a=1920 mantissa_b=1550 product=2976000 expected_product=2976000
# Time=190 : RIGHT RESULT! mantissa_a=212 mantissa_b= 398 product= 84376 expected_product= 84376
# Time=200 : RIGHT RESULT! mantissa_a=1216 mantissa_b= 407 product= 494912 expected_product= 494912
# Time=210 : RIGHT RESULT! mantissa_a= 293 mantissa_b= 967 product= 283331 expected_product= 283331
# Time=220 : RIGHT RESULT! mantissa_a= 600 mantissa_b= 337 product= 202200 expected_product= 202200
# Time=230 : RIGHT RESULT! mantissa_a= 306 mantissa_b=1571 product= 480726 expected_product= 480726
# Time=240 : RIGHT RESULT! mantissa_a= 852 mantissa_b= 435 product= 370620 expected_product= 370620
# Time=250 : RIGHT RESULT! mantissa_a=1626 mantissa_b= 742 product=1206492 expected_product=1206492
# Time=260 : RIGHT RESULT! mantissa_a=1526 mantissa_b= 613 product= 935438 expected_product= 935438
# Time=270 : RIGHT RESULT! mantissa_a=1514 mantissa_b= 783 product=1185462 expected_product=1185462
# Time=280 : RIGHT RESULT! mantissa_a= 239 mantissa_b=1092 product= 260988 expected_product= 260988
# Time=290 : RIGHT RESULT! mantissa_a=1491 mantissa_b= 203 product= 300643 expected_product= 300643
# Time=300 : RIGHT RESULT! mantissa_a= 839 mantissa_b= 711 product= 596529 expected_product= 596529
# Time=310 : RIGHT RESULT! mantissa_a=1522 mantissa_b= 993 product=1511346 expected_product=1511346
# Time=320 : RIGHT RESULT! mantissa_a= 901 mantissa_b= 816 product= 735216 expected_product= 735216
# Time=330 : RIGHT RESULT! mantissa_a= 630 mantissa_b= 285 product= 179550 expected_product= 179550
# Time=340 : RIGHT RESULT! mantissa_a=1490 mantissa_b=1814 product=2702860 expected_product=2702860
# Time=350 : RIGHT RESULT! mantissa_a=1755 mantissa_b= 832 product=1460160 expected_product=1460160
# Time=360 : RIGHT RESULT! mantissa_a= 693 mantissa_b= 657 product= 455301 expected_product= 455301
# Time=370 : RIGHT RESULT! mantissa_a=1907 mantissa_b= 160 product= 305120 expected_product= 305120
# Time=380 : RIGHT RESULT! mantissa_a=1367 mantissa_b=1053 product=1439451 expected_product=1439451
# Time=390 : RIGHT RESULT! mantissa_a= 980 mantissa_b=2013 product=1972740 expected_product=1972740
# Time=400 : RIGHT RESULT! mantissa_a= 410 mantissa_b= 132 product= 54120 expected_product= 54120
# Time=410 : RIGHT RESULT! mantissa_a= 951 mantissa_b=1161 product=1104111 expected_product=1104111
# Time=420 : RIGHT RESULT! mantissa_a= 266 mantissa_b= 725 product= 192850 expected_product= 192850
# Time=430 : RIGHT RESULT! mantissa_a=1278 mantissa_b=1612 product=2060136 expected_product=2060136
# Time=440 : RIGHT RESULT! mantissa_a=1534 mantissa_b= 707 product=1084538 expected_product=1084538
# Time=450 : RIGHT RFSULT! mantissa_a=1928 mantissa_b=1468 rrndnum=2330304 rrndrnd=2830304 rrndrndprod=2830304
```

Figure 2.6: Results of stand-alone multiplier simulation

2.2.2 FPU simulation

The multiplier is now integrated into the FPU, by replacing the previous command:

```
product = mantissa_a*mantissa_b
```

with our multiplier:

```
mbe_rad4_mult mantissa_multiplier(mantissa_a, mantissa_b, product)
```

The FPU is now simulated and the inputs are the same used in the simulation in Section 1.1.1. The results obtained, which are correct and coherent with the expectations, are shown below in Figure 2.7 and Table 2.2.

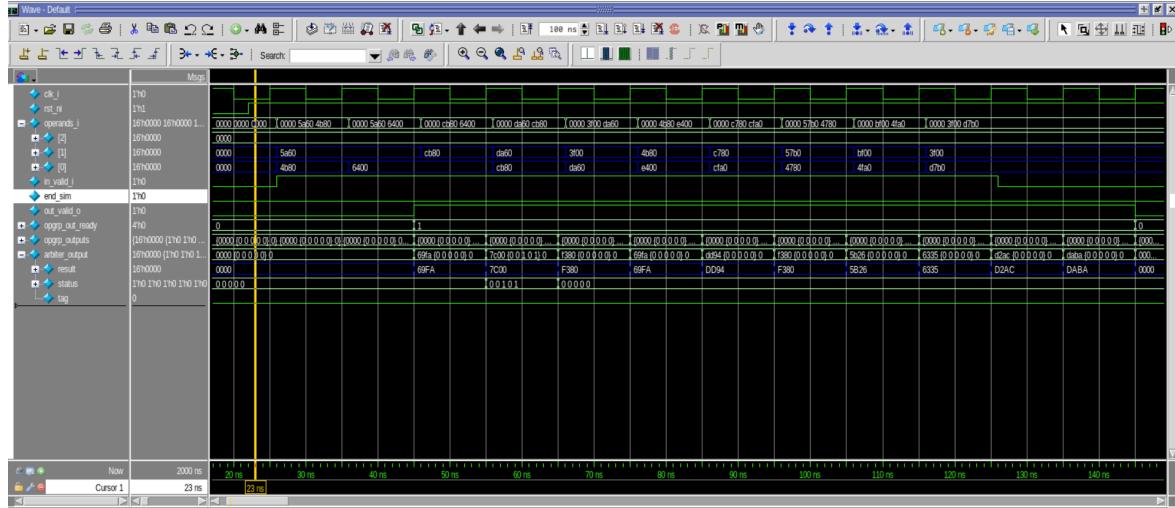


Figure 2.7: Results of FPU with integrated multiplier simulation

	<i>a</i>	<i>b</i>	<i>r</i>
15	0x4B80	204	0x5A60
1024	0x6400	204	0x5A60
1024	0x6400	-15	0xCB80
-15	0xCB80	-204	0xDA60
-204	0xDA60	1.75	0x3F00
-1024	0xE400	15	0x4B80
-30.5	0xCFA0	-7.5	0xC780
7.5	0x4780	123	0x57B0
30.5	0x4FA0	-1.75	0xBF00
-123	0xD7B0	1.75	0x3F00

Table 2.2: Summary of operands and results of multiplications

2.3 Synthesis

The floating point unit described in the file *fpnew.fma.sv* including the R4-MBE multiplier is synthesized with **compile_ultra** in order to find the maximum frequency and the area, which are summarized in Table 2.3.

Clock period	Frequency	Area
2.60 ns	385 MHz	$3795.6 \mu\text{m}^2$

Table 2.3: Clock period, frequency and area of FPU with R4-MBE multiplier synthesized with *compile_ultra* command

Figure 2.8 shows the results of the simulation obtained using the netlist generated from the synthesized architecture. The accuracy of the results can be evaluated comparing the values of line "result_o" in the waveform and the ones in table 2.2.

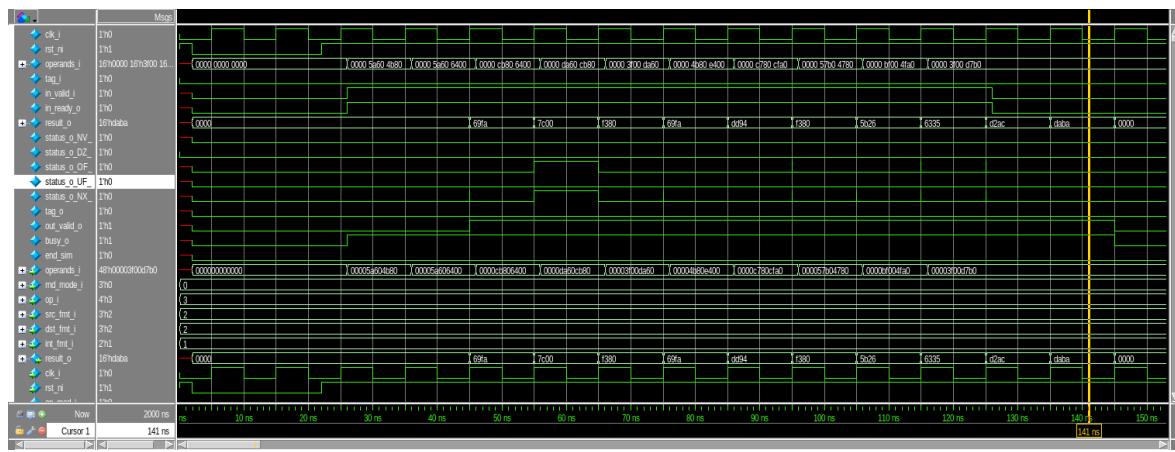


Figure 2.8: Waveform of FPU with R4-MBE multiplier synthesized with *compile_ultra* command

2.4 Explanations, comparisons and comments

It can be observed that the FPU works as expected and results obtained are equals to the correct values summarized in Table 2.2.

CHAPTER 3

Appendix

3.1 FPU synthesis reports

3.1.1 Reports of synthesis with *compile* command

REPORT AREA

```
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 11:28:38 2023
```

Librarys Used:

```
NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db
```

```
Number of ports:          469
Number of nets:           2837
Number of cells:          2299
Number of combinational cells: 2138
Number of sequential cells: 140
Number of macros/black boxes: 0
Number of buf/inv:         474
Number of references:     47

Combinational area:      2547.215996
Buf/Inv area:            282.492000
Noncombinational area:   747.460024
Macro/Black Box area:    0.000000
Net Interconnect area:   undefined Wire load has zero net area

Total cell area:          3294.676020
Total area:               undefined
1
```

REPORT TIMING

```
Information: Updating design information... UID-85
```

```

Report : timing
  -path full
  -delay max
  -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 11:28:38 2023

Operating Conditions: typical Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
             rising edge-triggered flip-flop clocked by MY_CLK
Endpoint: status_o[UF]
           output port clocked by MY_CLK
Path Group: MY_CLK
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----
fpnew_top          5K_hvratio_1_1       NangateOpenCellLibrary

Point                      Incr      Path
-----
clock MY_CLK rise edge        0.00      0.00
clock network delay ideal    0.00      0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.00      0.00 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.07      0.07 r
U857/ZN AND2_X1           0.04      0.11 r
U852/ZN AND3_X1           0.05      0.16 r
U851/ZN NAND2_X1          0.03      0.18 f
U1057/ZN NOR2_X1          0.04      0.23 r
U849/ZN AND4_X2           0.08      0.31 r
U823/ZN AND2_X1           0.05      0.36 r
U875/ZN NAND2_X1          0.02      0.39 f
U821/ZN OAI221_X1          0.07      0.46 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.00      0.46 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.03      0.49 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.04      0.53 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.04      0.57 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.03      0.60 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.04      0.65 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.04      0.68 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.04      0.73 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.04      0.76 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.05      0.82 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.03      0.84 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
                         0.04      0.89 r

```

```

sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.00      0.89 r
U1562/ZN NAND3_X1
          0.03      0.92 f
U1564/ZN OAI21_X1
          0.05      0.97 r
U1566/ZN NAND2_X1
          0.04      1.00 f
U866/ZN NAND2_X2
          0.05      1.05 r
U1641/ZN OAI222_X1
          0.07      1.12 f
U881/ZN INV_X1
          0.04      1.16 r
U1644/ZN NAND2_X1
          0.03      1.19 f
U862/ZN INV_X1
          0.06      1.25 r
U1680/ZN AOI22_X1
          0.05      1.29 f
U1681/ZN OAI221_X1
          0.04      1.34 r
U1682/ZN INV_X1
          0.04      1.38 f
U819/ZN OAI221_X1
          0.07      1.44 r
U1691/ZN INV_X1
          0.03      1.47 f
U790/ZN AOI221_X1
          0.09      1.56 r
U1050/ZN OAI211_X1
          0.05      1.60 f
U1700/ZN INV_X1
          0.04      1.64 r
U826/ZN AND2_X2
          0.06      1.70 r
U1748/ZN AOI22_X1
          0.04      1.74 f
U1749/ZN OAI21_X1
          0.04      1.78 r
U1750/ZN INV_X1
          0.02      1.80 f
U1751/ZN NOR4_X1
          0.09      1.89 r
U1064/ZN OAI221_X4
          0.09      1.98 f
U1897/ZN OAI211_X1
          0.04      2.03 r
U990/ZN OR2_X1
          0.04      2.07 r
U1941/ZN NAND2_X1
          0.02      2.09 f
U802/Z MUX2_X1
          0.07      2.16 f
U814/ZN NAND2_X1
          0.03      2.18 r
U884/ZN AND2_X1
          0.04      2.22 r
U782/ZN AND2_X2
          0.05      2.27 r
U832/ZN NAND2_X1
          0.04      2.32 f
U922/ZN NOR2_X1
          0.05      2.36 r
U921/ZN XNOR2_X1
          0.07      2.43 r
U1946/ZN NAND3_X1
          0.04      2.47 f
U914/ZN NOR2_X1
          0.04      2.51 r
U1948/ZN OAI21_X1
          0.03      2.54 f
U785/ZN NAND2_X1
          0.04      2.58 r
U772/ZN AND2_X1
          0.05      2.63 r
status_o[UF] out
          0.02      2.65 r
data arrival time
          2.65

clock MY_CLK rise edge
          3.22      3.22
clock network delay ideal
          0.00      3.22
clock uncertainty
          -0.07     3.15
output external delay
          -0.50     2.65
data required time
          2.65

-----
data required time
          2.65
data arrival time
          -2.65

-----
slack MET
          0.00

```

3.1.2 Reports of synthesis with *compile* command before *optimization_registers* command

REPORT AREA

```
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 12:47:02 2023
```

Librarys Used:

```
NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db
```

Number of ports:	461
Number of nets:	3268
Number of cells:	2791
Number of combinational cells:	2521
Number of sequential cells:	253
Number of macros/black boxes:	0
Number of buf/inv:	613
Number of references:	50
Combinational area:	2820.663992
Buf/Inv area:	365.484000
Noncombinational area:	1345.960043
Macro/Black Box area:	0.000000
Net Interconnect area:	undefined Wire load has zero net area
Total cell area:	4166.624035
Total area:	undefined
1	

REPORT TIMING

```
Information: Updating design information... UID=85
```

```
Report : timing
-path full
-delay max
-max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 12:47:02 2023
```

```
Operating Conditions: typical Library: NangateOpenCellLibrary
Wire Load Model Mode: top
```

```
Startpoint: MY_CLK_r_REG86_S1
    rising edge-triggered flip-flop clocked by MY_CLK
Endpoint: MY_CLK_r_REG13_S2
    rising edge-triggered flip-flop clocked by MY_CLK
Path Group: MY_CLK
Path Type: max
```

```
Des/Clust/Port      Wire Load Model      Library
-----
```

fpnew_top

5K_hvratio_1_1

NangateOpenCellLibrary

Point

Incr

Path

clock MY_CLK rise edge	0.00	0.00
clock network delay ideal	0.00	0.00
MY_CLK_r_REG86_S1/CK DFFS_X1	0.00	0.00 r
MY_CLK_r_REG86_S1/Q DFFS_X1	0.10	0.10 r
U1580/ZN OAI21_X1	0.04	0.14 f
U1581/ZN INV_X1	0.04	0.18 r
U1025/Z BUF_X2	0.05	0.23 r
U1005/Z MUX2_X1	0.08	0.31 f
U1041/ZN AND2_X1	0.04	0.34 f
U1668/ZN NAND2_X1	0.04	0.38 r
U814/ZN OAI222_X2	0.07	0.46 f
U1669/Z MUX2_X1	0.08	0.53 f
U1670/ZN NAND2_X1	0.03	0.57 r
U1745/ZN NAND3_X1	0.03	0.60 f
U1747/ZN NOR3_X1	0.05	0.65 r
U1748/ZN OAI222_X1	0.05	0.70 f
U1190/ZN NOR2_X1	0.05	0.75 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.00	0.75 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.03	0.78 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.82 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.86 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.90 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.03	0.94 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.98 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.05	1.03 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.07	1.10 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.00	1.10 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	1.10 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.13 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.16 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.19 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.23 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.02	1.25 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.04	1.29 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.05	1.34 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	1.34 f
U1758/ZN AOI22_X1	0.04	1.38 r
U1759/ZN OAI21_X1	0.04	1.42 f
U981/ZN INV_X2	0.05	1.48 r

U979/ZN AND2_X1	0.05	1.52 r
U1042/ZN NAND2_X1	0.03	1.55 f
U1105/ZN NOR3_X1	0.06	1.62 r
U1028/ZN NAND2_X1	0.04	1.65 f
U1027/ZN INV_X2	0.04	1.70 r
U1091/ZN AND2_X1	0.05	1.74 r
U1088/ZN NAND2_X1	0.03	1.77 f
U1177/ZN OAI221_X1	0.04	1.81 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.00	1.81 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.03	1.84 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.04	1.88 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.04	1.91 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.04	1.95 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.03	1.98 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.05	2.04 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.00	2.04 f
MY_CLK_r_REG13_S2/D DFFR_X1	0.01	2.05 f
data arrival time		2.05
clock MY_CLK rise edge	2.16	2.16
clock network delay ideal	0.00	2.16
clock uncertainty	-0.07	2.09
MY_CLK_r_REG13_S2/CK DFFR_X1	0.00	2.09 r
library setup time	-0.04	2.05
data required time		2.05

data required time		2.05
data arrival time		-2.05

slack MET		0.00

1

3.1.3 Reports of synthesis with *compile_ultra* command

REPORT AREA

Report : area
 Design : fpnew_top
 Version: S-2021.06-SP4
 Date : Sun Dec 10 10:59:48 2023

Librarys Used:

NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db

Number of ports:	96
Number of nets:	3245
Number of cells:	2999
Number of combinational cells:	2865

```

Number of sequential cells:          133
Number of macros/black boxes:       0
Number of buf/inv:                 491
Number of references:              47

Combinational area:                3152.365996
Buf/Inv area:                     283.024001
Noncombinational area:             708.624023
Macro/Black Box area:              0.000000
Net Interconnect area:             undefined Wire load has zero net area

Total cell area:                  3860.990019
Total area:                       undefined
1

```

REPORT TIMING

Information: Updating design information... UID-85

```

Report : timing
  -path full
  -delay max
  -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Sun Dec 10 10:59:48 2023

```

```

Operating Conditions: typical    Library: NangateOpenCellLibrary
Wire Load Model Mode: top

```

```

Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
            rising edge-triggered flip-flop clocked by MY_CLK
Endpoint: status_o[UF]
           output port clocked by MY_CLK
Path Group: MY_CLK
Path Type: max

```

Des/Clust/Port	Wire Load Model	Library
fpnew_top	5K_hvratio_1_1	NangateOpenCellLibrary

Point	Incr	Path
clock MY_CLK rise edge	0.00	0.00
clock network delay ideal	0.00	0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti	0.00	0.00 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti	0.08	0.08 r
U1613/ZN NAND2_X1	0.03	0.11 f
U1117/ZN NOR2_X1	0.05	0.15 r
U1187/ZN AND3_X1	0.07	0.22 r
U1919/ZN OAI21_X1	0.03	0.26 f
U1920/ZN AND2_X1	0.04	0.29 f
U1781/ZN OAI21_X1	0.04	0.33 r
U1728/ZN OAI211_X1	0.05	0.38 f
U1718/ZN OR2_X1	0.07	0.44 f
U1936/ZN OAI21_X1	0.04	0.48 r

U1949/ZN AOI21_X1	0.03	0.52 f
U1960/ZN OAI21_X1	0.04	0.56 r
U1742/ZN NAND2_X1	0.03	0.59 f
U1737/ZN INV_X1	0.04	0.63 r
U1785/ZN OAI22_X1	0.04	0.68 f
U1097/ZN OR2_X2	0.06	0.74 f
U1969/ZN NAND2_X2	0.07	0.81 r
U1371/Z BUF_X1	0.06	0.87 r
U2007/ZN OR2_X1	0.04	0.91 r
U2010/ZN AND4_X2	0.07	0.97 r
U2013/ZN OAI21_X1	0.04	1.01 f
U2016/ZN NAND2_X1	0.03	1.05 r
U2038/ZN AND4_X2	0.07	1.12 r
U2135/ZN INV_X1	0.03	1.15 f
U1109/ZN OR2_X1	0.07	1.22 f
U2148/ZN OAI22_X1	0.07	1.28 r
U1142/ZN AND2_X1	0.06	1.34 r
U1260/ZN NAND4_X1	0.05	1.39 f
U1694/ZN AND2_X1	0.05	1.44 f
U1323/ZN NAND2_X1	0.04	1.48 r
U1765/ZN NAND3_X1	0.05	1.53 f
U1724/ZN OAI21_X2	0.05	1.57 r
U1637/ZN AND3_X1	0.06	1.64 r
U1743/ZN NOR2_X1	0.03	1.66 f
U1784/ZN NOR2_X2	0.05	1.71 r
U1794/ZN NAND4_X1	0.04	1.75 f
U1793/ZN NAND2_X1	0.04	1.79 r
U1741/ZN AND2_X1	0.05	1.84 r
status_o[UF] out	0.02	1.86 r
data arrival time		1.86
<hr/>		
clock MY_CLK rise edge	2.43	2.43
clock network delay ideal	0.00	2.43
clock uncertainty	-0.07	2.36
output external delay	-0.50	1.86
data required time		1.86
<hr/>		
data required time		1.86
data arrival time		-1.86
<hr/>		
slack MET		0.00

1

3.1.4 Reports of synthesis with *compile* command and CSA architecture before *optimization_registers* command

REPORT AREA

Report : area
 Design : fpnew_top
 Version: S-2021.06-SP4
 Date : Wed Dec 13 19:40:25 2023

Librarys Used:

NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db

```

Number of ports:          532
Number of nets:           3187
Number of cells:          2567
Number of combinational cells: 2401
Number of sequential cells: 140
Number of macros/black boxes: 0
Number of buf/inv:         599
Number of references:     50

Combinational area:      2808.693994
Buf/Inv area:             365.217999
Noncombinational area:    747.460024
Macro/Black Box area:     0.000000
Net Interconnect area:    undefined Wire load has zero net area

Total cell area:          3556.154018
Total area:                undefined
1

```

REPORT RESOURCES

```

Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 19:40:25 2023

```

```

Resource Sharing Report for design fpnew_top in file
..../cvfpu_lite/src/fpnew_top.sv
=====
```

	Contained	Resource	Module	Parameters	R
r428	DW01_cmp2	width=3	gen_operation_groups[0].i_opgroup_block/i_arbiter/gt_208_G4		

```

Implementation Report
=====
```

Current	Set	Cell	Module
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes			

```

1
=====
```

REPORT TIMING

```

Information: Updating design information... UID-85

```

```

Report : timing
  -path full
  -delay max
  -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 19:40:25 2023

```

Operating Conditions: typical Library: NangateOpenCellLibrary
 Wire Load Model Mode: top

```

Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
            rising edge-triggered flip-flop clocked by MY_CLK
Endpoint: status_o[UF]
          output port clocked by MY_CLK
Path Group: MY_CLK
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----
fpnew_top           5K_hvratio_1_1       NangateOpenCellLibrary

Point                Incr      Path
-----
clock MY_CLK rise edge        0.00      0.00
clock network delay ideal    0.00      0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.00      0.00 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.07      0.07 r
U1294/ZN AND2_X1         0.04      0.11 r
U1136/ZN AND2_X1         0.04      0.15 r
U1103/ZN NAND3_X1        0.03      0.19 f
U1764/ZN OAI211_X1        0.04      0.22 r
U1269/ZN AOI221_X1        0.04      0.26 f
U1127/ZN AOI211_X1        0.09      0.35 r
U1121/ZN OAI211_X1        0.04      0.39 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.00      0.39 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.04      0.44 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.04      0.48 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.03      0.51 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.05      0.57 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.04      0.61 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.06      0.67 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti
                           0.00      0.67 r
U1296/ZN NAND2_X1         0.03      0.70 f
U1298/ZN OAI21_X1         0.04      0.74 r
U1300/ZN NAND2_X1         0.03      0.78 f
U1039/ZN NAND2_X1         0.03      0.81 r
U808/ZN OAI222_X1         0.06      0.87 f
U1844/ZN INV_X1           0.04      0.91 r
U1845/ZN NAND2_X1         0.03      0.95 f
U968/Z BUF_X1              0.04      0.99 f
U890/Z BUF_X1              0.04      1.03 f
U1888/ZN OAI221_X1         0.07      1.10 r
U1892/ZN AOI22_X1           0.03      1.13 f
U985/ZN OAI221_X1           0.04      1.17 r
U828/ZN OR2_X1              0.04      1.21 r
U849/ZN AND3_X2              0.05      1.27 r
U1041/ZN OAI211_X1           0.05      1.32 f
U975/ZN NOR2_X1              0.06      1.38 r

```

U1951/ZN AOI22_X1	0.04	1.41 f
U1952/ZN OAI21_X1	0.04	1.46 r
U1953/ZN INV_X1	0.03	1.48 f
U1048/ZN AOI22_X1	0.06	1.54 r
U1116/ZN OAI221_X1	0.06	1.60 f
U1151/ZN OAI211_X1	0.04	1.65 r
U2140/ZN OAI211_X1	0.04	1.69 f
U878/Z MUX2_X1	0.07	1.76 f
U1148/ZN NAND2_X1	0.03	1.79 r
U865/ZN AND2_X1	0.04	1.83 r
U1075/ZN AND2_X1	0.04	1.87 r
U846/ZN AND3_X1	0.05	1.92 r
U1214/ZN XNOR2_X1	0.05	1.98 r
U2146/ZN NAND3_X1	0.03	2.01 f
U1164/ZN NOR2_X1	0.04	2.05 r
U2149/ZN OAI21_X1	0.03	2.08 f
U1150/ZN NAND2_X1	0.03	2.11 r
U1108/ZN AND2_X1	0.05	2.16 r
status_o[UF] out	0.02	2.18 r
data arrival time		2.18
<hr/>		
clock MY_CLK rise edge	2.75	2.75
clock network delay ideal	0.00	2.75
clock uncertainty	-0.07	2.68
output external delay	-0.50	2.18
data required time		2.18
<hr/>		
data required time		2.18
data arrival time		-2.18
<hr/>		
slack MET		0.00

1

3.1.5 Reports of synthesis with *compile* command and CSA architecture after *optimization_registers* command

REPORT AREA

Report : area
 Design : fpnew_top
 Version: S-2021.06-SP4
 Date : Wed Dec 13 21:00:48 2023

Librarys Used:

NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db

Number of ports:	524
Number of nets:	3250
Number of cells:	2685
Number of combinational cells:	2404
Number of sequential cells:	259
Number of macros/black boxes:	0
Number of buf/inv:	561
Number of references:	52

```
Combinational area: 2774.379994
Buf/Inv area: 325.052001
Noncombinational area: 1377.880044
Macro/Black Box area: 0.000000
Net Interconnect area: undefined Wire load has zero net area

Total cell area: 4152.260039
Total area: undefined
1
```

REPORT RESOURCES

```
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 21:00:48 2023
```

```
Resource Sharing Report for design fpnew_top in file
..../cvfpu_lite/src/fpnew_top.sv
```

```
=====
Contained Resource Module Parameters Re
r428 DW01_cmp2 width=3 gen_operation_groups[0].i_opgroup_block/i_arbiter/gt_208_G4
```

```
Implementation Report
```

```
=====
Current Set Cell Module
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
```

```
1
```

REPORT TIMING

```
Information: Updating design information... UID-85
```

```
Report : timing
-path full
-delay max
-max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 21:00:48 2023
```

```
Operating Conditions: typical Library: NangateOpenCellLibrary
Wire Load Model Mode: top
```

```
Startpoint: MY_CLK_r_REG144_S2
            rising edge-triggered flip-flop clocked by MY_CLK
Endpoint: status_o[UF]
          output port clocked by MY_CLK
Path Group: MY_CLK
Path Type: max
```

Des/Clust/Port	Wire Load Model	Library
fpnew_top	5K_hvratio_1_1	NangateOpenCellLibrary
Point	Incr	Path
clock MY_CLK rise edge	0.00	0.00
clock network delay ideal	0.00	0.00
MY_CLK_r_REG144_S2/CK DFFR_X1	0.00	0.00 r
MY_CLK_r_REG144_S2/Q DFFR_X1	0.12	0.12 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.00	0.12 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.07	0.19 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.00	0.19 r
U781/ZN NAND4_X1	0.05	0.24 f
U1261/ZN OAI22_X1	0.06	0.30 r
U1784/ZN NAND2_X1	0.06	0.36 f
U1058/ZN INV_X2	0.07	0.43 r
U1860/ZN NAND3_X1	0.04	0.47 f
U1091/ZN OAI221_X1	0.05	0.52 r
U1003/ZN NOR2_X1	0.04	0.56 f
U911/ZN NAND2_X2	0.06	0.62 r
U1877/ZN INV_X1	0.04	0.66 f
U1880/ZN AOI22_X1	0.06	0.72 r
U1097/ZN AND2_X2	0.05	0.77 r
U1092/ZN NAND4_X2	0.05	0.81 f
U1907/ZN INV_X1	0.04	0.86 r
U885/ZN AND2_X2	0.06	0.91 r
U2048/ZN AOI22_X1	0.04	0.95 f
U1082/ZN AND2_X1	0.04	0.99 f
U2049/ZN NOR4_X1	0.09	1.09 r
U1291/ZN OAI221_X4	0.09	1.18 f
U2122/ZN OAI211_X1	0.04	1.22 r
U926/ZN AND3_X1	0.06	1.28 r
U748/ZN AND3_X1	0.05	1.33 r
U899/ZN AND2_X2	0.05	1.37 r
U893/ZN AND2_X2	0.05	1.42 r
U1062/ZN NAND2_X1	0.03	1.46 f
U1171/ZN XNOR2_X1	0.05	1.51 f
U1079/ZN OAI21_X1	0.04	1.55 r
U1076/ZN NAND2_X1	0.03	1.58 f
U1049/ZN NAND2_X1	0.03	1.61 r
U1016/ZN AND2_X1	0.05	1.66 r
status_o[UF] out	0.02	1.68 r
data arrival time		1.68
clock MY_CLK rise edge	2.25	2.25
clock network delay ideal	0.00	2.25
clock uncertainty	-0.07	2.18
output external delay	-0.50	1.68
data required time		1.68
data required time		1.68
data arrival time		-1.68
slack MET		0.00

1

3.1.6 Reports of synthesis with *compile* command and PPARCH architecture before *optimization_registers* command

REPORT AREA

```
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 16:17:02 2023
```

Librarys Used:

```
NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db
```

```
Number of ports:          470
Number of nets:           3009
Number of cells:          2471
Number of combinational cells: 2310
Number of sequential cells: 140
Number of macros/black boxes: 0
Number of buf/inv:         581
Number of references:     53

Combinational area:      2702.825995
Buf/Inv area:             356.971999
Noncombinational area:    747.460024
Macro/Black Box area:     0.000000
Net Interconnect area:    undefined Wire load has zero net area

Total cell area:          3450.286019
Total area:                undefined
1
```

REPORT RESOURCES

```
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 13 16:17:02 2023
```

```
Resource Sharing Report for design fpnew_top in file
..../cvfpu_lite/src/fpnew_top.sv
```

```
=====
          Contained          Resource  Module      Parameters  Re
r429      DW01_cmp2      width=3      gen_operation_groups[0].i_opgroup_block/i_arbiter/gt_208_G4
```

```
Implementation Report
```

```
=====          Current          Set          Cell          Module
```

```
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
```

1

REPORT TIMING

Information: Updating design information... UID-85

Report : timing
 -path full
 -delay max
 -max_paths 1

Design : fpnew_top

Version: S-2021.06-SP4

Date : Wed Dec 13 16:17:02 2023

Operating Conditions: typical Library: NangateOpenCellLibrary

Wire Load Model Mode: top

```
Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
            rising edge-triggered flip-flop clocked by MY_CLK
Endpoint:  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
            rising edge-triggered flip-flop clocked by MY_CLK
Path Group: MY_CLK
Path Type: max
```

Des/Clust/Port	Wire Load Model	Library
fpnew_top	5K_hvratio_1_1	NangateOpenCellLibrary

Point	Incr	Path
clock MY_CLK rise edge	0.00	0.00
clock network delay ideal	0.00	0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	0.00 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.07	0.07 r
U1240/ZN INV_X1	0.03	0.09 f
U1284/ZN NOR3_X1	0.07	0.16 r
U1285/ZN NAND3_X1	0.05	0.21 f
U1318/ZN INV_X1	0.04	0.24 r
U1334/ZN NAND2_X1	0.04	0.29 f
U779/ZN AOI22_X1	0.06	0.34 r
U1335/ZN INV_X1	0.02	0.37 f
U1338/ZN OAI21_X1	0.06	0.43 r
U1339/ZN INV_X1	0.03	0.45 f
U1342/ZN OAI21_X1	0.06	0.52 r
U1346/ZN OAI21_X1	0.04	0.56 f
U1347/ZN OAI21_X1	0.04	0.60 r
U1348/ZN INV_X1	0.03	0.63 f
U1173/ZN XNOR2_X1	0.06	0.69 r
U1172/ZN XOR2_X1	0.08	0.76 r
U1363/ZN NAND2_X1	0.04	0.80 f
U1366/ZN OAI21_X1	0.07	0.88 r
U1369/ZN INV_X1	0.03	0.91 f
U1370/ZN OAI21_X1	0.04	0.95 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active		

gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	0.95 r
	0.03	0.98 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.06	1.04 f
	0.03	1.07 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.10 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	1.10 f
U940/Z BUF_X1	0.05	1.15 f
U1394/ZN AOI211_X1	0.09	1.24 r
U1398/ZN OAI21_X1	0.05	1.28 f
U1417/ZN OAI21_X1	0.07	1.36 r
U1418/ZN INV_X1	0.05	1.40 f
U886/ZN NAND2_X2	0.07	1.47 r
U1440/ZN OAI22_X1	0.05	1.52 f
U1442/Z MUX2_X1	0.08	1.59 f
U1443/ZN INV_X1	0.04	1.63 r
U1468/Z MUX2_X1	0.05	1.68 r
U1469/ZN INV_X1	0.03	1.71 f
U1534/Z MUX2_X1	0.07	1.79 f
U1535/ZN NAND2_X1	0.03	1.82 r
U1596/ZN NAND4_X1	0.05	1.87 f
U1597/ZN NOR3_X1	0.06	1.93 r
U1598/ZN OAI222_X1	0.06	1.99 f
U1599/ZN NOR2_X1	0.05	2.04 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.00	2.04 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.04	2.08 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.05	2.13 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.04	2.17 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.05	2.22 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.05	2.27 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.06	2.33 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.05	2.38 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan	0.00	2.38 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	2.38 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.06	2.43 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	2.46 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.04	2.50 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.04	2.55 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.08	2.63 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.05	2.68 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.07	2.75 f

```

gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
          0.00      2.75 f
U1633/ZN AOI22_X1           0.05      2.79 r
U1634/ZN OAI21_X1           0.03      2.83 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
          0.01      2.84 f
data arrival time           2.84

clock MY_CLK rise edge     2.95      2.95
clock network delay ideal   0.00      2.95
clock uncertainty           -0.07     2.88
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active
          0.00      2.88 r
library setup time          -0.04     2.84
data required time          2.84
-----
data required time          2.84
data arrival time           -2.84
-----
slack MET                  0.00

```

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3.1.7 Reports of synthesis with *compile* command and PPARCH architecture after *optimization_registers* command

REPORT AREA

Report : area
 Design : fpnew_top
 Version: S-2021.06-SP4
 Date : Wed Dec 13 17:16:19 2023

Librarys Used:

NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db

Number of ports:	462
Number of nets:	3269
Number of cells:	2792
Number of combinational cells:	2521
Number of sequential cells:	253
Number of macros/black boxes:	0
Number of buf/inv:	613
Number of references:	50
Combinational area:	2820.663992
Buf/Inv area:	365.484000
Noncombinational area:	1345.960043
Macro/Black Box area:	0.000000
Net Interconnect area:	undefined Wire load has zero net area
Total cell area:	4166.624035
Total area:	undefined

1

[REPORT RESOURCES]

Report : resources
 Design : fpnew_top
 Version: S-2021.06-SP4
 Date : Wed Dec 13 17:16:19 2023

Resource Sharing Report for design fpnew_top in file
/cvfpu_lite/src/fpnew_top.sv

		Contained	Resource	Module	Parameters	R
r429	DW01_cmp2	width=3	gen_operation_groups[0].i_opgroup_block/i_arbiter/gt_208_G4			

Implementation Report

	Current	Set	Cell	Module
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan				

1

[REPORT TIMING]

Information: Updating design information... UID-85

Report : timing
 -path full
 -delay max
 -max_paths 1
 Design : fpnew_top
 Version: S-2021.06-SP4
 Date : Wed Dec 13 17:16:19 2023

Operating Conditions: typical Library: NangateOpenCellLibrary
 Wire Load Model Mode: top

Startpoint: MY_CLK_r_REG86_S1
 rising edge-triggered flip-flop clocked by MY_CLK
 Endpoint: MY_CLK_r_REG13_S2
 rising edge-triggered flip-flop clocked by MY_CLK
 Path Group: MY_CLK
 Path Type: max

Des/Clust/Port	Wire Load Model	Library
fpnew_top	5K_hvratio_1_1	NangateOpenCellLibrary

Point	Incr	Path
clock MY_CLK rise edge	0.00	0.00
clock network delay ideal	0.00	0.00
MY_CLK_r_REG86_S1/CK DFFS_X1	0.00	0.00 r
MY_CLK_r_REG86_S1/Q DFFS_X1	0.10	0.10 r
U1582/ZN OAI21_X1	0.04	0.14 f

U1583/ZN INV_X1	0.04	0.18 r
U1027/Z BUF_X2	0.05	0.23 r
U1007/Z MUX2_X1	0.08	0.31 f
U1043/ZN AND2_X1	0.04	0.34 f
U1670/ZN NAND2_X1	0.04	0.38 r
U816/ZN OAI222_X2	0.07	0.46 f
U1671/Z MUX2_X1	0.08	0.53 f
U1672/ZN NAND2_X1	0.03	0.57 r
U1747/ZN NAND3_X1	0.03	0.60 f
U1749/ZN NOR3_X1	0.05	0.65 r
U1750/ZN OAI222_X1	0.05	0.70 f
U1192/ZN NOR2_X1	0.05	0.75 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.00	0.75 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.03	0.78 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.82 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.86 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.90 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.03	0.94 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.04	0.98 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.05	1.03 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.07	1.10 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.00	1.10 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	1.10 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.13 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.16 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.19 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.03	1.23 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.02	1.25 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.04	1.29 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.05	1.34 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].active	0.00	1.34 f
U1760/ZN AOI22_X1	0.04	1.38 r
U1761/ZN OAI21_X1	0.04	1.42 f
U983/ZN INV_X2	0.05	1.48 r
U981/ZN AND2_X1	0.05	1.52 r
U1044/ZN NAND2_X1	0.03	1.55 f
U1107/ZN NOR3_X1	0.06	1.62 r
U1030/ZN NAND2_X1	0.04	1.65 f
U1029/ZN INV_X2	0.04	1.70 r
U1093/ZN AND2_X1	0.05	1.74 r
U1090/ZN NAND2_X1	0.03	1.77 f
U1179/ZN OAI221_X1	0.04	1.81 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0]	0.00	1.81 r

```

0.00      1.81 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.03      1.84 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.04      1.88 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.04      1.91 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.04      1.95 r
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.03      1.98 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.05      2.04 f
sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lan
          0.00      2.04 f
MY_CLK_r_REG13_S2/D DFFR_X1
data arrival time
          0.01      2.05 f
          2.05

clock MY_CLK rise edge
          2.16      2.16
clock network delay ideal
          0.00      2.16
clock uncertainty
          -0.07     2.09
MY_CLK_r_REG13_S2/CK DFFR_X1
library setup time
          0.00      2.09 r
          -0.04     2.05
data required time
          2.05
-----
data required time
          2.05
data arrival time
          -2.05
-----
slack MET
          0.00

```

1

3.2 R4-MBE multiplier

3.2.1 Booth Encoder Radix-4

```

1 module booth_encoder_rad4 (
2   input logic b_next,
3   input logic b_n,
4   input logic b_prev,
5   input logic [10:0] A,
6   output logic neg,
7   output logic [11:0] A_out
8 );
9
10 logic [2:0] b_temp;
11
12 always_comb begin
13
14   b_temp = {b_next, b_n, b_prev};
15
16   case (b_temp)
17     3'b000: begin
18       A_out = 12'b000000000000;
19       neg = 1'b0;
20     end
21     3'b001, 3'b010: begin

```

```

22     A_out = {1'b0, A};
23     neg = 1'b0;
24   end
25   3'b011: begin
26     A_out = {A, 1'b0};
27     neg = 1'b0;
28   end
29   3'b100: begin
30     A_out = ~{A, 1'b0};
31     neg = 1'b1;
32   end
33   3'b101, 3'b110: begin
34     A_out = ~{1'b0, A};
35     neg = 1'b1;
36   end
37   3'b111: begin
38     A_out = 12'b000000000000;
39     neg = 1'b0;
40   end
41   endcase
42 end
43
44 endmodule

```

3.2.2 Dadda tree

```

1 module dadda_tree (
2   input logic [11:0] pp1,
3   input logic [11:0] pp2,
4   input logic [11:0] pp3,
5   input logic [11:0] pp4,
6   input logic [11:0] pp5,
7   input logic [11:0] pp6,
8   input logic s1,
9   input logic s2,
10  input logic s3,
11  input logic s4,
12  input logic s5,
13  input logic s6,
14
15  output logic [21:0] carry,
16  output logic [21:0] sum
17 );
18
19 wire h1_c, h1_s;
20 wire h2_c, h2_s;
21 wire h3_c, h3_s;
22 wire h4_c, h4_s;
23 wire h5_c, h5_s;
24 wire h6_c, h6_s;
25 wire h7_c, h7_s;
26 wire h8_c, h8_s;
27 wire h9_c, h9_s;
28 wire h10_c, h10_s;
29 wire h11_c, h11_s;
30 wire h12_c, h12_s;
31
32 wire a1_c, a1_s;

```

```
33  wire a2_c, a2_s;
34  wire a3_c, a3_s;
35  wire a4_c, a4_s;
36  wire a5_c, a5_s;
37  wire a6_c, a6_s;
38  wire a7_c, a7_s;
39  wire a8_c, a8_s;
40  wire a9_c, a9_s;
41  wire a10_c, a10_s;
42  wire a11_c, a11_s;
43  wire a12_c, a12_s;
44  wire a13_c, a13_s;
45  wire a14_c, a14_s;
46  wire a15_c, a15_s;
47  wire a16_c, a16_s;
48  wire a17_c, a17_s;
49  wire a18_c, a18_s;
50  wire a19_c, a19_s;
51  wire a20_c, a20_s;
52  wire a21_c, a21_s;
53  wire a22_c, a22_s;
54  wire a23_c, a23_s;
55  wire a24_c, a24_s;
56  wire a25_c, a25_s;
57  wire a26_c, a26_s;
58  wire a27_c, a27_s;
59  wire a28_c, a28_s;
60  wire a29_c, a29_s;
61  wire a30_c, a30_s;
62  wire a31_c, a31_s;
63  wire a32_c, a32_s;
64  wire a33_c, a33_s;
65  wire a34_c, a34_s;
66  wire a35_c, a35_s;
67  wire a36_c, a36_s;
68  wire a37_c, a37_s;
69  wire a38_c, a38_s;
70  wire a39_c, a39_s;
71  wire a40_c, a40_s;
72  wire a41_c, a41_s;
73  wire a42_c, a42_s;
74  wire a43_c, a43_s;
75  wire a44_c, a44_s;
76
77 //layer1
78 half_adder h1 (pp1[6],pp2[4],h1_s,h1_c);
79 half_adder h2 (pp1[7],pp2[5],h2_s,h2_c);
80 half_adder h3 (pp1[8],pp2[6],h3_s,h3_c);
81 half_adder h4 (pp1[9],pp2[7],h4_s,h4_c);
82 half_adder h5 (1'b1,pp3[11],h5_s,h5_c);
83 half_adder h6 (1'b1,pp4[11],h6_s,h6_c);
84 full_adder f1 (pp3[4],pp4[2],pp5[0],a1_s,a1_c);
85 full_adder f2 (pp3[5],pp4[3],pp5[1],a2_s,a2_c);
86 full_adder f3 (pp1[10],pp2[8],pp3[6],a3_s,a3_c);
87 full_adder f4 (pp4[4],pp5[2],pp6[0],a4_s,a4_c);
88 full_adder f5 (pp1[11],pp2[9],pp3[7],a5_s,a5_c);
89 full_adder f6 (pp4[5],pp5[3],pp6[1],a6_s,a6_c);
90 full_adder f7 (s1,pp2[10],pp3[8],a7_s,a7_c);
91 full_adder f8 (pp4[6],pp5[4],pp6[2],a8_s,a8_c);
92 full_adder f9 (s1,pp2[11],pp3[9],a9_s,a9_c);
93 full_adder f10 (pp4[7],pp5[5],pp6[3],a10_s,a10_c);
94 full_adder f11 (~s1,~s2,pp3[10],a11_s,a11_c);
```

```

95    full_adder f12 (pp4[8],pp5[6],pp6[4],a12_s,a12_c);
96    full_adder f13 (pp4[9],pp5[7],pp6[5],a13_s,a13_c);
97    full_adder f14 (~s3,pp4[10],pp5[8],a14_s,a14_c);
98
99 //layer2
100 half_adder h7 (pp1[4],pp2[2],h7_s,h7_c);
101 half_adder h8 (pp1[5],pp2[3],h8_s,h8_c);
102 half_adder h9 (1'b1,pp5[11],h9_s,h9_c);
103 full_adder f15 (h1_s,pp3[2],pp4[0],a15_s,a15_c);
104 full_adder f16 (h1_c,h2_s,pp3[3],a16_s,a16_c);
105 full_adder f17 (h2_c,h3_s,a1_s,a17_s,a17_c);
106 full_adder f18 (h3_c,h4_s,a2_s,a18_s,a18_c);
107 full_adder f19 (h4_c,a3_s,a4_s,a19_s,a19_c);
108 full_adder f20 (a3_c,a5_s,a6_s,a20_s,a20_c);
109 full_adder f21 (a5_c,a7_s,a8_s,a21_s,a21_c);
110 full_adder f22 (a7_c,a9_s,a10_s,a22_s,a22_c);
111 full_adder f23 (a9_c,a11_s,a12_s,a23_s,a23_c);
112 full_adder f24 (a11_c,h5_s,a13_s,a24_s,a24_c);
113 full_adder f25 (h5_c,a14_s,pp6[6],a25_s,a25_c);
114 full_adder f26 (a14_c,h6_s,pp5[9],a26_s,a26_c);
115 full_adder f27 (h6_c,pp5[10],~s4,a27_s,a27_c);
116
117 //layer3
118 half_adder h10 (pp1[2],pp2[0],h10_s,h10_c);
119 half_adder h11 (pp1[3],pp2[1],h11_s,h11_c);
120 half_adder h12 (pp6[11],1'b1,h12_s,h12_c);
121 full_adder f28 (h7_s,pp3[0],s3,a28_s,a28_c);
122 full_adder f29 (h7_c,h8_s,pp3[1],a29_s,a29_c);
123 full_adder f30 (h8_c,a15_s,s4,a30_s,a30_c);
124 full_adder f31 (a15_c,a16_s,pp4[1],a31_s,a31_c);
125 full_adder f32 (a16_c,a17_s,s5,a32_s,a32_c);
126 full_adder f33 (a17_c,a1_c,a18_s,a33_s,a33_c);
127 full_adder f34 (a18_c,a2_c,a19_s,a34_s,a34_c);
128 full_adder f35 (a19_c,a4_c,a20_s,a35_s,a35_c);
129 full_adder f36 (a20_c,a6_c,a21_s,a36_s,a36_c);
130 full_adder f37 (a21_c,a8_c,a22_s,a37_s,a37_c);
131 full_adder f38 (a22_c,a10_c,a23_s,a38_s,a38_c);
132 full_adder f39 (a23_c,a12_c,a24_s,a39_s,a39_c);
133 full_adder f40 (a24_c,a13_c,a25_s,a40_s,a40_c);
134 full_adder f41 (a25_c,a26_s,pp6[7],a41_s,a41_c);
135 full_adder f42 (a26_c,a27_s,pp6[8],a42_s,a42_c);
136 full_adder f43 (a27_c,h9_s,pp6[9],a43_s,a43_c);
137 full_adder f44 (h9_c,pp6[10],~s5,a44_s,a44_c);
138
139 assign sum = {h12_s,a44_s,a43_s,a42_s,a41_s,a40_s,a39_s,a38_s,a37_s,a36_s,a35_s,a34_s,
140           a33_s,a32_s,a31_s,a30_s,a29_s,a28_s,h11_s,h10_s,pp1[1],pp1[0]};
141 assign carry = {a44_c,a43_c,a42_c,a41_c,a40_c,a39_c,a38_c,a37_c,a36_c,a35_c,a34_c,a33_c,
142           a32_c,a31_c,a30_c,a29_c,a28_c,h11_c,h10_c,s2,1'b0,s1};
143
144 endmodule

```

3.2.3 Modified Booth Encoder Radix-4 Multiplier

```

1 module mbe_rad4_mult (
2   input logic [10:0] mantissa_a,
3   input logic [10:0] mantissa_b,
4
5   output logic [21:0] product

```

```

6 );
7
8 wire [11:0] pp1, pp2, pp3, pp4, pp5, pp6;
9 wire s1, s2, s3, s4, s5, s6;
10 wire [21:0]sum, carry;
11
12 booth_encoder_rad4 b1 (mantissa_b[1],mantissa_b[0],1'b0,mantissa_a,s1,pp1);
13 booth_encoder_rad4 b2 (mantissa_b[3],mantissa_b[2],mantissa_b[1],mantissa_a,s2,pp2);
14 booth_encoder_rad4 b3 (mantissa_b[5],mantissa_b[4],mantissa_b[3],mantissa_a,s3,pp3);
15 booth_encoder_rad4 b4 (mantissa_b[7],mantissa_b[6],mantissa_b[5],mantissa_a,s4,pp4);
16 booth_encoder_rad4 b5 (mantissa_b[9],mantissa_b[8],mantissa_b[7],mantissa_a,s5,pp5);
17 booth_encoder_rad4 b6 (1'b0,mantissa_b[10],mantissa_b[9],mantissa_a,s6,pp6);
18
19 dadda_tree d1 (pp1,pp2,pp3,pp4,pp5,pp6,s1,s2,s3,s4,s5,s6,carry,sum);
20
21 assign product = carry+sum;
22
23 endmodule

```

3.3 Reports of the complete FPU synthesis with *compile ultra* command

REPORT AREA

Report : area
 Design : fpnew_top
 Version: S-2021.06-SP4
 Date : Mon Nov 27 19:01:41 2023

Librarys Used:

NangateOpenCellLibrary File: /eda/dk/nangate45/synopsys/NangateOpenCellLibrary_typical_ecsm.db

Number of ports:	96
Number of nets:	3150
Number of cells:	2876
Number of combinational cells:	2742
Number of sequential cells:	133
Number of macros/black boxes:	0
Number of buf/inv:	451
Number of references:	46
Combinational area:	3087.462001
Buf/Inv area:	263.340001
Noncombinational area:	708.092023
Macro/Black Box area:	0.000000
Net Interconnect area:	undefined Wire load has zero net area
Total cell area:	3795.554024
Total area:	undefined
1	

REPORT TIMING

Information: Updating design information... UID-85

```
Report : timing
          -path full
          -delay max
          -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 27 19:01:41 2023
```

Operating Conditions: typical Library: NangateOpenCellLibrary
Wire Load Model Mode: top

```
Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_l  
            rising edge-triggered flip-flop clocked by MY_CLK  
Endpoint: status_o[UF]  
           output port clocked by MY_CLK  
Path Group: MY_CLK  
Path Type: max
```

Des/Clust/Port	Wire Load Model	Library
fpnew_top	5K_hvratio_1_1	NangateOpenCellLibrary
Point	Incr	Path
clock MY_CLK rise edge	0.00	0.00
clock network delay ideal	0.00	0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti	0.00	0.00 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[2].active_format.i_fmt_slice/gen_num_lanes[0].acti	0.09	0.09 f
U1711/ZN NOR2_X2	0.06	0.15 r
U1170/ZN AND3_X1	0.06	0.21 r
U1685/ZN NAND2_X1	0.03	0.24 f
U1743/ZN OR2_X2	0.07	0.31 f
U1654/Z MUX2_X1	0.08	0.38 r
U1311/ZN AND2_X1	0.05	0.43 r
U1525/ZN OAI21_X1	0.03	0.46 f
U2003/ZN AOI21_X1	0.05	0.51 r
U2019/ZN OAI21_X1	0.03	0.55 f
U1164/ZN AND2_X1	0.04	0.59 f
U2037/ZN OR2_X1	0.06	0.65 f
U1156/ZN AND2_X2	0.04	0.70 f
U1712/ZN NOR2_X1	0.04	0.74 r
U1713/ZN NAND2_X1	0.03	0.77 f
U1714/ZN NAND3_X1	0.04	0.81 r
U2041/ZN OR2_X2	0.06	0.87 r
U2090/ZN INV_X1	0.03	0.90 f
U2091/ZN AOI22_X1	0.05	0.95 r
U2093/ZN AND2_X1	0.05	1.01 r
U2094/ZN OAI22_X1	0.04	1.05 f
U1691/ZN OR2_X1	0.05	1.10 f
U1690/ZN NOR2_X1	0.04	1.15 r
U1682/ZN OR2_X1	0.04	1.19 r
U1748/ZN NOR2_X1	0.03	1.21 f
U1176/ZN AND2_X1	0.04	1.25 f
U2178/ZN INV_X1	0.03	1.29 r
U2179/ZN AND2_X1	0.04	1.33 r
U2184/ZN NOR2_X1	0.02	1.35 f

U2186/ZN OAI21_X1	0.05	1.40 r
U2189/ZN AND3_X1	0.06	1.46 r
U1710/ZN NAND2_X1	0.03	1.49 f
U1707/ZN NAND2_X2	0.05	1.54 r
U1441/ZN INV_X1	0.05	1.59 f
U1180/ZN AND2_X1	0.06	1.65 f
U1643/ZN NOR3_X2	0.09	1.75 r
U1265/ZN AND3_X1	0.07	1.81 r
U1689/ZN OAI211_X1	0.04	1.85 f
U2546/ZN INV_X1	0.03	1.88 r
U1670/ZN NAND4_X1	0.04	1.92 f
U1740/ZN NAND2_X1	0.04	1.96 r
U1681/ZN AND2_X1	0.05	2.01 r
status_o[UF] out	0.02	2.03 r
data arrival time		2.03
clock MY_CLK rise edge	2.60	2.60
clock network delay ideal	0.00	2.60
clock uncertainty	-0.07	2.53
output external delay	-0.50	2.03
data required time		2.03

data required time		2.03
data arrival time		-2.03

slack MET		0.00
