Moray, Peru

HIGH SPEED ADDER

Carry-Ripple Adder (CRA)

WHAT WE KNOW …

Si … we derived

C
R
A

xi yi Ci	Si	Ci+1
0 0 0	0	0
0 0 1	1	0
0 1 0	1	0
0 1 1	0	1
1 0 0	1	0
1 0 1	0	1
1 1 0	0	1
1 1 1	1	1

$S_i = C_i \oplus x_i \oplus y_i$

Carry out C_{i+1} ?

C
R
A

xi yi Ci	Si	Ci+1
0 0 0	0	0
0 0 1	1	0
0 1 0	1	0
0 1 1	0	1
1 0 0	1	0
1 0 1	0	1
1 1 0	0	1
1 1 1	1	1

xiyi \ Ci	0	1
00		
01		1
11	1	1
10		1

C
R
A

New carry out C_{i+1}

x_i y_i C_i	S_i	C_{i+1}
0 0 0	0	0
0 0 1	1	0
0 1 0	1	0
0 1 1	0	1
1 0 0	1	0
1 0 1	0	1
1 1 0	0	1
1 1 1	1	1

x_iy_i \ C_i	0	1
00		
01		1
11	1	1
10		1

$$C_{i+1} = x_i y_i + x_i C_i + y_i C_i$$

CRA equations (new...)

$S_i = C_i \oplus x_i \oplus y_i$

$C_{i+1} = x_i y_i + x_i C_i + y_i C_i$

C
R
A

C R A

CRA equations; for i = 0

$S_i = C_i \oplus x_i \oplus y_i$

$C_{i+1} = x_i y_i + x_i C_i + y_i C_i$

CRA equations; i = 0 (1-bit)

C
R
A

$S_i = C_i \oplus x_i \oplus y_i$

$C_{i+1} = x_i y_i + x_i C_i + y_i C_i$

For i = 0

$S_0 = C_0 \oplus x_0 \oplus y_0$

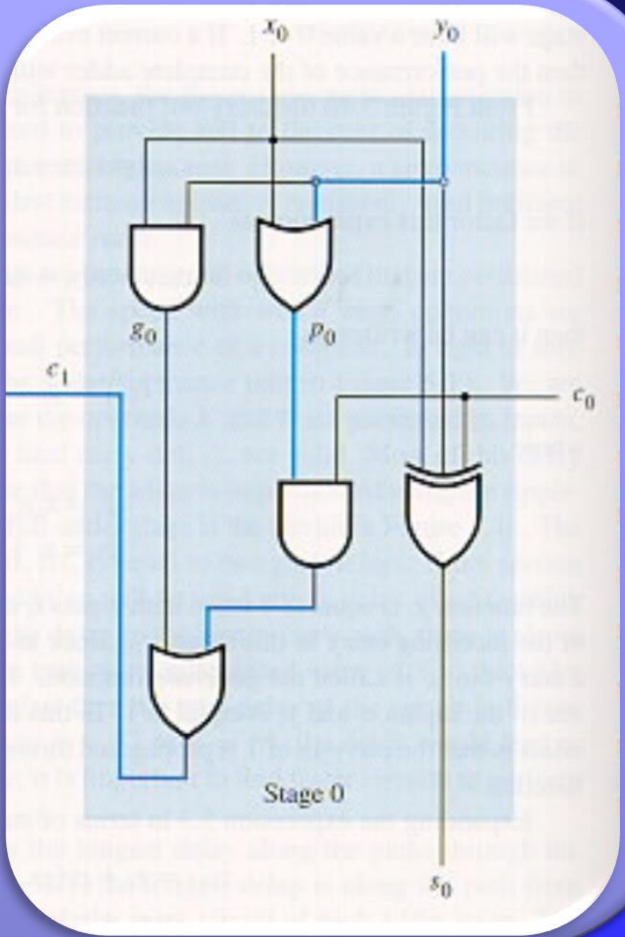
$$C_1 = x_0 y_0 + x_0 C_0 + y_0 C_0$$
$$= x_0 y_0 + C_0(x_0 + y_0)$$

NEW CRA Implementation

$S_0 = C_0 \oplus x_0 \oplus y_0$

1-bit

CRA

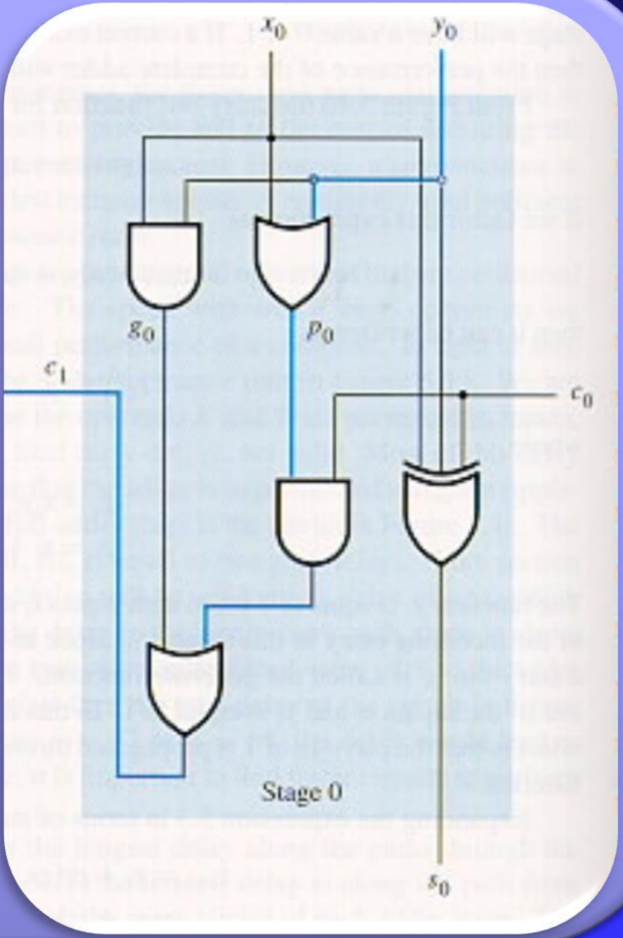


$$S_0 = C_0 \oplus x_0 \oplus y_0$$

$$C_1 = x_0 y_0 + C_0(x_0 + y_0)$$

1-bit

CRA



$S_1 = C_1 \oplus x_1 \oplus y_1$

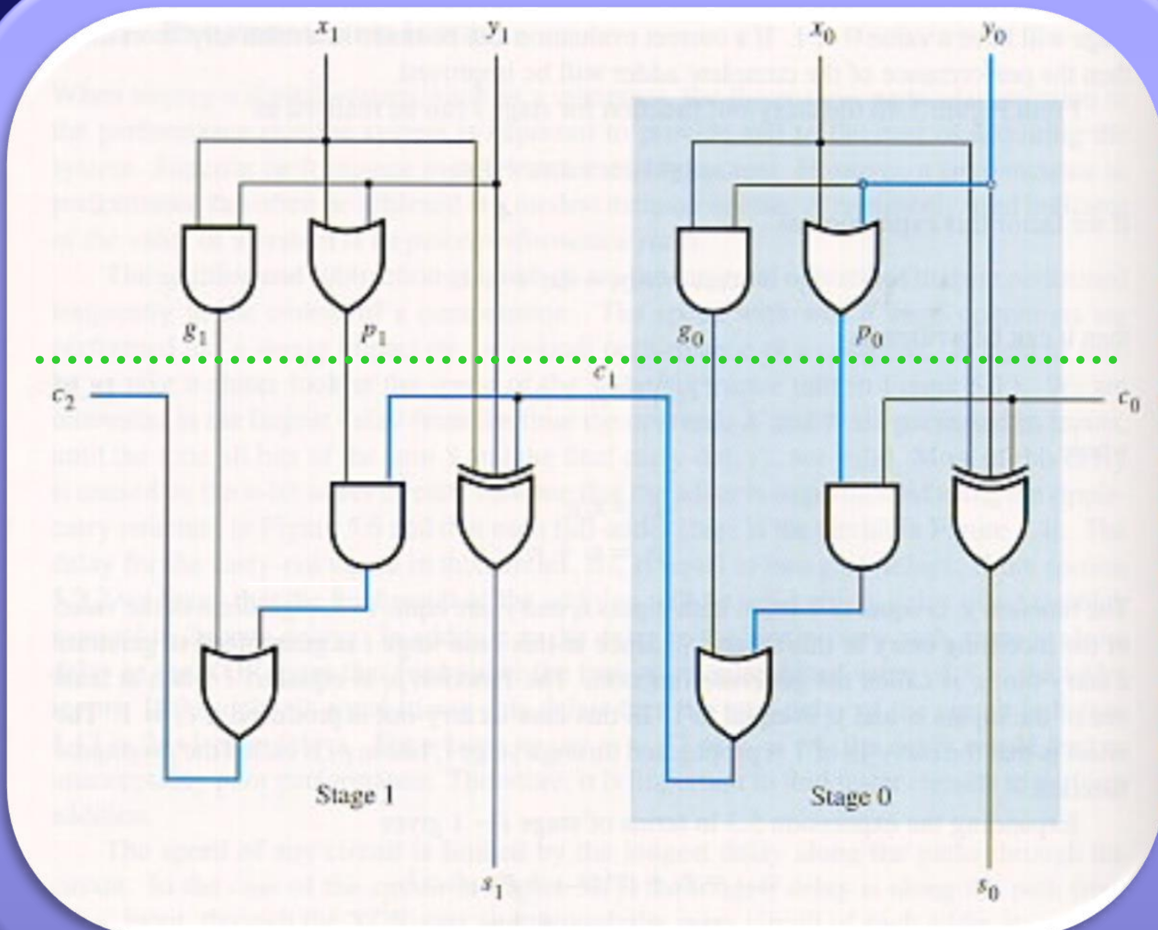
$S_0 = C_0 \oplus x_0 \oplus y_0$

$C_2 = x_1y_1 + C_1(x_1 + y_1)$

$C_1 = x_0y_0 + C_0(x_0 + y_0)$

2-bit

C
R
A



Gate Delay (nsec)

	inputs		
Gate	2	3	4
AND	2.4	2.8	3.2
OR	2.4	2.8	3.2
NAND	1.4	1.8	2.8

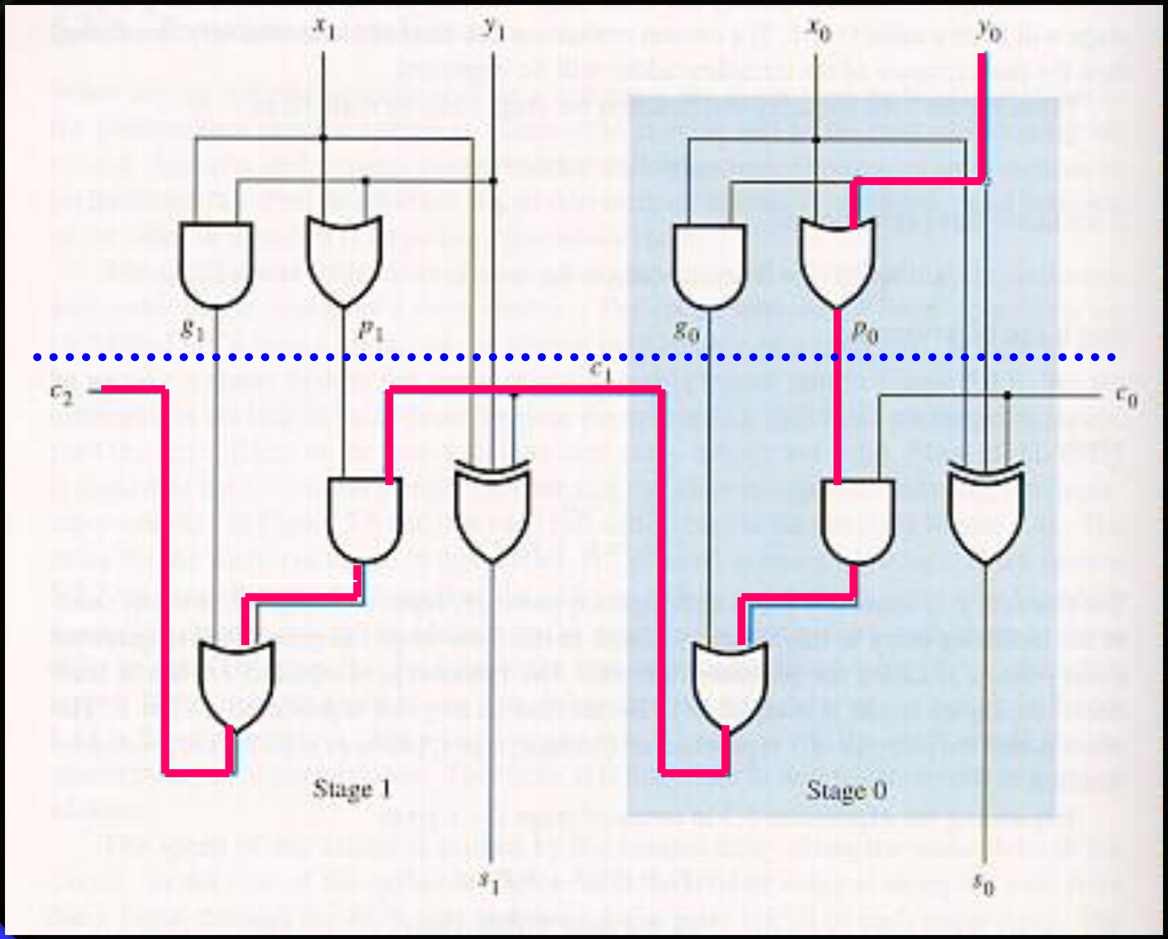
Rate of addition

The rate of addition of binary numbers is usually measured by the carry propagation time of the Adder…

y_0 … c_2 -- the longest path …

2-bit

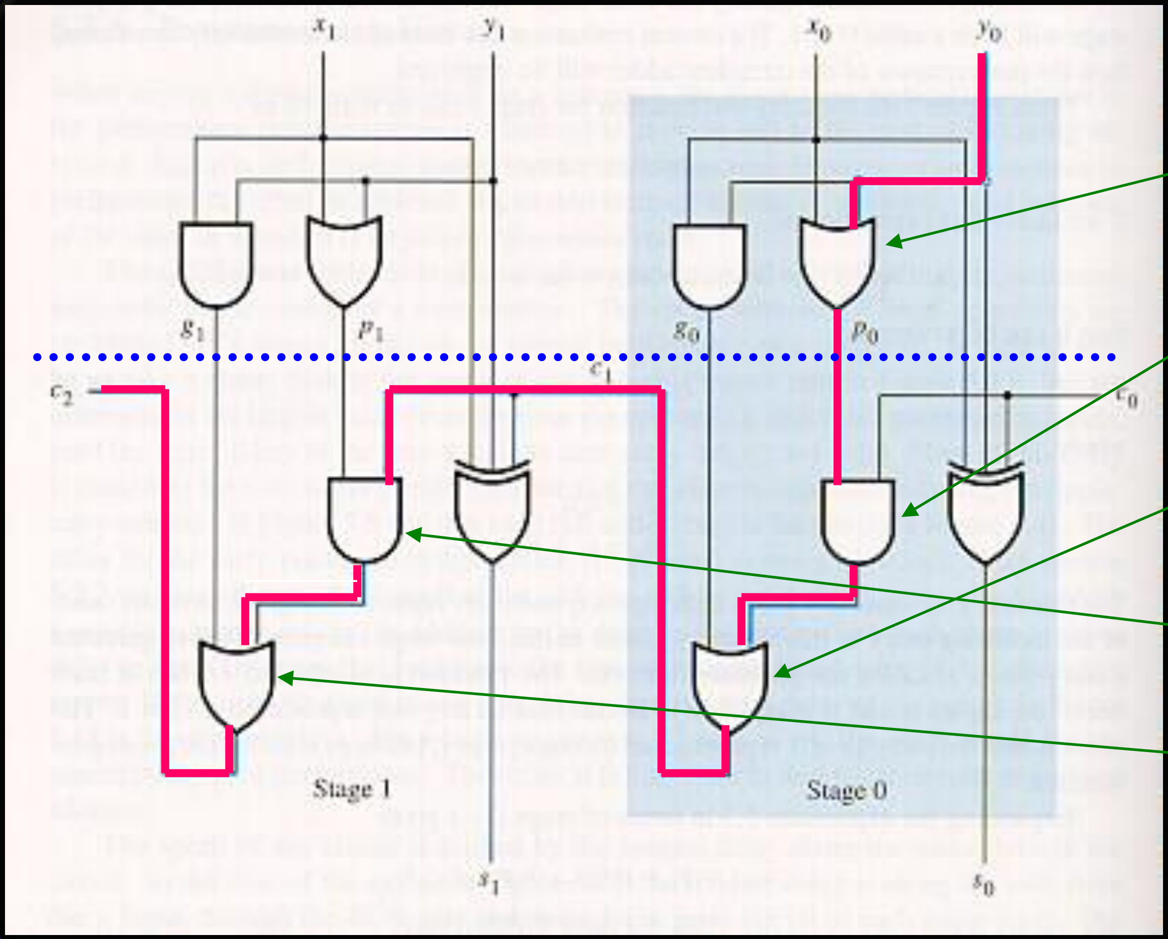
CRA



y_0 … c_2 = 12 nsec

2-bit

CRA



2.4
+
2.4
+
2.4
+
2.4
+
2.4
=
12

Look -Ahead Adder (LAA)

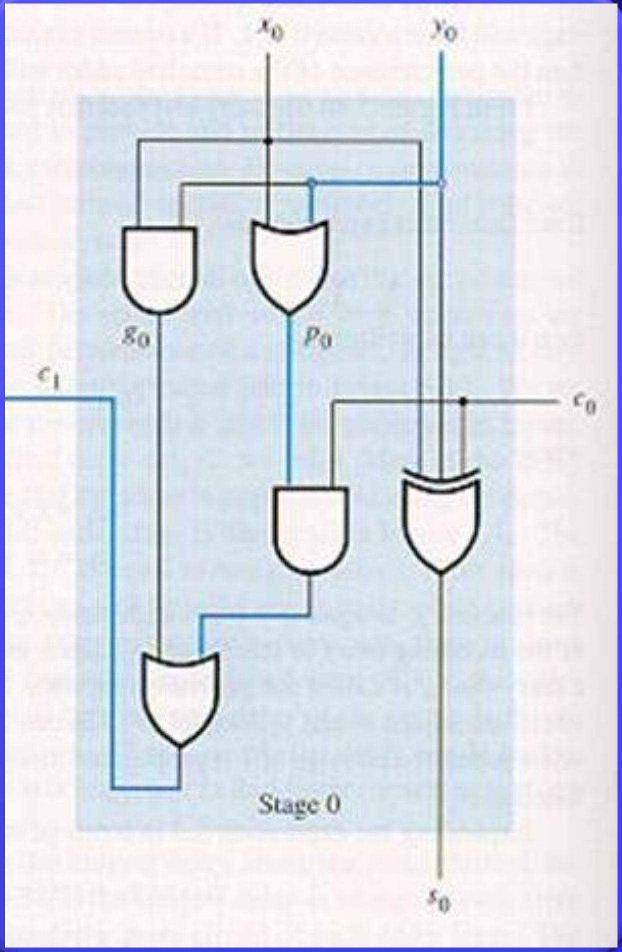
WE WILL LEARN ABOUT A HIGH SPEED ADDER

1-bit CRA Full adder equations

C
R
A

$$S_0 = C_0 \oplus x_0 \oplus y_0$$

$$C_1 = x_0 y_0 + C_0(x_0 + y_0)$$



p_0 - g_0

C
R
A

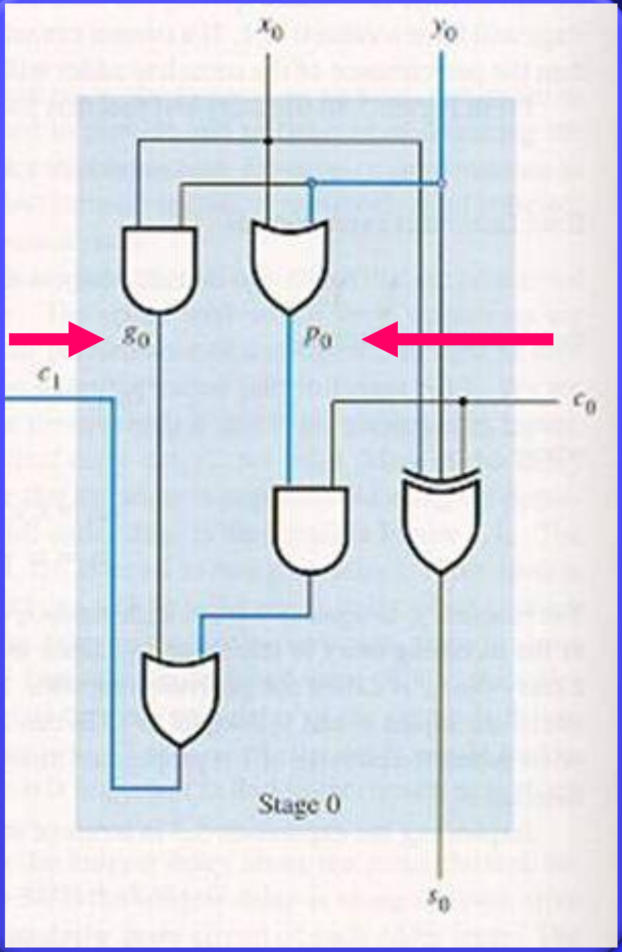
$$S_0 = C_0 \oplus x_0 \oplus y_0$$

$$C_1 = x_0 y_0 + C_0(x_0 + y_0)$$

if,

$$g_0 = x_0\, y_0$$

$$p_0 = x_0 + y_0$$



C R A

p_0 = internal propagated carry
g_0 = internal generated carry

$$S_0 = C_0 \oplus x_0 \oplus y_0$$

$$C_1 = x_0 y_0 + C_0(x_0 + y_0)$$

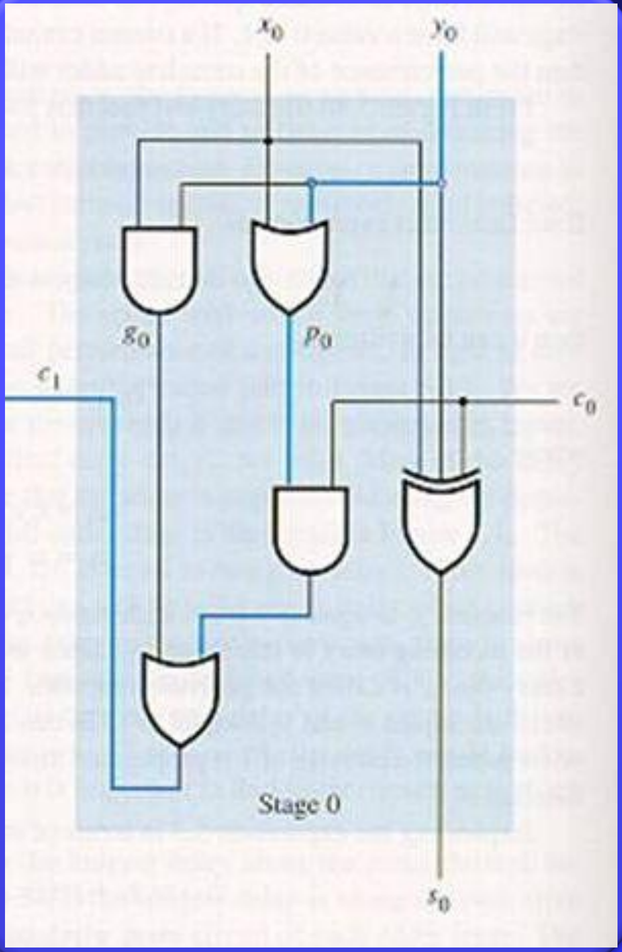
if,

$$g_0 = x_0 y_0$$

$$p_0 = x_0 + y_0$$

then,

$$C_1 = g_0 + C_0 p_0$$



go – po … an explanation

Full adder: Truth table

xi	yi	Ci	S	Ci+1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Observations

xi yi Ci	S	Ci+1
0 0 0	0	0
0 0 1	1	0
0 1 0	1	0
0 1 1	0	1
1 0 0	1	0
1 0 1	0	1
1 1 0	0	1
1 1 1	1	1

Observations

xi	yi	Ci	S	Ci+1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Carry is Propagated for yi

Carry is Propagated for xi

Observations

xi	yi	Ci	S	Ci+1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Carry is Propagated for yi

Carry is Propagated for xi

Carry is Generated

Propagated Carry…

xi	yi	Ci	S	Ci+1	
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	0	
0	1	1	0	1	P
1	0	0	1	0	
1	0	1	0	1	P
1	1	0	0	1	G
1	1	1	1	1	

⊕ ⊕

Generated Carry

xi	yi	Ci	S	Ci+1	
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	0	
0	1	1	0	1	P
1	0	0	1	0	
1	0	1	0	1	P
1	1	0	0	1	G
1	1	1	1	1	

$$P_i = \overline{x_i} \cdot y_i + x_i \cdot \overline{y_i}$$

$$P_i = y_i \oplus x_i$$

$$G_i = x_i \cdot y_i$$

The logical trick … for Pi

xi yi Ci	S	Ci+1	
0 0 0	0	0	
0 0 1	1	0	
0 1 0	1	0	
0 1 1	0	1	P
1 0 0	1	0	
1 0 1	0	1	P
1 1 0	0	1	G
1 1 1	1	1	

xi	yi	$yi \oplus xi$	
0	1	?	
1	0	?	

$$Pi = yi \oplus xi$$

$$Gi = xi \cdot yi$$

Therefore …

x_i	y_i	C_i	S	C_{i+1}	
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	0	
0	1	1	0	1	P
1	0	0	1	0	
1	0	1	0	1	P
1	1	0	0	1	G
1	1	1	1	1	

xi	yi	$y_i \oplus x_i$	yi+xi
0	1	1	?
1	0	1	?

$P_i = y_i \oplus x_i$

$G_i = x_i \cdot y_i$

Therefore …

xi yi Ci	S	Ci+1	
0 0 0	0	0	
0 0 1	1	0	
0 1 0	1	0	
0 1 1	0	1	P
1 0 0	1	0	
1 0 1	0	1	P
1 1 0	0	1	G
1 1 1	1	1	

xi	yi	yi ⊕ xi	yi+xi
0	1	1	1
1	0	1	1

$P_i = y_i \oplus x_i = y_i + x_i$

$G_i = x_i \cdot y_i$

Pi and Gi …

$$P_i = y_i + x_i$$

$$G_i = x_i \cdot y_i$$

Derive and implement the LAA

Sum and Carry out equations

$$S_i = C_i \oplus x_i \oplus y_i$$

$$C_{i+1} = C_i(x_i + y_i) + x_i y_i$$

… and the new internal Carries

$$S_i = C_i \oplus x_i \oplus y_i$$

$$C_{i+1} = C_i(x_i + y_i) + x_i y_i$$

$$P_i = x_i + y_i$$

$$G_i = x_i y_i$$

Then, $C_{i+1} = f(C_i, P_i, G_i)$ is

$S_i = C_i \oplus x_i \oplus y_i$

$C_{i+1} = C_i(x_i + y_i) + x_i y_i$

$P_i = x_i + y_i$

$G_i = x_i y_i$

$\boxed{C_{i+1} = C_i P_i + G_i}$

LAA Equations

L
A
A

$$\boxed{S_i = C_i \oplus x_i \oplus y_i}$$

$$P_i = x_i + y_i$$

$$G_i = x_i y_i$$

$$\boxed{C_{i+1} = C_i P_i + G_i}$$

Next we will derive the LAA equations for two-bits or two-stages

C_{i+1} for $i = 0, 1, 2, 3, \ldots = C_1$

L
A
A

$$C_{i+1} = C_i P_i + G_i$$

$i = 0$, $C_1 = C_0 P_0 + G_0$

C_{i+1} for $i = 0, 1, 2, 3, \ldots = C_2$

L

A

A

$C_{i+1} = C_i P_i + G_i$

$i = 0$, $C_1 = C_0 P_0 + G_0$

$i = 1$, $C_2 = C_1 P_1 + G_1$

C_{i+1} for $i = 0,1,2,3,\ldots = C_2$

L
A
A

$C_{i+1} = C_i P_i + G_i$

$i = 0,\ C_1 = C_0 P_0 + G_0$

$i = 1,\ C_2 = C_1 P_1 + G_1$

$= (C_0 P_0 + G_0) P_1 + G_1$

C_{i+1} for i = 0,1,2,3,… = C_2

L
A
A

$C_{i+1} = C_i P_i + G_i$

$i = 0,\ C_1 = C_0 P_0 + G_0$

$i = 1,\ C_2 = C_1 P_1 + G_1$

$= (C_0P_0 + G_0)P_1 + G_1$

$= C_0 P_0 P_1 + G_0 P_1 + G_1$

Expanded LAA equations

L
A
A

$C_{i+1} = C_i P_i + G_i$

$i = 0,\ C_1 = C_0 P_0 + G_0$

$i = 1,\ C_2 = C_1 P_1 + G_1$

$= (C_0 P_0 + G_0) P_1 + G_1$

$= C_0 P_0 P_1 + G_0 P_1 + G_1$

$S_i = C_i \oplus x_i \oplus y_i$

Expanded 2-bit LAA equations

L
A
A

$C_{i+1} = C_i P_i + G_i$

$C_1 = C_0 P_0 + G_0$ ← $i = 0$

$S_i = C_i \oplus x_i \oplus y_i$

$S_0 = C_0 \oplus x_0 \oplus y_0$ ← $i = 0$

Expanded 2-bit LAA equations

L
A
A

$C_{i+1} = C_i P_i + G_i$

$C_1 = C_0 P_0 + G_0$ ← $i = 0$

$C_2 = C_0 P_0 P_1 + G_0 P_1 + G_1$ ← $i = 1$

$S_i = C_i \oplus x_i \oplus y_i$

$S_0 = C_0 \oplus x_0 \oplus y_0$ ← $i = 0$

$S_1 = C_1 \oplus x_1 \oplus y_1$ ← $i = 1$

Expanded 2-bit LAA equations

L
A
A

$C_{i+1} = C_i P_i + G_i$

$P_i = x_i + y_i$

$C_1 = C_0 P_0 + G_0$ ← i = 0 → $P_0 = x_0 + y_0$

$C_2 = C_0 P_0 P_1 + G_0 P_1 + G_1$ ←

$S_i = C_i \oplus x_i \oplus y_i$

$G_i = x_i y_i$

$S_0 = C_0 \oplus x_0 \oplus y_0$ ← i = 0 → $G_0 = x_0 y_0$

$S_1 = C_1 \oplus x_1 \oplus y_1$ ←

Expanded 2-bit LAA equations

LAA

$C_{i+1} = C_i P_i + G_i$

$P_i = x_i + y_i$

$C_1 = C_0 P_0 + G_0$ ⟵ $i = 0$ → $P_0 = x_0 + y_0$

$C_2 = C_0 P_0 P_1 + G_0 P_1 + G_1$ ⟵ $i = 1$ → $P_1 = x_1 + y_1$

$S_i = C_i \oplus x_i \oplus y_i$

$G_i = x_i y_i$

$S_0 = C_0 \oplus x_0 \oplus y_0$ ⟵ $i = 0$ → $G_0 = x_0 y_0$

$S_1 = C_1 \oplus x_1 \oplus y_1$ ⟵ $i = 1$ → $G_1 = x_1 y_1$

2-bit LAA equations

L
A
A

$C_1 = C_0 P_0 + G_0$

$C_2 = C_0 P_0 P_1 + G_0 P_1 + G_1$

$S_0 = C_0 \oplus x_0 \oplus y_0$

$S_1 = C_1 \oplus x_1 \oplus y_1$

$P_0 = x_0 + y_0$

$P_1 = x_1 + y_1$

$G_0 = x_0 y_0$

$G_1 = x_1 y_1$

2-bit LAA equations; both stages

L
A
A

$C_1 = C_0 P_0 + G_0$

$C_2 = C_0 P_0 P_1 + G_0 P_1 + G_1$

$S_0 = C_0 \oplus x_0 \oplus y_0$

$S_1 = C_1 \oplus x_1 \oplus y_1$

$P_0 = x_0 + y_0$

$P_1 = x_1 + y_1$

$G_0 = x_0 y_0$

$G_1 = x_1 y_1$

Implement

First stage

L
A
A

$C_1 = C_0 P_0 + G_0$

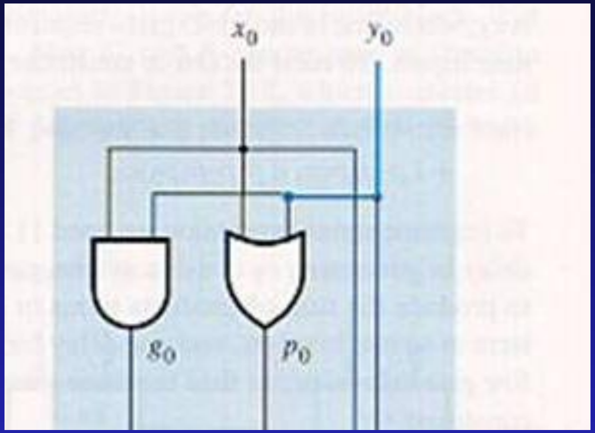
$S_0 = C_0 \oplus x_0 \oplus y_0$

$P_0 = x_0 + y_0$

$G_0 = x_0 y_0$

Implement

1-bit LAA @ CRA (same)



$p_0 = x_0 + y_0$

$g_0 = x_0\, y_0$

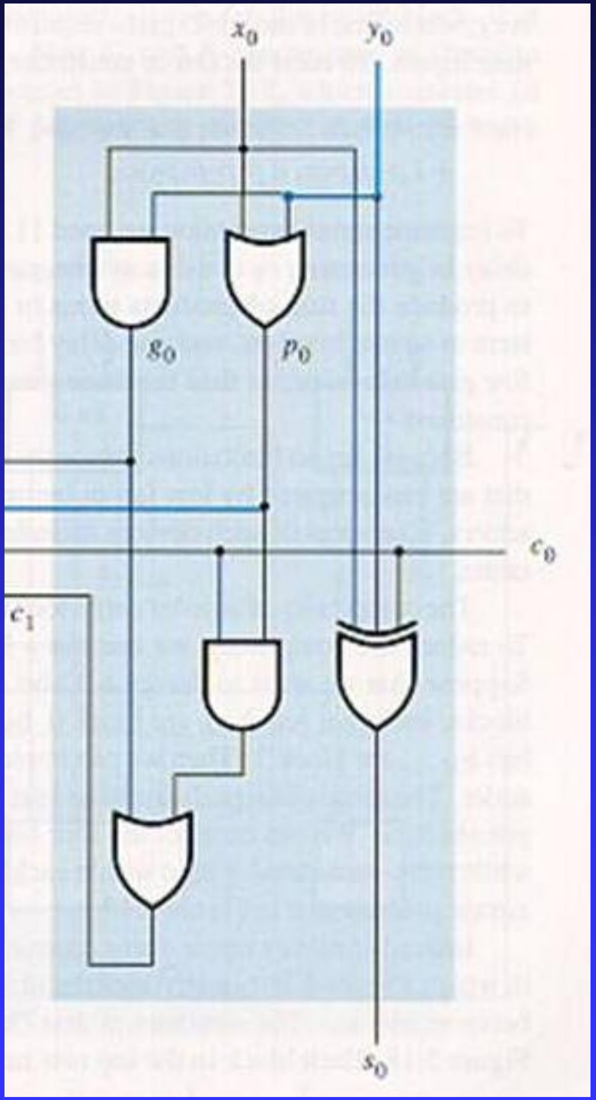
1-bit LAA @ CRA (same)

$c_1 = c_0 p_0 + g_0$

$S_0 = c_0 \oplus x_0 \oplus y_0$

$p_0 = x_0 + y_0$

$g_0 = x_0 y_0$



Second stage

L
A
A

$c_2 = c_0 p_0 p_1 + g_0 p_1 + g_1$

$s_1 = c_1 \oplus x_1 \oplus y_1$

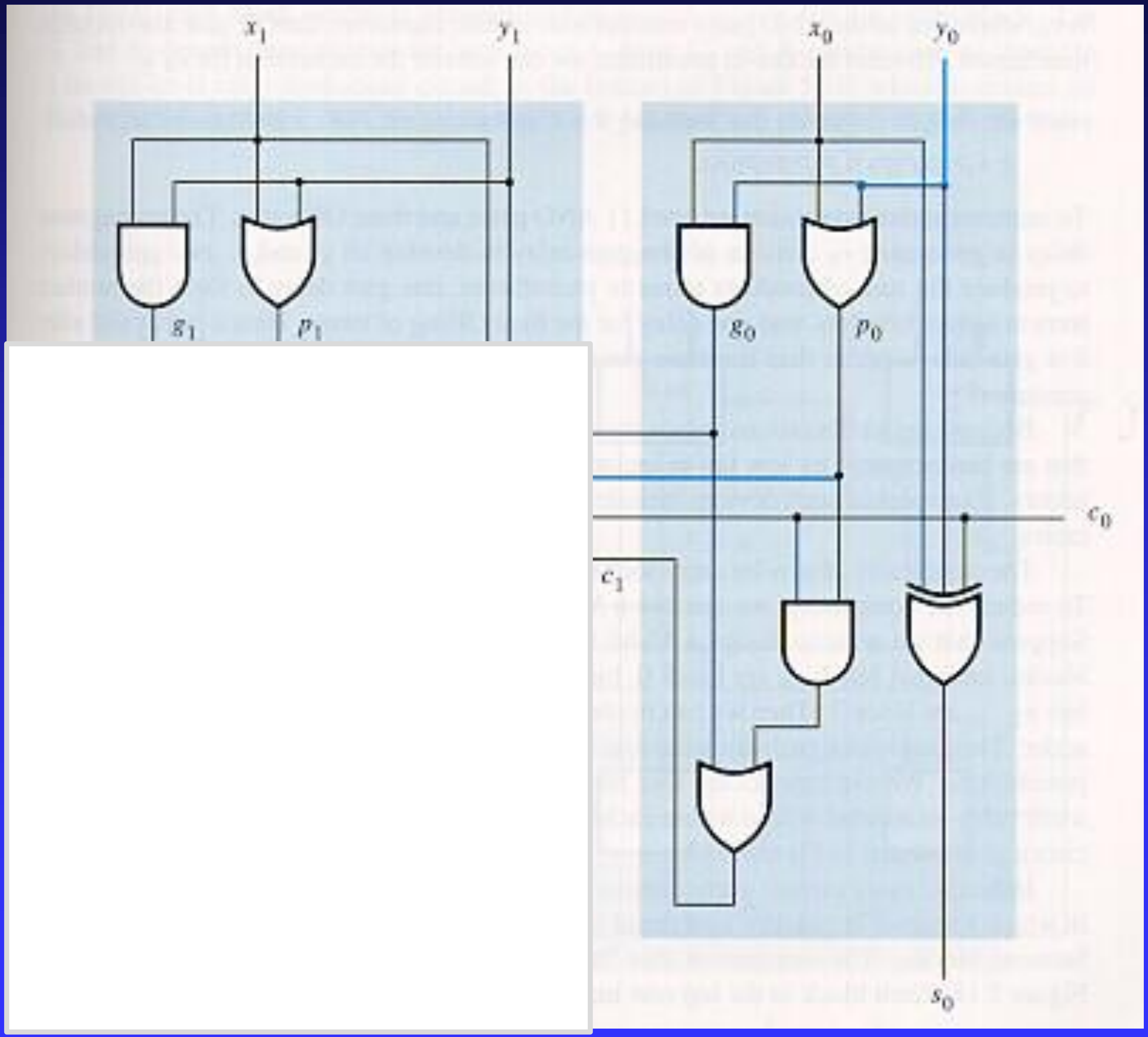
$p_1 = x_1 + y_1$

$g_1 = x_1 y_1$

Implement

2-bit

LAA



$g_1 = x_1 \, y_1$

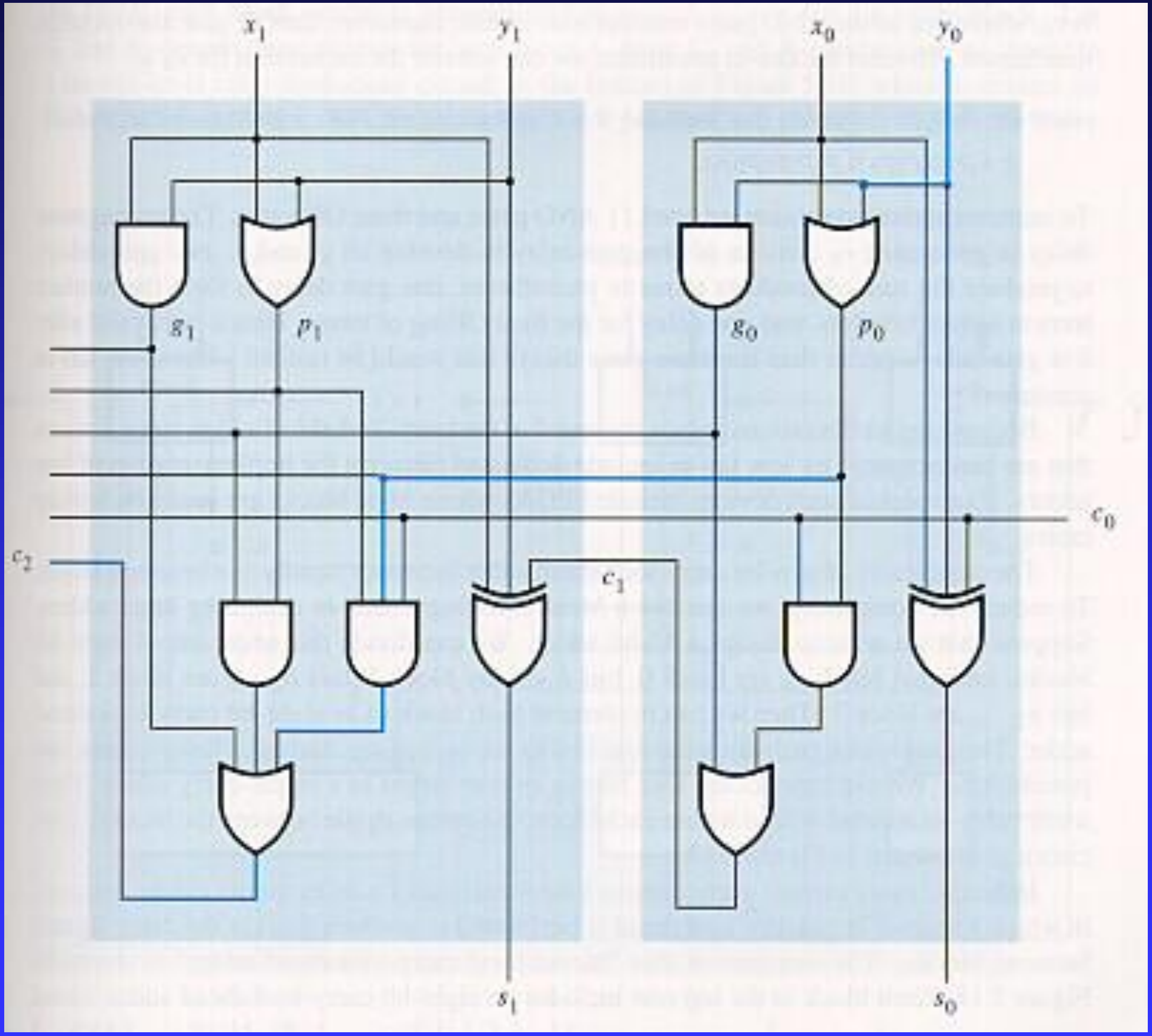
$p_1 = x_1 + y_1$

2-bit

L A A

$s_1 = c_1 \oplus x_1 \oplus y_1$

$c_2 = c_0\, p_0\, p_1 + g_0\, p_1 + g_1$



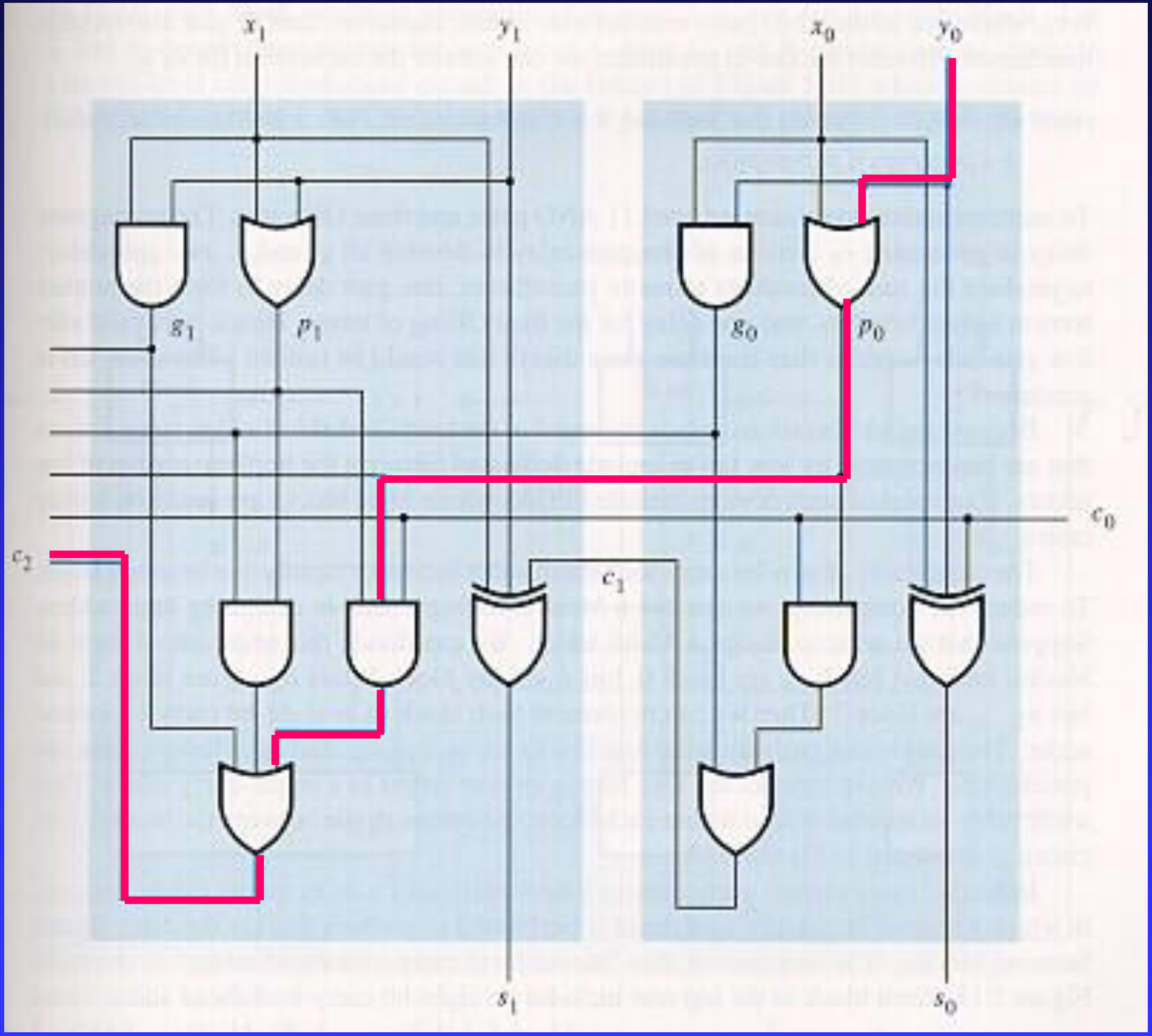
$g_1 = x_1\, y_1$

$p_1 = x_1 + y_1$

y_0 ... C_2 - the longest path ...

2-bit

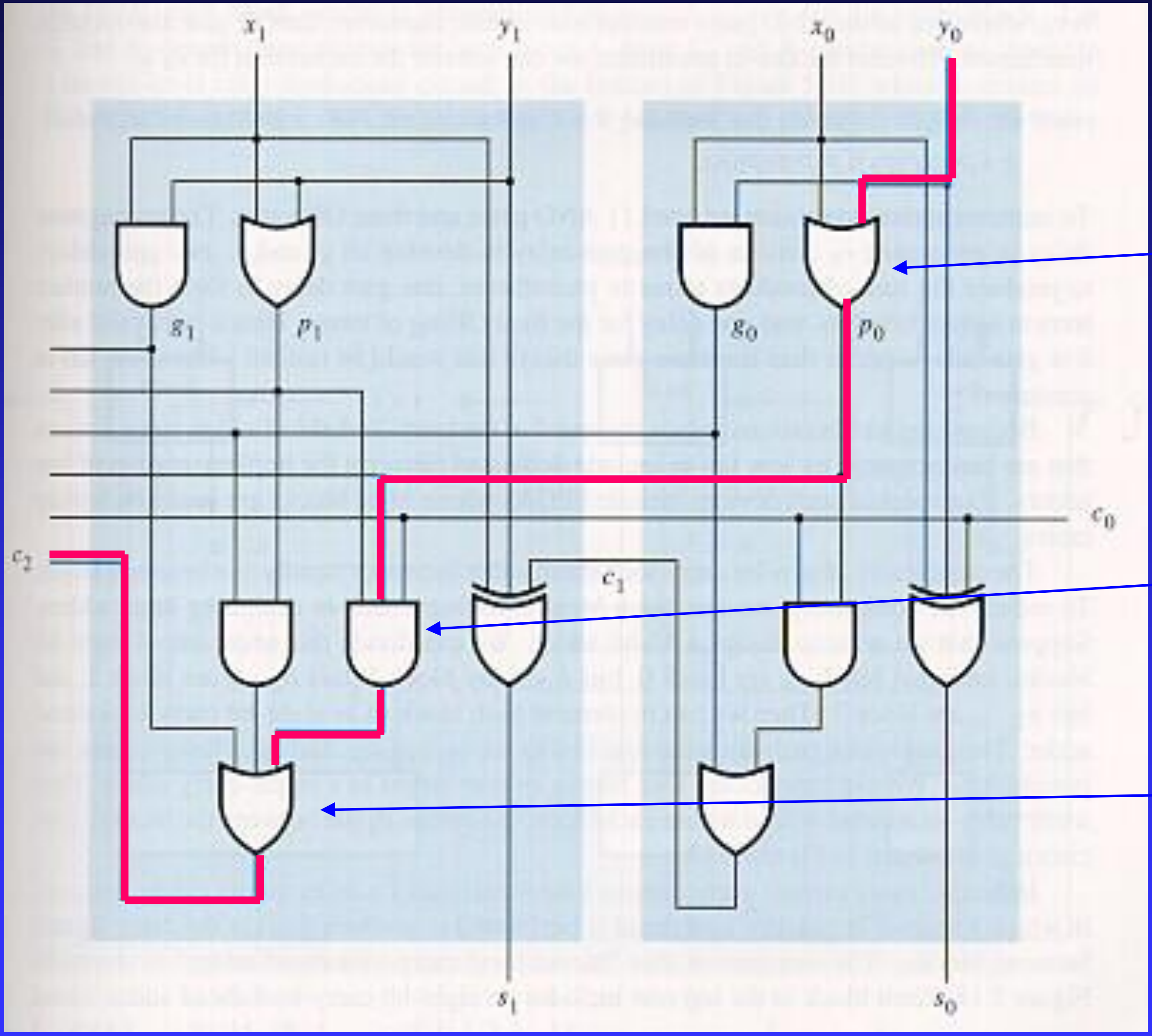
C
R
A



y_0 ... c_2 = 8 nsec

2-bit

C
R
A



2.4

+

2.8

+

2.8

=

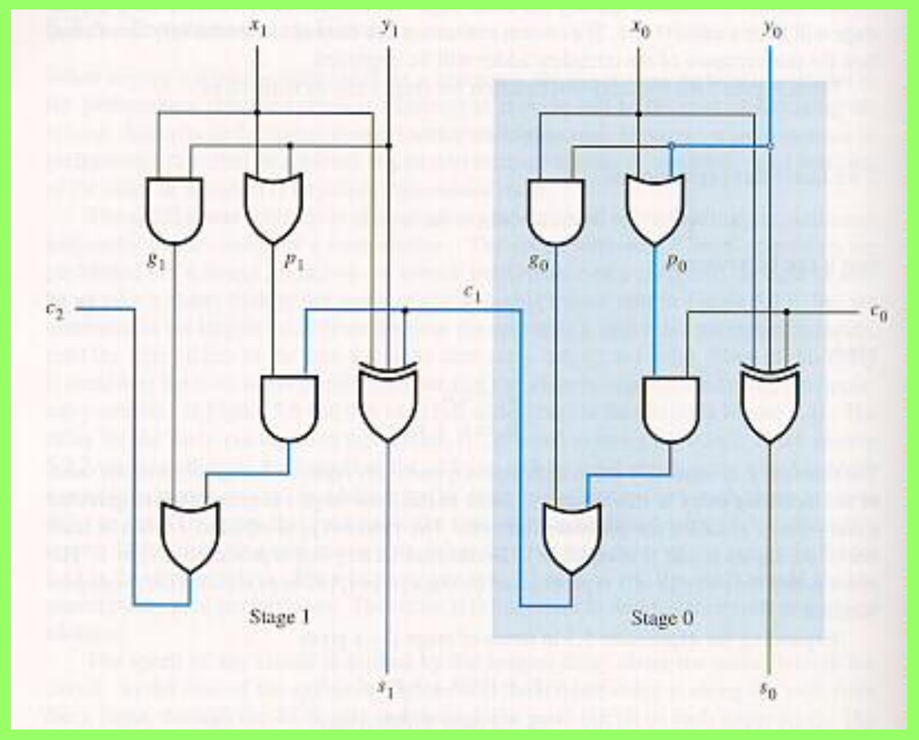
8.0

Comparison → 33.3%

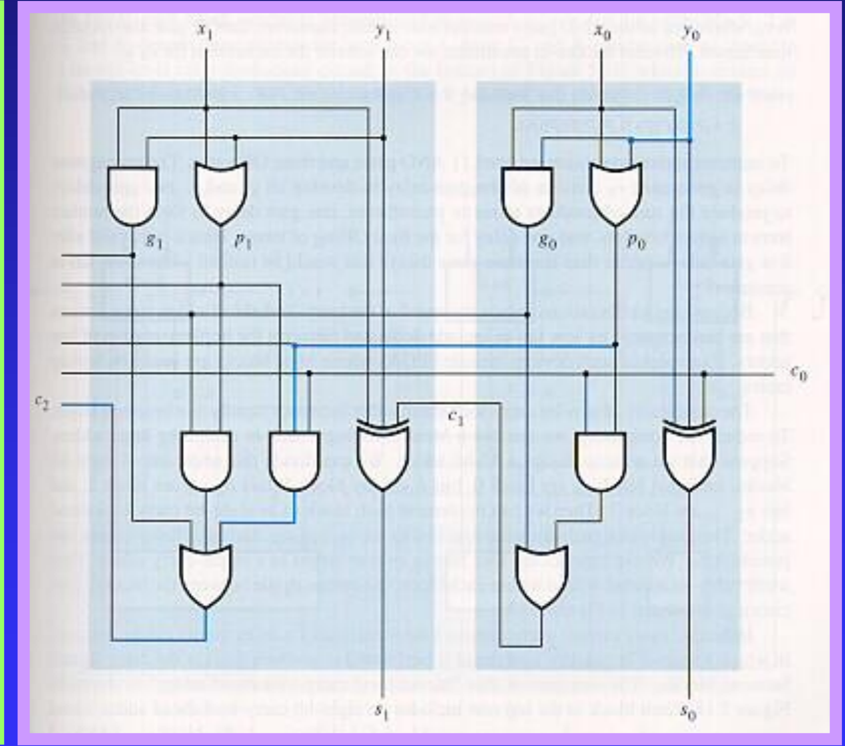
2-bit Carry-Ripple Adder	= 12 nsec
2-bit Look-Ahead Carry Adder	= 8 nsec

LAA has an extra gate than CRA; but LAA is 33.3% faster than CRA

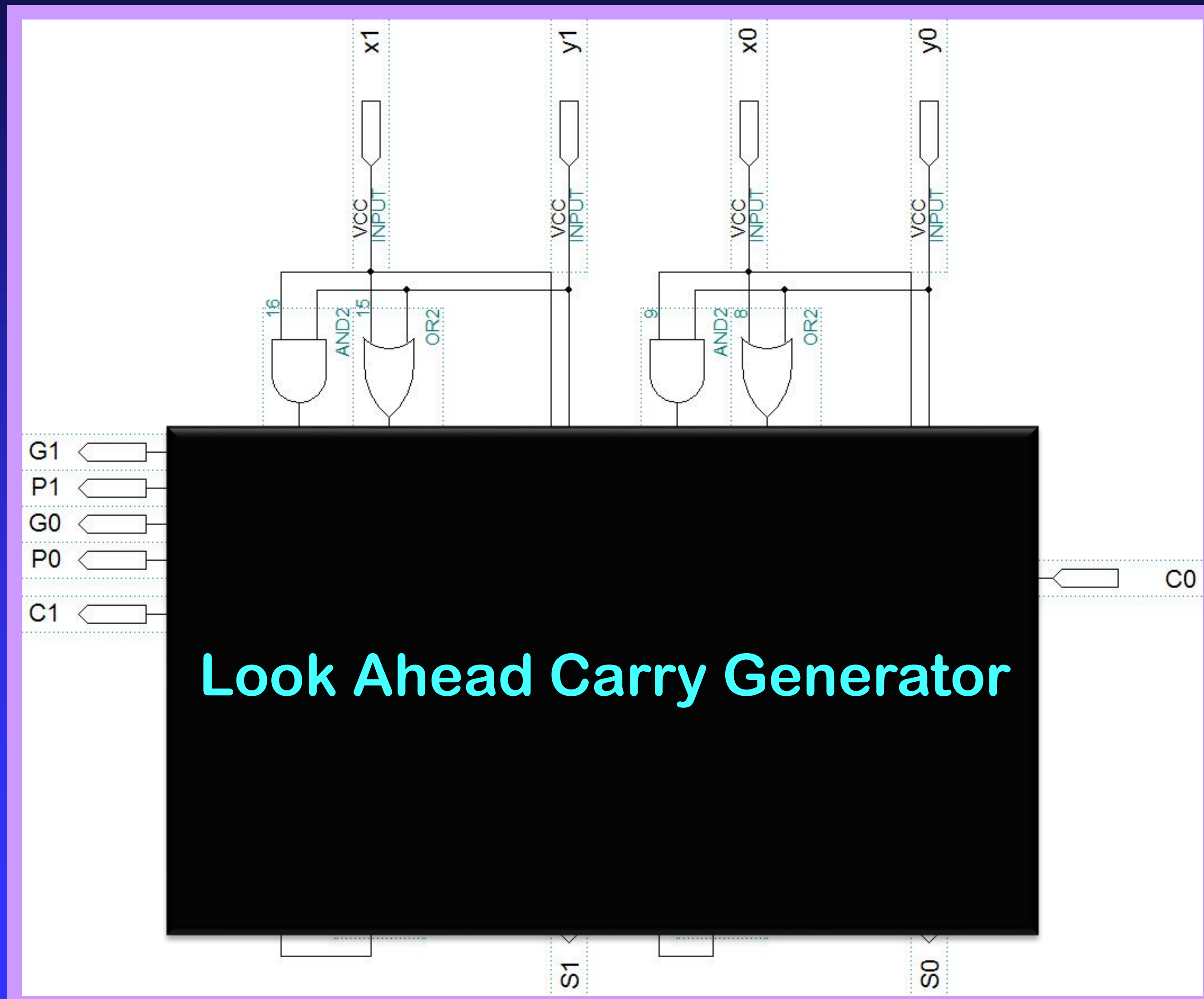
CRA



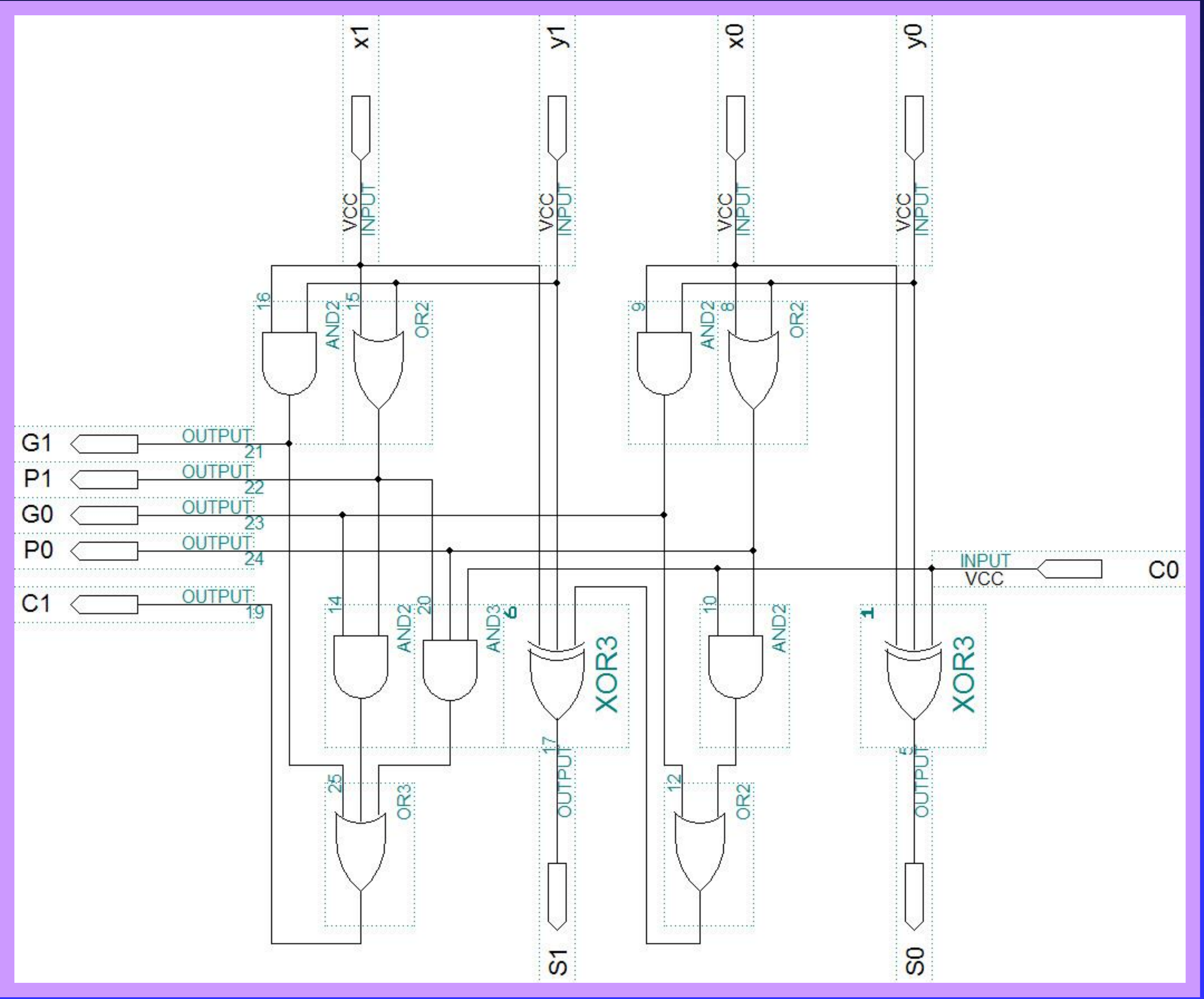
LAA



VHDL … LAA


x1
y1
x0
y0
VCC
INPUT
VCC
INPUT
VCC
INPUT
VCC
INPUT
16
AND2
15
OR2
9
AND2
8
OR2
G1
P1
G0
P0
C1
C0
Look Ahead Carry Generator
S1
S0

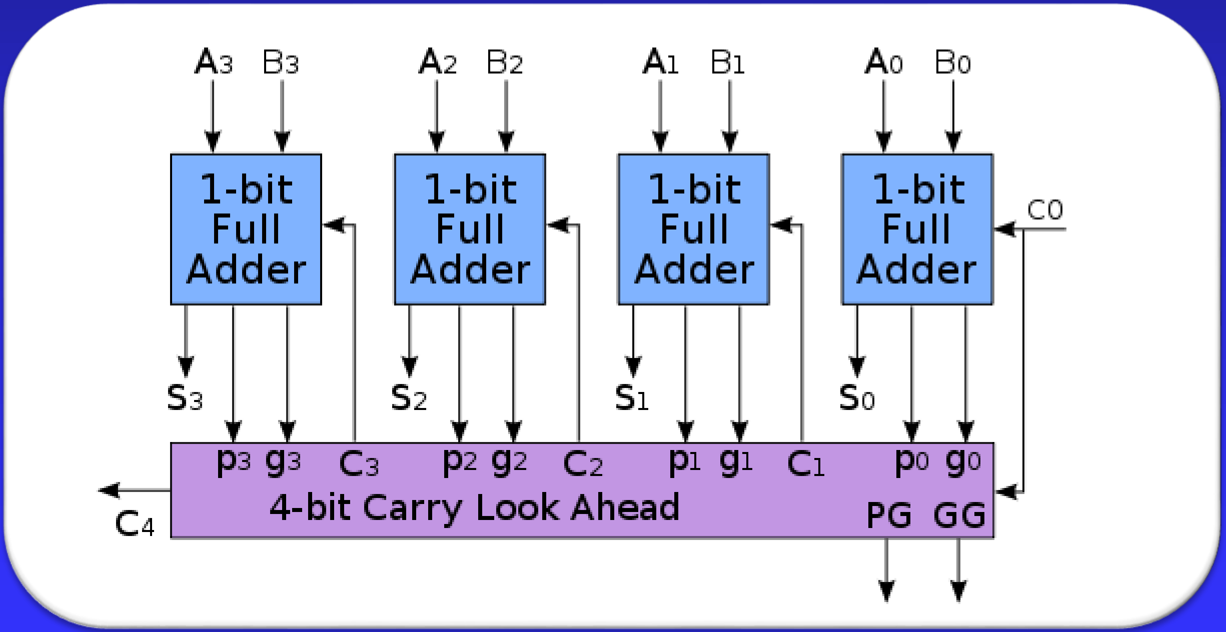
VHDL … LAA



x1
y1
x0
y0
VCC
INPUT
AND2
OR2
G1
P1
G0
P0
C1
OUTPUT
INPUT
VCC
C0
AND3
XOR3
S1
S0

LAA limitation ..

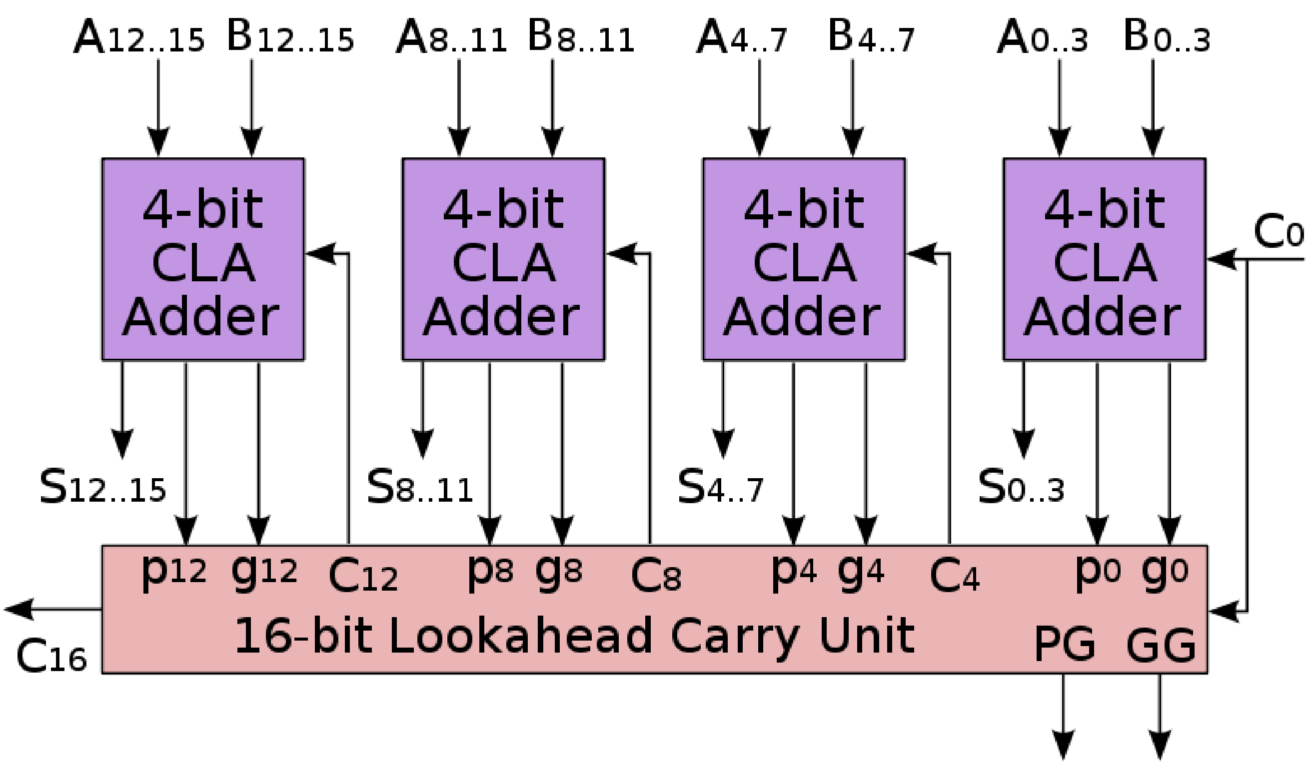
- LAA cannot go beyond 4 bits of look-ahead



http://www.online-utility.org/image/gallery.jsp?title=Computer+diagrams

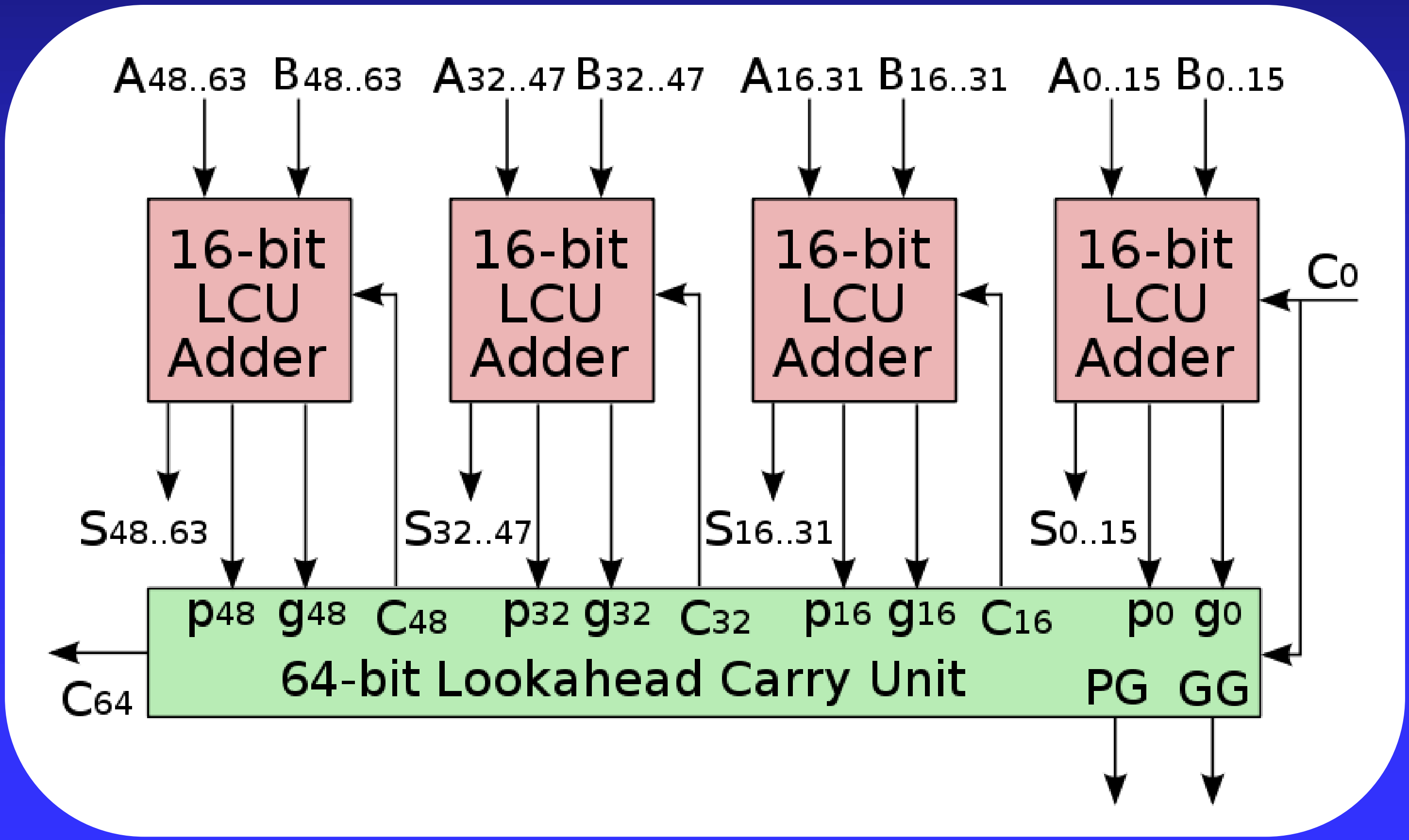
16-bit LAA

- For a 16bit LAA, 4x4 LAA's should be used



64-bit LAA

- For a 64 bit LAA, 16x4 LAA's should be used



Adder part of the ALU

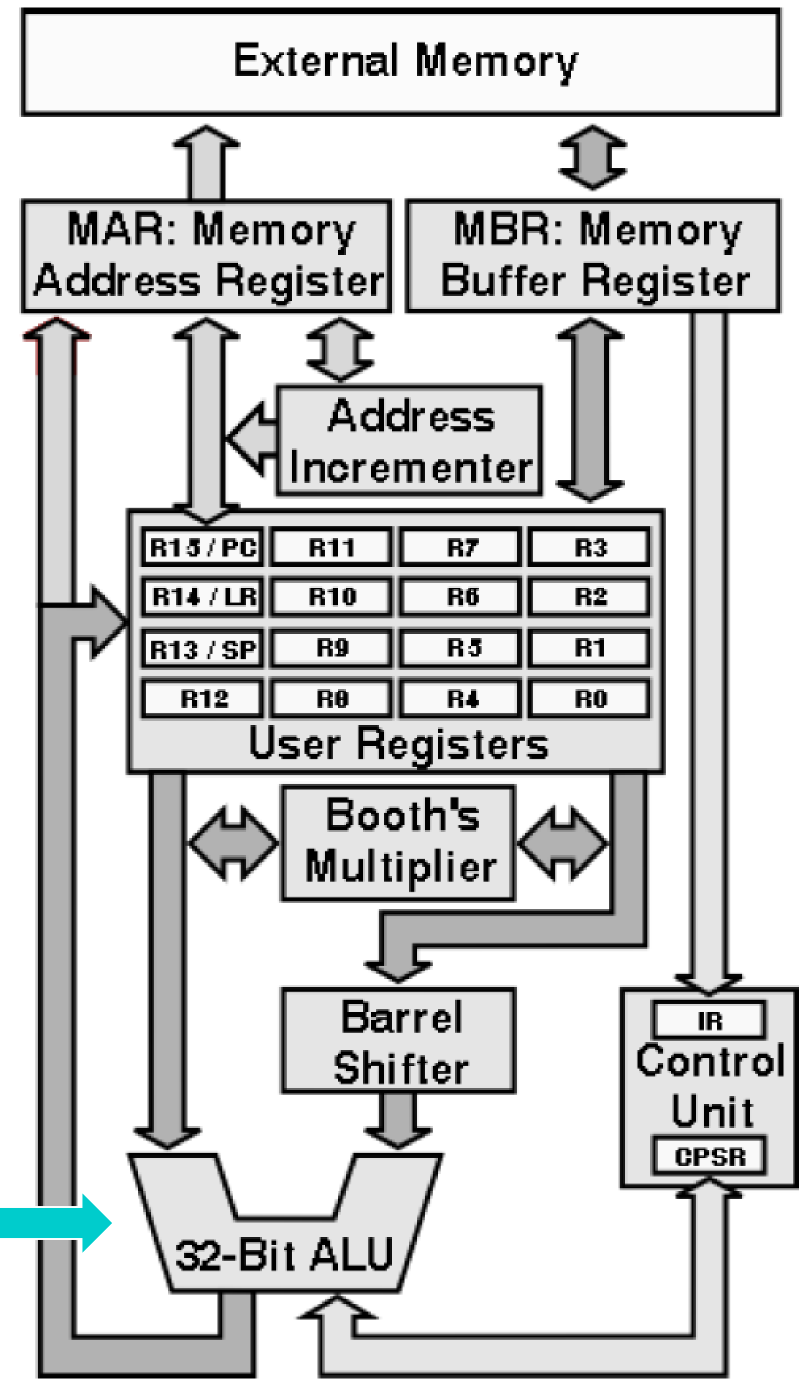


fig 1.1 ARM Block Diagram

We will design ALU's