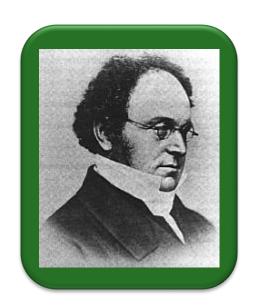


Binary Logic → continue

DeMorgan Theorems



Augustus DeMorgan (1806-1871)



British mathematician born in India

DeMorgan's theorems

•
$$\overline{x+y} = \overline{x} \cdot \overline{y}$$

•
$$\overline{x \cdot y} = \overline{x + y}$$

- breaking the bar changes the logic operation (OR) under the bar
- breaking the bar changes the logic operation (AND) under the bar

Proof of the DeMorgan's theorem

Proof of the DeMorgan's theorem

X	у	X	y	ху	ху	<u>_</u> x+y	x y	x + y	${x + y}$
0	0								
0	1								
1	0								
1	1								

Proof of the DeMorgan's theorem

X	у	X	y	ху	ху	<u>_</u> x+ <u>y</u>	x y	x + y	${x + y}$
0	0	1	1	0					
0	1	1	0	0					
1	0	0	1	0					
1	1	0	0	1					

Proof of the first DeMorgan's theorem

X	у	X	$\left \frac{}{y} \right $	ху	ху	<u>_</u> x+y	<u></u>	x + y	${x + y}$
0	0	1	1	0	1	1			
0	1	1	0	0	1	1			
1	0	0	1	0	1	1			
1	1	0	0	1	0	0			

Proof of both DeMorgan's theorems

X	у	X	$\left \frac{}{y} \right $	ху	ху		<u></u>	x + y	${x + y}$
0	0	1	1	0	1	1	1	0	1
0	1	1	0	0	1	1	O	1	0
1	0	0	1	0	1	1	O	1	0
1	1	0	0	1	0	0	0 _	1	$oxed{0}$

Perfect Induction

Example: Using DeMorgan's

$$\overline{AB+C}$$

First application of the theorem

$$\overline{AB} + C = \overline{AB}C$$

Second application of theorem

$$\overline{A} \, \overline{B} + C = A \, \overline{B} \, \overline{C}$$

$$= (\overline{A} + \overline{B}) \, \overline{C}$$

Distribute...

$$\overline{AB} + \overline{C} = \overline{ABC}$$

$$= (\overline{A} + \overline{B}) \overline{C}$$

$$= (\overline{A} + B) \overline{C}$$

$$= (\overline{A} + B) \overline{C}$$

$$= \overline{AC} + B \overline{C}$$

Sum-of-products form

$$\overline{AB} + C = A\overline{B}\overline{C}$$

$$= (\overline{A} + \overline{B})\overline{C}$$

$$= (\overline{A} + B)\overline{C}$$

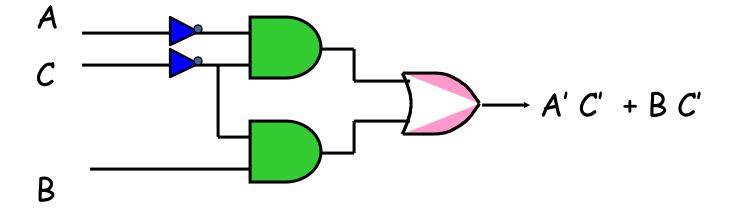
$$= \overline{AC} + B\overline{C}$$

Implement with gates

Sum-of-Products form

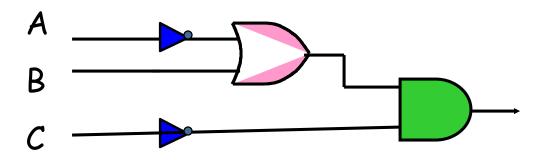
Ready to see the circuit?

The SOP leads to "two-level-realization"

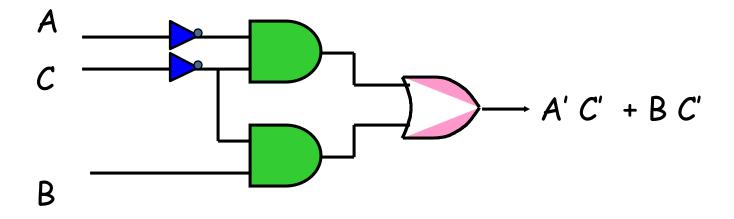


factor ... "multi-level-realization"

$$A' C' + B C' = C'(A'+B)$$



Fun-in & Fan-out



Fan-in: max number of inputs a gate can accept

Fan-out: max number of inputs a gate can drive

More gates....

More Gates

- NOR (Not OR)
- NAND (Not AND)

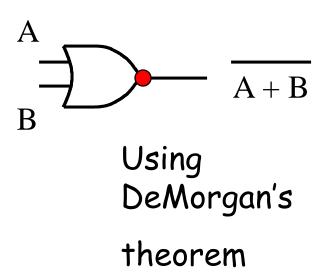
OR

Α	В	OR	NOR
0	0	0	
0	1	1	
1	0	1	
1	1	1	

NOR

Α	В	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

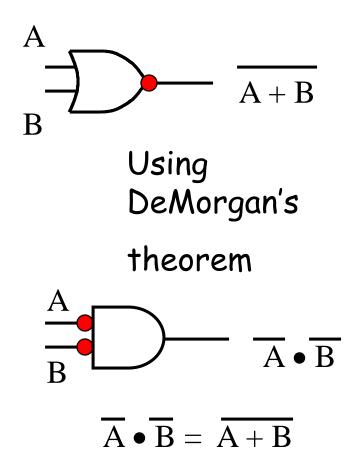
NOR



Α	В	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

•
$$\overline{x+y} = \overline{x} \cdot \overline{y}$$

NOR



Α	В	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

AND ... Not AND

Α	В	AND	NAND
0	0	0	
0	1	0	
1	0	0	
1	1	1	

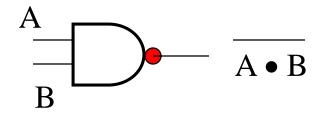


NAND

Α	В	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



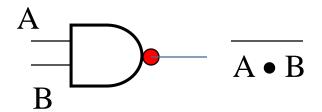
NAND



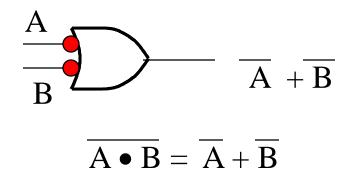
Using DeMorgan's theorem

Α	В	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

NAND

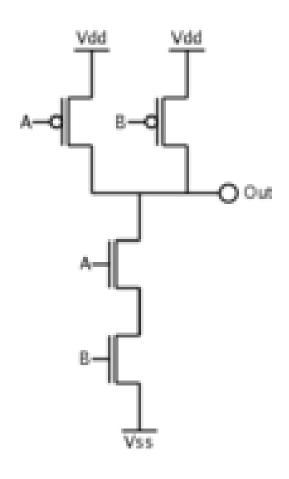


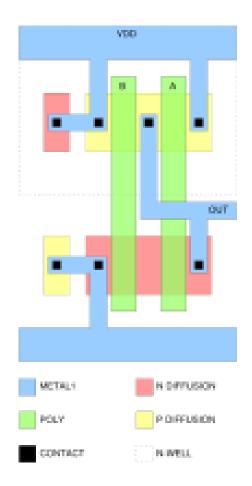
Using DeMorgan's theorem



Α	В	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

NAND: CMOS and gate layout





Universality of NAND and NOR Gates

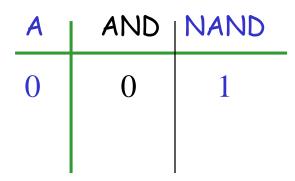
...can implement any Boolean expression

Universality of NAND: NOT



Proof





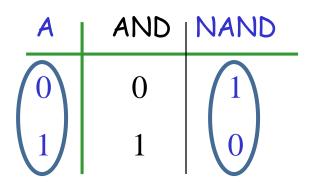
Proof



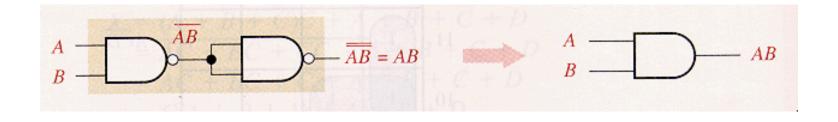
Α	AND	NAND
0	0	1
1	1	0

Proof

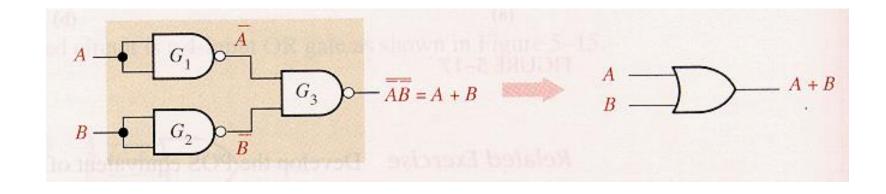




Universality of NAND: AND

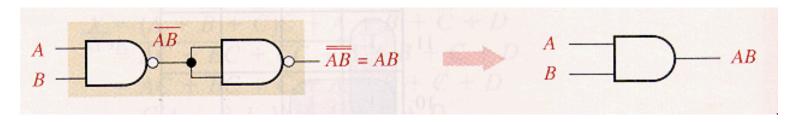


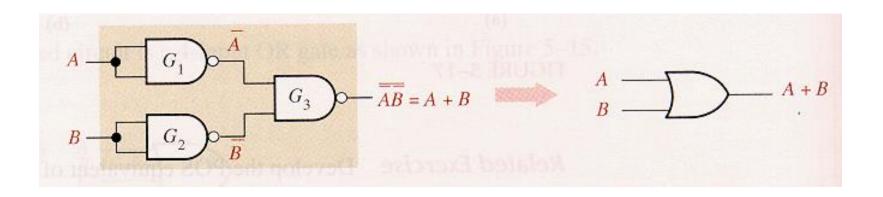
Universality of NAND: OR



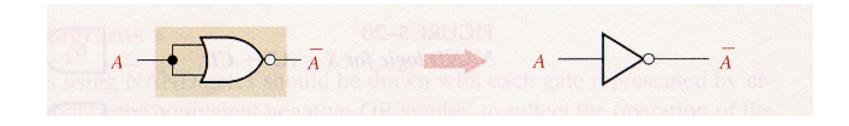
All



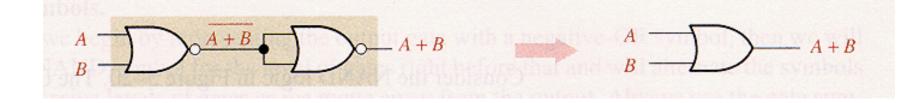




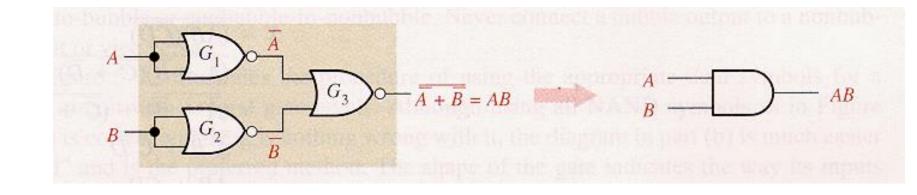
Universality of NOR: NOT



Universality of NOR: OR



Universality of NOR: AND



Example: implement (two-level-realization) the

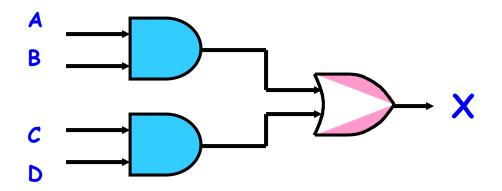
Boolean function: X = AB + CD, using:

- 1. AND, OR gates
- 2. NAND gates

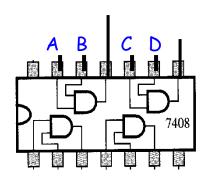
You have ...5 minutes ...

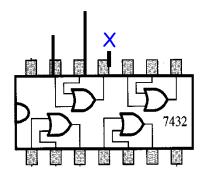
GEA

1) X = AB + CD; Using AND, OR gates

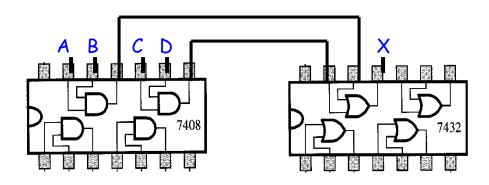


X = AB + CD; Using Chips





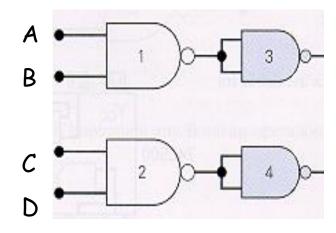
X = AB + CD; Using Chips

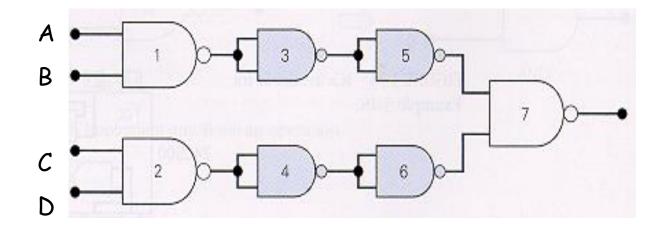


A

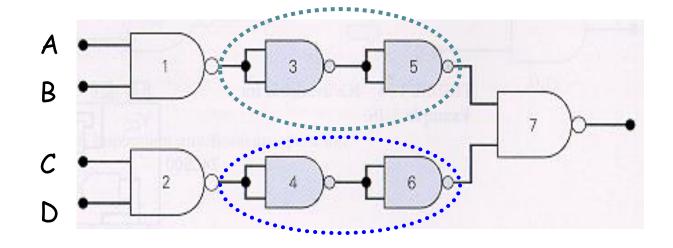
B

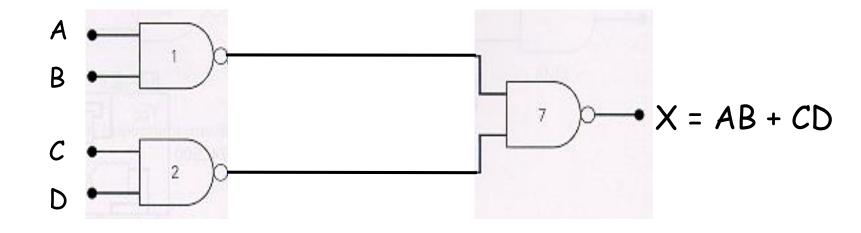
D



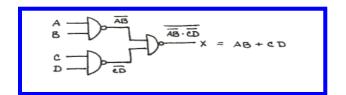


Two inverts cancel each other



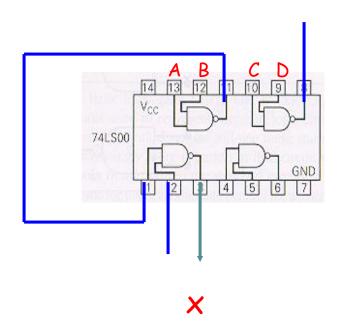


Note: 2 inverts in series cancel each other

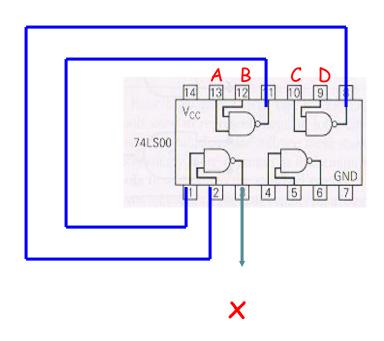


Proof

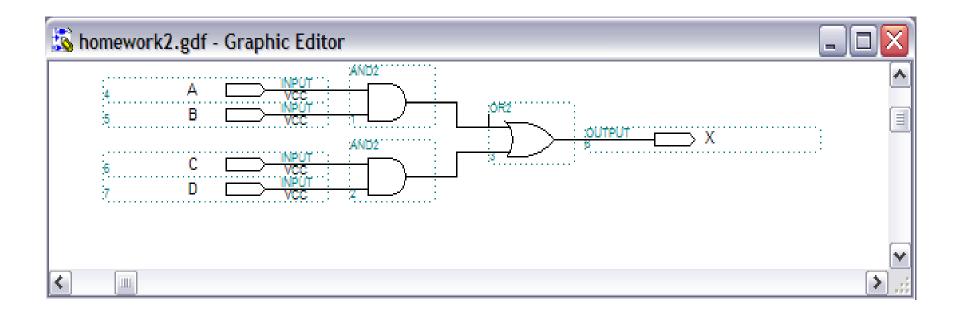
X = AB + CD; Using NAND chips



X = AB + CD; Using NAND chips



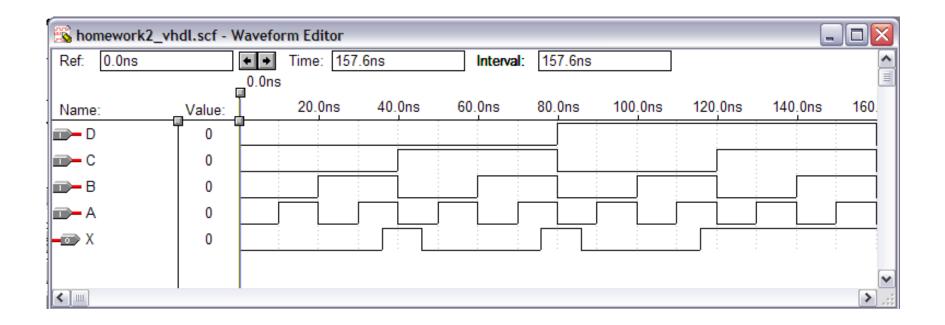
X = AB + CD; Using VHDL



VHDL Code: X = AB + CD

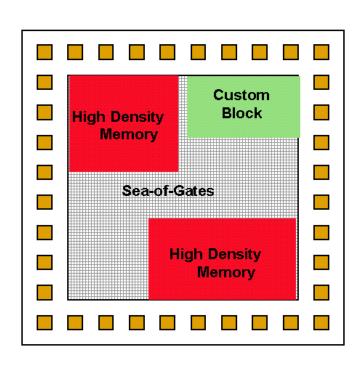
```
nomework2_vhdl.vhd - Text Editor
  entity homework2 vhdl is
       port (a,b,c,d: in bit;
              x: out bit);
  end homework2_vhd1;
  architecture dataflow of homework2_vhdl is
  begin
       x \le (a \text{ and } b) \text{ or } (c \text{ and } d);
  end dataflow;
                   24
                           INS 🗀 🕕
 Line
             Col
```

Waveform



An array with many NAND gates

Sea-of-Gates Array Technology



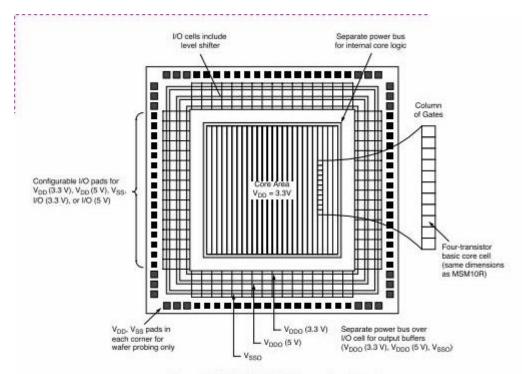
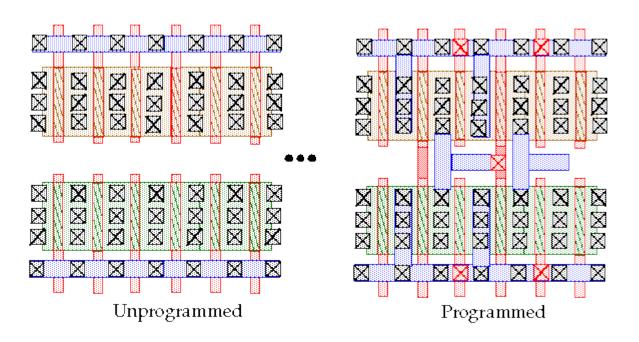


Figure 7. MSM13R0000 Array Architecture

An array with many NAND gates

Sea-of-Gates Array Technology



... two more gates

- ✓ XOR
- ✓ XNOR



OR gate

Α	В	OR gate
0	0	0
0	1	1
1	0	1
1	1	1

XOR (eXclusiveOR) gate

Α	В	OR gate	XOR gate
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

XOR (eXclusiveOR) gate



Α	В	OR gate	XOR gate
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

$$A \times B = A \oplus B$$
$$= \overline{A}B + A\overline{B}$$

It produces a high output whenever the two inputs are at opposite levels

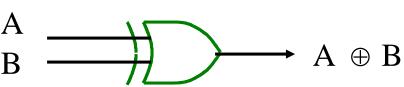
XOR (eXclusiveOR) gate

Α	В	OR gate	XOR gate
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

$$A \times B = A \oplus B$$

$$= \overline{A}B + \overline{A}B$$

It produces a high output whenever the two inputs are at opposite levels



Another gate ... XNOR

 $A \oplus B = ?$

XNOR (eXclusiveNOR) gate

Α	В	XOR gate	XNOR gate
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

0

XNOR (eXclusiveNOR) gate



Α	В	XOR gate	XNOR gate
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

$$A \times B = \overline{A} \oplus B$$

$$= \overline{A} \overline{B} + A B$$

0

