CURRÍCULUM VÍTAE NORMALIZADO

Paul Carpenter

Generated from: Editor CVN de FECYT

Date of document: 12/08/2016

v 1.4.0

b905b70190c71d0a9f35865a8911703d

This electronic file (PDF) has embedded CVN technology (CVN-XML). The CVN technology of this file allows you to export and import curricular data from and to any compatible data base. List of adapted databases available at: http://cvn.fecyt.es/

GOBIERNO DE ESPAÑA
MINISTERIO DE ECONOMÍA Y COMPETITIVIDAD

FECYT FUNDACIÓN ESPAÑOLA PARA LA CIENCIA Y LA TECNOLOGÍA

Summary of CV

This section describes briefly a summary of your career in science, academic and research; the main scientific and technological achievements and goals in your line of research in the medium -and long- term. It also includes other important aspects or peculiarities.

I am an established academic researcher active in high-performance computing (HPC), specifically parallel programming models, system software support for inter-node resource sharing, and interconnect energy efficiency. My research career comprises eight years in industrial research and development at ARM, a PhD in Computer Architecture from Universitat Politècnica de Catalunya (UPC), and four years in academic research: three at UPC and one at Barcelona Supercomputing Center (BSC).

I am co-chair of Programming Environment in ETP4HPC, EC's partner in the HPC Contractual Public-Private Partnership (CPPP). I am also member of the editorial team of Rethink Big, an FP7 project producing a roadmap for the EC, relating to hardware acceleration for big data. Finally, I am Leader of the Research Work Package (WP) in EuroLab-4-HPC. This WP involves supporting inter-disciplinary research visits across Europe, mentoring European researchers in technology transfer, and preparing a roadmap for academic HPC research excellence.

I am Principal Investigator of EUROSERVER, an EC FP7 project with €1.1M and 137 PMs at BSC, and leader of WP3 "Enablement of Software Compute Node" in EXANODE, an EC FP7 project with €444k and 87 PMs at BSC. I am (co-)advisor of 5 PhD students (one already graduated Excel·lent cum Laude), plus manager of one engineer. My research lines, which grew out of my industrial research experience, have led to 31 papers, of which 7 are in CORE A/A+ conferences, including MICRO 2012, SC 2013 (Best Student Paper), and IEEE Transactions in Computers (Featured Article of the Month).

At ARM, I was technical lead and/or project manager for several successful embedded software products. I was a core member of the multi-disciplinary team that designed ARM Advanced SIMD, implemented in almost 50% of all mobile phones worldwide, and principal researcher on 3 international granted patents. I have further experience of commercialisation and entrepreneurship as author of a commercially available video game, founder of a successful software consulting company, and co-founder of Talaia Systems, which was finalist in Fundación Repsol Entrepreneurship Fund 2013.

General quality indicators of scientific research

This section describes briefly the main quality indicators of scientific production (periods of research activity, experience in supervising doctoral theses, total citations, articles in journals of the first quartile, H index...). It also includes other important aspects or peculiarities.

I received my PhD in Computer Architecture from Universitat Politècnica de Catalunya in 2011 (Excel·lent cum Laude). My publication record is:
- Total publications: 31
- Papers in international CORE A ranked conferences: 7 [*], including MICRO 2012, SC 2013
- Citations: 195 (Google Scholar)
- H-index: 6 (Google Scholar)
- i10-index: 5 (Google Scholar)
- Google Scholar: https://scholar.google.es/citations?hl=en&user=V9UomEgAAAAJ

I have the following awards directly related to my scientific output:
- IEEE Transactions on Computers (impact factor 1.659) Featured Paper of the Month (1 of 28 papers published)
- Best Student Paper Award at SC'13 (Microsoft Research h-index 81)
- Candidate Best Paper at IEEE LCN 2015
- HiPEAC Paper Award 2012

I have demonstrated strong impact and leadership in EC high-performance computing strategy:
- Co-chair of Programming Environment in ETP4HPC
- Member of the editorial team of Rethink Big
- Leader of the Research Work Package in EuroLab-4-HPC

I am manager of one engineer, and (co-)advisor of 5 PhD students:
- Karthikeyan Saravanan, “Energy Optimisations in Interconnects for HPC”, started Q3 2011 (co-advisor).
- Branimir Dickov, "MPI Layer Techniques to Improve Network Energy Efficiency”, started Q1 2009, graduated 10/12/2015 (Excel·lent cum Laude).
- Renan Fischer e Silva, "Interconnect Energy Savings on Microserver Workloads", started Q1 2014 (advisor).
- Luis Garrido, "Virtualisation Techniques for the Exploitation of Resources Across Coherence Islands", started Q2 2014 (co-advisor).
- Ugljesa Milic, "Multicore Architecture Optimization for HPC Applications", started 2013 (co-advisor).

I am also active in research exploitation, as co-founder of BSC spin-off Talaia Systems, which was finalist in Fundación Repsol Entrepreneurship Fund 2013, as well as research dissemination through 10 invited talks and 2 videos. I attracted research funding as single BSC contact for EUROSERVER since the beginning of the proposal writing stage (€1.1M and 137 PMs at BSC). Since 2014, I am the Principal Investigator of EUROSERVER, and since 2016, I am the Principal Investigator of EXANODE.

I was engaged in industrial research at ARM Research Group, Cambridge, for the period 2003—2005. In this time, I was part of the small multi-disciplinary team (<5 people) that designed ARM Advanced SIMD. Advanced SIMD has been successfully exploited, as it is used in close to 50% of all mobile phones worldwide.

I am principal researcher and first author on 3 international granted patents.

---

[*] In computer systems, the top international conferences use a rigorous review process with 3 to 7 reviews per paper and acceptance rates of 15% to 25%. Journal publications are archives for updated and extended versions of conference publications. The respected CORE ranking: A* (flagship conference, leading venue in a discipline), A (excellent conference, highly respected in a discipline), B (good conference, well regarded in a discipline) and C (meets minimum standards).

Paul Carpenter

Surname(s):	**Carpenter**
Name:	**Paul**
DNI:	**X7531222X**
ORCID:	**orcid.org/0000-0002-9392-0521**
ResearcherID:	**C-3790-2012**
Date of birth:	**25/10/1974**
Gender:	**Male**
Nationality:	**United Kingdom**
Country of birth:	**United Kingdom**
Aut. region/reg. of birth:	**Gloucestershire, Wiltshire and North Somerset**
Contact province:	**Barcelona**
City of birth:	**Bristol**
Contact address:	**Barcelona Supercomputing Center**
Rest of contact address:	**c/ Jordi Girona 31**
Postcode:	**08034**
Contact country:	**Spain**
Contact aut. region/reg.:	**Catalonia**
Contact city:	**Barcelona**
Land line phone:	**(+34) 934137735**
Email:	**paul.carpenter@acm.org**
Mobile phone:	**(+34) 722513230**
Personal web page:	**www.paul-carpenter.org**

Current professional situation

Employing entity: Barcelona Supercomputing Center

Type of entity: R&D Centre

Department: Barcelona Supercomputing Center

Professional category: Senior Researcher

Educational Management (Yes/No): No

City employing entity: Barcelona, Spain

Start date: 01/09/2014

Dedication regime: Full time

Performed tasks: Leading Microserver Architectures and System Software team, which focusses on (a) hypervisor support for programming model abstractions and coherence islands, (b) interconnect requirements, topology and energy proportionality for new system architectures with coherence islands, (c) interconnect energy proportionality for HPC workloads on Ethernet and InfiniBand, and (d) performance and energy evaluation of data centre workloads on prototype hardware. Principal Investigator (PI) for FP7 Euroserver Project (137 PMs at BSC). Director / codirector for five PhD students, and managing one engineer. Member of European Exascale Software Initiative 2 (EESI 2) Working Group on Energy Efficiency. Co-chair of Working Group on Programming Models in EXDCI and the European Technology Platform for High Performance Computing (ETP4HPC) for the 2015 update of the Strategic Research Agenda. ETP4HPC is the main organisation that represents the whole HPC industry and academic within Europe (now 69 members). WP leader for Eurolab-4-HPC WP2 Research. Member of Editorial Team for Rethink Big. Reviewer for Microprocessors and Microsystems (2016). Member of three PhD predefence committees. External reviewer on one PhD thesis.

Applicability in teaching and/or research: PI of FP7 Euroserver project (137 PMs at BSC). Director or codirector for five PhD students: * Karthikeyan Saravanan, "Energy Optimisations in Interconnects for HPC", started Q3 2011 (coadvisor), * Branimir Dickov, "MPI Layer Techniques to Improve Network

Energy Efficiency", started Q1 2009, graduated 10/12/2015 (Excel·lent cum Laude), * Renan Fischer e Silva, "Interconnect Energy Savings on Microserver Workloads", started Q1 2014 (advisor), Luis Garrido, "Virtualisation Techniques for the Exploitation of Resources Across Coherence Islands", started Q2 2014 (coadvisor), Ugljesa Milic, "Multicore Architecture Optimization for HPC Applications", started 2013 (coadvisor).

Previous positions and activities

	Employing entity	Professional category	Start date
1	Universitat Politècnica de Catalunya	Senior Researcher	01/11/2011
2	Paul Carpenter Consulting Ltd	Managing Director	08/06/2003
3	ARM	Senior Software Engineer	01/08/1997
4	ARM	Web developer	1996
5	System Interrupt	Developer	1991

1 **Employing entity:** Universitat Politècnica de Catalunya **Type of entity:** University

Professional category: Senior Researcher

Start-End date: 01/11/2011 - 01/09/2014 **Duration:** 2 years - 10 months

Performed tasks: Senior Researcher in the Heterogeneous Architectures Group led by Alex Ramirez (Associate professor). Co-chair of Working Group on Programming Models in the European Technology Platform for High Performance Computing (ETP4HPC), the main organisation that represents the whole HPC industry and academia within Europe (now 64 members: companies, SMEs and research centres). Attended technical workshops during the development of the ETP4HPC Strategic Research Agenda (SRA) in Paris (2012), Munich (2012), Barcelona (2012), Bologna (2012) and Barcelona (2013). Led technical aspects of procurement of the ARM+GPU ("Pedraforca") prototype (budget €700k: 72 nodes with Nvidia Tesla K20 GPUs), including the open call and interactions with the winning supplier (Bull), as well as system performance analysis and project reporting within the FP7 PRACE-1IP project. Full member of HiPEAC Network of Excellence since April 2012. Performed analysis on sustainability of the HiPEAC Network of Excellence, to understand public and private funding of comparable research networking organisations, as well as legal, financial and organisational structure, with presentations and discussions at three physical Steering Committee meetings. Best Paper Award at SAMOS Workshop 2009 and OMHI Workshop 2014; Best Student Paper Award at SC14. HiPEAC Paper Award 2012 (€1,000). Member of IPDPS 2013 Program Committee. Reviewer for Microprocessors and Microsystems (2011), IEEE Transactions on Parallel and Distributed Systems (2012, 2013), ICCD 2012, IEEE IPDPS 2013 PhD Forum, International Journal of Parallel Programming (2011, 2012) and IEEE Access (2014). Reviewed papers for IPDPS 2011, Euro-Par 2012, TACO 2012 and Euro-Par 2013. Attended EU ICT Competitiveness Week 2012 by invitation. Panel member at DATE 2013, "Embedding High Performance Computing: A supercomputer in your pocket or ultra low power exaflop design". One of 200 "promising young researchers" out of ~2,000 applicants selected to spend a week with 24 recipients of the Abel Prize, Fields Medal, Nevanlinna Prize, and ACM A.M. Turing Award at the Heidelberg Laureate Forum 2014. Member of the team led by Alex Ramirez that received the HiPEAC Technology Transfer Award 2012 for the CARMA (CUDA on ARM) development kit that was productized by SECO. Member of founding team of two serious attempted startups. Finalist in Fundación Repsol Entrepreneurs Fund 2013 for Talaia Systems.

Applicability in teaching and/or research: Delivered Mont-Blanc talks at IS-ENES 2014 (Hamburg), RIKEN AICS 2013 (Tokyo), EU Workshop on strategic directions for next-generation computing 2013 (Brussels), ISCA 2013 (Tel Aviv), LEAP 2013 (London), DATE 2013 (Grenoble), IS-ENES 2013 (Toulouse), and BUX 2012 (Warwick).

2 **Employing entity:** Paul Carpenter Consulting Ltd **Type of entity:** Business
Professional category: Managing Director
Start-End date: 08/06/2003 - 2006
Type of contract: Permanent employment contract
Performed tasks: In 2003, I founded a small consulting company, “Paul Carpenter Consulting Ltd”. The company was incorporated in UK as a limited liability company, with company number 04791370. In addition to the technical responsibilities, I handled VAT [IVA], PAYE payroll and financial reporting. My first consulting opportunity, at ARM, started June 2003, and was extended several times, ending in April 2005. I was part of the small team (<5 people) in the ARM Research Group that designed the ARM Advanced SIMD / NEON vector ISA. It was unusual for ARM to use an external consultant, especially for key IP in the ARM architecture, but few people had the necessary skills. Advanced SIMD is a key part of the ARM architecture, and mandatory in ARMv8-A. It was first introduced in ARM Cortex-A8, in 2005, and the design has changed little as of 2015. This work led to one related worldwide patent. I was author of much of the NEON software training material including the “NEON Code Examples”, RDB01-GENC-003057 (confidential). From July to October 2015, I was engaged at Berkeley Design Technology (BDTI), Inc. in Berkeley, CA. BDTI is respected in the embedded industry as a provider of independent benchmarking and analysis. I performed the analysis for BDTI “Insider Insights on the ARM11’s Signal-Processing Capabilities” (using hardware) and “Assessing Cortex-R4 and Cortex-A8 Signal and Media Processing Performance” (using a cycle-accurate simulator). In addition to providing the technical results and analysis, I delivered a two-day training course about the ARM Architecture and Advanced SIMD to BDTI engineers.

3 **Employing entity:** ARM **Type of entity:** Business
City employing entity: Cambridge, East Anglia, United Kingdom
Professional category: Senior Software Engineer
Start-End date: 01/08/1997 - 01/10/2002 **Duration:** 5 years
Type of contract: Permanent employment contract
Dedication regime: Full time
Performed tasks: Senior Software Engineer. Technical lead for embedded ARM MP3 Decoder (two engineers) and Microsoft Windows Media Audio Decoder (two engineers), both licensed as standard software in several ASSPs (one with >50 design wins), and used by most early portable audio players, including S3 Diamond Rio Receiver, Creative Nomad and Empeg Car. Lead customer on MP3 decoder project recommended us to Microsoft for WMA decoder. Technical lead on Dolby Digital (AC-3) decoder. Handled Dolby certification process, including visit to Dolby Labs in San Francisco, CA; Dolby certification passed first time. Technical lead on MPEG-4 video decoder (three engineers) and development of reusable MOVE video codec components (four engineers). For all projects: feasibility study, development and performance/footprint optimization, programmer's guide (in collaboration with Technical Publications group), ongoing maintenance, training of Support Group (for first level of customer support), advanced customer support via email and phone, technical guidance/training visits for international sales teams, demonstration at annual ARM Partner Meeting (APM) in Cambridge, and accompanying sales on customer visits. Engineering lead for mass storage software segment, involving technical support to business development and analysis of performance and memory footprint. Engineer on V22bis software modem (AS404). Interactions with CPU Architecture team regarding the ARM ISA (usefulness and/or semantics of proposed instructions) and core micro-architecture (choice of multiplier, forwarding paths, etc.). Represented ARM at MPEG-4 Industry Forum (M4IF), Singapore (2001), in order to improve the efficiency of the MPEG-4 video standard on general purpose processors.
Field of management activity: Project manager for MPEG-4 video decoder and for MOVE coprocessor, responsible for successful completion of project within time and budget constraints. Working closely with Product Manager; managing two to four engineers.
Applicability in teaching and/or research: Invented MOVE coprocessor and defined the architecture: an accelerator for video encode (one worldwide patent) which was a standard component on the ARM PrimeXsys Wireless Platform. Internal training on MOVE coprocessor. Performance analysis and memory footprint studies for PVPlayer, Superscape, SolidStreaming, Digital Audio Broadcast (DAB), GSM-AMR, and task parallelism of MPEG-4 Video. Attended six training courses, two technical and four to develop leadership and managerial skills. Worked with

ARM's PR company to write an article for EETimes. Co-author of two white papers on the ARM DevZone website. Shadowed the group's representative to the ARM corporate patent review committee. Delivered customer training, including onsite at Sony (Tokyo), Toshiba (Tokyo), Ericsson (Lund, Sweden) and Cirrus Logic (Denver, Colorado).

4 **Employing entity:** ARM **Type of entity:** Business
City employing entity: Cambridge, East Anglia, United Kingdom
Professional category: Web developer
Start-End date: 1996 - 01/08/1997 **Duration:** 2 years
Type of contract: Temporary employment contract
Dedication regime: Part time
Performed tasks: I was the primary developer of the ARM corporate website at www.arm.com. This started as a summer internship, but it continued on a flexible part-time basis during my MA studies. I worked closely with the head of corporate communications, and was included in marketing and branding discussions in the key period leading up to the $1 billion IPO in April 1998. During this time, the website was expanded from a limited site aimed at engineers in companies already in close contact with ARM to target new audiences, including general interest and investors. During this time I made contact with the Software Systems Division and started work on image processing algorithms, which led to permanent employment at ARM.

5 **Employing entity:** System Interrupt **Type of entity:** Business
City employing entity: Bristol, United Kingdom
Professional category: Developer
Start-End date: 1991 - 1993
Dedication regime: Part time
Performed tasks: From approx. 1991 to 1993 I developed Phaethon for Acorn Archimedes. This was initially a personal project, but an early version of the game was discovered by The Serial Port Ltd, and it was launched commercially in December 1993 under the System Interrupt label. Phaethon received positive reviews ("If System Interrupt is going to keep up this standard with future releases, it is soon going to become established as one of the top entertainment labels for Acorn machines", Archimedes World, Jan 1994; "The motion is smooth, fast, and very polished", Acorn Computing, Dec 1993). It is now freely available from Acorn Arcade: http://www.acornarcade.com/forums/viewthread.php?newsid=879. The game was implemented in 17,684 lines of assembler, and it features texture mapped graphics and triple buffering, techniques that were innovative at the time. I published six other small programs as open source in magazines between 1988 and 1992.

Education

University education

1st and 2nd cycle studies and pre-Bologna degrees

1 **University degree:** Higher degree
Name of qualification: Diploma in Computer Science (MA), distinction
City degree awarding entity: Cambridge, United Kingdom
Degree awarding entity: University of Cambridge **Type of entity:** University
Date of qualification: 1997
Average mark: Outstanding
Standardised degree: Yes

2 **University degree:** Middle degree
Name of qualification: BA Hons Mathematics, double first class (Wrangler)
City degree awarding entity: Cambridge, United Kingdom
Degree awarding entity: University of Cambridge **Type of entity:** University
Date of qualification: 1996
Average mark: Outstanding
Prize: Kings Scholarship (twice)
Standardised degree: Yes

Doctorates

Doctorate programme: Arquitectura y tecnología de computadores
Degree awarding entity: Universitat Politècnica de Catalunya **Type of entity:** University
City degree awarding entity: Barcelona, Spain
Date of degree: 24/10/2011
Thesis title: Running Stream-like Programs on Heterogeneous Multi-core Systems
Thesis director: Eduard Ayguade
Thesis co-director: Alex Ramirez
Obtained qualification: Excel·lent cum laude
Standardised degree: Yes

Specialised, lifelong, technical, professional and refresher training (other than formal academic and healthcare studies)

1 **Type of training:** Course
Training title: People and Team Direction
City awarding entity: Barcelona, Catalonia, Spain
Awarding entity: Omneom
Aims of the entity: Familiarise with distinct tools to develop high performing research teams
Training manager: Cesar Llorente

End date: 11/07/2016 **Duration in hours:** 8 hours

2 **Training title:** Heidelberg Laureate Forum (HLF) 2014
City awarding entity: Heidelberg, Germany
Awarding entity: Klaus Tschira Foundation
Aims of the entity: I was an invited participant to the 2nd Heidelberg Laureate Forum (HLF), with worldwide selection and an acceptance rate <10%. The HLF offered all accepted young researchers the opportunity to personally interact with the laureates of the most prestigious prizes in the fields of mathematics and computer science. For one week, the recipients of the Abel Prize, the ACM A.M. Turing Award, the Fields Medal, and the Nevanlinna Prize engaged in a cross-generational scientific dialogue with young researchers.
End date: 26/09/2014 **Duration in hours:** 32 hours

3 **Training title:** How to Write a Competitive Proposal for Horizon 2020
City awarding entity: Barcelona, Spain
Awarding entity: Hyperion Ltd.
Aims of the entity: To train researchers, research managers and research support services in writing professional and competitive proposals for European Commission Horizon 2020.
End date: 16/12/2013 **Duration in hours:** 4 hours

4 **Training title:** Business Plan per a spin offs universitàries
City awarding entity: Barcelona, Spain
Awarding entity: Universitat Politècnica de Catalunya **Type of entity:** University
Aims of the entity: Course aimed at UPC professors to move from technological research to business plan, identify key elements of commercial success and understand the basics of a business plan.
End date: 2012 **Duration in hours:** 8 hours

5 **Training title:** How to Write a Competitive Proposal for Framework 7
City awarding entity: Barcelona, Spain
Awarding entity: Hyperion Ltd.
Aims of the entity: To train researchers, research managers and research support services in writing professional and competitive proposals for European Commission Framework Programme 7.
End date: 11/11/2011 **Duration in hours:** 7 hours

6 **Training title:** 2008 International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES)
City awarding entity: L'Aquila, Italy
Awarding entity: HiPEAC
Aims of the entity: Dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry.
End date: 19/07/2008 **Duration in hours:** 48 hours

7 **Training title:** 2007 International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES)
City awarding entity: L'Aquila, Italy
Awarding entity: HiPEAC
Aims of the entity: Dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry.
End date: 20/07/2007 **Duration in hours:** 48 hours

8 **Training title:** Riding the waves of mobile phone development
City awarding entity: Bracknell, Berkshire, Buckinghamshire and Oxfordshire, United Kingdom
Awarding entity: ENEA

Aims of the entity: Learn about future of embedded technology within mobile phones and meet industry experts.
End date: 14/06/2005 **Duration in hours:** 5 hours

9 **Training title:** Basics of Building a Business (B3)
City awarding entity: Cambridge, United Kingdom
Awarding entity: Cambridge Entrepreneurship Centre (CEC), Judge Institute of Management Studies, University of Cambridge
Aims of the entity: Basics of entrepreneurship, and how to get started and grow a business. Given by the Judge Institute of Management Studies, ranked 13 worldwide in FT's Global MBA Ranking 2015.
End date: 2003 **Duration in hours:** 12 hours

10 **Training title:** Negotiation Skills
City awarding entity: Cambridge, United Kingdom
Awarding entity: Mentor Group
End date: 10/10/2001 **Duration in hours:** 16 hours

11 **Training title:** 3G Mobile Communication Systems Foundation Course at DSP2000
City awarding entity: London, United Kingdom
Aims of the entity: Fundamentals of 3G communication systems: signal processing for CDMA, FHSS, DSSS, etc.
End date: 07/12/2000 **Duration in hours:** 16 hours

12 **Training title:** MSProject Global v5.0
City awarding entity: Cambridge, United Kingdom
Awarding entity: ARM
Aims of the entity: Project Manager training for MSProject Global v5.0
End date: 27/07/2000 **Duration in hours:** 2 hours

13 **Training title:** Learning the Ropes
City awarding entity: Cambridge, United Kingdom
Awarding entity: Mentor Group
Aims of the entity: Improve communication skills, learn how to match medium with message, practice key influencing strategies, prepare for effective reviews.
End date: 12/07/2000 **Duration in hours:** 24 hours

14 **Training title:** Project Management and ARM Processes
City awarding entity: Cambridge, United Kingdom
Awarding entity: ARM
End date: 17/01/2000 **Duration in hours:** 8 hours

15 **Training title:** Presentation Skills
City awarding entity: Cambridge, United Kingdom
Awarding entity: Mentor Group
End date: 24/11/1999 **Duration in hours:** 16 hours

Language skills

Language	Listening skills	Reading skills	Spoken interaction	Speaking skills	Writing skills
German		A1	A1	A1	A1
Catalan		B1	B1	B1	B1
Spanish		B1	B1	B1	B1
English		C1	C1	C1	C1

Teaching experience

Experience supervising doctoral thesis and/or final year projects

1 **Project title:** MPI Layer Techniques to Improve Network Energy Efficiency (co-director)
Type of project: Doctoral thesis
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Branimir Dickov
Obtained qualification: Excel·lent cum Laude
Date of reading: 10/12/2015

2 **Project title:** Energy Optimisations in Interconnects for HPC (co-director, to graduate 2016)
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Karthikeyan Saravanan

3 **Project title:** Interconnect Energy Savings on Microserver Workloads (director, started 2014)
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Renan Fischer e Silva

4 **Project title:** Multicore Architecture Optimizations for HPC Applications (co-director)
Entity: Universitat Politècnica de Catalunya
Student: Ugljesa Milic

5 **Project title:** Virtualisation Techniques for the Exploitation of Resources Across Coherence Islands (started 2014)
Entity: Universitat Politècnica de Catalunya **Type of entity:** University
Student: Luis Garrido

Scientific and technological experience

Scientific or technological activities

R&D projects funded through competitive calls of public or private entities

1 **Name of the project:** ExaNoDe
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Eduard Ayguade; Paul Carpenter
Name of the programme: H2020-FETHPC-2014
Code according to the funding entity: 671578
Start-End date: 01/10/2015 - 30/09/2018
Total amount: 8.629.250 €
Applicant's contribution: Leader of WP3 Enablement of Software Compute Node (total 242 PMs). Leader of task to develop OmpSs task-based programming model to address the issues related with building exascale systems from low-power components, including supporting the ExaNode UNIMEM architecture in SMP OmpSs, Cluster OmpSs and hybrid MPI+OmpSs.

2 **Name of the project:** EuroLab-4-HPC
Geographical area: European Union
Degree of contribution: Leader Workpackage 2 Research
Entity where project took place: Barcelona Supercomputing Center **Type of entity:** Public Research Body
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Mateo Valero
Start-End date: 01/09/2015 - 31/08/2017 **Duration:** 2 years
Relevant results: EuroLab-4-HPC is a two-year Horizon 2020 project to build the foundation for a European Research Centre of Excellence in High-Performance Computing (HPC) systems. The main objectives are to (a) join HPC system research groups around a long-term HPC research agenda, by forming an HPC research roadmap and joining forces behind it, (b) define an HPC curriculum to foster future European technology leaders, (c) accelerate commercial uptake of new HPC technologies, (d) build an HPC ecosystem of researchers, system providers, VCs etc., and (e) form a business model for the EuroLab-4-HPC excellence centre. Website: www.eurolab4hpc.eu
Applicant's contribution: Leader WP2 Research, which (i) sets a long-term vision for excellence in European academic HPC research, (ii) coordinates efforts to build common research platforms, including multi-disciplinary workshops to address cross-cutting issues and short research stays, and (iii) identifies seeds for innovation and exploitation, as well as mentoring and monitoring of the research projects to accelerate innovations in HPC. Oversaw first call for cross-site actions, which is supporting short research visits between European industrial and academic research centres, with the aim of increasing multi-disciplinary collaboration. (Co-)organised workshop at HiPEAC Fall Computing Systems Week 2015 in Milan, "EuroLab-4-HPC: Fostering Excellence in HPC System Research". Overseeing the development of the EuroLab-4-HPC long-term academic roadmap for excellence in European HPC research, covering all layers of HPC computing systems from application to hardware, with a timescale of eight to ten years. Active as the leader of the Working Group on "HPC application evolution and requirements".

3 **Name of the project:** EuroServer
Type of project: Research and development, including transfer
Geographical area: European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Type of entity: R&D Centre
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Paul Carpenter
Nº of researchers: 29
Type of participation: Principal investigator
Name of the programme: FP7-ICT-2013-10
Code according to the funding entity: 610456
Start-End date: 01/09/2013 - 31/01/2017
Duration: 3 years - 5 months
Participating entity/entities: ARM Ltd; Barcelona Supercomputing Center; Chalmers Tekniska Hoegskola; Commissariat a L'Energie Atomique et Aux Energies Alternatives (CEA); Eurotech; Foundation for Research and Technology Hellas (FORTH); OnApp; STMicroelectronics; Technische Universitaet Dresden
Total amount: 12.255.791 €
Relevant results: System architecture and software stack to improve data centre energy-efficiency and cost, by using 64-bit ARM cores, 2.5D heterogeneous silicon-on-silicon integration, FD-SOI, and coherence islands. The architecture will be evaluated using two fully integrated full-system prototypes. Web site: euroserver-project.eu.
Dedication regime: Full time
Applicant's contribution: Principal Investigator (PI) and project leader at BSC (€1.12 M and 137 person-months at BSC). Director of two PhD students: (a) hypervisor support for programming models and (b) interconnect topology and energy proportionality. Leader of dissemination task. Editor and main author of the project's publication at DSD 2014.

4 **Name of the project:** Rethink Big
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Type of entity: R&D Centre
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Adrian Cristal
Name of the programme: FP7-ICT-2013-11
Code according to the funding entity: 619788
Start-End date: 01/03/2014 - 28/02/2016
Total amount: 2.596.923 €
Relevant results: The objective of the RETHINK big Project is to bring together the key European hardware, networking, and system architects with the key producers and consumers of Big Data to identify the industry coordination points that will maximize European competitiveness in the processing and analysis of Big Data over the next 10 years. Website: rethinkbig-project.eu
Dedication regime: Part time
Applicant's contribution: Member of Editorial team and key role in BSC's coordination of the project.

5 **Name of the project:** HiPEAC-3
Geographical area: European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Mateo Valero
Nº of researchers: 337
Type of participation: Team member

Name of the programme: FP7-ICT-2011-7
Code according to the funding entity: 287759
Start-End date: 01/02/2012 - 31/01/2016
Participating entity/entities: ARM; Barcelona Supercomputing Center; Chalmers Tekniska Hoegskola; Commissariat a l'Energie Atomique et Aux Energies Alternatives (CEA); Ericsson; Foundation for Research and Technology Hellas (FORTH); IBM Israel - Science and Technology; Institut National de Recherche en Informatique et en Automatique; Recore Systems; Rheinsch-Westfaelische Technische Hochschule Aachen; STMicroelectronics; Thales; Universiteit Gent
Total amount: 3.800.000 €
Relevant results: HiPEAC is a European Network of Excellence (NoE) with the mission to steer and increase European research in the area of high-performance and embedded computing systems. “The HiPEAC network, since its creation in 2004, triggered fundamental changes in the European computing systems community, and it has created a long lasting impact in Europe” (EU Project Officer Panagiotis Tsarchopoulos). The network stimulates cooperation between a) academia and industry and b) computer architects and tool builders. HiPEAC has 430 members from 275 institutions in 37 countries. Website: hipeac.net
Applicant's contribution: I handled the task to analyse options for self-sustainability of the HiPEAC Network of Excellence, beyond the end of the EU Network of Excellence instrument. This task required an analysis of comparable research organisations, projections of income versus ongoing expenses, and legal, financial and organisational structure. I was also the proofreader for HIPEACinfo quarterly newsletter, which is sent to more than 500 researchers and company managers from academia and industry, in Europe, America and Asia.

6 **Name of the project:** Mont-Blanc
Geographical area: European Union
Entity where project took place: Barcelona Supercomputing Center
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Filippo Mantovani
Nº of researchers: 30
Type of participation: Team member
Name of the programme: FP7-ICT-2011-7
Code according to the funding entity: 288777
Start-End date: 01/10/2011 - 30/09/2014
Participating entity/entities: ARM Limited; Barcelona Supercomputing Center; Bayerische Akademie der Wissenschaften; Bull SAS; Centre National de la Recherche Scientifique (CNRS); Consorzio Interuniversitario CINECA; Forschungszentrum Jülich GmbH; Gnodal Ltd; Grand Equipement National de Calcul Intensif (GENCI); Universidad de Cantabria
Total amount: 14.500.000 €
Relevant results: Designed new type of computer architecture built from energy-efficient solutions used in embedded and mobile devices. The Mont-Blanc prototype, which is already operational, has 135 nodes, each a dual-core Samsung Exynos 5 with 4 GB RAM, 16 GB uSD, 1 GbE, and Ubuntu 14.04.
Applicant's contribution: Co-advising PhD student researching interconnect energy proportionality. Leading engineer analysing the performance of data centre applications on the Mont-Blanc prototype system. Presented invited talks at IS-ENES 2014 (Hamburg, Germany), RIKEN AICS 2013 (Tokyo, Japan), EU Workshop on strategic directions for next-generation computing 2013 (Brussels, Belgium), ISCA 2013 (Tel Aviv, Israel), LEAP 2013 (London, UK), DATE 2013 (Grenoble, France), IS-ENES 2013 (Toulouse, France), and BUX 2012 (Warwick, UK).

7 **Name of the project:** PRACE-1IP
Type of project: Precompetitive development **Geographical area:** European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Name principal investigator (PI, Co-PI....): Sergi Girona
Type of participation: Team member

Name of the programme: FP7-INFRA-20101-2.3.1
Start-End date: 01/07/2010 - 31/12/2013 **Duration:** 2 years
Participating entity/entities: Barcelona Supercomputing Center (BSC); Computation-based Science and Technology Research Center, The Cyprus Institute (CaSToRC); Consorzio Interuniversitario CINECA; Eidgenössische Technische Hochschule Zürich (ETH Zürich); Executive agency "Electronic communication networks and information systems (NCSA); Forschungszentrum Jülich GmbH; GCS – GAUSS Centre for Supercomputing e.V; Grand Equipement National de Calcul Intensif (GENCI); Greek Research and Technology Network S.A. (GRNET); IT Center for Science Ltd. (CSC); Institute of Physics Belgrade; Johannes Kepler University of Linz (JKU); Laboratory for Advanced Computing of the University of Coimbra (UC-LCA); National University of Ireland, Galway; Poznan Supercomputing and Networking Center (PSNC); SURFsara (formerly SARA Computing and Networking Services); Swedish National Infrastructure for Computing (SNIC); Technical University of Ostrava (VŠB); The Engineering and Physical Sciences Research Council (EPSRC); UNINETT Sigma AS; UYBHM – Ulusal Yuksek Basarimli Hesaplama Merkezi, Istanbul Technical University – National Center for High Performance Computing
Total amount: 27.744.964 €
Relevant results: PRACE (Partnership for Advanced Computing in Europe) was established in 2010 to create a pan-European research infrastructure for world-class supercomputers, and which provides access to the major public supercomputing resources in Europe through an open peer-review process. It also supports users and user communities in porting, scaling and optimising their applications, and provides extensive training through six PRACE Advanced Training Centres (PATC). PRACE-1IP funded the first implementation phase of PRACE, and WP9 explored advanced technologies for next-generation systems by building and evaluating innovative prototype systems.
Applicant's contribution: I led the technical aspects of the procurement of the ARM+GPU prototype, which was part of PRACE's activity to affect the next generation of supercomputers and evaluate technologies that will need multiple iterations to become viable HPC alternatives to the mature contemporary solutions. ARM+GPU ("Pedraforca") has a budget of €700k, and comprised 72 ARM-based nodes, each with an Nvidia Tesla K20 accelerator. This task included defining the open call and interacting with the winning supplier (Bull), as well as performing system performance analysis, and project reporting.

8 **Name of the project:** Computación de Altas Prestaciones V (TIN2007-60625)
Geographical area: National
Degree of contribution: Researcher
Entity where project took place: Universitat Politècnica de Catalunya **Type of entity:** University
City of entity: Barcelona, Spain
Name principal investigator (PI, Co-PI....): Mateo Valero
Nº of researchers: 116
Type of participation: Team member
Name of the programme: Consolider
Start-End date: 10/2007 - 08/2012
Total amount: 3.014.110 €

9 **Name of the project:** ACOTES - Advanced Compiler Technologies for Embedded Streaming
Geographical area: European Union
Degree of contribution: Researcher
Entity where project took place: Departamento de Arquitectura de Computadores (UPC) **Type of entity:** University
City of entity: Barcelona, Catalonia, Spain
Name principal investigator (PI, Co-PI....): Eduard Ayguade
Nº of researchers: 3
Funding entity or bodies:
Unión Europea **Type of entity:** State agency

Type of participation: Team member

Name of the programme: FP6-2005-IST-5
Code according to the funding entity: 034869
Start-End date: 01/06/2006 - 31/05/2009
Participating entity/entities: Association pour la Recherche et le Développement des Methods et Processus Industriels, Armines; IBM Israel - Science and Technology; Institut National de Recherche en Informatique et en Automatique (INRIA); NXP Semiconductors Netherlands; STMicroelectronics; Silicon Hive; Universitat Politècnica de Catalunya
Total amount: 5.021.442 €
Relevant results: The ACOTES project worked to increase programmer productivity in the area of streaming applications, through advances in programming model and compiler technology. The programming model introduced C annotations to define the streaming semantics. A source-to-source compiler supported high-level transformations controlled by the partitioning algorithm. The translated program used the Nanos++ runtime system. The project also included work on vectorisation in the GCC backend.
Dedication regime: Full time
Applicant's contribution: Research during PhD studies: abstract model of streaming program and the target hardware (Abstract Streaming Machine). Static partitioning algorithm and static buffer sizing algorithm for the prototype ACOTES compiler. Starsscheck, a tool (based on Valgrind) to check correctness of the annotations. Contributed to project deliverables. Attended ACOTES project meetings in Eindhoven, Netherlands (October 2006) and Haifa, Israel (April 2007), and Cambridge, UK (December 2007).

10 **Name of the project:** EXDCI
Geographical area: European Union
Degree of contribution: Researcher
Entity where project took place: Barcelona Supercomputing Center
Name principal investigator (PI, Co-PI....): Sergi Girona
Type of participation: Team member
Name of the programme: H2020-FETHPC-2014, FETHPC-2-2014 - HPC Ecosystem Development
Code according to the funding entity: 671558
Start date: 01/09/2015
Relevant results: EXDCI (European Extreme Data & Computing Initiative) has the objective to coordinate the development of a common strategy for the European HPC ecosystem. The two most significant HPC bodies in Europe, PRACE and ETP4HPC, join their expertise in this 30-month project, which started September 2015. EXDCI is producing and aligning roadmaps for HPC technology and applications, measuring the implementation of the European HPC strategy, and building and maintaining relations with other international HPC activities and regions. Website: exdci.eu.
Applicant's contribution: Co-leader of task related to ecosystem and roadmap towards extreme and pervasive data and computing: high-productivity programming environments and system software. This is an continuation of my role as co-leader of Working Group on Programming Environment for the ETP4HPC SRA, held since 2012.

R&D non-competitive contracts, agreements or projects with public or private entities

1 **Name of the project:** BDTI performance analysis
Type of project: Research and development, including transfer
Degree of contribution: Scientific coordinator
Entity where project took place: BDTI, Inc. **Type of entity:** Business
City of entity: Berkeley, United States of America
Name principal investigator (PI, Co-PI....): Paul Carpenter
Nº of researchers: 1 **Nª people/year:** 1
Participating entity/entities: Paul Carpenter Consulting Ltd.
Start date: 25/07/2005 **Duration:** 3 months

Relevant results: Performance and memory footprint optimisation and analysis for multimedia codec and BDTI Benchmarks on ARM11 (hardware) and ARM Cortex-A8 processor (cycle-accurate simulator). Delivered two-day training course to BDTI engineers.

2 **Name of the project:** ARM codec representative in development of NEON ISA
Entity where project took place: ARM Holdings PLC **Type of entity:** Business
City of entity: Cambridge, United Kingdom
Name principal investigator (PI, Co-PI....): Paul Carpenter
Nº of researchers: 1 **Nª people/year:** 1
Participating entity/entities: Paul Carpenter Consulting Ltd.
Start date: 16/06/2003 **Duration:** 1 year - 10 months
Relevant results: Part of the small team (<5 people) in the ARM Research Group (corporate headquarters in Cambridge, UK) that designed the ARM Advanced SIMD / NEON vector ISA. Inventor on one related worldwide patent. Author of NEON software training material (presentation and document "NEON Code Examples", RDB01-GENC-003057). Advanced SIMD was introduced in ARM Cortex-A8 (2005) and the design has changed little as of 2015. Advanced SIMD is mandatory in the latest ARM Architecture (ARMv8-A), and in 64-bit mode it is the only support for SIMD.

Results

Industrial and intellectual property

1 **Title registered industrial property:** Data filtering
Description of qualities: A method, computer program product and data processing apparatus for filtering data, in particular for use in deblocking filters. The method comprising applying a plurality of m filter coefficients which each have a value which is a negative power of two and which sum to one, to a plurality of m input data items to produce a filtered output data item, by performing a sequence of averaging calculations comprising averaging input data items to which a smallest filter coefficient is to be applied to produce first averaged data and averaging the first averaged data with other averaged input data or with input data items to which larger filter coefficients are to be applied the plurality of m filter coefficients being applied to the plurality of m input data items via a sequence of averaging calculations such that a data width of any calculated data does not exceed that of the input data being averaged.
Inventors/authors/obtainers: Paul Matthew Carpenter; Dominic Hugo Symes
Entity holder of rights: ARM Limited
Nº of application: 10/764473
Country of inscription: United States of America
Date of register: 27/01/2004
Conferral date: 01/01/2008
Nº of patent: US7315875 B2
EU patent: Yes
International non-EU patent: Yes
Licences: Yes
Companies: ARM Holdings plc
Products: ARM Video decoder (licenced at least twice), MOVE video components

2 **Title registered industrial property:** Inserting Bits Within a Data Word
Description of qualities: A data processing system (2) is provided which supports shift-and-insert instructions SLI, SRI which serve to shift a source data value by a specified shift amount and then insert bits from that shifted value other than the shifted-in bits into a destination value with the remaining bits within that destination value being unaltered.

Inventors/authors/obtainers: Paul Matthew Carpenter; Simon Andrew Ford
Entity holder of rights: ARM Holdings PLC
Nº of application: PCT/GB2004/003343
Country of inscription: United Kingdom
Date of register: 03/08/2004
Conferral date: 22/06/2006
Nº of patent: WO2005088441 A3
EU patent: Yes
International non-EU patent: Yes **PCT patent:** Yes
Licences: Yes
Products: ARM Advanced SIMD, ARMv8-A Architecture Licence, ARM Cortex-A8,A9,A15,A53,A57, etc.

3 **Title registered industrial property:** Data processing using a coprocessor
Description of qualities: A data processing system using a main processor 8 and a coprocessor 10 provides coprocessor load instructions (USALD) for loading a variable number of data values dependent upon alignment into the coprocessor 10 and also specifying data processing operations to be performed upon operands within those loaded data words to generate result data words. The specified coprocessor processing operations may be a sum of absolute differences calculation for a row of pixel byte values. The result of this may be accumulated within an accumulate register 22. A coprocessor memory 18 is provided within the coprocessor 10 to provide local storage of frequently used operand values for the coprocessor 10.
Inventors/authors/obtainers: Paul Matthew Carpenter; Peter James Aldworth
Entity holder of rights: ARM Limited
Nº of application: WO/2002/067113
Country of inscription: United Kingdom
Date of register: 13/12/2001
Conferral date: 29/08/2002
Nº of patent: WO2002067113 A1
Spanish patent: Yes **EU patent:** Yes
International non-EU patent: Yes **PCT patent:** Yes
Licences: Yes
Companies: ARM Holdings plc
Products: MOVE video accelerator, PrimeXsys Wireless Platform

4 **Description of qualities:** ARM MP3 Decoder. Technical lead. Licensed as standard software in several ASSPs (one with >50 design wins), and used by most early portable audio players, including S3 Diamond Rio Receiver, Creative Nomad and Empeg Car. Lead customer on MP3 decoder project recommended us to Microsoft for WMA decoder. This product was a major success for the ARM Software Systems Group.
Licences: Yes
Products: ARM AS022

5 **Description of qualities:** ARM Windows Media Audio (WMA) Decoder. Technical lead. Licensed as standard software in several ASSPs (one with >50 design wins), and used by most early portable audio players, including S3 Diamond Rio Receiver, Creative Nomad and Empeg Car.
Licences: Yes

6 **Description of qualities:** Dolby Digital (AC-3) Decoder. Technical lead.
Licences: Yes
Products: AS404

7 **Description of qualities:** MPEG-4 Video Codec. Technical lead. Licenced by ARM and integrated as embedded software in at least two customer ASSPs
Entity holder of rights: ARM

Licences: Yes

8 **Description of qualities:** V22bis Software Modem.
Products: ARM AS404

Scientific and technological activities

Scientific production

Publications, scientific and technical documents

1 Victor Garcia; Alejandro Rico; Carlos Villavieja; Paul Carpenter; Nacho Navarro; Alex Ramirez. Adaptive Runtime-Assisted Block Prefetching on Chip-Multiprocessors. International Journal of Parallel Programming. pp. 1 - 21. Springer, 29/04/2016.
Type of production: Scientific paper

2 Peter Radojkovic; Paul Carpenter; Miquel Moretó; Vladimir Cakarevic; Javier Verdu; Alex Pajuelo; Francisco Cazorla; Mario Nemirovsky; Mateo Valero. Thread Assignment in Multicore/Multithreaded Processors: A Statistical Approach. IEEE Transactions on Computers. pp. 256 - 269. IEEE, 27/03/2015. Available on-line at: <http://dx.doi.org/10.1109/TC.2015.2417533>.
Type of production: Scientific paper
Format: Journal
Position of signature: 2
Degree of contribution: Author or co-author of article in journal with external admissions assessment committee
Total no. authors: 9
Corresponding author: No
Impact source: JCR
Impact index in year of publication: 1.659

Relevant results: Featured paper of the month for January 2016 (1 featured paper of 28 published), promoted on front page and downloadable for free for one month, with English and Chinese videos.

3 Paul Carpenter; Alex Ramirez; Eduard Ayguadé. The Abstract Streaming Machine: Compile-Time Performance Modelling of Stream Programs on Heterogeneous Multiprocessors. Transactions on HiPEAC. 5 - 3, Per Stenstrom, 01/01/2011. ISBN 978-3-642-19448-1
Type of production: Scientific paper
Format: Journal
Position of signature: 1
Total no. authors: 3
Corresponding author: Yes

4 Harm Munk; Eduard Ayguadé; Cédric Bastoul; Paul Carpenter; Zbigniew Chamski; Albert Cohen; Marco Cornero; Philippe Dumont; Marc Duranton; Mohammed Fellahi; Roger Ferrer; Razya Ladelszy; Menno Lindwer; Xavier Martorell; Cupertino Miranda; Dorit Nuzman; Andrea Orstein; Antoniu Pop; Sebastian Pop; Louis-Noël Pouchet; Alex Ramirez; David Rodenas; Erven Rohou; Ira Rosen; Uzi Shvadron; Konrad Trifunovic; Ayal Zaks. ACOTES Project: Advanced Compiler Technologies for Embedded Streaming. International Journal of Parallel Programming. 39 - 3, pp. 397 - 450. Bilha Mendelson, Koen Bosschere, Mateo Valero, 01/04/2010. ISSN 0885-7458
Type of production: Scientific paper
Format: Journal
Position of signature: 4
Impact source: SJR
Impact index in year of publication: 0.554

5 Paul Carpenter; Alex Ramirez; Eduard Ayguadé. Buffer sizing for self-timed stream programs on heterogeneous distributed memory. Lecture Notes in Computer Science. 5952, Springer, 25/01/2010.
Type of production: Scientific paper **Format:** Journal
Position of signature: 1
Total no. authors: 3 **Corresponding author:** Yes
Impact source: SJR
Impact index in year of publication: 0.329

6 Paul Carpenter; Alex Ramirez; Eduard Ayguadé. The Abstract Streaming Machine: Compile-Time Performance Modeling of Stream Programs on Heterogeneous Processors. Lectures Notes in Computer Science. 5657, Springer, 21/07/2009.
Type of production: Scientific paper
Position of signature: 1
Total no. authors: 3 **Corresponding author:** Yes
Impact source: SJR
Impact index in year of publication: 0.342

7 Paul Carpenter; Alex Ramirez; Eduard Ayguade. The Abstract Streaming Machine. HiPEAC ACACES 2008 Summer School Poster Abstracts. Academic Press. pp. 305 - 308. 16/07/2008. ISBN 978 90 382 1288 3
Type of production: Scientific paper
Position of signature: 1

8 Paul Carpenter; David Rodenas; Xavier Martorell; Alex Ramirez; Eduard Ayguadé. A Streaming Machine Description and Programming Model. Lecture Notes in Computer Science. 4599, pp. 107 - 116. Springer, 07/2007.
Type of production: Scientific paper
Impact source: SJR
Impact index in year of publication: 0.311

9 Paul Carpenter; Guy Lonsdale. Technical Research Priorities: Programming Environment. ETP4HPC Strategic Research Agenda 2015 Update. 16/12/2015.
Type of production: Book chapter **Format:** Scientific and technical document or report

10 Paul Carpenter; Guy Lonsdale. Technical Research Priorities: Programming Environment. ETP4HPC Strategic Research Agenda. 05/2013.
Type of production: Book chapter

11 Paul Carpenter; David Rodenas; Xavier Martorell; Alex Ramirez; Eduard Ayguadé. Code generation for streaming applications based on an abstract machine description. 04/2007.
Type of production: Scientific-technical report
Position of signature: 1

12 Barney Wragg; Paul Carpenter. An Optimised Software Solution for an ARM Powered MP3 Decoder. 27/10/2000.
Type of production: Scientific-technical report

13 Extreme Value Theory: Solving intractable computer science problems. 12/2015. Available on-line at: <https://www.youtube.com/watch?v=Zaq2g_bVD6s>.
Type of production: Dissemination video **Format:** Scientific and technical document or report
Corresponding author: No
Relevant results: Dissemination video for Extreme Value Theory. Coauthor and narrator.

14 Paul Carpenter. Europe invests realising next-generation green computing for micro-servers and scalable compute. 28/03/2014.
Type of production: Press release

15 Alya Red: A computational heart. 09/2012. Available on-line at: <https://www.youtube.com/watch?v=hiKgDOXIPfk>.
Type of production: Dissemination video **Format:** Scientific and technical document or report
Relevant results: Dissemination video for Alya Red simulation of a human heart. Narrator.

16 Alan Lewis; Paul Carpenter. Optimizing Digital Video Codecs in ARM Cores. EE Times. 20/09/2001.
Format: Scientific and technical document or report

Works submitted to national or international conferences

1 **Title of the work:** Controlling Network Latency in Mixed Hadoop Clusters: Do We Need Active Queue Management?
Name of the conference: 41st Annual IEEE Conference on Local Computer Networks (LCN 2016)
City of event: Dubai, United Arab Emirates
Date of event: 07/11/2016
End date: 10/11/2016
Renan Fischer e Silva; Paul Carpenter.

2 **Title of the work:** Large-Memory Nodes for Energy Efficient High-Performance Computing
Name of the conference: International Symposium on Memory Systems (MEMSYS 2016)
City of event: Washington, DC, United States of America
Date of event: 03/10/2016
End date: 06/10/2016
Darko Zivanovic; Milan Radulovic; German Lloret; David Zaragoza; Janko Strassburg; Paul Carpenter; Petar Radojkovic; Eduard Ayguade.

3 **Title of the work:** Rebalancing the Core Front-End through HPC Code Analysis
Name of the conference: 2016 IEEE International Symposium on Workload Characterisation (IISWC 2016)
City of event: Providence, RI, United States of America
Date of event: 25/09/2016
End date: 27/09/2016
Ugljesa Milic; Paul Carpenter; Alejandro Rico; Alex Ramirez.

4 **Title of the work:** ALYA Multi-Physics System on GPUs: Offloading Large-Scale Computational Mechanics Problems
Name of the conference: GPU Technology Conference (GTC)
City of event: San Jose, CA, United States of America
Date of event: 04/04/2016
End date: 07/04/2016
Organising entity: Nvidia
Vishal Mehta; Paul Carpenter.

5 **Title of the work:** EUROSERVER: Share-Anything Scale-Out Micro-Server Design
Name of the conference: Design Automation and Test in Europe (DATE)
City of event: Dresden, Germany

Date of event: 14/03/2016
End date: 18/03/2016
Manolis Marazakis; John Goodacre; Didier Fuin; Paul Carpenter; John Thomson; Emil Matus; Antimo Bruno; Per Stenstrom; Jerome Martin; Yves Durand; Isabelle Dor.

6 **Title of the work:** Self-Tuned Software-Managed Energy Reduction in InfiniBand Links
Name of the conference: 21st IEEE International Conference on Parallel and Distributed Systems (ICPADS)
City of event: Melbourne, Australia
Date of event: 14/12/2015
End date: 17/12/2015
With external admission assessment committee: Yes
Branimir Dickov; Paul Carpenter; Miquel Pericas; Eduard Ayguadé. "2015 21st IEEE International Conference on Parallel and Distributed Systems (ICPADS)".

7 **Title of the work:** Exploring Interconnect Energy Savings Under East-West Traffic Pattern of MapReduce Clusters
Name of the conference: 40th IEEE Conference on Local Computer Networks (LCN)
City of event: Clearwater Beach, FL, United States of America
Date of event: 26/10/2015
End date: 29/10/2015
With external admission assessment committee: Yes
Renan Fischer e Silva; Paul Carpenter.

8 **Title of the work:** Exploring Multiple Sleep Modes in On/Off based Energy Efficient HPC Networks
Name of the conference: 33rd IEEE International Conference on Computer Design (ICCD)
City of event: New York City, United States of America
Date of event: 18/10/2015
End date: 21/10/2015
With external admission assessment committee: Yes
Karthikeyan P. Saravanan; Paul M. Carpenter; Alex Ramirez. "Proceedings of the 33rd IEEE International Conference on Computer Design (ICCD)".

9 **Title of the work:** Exploiting CUDA Dynamic Parallelism for Low-Power ARM-Based Prototypes
Name of the conference: GPU Technology Conference (GTC)
City of event: San Jose, CA, United States of America
Date of event: 17/03/2015
End date: 20/03/2015
Organising entity: Nvidia
Vishal Mehta; Paul Carpenter.

10 **Title of the work:** Analyzing performance improvements and energy savings in Infiniband Architecture using network compression
Name of the conference: 26th International Symposium on Computer Architecture and High Performance Computing, SBAC-PAD 2014
City of event: Paris, Île de France, France
Date of event: 22/10/2014
End date: 24/10/2014
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Branimir Dickov; Miquel Pericas; Paul Carpenter; Nacho Navarro; Eduard Ayguade. En: 2014 IEEE 26th International Symposium on Computer Architecture and High Performance Computing

(SBAC-PAD). pp. 73 - 80. Pierre Sens, Philippe O. A. Navaux, Alfredo Goldman, Laxmikant Kale, ISBN 978-1-4799-6904-3

11 **Title of the work:** Software-Managed Power Reduction in Infiniband Links.
Name of the conference: The 43rd Annual Conference on Parallel Processing (ICPP-2014)
City of event: Minneapolis, United States of America
Date of event: 09/09/2014
End date: 12/09/2014
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Branimir Dickov; Miquel Pericas; Paul Carpenter; Nacho Navarro; Eduard Ayguade. En: 43rd International Conference on Parallel Processing (ICPP), 2014. pp. 311 - 320. David Du, Anand Tripathi, ISBN 978-1-4799-5618-0

12 **Title of the work:** EUROSERVER: Energy Efficient Node for European Micro-servers. (I was editor and primary author on this paper).
Name of the conference: Euromicro Conference on Digital System Design (DSD) 2014
City of event: Verona, Veneto, Italy
Date of event: 27/08/2014
End date: 29/08/2014
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Yves Durand; Paul Carpenter; Stefano Adami; Angelos Bilas; Denis Dutoit; Alexis Farcy; Georgi Gaydadjiev; John Goodacre; Manolis Katevenis; Manolis Marazakis; Emil Matus; Iakovos Maovroidis; John Thomson. En: 17th Euromicro Conference on Digital System Design (DSD), 2014. pp. 206 - 213. Davide Quaglia, Francesco Leporati, José Silva Matos, ISBN 978-1-4799-5793-4

13 **Title of the work:** Adaptive Runtime-Assisted Block Prefetching on Chip-Multiprocessors.
Name of the conference: Third International Workshop on On-chip memory hierarchies and interconnects: organization, management and implementation, 2014
City of event: Porto, Portugal
Date of event: 25/08/2014
End date: 25/08/2014
Publication in conference proceedings: Yes
Victor Garcia; Alejandro Rico; Carlos Villavieja; Paul Carpenter; Alex Ramirez; Nacho Navarro. "Euro-Par 2014: Parallel Processing Workshops". ISSN 0302-9743, ISBN 978-3-319-14312-5

14 **Title of the work:** A Performance Perspective on Energy Efficient HPC Links
Name of the conference: 28th International Conference on Supercomputing, ICS 2014
Geographical area: Non EU International
City of event: Munich, Germany
Date of event: 10/06/2014
End date: 13/06/2014
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Karthikeyan Saravanan; Paul Carpenter; Alex Ramirez. En: Proceedings of the 28th ACM international conference on Supercomputing. pp. 313 - 322. Arndt Bode, Michael Gerndt, Per Stenström, Lawrence Rauchwerger, Barton Miller, Martin Schulz, ISBN 978-1-4503-2642-1

15 **Title of the work:** Supercomputing with Commodity CPUs: Are Mobile SoCs Ready for HPC?
Name of the conference: The International Conference for High Performance Computing, Networking, Storage and Analysis (SC '13)

City of event: Denver, United States of America
Date of event: 17/11/2013
End date: 22/11/2013
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Nikola Rajovic; Paul M. Carpenter; Isaac Gelado; Nikola Puzovic; Alex Ramirez; Mateo Valero. En: Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis. William Gropp, Satoshi Matsuoka, ISBN 978-1-4503-2378-9

16 **Title of the work:** Power/Performance Evaluation of Energy Efficient Ethernet (EEE)
Name of the conference: IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2013
City of event: Austin, United States of America
Date of event: 21/04/2013
End date: 23/04/2013
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Karthikeyan P. Saravanan; Paul M. Carpenter; Alex Ramirez. En: 2013 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS). pp. 205 - 214. ISBN 978-1-4673-5777-7

17 **Title of the work:** Kernel Partitioning of Streaming Applications: A Statistical Approach to an NP-complete Problem
Name of the conference: International Symposium on Microarchitecture (MICRO-45)
City of event: Vancouver, Canada
Date of event: 01/12/2012
End date: 05/12/2012
Publication in conference proceedings: Yes
Petar Radojkovic; Paul M. Carpenter; Miquel Moreto; Alex Ramirez; Francisco J. Cazorla. En: Proceedings of the 2012 45th Annual IEEE/ACM International Symposium on Microarchitecture. pp. 401 - 412. ISBN 978-0-7695-4924-8

18 **Title of the work:** Starsscheck: A tool to find errors in task-based parallel programs
Name of the conference: 16th International Euro-Par Conference on Parallel and Distributed Computing (Euro-Par 2010)
City of event: Ischia, Italy
Date of event: 31/08/2010
End date: 03/09/2010
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
En: 16th International Euro-Par Conference Ischia, Italy, August 31 - September 3, 2010 Proceedings, Part 1. pp. 2 - 13. Domenico Talia, Pasqua D'Ambra, Mario Rosario Guarracino, ISBN 978-3-642-15276-4

19 **Title of the work:** Buffer sizing for self-timed stream programs on heterogeneous distributed memory multiprocessors
Name of the conference: International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC 2010)
City of event: Pisa, Italy
Date of event: 25/01/2010
End date: 27/01/2010
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes

Paul Carpenter; Alex Ramirez; Eduard Ayguadé. En: Lecture Notes in Computer Science. 5952, Yale N. Patt, Pierfrancesco Foglia, Evelyn Duesterwald, Paolo Faraboschi, Xavier Martorell, ISBN 978-3-642-11514-1

20 **Title of the work:** Mapping stream programs onto heterogeneous multiprocessor systems
Name of the conference: International Conference on Compilers, Architecture, and Synthesis for Embedded Systems
City of event: Grenoble, France
Date of event: 11/10/2009
End date: 17/10/2009
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Paul Carpenter; Alex Ramirez; Eduard Ayguadé. En: Proceedings of the 2009 international conference on Compilers, architecture, and synthesis for embedded systems. pp. 57 - 66. Joerg Henkel, Sri Parameswaran, ISBN 978-1-60558-626-7

21 **Title of the work:** The Abstract Streaming Machine: Compile-Time Performance Modelling of Stream Programs on Heterogeneous Multiprocessors
Name of the conference: SAMOS Workshop - International Workshop on Systems, Architectures, Modeling, and Simulation (Best paper award)
City of event: Samos, Greece
Date of event: 20/07/2009
End date: 23/07/2009
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Paul Carpenter; Alex Ramirez; Eduard Ayguadé. En: Lecture Notes in Computer Science. 5657, Koen Bertels, Nikitas Dimopoulos, Cristina Silvano, Stephan Wong, ISBN 978-3-642-03137-3

22 **Title of the work:** A Streaming Machine Description and Programming Model
Name of the conference: VII International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS Workshop VII)
Geographical area: European Union
City of event: Samos, Greece
Date of event: 16/07/2007
End date: 19/07/2007
Publication in conference proceedings: Yes **With external admission assessment committee:** Yes
Paul Carpenter; David Rodenas; Xavier Martorell; Alex Ramirez; Eduard Ayguadé. En: Lecture Notes in Computer Science Vol 4599. pp. 107 - 116. Stamatis Vassiliadis, Mladen Berekovic, Timo D. Hämäläinen, ISBN 978-3-540-73622-6

23 **Title of the work:** Abstract Streaming Machine for Compiler Optimizations
Name of the conference: Third International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES 2007)
City of event: L'Aquila, Italy
Date of event: 2007
With external admission assessment committee: Yes
Paul Carpenter; Alex Ramirez; Eduard Ayguadé.

24 **Title of the work:** Audio decompression using 32-bit RISC CPU versus traditional DSP
Name of the conference: Silicon for Audio - AES 16th UK Conference
Type of event: Conference

Date of event: 09/04/2001
End date: 10/04/2001
Publication in conference proceedings: Yes
Marc Bringmann; Paul Carpenter; John Graley. "Audio Engineering Society 16th UK Conference". En: Proceedings of the AES 16th UK Conference: Silicon for Audio.

Other dissemination activities

1 **Title of the work:** RETHINKing big data hardware: A Roadmap for European Industry
Name of the event: Barcelona Big Data Congress 2016
Type of event: Conferences given
City of event: Barcelona, Spain
Date of event: 05/10/2016
Paul Carpenter.

2 **Title of the work:** ExaNoDe European Exascale Processor & Memory Node Design
Name of the event: ISC Workshop on International Cooperation
Type of event: Conferences given
City of event: Frankfurt, Germany
Date of event: 03/08/2016
Paul Carpenter.

3 **Title of the work:** ExaNoDe video interview for Primeur Magazine
Name of the event: ISC 2016
Type of event: Media interviews
City of event: Frankfurt, Germany
Date of event: 23/06/2016
Organising entity: Primeur Magazine
Paul Carpenter. Available on-line at: <http://primeurmagazine.com/weekly/AE-PR-09-16-33.html>.

4 **Title of the work:** ARM technology video interview for ARM Annual Partner Meeting
City of event: Frankfurt, Germany
Date of event: 22/06/2016
Paul Carpenter.

5 **Title of the work:** State of Preliminary Eurolab-4-HPC Roadmap
Name of the event: EuroLab-4-HPC: Building and integrated systems and HPC community
Type of event: Conferences given
City of event: Porto, Portugal
Date of event: 20/04/2016
Theo Ungerer; Paul Carpenter.

6 **Title of the work:** Building a globally competitive HPC Technology Provision Value Chain in Europe
Name of the event: Big Data Value Association Summit
Type of event: Conferences given
City of event: Madrid, 18/06/2015, Spain
Date of event: 18/06/2015
Organising entity: Big Data Value Association (BDVA)
Marcin Ostacz (management presenter); Paul Carpenter (technical presenter).

7 **Title of the work:** Euroserver project booth
Name of the event: ARTEMISIA Co-Summit 2015
Type of event: Fairs and exhibitions
City of event: Berlin, Germany
Date of event: 10/03/2015
Organising entity: ARTEMIS Industry Association

8 **Title of the work:** MONT-BLANC: European Scalable and Power Efficient HPC Platform Based on Low-Power Embedded Technology
Name of the event: Exascale Technologies & Innovation in HPC for Climate Models - 3rd HPC Workshop
Type of event: Conferences given
City of event: Hamburg, Germany
Date of event: 17/03/2014
Paul Carpenter (presenter).

9 **Title of the work:** Position of Mont-Blanc 2 Project
Name of the event: EU Workshop on Next Generation Computing Systems: Components and Architectures for a Scalable Market
Type of event: EU Workshop
City of event: Brussels, Belgium
Date of event: 10/12/2013
Organising entity: European Commission DG CONNECT, Complex Systems and Advanced Computing
Alex Ramirez; Paul Carpenter (presenter).

10 **Title of the work:** The Mont-Blanc Project: Are Mobile Processors Ready for HPC?
Name of the event: Fourth AICS International Symposium
Type of event: Conferences given
City of event: Kobe, Japan
Date of event: 02/12/2013
Paul Carpenter (presenter); Nikola Rajovic; Nikola Puzovic; Alex Ramirez.

11 **Title of the work:** European Scalable and Power Efficient HPC Platform Based on Low-Power Embedded Technology
Name of the event: ISCA 2013 EU-FP7 Workshop: Synopsis of FP7 Computer Systems and Transitioning to Horizon 2020
Type of event: Conferences given
City of event: Tel Aviv, Israel
Date of event: 23/06/2013
Alex Ramirez; Paul Carpenter (presenter).

12 **Title of the work:** Experiences with Mobile Processors for Energy Efficient HPC
Name of the event: Low Energy Application Parallelism (LEAP) Conference
Type of event: Conferences given
City of event: London, United Kingdom
Date of event: 21/05/2013
Alex Ramirez; Nikola Rajovic; Alejandro Rico; James Vipond; Paul Carpenter (presenter and panel member); Nikola Puzovic.

13 **Title of the work:** Embedding High Performance Computing: A supercomputer in your pocket or ultra low power exaflop design?
Name of the event: Design, Automation & Test in Europe (DATE), 2013

Type of event: Conferences given
City of event: Grenoble, France
Date of event: 22/03/2013
Paul Carpenter (panel member).

14 **Title of the work:** Experiences with Mobile Processors for Energy Efficient HPC
Name of the event: Design, Automation & Test in Europe (DATE), 2013
Type of event: Conferences given
City of event: Grenoble, France
Date of event: 20/03/2013
Alex Ramirez; Nikola Rajovic; Alejandro Rico; James Vipond; Nikola Puzovic; Paul Carpenter (presenter).
"Experiences with Mobile Processors for Energy Efficient HPC".

15 **Title of the work:** The Next Generation Supercomputer
Name of the event: IS-ENES workshop on HPC for Climate Models
Type of event: Conferences given
City of event: Toulouse, France
Date of event: 30/01/2013
Alex Ramirez; Paul Carpenter (presenter).

16 **Title of the work:** The Mont-Blanc Approach Towards Exascale; Leader discussion section on Advanced Architecture.
Name of the event: BUX Bull User Group
Type of event: Conferences given
City of event: Warwick, United Kingdom
Date of event: 05/09/2012
Alex Ramirez; Paul Carpenter (presenter).

R&D management and participation in scientific committees

Scientific, technical and/or assessment committees

1 **Committee title:** Leader of Working Group on HPC application evolution and requirements
Affiliation entity: EuroLab-4-HPC
Start-End date: 01/09/2015 - 31/08/2017

2 **Committee title:** Milan Pavlovic PhD predefence (Secretari)
Start date: 02/10/2015

3 **Committee title:** Vinoth Elangovan PhD predefence (Vocal)
Start date: 13/11/2014

4 **Committee title:** Tassadaq Hussain PhD Predefence Committee (President)
Start date: 03/10/2014

5 **Committee title:** Member of EESI2 working group on energy efficiency. The main goals of the second European Exascale Software Initiative (EESI2) were to elaborate an evolutive European vision and roadmap and to propose recommendations to address the challenges of Extreme Data and Extreme Computing on the new generation of Exascale computers expected in 2020.
Start date: 20/06/2014

6 **Committee title:** European Technology Platform for High Performance Computing (ETP4HPC) Strategic Research Agenda Co-chair Working Group on Programming Models. ETP4HPC is the industry-led forum that, in dialog with the European Commission, defines the European HPC technology research priorities to achieve EU growth, competitiveness and sustainability
Geographical area: European Union
Affiliation entity: European Technology Platform for High-Performance Computing (ETP4HPC) **Type of entity:** Associations and Groups
City affiliation entity: Amsterdam, Noord-Holland, Holland
Start date: 25/05/2012

7 **Committee title:** IEEE IPDPS 2013 Program Committee
Geographical area: Non EU International

Organization of R&D activities

1 **Title of the activity:** DTHPC: Workshop on Disruptive Technologies in High-Performance Computing in the Next Decade
Type of activity: Workshop
City of event: Stockholm, Sweden
Convening entity: HiPEAC
Type of participation: Organiser
Start-End date: 23/01/2017 - 25/01/2017

2 **Title of the activity:** EUROSERVER: Green Data Centers / Microserver: System architecture, Software tools
Type of activity: Workshop
City of event: Stockholm, Sweden
Convening entity: HiPEAC **Type of entity:** Associations and Groups
Type of participation: Organiser
Start-End date: 23/01/2017 - 25/01/2017

3 **Title of the activity:** EuroLab-4-HPC: Fostering Excellence in HPC System Research. Co-organiser.
Type of activity: Workshop
City of event: Milan, Italy
Type of participation: Organiser
Start-End date: 21/09/2015 - 21/09/2015 **Duration:** 1 day

Evaluation and revision of R&D projects and articles

Performed tasks: Member of IPDPS 2013 Program Committee. Reviewer for Microprocessors and Microsystems (2011, 2016), IEEE Transactions on Parallel and Distributed Systems (2012, 2013), ICCD 2012, IEEE IPDPS 2013 PhD Forum, International Journal of Parallel Programming (2011, 2012) and IEEE Access (2014). Reviewed papers for IPDPS 2011, Euro-Par 2012, TACO 2012 and Euro-Par 2013.

Other achievements

Stays in public or private R&D centres

1 **Entity:** Berkeley Design Technology, Inc. (BDTI)
City of entity: Berkeley, United States of America
Start-End date: 25/07/2005 - 28/10/2005 **Duration:** 3 months
Goals of the stay: Contracted
Provable tasks: Performance analysis of multimedia codec and micro-benchmarks on ARM11 and ARM Cortex-A8 processor. Delivered two-day training course to BDTI engineers.

2 **Entity:** ARM Limited **Type of entity:** Business
City of entity: Cambridge, East Anglia, United Kingdom
Start-End date: 16/06/2003 - 08/04/2005 **Duration:** 1 year - 10 months
Goals of the stay: Contracted
Provable tasks: Part of the small team (<5 people) in the ARM Research Group (corporate headquarters in Cambridge, UK) that designed the ARM Advanced SIMD / NEON vector ISA. Inventor on one related worldwide patent. Author of NEON software training material (presentation and document "NEON Code Examples", RDB01-GENC-003057). Advanced SIMD was introduced in ARM Cortex-A8 (2005) and the design has changed little as of 2015. Advanced SIMD is mandatory in the latest ARM Architecture (ARMv8-A), and in 64-bit mode it is the only support for SIMD.

3 **Entity:** Cirrus Logic
City of entity: Denver, United States of America
Start-End date: 05/10/1998 - 16/10/1998 **Duration:** 10 days
Goals of the stay: Contracted
Provable tasks: Optimisation of HDD firmware including servo control algorithm. Training for Cirrus Logic and customers.

Obtained grants and scholarships

1 **Name of the grant:** King's Scholarship
Aims: Pre-doctoral
Awarding entity: King's College, Cambridge **Type of entity:** University Centres and Structures and Associated Bodies
Conferral date: 1995 **Duration:** 1 year
Entity where activity was carried out: University of Cambridge

2 **Name of the grant:** King's Scholarship
Aims: Pre-doctoral
Awarding entity: King's College Cambridge **Type of entity:** University Centres and Structures and Associated Bodies
Conferral date: 1994

Other types of collaboration with researchers or technologists

Name principal investigator (PI, Co-PI....): Per Stenstrom
Description of the collaboration: Proofreader for HiPEACinfo Newsletter
Start date: 28/05/2012 **Duration:** 3 years - 6 months
Relevant results: Proofreader for HiPEACinfo newsletter physically distributed to 500 researchers from academia and industry, and company managers in Europe, America and Asia

Scientific societies and professional associations

1 **Name of the society:** Institute of Electrical and Electronics Engineers (IEEE)
Professional category: Member
Start date: 01/01/2004

2 **Name of the society:** Association of Computing Machinery
Professional category: Lifetime Professional Member
Start date: 01/12/2002

Co-operation networks

1 **Name of the network:** Full Member
Identification of the network: European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
Start date: 30/04/2012

2 **Name of the network:** Member
Identification of the network: Association of Independent Computer Specialists
Start date: 19/05/2003 **Duration:** 2 years

Prizes, mentions and distinctions

1 **Description:** IEEE Transactions on Computers Featured Article of the Month January 2016
Awarding entity: IEEE Computer Society **Type of entity:** Associations and Groups
Conferral date: 01/2015
Recognition linked: Radojkovic et al is featured paper of the month (of 28 papers published) for January 2016 issue of IEEE Transactions on Computers (impact factor 1.659). The article is promoted on the journal's website and is freely available for one month. It is also promoted by videos in English and Chinese.

2 **Description:** Diploma in recognition for Best Student Paper
Awarding entity: UPC Consell Social **Type of entity:** University Centres and Structures and Associated Bodies
City awarding entity: Barcelona, Catalonia, Spain

Conferral date: 01/09/2014

3 **Description:** Best Paper Award
Awarding entity: Third International Workshop on On-chip Memory Hierarchies and Interconnects: Organisation, Management and Implementation
City awarding entity: Porto, Portugal
Conferral date: 25/08/2014

4 **Description:** Best Student Paper Award
Awarding entity: International Conference for High Performance Computing, Networking, Storage and Analysis (SC13)
City awarding entity: Denver, United States of America
Conferral date: 22/11/2013

5 **Description:** Finalist Fundación Repsol Entrepreneurship Fund 2013
Awarding entity: Fundación Repsol
City awarding entity: Madrid, Spain
Conferral date: 22/05/2013
Recognition linked: I was one of the four co-founders of Talaia Systems, an attempted start-up to commercialise the technology from the Mont-Blanc project. We aimed to build high-performance computing systems using mobile system-on-chips, and we had discussions with several vendors and potential investors.

6 **Description:** Winner International Science & Engineering Visualisation Challenge (video)
Awarding entity: National Science Foundation and Science Magazine
Conferral date: 01/11/2012
Recognition linked: Narrator of video "Alya Red, a Computational Heart", which received first place.

7 **Description:** HiPEAC Paper Award 2012
Awarding entity: European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
Conferral date: 2012
Recognition linked: Prize recognizing paper in MICRO-45 (2012). The HiPEAC Paper Award aims to encourage HiPEAC members to publish their work at highly competitive conferences in which Europe is not strongly represented.

8 **Description:** HiPEAC Technology Transfer Award
Awarding entity: European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
Conferral date: 2012
Recognition linked: Member of the team that received the HiPEAC Technology Transfer Award for the CARMA (CUDA on ARM) development kit

9 **Description:** Best Paper Award
Awarding entity: International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS Workshop 2009)
City awarding entity: Samos, Greece
Conferral date: 23/07/2009

10 **Description:** King's Scholarship (1995--1996)
Awarding entity: King's College, University of Cambridge
City awarding entity: Cambridge, United Kingdom

Conferral date: 1995
Recognition linked: The King's Scholar (K.S.) is awarded for obtaining a first class in the annual examination

11 **Description:** King's Scholar (1994--1995)
Awarding entity: King's College, University of Cambridge **Type of entity:** University
City awarding entity: Cambridge, United Kingdom
Conferral date: 1994
Recognition linked: The King's Scholar (K.S.) is awarded for obtaining a first class in the annual examination