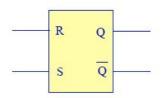
Sistemas Digitais

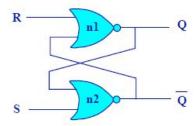
Flip-Flop, Latches e Registradores.

O Latch RS

símbolo



circuito com portas nor



R	s	Q_{t+1}	comentário
0	0	Qt	mantém estado anterior
0	1	1	estado set
1	0	0	estado reset
1	1	-	proibido

O Latch RS Controlado

símbolo

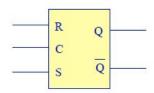
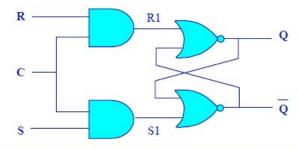


tabela de transição de estados

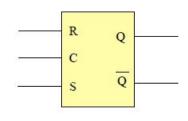
circuito com portas nor e and



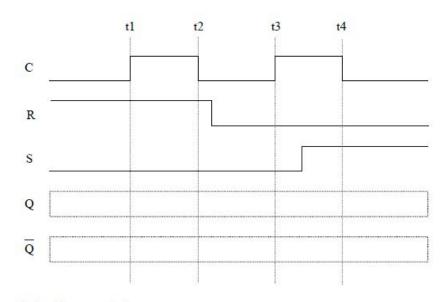
C	R	s	Q_{t+1}	comentário
0	X	X	Qt	mantém estado anterior
1	0	0	Qt	mantém estado anterior
1	0	1	1	estado set
1	1	0	0	estado reset
1	1	1	=	proibido

O Latch RS Controlado





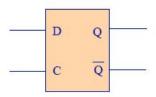
			N. I
C	R	S	Q _{t+1}
0	X	X	Q _t
1	0	0	Q _t
1	0	1	1
1	1	0	0
1	1	1	

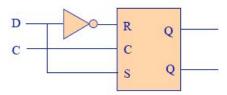


O Latch D

símbolo

circuito a partir do latch RS controlado

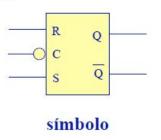




C	D	Q_{t+1}	comentário
0	X	Q _t	mantém estado anterior
1	0	0	estado reset
1	1	1	estado set

Latches com ativação em lógica complementar

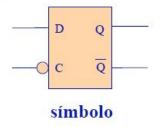
Latch RS



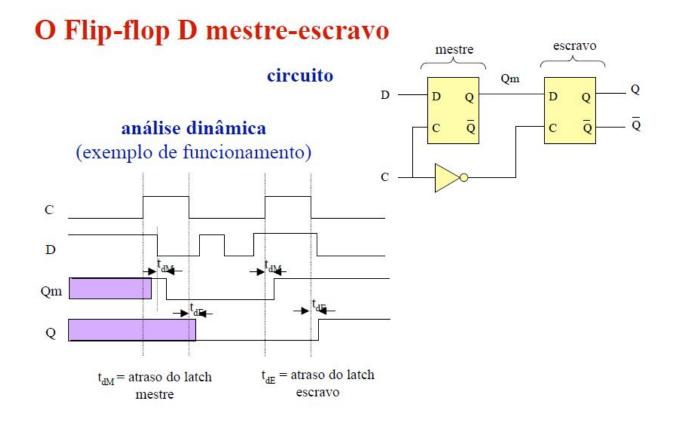
C	R	S	Q_{t+1}
1	X	X	Qt
0	0	0	Q_t
0	0	1	1
0	1	0	0
0	1	1	

tabela de transição de estados

Latch D

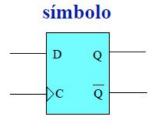


C	D	Q_{t+1}
1	X	Q _t
0	0	0
0	1	1



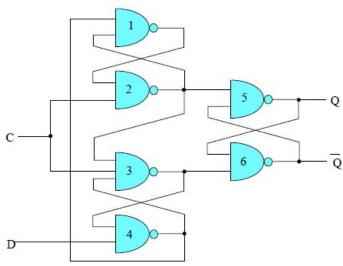
O Flip-flop D disparado pela borda ascendente

(ou Flip-flop D sensível à borda ascendente)

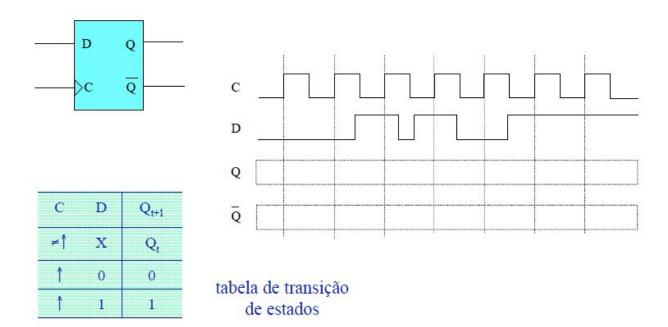


C	D	Q _{t+1}
≠ ↑	X	Qt
1	0	0
1	1	1

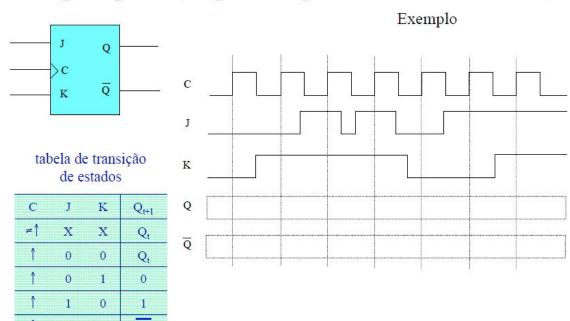




O Flip-flop D disparado pela borda ascendente



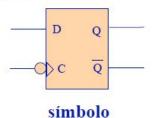
O Flip-flop JK (disparado pela borda ascendente)



Flip-flops disparados pela borda descendente

(ou Flip-flops sensíveis à borda descendente)

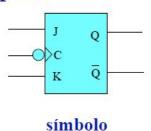


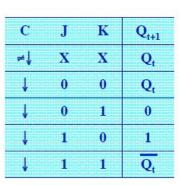


C	D	Q_{t+1}
≠↓	X	Q _t
1	0	0
1	1	1

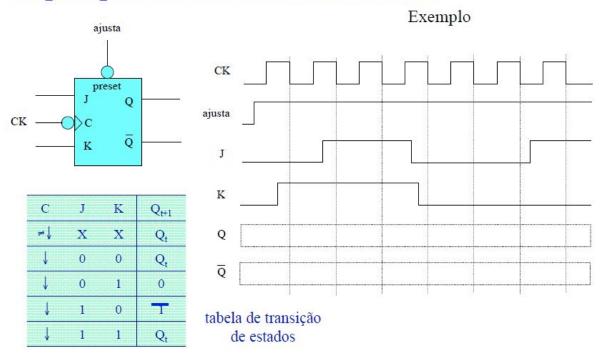
tabela de transição de estados

Flip-flop JK

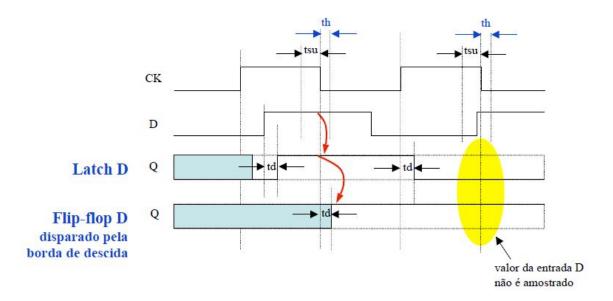




Flip-flops com set e reset assíncronos



Tempo de Preparação - tp (setup time)
Tempo de Manutenção - tsu (hold time)
Atraso de Propagação - td ou tp (propagation delay)

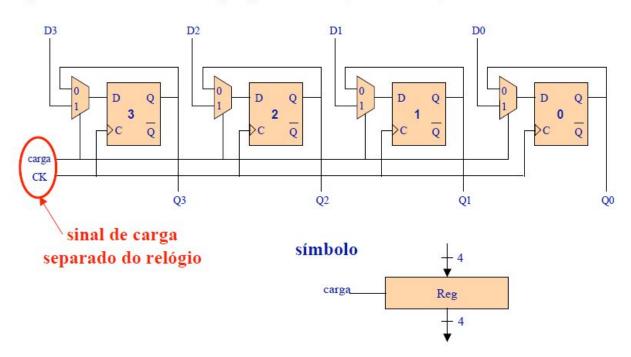


Registradores

Registrador com carga paralela (versão 1)

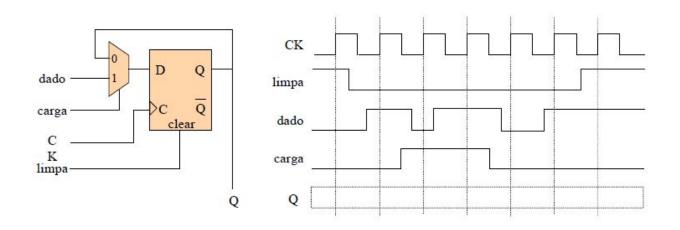
entradas individuais D3 D2 D4 D5 D5 D6 D7 D7 D7 D8 D8 D9 D9 Q0 D9 Q1 D9 Q0 Sinal de carga (relógio)

Registrador com carga paralela (versão 2)

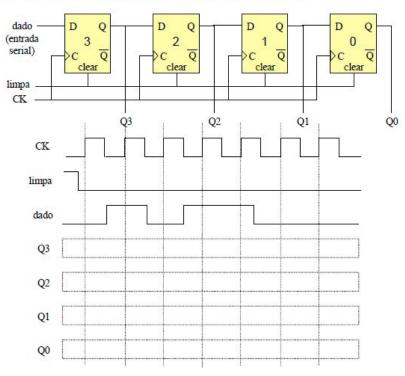


Registrador com carga paralela (versão 2)

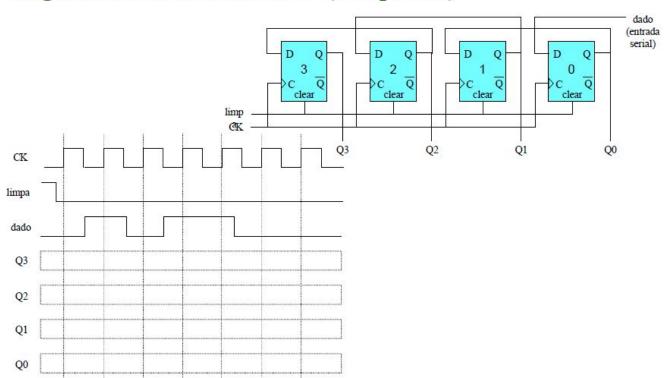
Exemplo



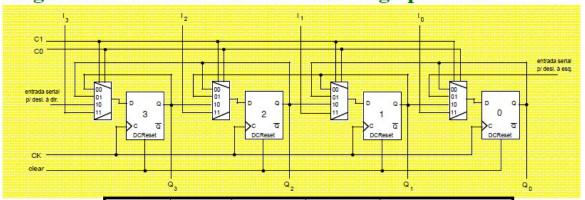
Registrador de deslocamento (à direita)



Registrador de deslocamento (à esquerda)

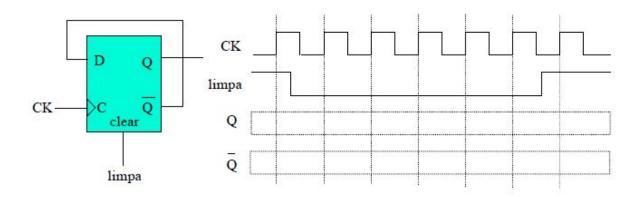


Registrador de deslocamento com carga paralela



clear	CK	C1	C0	operação
0	≠ ↑	X	X	mantém conteúdo
0	1	0	0	mantém conteúdo
0	1	0	1	desloca à esquerda
0	1	1	0	desloca à direita
0	1	1	1	carga paralela
1	X	X	X	zera conteúdo

Registrador contador (1 bit)



Registrador contador (3 bits)

