Assignment 1
Cyclic Redundant Check

Grupo 5 Turma 1
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Encoder

- Approach using the Properties of the Remainder
  - 58 XOR gates needed
  - 9 XOR propagation time delays in the worst case
- Optimized solution
  - By doing the most common operations in parallel:
    - 38 XOR gates
    - 4 XOR propagation time delay in the worst case (r1,r5,r6)

Encoder

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	a0+a13	a1+a6	a1+a12	a2+a4	a2+a5	a3+a5	a3+a10	a4+a6	a7+a9	a8+a14	a8+a15	a10+a12	a11+a15	a10+a12+a14	a11+a13+a15	a8+a11+a14	a3+a5+a7	a1+a2+a4+a6	a0+a7+a9+a13
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0
4	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
2	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Encoder
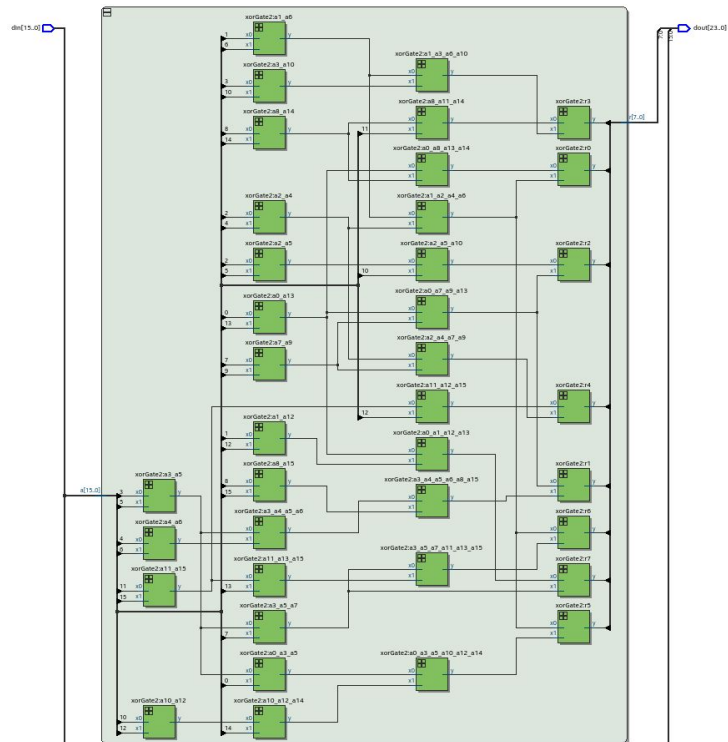
Checker

- After some reading, we followed what Allegro Microsystems does in their SPI and I2C sensors: a Linear Feedback Shift Register
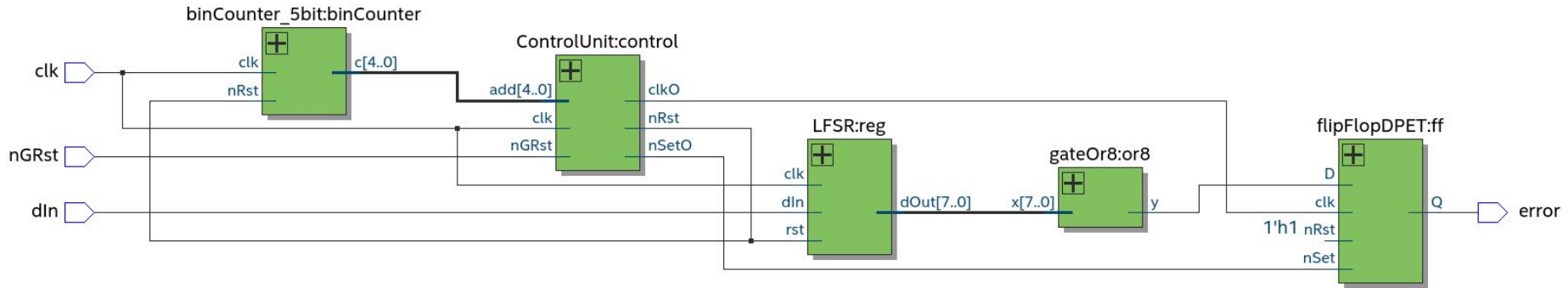
Checker

- Implementation cost
  - 5 bit binary counter
    - 3 AND gates
    - 4 XOR gates
    - 5 DFlipFlop
  - Control Unit
    - 4 NAND gates
    - 1 NOR gate
  - LSFR
    - 5 XOR gates
    - 8 DFlipFlop
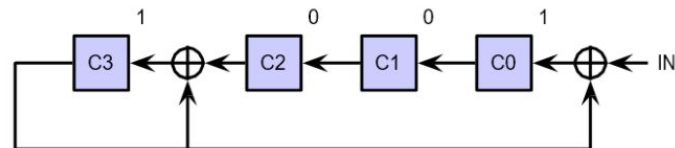 - 7 OR gates (for the gateOr8)
  - 1 DFlipFlop

Figure 2: Post-Multiply LFSR for G_1 = 11001 (PST-LFSR1).