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CENTROALGORITMI

Testbenches

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Escola de Engenharia
COMPETE
QREN QUADRO DE REFERÊNCIA ESTRATÉGICO NACIONAL
União Europeia
Fundo Europeu de Desenvolvimento Regional
FCT Fundação para a Ciência e a Tecnologia
MINISTÉRIO DA CIÊNCIA, TECNOLOGIA E ENSINO SUPERIOR Portugal

What is a testbench?

- Testbench is a program designed to generate predefined sequence of inputs and optionally observe outputs.
- It can be self-checking if output verification is automatic.
- In terms of input vectors to be used can be classified as:
  - Exhaustive
  - Golden vector
  - Random
- Testbench in verilog is a program that wraps around an actual design.

What is a testbench?

- Verification of outputs can be done during or after the simulation.
- Analysis of the result can be done through waveforms or log files with data about simulation.

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TestBench: Exhaustive

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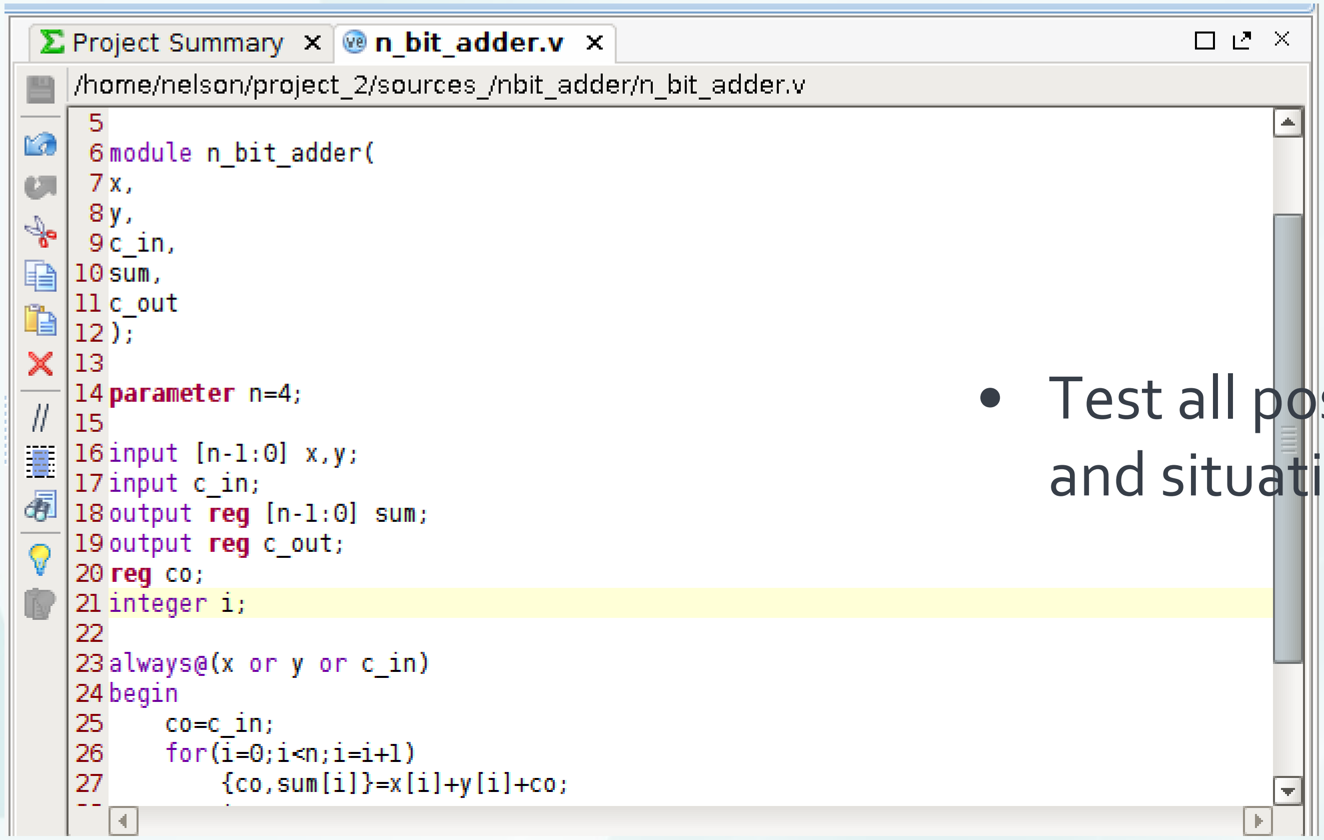
Project Summary | n_bit_adder.v

/home/nelson/project_2/sources_/nbit_adder/n_bit_adder.v

```

module n_bit_adder(
x,
y,
c_in,
sum,
c_out
);

parameter n=4;

input [n-1:0] x,y;
input c_in;
output reg [n-1:0] sum;
output reg c_out;
reg co;
integer i;

always@(x or y or c_in)
begin
    co=c_in;
    for(i=0;i<n;i=i+1)
        {co,sum[i]}=x[i]+y[i]+co;
```

- Test all possibilities and situations;

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TestBench: Exhaustive

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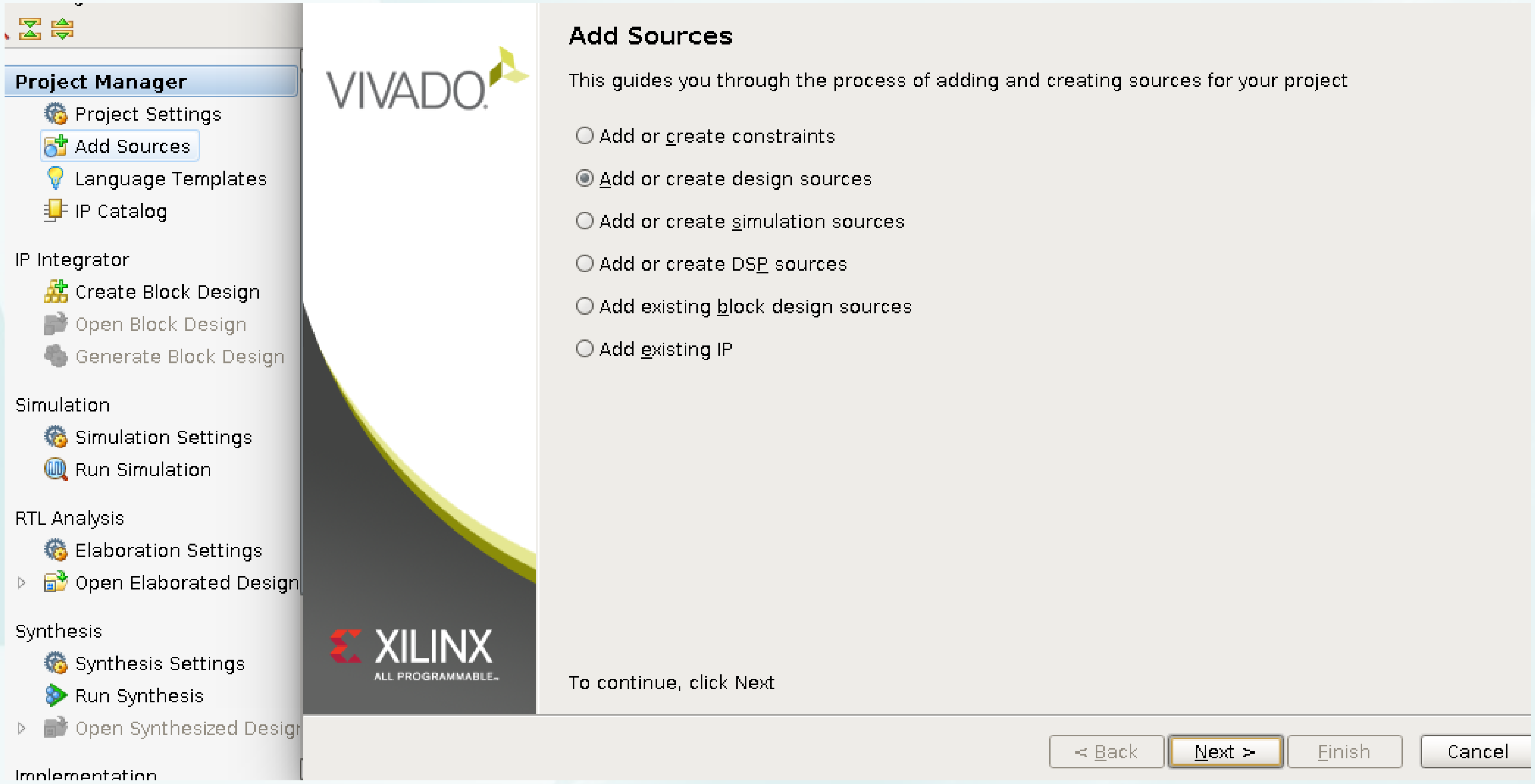

Add Sources

This guides you through the process of adding and creating sources for your project

- ○ Add or create constraints
- ● Add or create design sources
- ○ Add or create simulation sources
- ○ Add or create DSP sources
- ○ Add existing block design sources
- ○ Add existing IP

To continue, click Next

< Back | Next > | Finish | Cancel

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TestBench: Exhaustive

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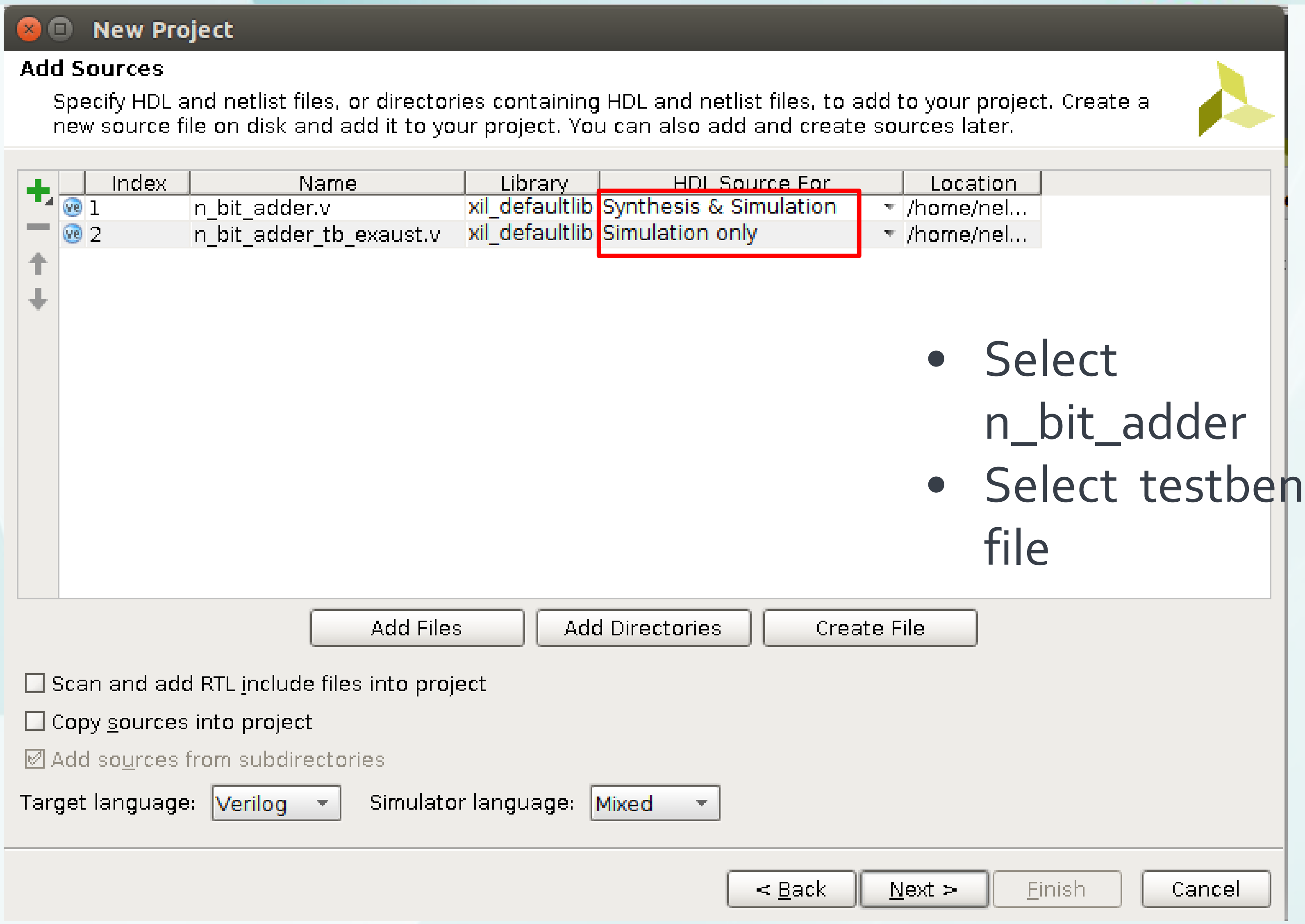
New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Index	Name	Library	HDL Source For	Location
1	n_bit_adder.v	xil_defaultlib	Synthesis & Simulation	/home/nel...
2	n_bit_adder_tb_exaust.v	xil_defaultlib	Simulation only	/home/nel...

☐ Scan and add RTL include files into project

☐ Copy sources into project

☑ Add sources from subdirectories

Target language: Verilog

Simulator language: Mixed

- Select n_bit_adder
- Select testbench file

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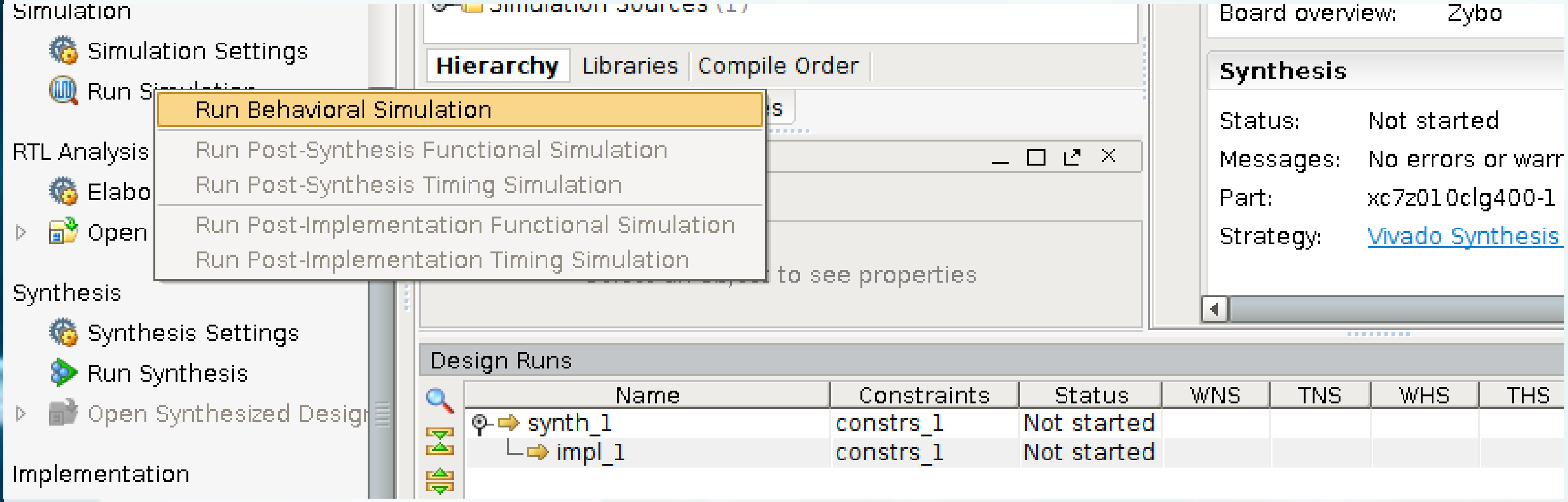

Board overview: Zybo

Synthesis

Status: Not started
Messages: No errors or warn
Part: xc7z010clg400-1
Strategy: Vivado Synthesis

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS
synth_1	constrs_1	Not started				
impl_1	constrs_1	Not started				

- Run Behavioral Simulation;

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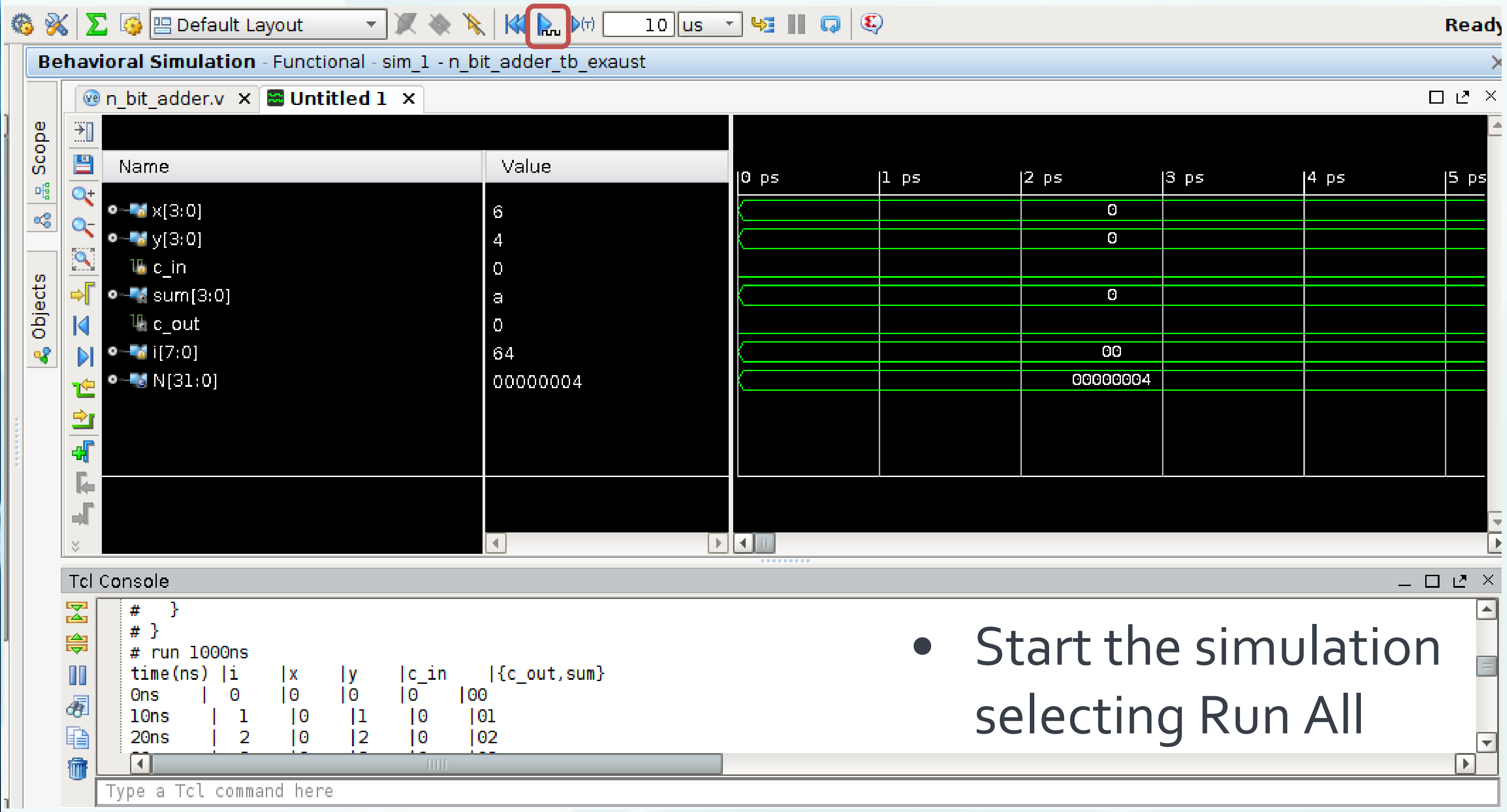
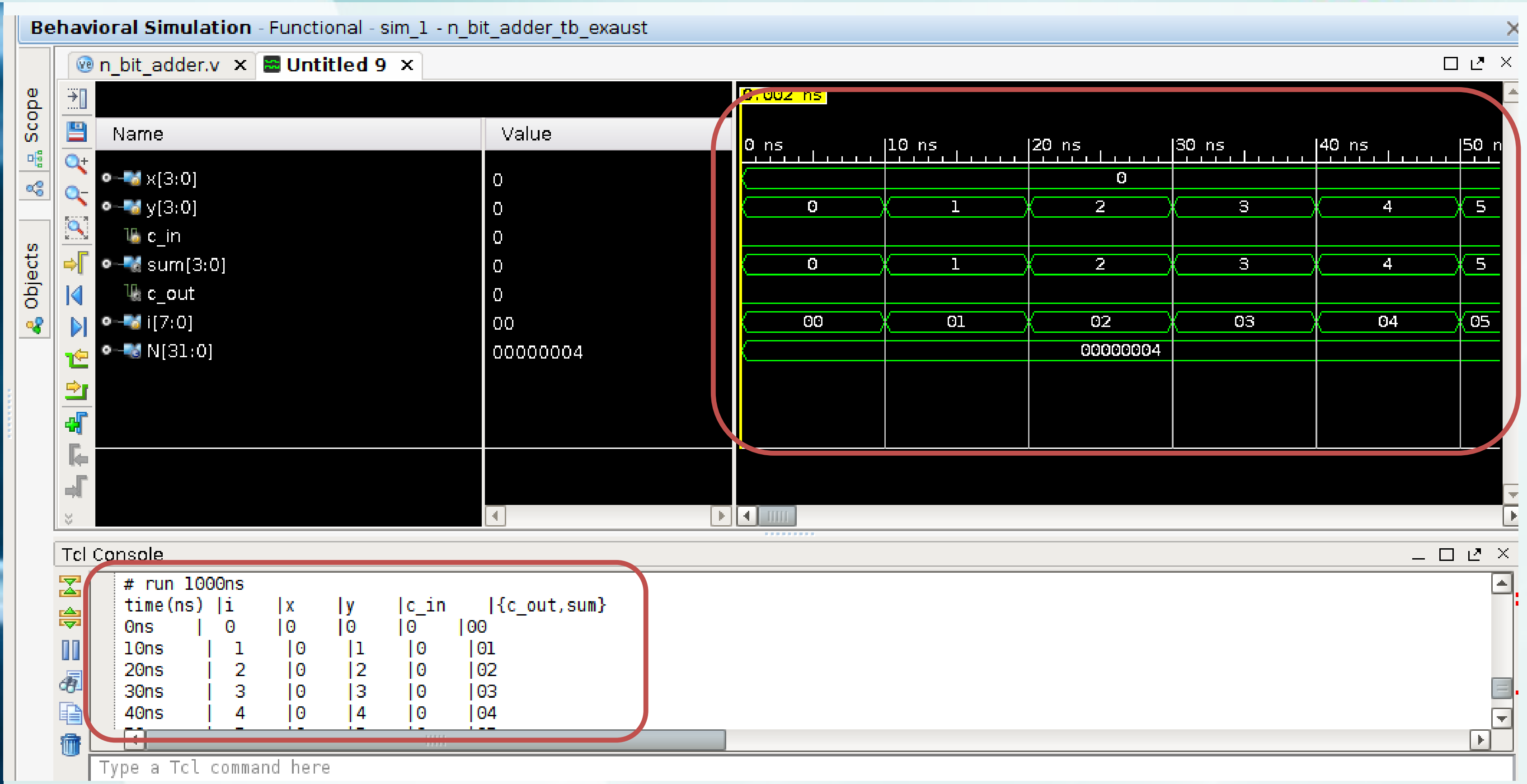


Name	Value
x[3:0]	6
y[3:0]	4
c_in	0
sum[3:0]	a
c_out	0
i[7:0]	64
N[31:0]	00000004

```
#   }
# }
# run 1000ns
time(ns) |i    |x    |y    |c_in    |{c_out,sum}
0ns      |  0  |0    |0    |0    |00
10ns     |  1  |0    |1    |0    |01
20ns     |  2  |0    |2    |0    |02
```

- Start the simulation selecting Run All

TestBench: Exhaustive



Behavioral Simulation - Functional - sim_1 - n_bit_adder_tb_exaust

Name	Value
x[3:0]	0
y[3:0]	0
c_in	0
sum[3:0]	0
c_out	0
i[7:0]	00
N[31:0]	00000004

```
# run 1000ns
time(ns) |i     |x    |y    |c_in    |{c_out,sum}
0ns     |  0    |0    |0    |0     |00
10ns     |  1    |0    |1    |0     |01
20ns     |  2    |0    |2    |0     |02
30ns     |  3    |0    |3    |0     |03
40ns     |  4    |0    |4    |0     |04
```

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TestBench: Golden Vectors

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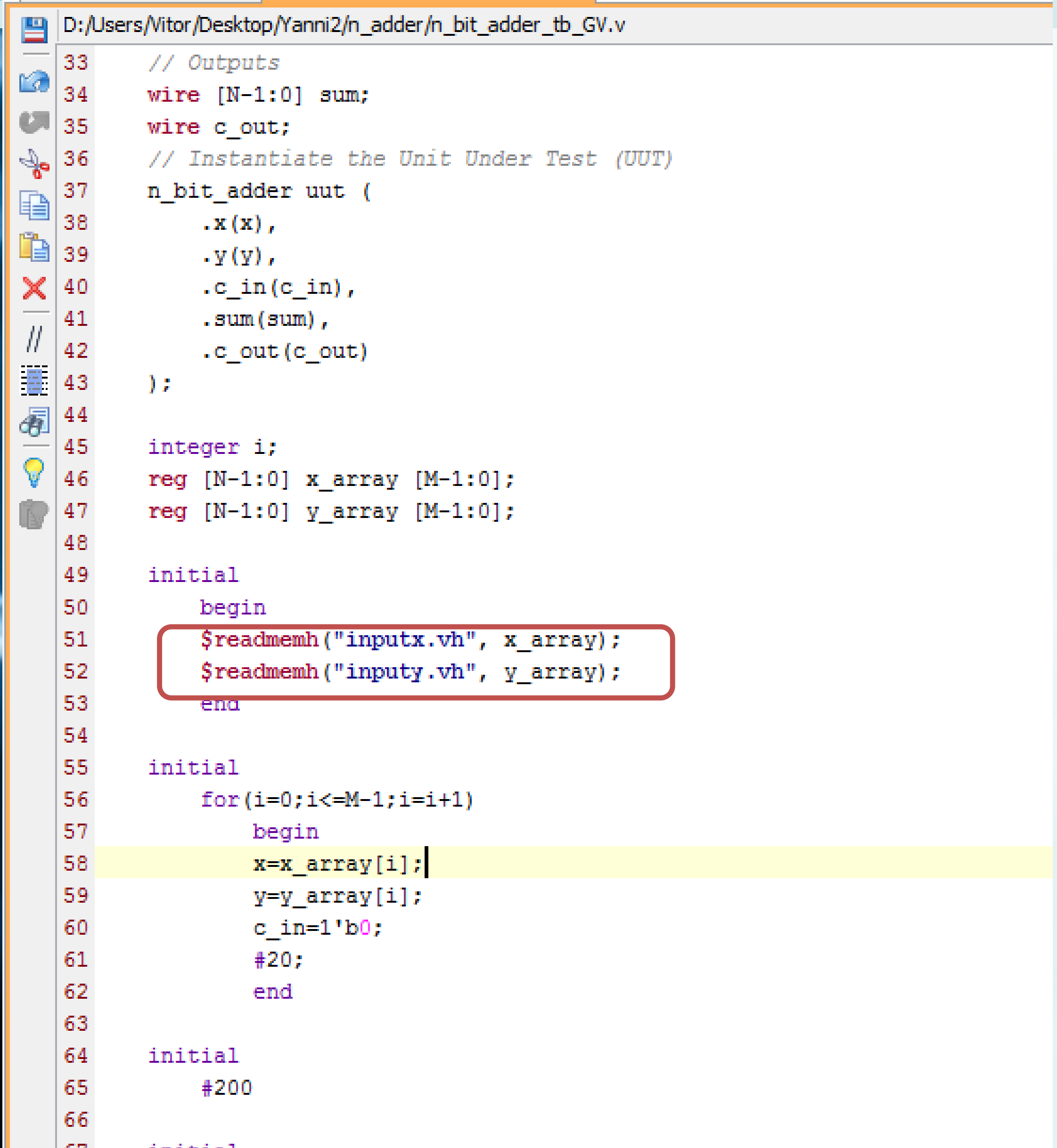
D:/Users/Vitor/Desktop/Yanni2/n_adder/n_bit_adder_tb_GV.v

```
    // Outputs
    wire [N-1:0] sum;
    wire c_out;
    // Instantiate the Unit Under Test (UUT)
    n_bit_adder uut (
        .x(x),
        .y(y),
        .c_in(c_in),
        .sum(sum),
        .c_out(c_out)
    );

    integer i;
    reg [N-1:0] x_array [M-1:0];
    reg [N-1:0] y_array [M-1:0];

    initial
        begin
        $readmemh("inputx.vh", x_array);
        $readmemh("inputy.vh", y_array);
        end

    initial
        for(i=0;i<=M-1;i=i+1)
            begin
            x=x_array[i];
            y=y_array[i];
            c_in=1'b0;
            #20;
            end

    initial
        #200

```

Test modules specifying conditions in text files;

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TestBench: Golden Vectors

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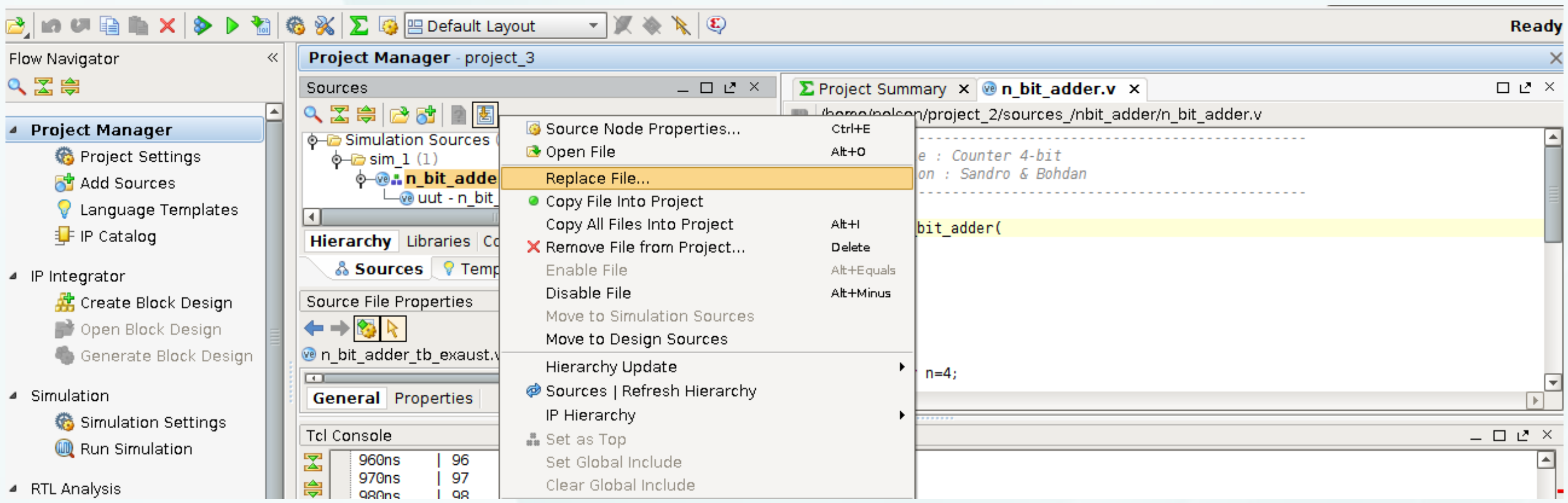

/home/nelson/project_2/sources_/nbit_adder/n_bit_adder.v

```
e : Counter 4-bit
on : Sandro & Bohdan

bit_adder(

n=4;
```

```
960ns | 96
970ns | 97
980ns | 98
```

- Replace the testbench file

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TestBench: Golden Vectors

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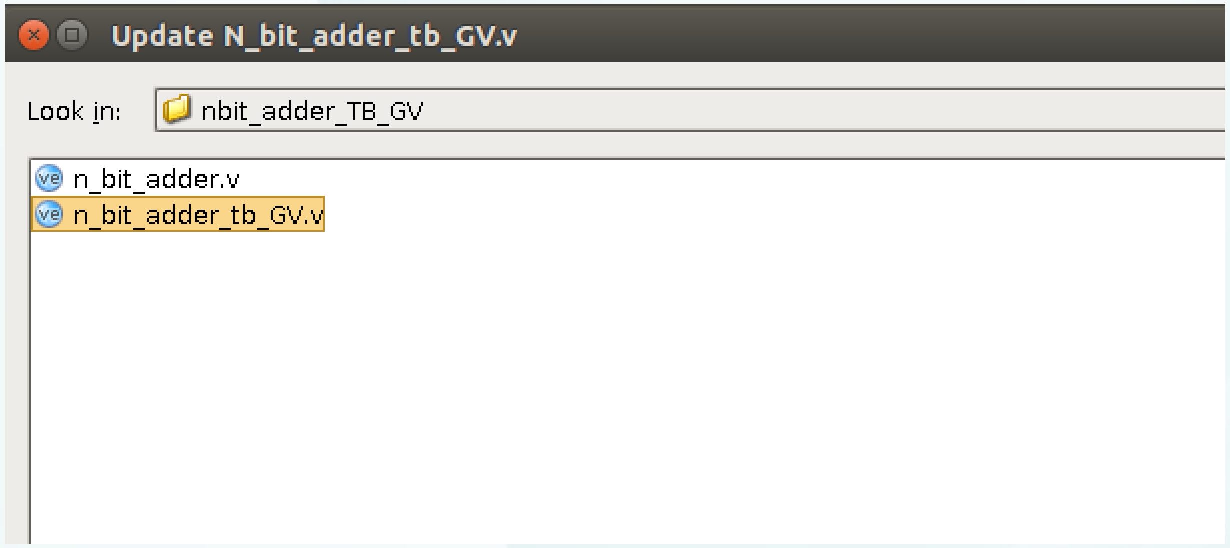

- Select the Golden Vector testbench file

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TestBench: Golden Vectors

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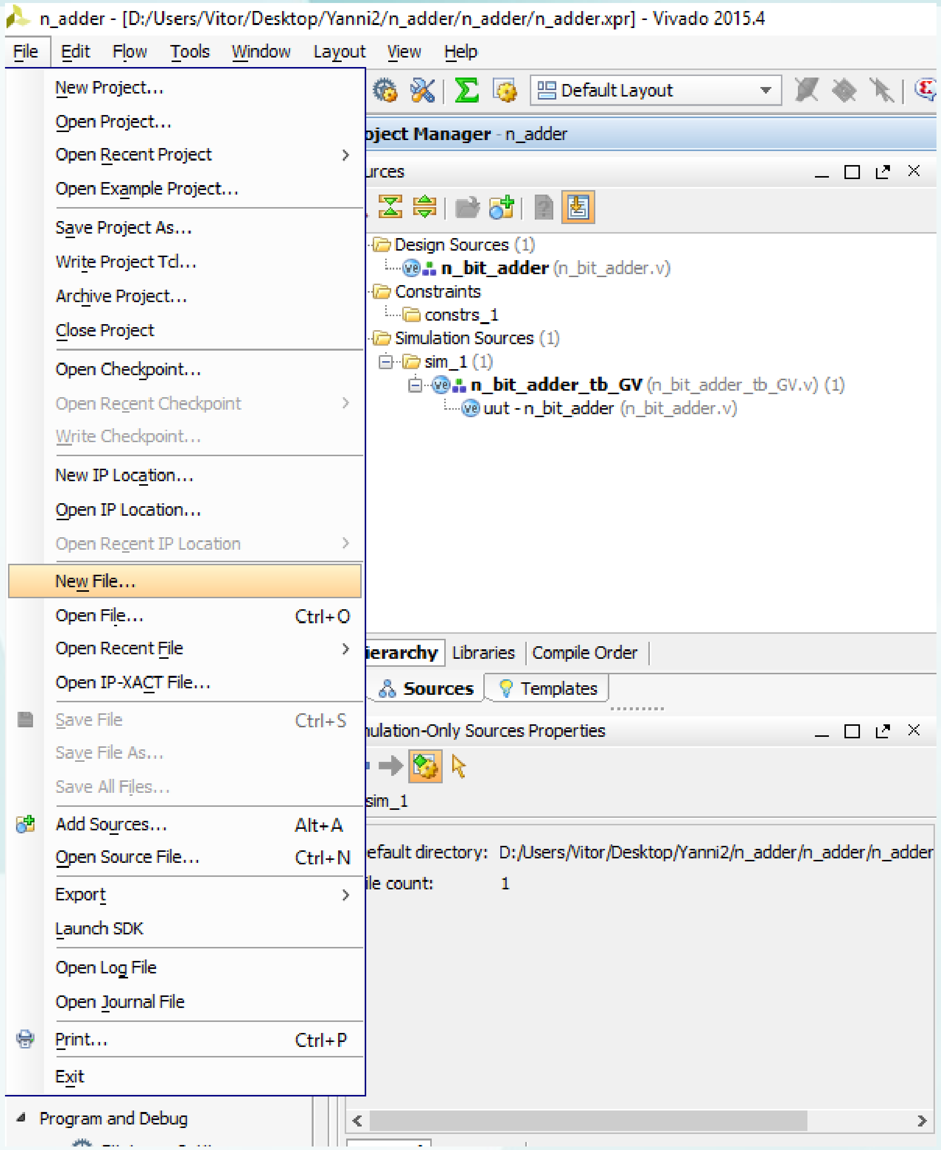
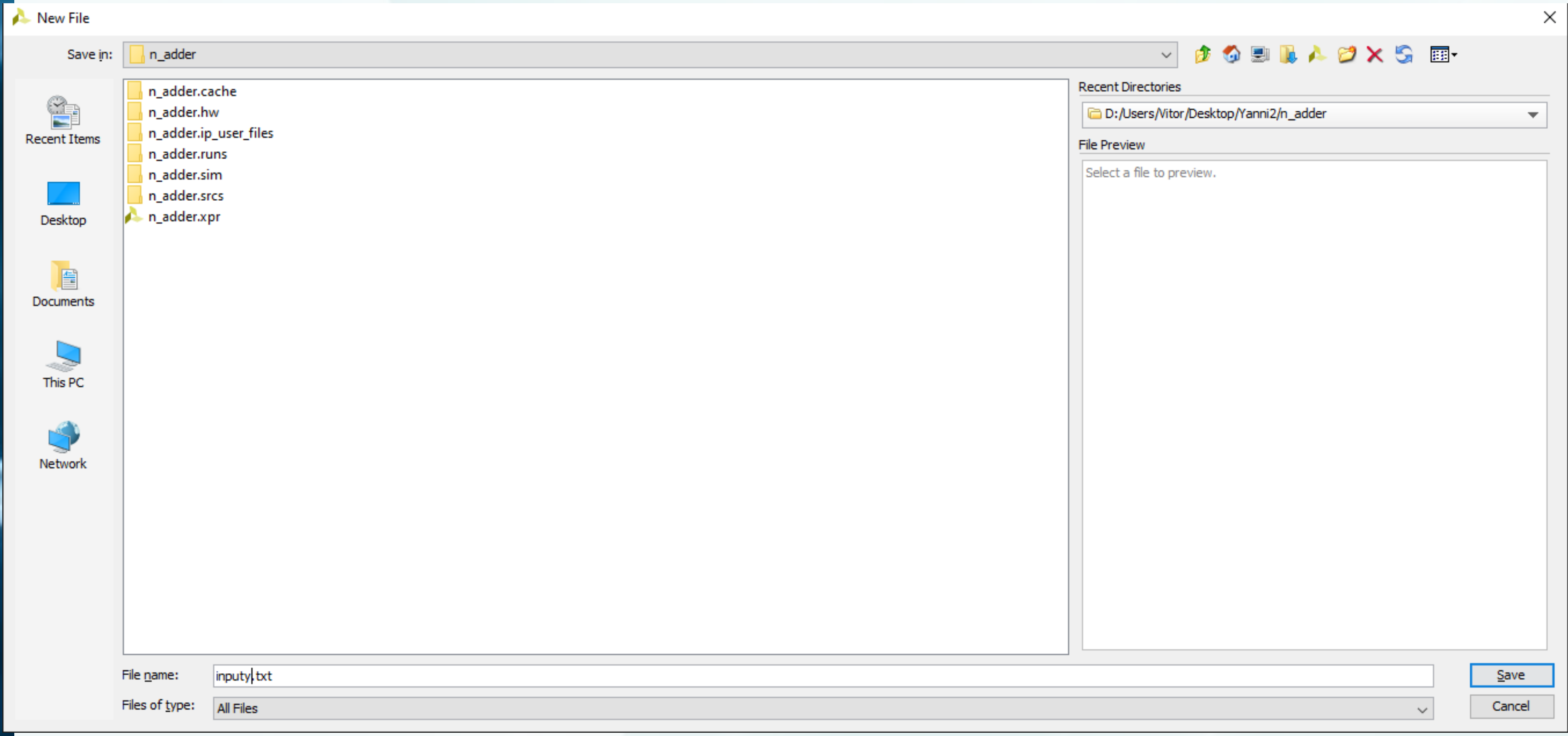

n_adder - [D:/Users/Vitor/Desktop/Yanni2/n_adder/n_adder/n_adder.xpr] - Vivado 2015.4

efault directory: D:/Users/Vitor/Desktop/Yanni2/n_adder/n_adder/n_adder
ile count: 1

- Create new files

TestBench: Golden Vectors



Save in: n_adder

n_adder.cache
n_adder.hw
n_adder.ip_user_files
n_adder.runs
n_adder.sim
n_adder.srcs
n_adder.xpr

Recent Directories: D:/Users/Vitor/Desktop/Yanni2/n_adder

File Preview: Select a file to preview.

File name: inputy.txt

Files of type: All Files

- Named:
  - inputx.txt
  - Inputy.txt

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TestBench: Golden Vectors

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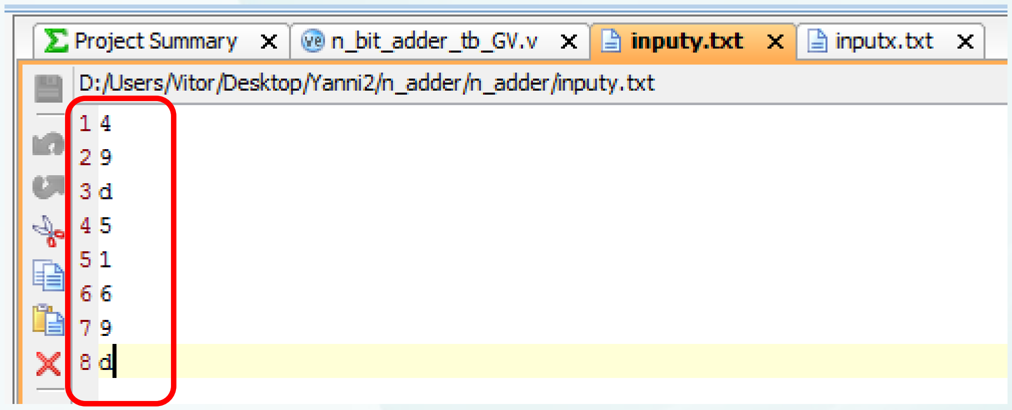

D:/Users/Vitor/Desktop/Yanni2/n_adder/n_adder/inputy.txt

```
4
9
d
5
1
6
9
d
```

- Fill the files

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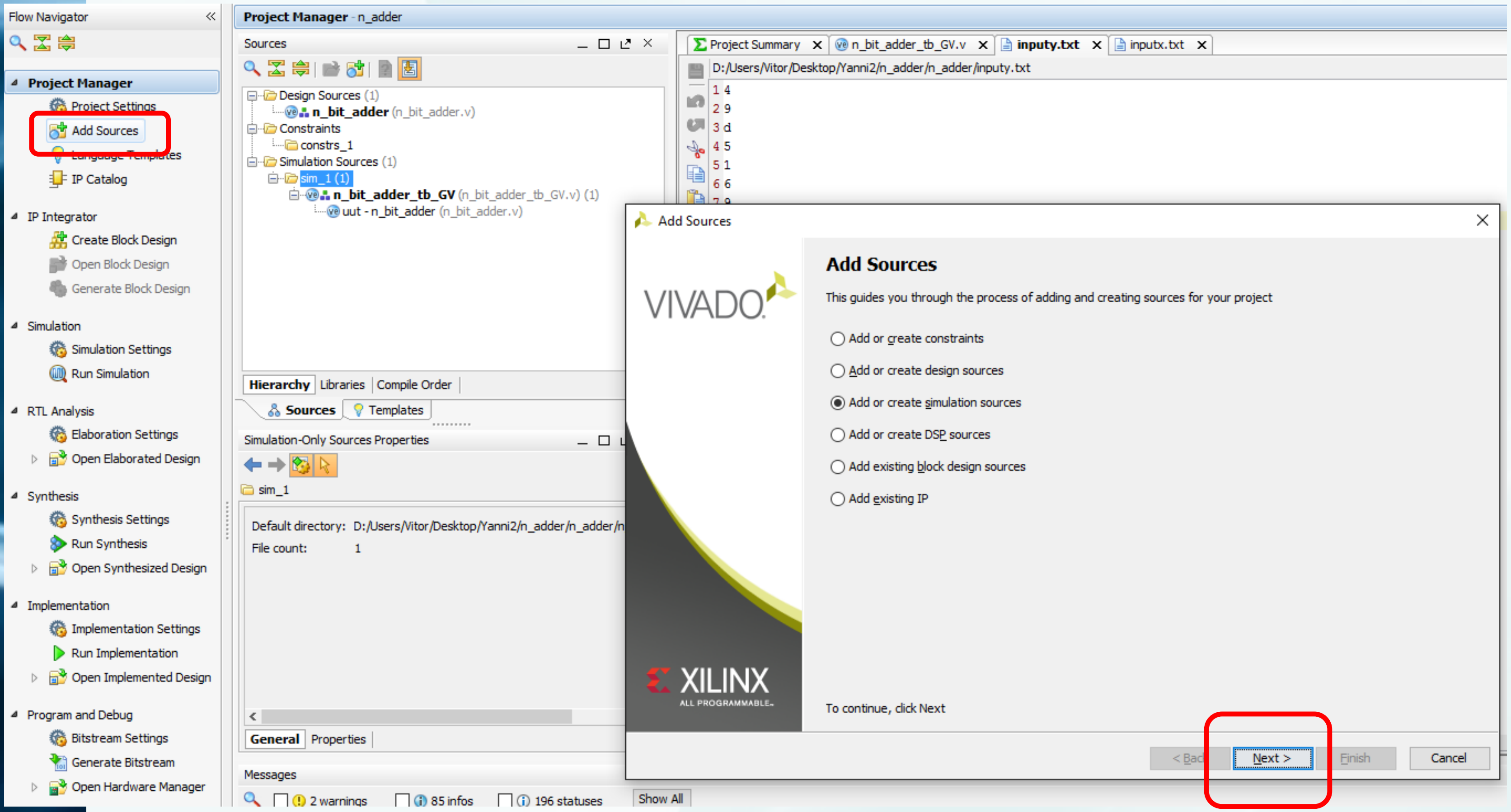


D:/Users/Vitor/Desktop/Yanni2/n_adder/n_adder/inputy.txt

```
1 4
2 9
3 d
4 5
5 1
6 6
7 9
```

Default directory: D:/Users/Vitor/Desktop/Yanni2/n_adder/n_adder/n
File count: 1

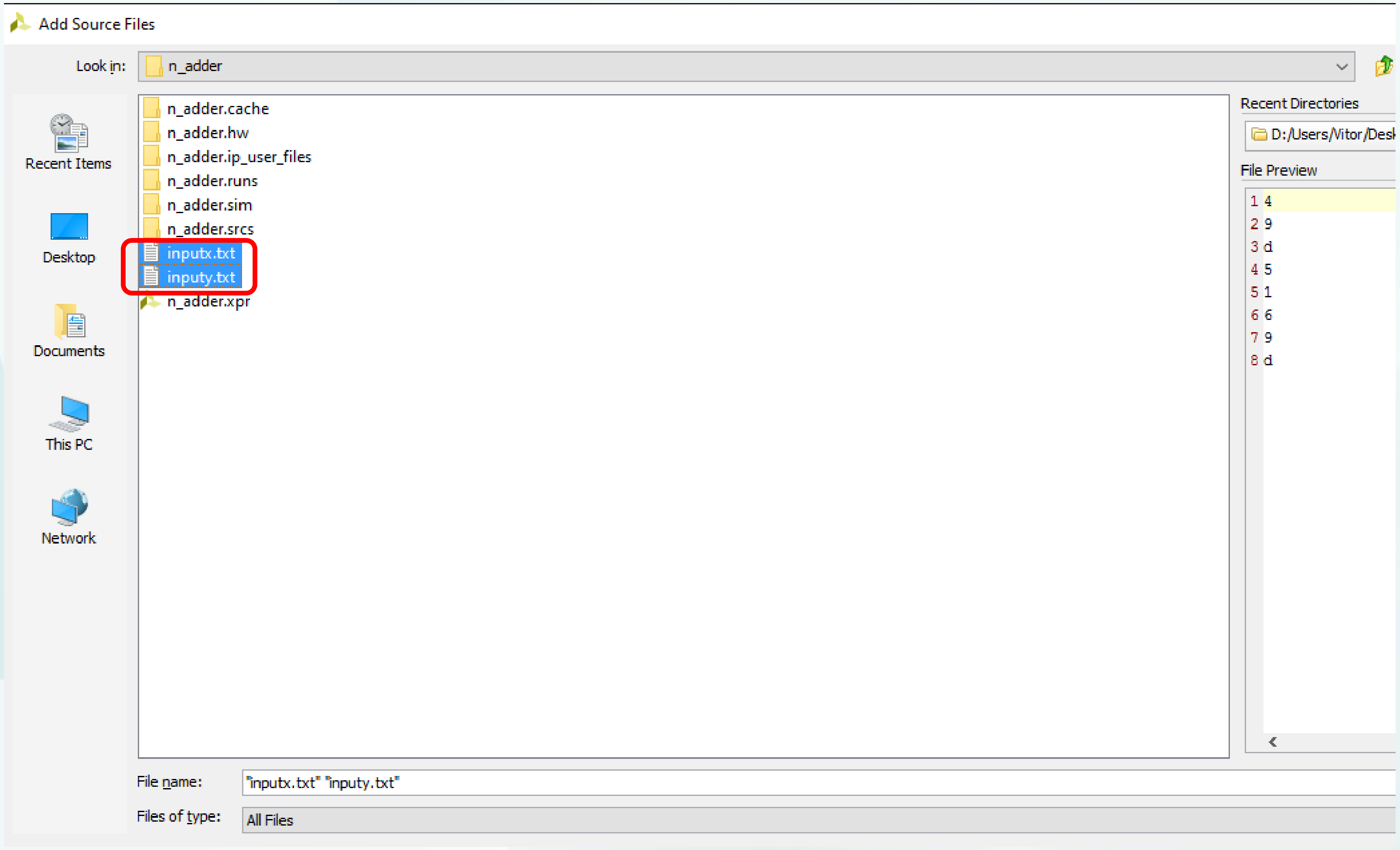
Add Sources

This guides you through the process of adding and creating sources for your project

- ( ) Add or create constraints
- ( ) Add or create design sources
- [✓ Add or create simulation sources]
- ( ) Add or create DSP sources
- ( ) Add existing block design sources
- ( ) Add existing IP

To continue, click Next

- Add the created files as simulation sources



Look in: n_adder

n_adder.cache
n_adder.hw
n_adder.ip_user_files
n_adder.runs
n_adder.sim
n_adder.srcs
inputx.txt
inputy.txt
n_adder.xpr

Recent Directories: D:/Users/Vitor/Desk

File Preview:

```
1 4
2 9
3 d
4 5
5 1
6 6
7 9
8 d
```

File name: "inputx.txt" "inputy.txt"

Files of type: All Files

- Add the created files as simulation sources

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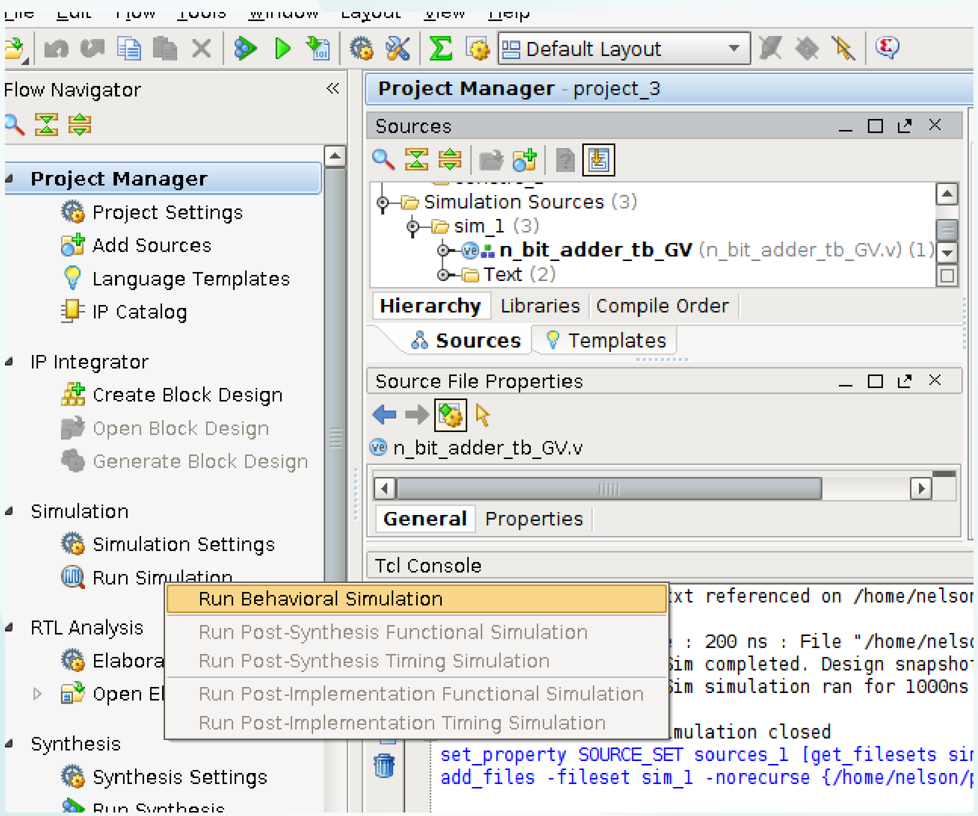
TestBench: Golden Vectors



```
xt referenced on /home/nelsor

: 200 ns : File "/home/nelsc
im completed. Design snapsho
im simulation ran for 1000ns

mulation closed
set_property SOURCE_SET sources_1 [get_filesets sir
add_files -fileset sim_1 -norecurse {/home/nelson/
```

- Run the Simulation

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TestBench: Golden Vectors

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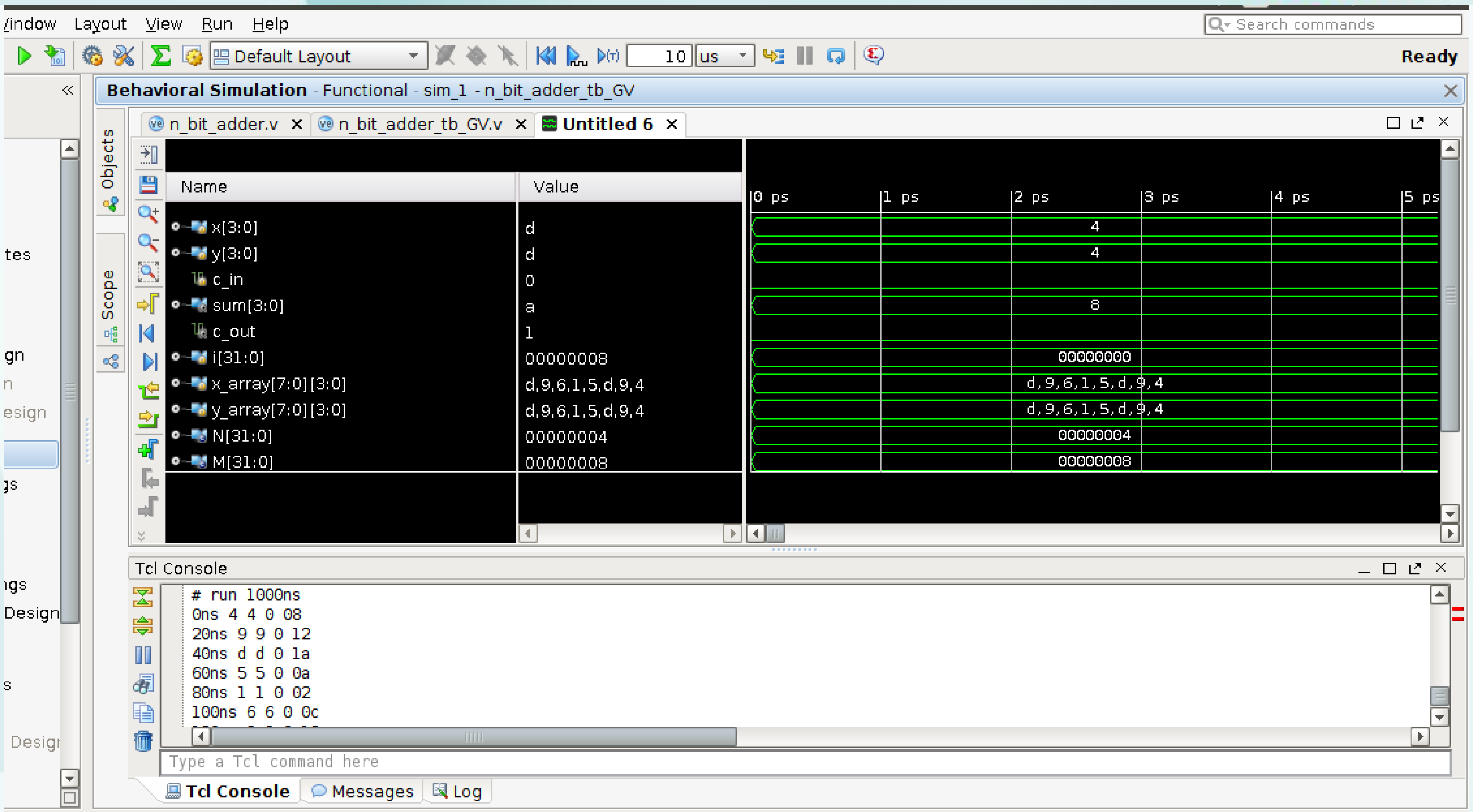
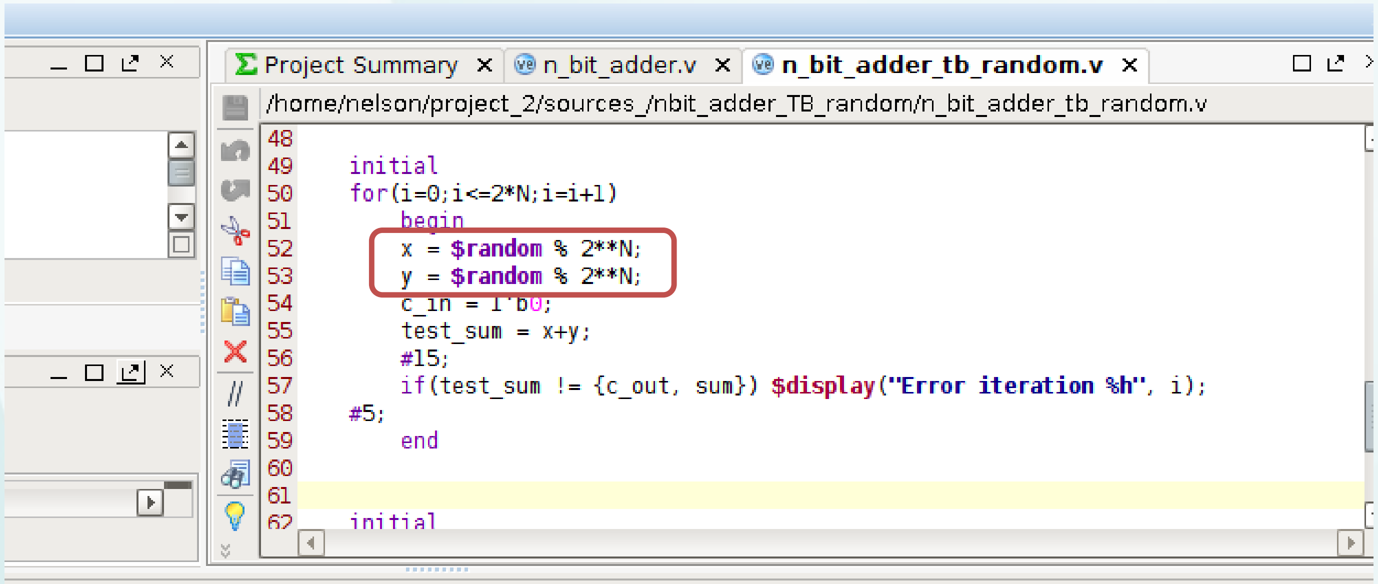


Name	Value
x[3:0]	d
y[3:0]	d
c_in	0
sum[3:0]	a
c_out	1
i[31:0]	00000008
x_array[7:0][3:0]	d,9,6,1,5,d,9,4
y_array[7:0][3:0]	d,9,6,1,5,d,9,4
N[31:0]	00000004
M[31:0]	00000008

```
# run 1000ns
0ns  4 4 0 08
20ns  9 9 0 12
40ns  d d 0 1a
60ns  5 5 0 0a
80ns  1 1 0 02
100ns  6 6 0 0c
```

- Verify the results;

TestBench: Random


Project Summary n_bit_adder.v n_bit_adder_tb_random.v

/home/nelson/project_2/sources_/nbit_adder_TB_random/n_bit_adder_tb_random.v

```

    initial
    for(i=0;i<=2*N;i=i+1)
        begin
        x = $random % 2**N;
        y = $random % 2**N;
        c_in = 1'b0;
        test_sum = x+y;
        #15;
        if(test_sum != {c_out, sum}) $display("Error iteration %h", i);
    #5;
        end

    initial
```

- Test random situations;

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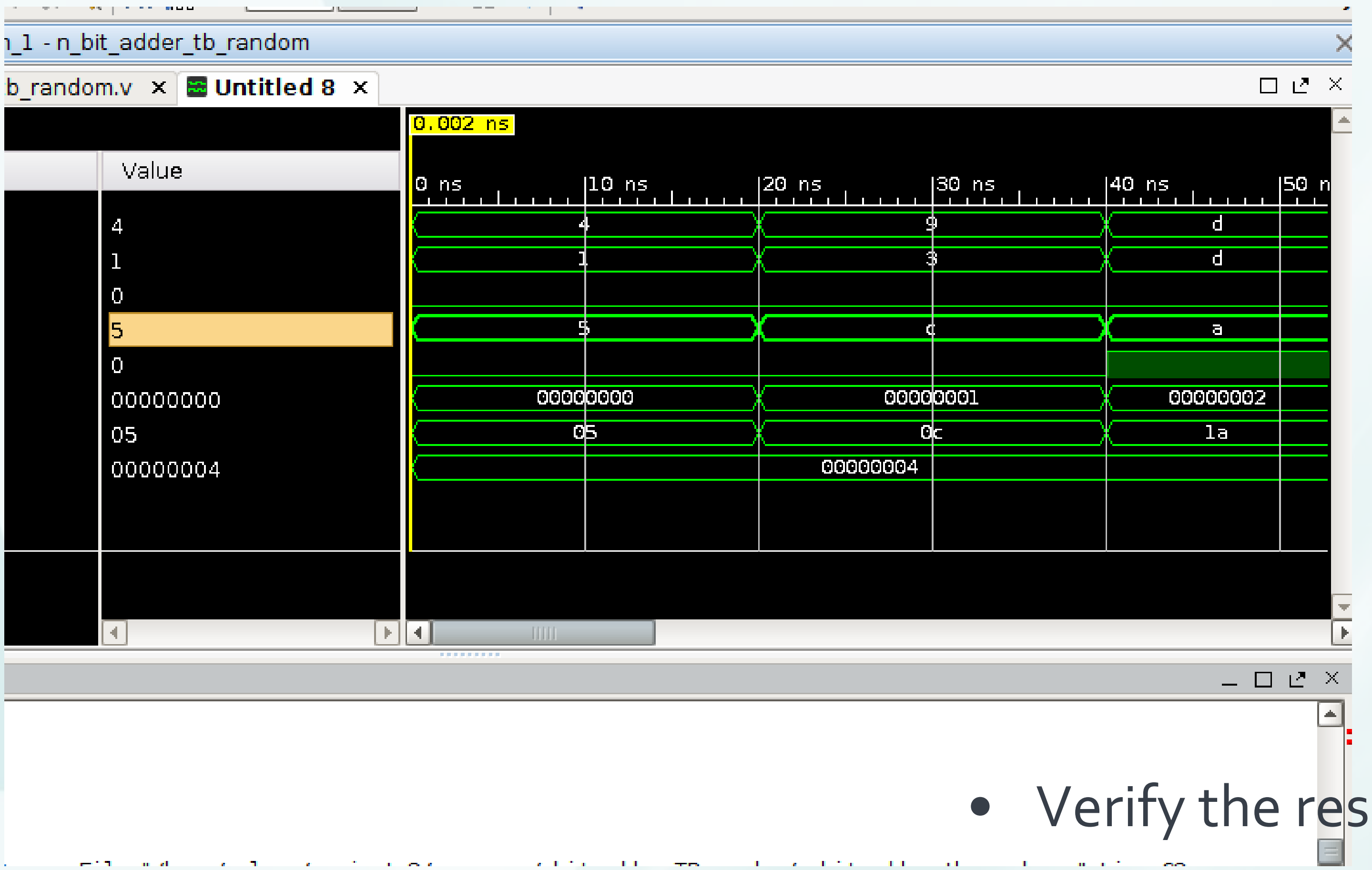
TestBench: Golden Vectors



```
4          4          9          d
1          1          3          d
0
5          5          c          a
0
00000000   00000000   00000001   00000002
05         05         0c         1a
00000004   00000004
```

- Verify the results;