

Xilinx Vivado Logic Analyzer



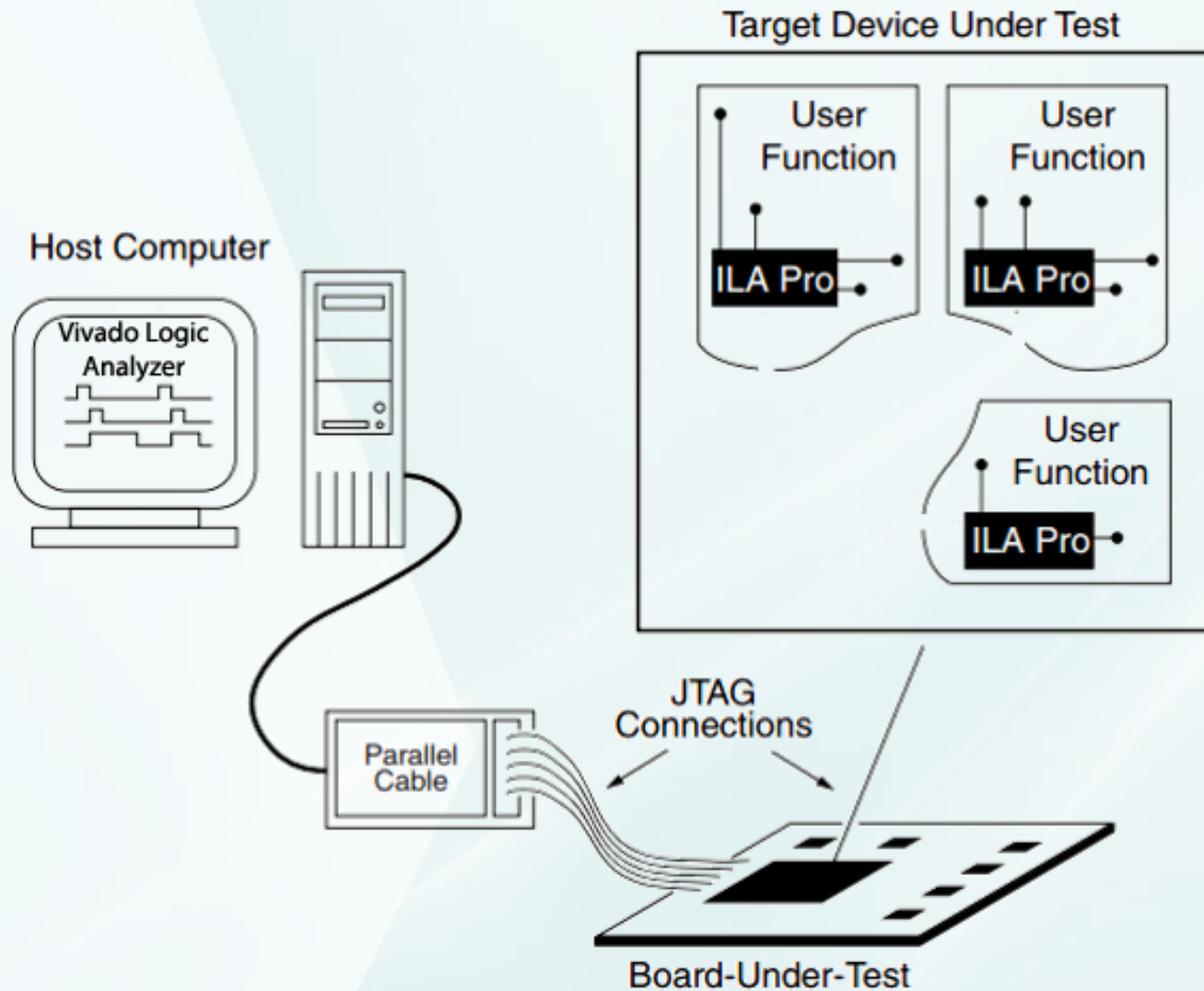
Group Stage

- This document contains a tutorial designed to help debug complex FPGA designs
- This tutorial describes the steps involved in taking a small RTL design and the multiple ways of inserting the **Integrated Logic Analyzer** (ILA) core to help debug the design
- This debug method:
 - Allows to visualize the FPGA's internal signals;
 - Debugging in runtime that allows:
 - To validate system's behavior
 - To detect bugs that aren't spotted in simulation
 - To accelerate the debugging process

- Integrated Logic Analyzer (ILA):
 - Can be used to **monitor the internal signals of a design.**
 - Includes many advanced features of modern logic analyzers, including **Boolean trigger equations**, and **edge transition triggers.**
 - **All design clock constraints** that are applied to your design **are also applied** to the components inside the **ILA** core, since the ILA core is synchronous to the design being monitored,

- Vivado Logic Analyzer uses the FPGA's resources:
 - Block RAM: Trigger and data;
 - Triggers Compare Logic (*Slice Logic*)
- So, it is necessary to reserve some FPGA resources for the logic associated with this tool.

Vivado Debug Design



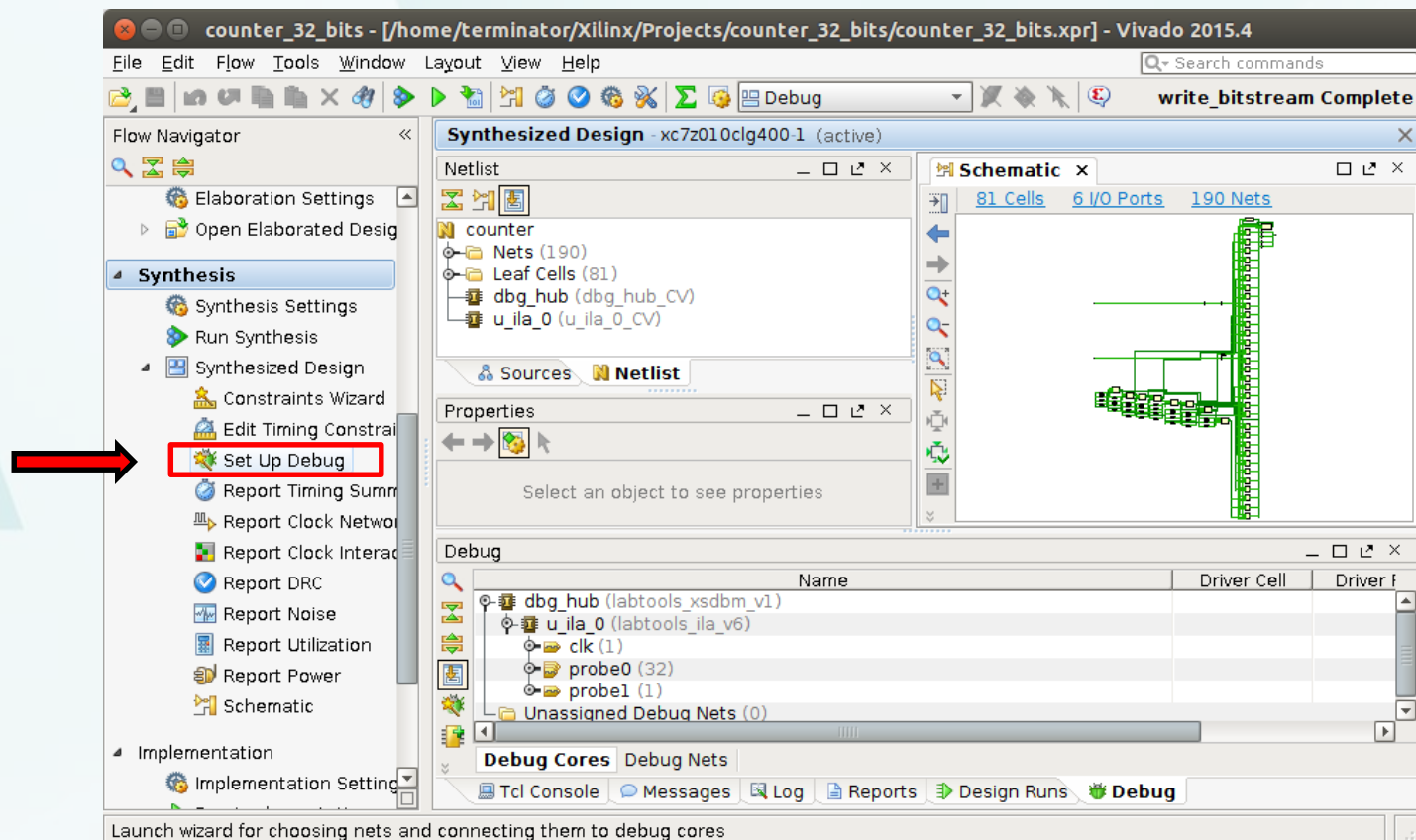
- **Create a Verilog RTL Project**

- **Ex 32-bits Counter:**

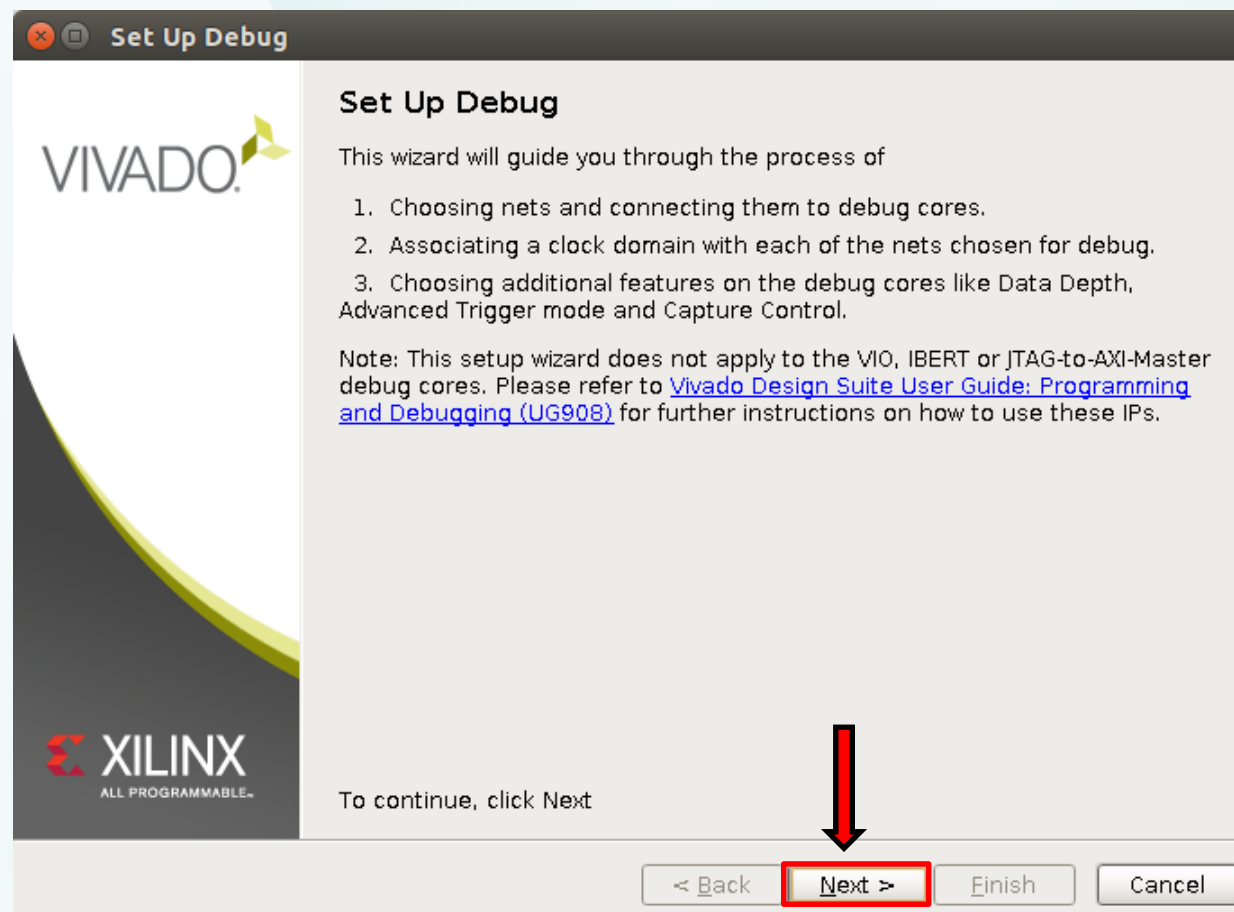
- module top (reset, clk, cnt);
 - input clk;
 - input reset;
 - output [3:0] cnt;
 - • (* mark_debug="true" *) reg [31:0] counter;
 - • always @(posedge clk) begin
 - if(reset)
 - counter <= 0;
 - else
 - counter = counter + 1;
 - end
 - • assign cnt = counter[31:28];
 - endmodule

- Debug Main Steps:
 - Map I/O pins [I/O Planning]:
 - CLK → L16 (Zybo's External Clock)
 - Reset → T16 (Switch 1)
 - Cnt [Place automatically]

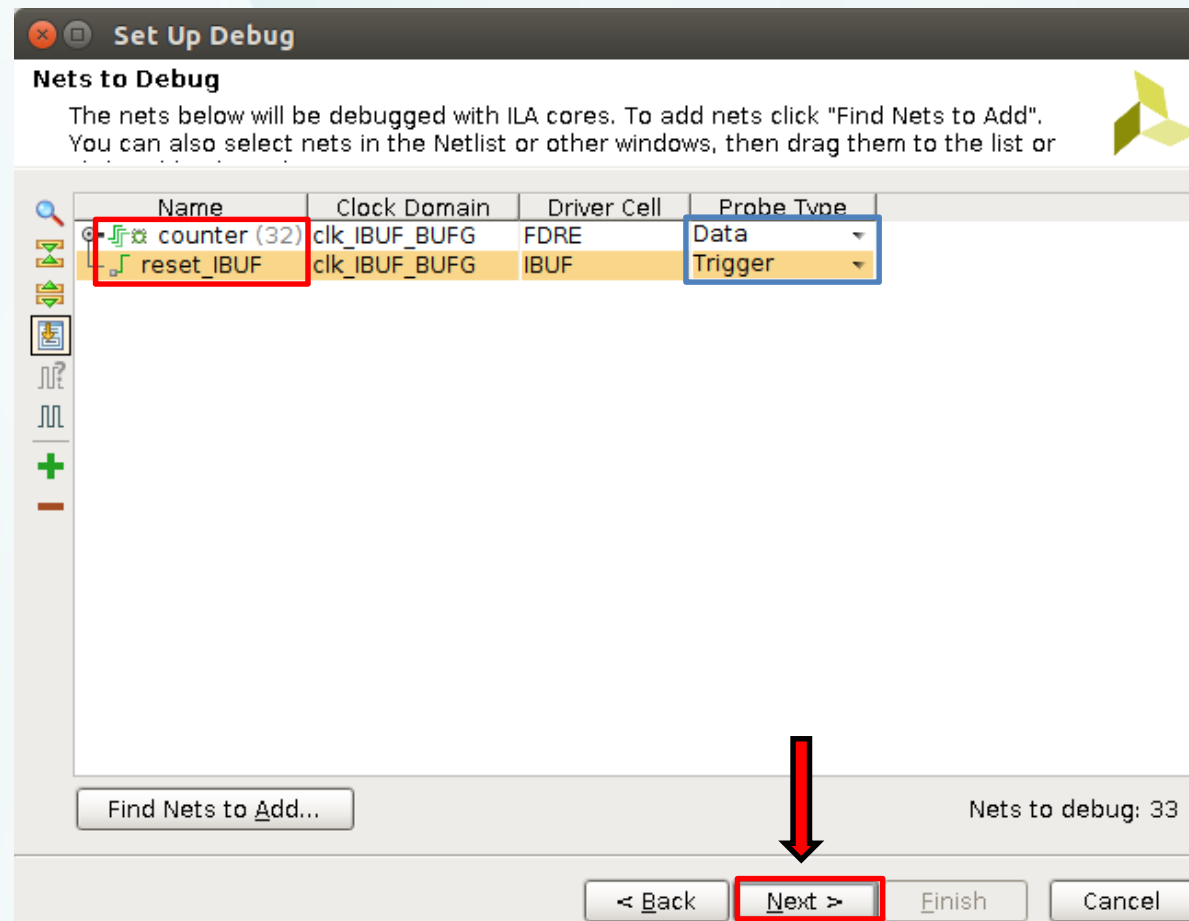
- Debug Main Steps:
 - Synthesize Design
 - Open Synthesized Design
 - Setup Debug



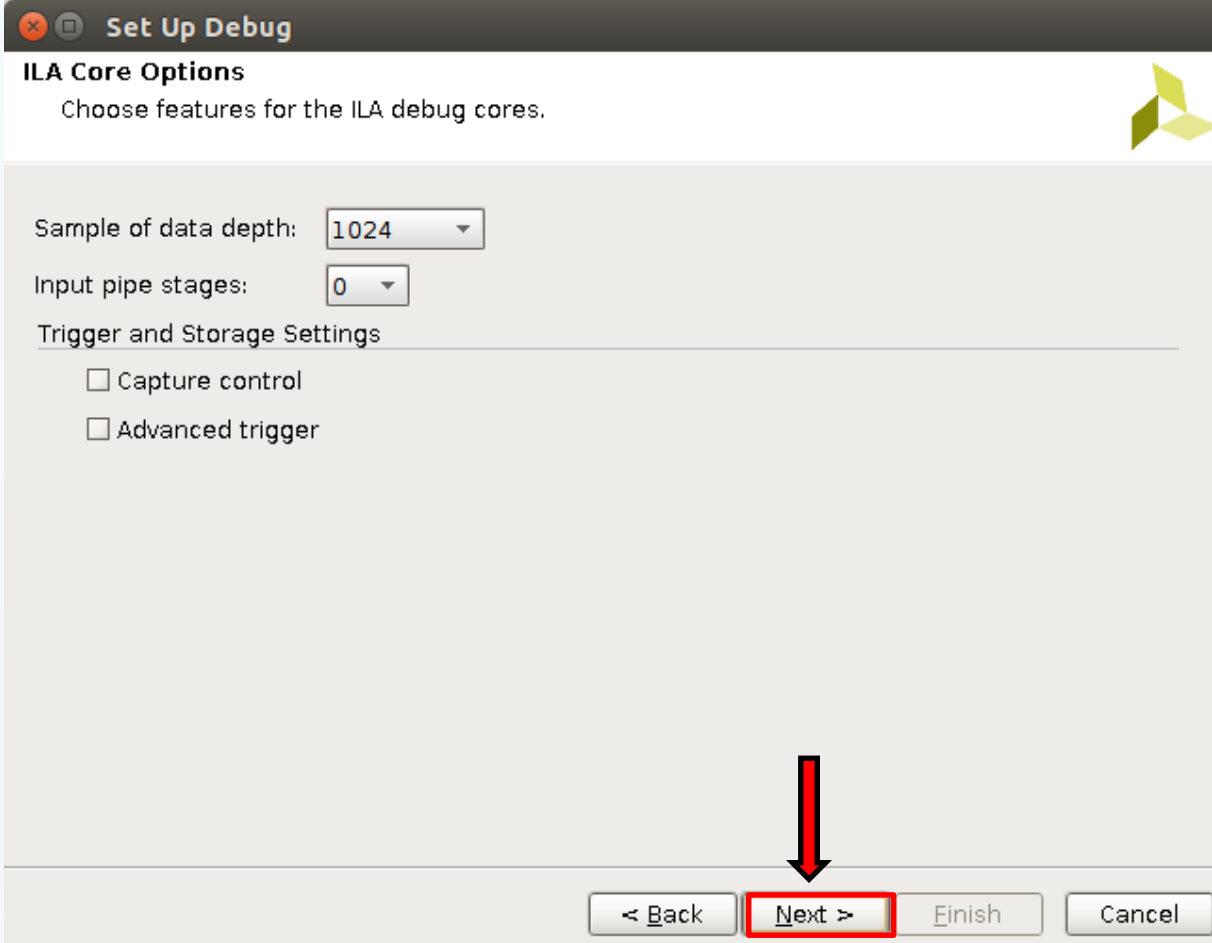
- Debug Main Steps:
 - Click Next



- Debug Main Steps:
 - Select Data and Trigger signals
 - Click Next



- Debug Main Steps:
 - Click Next



The image shows a 'Set Up Debug' dialog box with the title bar 'Set Up Debug'. The main section is titled 'ILA Core Options' with the instruction 'Choose features for the ILA debug cores.' and a yellow 3D cube icon. It contains two dropdown menus: 'Sample of data depth' set to '1024' and 'Input pipe stages' set to '0'. Below these is a section titled 'Trigger and Storage Settings' with two unchecked checkboxes: 'Capture control' and 'Advanced trigger'. At the bottom, there are four buttons: '< Back', 'Next >', 'Finish', and 'Cancel'. A red arrow points down to the 'Next >' button, which is also highlighted with a red rectangular border.

Set Up Debug

ILA Core Options
Choose features for the ILA debug cores.

Sample of data depth: 1024

Input pipe stages: 0

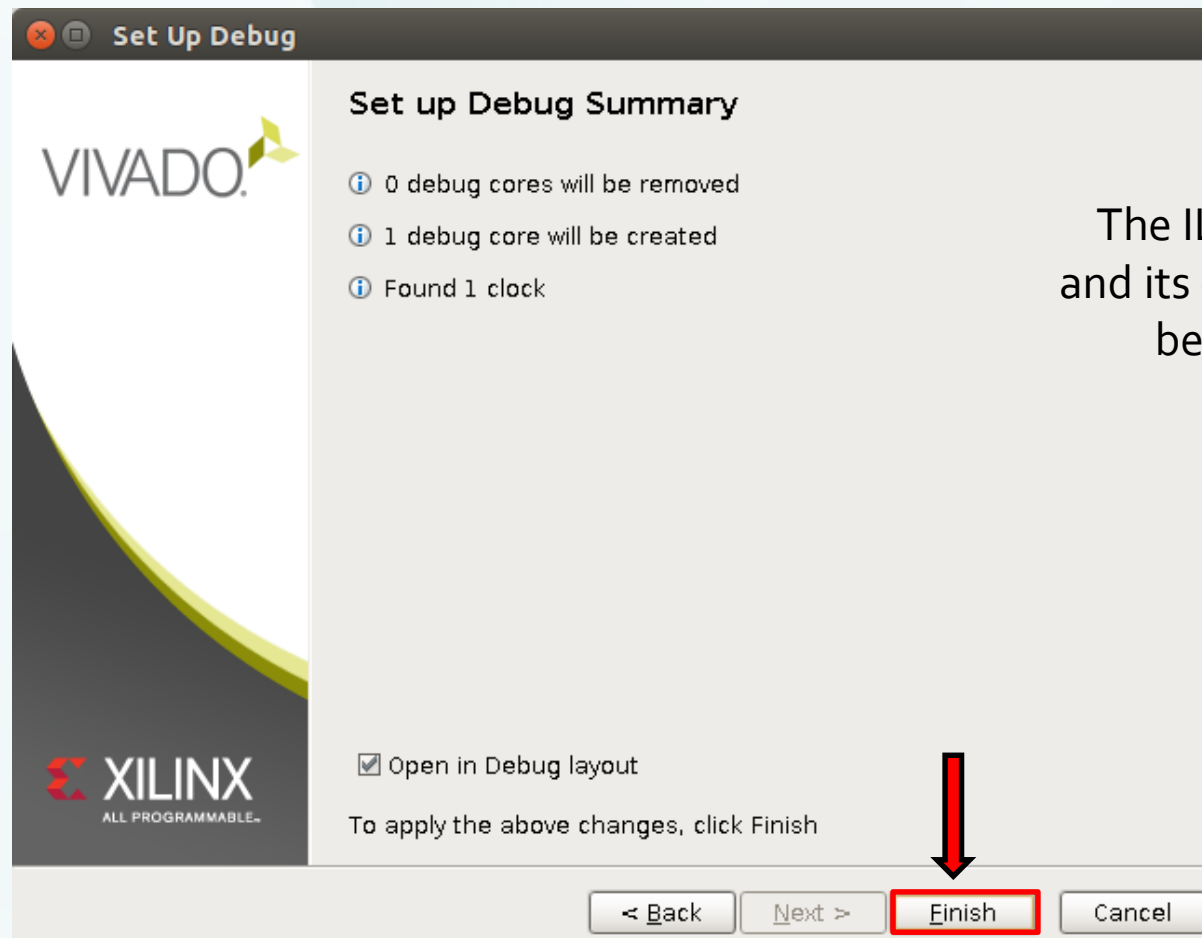
Trigger and Storage Settings

☐ Capture control

☐ Advanced trigger

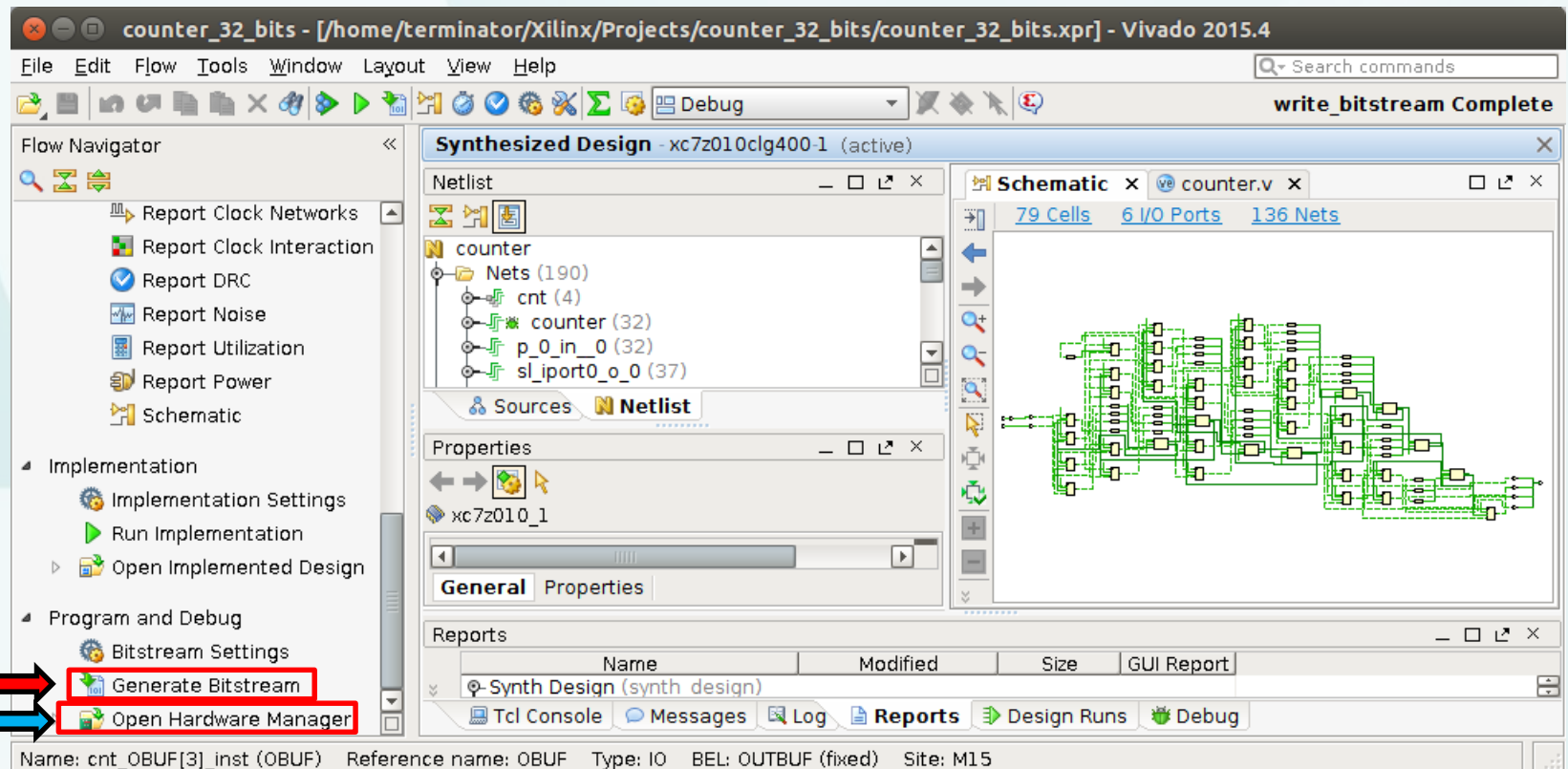
< Back **Next >** Finish Cancel

- Debug Main Steps:
 - Click Finish

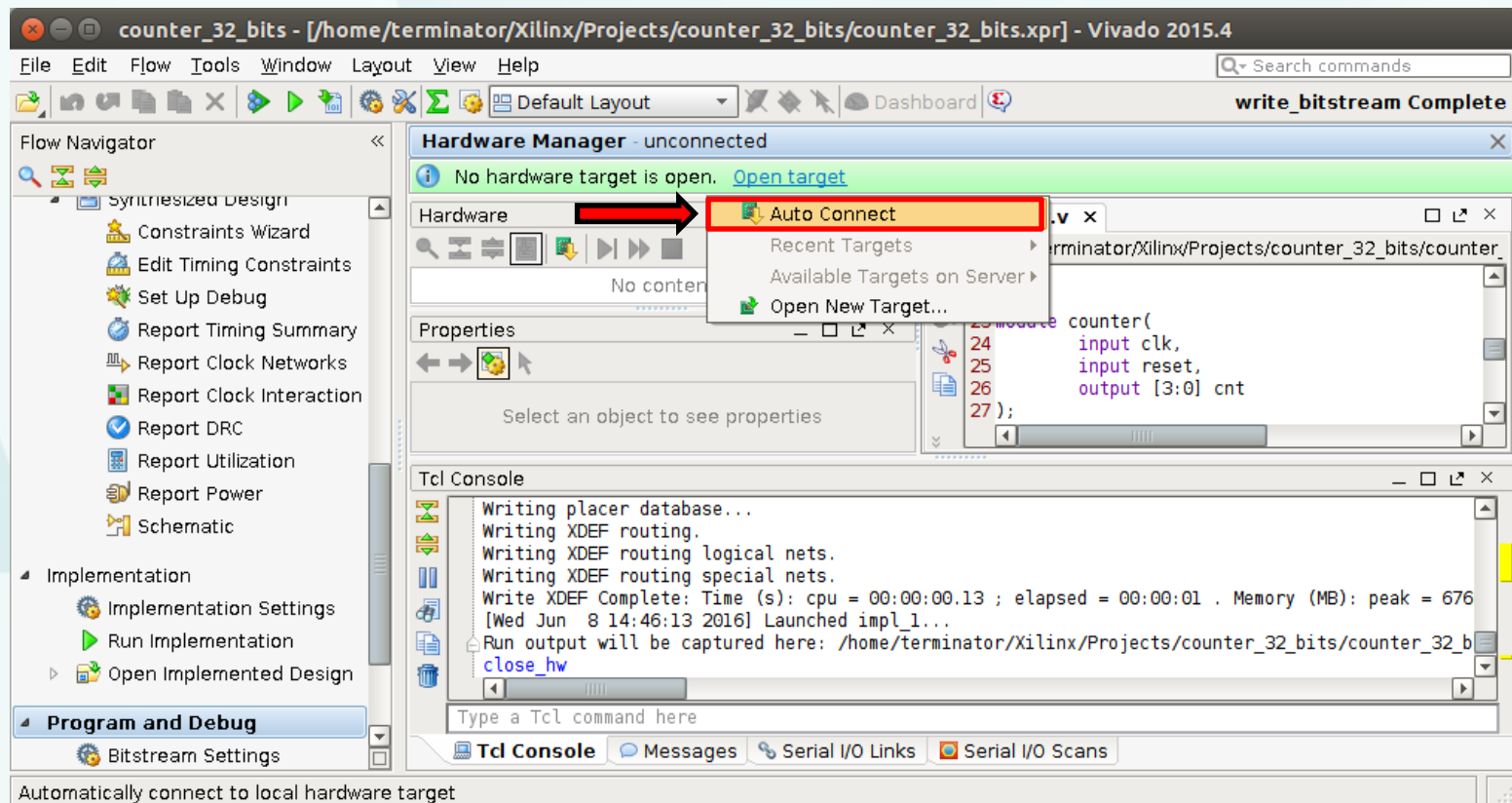


The ILA debug core
and its connections will
be connected

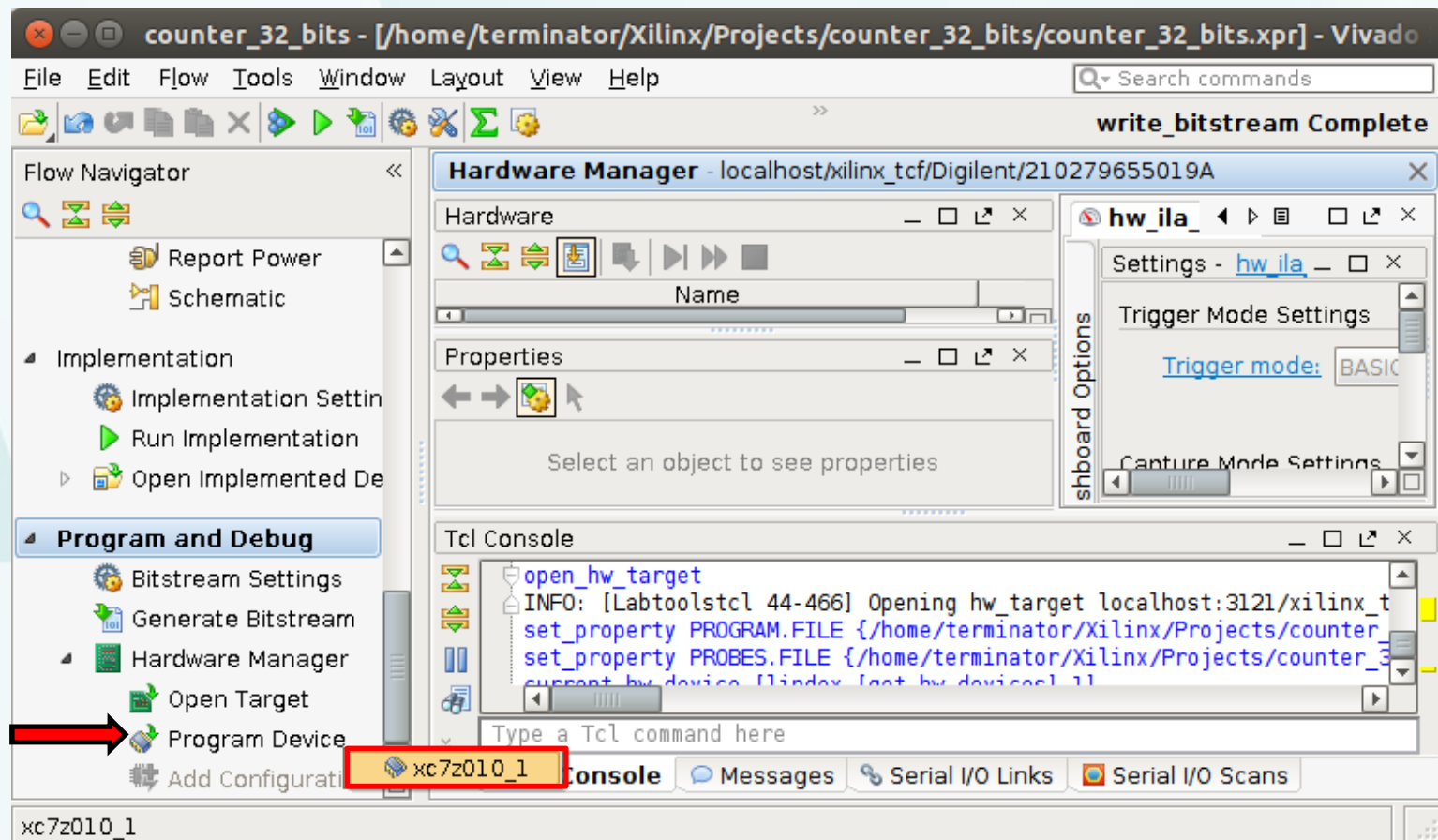
- Debug Main Steps:
 - Implement Design
 - **Generate Bitstream**
 - Open Hardware Target



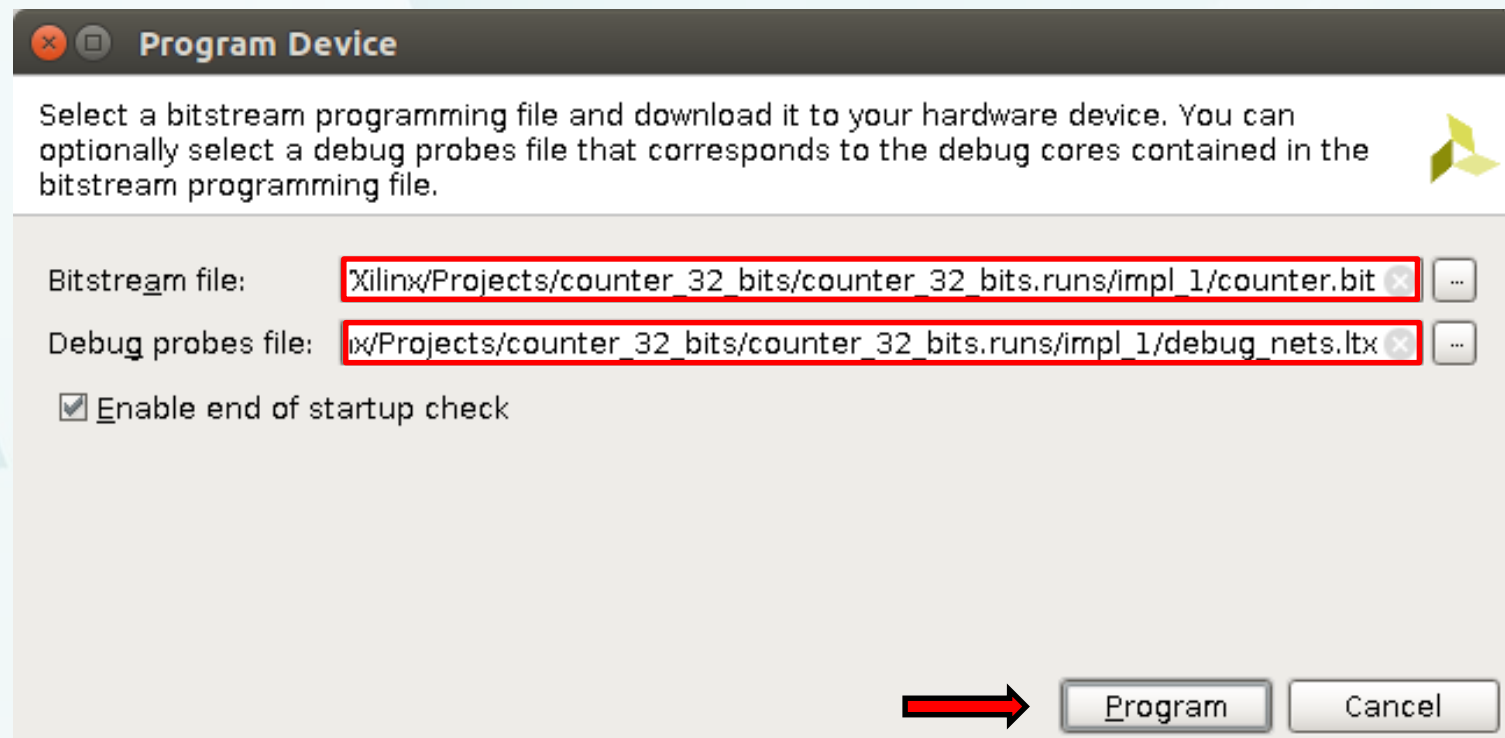
- Debug Main Steps:
 - Open Target → Auto Connect



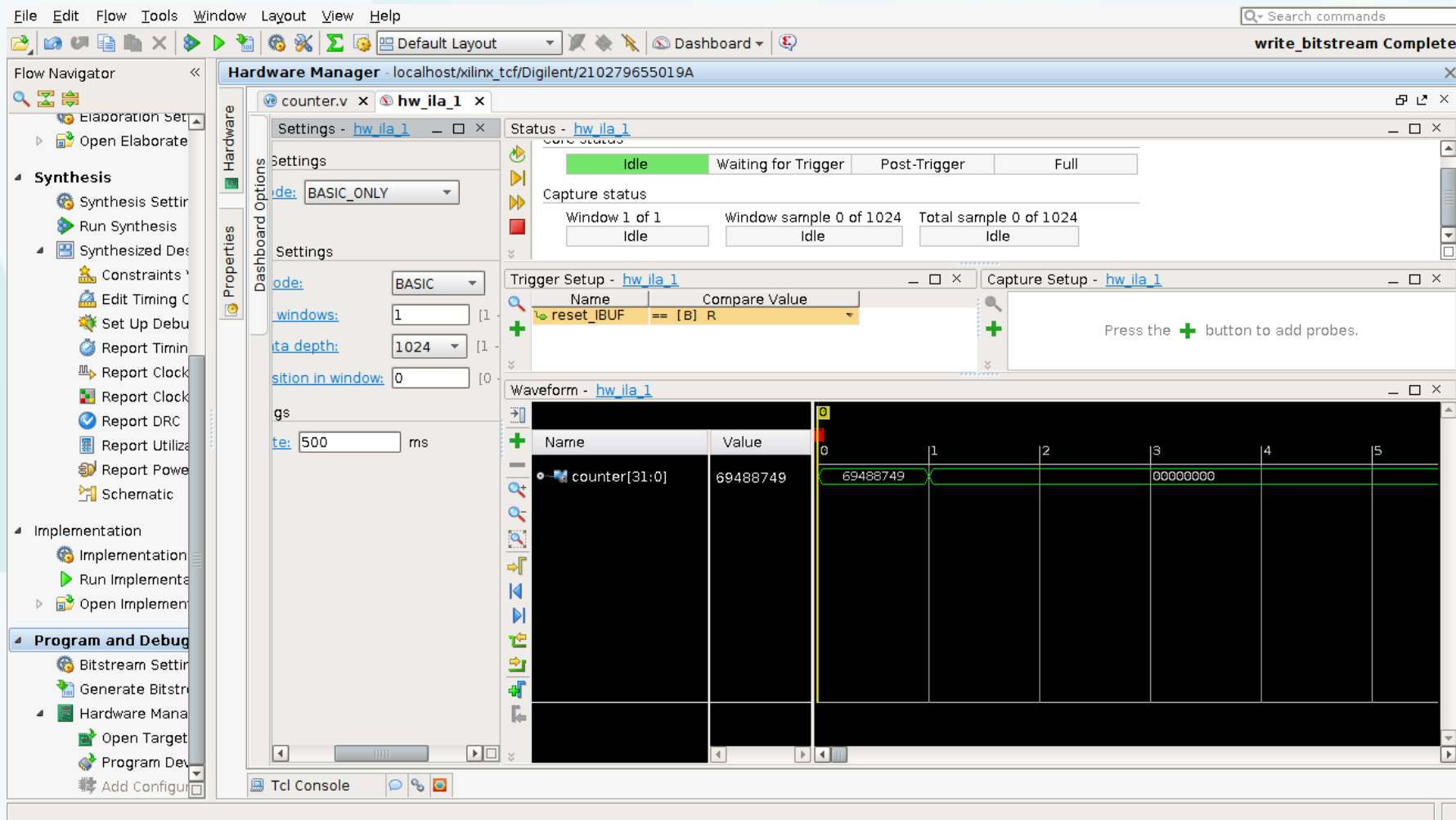
- Debug Main Steps:
 - Program FPGA Device



- Debug Main Steps:
 - Program FPGA Device
 - Select **Bitstream** and **Debug Probes**



- Vivado Logic Analyzer:



The screenshot displays the Vivado Logic Analyzer interface. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The Flow Navigator on the left shows the project hierarchy, with the 'Program and Debug' section selected. The Hardware Manager window shows the hardware configuration for 'hw_ila_1'. The Settings window for 'hw_ila_1' shows the 'BASIC' mode and various settings. The Status window shows the current status of the logic analyzer. The Trigger Setup window shows the trigger condition 'reset_IBUF == [B] R'. The Capture Setup window shows the capture setup. The Waveform window shows the captured data for 'counter[31:0]'.

File Edit Flow Tools Window Layout View Help

Search commands

write_bitstream Complete

Flow Navigator

- Elaboration Set
- Open Elaborate
- Synthesis
 - Synthesis Setting
 - Run Synthesis
 - Synthesized Design
 - Constraints
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing
 - Report Clock
 - Report Clock
 - Report DRC
 - Report Utilization
 - Report Power
 - Schematic
- Implementation
 - Implementation
 - Run Implementation
 - Open Implementation
- Program and Debug
 - Bitstream Setting
 - Generate Bitstream
 - Hardware Manager
 - Open Target
 - Program Device
 - Add Configuration

Hardware Manager - localhost/xilinx_tcf/Digilent/210279655019A

counter.v hw_ila_1

Settings - hw_ila_1

Settings

Mode: BASIC_ONLY

Settings

Mode: BASIC

Windows: 1

Bit depth: 1024

Position in window: 0

Time: 500 ms

Status - hw_ila_1

Core status

Idle Waiting for Trigger Post-Trigger Full

Capture status

Window 1 of 1 Window sample 0 of 1024 Total sample 0 of 1024

Idle Idle Idle

Trigger Setup - hw_ila_1

Name	Compare Value
reset_IBUF	== [B] R

Capture Setup - hw_ila_1

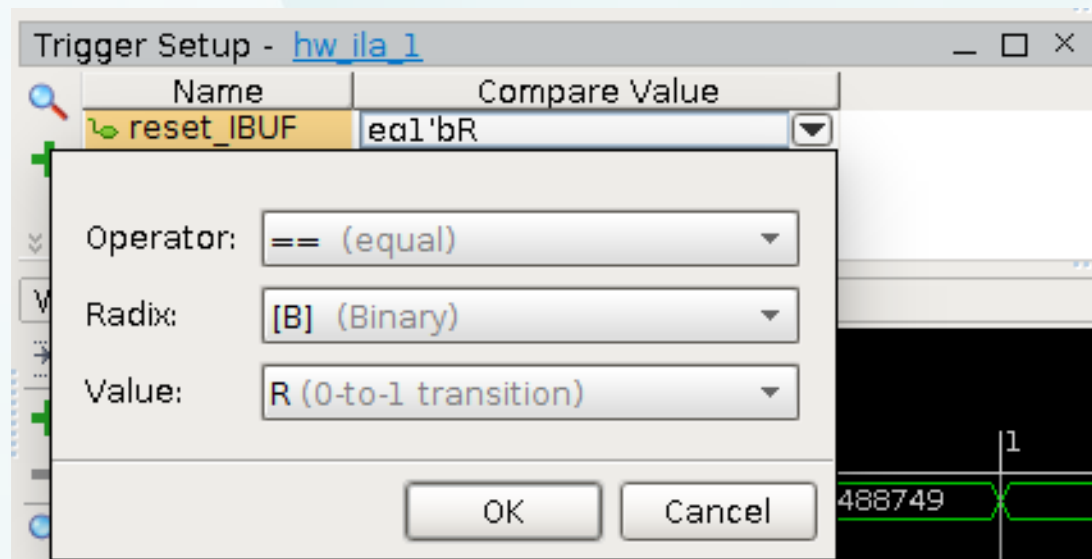
Press the + button to add probes.

Waveform - hw_ila_1

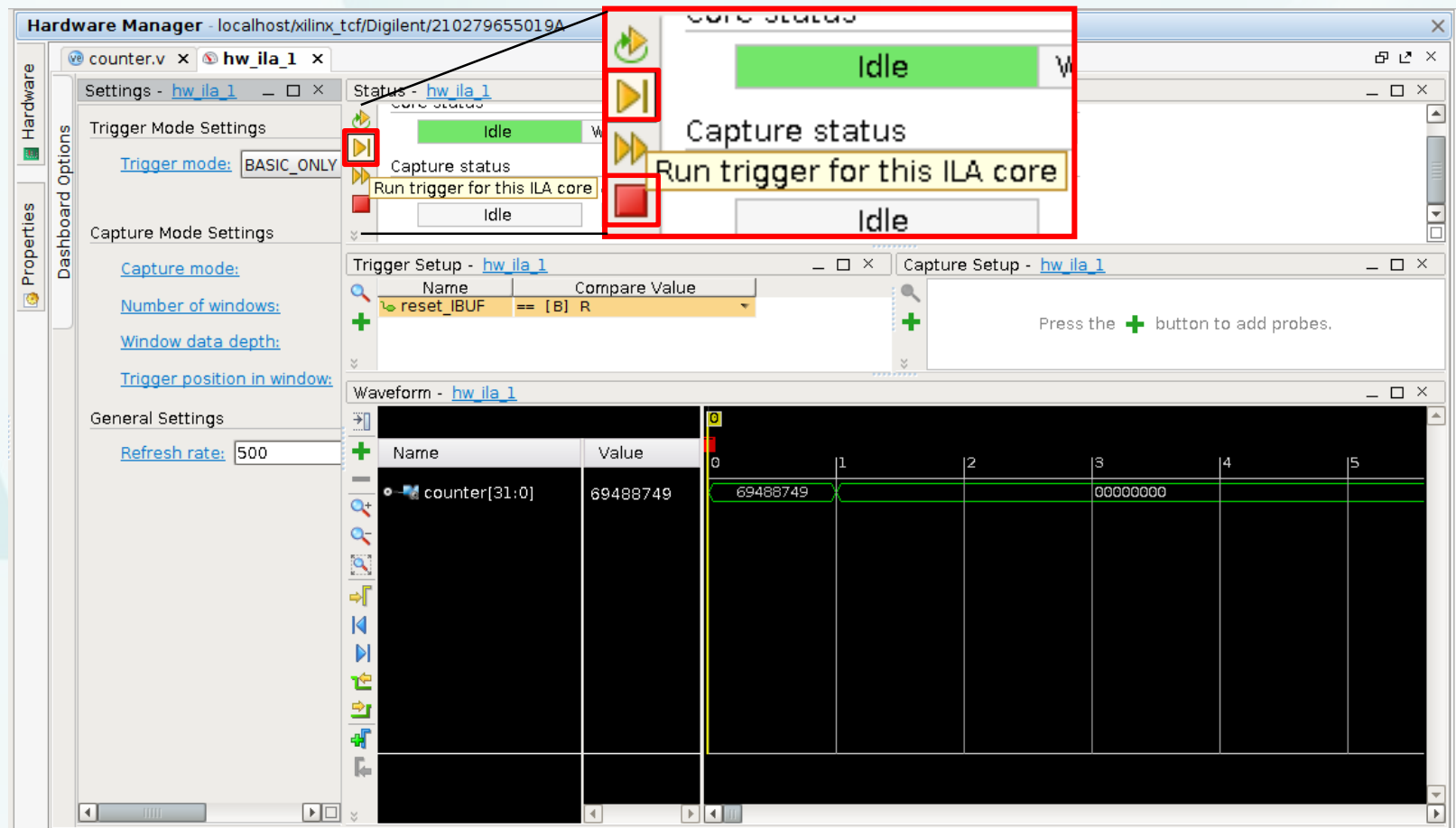
Name	Value
counter[31:0]	69488749

Tcl Console

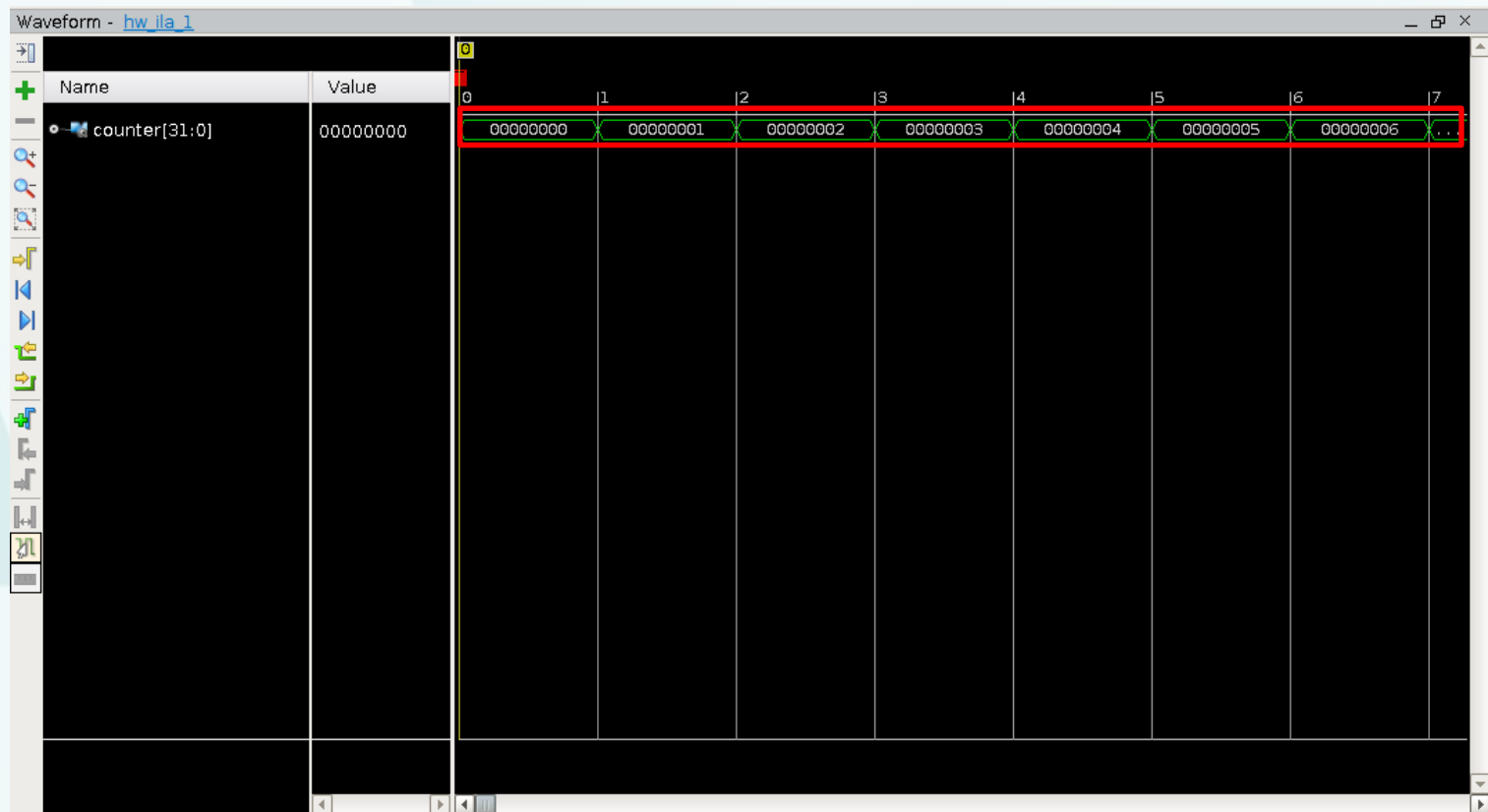
- Vivado Logic Analyzer:
 - Setup Trigger
 - Select **Trigger Name** and **Compare Value**



- Vivado Logic Analyzer:
 - Start/Stop Capturing Samples



- Vivado Logic Analyzer:
 - **Visualize Capture Data** after triggering the signal



Questions?