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TSN Switch User Manual

(version 1.0)

OpenTSN

OpenTSN Open Source Project Team

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Version history

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1 Overview

This document is a user manual for Time Sensitive Networking (TSN) hardware.

The operation steps of TSN switch board and project compilation are described.

The TSN switch includes 4 Gigabit Ethernet interfaces, supports IEEE 802.1AS,

802.1Qch, 802.1Qbv, 802.1Qcc standards.

2. Description of the board

As shown in Figure 21 below, it is a TSN network card, and its external interface has corresponding

Notes and tables have instructions.

Figure 2-1 Board Diagram

The detailed description of the interfaces marked 0-3 in the above figure is shown in Table 2-1.

Table 2-1 TSE overall architecture top-level signal definition

Numbering	Interface description
0	No. 0 Gigabit Ethernet interface
1	Gigabit Ethernet port 1

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2	Gigabit Ethernet port 2
3	Gigabit Ethernet port 3

3. Build hardware engineering

3.1, code download

The TSN switch hardware code download URL is https://github.com/fast codesign/OpenTSN3.0-centrilized\Hardware\code\TSNSWITCH3.0

3.2. IP Core Customization

Users need to generate the IP cores (including

PLL, RAM, FIFO, etc.), and put the generated IP core folder and its qsys file in

Set in OpenTSN3.0-centrilized\Hardware\project_demo\TSNSWITCH3.0

Under the _FPGA_4port\ipcore directory, please refer to the parameter settings of each IP core for details.

OpenTSN3.0centrilized\Hardware\project_demo\TSNSWITCH3.0_FPG

A_4port\ipcore/readme.txtÿ

3.3, project compilation

User in OpenTSN3.0-centrilized\Hardware\project_demo\TSNSWIT

Execute make in the CH3.0_FPGA_4port\script file/Makefile directory, and then the project starts.

Start synthesis, place and route, generate sof files, static timing analysis, etc.; appear on the interface

When compile finish, it indicates that the project has been compiled. In OpenTSN3.0-

centrilized\Hardware\project_demo\TSNSWITCH3.0_FPGA_4port/outp

The sof file is generated in the ut_files directory.

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4. Logic download to **FPGA**

The specific operation steps for downloading TSN network card logic to FPGA are as follows:

1) Use the download cable to connect the computer for compiling the project to the hardware development board shown in Figure 2-1.

2) Open Inter Quartus, click tools->programmer->addfiles, add

Add the compiled TSN_FPGA_4port.sof file/TSN_FPGA_4port.jic (if

Firmware is required, sof file needs to be converted into jic file first). As shown in Figure 4-1 below

Show.

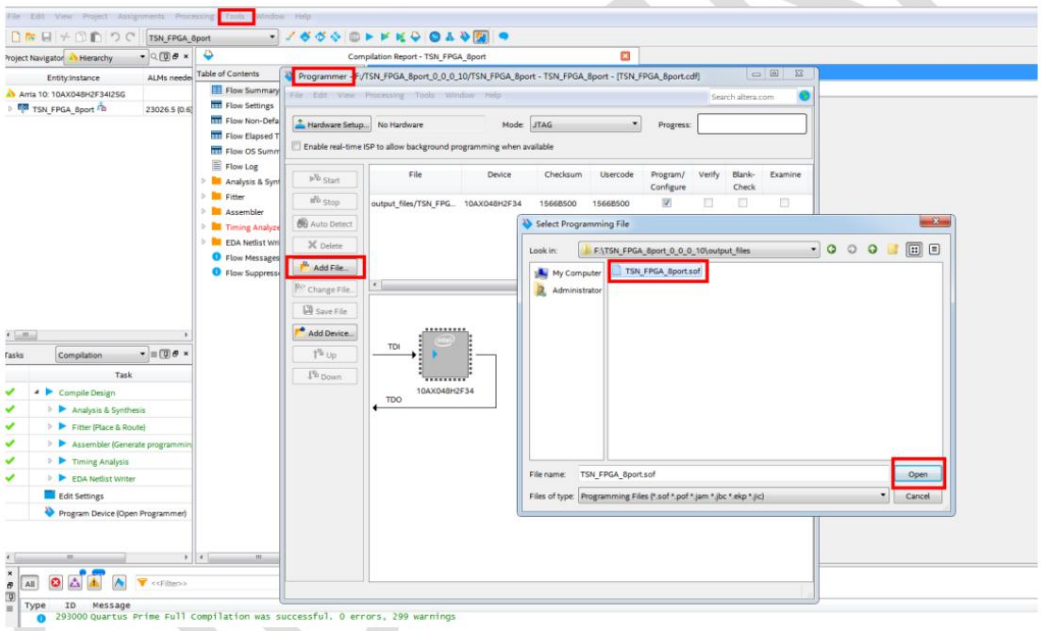

Figure 4-1 Add .sof/jic file

3) Select the USB serial port of the download cable, and select JTAG mode to download, click start

Start downloading the TSN logic to the FPGA. As shown in Figure 4-2 below.

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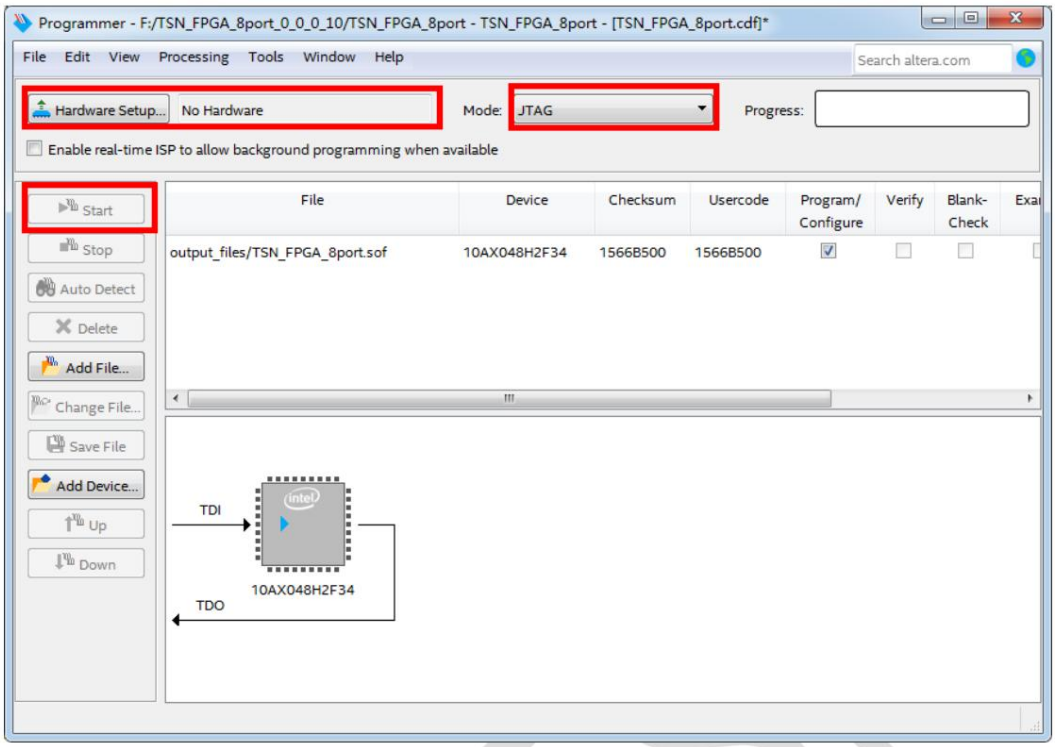

Figure 4-2 Download TSN hardware logic

5. Engineering board debugging

The general operation steps of upper board debugging are as follows:

1) Click tools->signaltaplogicAnalyzer, in the trigger signal column, select

Set the trigger parameters for the signal to be debugged. As shown in Figure 5-3 below.

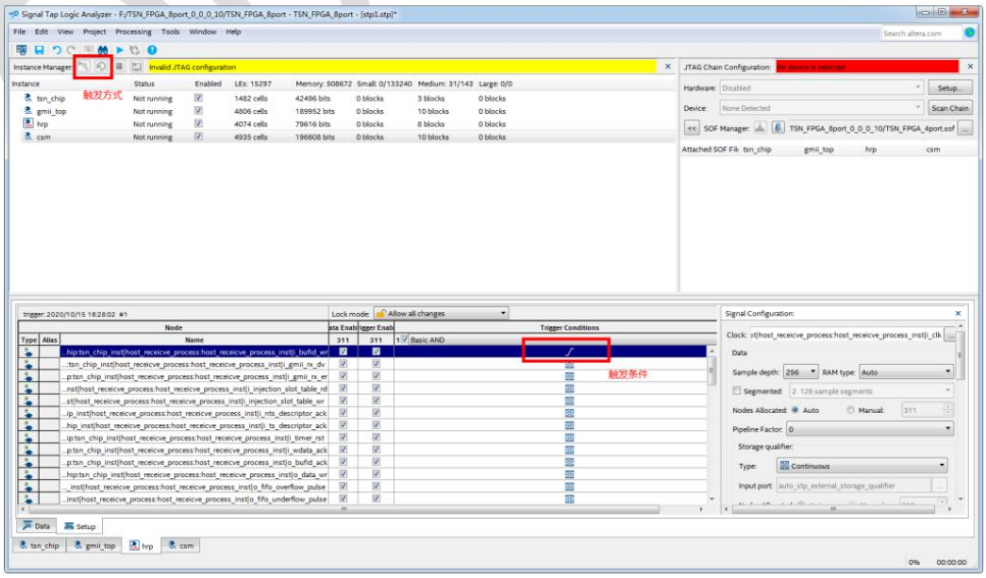

Figure 5-3 Setting trigger parameters

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1) Select single-step trigger or continuous trigger to see the specific data of the debug signal. Such as

As shown in Figure 5-4 below.

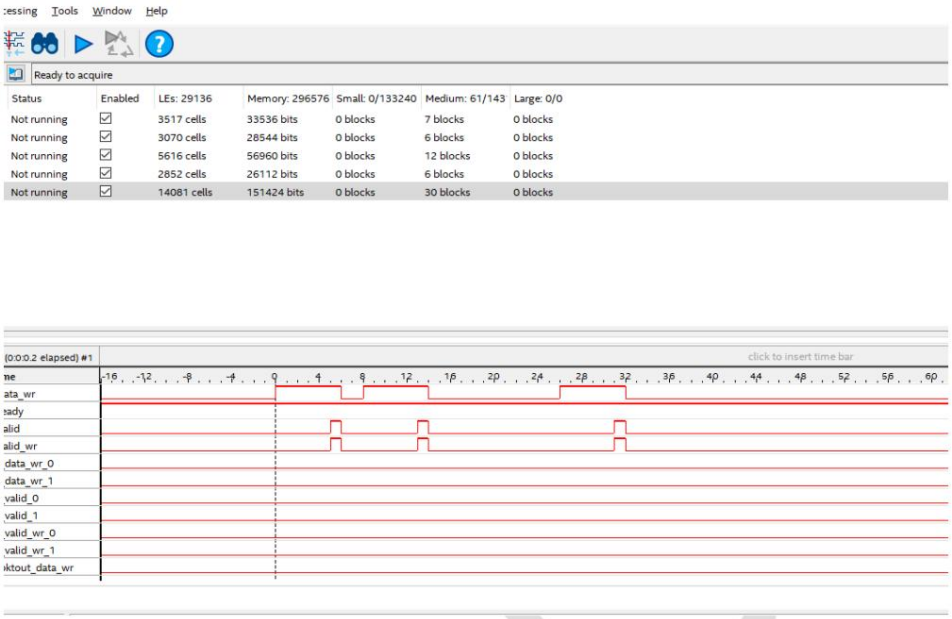

Figure 5-4 The specific data of the debug signal