TSN Network Card User Manual

(version 1.0)

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Version history

Version revision time		modify the content	file identification
1.0	2021.4	first edition	OpenTSN3.0

content

1 Overview

This document is a user manual for Time Sensitive Networking (TSN) hardware.

The operation steps of TSN network card board and project compilation are described.

The TSN network card contains 4 Gigabit Ethernet interfaces, which can be time-sensitive grouping of end systems precise control of injection and commit times.

2. Description of the board

As shown in Figure 21 below, it is a TSN network card, and its external interface has corresponding Notes and tables have instructions.

Figure 2-1 Board Diagram

The detailed description of the interfaces marked 0-3 in the above figure is shown in Table 2-1.

Table 2-1 TSE overall architecture top-level signal definition

Numbering	Interface Description
0	No. 0 Gigabit Ethernet interface, not used yet
1	No. 1 Gigabit Ethernet interface, connected to the switch

2	No. 2 Gigabit Ethernet interface, not used yet
3	No. 3 Gigabit Ethernet interface to connect with the host

3. Build hardware engineering

3.1, code download

The TSN network card hardware code download URL is OpenTSN3.0-centrilized \Hardware\code\TSNNIC3.0ÿ

3.2. IP Core Customization

Users need to generate the IP cores (including PLL, RAM, FIFO, etc.), and put the generated IP core folder and its qsys file in Set in OpenTSN3.0-centrilized\Hardware\project_demo\TSNNIC3.0_FPG In the A_2port\ipcore directory, see OpenTSN3.0-centrilized\Hardware\project_demo\TSNNIC3.0_FPGA_2port\ipcore/rea dme.txtÿ

3.3, project compilation

User in OpenTSN3.0-centrilized\Hardware\project_demo\TSNN Execute make in the IC3.0_FPGA_2port\script file\Makefile directory, and then the project starts Start synthesis, place and route, generate sof files, static timing analysis, etc.; appear on the interface When compile finish, it indicates that the project has been compiled. In OpenTSN3.0-centrilized\Hardware\project_demo\TSNNIC3.0_FPGA_2port/output_fil

The sof file is generated in the es directory.

4. Logic download to **FPGA**

The specific operation steps for downloading TSN network card logic to FPGA are as follows:

1) Use the download cable to connect the computer for compiling the project to the hardware development board shown in Figure 2-1.

2) Open Inter Quartus, click tools->programmer->addfiles, add

Add the compiled TSN_FPGA_4port.sof file/TSN_FPGA_4port.jic (if

Firmware is required, sof file needs to be converted into jic file first). As shown in Figure 4-1 below

Show.

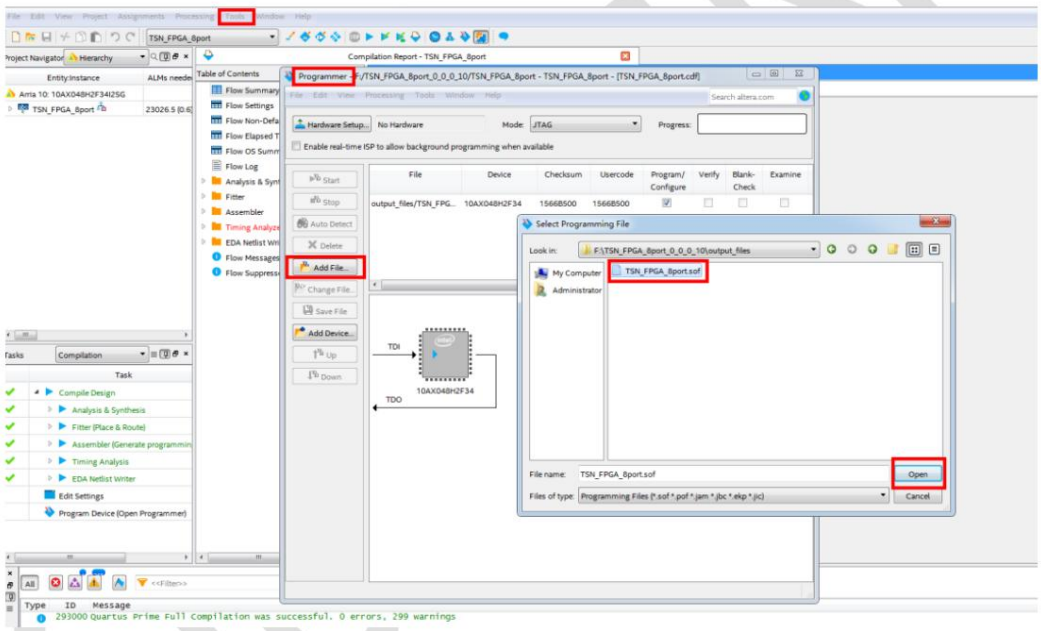

Figure 4-1 Add .sof/jic file

3) Select the USB serial port of the download cable, and select JTAG mode to download, click start

Start downloading the TSN logic to the FPGA. As shown in Figure 4-2 below.

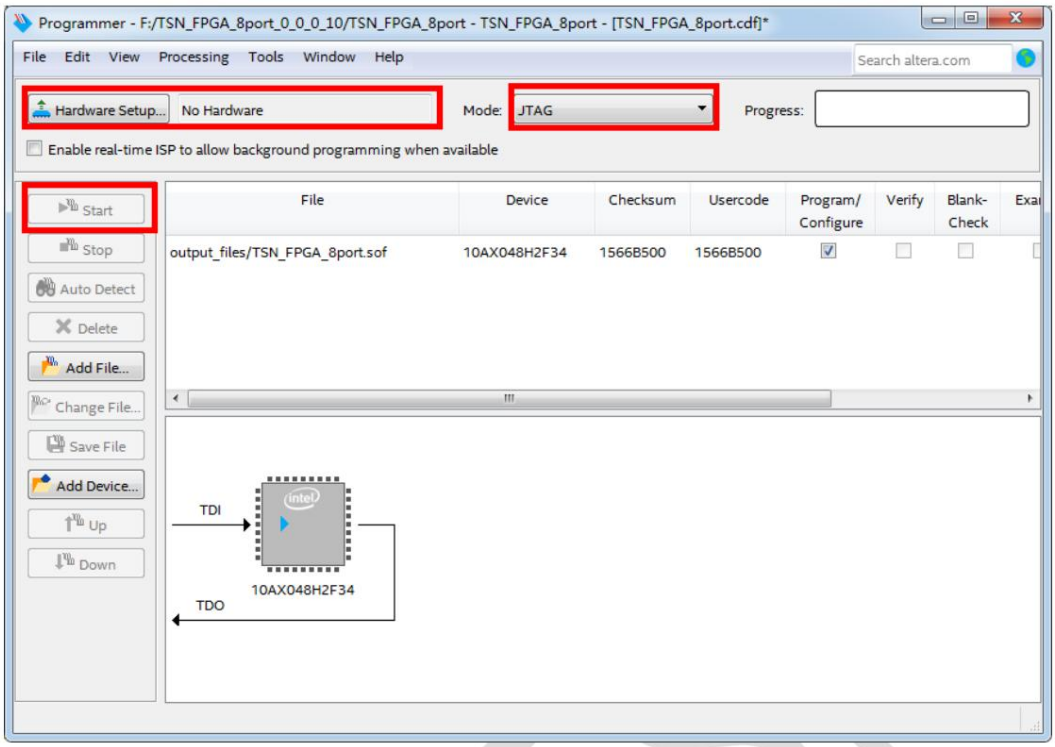

Figure 4-2 Download TSN hardware logic

5. Engineering board debugging

The general operation steps of upper board debugging are as follows:

1) Click tools->signaltaplogicAnalyzer, in the trigger signal column, select

Set the trigger parameters for the signal to be debugged. As shown in Figure 5-3 below.

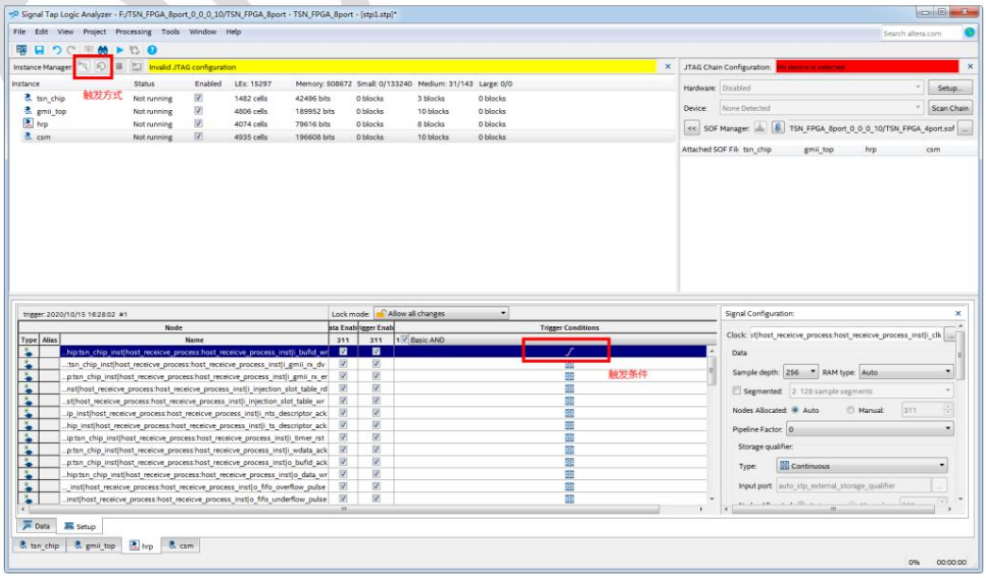

Figure 5-3 Setting trigger parameters

1) Select single-step trigger or continuous trigger to see the specific data of the debug signal. Such as

As shown in Figure 5-4 below.

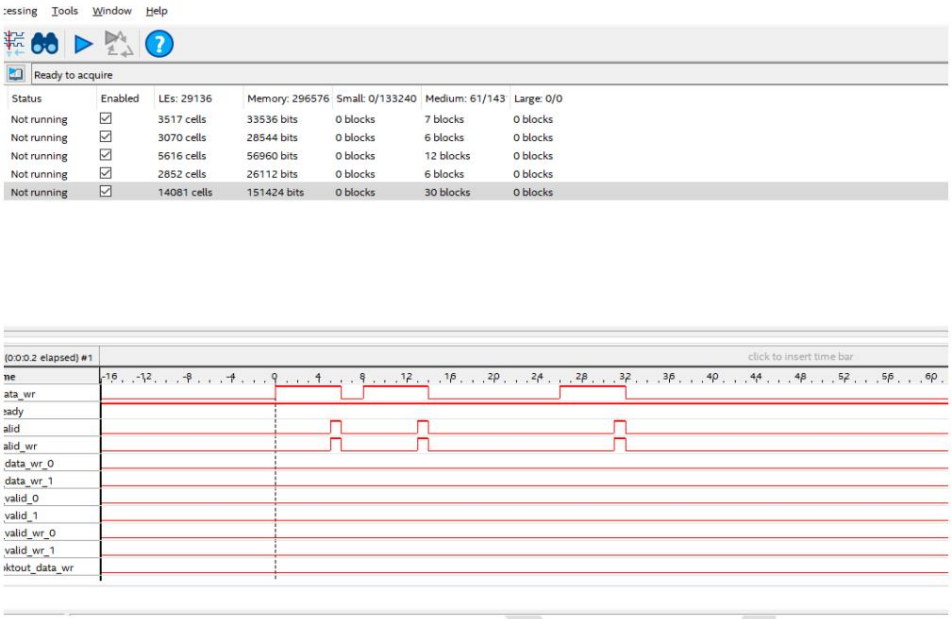

Figure 5-4 The specific data of the debug signal