European XFEL Cavity BPM Data Sheet

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1 Introduction

For the E-XFEL a cavity BPM was designed consisting of the 3.3 GHz cavity pickup, RFFE board, ADC16HL sampling board, the GPAC carrier board and additional boards (transition cards, EVR) supporting the application. The aim is to measure sub um resolution of the beam position.
The system will measure I/Q amplitudes of reference, x and y channel of the Cavity RFFE and calculate the position with low latency in a Virtex-5 FXT FPGA. Low latency is important for feedback systems relying on beam position information.

1.1 Purpose

The aim of this document is to provide a global overview of the measurement technique with the GPAC and to describe the user interface to the BPM FPGAs on the GPAC.

1.2 Scope

This document provides a global overview of the cavity BPM interface and specifies the user interface. This document is a starting point which links to the detail information in the implementation in hardware, firmware and/or software.

1.3 Definitions, acronyms, and abbreviations

This document is based on the “IEEE Recommended Practice for Software Requirements Specifications” [1].

ADC	Analog Digital Converter.
BPM	Beam Position Monitor
CORDIC	COordinate Rotation DIgital Computer), Aka Volder's algorithm is an algorithm used to translate Cartesian (x, y) to polar (amplitude, phase) coordinate systems.
EVR	EVent Receiver. Decoder of the Event Link at PSI. This is a standard PSI VME card used to decode event link messages for trigger generation.
FPGA	Field Programmable Gate Array. Programmable logic device.
GOF	Glas Optical Fiber.
I2C	see IIC
IIC	IIC or I²C (Inter Integrated Circuit bus) is a multi-master serial bus defined / specified by Philips.
PPC	PowerPC (Performance optimization with enhanced risc Performance Computing) is a RISC architecture created by an alliance of big companies Apple/IBM/Motorola.
Reg	Register. Mathematically z^-1
RTM	Rear transition card. Sometimes called “Transition Card”
SFP	Small form-Factor Pluggable is a compact, hot-pluggable multi-gigabit optical or/and electrical transceiver interface.

1.4 References

[1] IEEE Std 830-1998, Recommended Practice for Software Requirements Specifications.

[2] PSI 2012, RFFE schematic 3G3_Cavity_RFFE_V2R2prj.pdf
..\02_Design\RFFE\04_Datasheet\01_Reference\EXFEL_Cavity_RFFE_120700B_r4.pdf

[3] PSI 2012, Cavity BPM ADC Data Processing Ideas,
Cavity_BPM_ADC_Data_Processing_Ideas_v1r4.pdf
01_Reference\Cavity_BPM_ADC_Data_Processing_Ideas_v1r4.pdf

[4] PSI 2012, ADC16HL Firmware Interface Data Sheet
..\02_Design\ADC16HL\04_Data_Sheet\ADC16HL_data_sheet.pdf

[5] PSI 2012, European XFEL Cavity BPM bpm_cav_exfel Data Sheet
..\02_Design\BPM_FPGA\06_EDK\pcores\bpm_cav_exfel_v1_00_a\doc\bpm_cav_exfel.pdf

[6] PSI 2013, European XFEL Cavity BPM Software Data Sheet
..\02_Design\BPM_FPGA\06_EDK\sw\doc\bpm_cav_exfel_sw.pdf

1.5 Overview

Chapter 2 provides an overview and how the firmware is related to other firmware used. Chapter 3 contains all the detail information on the user interfaces.

2 Overall description

One possible system in which the BPM measurement will be integrated / used might look like this:

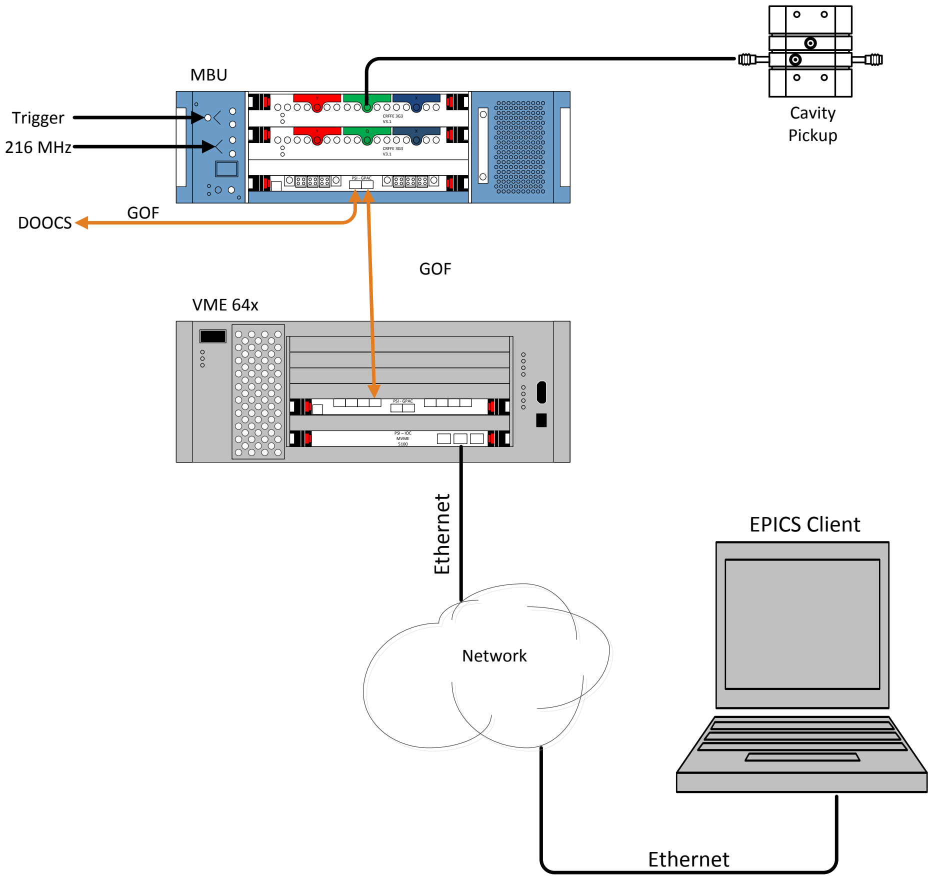


Figure 1: BPM Integration Overview

The pickup is connected by HF cables to the MBU. The MBU is a box which contains all necessary infrastructure like power, cooling, trigger handling, RF parts, digitizers, calculations, feedbacks and generic control system interface for the BPM application.

Figure 2 illustrates the main devices used for the BPM system. On the far left the pickups are drawn, which are connected to the RFFE [2]. Within the RFFEs the 3.3 GHz signals from the pickups are mixed with a machine RF (216.6667 MHz) derived frequency in order to get a pulse long enough to be measured with the six, 16 bit, 160 MSa/s ADCs on the ADC16HL piggyback board [4]. The ADC data is processed [5] on the GPAC and is finally provided to the control system.

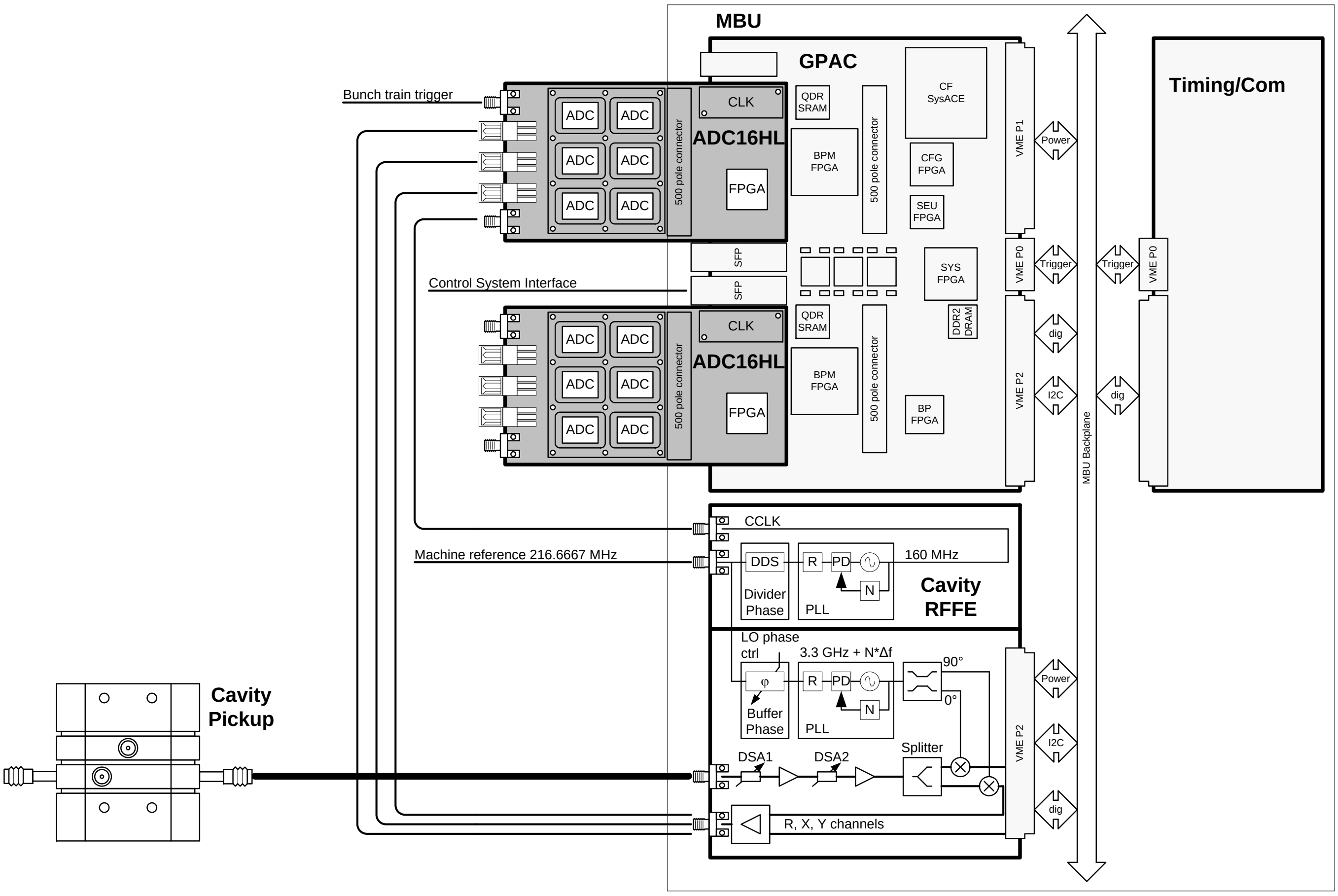


Figure 2: Cavity BPM Device Overview

The control system configures the BPM system by means of providing signals and information concerning the timing of the beam (a very stable machine RF and event system containing bunch train trigger, bunch number, etc.), the charge and filling pattern expected. This information has to be sent to the BPM system in advance, e.g. before the bunch train is fired.
The following figure is intended to clarify the functions of the interconnected devices that form a chain of signal processing modules. This modifies the 3.3 GHz signal starting at the cavity pickup and ending at the calculation of position and charge made available to the control system. This figure is as well important because it structures the following chapters following the signal path from the pickups on the left to the position and charge calculation on the right.

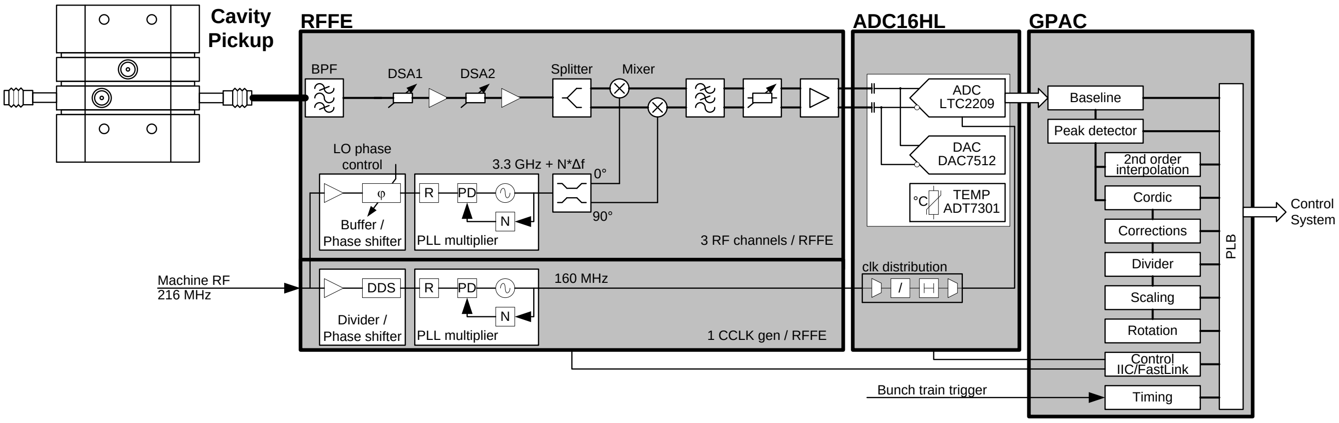


Figure 3: Cavity BPM Data Flow Overview

Please note: The figure above does not describe the control system part, because the information is presented on the IBM® PLB interface to the user. There are many possibilities for the user/developer to access the data on the PLB interface, please remember the PLB is a multi master, multi bit-width, burst and single transfer capable bus. One way to access the data on the GPAC by means of PLB (the intended use for the E-XFEL) is an optical fiber SFP connection, bridging the PLB transparently (e.g. allowing access to the addresses directly). Another way, which we use for tests at the SwissFEL Testinjector and the FLASH 2012 control system, is the VME interface. However there are many other interfaces possible like those provided/supported by XILINX® such as UART (RS232) and PCIe to name a few. Common to all interfaces is the concept of a bus being addressed and read (or written), hence knowing one of these access methods will give you a basic understanding for porting to another interface. And finally please note the PLB is a multi-master bus concept allowing several of the mentioned interface techniques simultaneously (e.g. the VME, the optical fiber SFP connection, local PPC on the FPGA and PCIe access can coexist on the GPAC).

3 RFFE Interface overview

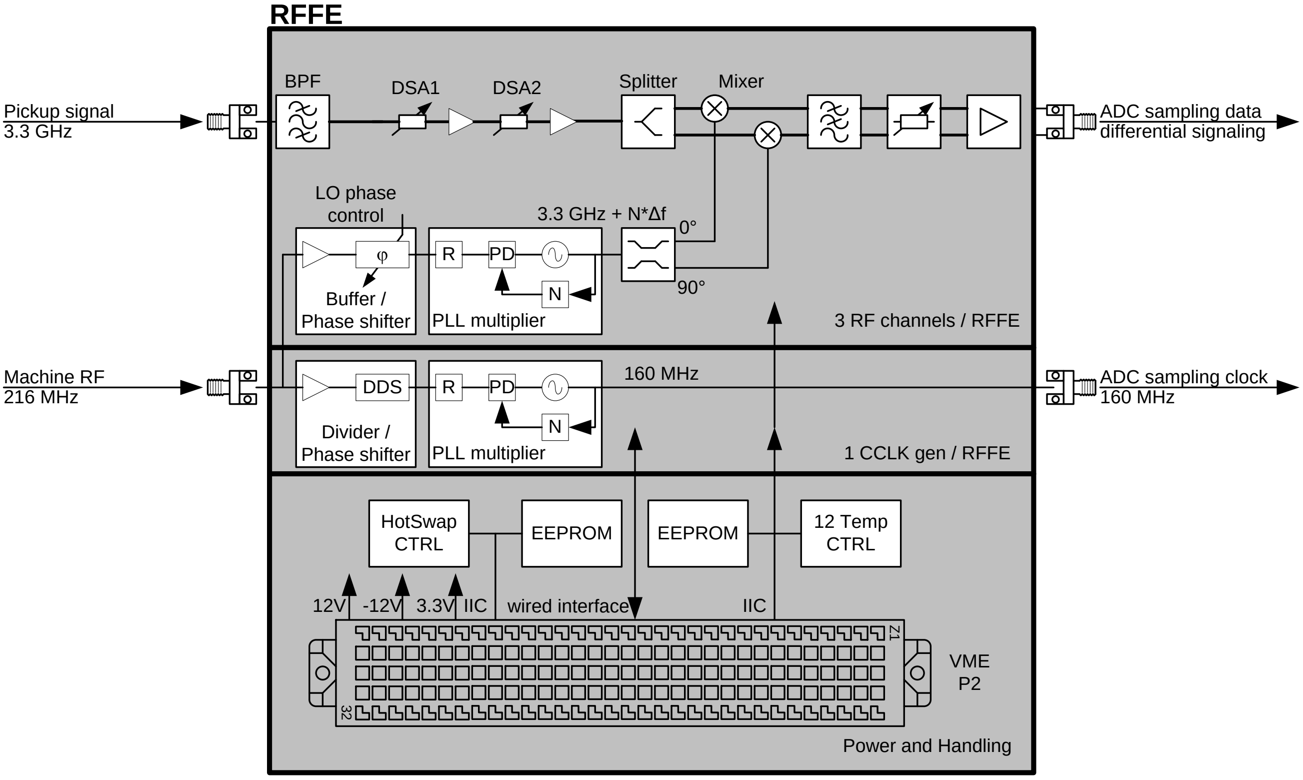


Figure 4: Overview of Blocks in the Cavity RFFE

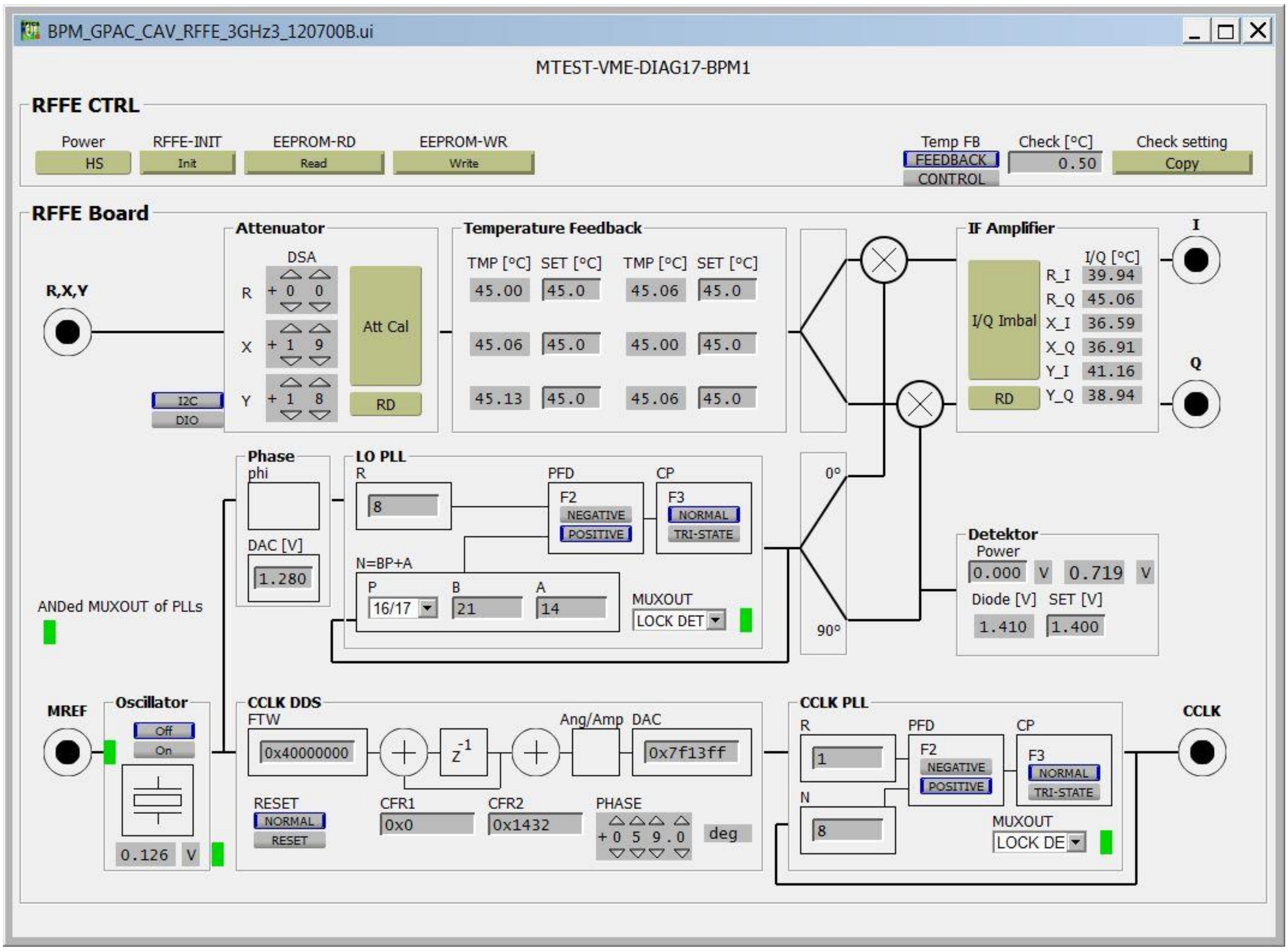
The RFFE [2] is a VME form factor board used for high frequency electronics at the cavity pickup. This board has a large variety of functions some of them are passive elements such as filters, splitters and amplifiers and additionally highly configurable components such as DACs (for phase shifting), PLLs, DDS, EEPROMs, switched attenuators (accounting for the beam charge), temperature sensors and feedback systems. The controllable chips are connected to one of the two IIC interfaces allowing the user to customize/adjust the board behavior. The advantage of the IIC bus is that the required clock for the chips is provided by the IIC master residing on the GPAC that is stopped during measurements of the beam data. There are also directly wired signals from the RFFE for intra-train control of the GPAC (e.g. a fast attenuator adjusts for high differences between set and measured beam charge) or power handling if a board is removed during operation.

There are two IIC buses available on the RFFE board. One is for the power management and identification of the board whilst the second bus is for RF functionality:

Power IIC:
The HotSwap controllers check the power consumption and the voltage levels on the RFFE, the adjacent EEPROM stores the identification of the board and the power sequencing.

RF IIC:
The second IIC bus controls the main functionality of the RFFE whilst the adjacent EEPROM is intended for calibration settings of the board.

In order to compensate temperature dependent drifts, 6 temperature feedbacks (within +/- 0.1° C) stabilizes the temperature at particular locations on the RFFE board. The following figure shows the main control panel of the RFFE and should clarify some of the functions described.


BPM_GPAC_CAV_RFFE_3GHz3_120700B.ui

MTEST-VME-DIAG17-BPM1

RFFE CTRL

Check [°C] 0.50

RFFE Board

Attenuator DSA: R +0 0; X +1 9; Y +1 8

Temperature Feedback

TMP [°C]	SET [°C]	TMP [°C]	SET [°C]
45.00	45.0	45.06	45.0
45.06	45.0	45.00	45.0
45.13	45.0	45.06	45.0

IF Amplifier

	I/Q [°C]
R_I	39.94
R_Q	45.06
X_I	36.59
X_Q	36.91
Y_I	41.16
Y_Q	38.94

Phase phi; DAC [V] 1.280

LO PLL: R 8; N=BP+A: P 16/17, B 21, A 14; MUXOUT LOCK DET

Detektor: Power 0.000 V, 0.719 V; Diode [V] 1.410; SET [V] 1.400

Oscillator: 0.126 V

CCLK DDS: FTW 0x40000000; DAC 0x7f13ff; CFR1 0x0; CFR2 0x1432; PHASE +0 5 9 . 0 deg

CCLK PLL: R 1; N 8; MUXOUT LOCK DE

Figure 5: QT Control View of Blocks in the Cavity RFFE

The pickup signals (R, X, Y) are attenuated and then mixed with a signal provided by a PLL that is locked to the machine RF (MREF). The control panel above is only a subset of the features provided by the RFFE chips. In order to make the setting easier, only the relevant registers/features are implemented for the control system. These registers contain sometimes related control elements which have to be constructed from several setting on the user panel. In the display physical units are used instead of raw register content if sensible.

The ADC sampling clock is derived from the machine RF (MREF, 216.6667 MHz) by a DDS and multiplied / cleaned by the PLL.

For each channel the attenuator and mixer on the RFFE is temperature controlled. Whereby the local feedback systems maintains local board temperatures constant preventing temperature related drifts.

For additional information please refer to the RFFE [2] schematic and the related chip datasheets.

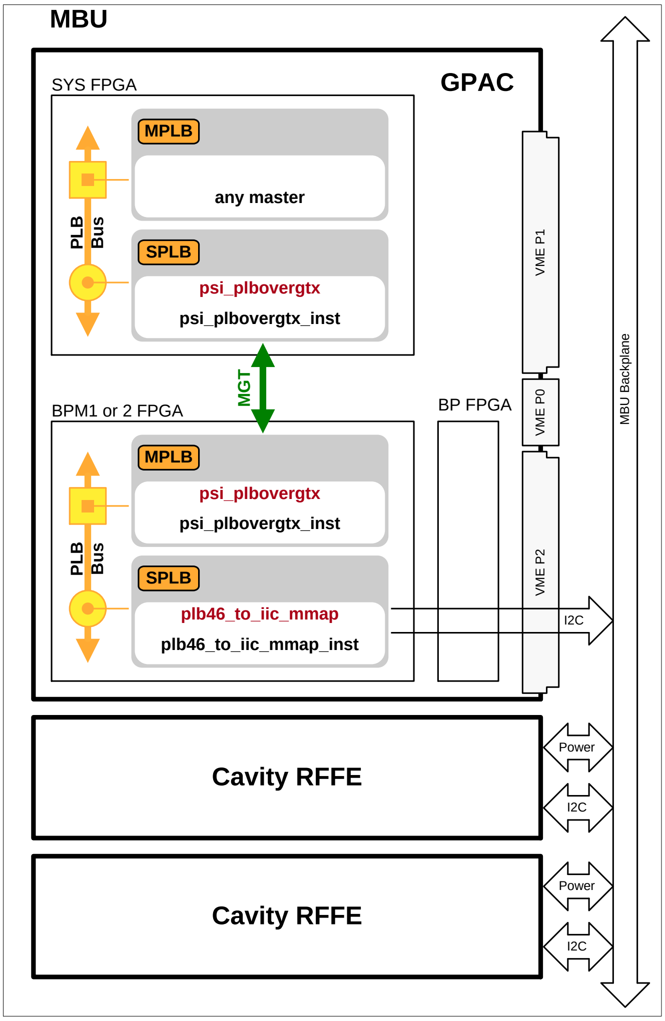


Figure 6: Overview on IIC Interface to the RFFE

The GPAC provides the user the interface to the IIC buses allowing control over the RFFE.
In order to allow several PLB masters access to the RFFE without interfering with a currently running request a PLB component called PLB46_to_IIC_MMAP was placed in the BPM FPGAs. This component provides a write FIFO interface to the IIC bus and a memory map of the data read from the IIC bus. The components allow an individual interrupt for signaling completion of a particular request to a particular master. The component reads, without master interaction after each bunch train particular IIC channels for quick access by the control system (e.g. temperatures, PLL lock indicators, etc.).

4 ADC16HL Interface overview

The mezzanine board ADC16HL contains a local oscillator 160 MHz (SL570), Clock distribution chip (LMK01020), six, 160 MSa/s, 16 bit ADCs (LTC2209), temperature sensors (ADT7301), offset compensation circuitry DAC (DAC7512) and ADC (LTC2448) all connected to a Spartan-3A FPGA. Each chip has different interfaces such as direct connections and serial protocols of varying bit length, phases and bit rates. The Spartan-3A FPGA acts as an intermediate layer hiding parts of the framing and communication interfaces from the user and providing a common interface to access them all.

The ADC16HL has differentially routed traces for the ADC data/clock and for the board settings. All signals are connected to the 500 pole connector matching the GPAC board. The board settings are carried out by means of a differentially routed serial protocol from the GPAC called FastLink.

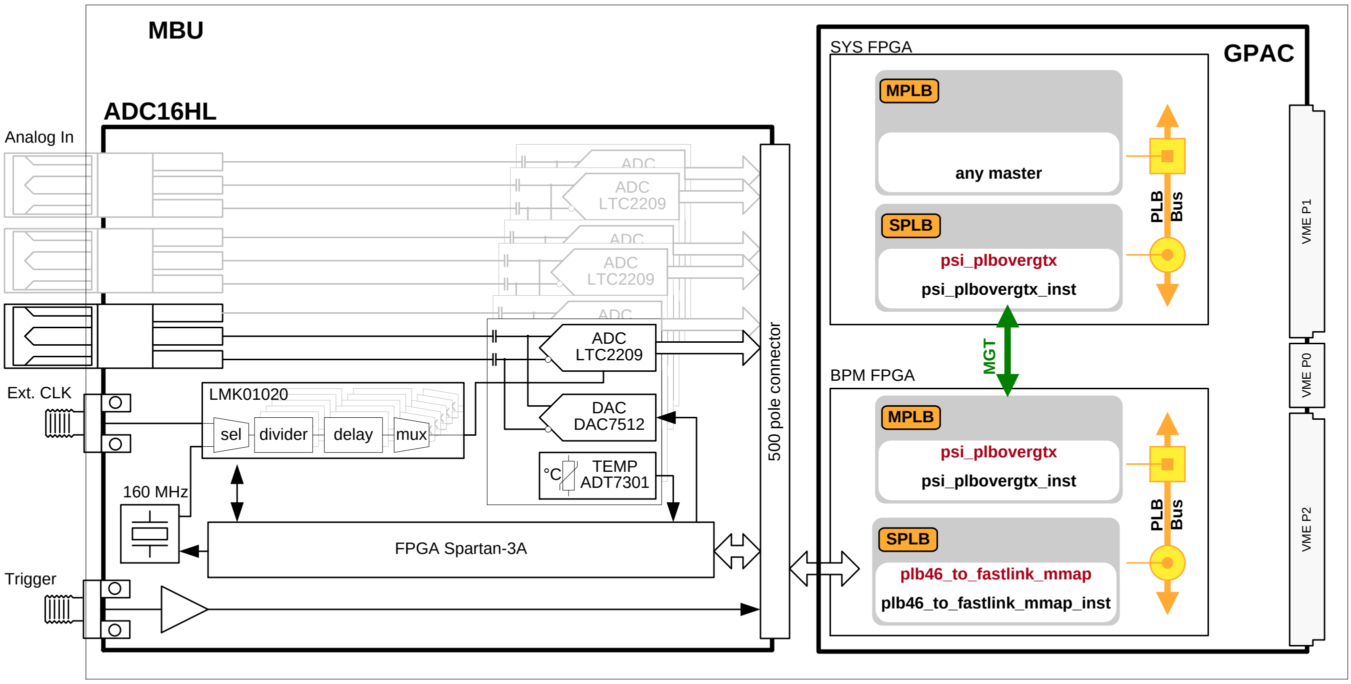
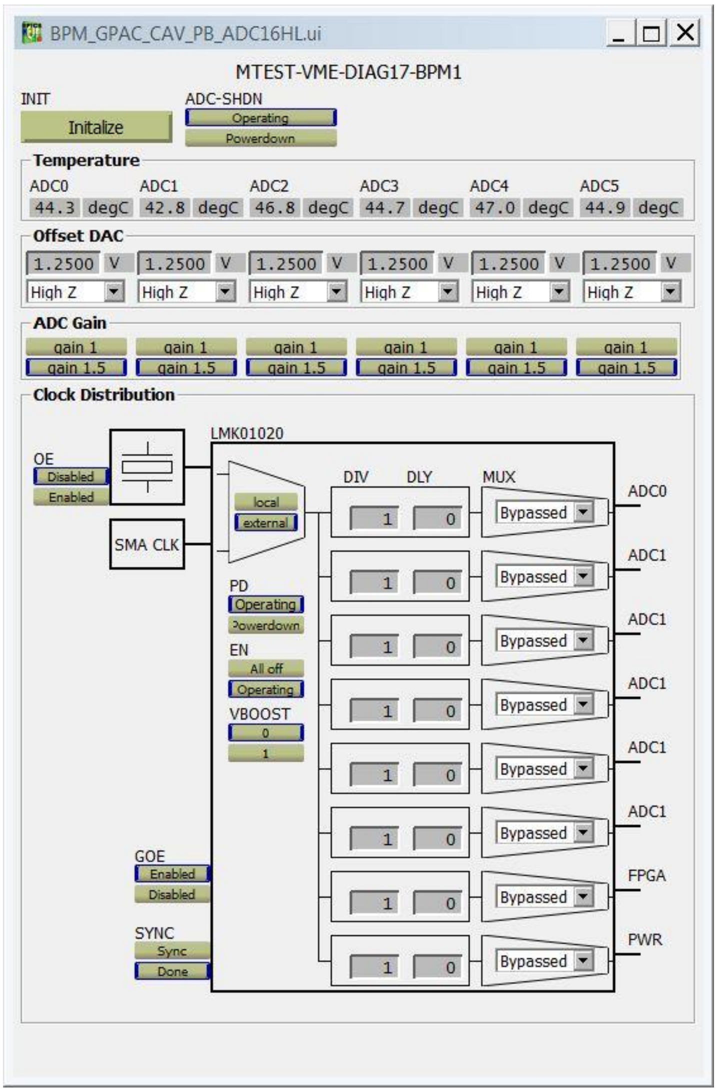


Figure 7: Overview on FastLink Interface to the ADC16HL

The GPAC provides the user the interface to the FastLink bus allowing control over the ADC piggyback board.

In order to allow several PLB masters access to the ADC16HL without interfering with a currently running request a PLB component called PLB46_to_FASTLINK_MMAP was placed in the BPM FPGAs.

This component provides a write FIFO interface to the FastLink bus and a memory map of the data read from the FastLink bus. The components allow an individual interrupt for signaling completion of a particular request to a particular master. The component reads without master interaction after each bunch train particular FastLink channels for quick access by the control system (e.g. temperatures, status, etc.).



BPM_GPAC_CAV_PB_ADC16HL.ui

MTEST-VME-DIAG17-BPM1

INIT: Initalize

ADC-SHDN: Operating / Powerdown

Temperature

ADC0	ADC1	ADC2	ADC3	ADC4	ADC5
44.3 degC	42.8 degC	46.8 degC	44.7 degC	47.0 degC	44.9 degC

Offset DAC

1.2500 V	1.2500 V	1.2500 V	1.2500 V	1.2500 V	1.2500 V
High Z	High Z	High Z	High Z	High Z	High Z

ADC Gain

gain 1	gain 1	gain 1	gain 1	gain 1	gain 1
gain 1.5	gain 1.5	gain 1.5	gain 1.5	gain 1.5	gain 1.5

Clock Distribution

DIV	DLY	MUX	
1	0	Bypassed	ADC0
1	0	Bypassed	ADC1
1	0	Bypassed	ADC1
1	0	Bypassed	ADC1
1	0	Bypassed	ADC1
1	0	Bypassed	ADC1
1	0	Bypassed	FPGA
1	0	Bypassed	PWR

Figure 8: QT Control View on Blocks in the ADC16HL

Figure 8 displays the user interface to the ADC16HL as a QT panel. This control panel is a subset of the features provided by the ADC16HL chips. To simplify the settings only relevant registers are used. These registers contain sometimes related control elements that have to be constructed from several setting on the user panel. In the display physical units are used instead of raw register content if sensible.

5 GPAC Interface overview

The processing of the digitized data is carried out in the BPM FPGA of the GPAC in a firmware called “bpm_cav_exfel”.

The processing firmware consists of several major blocks that are summarized next with more detail on the following pages:

A finite state machine (FSM) manages this core. The state machine receives the mode of operation from the user application and controls the various blocks in order to provide the desired functionality.

The data adjustment (ADJUST) block is needed in order to fulfill the setup and hold time requirements of the FPGA input flip-flops due to the feature of setting individual sampling clock delays for each ADC channel. For example the individual sampling clock phase matches up with the data rise and fall times and hence the FPGA needs to move the data sampling window away from these data changes into a stable region in order to consistently retrieve the data.

In order to move the trigger in time a programmable delay (DELAY) is implemented. This decouples the external trigger requirement to match exactly the occurrence of the trigger to the signal being measured.

The base line can be subtracted automatically from the measurement values in order to adjust for reference level fluctuations due to various effects (disturbance of other channels, pile up effects, temperature, offset of the RFFE amplifier, ADC variations, etc.). The user can select if the calculated baseline of each channel shall be subtracted. The calculated baseline is provided to the user as raw data (Base line calc), which is a feature that indicates the noise level on the cables.

The calculation block (CALC) carries out the main processing. For the BPM project a sophisticated calculation engine is required which resides in this block [3].

Finally the consistently sampled data is stored in memory (MEM) and can be read by the user. The outputs of the storages are connected to software accessible memory address spaces that in turn are readable by the control system as single values or bursts transfers (DMA).

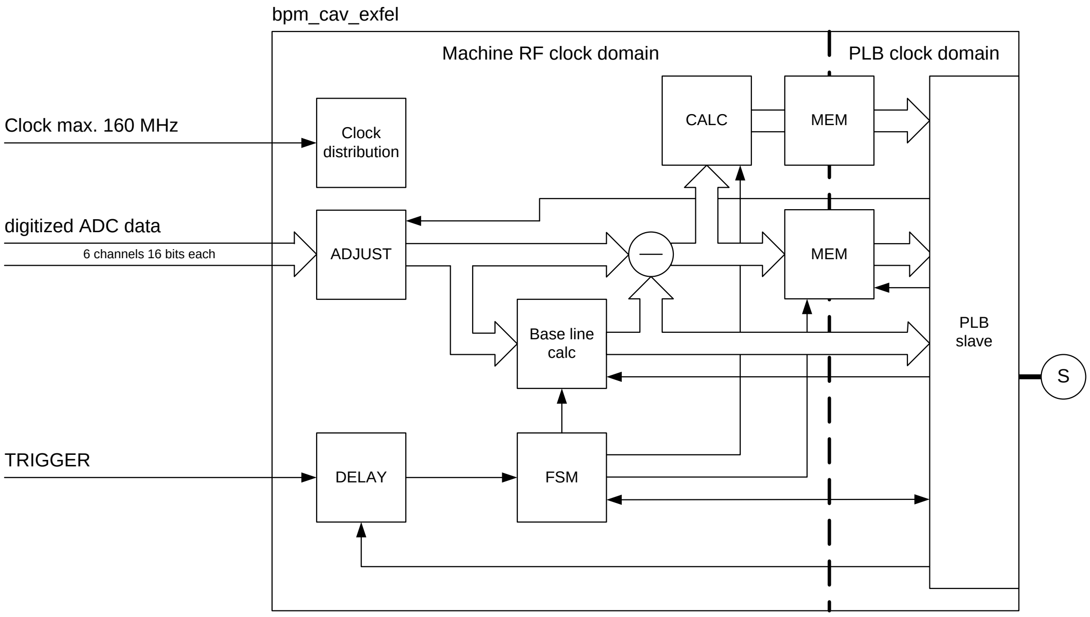


Figure 9: Block Diagram of the Firmware bpm_cav_exfel

Due to the main functionality, which is implemented in the calculation core, a rough overview will be given:

In a first step the peak of the reference I/Q ADC data has to be found inside the sampling window by the block called MAX.

After finding the I/Q peaks, a conversion from cartesian to polar coordinates are calculated (in the block CORDIC). The amplitudes (x_cd_amp, y_cd_amp and r_cd_amp) and phases (x_cd_phase, y_cd_phase and r_cd_phase) are stored for each bunch separately and can be retrieved by the control system. At the same time the Interpolation block calculates by means of a second order interpolation the top sample (s_top) and the deviation in degrees (t_top) from the peak is sampled. This information is important for a feedback which keeps the sampling point at the top of the analogue I/Q pulse.

The next calculation steps are performed for correcting various effects. First the I/Q imbalance is corrected, then a correction which accounts for the attenuator variation is done and finally a beam angle correction needs to be applied.

The next step is to divide the pickup position information with the charge in order to obtain the charge independent position information followed by scaling (x_egu, y_egu q_egu) to physical units [mm and pC].

To enable comparison of position information for several pickups, the mechanical shifts (rotation of the pickup compared to an arbitrary reference) have to be calculated. This is carried out by a rotation matrix (rot11…rot22) before the samples are stored in user accessible buffers.

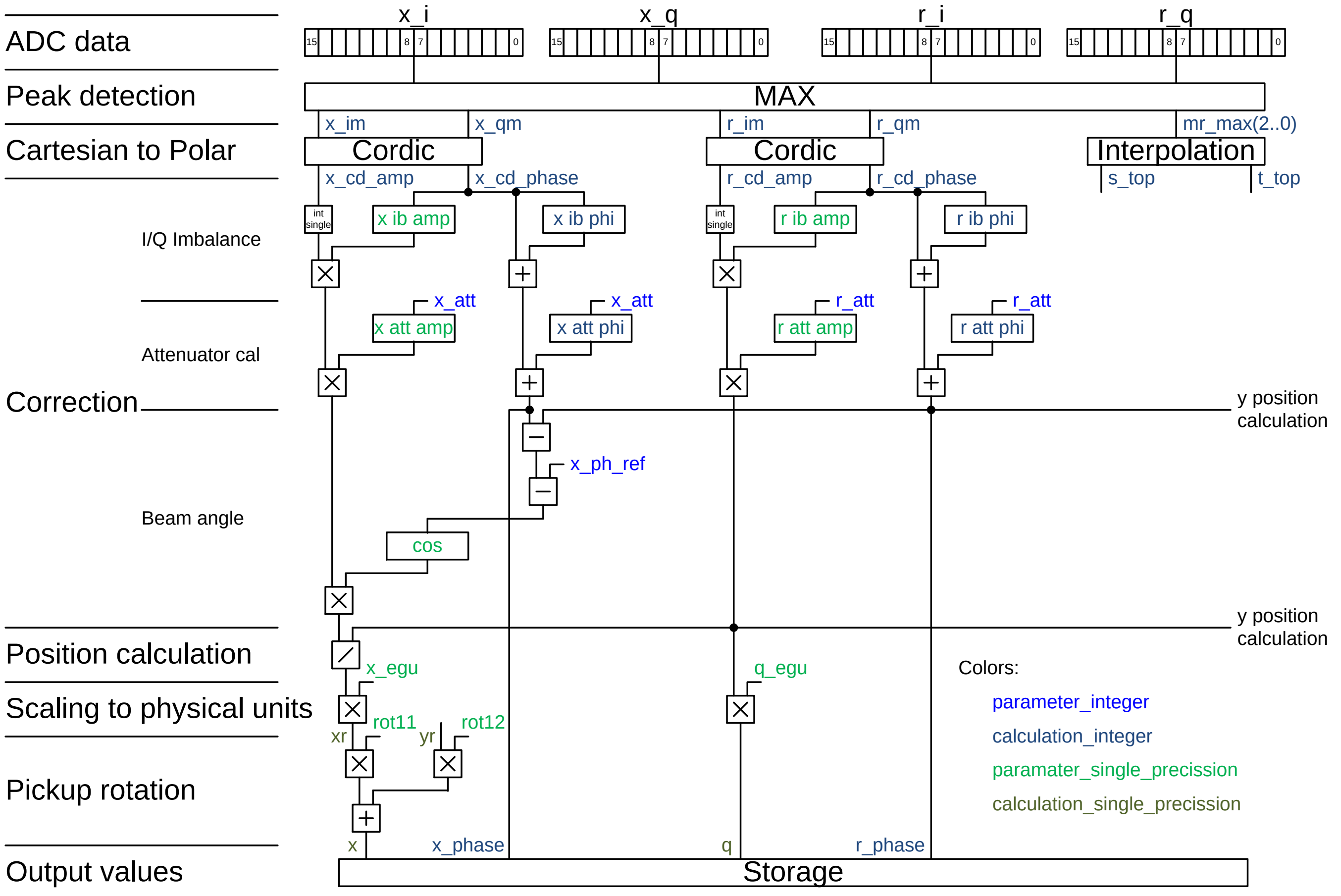
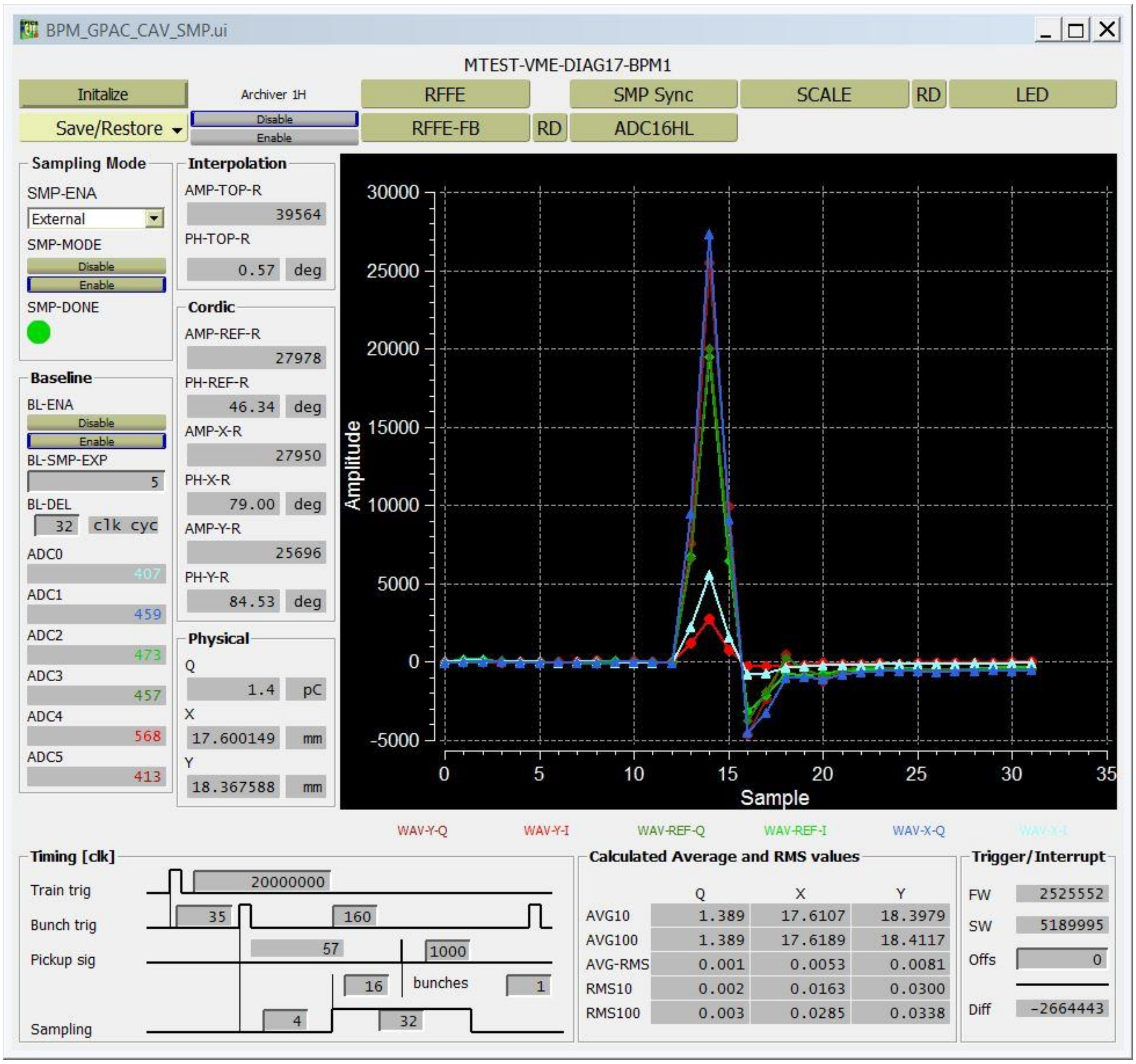


Figure 10: Calculation Pipeline

All the calculations so far are implemented in firmware due to performance reasons and to keep the latency as low as possible.



MTEST-VME-DIAG17-BPM1

Archiver 1H: Disable / Enable

Sampling Mode

SMP-ENA: External

SMP-MODE: Disable / Enable

SMP-DONE ●

Baseline

BL-ENA: Disable / Enable

BL-SMP-EXP: 5

BL-DEL: 32 clk cyc

ADC0: 407

ADC1: 459

ADC2: 473

ADC3: 457

ADC4: 568

ADC5: 413

Interpolation

AMP-TOP-R: 39564

PH-TOP-R: 0.57 deg

Cordic

AMP-REF-R: 27978

PH-REF-R: 46.34 deg

AMP-X-R: 27950

PH-X-R: 79.00 deg

AMP-Y-R: 25696

PH-Y-R: 84.53 deg

Physical

Q: 1.4 pC

X: 17.600149 mm

Y: 18.367588 mm

Timing [clk]

Train trig: 20000000

Bunch trig: 35, 160

Pickup sig: 57, 1000

16 bunches 1

Sampling: 4, 32

Calculated Average and RMS values

	Q	X	Y
AVG10	1.389	17.6107	18.3979
AVG100	1.389	17.6189	18.4117
AVG-RMS	0.001	0.0053	0.0081
RMS10	0.002	0.0163	0.0300
RMS100	0.003	0.0285	0.0338

Trigger/Interrupt

FW: 2525552

SW: 5189995

Offs: 0

Diff: -2664443

Figure 11: QT Control View of Blocks in the Sampled Data

Figure 11 displays the QT panel translating the features of the GPAC to human readable form allowing the user to customize the system to their needs or to the machine requirements.
Although the cartesian plot in the QT panel is only intended for commissioning it displays (equivalent to a high resolution oscilloscope) the raw input values used in the processing chain. Several signals from the processing chain (2nd order interpolation top and phase, the CORDIC amplitudes and phases) are visible to the user and may help identify problems in a simplified form.

6 Machine Interface Overview

The control (event) system of the E-XFEL machine will provide a signal denoted in this document as a bunch train trigger. This bunch train trigger informs the BPM that after a location dependant delay (B1.0) the bunch train will start; containing a predefined number of bunches (B0.0).

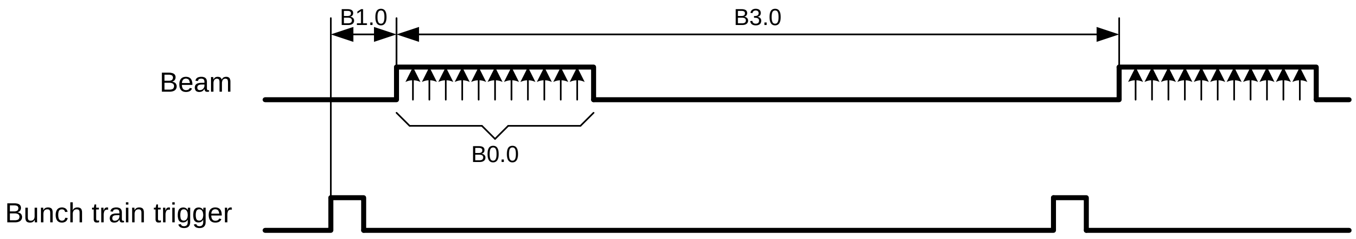


Figure 12: Machine Interface for the BPM

Time	Value	Description
B0.0	1…3072	Number of bunches in the bunch train. The BPM electronics will measure and calculate this amount of positions.
B1.0	System given	Delay between event transmitted on the event link cable (timing system of the machine) and the beam measured by a particular pickup. Stable delay, but depends on the position in the machine, hence different for each BPM
B3.0	max. 30 Hz	Bunch train repetition rate. This is a machine parameter, e.g. can be regarded as minimal delay between bunch trains.

The bunch train trigger is encoded in an event link of the E-XFEL.

7 Software Interface Overview

This chapter provides an overview and how the software [6] is related to other components/functions implemented in firmware and hardware. The most important point to realize is that the BPM FPGAs are implementing a Sytem On Chip (SOC) design using the PLB as multi-master, random access memory map, which means that all accesses can be done by the processor and in parallel by the control-system.

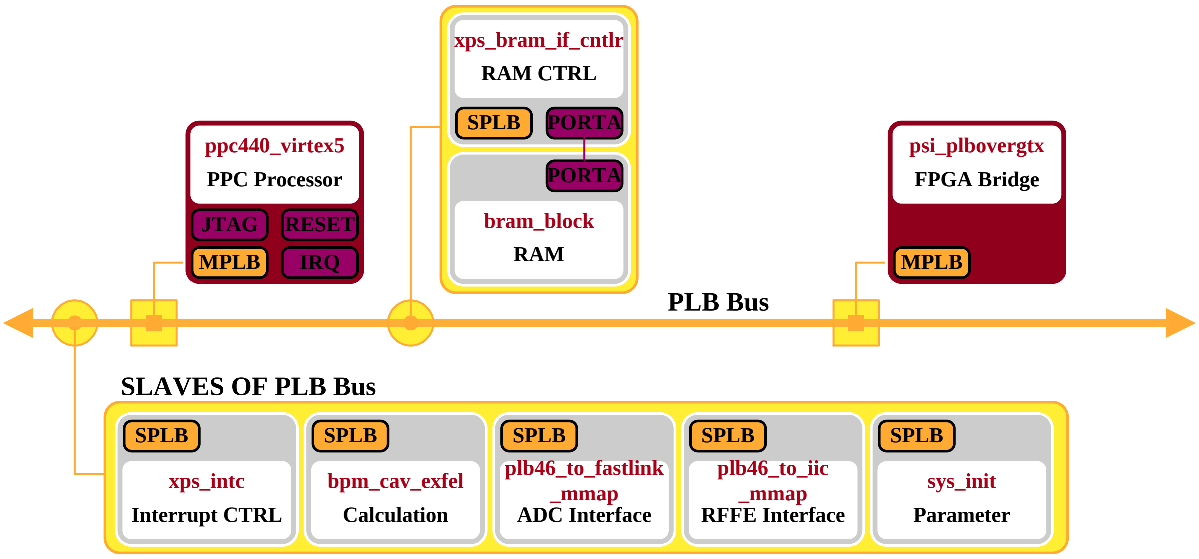


Figure 13: Cavity BPM SOC Firmware Overview (only a selection of used components)

The IBM® PLB is the backbone of the BPM FPGA firmware which allows connecting a PowerPC processor and a Multi Gigabit Tranceiver (MGT) based interface towards the control system as two independent masters on the bus. The PowerPC software is executed in a memory which is inside the FPGA and which is loaded together with the FPGA firmware. This means no additional loading of software is needed after the FPGA has got its firmware.
There are as well several slave components connected on the PLB. Some of these slave components are for organizing the processor like the interrupt controller (xps_intc), others are doing the interfacing to the cards (plb46_to_fastlink_mmap and plb46_to_iic_mmap), some implement a specialized storage for parameters (sys_init) and the main number crunching and data processing is done in the bpm_cav_exfel [5] component. For more details please refer to the documentation of the individual firmware implementations [6].

The next figure illustrates the main devices used in the BPM system. On the left hand side the pickups are drawn, which are connected to the RFFE by several meter long RF cables. Within the RFFEs the 3.3 GHz signals from the pickups are mixed with a machine RF derived frequency to obtain a pulse long enough to be measured with the six, 16 bit, 160 MSa/s ADC on the ADC16HL piggyback board. The ADC data is processed in the BPM FPGA on the GPAC and the results of the measurements and preprocessing calculations are finally provided to the control system.

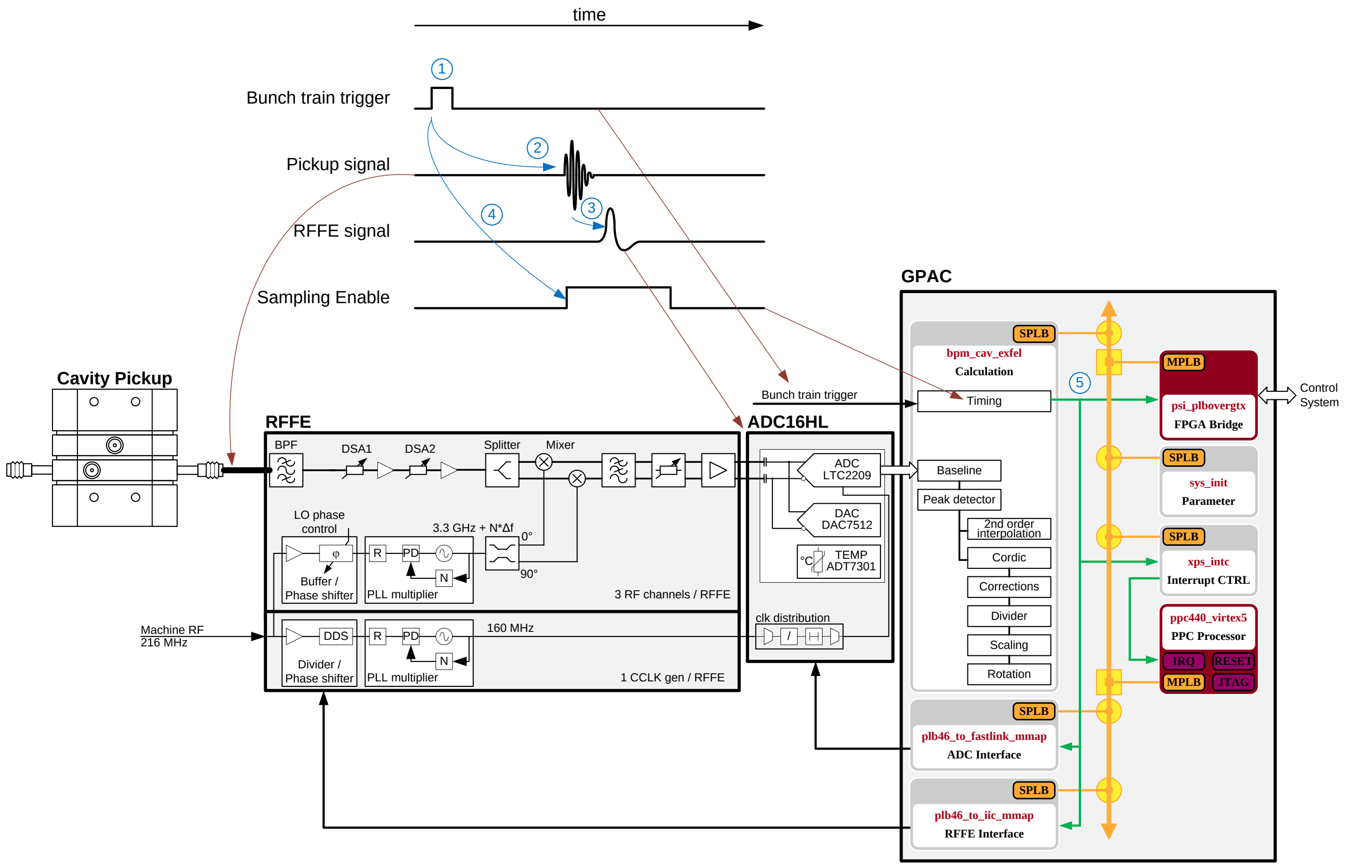


Figure 14: Cavity BPM Overview

The blue bullets in the figure above denote the following timing:

1.) The timing and event system of the machine provides a trigger pulse to the GPAC. Informing the GPAC that a new electron bunch is imminent.

2.) The electron bunch passing the pickup causes the pickup to generate a response oscillation (decaying 3.3 GHz oscillation).

3.) The RFFE down-converts the pickup response to a lower frequency (mixing the decaying pickup oscillation with a generated, stable, continuous 3.3 GHz signal)

4.) The GPAC opens a sampling window for the bunch to take measurements and do the beam parameter (position and charge) calculation. Basically sampling of ADC data and preprocessing the measurements.

5.) After completing the measurement/calculation an interrupt is issued to the control system to inform, that new data is available and ready to be picked up. At the same time it automatically triggers the read back of status information (temperatures, PLL lock status, …) from the ADC16HL board and the RFFE board.

The control system configures the BPM system by means of providing signals and information concerning the timing of the beam (a very stable machine RF and event system containing bunch train trigger, bunch number, etc.), the charge and filling pattern expected. This information has to be sent to the BPM system in advance, e.g. before the bunch train is fired.

7.1 Software based Set Values

There are several boards in a BPM system working together in order to measure the position and charge of the beam passing the pickup.
All these boards contain chips which have to be initialized or configured before they can contribute to the measurement. Because the interface to the boards (plb46_to_fastlink_mmap and plb46_to_iic_mmap) is reachable by memory access the user may choose to retrieve values directly from the hardware or write data directly to the hardware registers, however then the user has to construct the bit-patterns expected by the respective hardware chip. It turned out that this means a lot of bit arithmetic for the user which the user would like to avoid. For this feature a memory component was implemented (sys_init) which is readable and writable by the user. This component separates each setting into an own memory address, which isolates the various settings for the user (no needed for bit arithmetic, shift, mask, ...). The local processor on the GPAC constructs the register word as needed by the hardware and writes this word to the interface.

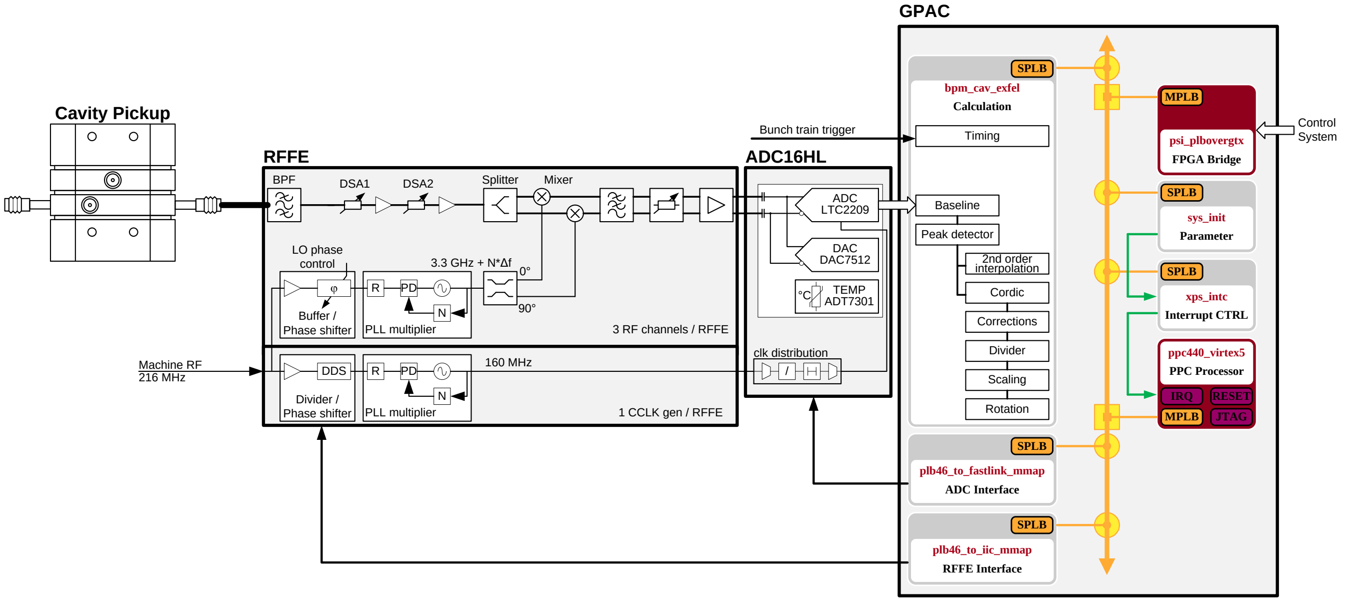


Figure 15: Set Values

7.2 Software based Sampling Time Feedback (DDS Feedback)

The sampling clock used by the ADCs is as well generated in the RFFE board. In order to minimize effects caused by the sampling clock jitter, the ADC sampling point shall be at the top of the I and Q pulse. Due to the same source of LO path and ADC clock generation in the RFFE board the sampling will have a fixed phase. The clock generation contains a DDS (Direct Digital Synthesis) chip which is basically a phase counter, phase offset register, phase-to-amplitude lookup table and a DAC. The phase offset register in the DDS chip is hence a simple way to move the ADC sampling clock in time (phase difference to the pickup signal)

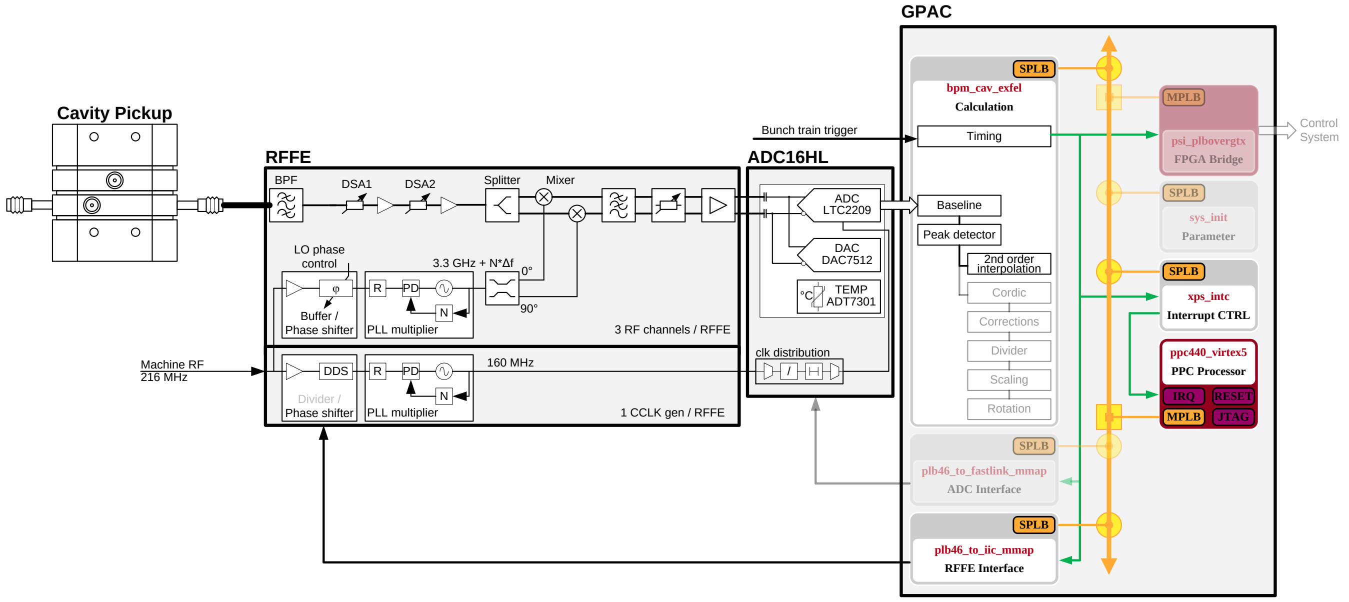


Figure 16: Sampling Time Feedback

The GPAC calculates from the 3 top samples of the pulse by means of a second order interpolation the top sample amplitude and the top sample phase. The top sample phase in turn is used in a software implemented PI feedback loop to control the DDS phase offset register.

In order to keep the ADC sampling of the I/Q pulse at the top, a feedback is implemented in the GPAC varying the DDS phase such that the desired second interpolation top phase is met. The feedback is basically a PI controller and due to its nature to correct slow drifts not a very performant implementation. This PI controller runs slowly in a software interrupt context.

7.3 Software based I/Q Phase Feedback

For the measurement accuracy it makes sense if the two ADC channels I and Q are both at full range. If the I and Q channel have the same amplitude then this leads to a 45° angle between I and Q value which in turn is the output of the CORDIC calculation. All we need to do, is to keep the I/Q phase of the reference channel at 45° by means of the LO phase shifter. This calculation is done as well in software with a simple PI feedback controller.

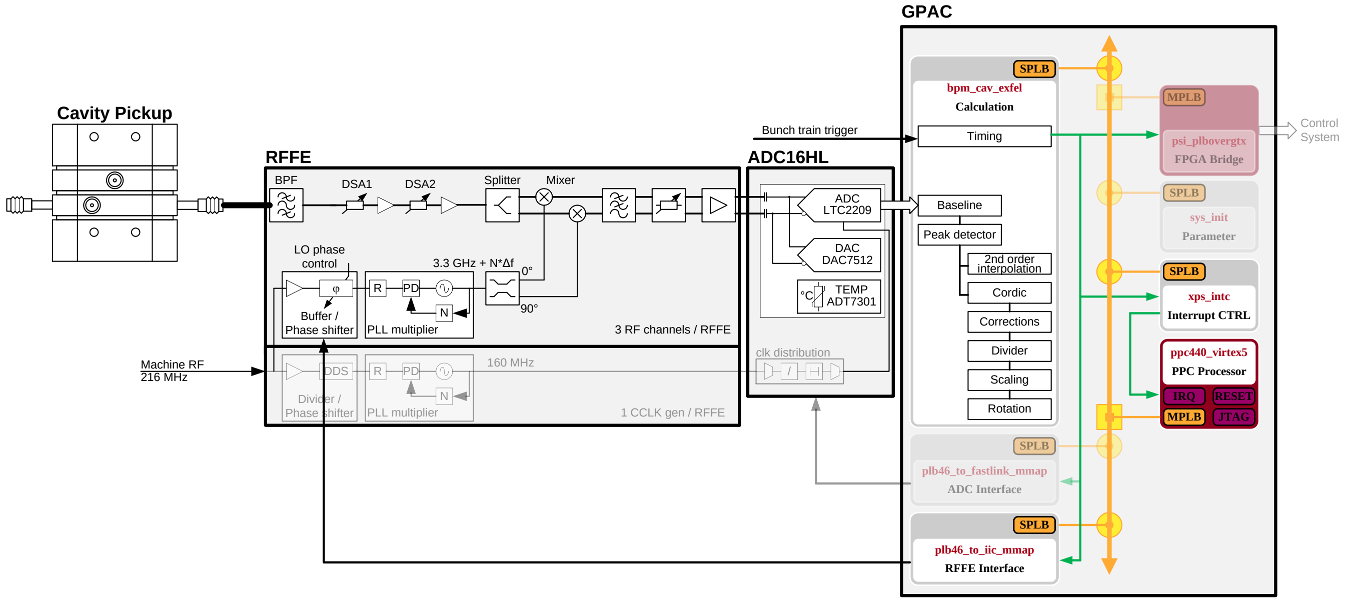


Figure 17: I/Q Phase Feedback

In order to minimize the sample to noise ratio both (I and Q) ADC samples are used at a high value. For this a feedback is implemented in the GPAC varying the LO phase such that the desired angle between I and Q is close to 45°. The feedback is basically a PI controller and due to its nature to correct slow drifts not a very performant implementation. This PI controller runs slowly in a software interrupt context.

7.4 Software based Attenuator Feedback

The charge of the beam can be changed over a wide range. In order to adjust for high beam currents attenuators are included in the RFFE board. These attenuators are automatically driven by the GPAC in a feedback in order to use the full range of the ADC independently from the beam charge set.

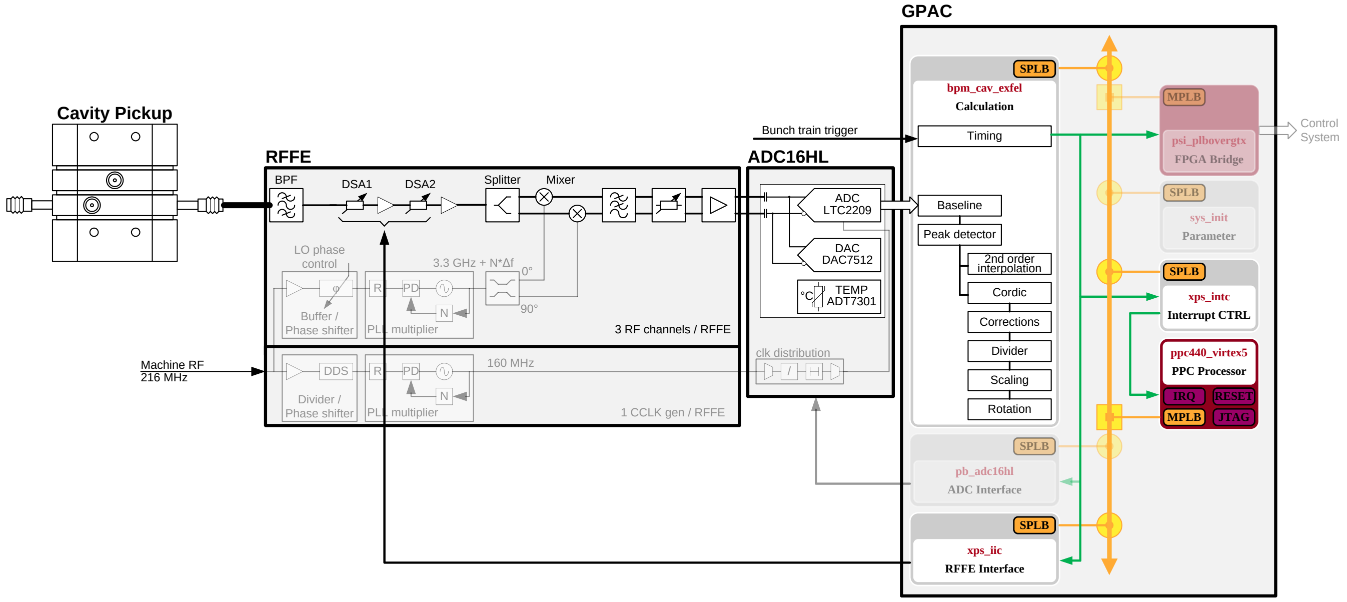


Figure 18: Attenuator Feedback

8 User interface

The user has full access to all registers by means of a simple address map (in contrast to systems which run function code). The PLB is a multi master system providing read and write access to more than one control unit. The PLB components are burst enabled hence chunks of data can be read (e.g. DMA access) in order to achieve a high data throughput in a system.
For detailed information on the blocks presented please refer to the links in the reference section they will guide you to the documents and provide additional information.

9 Appendix

None.