XFEL ADC16HL Firmware Interface Data Sheet

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1 Introduction

For the European XFEL project a fast 160 MSa/s ADC card with 6 channels for the use with cavity RFFEs was developed. This card contains temperature sensors, offset compensation circuits, clock distribution (delay and divider) and other features of minor importance (firmware version, LED interface, etc.).
The ADC16HL mezzanine board is a 6 channel ADC board with a resolution of 16 bit and a sampling rate of 160 MSa/s. The 500 pole mezzanine connector matches the PDC and GPAC carrier board pinning. All analog inputs are connected differentially to RADIALL connectors on the front. The sampling clock for the ADC's can be fed from a SMA connector, single ended or an internal free running 160 MHz quartz oscillator clock. The selection of the clock source/frequency/delay is configured at runtime by software.

1.1 Purpose

This document describes the firmware developed based on the schematic [2] and hardware user document [3].

1.2 Scope

The main scope is the Cavity BPM for the European XFEL, however the electronics is generic enough to be used many other projects/applications additionally.

1.3 Definitions, acronyms, and abbreviations

This document is based on the "IEEE Recommended Practice for Software Requirements Specifications" [1].

FPGA	Field Programmable Gate Array
Reg	Register. Mathematically z^-1
SPI	Serial Port Interface.
IIC	Inter Integrated Circuit bus. A Philips® specified serial bus used by various chip companies world wide.

1.4 References

[1] IEEE Std 830-1998, Recommended Practice for Software Requirements Specifications.
[2] PSI 2011, Schematic X-FEL BPM Electronics ADC16HL, ADC16HL_V2_Schematic.pdf
01_Reference\ADC16HL_V2_Schematic.pdf and 01_Reference\ADC16HL_V2_Assembly.pdf
[3] PSI 2009, User manual ADC16HL V2, Revision 1.0, ADC16HL_V2_Manual.pdf
01_Reference\ADC16HL_V2_Manual.pdf
[4] PSI 2005, FastLink Firmware Data Sheet fast_link_datasheet.rtf
01_Reference\fast_link_data_sheet.pdf
[5] National Semiconductor 2009, Datasheet LMK01000 Family 1.6 GHz High Performance Clock Buffer, Divider, and Distributor
01_Reference\lmk01000.pdf
[6] Linear Technology 2007, Datasheet 16-Bit, 160Msps ADC LTC2209

01_Reference\2209fb.pdf
[7] Analog Devices 2005, Datasheet Digital Temperature Sensor ADT7301
01_Reference\ADT7301.pdf
[8] Burr-Brown 2002, Datasheet 12-Bit Serial Input DAC, DAC7512
01_Reference\dac7512.pdf
[9] Linear Technology 2004, Datasheet 24-Bit High Speed 8-/16-Channel ΔΣ ADC, LTC2448
01_Reference\2444589fb.pdf

1.5 Overview

This document provides a detailed overview of the firmware interface and specifies the user interface.

2 Overall description

The mezzanine board ADC16HL contains a local oscillator 160 MHz (SL570), clock distribution chip (LMK01020) [5], six 160 MSa/s 16 bit ADCs (LTC2209) [6], temperature sensors (ADT7301) [7], offset compensation circuitry DAC (DAC7512) [8] and ADC (LTC2448) [9] all connected to a Spartan-3AN FPGA. Each chip has different interfaces such as direct connections and serial protocols of varying bit length, phases and bit rates. The Spartan-3AN FPGA acts as an intermediate layer hiding parts of the framing and communication interfaces from the user and provides a common interface to access them all.
The main clock (FB_U_CLK) may be switched off during measurement in order to prevent the clock of the FPGA interfering with the measurement.
The ADC16HL provides to the user the information (FB_U_IDLE) whether the current request received is still processed or whether new data can be accepted.

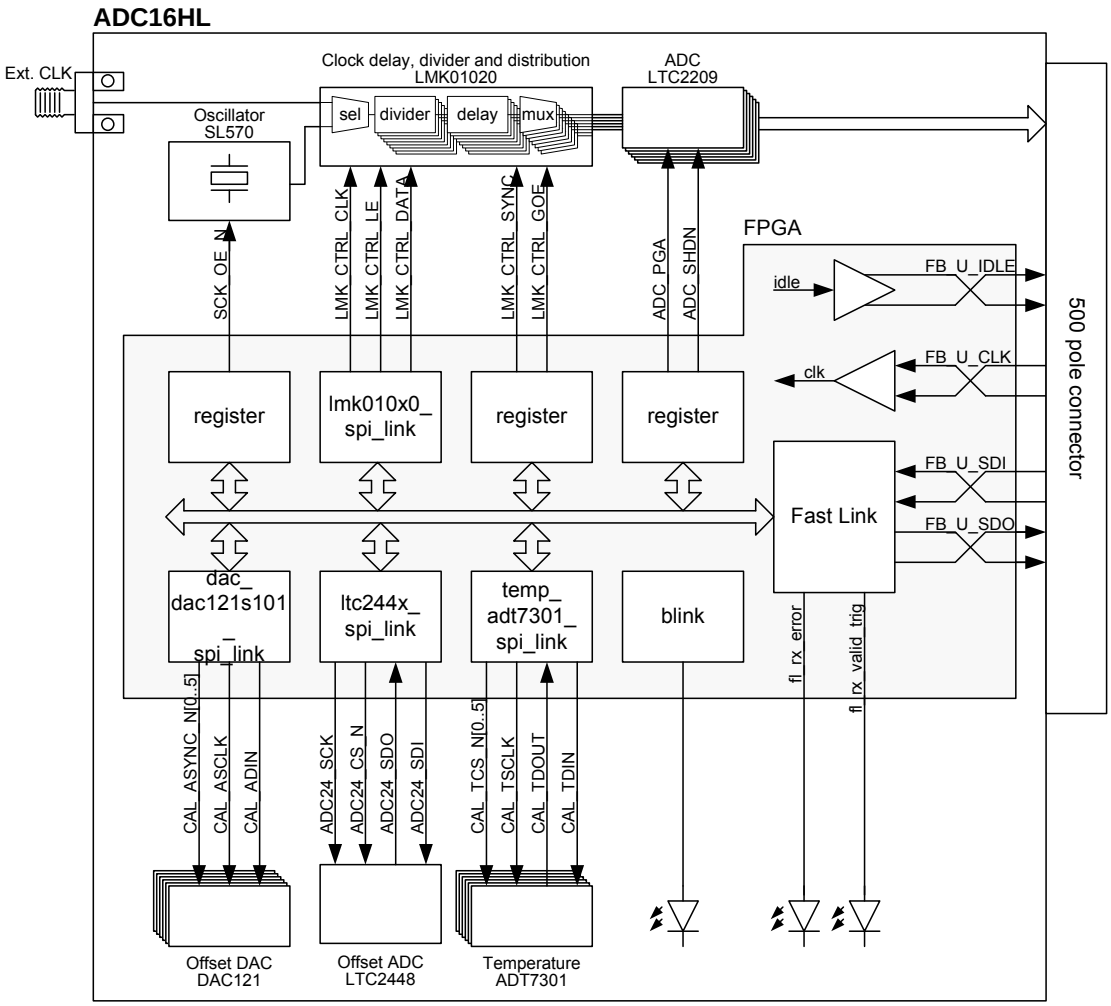

Figure 1: Overview

The ADC16HL has differentially routed 100 Ohm traces for the ADC data/clock and for the board settings. All signals are connected to the 500 pole connector matching the GPAC board pinning. The board settings are configured by means of a differentially routed serial protocol from the GPAC to the ADC16HL called FastLink [4].

The FastLink [4] is a serial link which transmits four 16 bit words. After each 4 bits of data a stuffing bit (inverted predeceasing bit) is inserted for resynchronization purposes. The frame begins with “start of frame” (SOF) bit which is always “1”. Then the following 15bits form the address, indicating the recipient of the following 16 bit of data. The frame is protected by a 16 bit CRC checksum. The frame finishes with an inter frame gap allowing the receiver to detect clearly the following SOF.

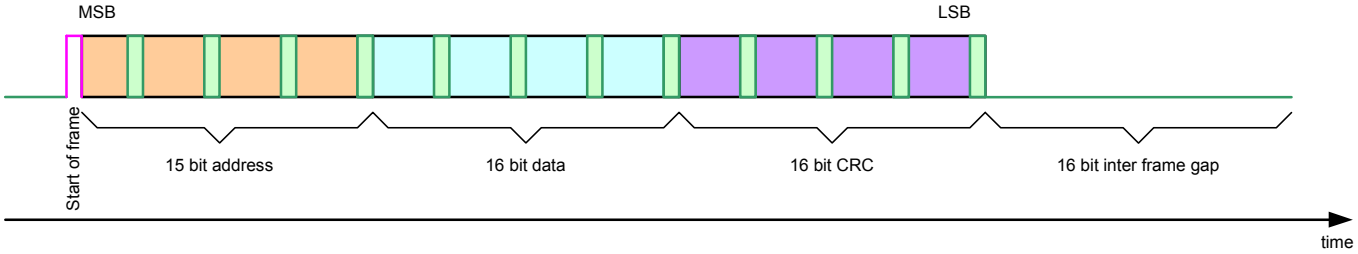

Figure 2: Frame Overview

2.1 User interface

2.1.1 FastLink Register ADT7301

This chapter is a summary and contains information from the Analog Devices datasheet [7]. For more information please refer to the schematic [2] of the ADC16HL and the relevant datasheets.

The ADC16HL mezzanine uses, for each of the six ADCs an individual temperature sensor for temperature monitoring (to improve life time of electronics due to ventilation/cooling failures) and adjustment of sampled data.
The ADT7301 is a temperature monitoring system in one small chip. It contains a band gap temperature sensor and a 13 bit ADC to measure the temperature with a resolution of 0.03125°C.

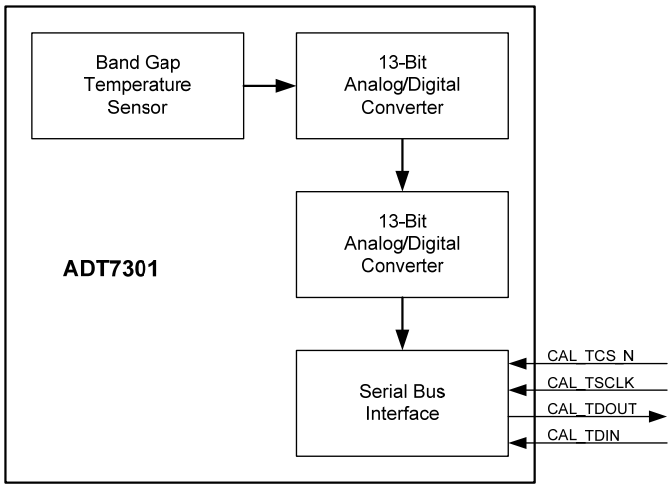

Figure 3: ADT7301 Block Diagram and Interface

The temperature value register is a 14 bit read only register that stores the temperature reading from the ADC in 13 bit “two complement” format plus a sign bit. The MSB (DB13) is the sign bit. The ADC can theoretically measure a 255°C temperature span. The internal temperature sensor has a working range from –40°C to +150°C.

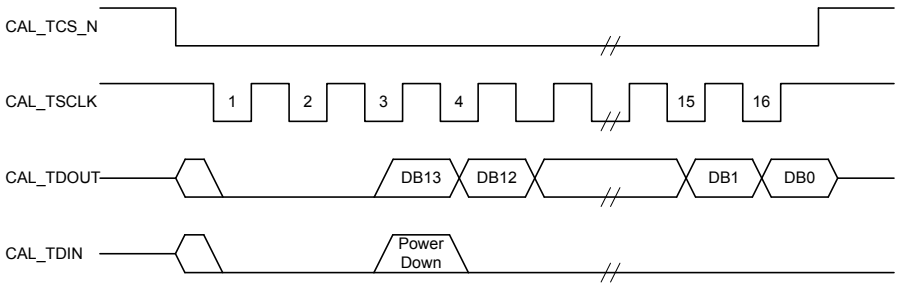

Figure 4: ADT7301 SPI Frame

On the ADC16HL board the SPI interface of the temperature sensors are connected to the FPGA and can be read by the FastLink.

Address	R/W	Bit	Name	Description
0x0000	W	0	ADT7301_0	SPI link to ADT7301ARMZ bit 13 ‘0’ = Normal operation ‘1’ = Chip powered down
	R	13:0	ADT7301_0	Positive temperature = d / 32 Negative temperature = (d − 16384) / 32
0x0001	W	0	ADT7301_1	SPI link to ADT7301ARMZ bit 13 ‘0’ = Normal operation ‘1’ = Chip powered down
	R	13:0	ADT7301_1	Positive temperature = d / 32 Negative temperature = (d − 16384) / 32
0x0002	W	0	ADT7301_2	SPI link to ADT7301ARMZ bit 13 ‘0’ = Normal operation ‘1’ = Chip powered down
	R	13:0	ADT7301_2	Positive temperature = d / 32 Negative temperature = (d − 16384) / 32
0x0003	W	0	ADT7301_3	SPI link to ADT7301ARMZ bit 13 ‘0’ = Normal operation ‘1’ = Chip powered down
	R	13:0	ADT7301_3	Positive temperature = d / 32 Negative temperature = (d − 16384) / 32
0x0004	W	0	ADT7301_4	SPI link to ADT7301ARMZ bit 13 ‘0’ = Normal operation ‘1’ = Chip powered down
	R	13:0	ADT7301_4	Positive temperature = d / 32 Negative temperature = (d − 16384) / 32
0x0005	W	0	ADT7301_5	SPI link to ADT7301ARMZ bit 13 ‘0’ = Normal operation ‘1’ = Chip powered down
	R	13:0	ADT7301_5	Positive temperature = d / 32 Negative temperature = (d − 16384) / 32

Table 1: ADT7301 FastLink Register Map

2.1.2 FastLink Register LMK010x0

This chapter is a summary and contains information from the National Semiconductor datasheet [5]. For more information please refer to the schematic [2] of the ADC16HL and the relevant datasheets.

The ADC16HL mezzanine uses, for each of the six ADCs, a separate clock for sampling the ADC data. The clock distribution chip allows to delay and/or divide the channels individually providing a flexible solution matching many sampling rate requirements of applications.

The LMK01000 family provides an easy way to divide and distribute high performance clock signals throughout the system. The LMK01000 family features two programmable clock inputs that allow the user to dynamically switch between different clock domains. Ether the machine reference might be used for machine synchronous sampling or a local oscillator for applications not needing such synchronization. The device features 8 clock outputs with independently programmable delay and divider adjustments.

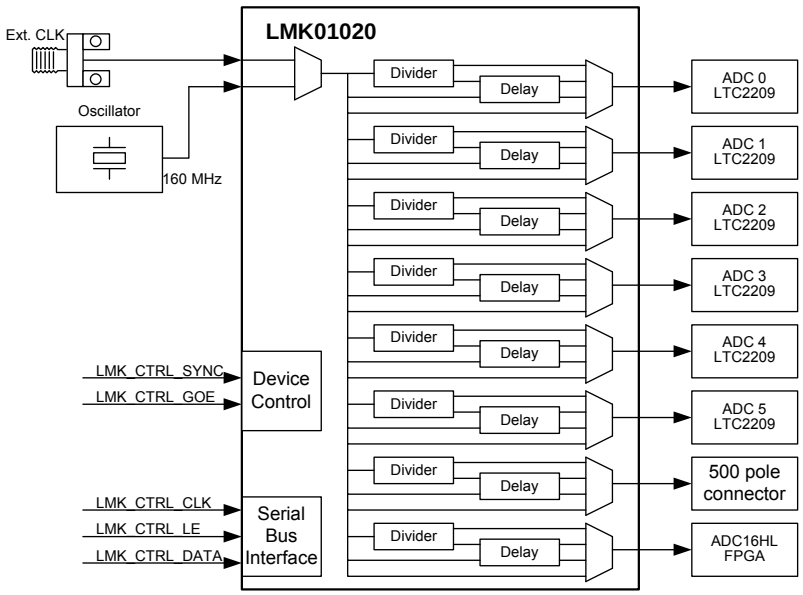

Figure 5: LMK01020 Block Diagram and Interface

The sampling clock can be derived from the machine RF for synchronous sampling or a local 160 MHz oscillator can be selected.
Each ADC is connected individually to the clock distribution chip. This implies that each ADC can sample at another phase (delay) and with a different sampling rate (divider).
One of the clocks is routed directly to the 500 pole connector and is intended to be used in a FPGA connected to the ADC16HL. This clock can be used for further processing of the digitized data.
There is one clock trace routed directly to the FPGA (Spartan3) on the ADC16HL board for synchronization of the switched power supply on the board with the analog data sampling.

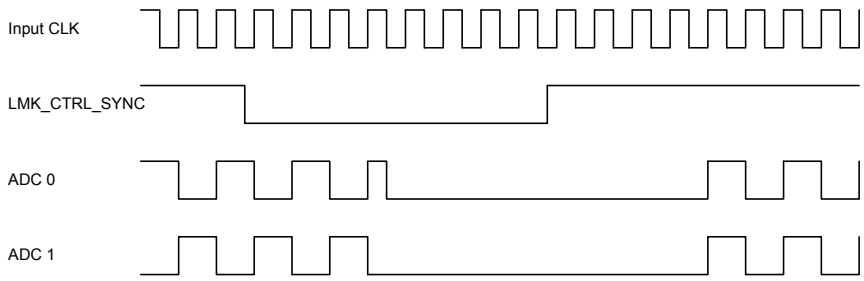

Figure 6: LMK01020 Clock Synchronization

When dividing a clock the phase info could be lost. The outputs of the device can be easily synchronized by an external pin called LMK_CTRL_SYNC.
The pin LMK_CTRL_GOE is the global output enable also used to stop outputs during configuration preventing the clock distribution chip from producing transients and/or invalid clocks. The chip internal multiplexors, dividers, delays and other features have to be configured using an SPI link to the chip.

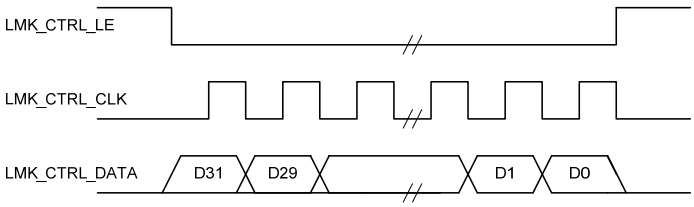

Figure 7: LMK01020 SPI Frame

The LMK01020 SPI is a 32 bit long serial stream starting with the MSB. Due to the nature of the FastLink of 16 bit data registers, two write accesses, first to the least significant 16 bits LMK010x0_LW and then to the most significant 16 bits LMK010x0_HW, have to be transmitted in order to start the SPI data frame from the ADC16HL FPGA to the LMK01020 registers in the chip.

Address	R/W	Bit	Name	Description
0x0006	W	15:0	LMK010x0_LW	LMK01000 clock distribution chip least significant word (bits 15:0) for 32 bit SPI
0x0007	W	15:0	LMK010x0_HW	LMK01000 clock distribution chip most significant word (bits 31:16) for 32 bit SPI Writing to this address triggers also the SPI link and the message is transmitted to the LMK01000
0x000F	W	7	LMK_CTRL_SYNC	Global clock output synchronization pin '0' = All divided clocks are set to logic low. '1' = All divided clocks are activated and will transition to a high state simultaneously.
	W	8	LMK_CTRL_GOE	Global output enable pin '0' = All the clock outputs are disabled. '1' = All the clock outputs are enabled.
0x0015	R	7	LMK_CTRL_SYNC	Global clock output synchronization pin '0' = All divided clocks are set to logic low. '1' = All divided clocks are activated and will transition to a high state simultaneously.
	R	8	LMK_CTRL_GOE	Global output enable pin '0' = All the clock outputs are disabled.

				'1' = All the clock outputs are enabled.

Table 2: LMK01020 FastLink Register Map

2.1.2.1 LMK01020 Internal Register Map

The transmitted frame contains in its 4 LSBs the register address followed by the 28 bit with the register content.

Reg.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data[27:0]																												A3	A2	A1	A0
R0	RESET	0	0	0	0	0	0	0	0	0	0	0	0	CLKout0_MUX		CLKout0_EN	CLKout0_DIV								CLKout0_DLY				0	0	0	0
R1	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout1_MUX		CLKout1_EN	CLKout1_DIV								CLKout1_DLY				0	0	0	1
R2	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout2_MUX		CLKout2_EN	CLKout2_DIV								CLKout2_DLY				0	0	1	0
R3	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout3_MUX		CLKout3_EN	CLKout3_DIV								CLKout3_DLY				0	0	1	1
R4	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout4_MUX		CLKout4_EN	CLKout4_DIV								CLKout4_DLY				0	1	0	0
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout5_MUX		CLKout5_EN	CLKout5_DIV								CLKout5_DLY				0	1	0	1
R6	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout6_MUX		CLKout6_EN	CLKout6_DIV								CLKout6_DLY				0	1	1	0
R7	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout7_MUX		CLKout7_EN	CLKout7_DIV								CLKout7_DLY				0	1	1	1
R9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Vboost	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	1
R14	0	1	CLKin_SELECT	0	EN_CLKout_Global	POWER DOWN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Table 3: LMK01020 Internal Register Map

2.1.2.2 LMK01020 Internal Register Map R0 to R7

The registers R0 to R7 contain the functionality of the eight clock channels:

CLKoutX_MUX[1:0] - Clock Output Multiplexers:

These two bits control the Clock Output Multiplexer for each clock output. Changing between the different modes changes the blocks in the signal path and therefore incurs a delay relative to the Bypassed mode. The different MUX modes and associated delays are listed below.

CLKoutX_MUX[1:0]	Mode	Added Delay Relative to Bypassed Mode
0	Bypassed	0 ps
1	Divided	100 ps
2	Delayed	400 ps (In addition to programmed delay)
3	Divided and Delayed	500 ps (In addition to programmed delay)

Table 4: LMK01020 Internal Register R0 to R7 CLKoutX_MUX

CLKoutX_DIV[7:0] - Clock Output Dividers

These eight bits control the clock output divider value. In order for these dividers to be active, the respective CLKoutX_MUX bit must be set to either "Divided" or "Divided and Delayed" mode. After all the dividers are programmed, the LMK_CTRL_SYNC pin must be used to ensure that all edges of the clock outputs are aligned. By adding the divider block to the output path a fixed delay of approximately 100 ps is incurred.
The actual Clock Output Divide value is twice the binary value programmed as listed in the table below.

CLKoutX_DIV[7:0]	Clock Output
0	Invalid
1	2
2	4
3	6
4	8
5	10
…	…
255	510

Table 5: LMK01020 Internal Register R0 to R7 CLKoutX_DIV

CLKoutX_DLY[3:0] - Clock Output Delays

These four bits control the delay stages for each clock output. In order for these delays to be active, the respective CLKoutX_MUX bit must be set to either "Delayed" or "Divided and Delayed" mode. By adding the delay block to the output path a fixed delay of approximately 400 ps is incurred in addition to the delay shown in the table below.

CLKoutX_DLY[3:0]	Delay [ps]
0	0
1	150
2	300
3	450
4	600
5	750
6	900
7	1050
8	1200
9	1350
10	1500

11	1650
12	1800
13	1950
14	2100
15	2250

Table 6: LMK01020 Internal Register R0 to R7 CLKoutX_DLY

CLKoutX_EN bit - Clock Output Enables
This bit controls whether an individual clock output is enabled or not. If the EN_CLKout_Global bit is set to zero or if GOE pin is held low, all CLKoutX_EN bit states will be ignored and all clock outputs will be disabled.

2.1.2.3 LMK01020 Internal Register Map R9 and R14

The registers R9 and R14 contain global signals affecting all channels.

Vboost - Voltage Boost Bit
Enabling this bit sets all clock outputs in voltage boost mode which increases the voltage at all outputs. This can improve the noise floor performance of the output, but also increases current consumption, potentially causing the output levels to be too high to meet the LVPECL/LVDS specifications. For the maximum frequency of 160 MHz this value should be set to low.

POWERDOWN Bit - Device Power Down
This bit can power down the device. Enabling this bit powers down the entire device and all blocks, regardless of the state of any of the other bits or pins.

EN_CLKout_Global Bit - Global Clock Output Enable
This bit overrides the individual CLKoutX_EN bits. When this bit is set to 0, all clock outputs are disabled, regardless of the state of any of the other bits or pins.

CLKin_SELECT Bit - Device CLKin Select
This bit determines which CLKin pin is used.

CLKin bit	Mode
0	CLKin1
1	CLKin0

Table 7: LMK01020 Internal Register R14 CLKin_SELECT

2.1.3 FastLink Register DAC7512

This chapter is a summary and contains information from the Burr-Brown datasheet [8]. For more information please refer to the schematic [2] of the ADC16HL and the relevant datasheets.

The ADC16HL mezzanine uses, for each of the six ADCs, a separate offset compensation circuitry. The core feature of this circuitry is a DAC which sets the offset voltage to a chosen value.

The DAC7512 is a single, 12-bit buffered voltage output Digital-to-Analog Converter (DAC). Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC7512 uses a versatile three-wire serial interface.

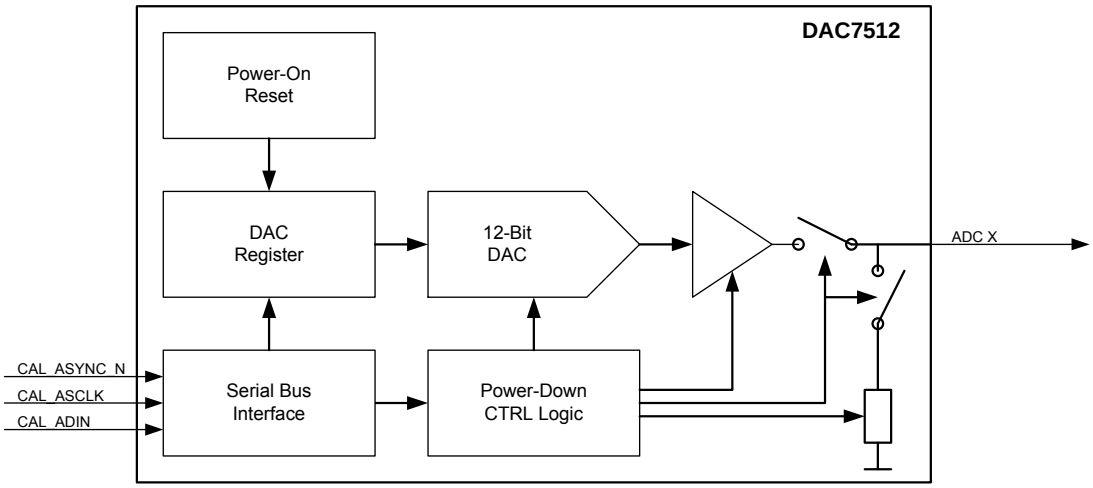

Figure 8: DAC7512 Block Diagram and Interface

On the ADC16HL board the SPI interface of the DACs are connected to the FPGA.

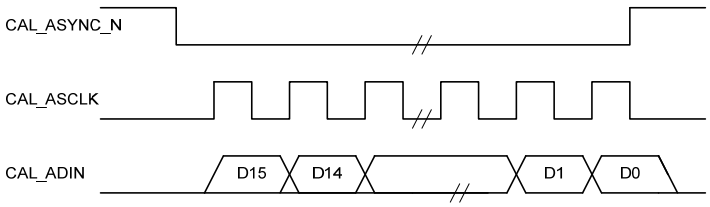

Figure 9: DAC7512 SPI Frame

The frame is sent as soon as a new value is written to the particular FastLink register:

Address	R/W	Bit	Name	Description
0x0008	W	11:0	DAC7512_0_D	Vout = VDD•D/4096
		13:12	DAC7512_0_CRTL	“00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z
0x0009	W	11:0	DAC7512_1_D	Vout = VDD•D/4096
		13:12	DAC7512_1_CRTL	“00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND

				“11” = Power down High-Z
0x000A	W	11:0	DAC7512_2_D	Vout = VDD•D/4096
		13:12	DAC7512_2_CRTL	“00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z
0x000B	W	11:0	DAC7512_3_D	Vout = VDD•D/4096
		13:12	DAC7512_3_CRTL	“00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z
0x000C	W	11:0	DAC7512_4_D	Vout = VDD•D/4096
		13:12	DAC7512_4_CRTL	“00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z
0x000D	W	11:0	DAC7512_5_D	Vout = VDD•D/4096
		13:12	DAC7512_5_CRTL	“00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z
0x000E	W	11:0	DAC7512_D	Vout = VDD•D/4096
		13:12	DAC7512_CRTL	“00” = Normal Operation “01” = Power down output 1 kΩ to GND “10” = Power down output 100 kΩ to GND “11” = Power down High-Z

Table 8: DAC7512 FastLink Register Map

Please note: The address 0x00E is a special case, because this address writes to all DACs simultaneously, e.g. allows you to set all DACs at the same time to the same value.

2.1.4 FastLink Register ADC16HL_CTRL and ADC16HL_STATUS

One of the FastLink registers allows the user to set particular bits directly for various purposes. Some of these bits have been documented in previous chapters.

Address	R/W	Bit	Name	Description
0x000F	W	0:5	ADC_PGA	Programmable gain amplifier control pin ‘0’ = Gain of 1, input range of 2.25 Vpp ‘1’ = Gain of 1.5, input range of 1.5 Vpp
	W	6	ADC_SHDN	Power shutdown pin ‘0’ = Normal operation ‘1’ = Chip powered down
	W	7	LMK_CTRL_SYNC	Global clock output synchronization pin ‘0’ = All divided clocks are set to logic low. ‘1’ = All divided clocks are activated and will transition to a high state simultaneously.
	W	8	LMK_CTRL_GOE	Global output enable pin ‘0’ = All the clock outputs are disabled. ‘1’ = All the clock outputs are enabled.
	W	11	SCK_OE_N	Local oscillator SL570 clock output enable '0' = clock disable '1' = clock enable
0x0015	R	0:5	ADC_PGA	Programmable gain amplifier control pin ‘0’ = Gain of 1, input range of 2.25 Vpp ‘1’ = Gain of 1.5, input range of 1.5 Vpp
	R	6	ADC_SHDN	Power shutdown pin ‘0’ = Normal operation ‘1’ = Chip powered down
	R	7	LMK_CTRL_SYNC	Global clock output synchronization pin ‘0’ = All divided clocks are set to logic low. ‘1’ = All divided clocks are activated and will transition to a high state simultaneously.
	R	8	LMK_CTRL_GOE	Global output enable pin ‘0’ = All the clock outputs are disabled. ‘1’ = All the clock outputs are enabled.
	R	11	SCK_OE_N	Local oscillator SL570 clock output enable '0' = clock disable '1' = clock enable
	R	13	ADC_PWR_GOOD	Power good indication from the ADC16HL card ‘0’ = Power failure on the card ‘1’ = Power ok
	R	15:14	SW2_1	Dipswitches SW2 and SW1 on the ADC16HL card

Table 9: ADC16HL_CTRL and ADC16HL_STATUS FastLink Register Map

2.1.5 FastLink Register LTC2448

This chapter is a summary and contains information from the Linear Technology datasheet [9]. For more information please refer to the schematic [2] of the ADC16HL and the relevant datasheets.

The ADC16HL mezzanine uses, for each of the six ADCs, a separate offset compensation circuit consisting of a ΔΣ ADC for measuring the necessary offset and through a DAC to adjust this offset.

The LTC2448 is an 8 channel differential high speed 24 bit “No Latency” ΔΣ ADC. This ADC uses a proprietary delta-sigma architecture enabling variable speed/resolution. This chip is configurable through a simple 4 wire serial interface.

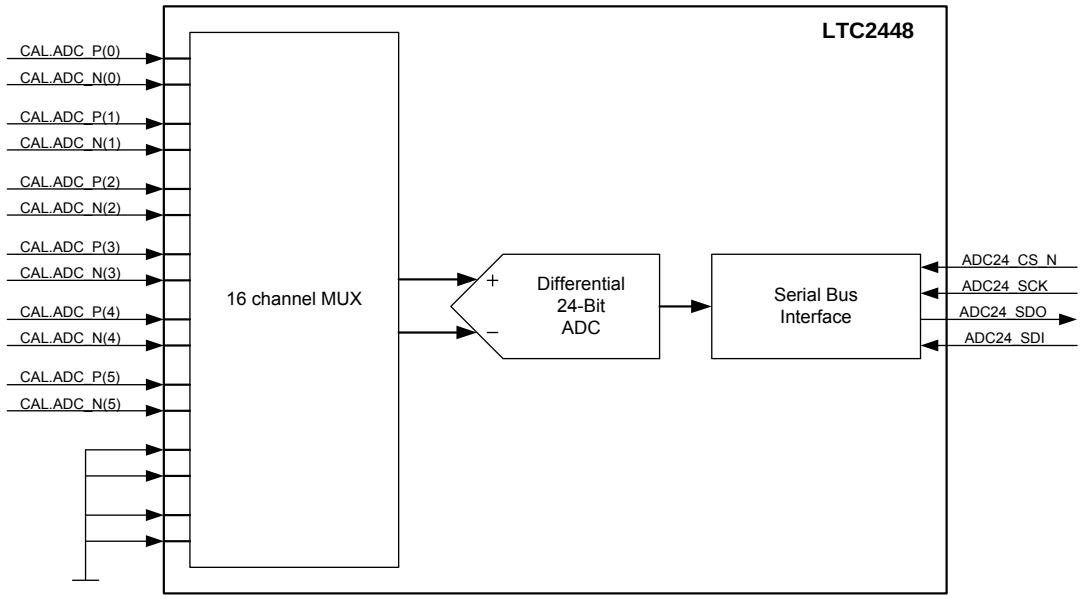

Figure 10: LTC2448 Block Diagram and Interface

Please note: The last two channels 6 and 7 are connected to GND and will not provide meaningful information.

On the ADC16HL board the SPI interface of the ADC is connected to the FPGA.

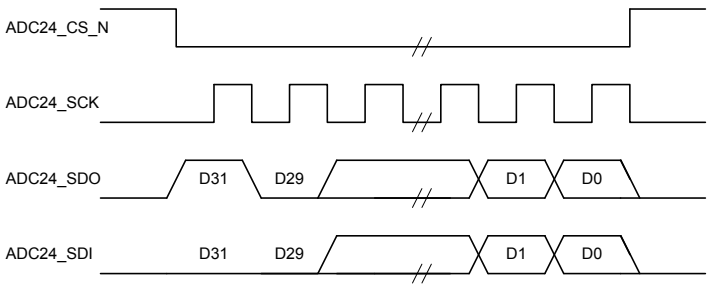

Figure 11: LTC2448 SPI Frame

The SPI frame is a 32 bit long serial stream starting with the MSB. Due to the nature of the FastLink of 16 bit data registers, two write accesses, first to the least significant 16 bits and then to the most significant 16 bits, have to be transmitted in order to start the SPI data frame from the ADC16HL FPGA to the registers in the chip.

Address	R/W	Bit	Name	Description
0x0010	W	15:0	LTC2448_LW_WR	LTC2448 ΔΣ ADCs chip least significant word (bits 15:0) for 32 bit SPI These bits are not relevant and shall be set to 0x0000
0x0011	W	15:0	LTC2448_HW_WR	LTC2448 ΔΣ ADCs chip most significant word (bits

				31:16) for 32 bit SPI Writing to this address triggers also the SPI link and the message is transmitted to the LTC2448 Bits 2:0 = Have to be “000” Bit 3 = TWOX : Two Times Oversampling [9] Bit 7:4 = OSR3 : OSR0 = Oversampling Sel [9] Bit 10:8 = A2:A0 = Channel to read Bit 11 = ODD = Has to be ‘0’ Bit 12 = SGL = Set to ‘0’ for diff. inputs Bit 13 = EN = Enable. Set to ‘1’ Bit 14 = ‘0’ Bit 15 = ‘1’
0x0012	R	15:0	LTC2448_LW_RD	LTC2448 ΔΣ ADCs chip least significant word (bits 15:0) from 32 bit SPI Bit 15:0: Least significant 16 bit of measurement
0x0013	R	15:0	LTC2448_HW_RD	LTC2448 ΔΣ ADCs chip most significant word (bits 31:16) for 32 bit SPI Bit 12:0: Most significant 13 bit of measurement Bit 13 = SIG = Sign Indicator Bit 14 = Always ‘0’ Bit 15 = EOC = End of Conversion

Table 10: LTC2448 FastLink Register Map

2.1.6 FastLink Register ADC16HL_FW

This register provides the application with the firmware version running on the ADC16HL board. This value is a constant.

Address	R/W	Bit	Name	Description
0x0014	R	15:0	ADC16HL_FW	The MSB denotes the major version number. The LSB denotes the minor version number.

Table 11: ADC16HL_FW FastLink Register Map

2.2 Performance

This chapter sums the tested static and dynamic requirements of the firmware. The chip used was a Spartan3 XC3S50AN-4 FPGA.

Features of the receiver design	
Max clock frequency	133 MHz
Flip Flop used	667
LUT used	738

Table 12: Design Features

2.3 Design constraints

None.

3 Appendix

None.