European XFEL Button BPM Manual

Revision 1.18
PSI, Villigen, 8.11.2016

Content

1 Introduction

The E-XFEL button BPM consists of a pickup with four button electrodes, EBRFFE front end, ADC12FL sampling board, the GPAC board, and additional boards (transition cards, EVR) supporting the application. The aim is to measure beam position and charge bunch-by-bunch. The system measures intensity of the four button pulses and calculates the position with low latency in a Virtex-5 FXT FPGA.

1.1 Purpose

The aim of this document is to provide a global overview of the measurement technique and to describe the user interface to the BPM FPGAs on the GPAC.

1.2 Scope

This document provides a global overview of the button BPM system and specifies the user interface. This document is a starting point which links to the detail information in the implementation in hardware, firmware and/or software.

1.3 History

Revision	Date	Author	Description
1.0	01.04.2014	W. Koprek	First version which only contains general overview and description of the interface to control system.
1.1	17.06.2014	W. Koprek	Re-arranged address space.
1.2	16.07.2014	W. Koprek	Added byte/bit convention. Changed bit arrangement in Table 3 at address 0x400
1.3	18.07.2014	W. Koprek	Added Table 7 describing CFG_FPGA Fixed bug in table 6. Address 0x00000000 changed to 0x00000220
1.4	11.11.2014	W. Koprek	Several changes in addresses. Added automatic gain control parameters. Moved ADC waveforms to BRAM. Moved position and charge readout to QDR2. Added valid measurement vector.
1.5	19.11.2014	W. Koprek	• Added minimum charge for filtering position data without beam. • Added description for fields 400 and 401 Modification marked in blue.
1.6	28.11.2014	W. Koprek	Added functional description of the amplitude calculation.
1.7	03.03.2015	W. Koprek	Modified parameters for amplitude calculation. Modified parameters for trigger settings. Modified parameters for position calculation.
1.8	03.03.2015	W. Koprek	Updated screen shots and field numbers

1.9	06.06.2015	W. Koprek	Few addresses have changed. They are marked in blue.
1.10	09.06.2015	W. Koprek	Corrected wrong addresses
1.11	16.06.2015	W. Koprek	Missing addresses added for mean and std readout.
1.12	13.07.2015	W. Koprek	Added software version to BPM FPGA
1.13	18.11.2015	W. Koprek	Added Save/Restore register description
1.14	27.11.2015	W. Koprek	Fixed addresses for statistics configuration
1.15	17.03.2016	W. Koprek	Fixed documentation error of base line correction enable address
1.16	18.03.2016	W. Koprek	Fixed typos in valid word description
1.17	15.04.2016	W. Koprek	Added relative charge threshold
1.18	08.11.2016	W. Koprek	Added status registers in SYS FPGA. Table 4.8.

1.4 Firmware and Software Version

This document is valid for the firmware and software version presented in the screen shot in Fig 1.1.

Firmware/Software

CF Card Present

FPGA	Conf	Version	Firmware	Software
CFG	Yes	0x2104006e	2015.04.17 15:22	2015.02.24 08:46
SEU	No			
SYS	Yes	0x2105000d	2015.04.16 14:50	2015.04.30 09:59
BP	Yes	0x2102004a	2015.04.24 16:38	2015.04.28 14:49
BPM1	Yes	0x2103003c	2015.05.29 10:16	2015.05.27 10:21
BPM2	Yes	0x2103003c	2015.05.20 21:53	2015.05.20 22:20

Figure 1.1. Screen shot of the EPICS panel with firmware and software version.

1.5 Definitions, acronyms, and abbreviations

This document is based on the “IEEE Recommended Practice for Software Requirements Specifications” [1].

ADC	Analog Digital Converter.
BPM	Beam Position Monitor. Usually measures the transversal beam bunch position and the bunch charge.
CORDIC	COordinate Rotation DIgital Computer), Aka Volder's algorithm is an algorithm used to translate Cartesian (x, y) to polar (amplitude, phase) coordinate systems.
EBRFFE	European Button BPM RF Front End
EVR	EVent Receiver. Decoder of the Event Link at PSI. This is a standard PSI VME card used to decode event link messages for trigger generation.
FPGA	Field Programmable Gate Array. Programmable logic device.
I2C	see IIC
IIC	IIC or I²C (Inter Integrated Circuit bus) is a multi-master serial bus defined / specified by Philips.
MPLB	PLB Master
PLB	IBM Processor Local Bus
PPC	PowerPC (Performance optimization with enhanced

	risc Performance Computing) is a RISC architecture created by an alliance of big companies Apple/IBM/Motorola.
Reg	Register. Mathematically z^-1
RTM	Rear transition card. Sometimes called “Transition Card”
SFP	Small form-Factor Pluggable is a compact, hot-pluggable multi-gigabit optical or/and electrical transceiver interface.
SPLB	PLB Slave

2 System Overview

Figure 1 illustrates the instance of one Button BPM system for European XFEL. One system consists of one MBU which contains four RFFEs and one GPAC board with two 12-bit ADC mezzanine cards. One Button BPM system can be connected to four BPMs.

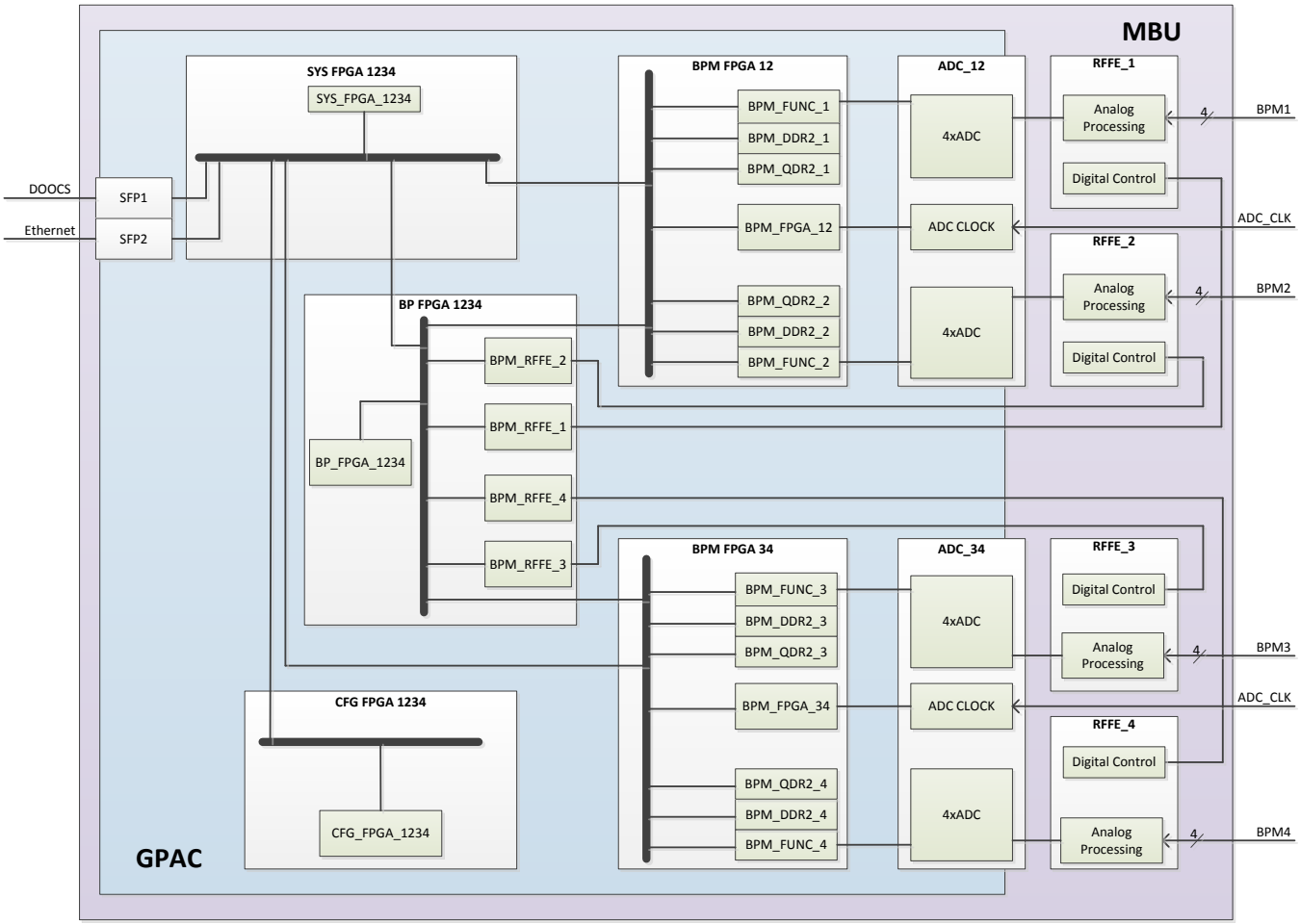


Figure 2.1: Button BPM System Overview

Each button BPM (BPM1/BPM2/BPM3/BPM4) consists of four buttons. Each button is connected to RFFE with an RF cable; hence each RFFE has four RF inputs. The RFFE contains peak detector for each channel. Then the output signals of the RFFEs are connected to ADCs. The GPAC board is equipped with two ADC mezzanine cards ADC12FL. Each ADC card contains eight 12-bit ADCs which can run with sampling frequency up to 500MHz. Each

ADC mezzanine is connected to two RFFEs. The ADC clock can be delivered from the machine using SMA connector on the front panel of the ADC, or it can run with local, free running 500MHz oscillator. The digital outputs from ADCs are connected to BPM FPGAs (BPM FPGA 12, BPM FPGA 34) for digital processing. The FPGA firmware calculates from sampled signals the amplitude for each channel and then position and charge in physical units. The calculated position and charge, as well as raw ADC samples can be transferred over SYS FPGA to control system. The GPAC board contains two SFPs on the front panel which are used to connect the control system. Both SFPs have symmetric interface which means that one can connect in parallel two control systems, e.g. DOOCS for regular operation and Ethernet for monitoring and maintenance.

3 Firmware and Embedded Software

3.1 BPM FPGA Firmware

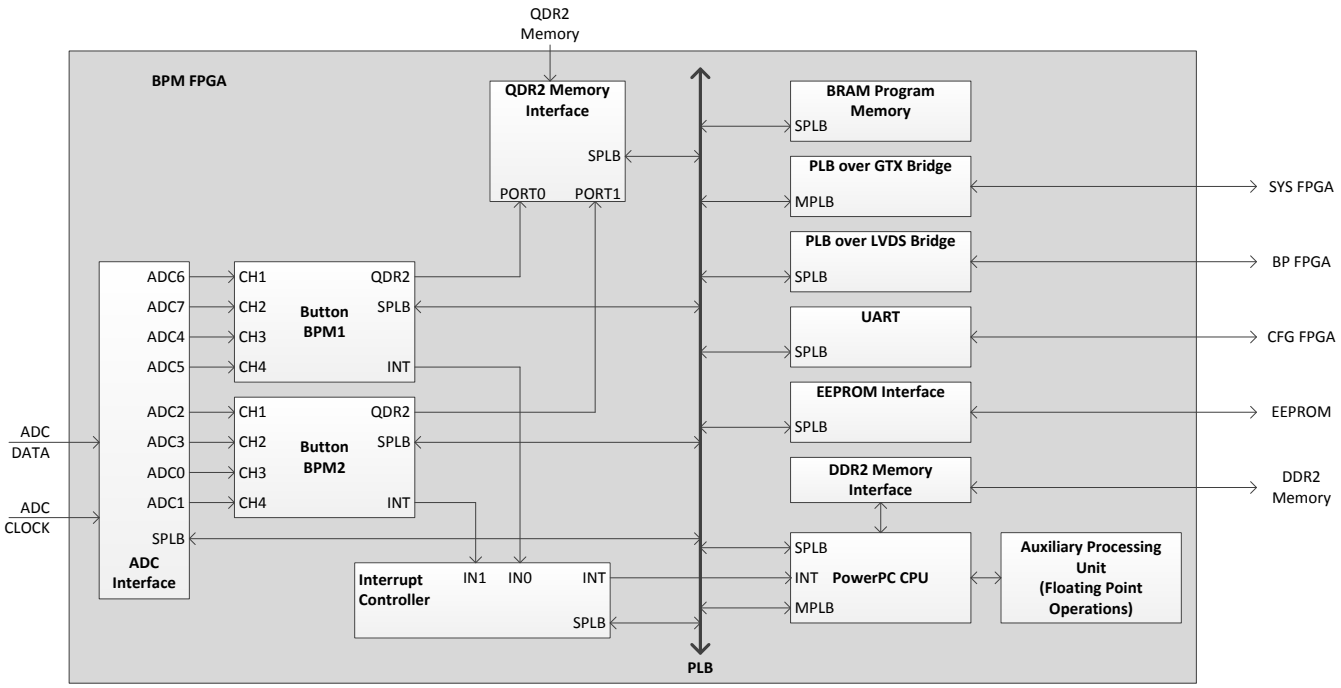


Figure 3.1. BPM FPGA Firmware Block Diagram

3.2 BP FPGA Firmware

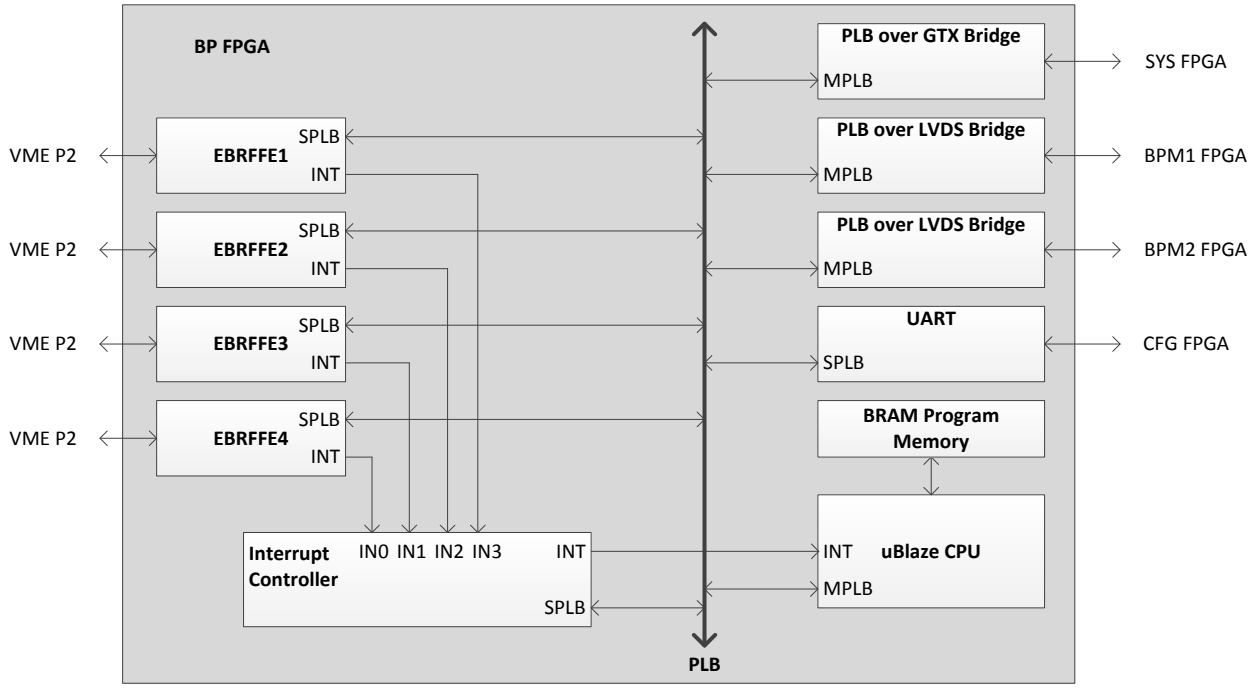


Figure 3.2. BP FPGA Firmware Block Diagram

3.3 Button BPM Component

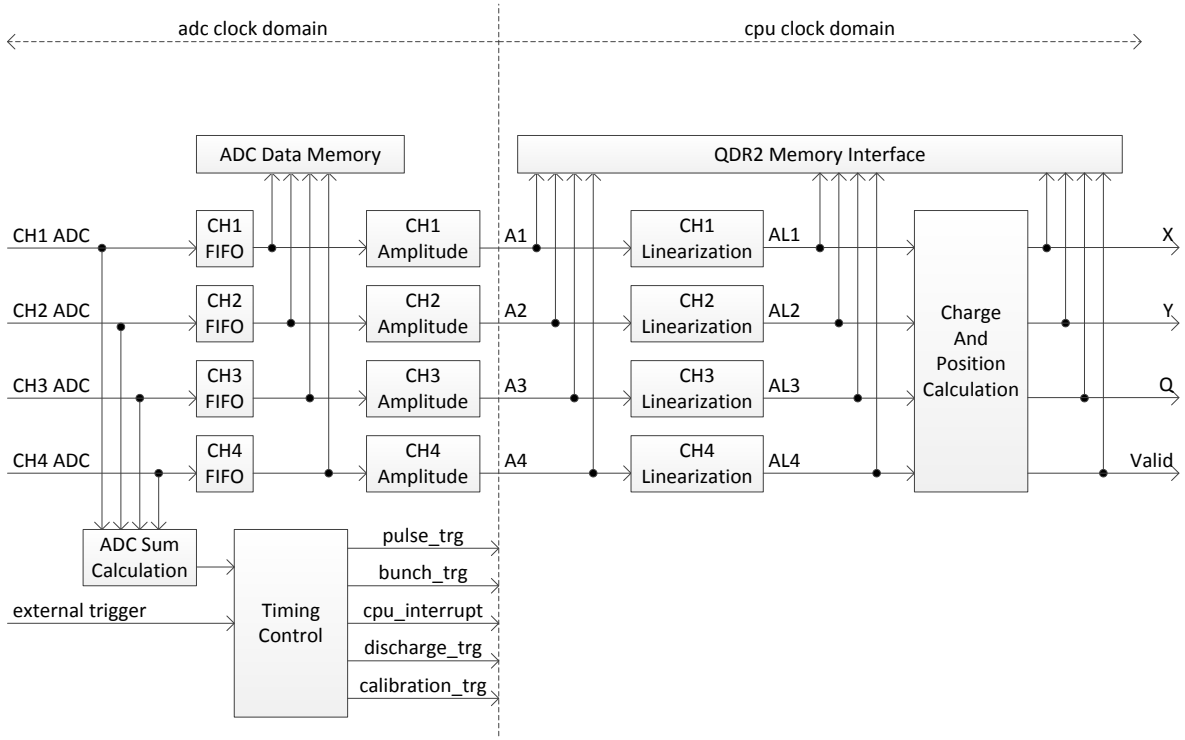


Figure 3.2. Block diagram of Button BPM Component

3.4 Timing Control

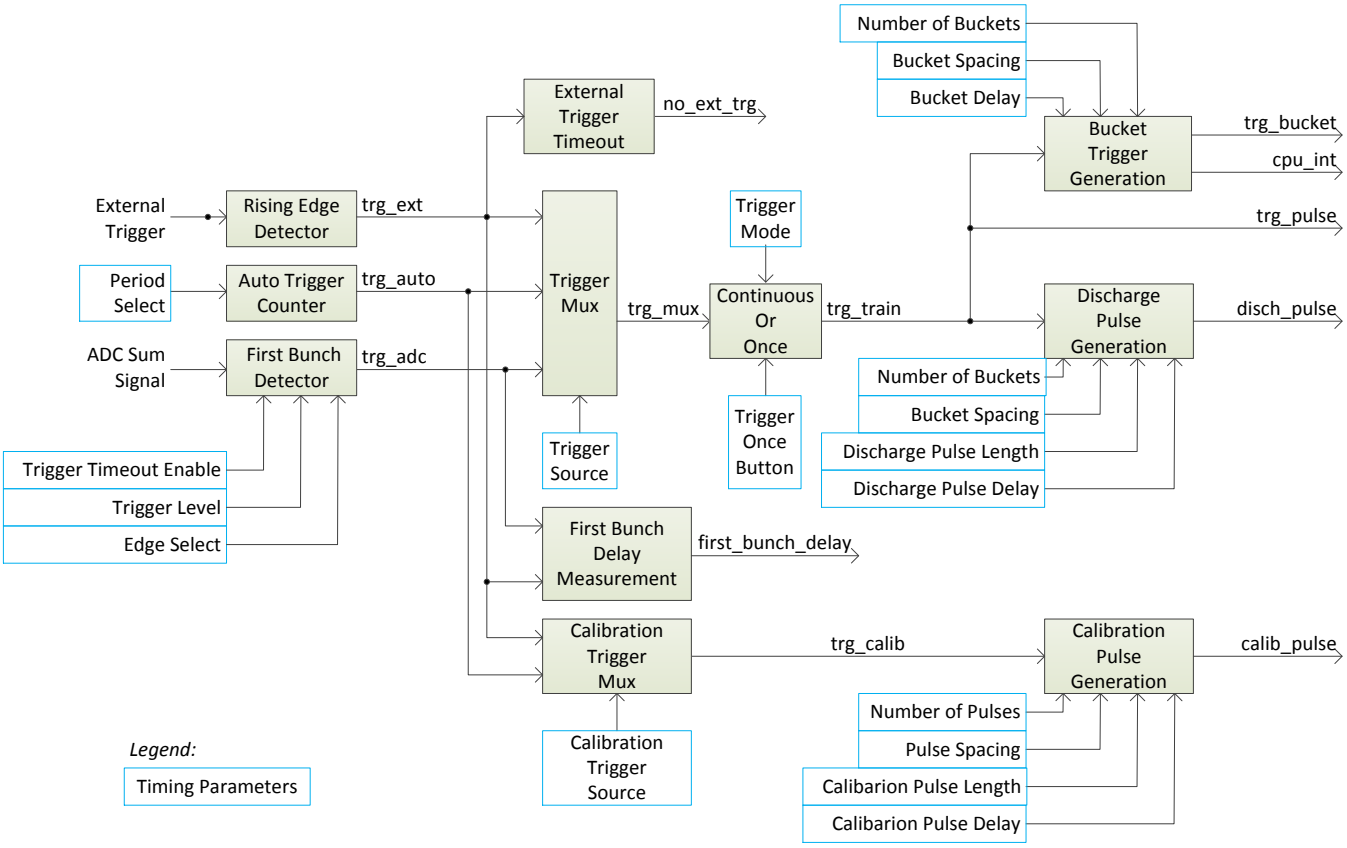


Figure 3.3. Timing Control Component Block Diagram

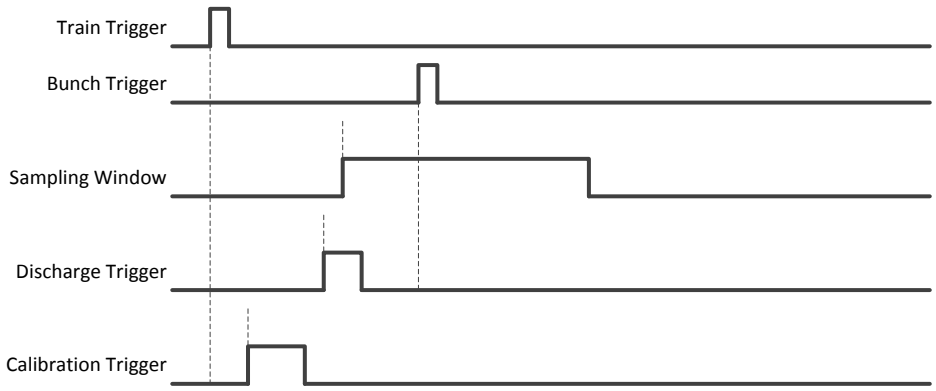


Figure 3.4. Timing Diagram of the Button BPM Component

3.5 Amplitude Calculation

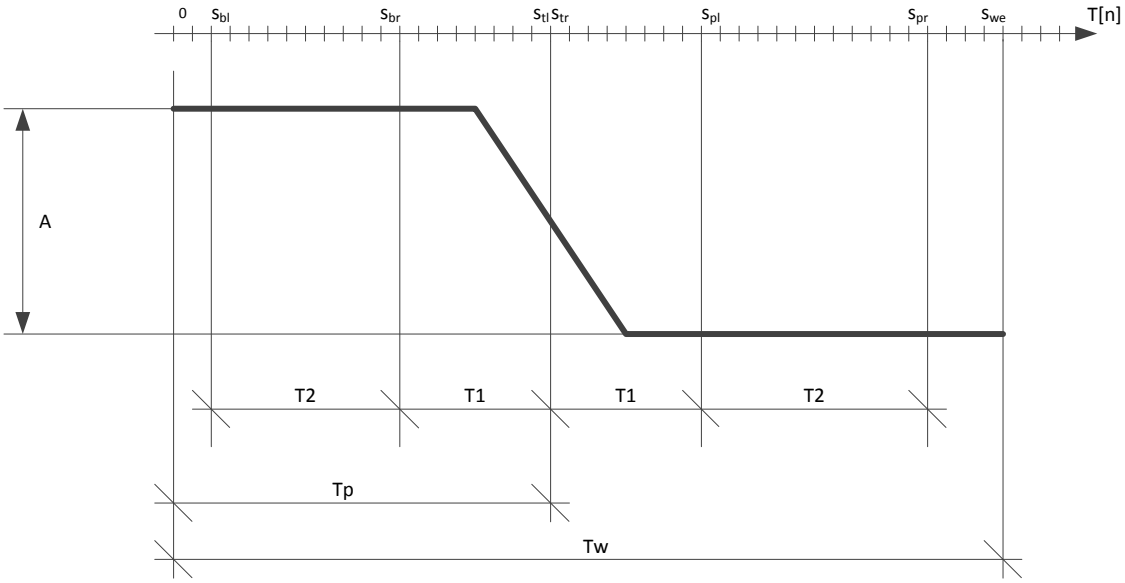


Figure 3.5. Concept of the pulse amplitude calculation

3.5.1 Units

'T' parameters are measured in clock cycles [clk cycle] of the FPGA computation pipeline
's' parameters are measured in sample number [n]
The relation between the two units is:

[clk cycle] = 2 * [n]

3.5.2 Definition of the User Parameters

T_w – sampling window length
T_p – number of samples before the trigger
T_1 – distance from the trigger sample to averaging windows
T_2 – length of the averaging windows

3.5.3 Calculation of the Firmware Parameters

Sample number to the left of the bunch trigger

$s_{tl} = 2*T_p - 1$

Sample number to the left of the bunch trigger

$s_{tr} = 2*T_p$

First sample of the base line averaging window

$s_{bl} = 2 * T_p - 2 * T_1 - 2 * T_2$

Last sample of the base line averaging window

$s_{br} = 2 * T_p – 2 * T_1 - 1$

First sample of the pulse averaging window

$s_{pl} = 2 * T_p + 2 * T_1$

Last sample of the pulse averaging window

$s_{pr} = 2 * T_p + 2 * T_1 + 2 * T_2 - 1$

Last sample of the sampling window

$s_{we} = 2 * T_w – 1$

3.5.4 Amplitude calculation

The amplitude is calculated in firmware based on the formula 1.

$$A = \frac{1}{s_{br}-s_{bl}} \sum_{k=s_{bl}}^{s_{br}} s_k - \frac{1}{s_{pr}-s_{pl}} \sum_{k=s_{pl}}^{s_{pr}} s_k \qquad (1)$$

3.5.5 Parameter rules

After calculation of the ‘s’ parameters, the settings rules are checked. The following rules are checked:

- $s_{bl} >= 0$
- $s_{br} – s_{bl} = T_2 – 1 > 0$
- $s_{pr} – s_{pl} = T_2 – 1 > 0$
- $s_{pr} <= s_{we}$

If one of the above rules is not fulfilled, the software sets default parameters as follows:

- $s_{bl} = 0$
- $s_{br} = 1$
- $s_{pl} = 2$
- $s_{pr} = 3$

The default parameters are kept as long as the user provides the valid ‘T’ parameters.

3.6 RFFE Input Voltage Detection

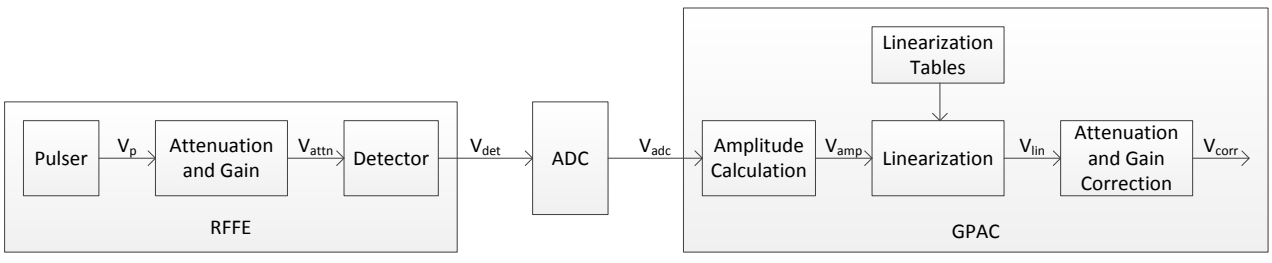


Figure 3.6. Block diagram of processing chain for RFFE input voltage detection

The on board pulser is used to generate calibration pulses with constant amplitude which emulate real beam induced pulses coming from BPM pickup. The pulser signal V_p cannot be measured directly by the firmware and its voltage is not known. But it is assumed that V_p is constant during single characterization procedure and its voltage is normalized to 1.
The pulser signal is attenuated and amplified. Its level V_{attn} depends on the settings of the attenuators and number of amplifiers it goes through. In case of the calibration procedure none of the amplifiers is used and the attenuation is changed from maximum to zero. Therefore V_{attn} is a function of attenuator settings in range from 0 dB to 31.5 dB, as presented in figure 3.7 and it calculated with formula

$$V_{attn} = V_p * 10^{\frac{Attn}{20}} \quad \text{where } V_p = 1\,V \qquad (3.1)$$

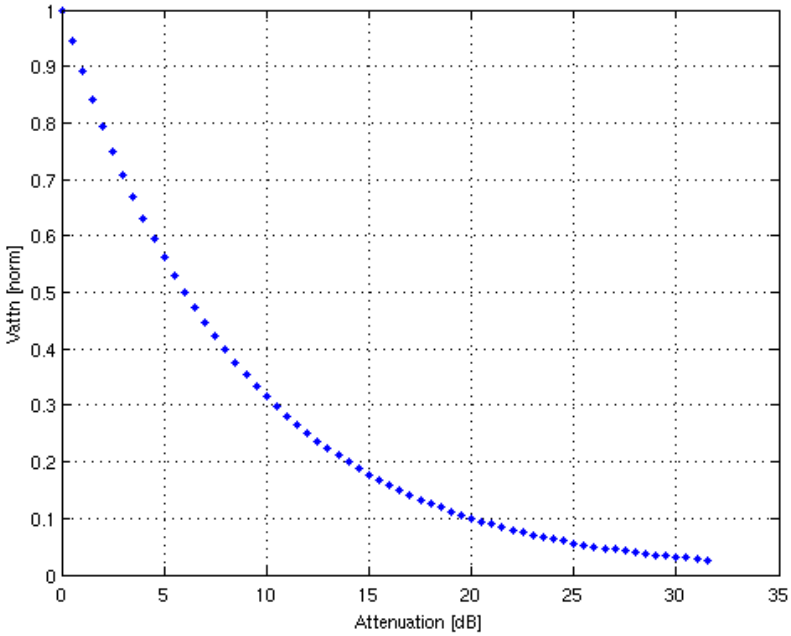


Figure 3.123. Attenuator output vs. attenuation set value.

The RFFE detector characterization procedure is done iteratively by changing the attenuation settings and reading the pulse amplitude V_{amp}. The scan procedure is presented in figure 3.123. The number of steps S is constant and it is equal to 64 steps of the attenuators. The number of iteration per step I is configurable and it is used to measure amplitude several times for the same attenuation settings. The software calculates average value of the I measurements in order to filter out random perturbations. The whole procedure is executed once for all four channels.

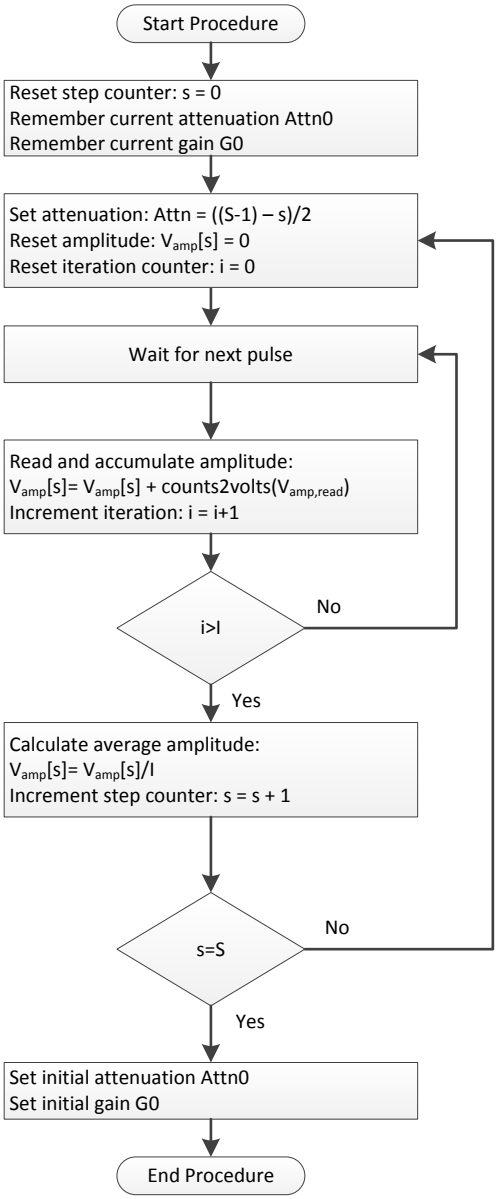


Figure 3.123. RFFE detector scan algorithm

The figure 3.124 presents an example result of the scan procedure.

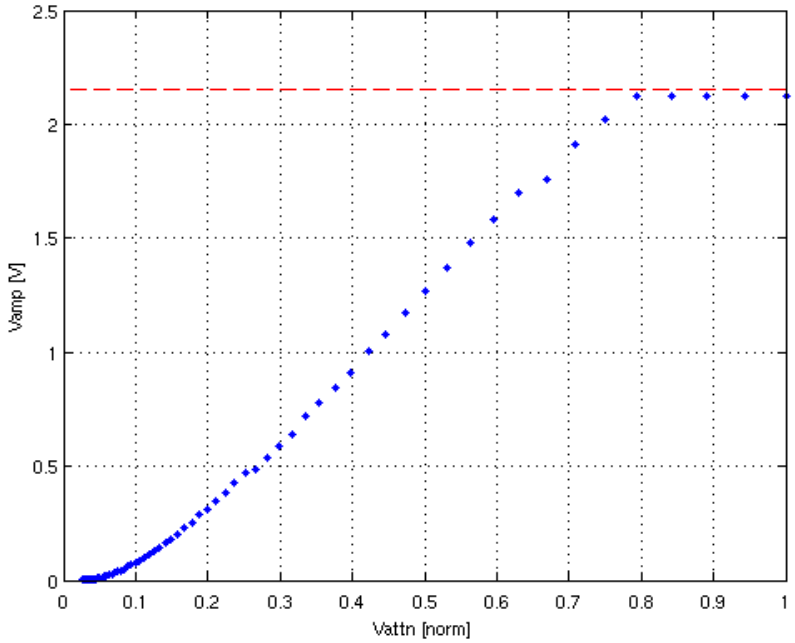


Figure 3.7. Scan result of the RFFE detector

The V_{amp} is the pulse amplitude calculated in FPGA from ADC signal (see section 3.5). This voltage is represented in FPGA as integer number $V_{amp,fpga}$ in range <0; 4095>, where number 0 corresponds to 0 V amplitude and 4095 corresponds to V_{adcmax} = 2.15 V amplitude (the red dashed line in figure 3.7). The V_{adcmax} is taken from a data sheet of the used ADC. The amplitude of V_{amp} = 2.15 V (can be reached when the base line of the RFFE detector is set to maximum voltage of the ADC which is $V_{adc,max}/2$. The $V_{amp,fpga}$ numbers are scaled to voltage with the formula

$$V_{amp} = V_{adcmax} * \frac{V_{amp,fpga}}{4095} \qquad (3.2)$$

In the next step the fit procedure is executed to find coefficients of the theoretical curve which matches best the measured V_{amp} curve. The goal of the fitting procedure is to find with given precision the coefficients a, b, c of the theoretical curve given by formula

$$V_{amp} = \sqrt[c]{a^c + (b * V_{attn})^c} - a \qquad (3.3)$$

The fitting algorithm is presented in figure 3.8. In the first step the coefficient table Tcoeff is initialized with default initial parameters

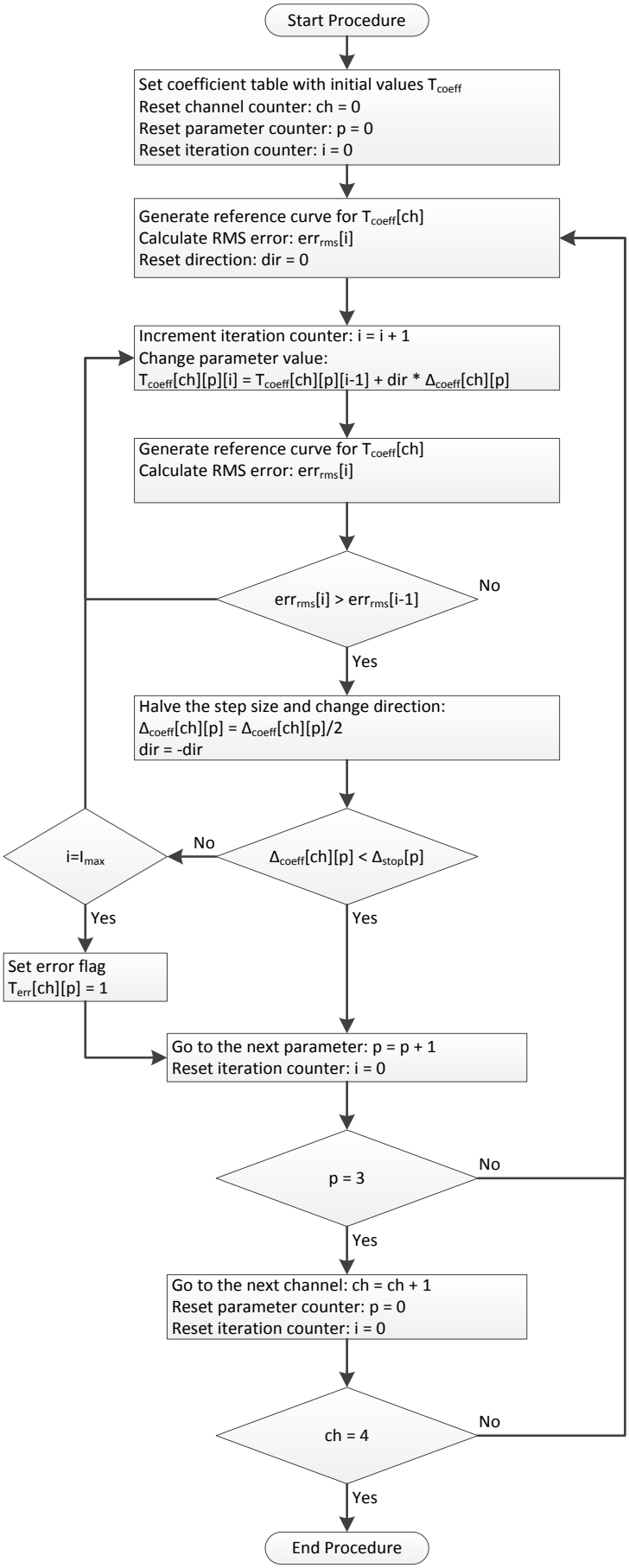
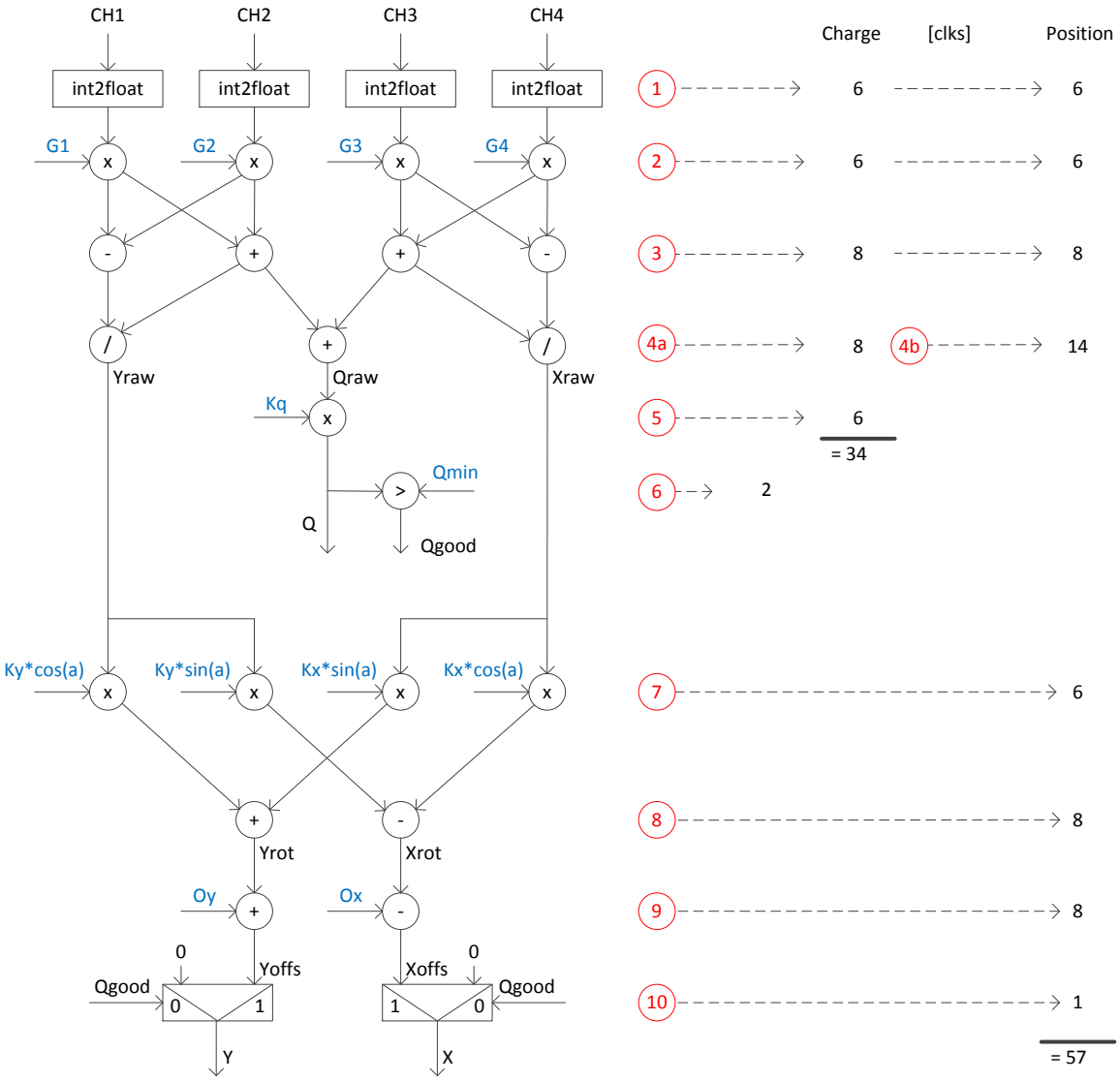


Figure 3.8. Fitting algorithm

3.7 Position calculation

Firmware implementation



Computation pipeline steps.

1. Conversion from unsigned integer to floating point number single precision.

3.8 Invalid measurement indication

3.8.1 Indication of invalid measurement of a single bunch

Each set of measurements (X, Y, Q) for each bunch has a corresponding valid vector. This is a 32-bit unsigned integer number. When the measurement is valid this number is zero. When

value is non zero the individual bits indicate reason(s) of the invalid measurement. The table 3.XX shows definition of the invalid vector bits.

Bit	Definition
0	Amplitude calculation error for channel 1
1	ADC min saturation for channel 1
2	ADC max saturation for channel 1
3	Base line out of range for channel 1
4	Reserved for channel 1
5	Reserved for channel 1
6	Amplitude calculation error for channel 2
7	ADC min saturation for channel 2
8	ADC max saturation for channel 2
9	Base line out of range for channel 2
10	Reserved for channel 2
11	Reserved for channel 2
12	Amplitude calculation error for channel 3
13	ADC min saturation for channel 3
14	ADC max saturation for channel 3
15	Base line out of range for channel 3
16	Reserved for channel 3
17	Reserved for channel 3
18	Amplitude calculation error for channel 4
19	ADC min saturation for channel 4
20	ADC max saturation for channel 4
21	Base line out of range for channel 4
22	Reserved for channel 4
23	Reserved for channel 4
24	Charge too small for position calculation
25	RFFE in calibration mode
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

Bits definition:

- Bits 0, 6, 12, 18 – amplitude calculation error. This error occurs when the settings of the amplitude calculation windows are invalid with respect to the sampling window size. Usually when the amplitude calculation sample indices exceed the sampling window length.
- 1, 7, 13, 19 – ADC min saturation. This error is set when one of the ADC samples used for amplitude calculation was in saturation. The saturation occurs when the ADC sample has value of -2048.
- 2, 8, 14, 20 – ADC max saturation. This error is set when one of the ADC samples used for amplitude calculation was in saturation. The saturation occurs when the ADC sample has value of +2047.

- 3, 8, 15, 21 – base line out of range. This happens when at least one sample used for base line calculation was out of the specified range in the base line feedback. This check is also done when the base line feedback is off.
- 24 – charge too small. When the charge measurement is below threshold given by the user, then the position values are set to 0. In this case this bit indicates such situation.
- 25 – rffe in calibration mode. This bit is set when the inputs of the RFFE are set to calibration mode. The device still measures charge and position, but this are not the beam properties.

3.8.2 Indication of invalid measurement of a bunch train

There is also a single register showing invalid measurement of the whole bunch train. The register has the same content as for individual bunches, but each bit is an OR function of the corresponding bit for each bunch in the train. The bit set to '1' indicates that at least one bunch in the train had the corresponding flag invalid.

3.8.3 Statistics

The statistics for Button BPM are calculated from pulse to pulse. The calculations are performed in PowerPC after each pulse. The statistics are calculated for position X and Y, charge, and channel amplitudes A1, A2, A3, and A4. The screenshot in Figure 3.XX presents the statistics table.

Statistics

Bucket select: 1 | Statistice length: 100 | Stat reset

	Single	Mean	Std Dev	Min	Max	p-p
X [mm]	-1.8843	-1.8443	0.0181	-1.9130	-1.7741	0.1389
Y [mm]	-0.5184	-0.5231	0.0039	-0.5371	-0.5057	0.0314
Q [pC]	412.5	417.8	2.2	409.9	426.6	16.8
A1	2136	2182	19	2112	2259	147
A2	2336	2387	21	2311	2471	160
A3	2428	2481	21	2402	2567	165
A4	3297	3345	19	3277	3421	144

Figure 3.XX Statistics table

The following parameters can be set by the user to calculate the statistics:

- 'Bucket select' – selects the bucket from 1 to 2700 - called later N bucket.
- 'Statistics length' – number of recent pulses from 1 to 511 used to calculate statistics - called later M.
- 'Stat reset' – the button is used to reset the statistics

The following values are calculated:

- 'Single' – single value from last pulse of the N-th bucket.
- 'Mean' – mean value of last M pulses for the N-th bucket.
- 'Std Dev' – standard deviation of last M pulses for the N-th bucket.
- 'Min' – minimum of the 'Single' value calculate from last 'Stat reset'

- ‘Max’ – maximum of the ‘Single’ value calculate from last ‘Stat reset’
- ‘p-p’ – pick-to-pick is the difference of ‘Max’ and ‘Min’ values

Control System Interface

The user has full access to all registers by means of a simple address map (in contrast to systems which run function code). The PLB is a multi-master system providing read and write access to more than one control unit. The PLB components are burst enabled hence chunks of data can be read (e.g. DMA access) in order to achieve a high data throughput in a system.

The address space of one GPAC for Button BPM system has size of 64MB. Table 1 presents arrangement of the address space inside GPAC. The Class names in the table have corresponding instances in Figure 1 represented as firmware blocks.

Table 4.1: Address space of one GPAC board.

Structure			Class	Start Address	End Address	Size [B]	Details
BPM1234 1xMBU (32MB)	Common for BPM1234		SYS_FPGA	0x00000000	0x000000FF	256	Table 4.8
			CFG_FPGA	0x00003000	0x00003FFF	4k	Table 4.7
			BP_FPGA	0x00100000	0x001000FF	256	Table 4.9
	BPM12	Common for BPM12	BPM_FPGA	0x00A00000	0x00A00FFF	4k	Table 4.2
		BPM1	BPM_EEPROM	0x00A04000	0x00A05FFF	8k	Table 4.7
			BPM_FUNC	0x00A10000	0x00A13FFF	16k	Table 4.3
			BPM_DDR2	0x00900000	0x008FFFFF	512k	Table 4.5
			BPM_QDR2	0x00B00000	0x00B7FFFF	512k	Table 4.4
			BPM_RFFE	0x00101000	0x00101FFF	4k	Table 4.6
		BPM2	BPM_EEPROM	0x00A06000	0x00A07FFF	8k	Table 4.7
			BPM_FUNC	0x00A20000	0x00A23FFF	16k	Table 4.3
			BPM_DDR2	0x00980000	0x009FFFFF	512k	Table 4.5
			BPM_QDR2	0x00B80000	0x00BFFFFF	512k	Table 4.4
			BPM_RFFE	0x00102000	0x00102FFF	4k	Table 4.6
	BPM34	Common for BPM34	BPM_FPGA	0x01200000	0x01200FFF	4k	Table 4.2
		BPM3	BPM_EEPROM	0x01204000	0x01205FFF	8k	Table 4.7
			BPM_FUNC	0x01210000	0x01213FFF	16k	Table 4.3
			BPM_DDR2	0x01100000	0x010FFFFF	512k	Table 4.5
			BPM_QDR2	0x01300000	0x0137FFFF	512k	Table 4.4
			BPM_RFFE	0x00103000	0x00103FFF	4k	Table 4.6
		BPM4	BPM_EEPROM	0x01206000	0x01206FFF	8k	Table 4.7
			BPM_FUNC	0x01220000	0x01223FFF	16k	Table 4.3
			BPM_DDR2	0x01180000	0x011FFFFF	512k	Table 4.5
			BPM_QDR2	0x01380000	0x013FFFFF	512k	Table 4.4
			BPM_RFFE	0x00104000	0x00104FFF	4k	Table 4.6

The address space consists of one common area (blue in Table 1) for all four BPMs. This common area contains registers for CFG FPGA, SYS FPGA, and BP FPGA. Then the rest of address space is split into two parts for BPM FPGA 12 and BPM FPGA 34. And again the BPM FPGA address space contains common part for two BPMs (BPM_FPGA) and then dedicated components for each BPM separately (BPM_FUNC, BPM_DDR2, BPM_QDR2, BPM_RFFE). Each class instance has start and end address in the 64MB address space. The last column contains reference to a table or a document which describes in details registers content of each component.

3.9 Convention

Figure 2 present byte and bit ordering used in this documentation.

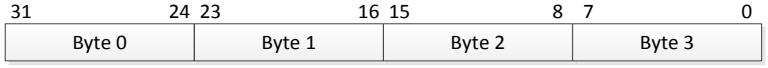


Figure 4.1. Byte and bit convention

3.10 Registers content description

The registers description in the following tables contains addresses relative to the base address of the class instance listed in Table 1. The second column contains data type of the register in firmware. The data type of the register on the control panel can be different then in firmware. Usually the integer register is represented as a float number on the control panel. In this case the description field contains scaling factor and/or offset for value conversion in control system. The last column contains reference number to control panel from EPICS. Screenshots of the EPICS control panels are in Appendix 4.1.

Table 4.2: Register description of BPM_FPGA class.

Class: BPM_FPGA				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x00000000	uint32	RO	BPM FPGA firmware version	500
0x00000004	uint32	RO	BPM FPGA firmware compilation year	501
0x00000008	uint32	RO	BPM FPGA firmware compilation month	501
0x0000000C	uint32	RO	BPM FPGA firmware compilation day	501
0x00000010	uint32	RO	BPM FPGA firmware compilation hour	501
0x00000014	uint32	RO	BPM FPGA firmware compilation minute	501
0x00000018	uint32	RO	BPM FPGA software compilation year	501
0x0000001C	uint32	RO	BPM FPGA software compilation month	501
0x00000020	uint32	RO	BPM FPGA software compilation day	501
0x00000024	uint32	RO	BPM FPGA software compilation hour	501
0x00000028	uint32	RO	BPM FPGA software compilation minute	501
0x00000201	uint8	RW	Selects which clock delivered from ADC mezzanine is used in BPM FPGA: 0 – clock from splitter output 3 1 – clock from PLL	239
0x00000203	uint8	RO	Lock status of the PLL in BPM FPGA: 0 – PLL not locked 1 – PLL locked	207
0x00000880	uint32	RW	Configuration of the clock in ADC card: 0 – [MO:216.6->433.3] External clock. Predefined settings. A 216MHz machine clock should be connected to SMA input on the ADC card. The PLL produces 433.3 MHz for the ADCs. 1 – [LO:500.0->433.3] Internal clock. Predefined settings. A 500MHz local oscillator is used for clock generation. The PLL synthesizes 433.3 MHz for the ADCs. 2 – [LO:500.0->500.0] Internal clock with no frequency synthesis. The PLL repeats the 500 MHz for the ADCs. 3 – Custom. Any other setting than predefined for External/Internal. It switches automatically to this mode whenever predefined settings are altered by the user.	107

Table 4.3: Registers description of BPM_FUNC class.

Class: BPM_FUNC				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x00000000	uint32	WO	Manual trigger of BPM. Writing anything to this address triggers once the BPM.	127
0x00000404	uint8	RW	Trigger source: 0 – Signal 1 – Machine trigger 2 – Auto trigger (2 s) 3 – Auto trigger (1 s) 4 – Auto trigger (0.5 s) 5 – Auto trigger (0.2 s) 6 – Auto trigger (0.1 s)	100
0x00000405	uint8	RW	Trigger mode: 0 – Continuous 1 – Single	101
0x00000406	uint8	RW	Bunch trigger edge: 0 – negative 1 – positive	106
0x00000407	uint8	RW	RFFE triggers crossing: 0 – crossed 1 – straight	123
0x00000408	uint16	RW	Number of ADC samples before bunch trigger	110
0x0000040A	uint16	RW	Number of ADC samples per one bunch	111
0x0000040C	uint32	RW	Delay of the first bunch with respect to the pulse trigger. Measured in clock cycles.	109
0x00000410	uint16	RW	Number of buckets. Now has to be set manually. Later the value comes from timing system.	112
0x00000412	uint16	RW	Bucket spacing in ADC clock cycles. Now has to be set manually. Later the value comes from the timing system.	116
0x00000414	uint16	RW	Length of the RFFE calibration pulse. Measured in clock cycles	126
0x00000416	uint16	RW	Length of the RFFE discharge pulse. Measured in clock cycles	115
0x00000418	int16	RW	Bunch trigger level in range from -8192 to 8192	105
0x0000041A	uint8	RW	Enable RFFE detector discharge trigger: 0 – off 1 – on	122
0x0000041B	uint8	RW	Enable RFFE calibration pulse: 0 – off 1 – on	121
0x0000041C	int32	RW	RFFE discharge pulse delay measured in clock cycles.	114
0x00000424	uint16	RW	Amplitude T1 parameter	117
0x00000426	uint16	RW	Amplitude T2 parameter	119
0x00000428	float	RW	Roll angle for position calculation	429
0x0000042C	uint16	RW	Number of calibration pulses	130
0x0000042E	uint16	RW	Calibration pulse spacing. It is integer multiple of the bucket spacing. This number simulates bunch spacing in a real machine.	131
0x00000430	float	RO	Minimum charge allowed in [pC]	420
0x00000434	float	RW	Position factor Ky	421
0x00000438	uint32	RW	Enable linearization of the RFFE detector: 0 – Off 1 - On	402
0x00000438	int32	RW	Linearization enable: 0 - disabled 1 - enabled	401
0x0000043C	uint8	RW	Calibration source: 0 – Machine trigger 1 – Auto trigger (2 s) 2 – Auto trigger (1 s) 3 – Auto trigger (0.5 s) 4 – Auto trigger (0.2 s) 5 – Auto trigger (0.1 s)	120

0x0000043D	uint8	RW	Trigger timeout enable: 0 - disabled 1 - enabled	118
0x00000448	float	RW	Position factor Kx	422
0x0000044C	float	RW	Charge scaling factor Kq	423
0x00000450	uint16	RW	Pickup orientation: 0 – 0 degrees 1 – 45 degrees	424
0x00000464	uint32	RW	BPM EEPROM command. Writing a value triggers an action: 0 – do nothing 1 – sets whole EEPROM to default state, works only if the magic word has secret value, otherwise it does nothing 2 – saves all sets to EEPROM 3 – sets selected set as default 4 – loads selected set 5 – saves selected set to RAM 6 – sets default values for selected set	600
0x00000470	float	RW	Internal offset for X position	425
0x00000474	float	RW	Internal offset for Y position	426
0x00000478	float	RW	External offset for X position	427
0x0000047C	float	RW	External offset for Y position	428
0x00002000	int16	RO	Channel 1 ADC samples. This is a waveform of 256 elements.	125
0x00002800	int16	RO	Channel 2 ADC samples. This is a waveform of 256 elements.	125
0x00003000	int16	RO	Channel 3 ADC samples. This is a waveform of 256 elements.	125
0x00003800	int16	RO	Channel 4 ADC samples. This is a waveform of 256 elements.	125

Table 4.4: Register description of class BPM_QDR2.

Class: BPM_QDR2				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x00000000	single	RO	X position waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	408, 405
0x00004000	single	RO	Y position waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	409, 406
0x00008000	single	RO	Charge waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	410, 407
0x0000C000	single	RO	Valid word waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	
0x00010000	single	RO	CH1 amplitude waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	440
0x00014000	single	RO	CH2 amplitude waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	440
0x00018000	single	RO	CH3 amplitude waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	440
0x0001C000	single	RO	CH4 amplitude waveform. As many elements as buckets: 800 for FLASH 2700 for XFEL	440

Table 5. Register description of class BPM_DDR2.

Class: BPM_DDR2				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x0000002C	uint16	RO	Base line calculation start sample	140

0x0000002E	uint16	RO	Base line calculation stop sample	140
0x00000030	uint16	RO	Top calculation start sample	140
0x00000032	uint16	RO	Top calculation stop sample	140
0x00000034	uint16	RO	Trigger edge left sample	140
0x00000036	uint16	RO	Trigger edge right sample	140
0x00000300	int16	RW	Base line level set point. Value from -2048 to 2047	393
0x00000302	uint16	RW	Base line level threshold. Value from 0 to 1000..	395
0x00000306	uint8	RW	Base line correction enable 0 – disabled 1 – enabled	396
0x00000307	uint8	RW	Base line level time threshold. Range from 1 to 100.	395.1
0x00000308	uint32	RO	Base line status	395.2
0x00000400	uint32	RW	RFFE amplifiers temperature control enable 0 – disabled 1 - enabled	389
0x00000404	uint32	RO	RFFE amplifier temperature control status: Bit[0] – Channel 1 saturated Bit[1] – Channel 2 saturated Bit[2] – Channel 3 saturated Bit[3] – Channel 4 saturated	
0x00000408	single	RW	RFFE Amplifier 1 temperature set point	
0x0000040C	single	RW	RFFE Amplifier 1 temperature set point	
0x00000410	single	RW	RFFE Amplifier 1 temperature set point	
0x00000414	single	RW	RFFE Amplifier 1 temperature set point	
0x00000504	uint32	RW	Number of the select BPM EEPROM set	602
0x00000508	uint32	RW	Number of the actually used BPM EEPROM set	604
0x0000050C	char[32]	RW	Name of the BPM EEPROM selected set	603
0x00001000	uint8	RW	Automatic gain control enable 0 – disabled 1 – enabled	382
0x00001001	uint8	RW	Automatic gain control maximum amplitude in [%].	382.1
0x00001002	uint8	RW	Automatic gain control minimum amplitude in [%].	382.2
0x00001003	uint8	RW	Automatic gain control time threshold for minimum amplitude	382.3
0x00001004	uint8	RO	Automatic gain control status: Bit[0] – signal too big Bit[1] – signal too small Bit[2] – gain reduced Bit[3] – gain increased Bit[4] – Max gain reached Bit[5] – Min gain reached Bit[6] – RFFE error	382.1 0
0x00001005	uint8	RO	Actual amplitude level in [%] measured by AGC	382.8
0x00001008	uint8	RW	Increase gain by one step. Writing ‘1’ to this register causes gain to be increased by one step. The register is automatically cleared to ‘0’.	600
0x00001009	uint8	RW	Decrease gain by one step. Writing ‘1’ to this register causes gain to be decreased by one step. The register is automatically cleared to ‘0’.	601
0x0000100A	uint8	RW	Automatic gain control mode 0 – Amplitude 1 – Limits	
0x0000100C	uint16	RW	Automatic gain control first bucket	382.4
0x0000100E	uint16	RW	Automatic gain control last bucket	382.5
0x00001010	single	RO	Calculated maximum allowed charge level in [pC]	382.6
0x00001014	single	RW	Automatic gain control maximum allowed charge in [pC]. Range from 20 to 3000.	382.6
0x00001018	single	RW	Automatic gain control maximum allowed position in [mm]. Range +/- 10 mm.	382.7
0x00001038	uint8	RW	Relative charge threshold in [%]. Value range from 0 to 100	433
0x00004000	single	RO	Amplitude mean value of channel 1	441
0x00004004	single	RO	Amplitude std deviation of channel 1	441
0x00004008	single	RO	Amplitude mean value of channel 2	441
0x0000400C	single	RO	Amplitude std deviation of channel 2	441
0x00004010	single	RO	Amplitude mean value of channel 3	441

0x00004014	single	RO	Amplitude std deviation of channel 3	441
0x00004018	single	RO	Amplitude mean value of channel 4	441
0x0000401C	single	RO	Amplitude std deviation of channel 4	441
0x00004020	single	RO	Mean value of X	406
0x00004024	single	RO	Std deviation of X	407
0x00004028	single	RO	Mean value of Y	412
0x0000402C	single	RO	Std deviation of Y	413
0x00004030	single	RO	Mean value of Q	415
0x00004034	single	RO	Std deviation of Q	416
0x000040AC	uint32	RW	Length of the statistics calculation. The number says how many of the past pulses are used for statistics. The value can be from 1 to 512.	431
0x000040B0	uint32	WO	Writing 1 resets the statistics calculations. The value is automatically changed back to 0	432
0x000040B8	uint32	RW	Select bucket for statistics	430

Table 4.5. Register description of class BPM_RFFE.

Class: BPM_RFFE				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x00000220	uint32	RO	RFFE board status. Possible values of bits [1:0]: 'X0' – Board not present '01' – Board ready '11' – Invalid RFFE board	305
0x00000110	int16	RW	Channel 1 detector bias adjust negative in [V]. Scaling factor: 0.000610426077402026	322
0x00000112	int16	RW	Channel 1 detector bias adjust positive in [V]. Scaling factor: 0.000610426077402026	318
0x00000114	int16	RW	Channel 2 detector bias adjust negative in [V]. Scaling factor: 0.000610426077402026	323
0x00000116	int16	RW	Channel 2 detector bias adjust positive in [V]. Scaling factor: 0.000610426077402026	319
0x00000118	int16	RW	Channel 3 detector bias adjust negative in [V]. Scaling factor: 0.000610426077402026	324
0x0000011A	int16	RW	Channel 3 detector bias adjust positive in [V]. Scaling factor: 0.000610426077402026	320
0x0000011C	int16	RW	Channel 4 detector bias adjust negative in [V]. Scaling factor: 0.000610426077402026	325
0x0000011E	int16	RW	Channel 4 detector bias adjust positive in [V]. Scaling factor: 0.000610426077402026	321
0x00000120	int16	RW	Channel 1 discharge buffer bias negative in [V]. Scaling factor: 0.000610426077402026	354
0x00000122	int16	RW	Channel 1 discharge buffer bias positive in [V]. Scaling factor: 0.000610426077402026	350
0x00000124	int16	RW	Channel 2 discharge buffer bias negative in [V]. Scaling factor: 0.000610426077402026	355
0x00000126	int16	RW	Channel 2 discharge buffer bias positive in [V]. Scaling factor: 0.000610426077402026	351
0x00000128	int16	RW	Channel 3 discharge buffer bias negative in [V]. Scaling factor: 0.000610426077402026	356
0x0000012A	int16	RW	Channel 3 discharge buffer bias positive in [V]. Scaling factor: 0.000610426077402026	352
0x0000012C	int16	RW	Channel 4 discharge buffer bias negative in [V]. Scaling factor: 0.000610426077402026	357
0x0000012E	int16	RW	Channel 4 discharge buffer bias positive in [V]. Scaling factor: 0.000610426077402026	353
0x00000130	int16	RW	Channel 1 discharge buffer offset common in [V]. Scaling factor: 0.000610426077402026614576974728360 4	358
0x00000132	int16	RW	Channel 1 discharge buffer offset differential in [V]. Scaling factor: 0.001220852154804053229153949456	362
0x00000134	int16	RW	Channel 2 discharge buffer offset common in [V]. Scaling factor: 0.000610426077402026614576974728360 4	359
0x00000136	int16	RW	Channel 2 discharge buffer offset differential in [V]. Scaling factor: 0.001220852154804053229153949456	363

0x00000138	int16	RW	Channel 3 discharge buffer offset common in [V]. Scaling factor: 0.000610426077402026614576974728360 4	360
0x0000013A	int16	RW	Channel 3 discharge buffer offset differential in [V]. Scaling factor: 0.001220852154804053229153949456	364
0x0000013C	int16	RW	Channel 4 discharge buffer offset common in [V]. Scaling factor: 0.000610426077402026614576974728360 4	361
0x0000013E	int16	RW	Channel 4 discharge buffer offset differential in [V]. Scaling factor: 0.001220852154804053229153949456	365
0x00000140	int16	RW	Channel 1 discharge buffer supply negative in [V]. Scaling factor: 0.000610426077402026	370
0x00000142	int16	RW	Channel 1 discharge buffer supply positive in [V]. Scaling factor: 0.000610426077402026	366
0x00000144	int16	RW	Channel 2 discharge buffer supply negative in [V]. Scaling factor: 0.000610426077402026	371
0x00000146	int16	RW	Channel 2 discharge buffer supply positive in [V]. Scaling factor: 0.000610426077402026	367
0x00000148	int16	RW	Channel 3 discharge buffer supply negative in [V]. Scaling factor: 0.000610426077402026	372
0x0000014A	int16	RW	Channel 3 discharge buffer supply positive in [V]. Scaling factor: 0.000610426077402026	368
0x0000014C	int16	RW	Channel 4 discharge buffer supply negative in [V]. Scaling factor: 0.000610426077402026	373
0x0000014E	int16	RW	Channel 4 discharge buffer supply positive in [V]. Scaling factor: 0.000610426077402026	369
0x00000154	uint16	RW	Channel 2 RFFE detector temperature set point in [^{0}C]. Scaling factor: 0.03818609775641025 Offset: -30.77	343
0x00000156	uint16	RW	Channel 1 RFFE detector temperature set point in [^{0}C]. Scaling factor: 0.03818609775641025 Offset: -30.77	342
0x00000158	uint16	RW	Channel 4 RFFE detector temperature set point in [^{0}C]. Scaling factor: 0.03818609775641025 Offset: -30.77	345
0x0000015A	uint16	RW	Channel 3 RFFE detector temperature set point in [^{0}C]. Scaling factor: 0.03818609775641025 Offset: -30.77	344
0x0000015C	uint8	RW	Channel 1 amplifier gain. Possible values: 0 – Low [0 dB] 1 – Medium (31 [dB]) 2 – High (52.5 [dB])	317
0x0000015D	uint8	RW	Channel 2 amplifier gain. Possible values: 0 – Low [0 dB] 1 – Medium (31 [dB]) 2 – High (52.5 [dB])	316
0x0000015E	uint8	RW	Channel 3 amplifier gain. Possible values: 0 – Low [0 dB] 1 – Medium (31 [dB]) 2 – High (52.5 [dB])	315
0x0000015F	uint8	RW	Channel 4 amplifier gain. Possible values: 0 – Low [0 dB] 1 – Medium (31 [dB]) 2 – High (52.5 [dB])	314
0x00000164	uint8	RW	Channel 1 attenuation in [dB]. Values range from 0 to 31.5 dB in 0.5dB steps. Scaling factor 0.5.	313
0x00000165	uint8	RW	Channel 2 attenuation in [dB]. Values range from 0 to 31.5 dB in 0.5dB steps. Scaling factor 0.5.	312
0x00000166	uint8	RW	Channel 3 attenuation in [dB]. Values range from 0 to 31.5 dB in 0.5dB steps. Scaling factor 0.5.	311
0x00000167	uint8	RW	Channel 4 attenuation in [dB]. Values range from 0 to 31.5 dB in 0.5dB steps. Scaling factor 0.5.	310
0x00000170	uint8	RW	Channel 1 switched mode regulator enable, ‘1’ – on	374
0x00000171	uint8	RW	Channel 2 switched mode regulator enable, ‘1’ – on	375
0x00000172	uint8	RW	Channel 3 switched mode regulator enable, ‘1’ – on	376
0x00000173	uint8	RW	Channel 4 switched mode regulator enable, ‘1’ – on	377
0x00000174	uint8	RW	Channel 1 5V linear regulator enable, ‘1’ – on	378
0x00000175	uint8	RW	Channel 2 5V linear regulator enable, ‘1’ – on	379

0x00000176	uint8	RW	Channel 3 5V linear regulator enable, '1' – on	380
0x00000177	uint8	RW	Channel 4 5V linear regulator enable, '1' – on	381
0x00000178	uint8	RW	Switch RF input. Possible values: 0 – RF signal 1 – Calibration pulse	300
0x0000017C	uint8	RW	High voltage enabled, '0' – on	398
0x0000017D	uint8	RW	6V enable, '1' – on	385
0x0000017E	uint8	RW	Self discharge, '1' – on	392
0x0000017F	uint8	RW	Detector temperature control enable, '0' – on	391
0x00000300	int16	RO	Channel 1 detector bias sensor positive in [V]. Scaling factor: 0.001220703125	326
0x00000302	int16	RO	Channel 1 detector bias sensor negative in [V]. Scaling factor: 0.001220703125	330
0x00000304	int16	RO	Channel 1 amplifier temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	338
0x00000306	int16	RO	Channel 1 detector temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	346
0x00000308	int16	RO	Channel 2 detector bias sensor positive in [V]. Scaling factor: 0.001220703125	327
0x0000030A	int16	RO	Channel 2 detector bias sensor negative in [V]. Scaling factor: 0.001220703125	331
0x0000030C	int16	RO	Channel 2 amplifier temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	339
0x0000030E	int16	RO	Channel 2 detector temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	347
0x00000310	int16	RO	Channel 3 detector bias sensor positive in [V]. Scaling factor: 0.001220703125	328
0x00000312	int16	RO	Channel 3 detector bias sensor negative in [V]. Scaling factor: 0.001220703125	332
0x00000314	int16	RO	Channel 3 amplifier temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	340
0x00000316	int16	RO	Channel 3 detector temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	348
0x00000318	int16	RO	Channel 4 detector bias sensor positive in [V]. Scaling factor: 0.001220703125	329
0x0000031A	int16	RO	Channel 4 detector bias sensor negative in [V]. Scaling factor: 0.001220703125	331
0x0000031C	int16	RO	Channel 4 amplifier temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	341
0x0000031E	int16	RO	Channel 4 detector temperature measurement in [^{0}C]. Scaling factor: 0.039125100160 Offset: -30.77	349

Table 4.6. Register description of class CFG_FPGA.

Class: CFG_FPGA				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x00000200	uint32	WO	RFFE1 power on. Write anything to switch on the power of RFFE1	301
0x00000204	uint32	WO	RFFE1 power off. Write anything to switch off the power of RFFE1	301
0x00000220	uint32	WO	RFFE2 power on. Write anything to switch on the power of RFFE2	301
0x00000224	uint32	WO	RFFE2 power off. Write anything to switch off the power of RFFE2	301
0x00000240	uint32	WO	RFFE3 power on. Write anything to switch on the power of RFFE3	301

0x00000244	uint32	WO	RFFE3 power off. Write anything to switch off the power of RFFE3	301
0x00000260	uint32	WO	RFFE4 power on. Write anything to switch on the power of RFFE4	301
0x00000264	uint32	WO	RFFE4 power off. Write anything to switch off the power of RFFE4	301
0x00000A00	uint32	RO	RFFE1 Status: Bit 0 – RFFE1 present Bit 1 – RFFE1 error Bit 2 – RFFE1 power good	302-bit 2 303-bit 1
0x00000A04	string8	RO	RFFE1 serial number. This is 8 character string	304
0x00000A20	uint32	RO	RFFE2 Status: Bit 0 – RFFE1 present Bit 1 – RFFE1 error Bit 2 – RFFE1 power good	302-bit 2 303-bit 1
0x00000A24	string8	RO	RFFE2 serial number. This is 8 character string	304
0x00000A40	uint32	RO	RFFE3 Status: Bit 0 – RFFE1 present Bit 1 – RFFE1 error Bit 2 – RFFE1 power good	302-bit 2 303-bit 1
0x00000A44	string8	RO	RFFE3 serial number. This is 8 character string	304
0x00000A60	uint32	RO	RFFE4 Status: Bit 0 – RFFE1 present Bit 1 – RFFE1 error Bit 2 – RFFE1 power good	302-bit 2 303-bit 1
0x00000A64	string8	RO	RFFE4 serial number. This is 8 character string	304

Table 4.7: Register description of class BPM_EEPROM

Class: BPM_EEPROM				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x00000020	uint32	RO	Default BPM EEPROM set	605
0x0000004C	char[32]	RW	XFEL device name.	601

Table 4.8: Register description of class SYS_FPGA

Class: SYS_FPGA				
Address	**Data type**	**Access**	**Description**	**Panel ref.**
0x00000060	uint32	RW	Loss of synchronization counter for the SFP2 connected to control system. Writing anything to this register resets the counter.	
0x00000100	uint32	RO	Trigger from RJ45 connector on the COM board active: 0 – no trigger 1 – trigger active	703
0x00000104	uint8	RW	Event number for Button BPM1/Cavity 1/Re-entrant 1	
0x00000105	uint8	RW	Event number for Button BPM2	
0x00000106	uint8	RW	Event number for Button BPM3/Cavity 2/Re-entrant 2	
0x00000107	uint8	RW	Event number for Button BPM4	
0x00008000	uint32	RO	RF pulse number from timing receiver	702

Table 4.9: Register description of class BP_FPGA

Class: BP_FPGA				
Address	**Data type**	**Access**	**Description**	**Panel**

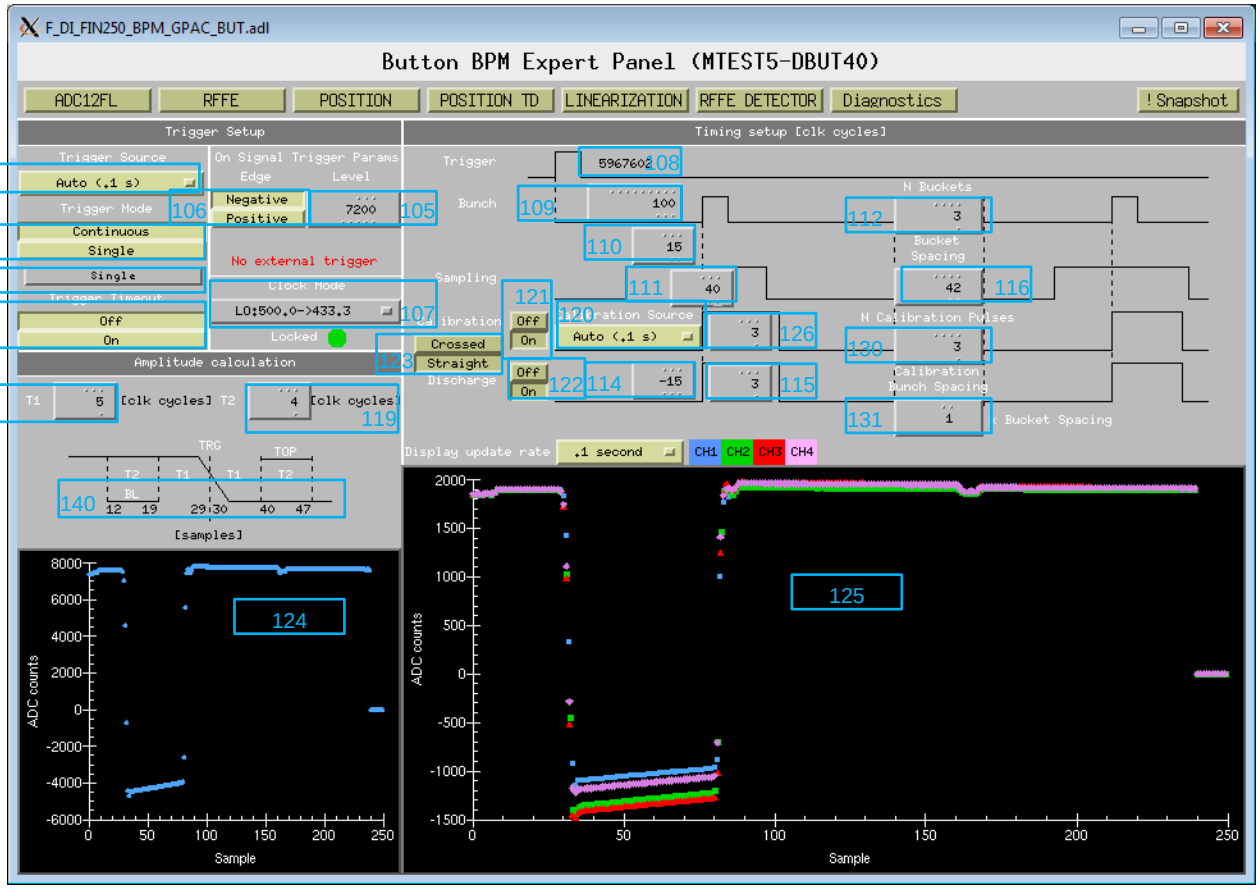
				ref.
0x00000034	uint32	RO	SFP status of COM board	700
0x00000038	uint32	RO	RJ45 connector status on COM board	701

4 Appendix

4.1 Screenshots of EPICS control panels

The screenshots of control panels presented in this appendix contain blue rectangles with reference numbers which are used to identify relation between user control panels and firmware registers described in chapter 3.

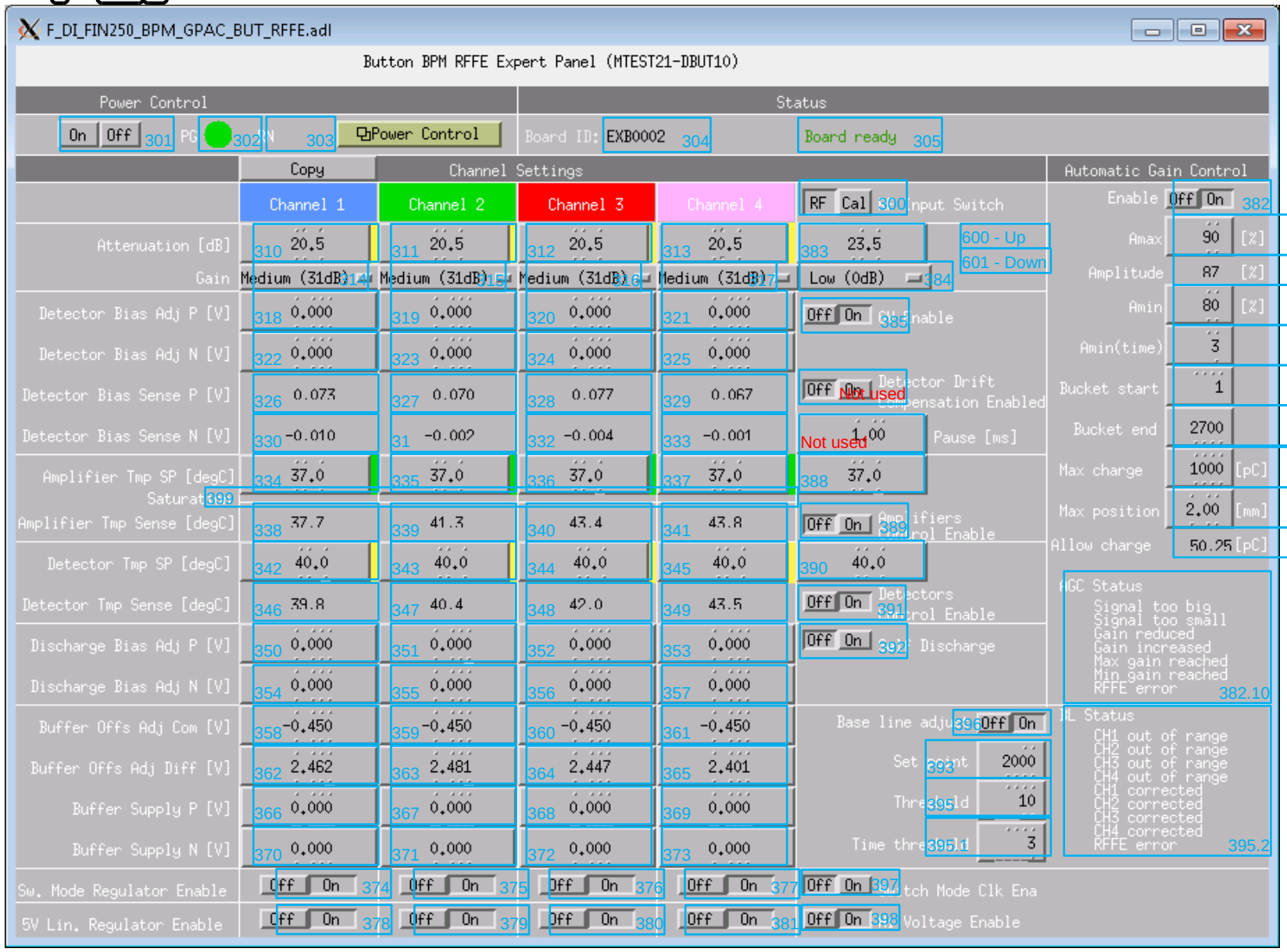
4.1.1 Main BPM control panel



Comments:

- 124 – this plot is sum of four ADC channels from plot 125. The sum is calculated in CPU.

4.1.2 RFFE control panel

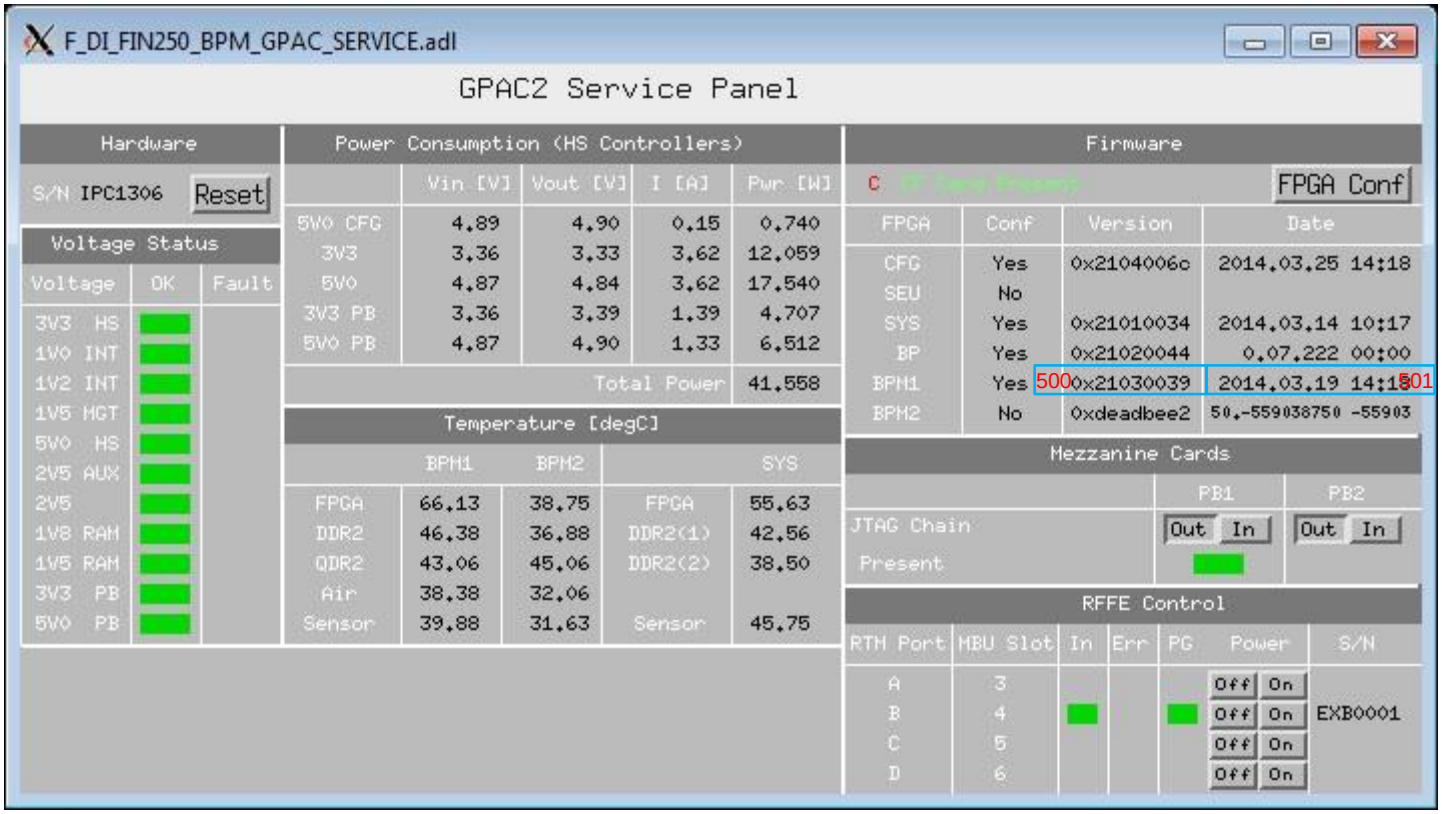

F_DI_FIN250_BPM_GPAC_BUT_RFFE.adl
Button BPM RFFE Expert Panel (MTEST21-DBUT10)
Power Control
Status
On Off 301
PG 302
N 303
Power Control
Board ID: EXB0002 304
Board ready 305
Copy
Channel Settings
Automatic Gain Control
Channel 1
Channel 2
Channel 3
Channel 4
RF Cal 300
Input Switch
Attenuation [dB]
20.5 310
20.5 311
20.5 312
20.5 313
23.5 383
600 - Up
601 - Down
Gain
Medium (31dB) 314
Medium (31dB) 315
Medium (31dB) 316
Medium (31dB) 317
Low (0dB) 384
Detector Bias Adj P [V]
0.000 318
0.000 319
0.000 320
0.000 321
Off On 385
Enable
Detector Bias Adj N [V]
0.000 322
0.000 323
0.000 324
0.000 325
Detector Bias Sense P [V]
0.073 326
0.070 327
0.077 328
0.067 329
Off On
Not used
Detector Drift Compensation Enabled
Detector Bias Sense N [V]
-0.010 330
-0.002 31
-0.004 332
-0.001 333
1.00
Not used
Pause [ms]
Amplifier Tmp SP [degC]
37.0 334
37.0 335
37.0 336
37.0 337
37.0 388
Saturat 399
Amplifier Tmp Sense [degC]
37.7 338
41.3 339
43.4 340
43.8 341
Off On 389
Detector Tmp SP [degC]
40.0 342
40.0 343
40.0 344
40.0 345
40.0 390
Detector Tmp Sense [degC]
39.8 346
40.4 347
42.0 348
43.5 349
Off On 391
Detectors Control Enable
Discharge Bias Adj P [V]
0.000 350
0.000 351
0.000 352
0.000 353
Off On 392
Discharge
Discharge Bias Adj N [V]
0.000 354
0.000 355
0.000 356
0.000 357
Buffer Offs Adj Com [V]
-0.450 358
-0.450 359
-0.450 360
-0.450 361
Base line adju 396 Off On
Buffer Offs Adj Diff [V]
2.462 362
2.481 363
2.447 364
2.401 365
Set point 393
2000
Buffer Supply P [V]
0.000 366
0.000 367
0.000 368
0.000 369
Threshold 395
10
Buffer Supply N [V]
0.000 370
0.000 371
0.000 372
0.000 373
Time thre 395.1
3
Sw. Mode Regulator Enable
Off On 374
Off On 375
Off On 376
Off On 377
Off On 397
Switch Mode Clk Ena
5V Lin. Regulator Enable
Off On 378
Off On 379
Off On 380
Off On 381
Off On 398
Voltage Enable
Enable Off On 382
Amax 90 [%] 382.1
Amplitude 87 [%] 382.8
Amin 80 [%] 382.2
Amin(time) 3 382.3
Bucket start 1 382.4
Bucket end 2700 382.5
Max charge 1000 [pC] 382.6
Max position 2.00 [mm] 382.7
Allow charge 50.25 [pC] 382.9
AGC Status
Signal too big
Signal too small
Gain reduced
Gain increased
Max gain reached
Min gain reached
RFFE error 382.10
AL Status
CH1 out of range
CH2 out of range
CH3 out of range
CH4 out of range
CH1 corrected
CH2 corrected
CH3 corrected
CH4 corrected
RFFE error 395.2

4.1.3 Position measurement panel

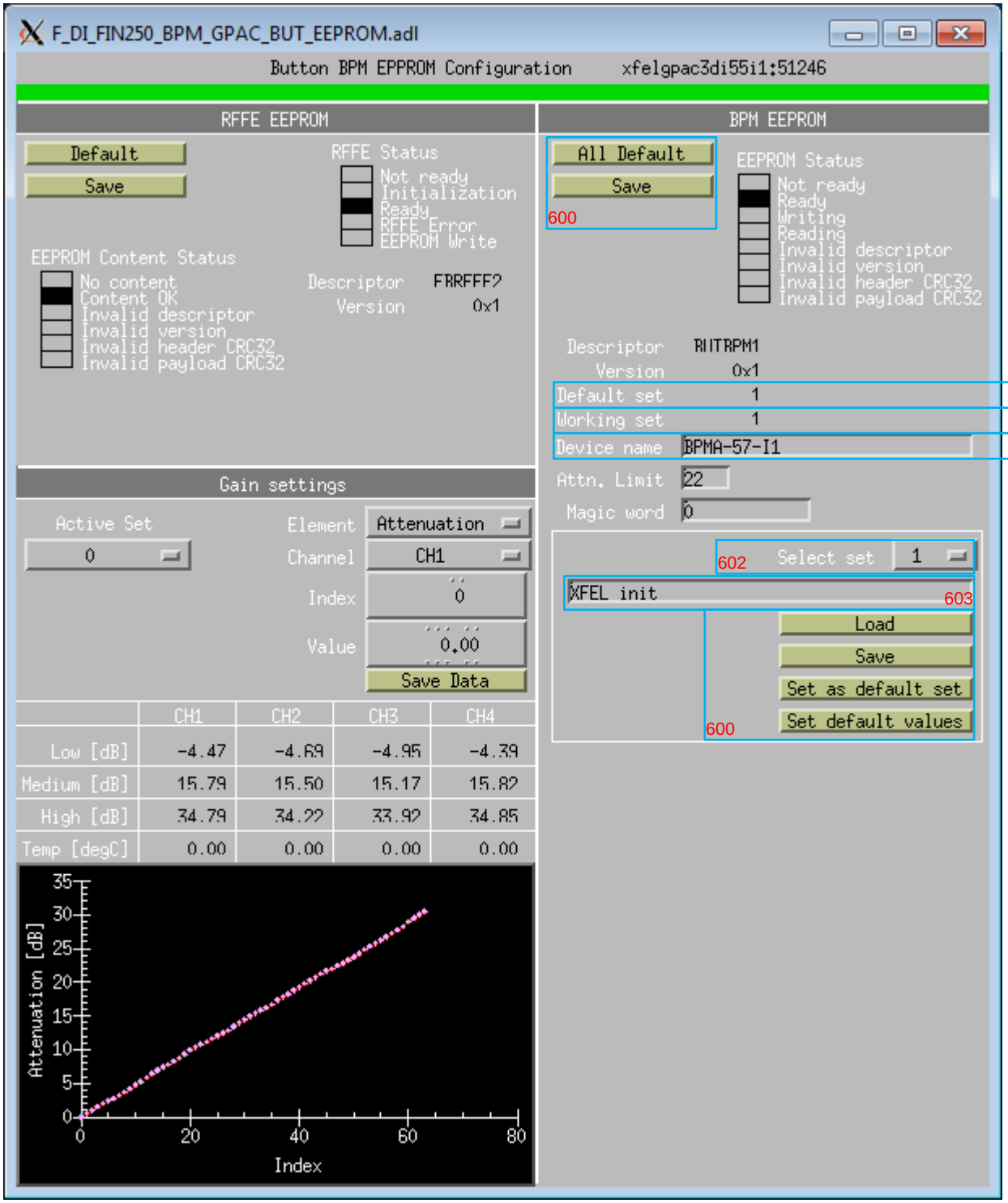
Comments:

- 408, 409, 410 – this is sliding window of X,Y, and Q values. Each window contains 100 values of the first bunch from last 100 bunch trains. With every new bunch train the first bunch value is attached to the 100 elements buffer and shifter by one. This shift buffer is realized in CPU. This method of data presentation is up to DESY – it is not necessary for normal operation of the system.
- 405, 406, 407 – this is X,Y and Q of the first bunch in the bunch train.
- 411, 412, 413 – average X, Y and Q for the sliding buffers from plot 408, 409, 410 calculated in CPU. This is optional
- 414, 415, 416 – the standard deviation of plots 408, 409, 410 calculated in CPU. This is optional.

4.1.4 GPAC Service Panel



4.1.5 RFFE EEPROM and BPM EEPROM Control



4.1.6 MBU COM Board and XFEL Timing Receiver