CFG FPGA Firmware in GPAC 2.1

Revision 1.18
PSI, Villigen, 13.06.2016

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1 Introduction

This document describes functions of the CFG FPGA firmware in GPAC. It also contains memory map of the CFG FPGA service component which is mapped to the address space of PLB in SYS FPGA.
The content of the read memory is updated every second by CFG FPGA.
Writing to the write memory causes immediate action in CFG FPGA firmware.

1.1 History

Revision	Date	Author	Description
1.0	01.04.2014	W. Koprek	First version which only contains general overview and description of the interface to control system.
1.1	18.07.2014	W. Koprek	Added readback of serial numbers of mezzanine cards - 0x870 and 0x878 Added readback of MAC address – 0x868
1.2	21.11.2014	W. Koprek	A new registers and address changes due to new functionalities.
1.3	07.01.2015	W. Koprek	Added temperature readout for RFFE hot swap controllers. Added location register for GPAC.
1.4	08.01.2015	W. Koprek	Changed sw compilation time from string to numbers
1.5	03.03.2015	W. Koprek	Added temperature measurement for RFFEs Added hardware reboot bit and DOOCS new start bit
1.6	06.07.2015	W. Koprek	Added revision number configuration and readback Added BoardID number for each board connected to P0 I2C Added two bits to address 0x810 Redefinition of status word for RFFEs
1.7	16.10.2015	W. Koprek	Changed document title Added section describing booting process.
1.8	26.10.2015	W. Koprek	Fixed address for Linux ready register
1.9	28.10.2015	W. Koprek	Added readout of temperature thresholds. Added register with reason of last GPAC reboot
1.10	05.11.2015	W. Koprek	Added control of ready LED for RFFEs
1.11	16.12.2015	W. Koprek	Added programming interface for adjustable oscillators Added PB BoardID registers Added programming interface for PB serial number C code size optimization
1.12	22.12.2015	W. Koprek	Added watchdog
1.13	08.01.2016	W. Koprek	Added MMC2 programming interface.
1.14	26.01.2016	W. Koprek	Added HS readout addresses for HS6
1.15	23.02.2016	W. Koprek	Bug fix in documentation
1.16	27.04.2016	W. Koprek	Added MBU readout
1.17	09.05.2016	W. Koprek	Added readout of MMC2 power supply failure register
1.18	13.06.2016	W. Koprek	Added readout of MMC2 memory

2 Memory Map of CFG FPGA Visible in SYS FPGA

2.1 Convention

The address map tables assume bit and byte ordering as presented in table 1.

Table 1. Bit and byte order convention

31 24	23 16	15 8	7 0
Byte 0	Byte 1	Byte 2	Byte 3

All addresses are relative to the base address of the CFG FPGA base address.

2.2 Read Memory Map

Address	Size	Description
0x800	uint32	CFG FPGA firmware version
0x804	char[8]	GPAC serial number string
0x80C	uint32	Bit 17: 1 – compact flash card present 0 – no compact flash card
0x810	uint32	Bit 0 – CFG FPGA firmware configuration done Bit 1 – SEU FPGA firmware configuration done Bit 2 – SYS FPGA firmware configuration done Bit 3 – BP FPGA firmware configuration done Bit 4 – BPM1 FPGA firmware configuration done Bit 5 – BPM2 FPGA firmware configuration done Bit 6 – PB1 FPGA firmware configuration done Bit 7 – PB2 FPGA firmware configuration done
0x814	uint32	Bit 0 – 3V3 HS voltage OK Bit 1 – 1V0 INT voltage OK Bit 2 – 1V2 INT voltage OK Bit 3 – 1V5 MGT voltage OK Bit 4 – 5V0 HS voltage OK Bit 5 – 2V5 AUX voltage OK Bit 6 – 2V5 voltage OK Bit 7 – 1V8 RAM voltage OK Bit 8 – 1V5 RAM voltage OK Bit 10 – 3V3 PB voltage OK Bit 11 – 5V0 PB voltage OK
0x818	uint32	Bit 0 – 3V3 HS voltage fault Bit 1 – 1V0 INT voltage fault Bit 2 – 1V2 INT voltage fault Bit 3 – 1V5 MGT voltage fault Bit 4 – 5V0 HS voltage fault Bit 5 – 2V5 AUX voltage fault Bit 6 – 2V5 voltage fault Bit 7 – 1V8 RAM voltage fault Bit 8 – 1V5 RAM voltage fault Bit 10 – 3V3 PB voltage fault Bit 11 – 5V0 PB voltage fault
0x81D	uint8	Output voltage of the 5V0 CFG HS controller. Scaling factor to [V]: 0.0605
0x81E	uint8	Current of the 5V0 CFG HS controller. Scaling factor to [A]: 0.03775
0x81F	uint8	Input voltage of the 5V0 CFG HS controller. Scaling factor to [V]: 0.023618
0x821	uint8	Output voltage of the 3V3 HS controller. Scaling factor to [V]: 0.0605

0x822	uint8	Current of the 3V3 HS controller. Scaling factor to [A]: 0.10067
0x823	uint8	Input voltage of the 3V3 HS controller. Scaling factor to [V]: 0.015424
0x825	uint8	Output voltage of the 5V0 HS controller. Scaling factor to [V]: 0.0605
0x826	uint8	Current of the 5V0 HS controller. Scaling factor to [A]: 0.06040
0x827	uint8	Input voltage of the 5V0 HS controller. Scaling factor to [V]: 0.023618
0x829	uint8	Output voltage of the 3V3 PB HS controller. Scaling factor to [V]: 0.0605
0x82A	uint8	Current of the 3V3 PB HS controller. Scaling factor to [A]: 0.06040
0x82B	uint8	Input voltage of the 3V3 PB HS controller. Scaling factor to [V]: 0.015424
0x82D	uint8	Output voltage of the 5V0 PB HS controller. Scaling factor to [V]: 0.0605
0x82E	uint8	Current of the 5V0 HS PB controller. Scaling factor to [A]: 0.06040
0x82F	uint8	Input voltage of the 5V0 PB HS controller. Scaling factor to [V]: 0.023618
0x830	uint16	BPM1 FPGA temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x832	uint16	BPM1 DDR2 temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x834	uint16	BPM1 QDR2 temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x836	uint16	BPM1 Ambient temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x838	uint16	BPM1 sensor temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x83A	uint16	BPM2 FPGA temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x83C	uint16	BPM2 DDR2 temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x83E	uint16	BPM2 QDR2 temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x840	uint16	BPM2 Ambient temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x842	uint16	BPM2 sensor temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x844	uint16	SYS FPGA temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x846	uint16	SYS DDR2-1 temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x848	uint16	SYS DDR2-2 temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x84C	uint16	SYS sensor temperature. Scaling factor to [^{o}C]: 0.0625, Offset: -2048
0x850	uint16	CFG FPGA firmware compilation date – Year
0x854	uint16	CFG FPGA firmware compilation date – Month
0x858	uint16	CFG FPGA firmware compilation date – Day
0x85C	uint16	CFG FPGA firmware compilation date – Hour
0x860	uint16	CFG FPGA firmware compilation date – Minute
0x864	uint8	Piggyback 1 present when value is 1
0x865	uint8	Piggyback 2 present when value is 1
0x866	uint8	Piggyback 1 board ID 1 – ADC12FL 2 – ADC16HL 3 – DAC16HL Other values – unknown piggyback
0x867	uint8	Piggyback 2 board ID 1 – ADC12FL 2 – ADC16HL 3 – DAC16HL Other values – unknown piggyback
0x868	uint8	Byte 0 of MAC address
0x869	uint8	Byte 1 of MAC address
0x86A	uint8	Byte 2 of MAC address
0x86B	uint8	Byte 3 of MAC address
0x86C	uint8	Byte 4 of MAC address
0x86D	uint8	Byte 5 of MAC address
0x86E	uint8	Byte 6 of MAC address

0x86F	uint8	Byte 7 of MAC address
0x870	char[8]	PB1 serial number string
0x878	char[8]	PB2 serial number string
0x880	uint32	Reserved
0x884	uint32	Revision number of the ACE file used for FPGA configuration.
0x88C	uint32	Actual value of the CFG FPGA check of Linux: 0 – no check 1 – check enabled
0x890	uint8	Temperature warning threshold in degC
0x891	uint8	Temperature alarm threshold in degC
0x892	uint8	Reason of the last GPAC reboot: Bit 0 – power down Bit 1 – temperature alarm Bit 2 – user reset Bit 3 – front panel handle opened Bit 4 – reset from serial console
0x894	uint32	Actual frequency of the adjustable oscillator 0 in [Hz]
0x898	uint32	Initial frequency of the adjustable oscillator 0 in [Hz]
0x89C	char[6]	Initial content of registers 7-12 of the adjustable oscillator 0
0x8A4	uint32	Actual frequency of the adjustable oscillator 1 in [Hz]
0x8A8	uint32	Initial frequency of the adjustable oscillator 1 in [Hz]
0x8AC	char[6]	Initial content of registers 7-12 of the adjustable oscillator 1
0x8B4	uint32	Watchdog counter measures time from last watchdog reset. It is scaled in [ms]. The scaling factor is 0.000016.
0x8B8	uint32	MMC2 byte write acknowledge register. The register contains counter which is incremented whenever the write operation to address 0x0B8 was successful.
0x940	uint32	Software compilation year
0x944	uint32	Software compilation month
0x948	uint32	Software compilation day
0x94C	uint32	Software compilation hour
0x950	uint32	Software compilation minute
0x954	uint32	GPAC location: 0 – VME 1 - MBU
0x958	uint32	GPAC restart register Bit[0] – if bit is set to ‘1’ then it means that GPAC has just started. Control system can set this bit to zero
0x95C	uint32	Control system dependent read/write register. GPAC does not change content of this register.
0xA01	uint8	Bit[0] – RFFE1 present
0xA02	uint8	RFFE1 error number: 0 – no error 1 – I2C bus timeout 3 – Invalid descriptor in EEPROM 5 – Not supported RFFE board ID 7 – To many hot swap controllers
0xA03	uint8	Bit[0] – RFFE1 power good
0xA04	char[8]	RFFE1 serial number string

0xA0C	uint8	Status register of the HS1 controller in RFFE1. Board dependent bit meaning
0xA0D	uint8	Fault register of the HS1 controller in RFFE1. Board dependent bit meaning
0xA0E	uint8	Current of the HS1 controller in RFFE1. Board dependent scaling factor.
0xA0F	uint8	Voltage of the HS1 controller in RFFE1. Board dependent scaling factor.
0xA10	uint8	Status register of the HS2 controller in RFFE1. Board dependent bit meaning
0xA11	uint8	Fault register of the HS2 controller in RFFE1. Board dependent bit meaning
0xA12	uint8	Current of the HS2 controller in RFFE1. Board dependent scaling factor.
0xA13	uint8	Voltage of the HS2 controller in RFFE1. Board dependent scaling factor.
0xA14	uint8	Status register of the HS3 controller in RFFE1. Board dependent bit meaning
0xA15	uint8	Fault register of the HS3 controller in RFFE1. Board dependent bit meaning
0xA16	uint8	Current of the HS3 controller in RFFE1. Board dependent scaling factor.
0xA17	uint8	Voltage of the HS3 controller in RFFE1. Board dependent scaling factor.
0xA18	int16	RFFE1 temperature, scaling factor 0.0625 for [degC].
0xA1A	uint8	BoardID – unique model number of the RFFE1 board
0xA21	uint8	Bit[0] – RFFE2 present
0xA22	uint8	RFFE2 error number: 0 – no error 1 – I2C bus timeout 3 – Invalid descriptor in EEPROM 5 – Not supported RFFE board ID 7 – To many hot swap controllers
0xA23	uint8	Bit[0] – RFFE2 power good
0xA24	char[8]	RFFE2 serial number string
0xA2C	uint8	Status register of the HS1 controller in RFFE2. Board dependent bits meaning
0xA2D	uint8	Fault register of the HS1 controller in RFFE2. Board dependent bits meaning
0xA2E	uint8	Current of the HS1 controller in RFFE2. Board dependent scaling factor.
0xA2F	uint8	Voltage of the HS1 controller in RFFE2. Board dependent scaling factor.
0xA30	uint8	Status register of the HS2 controller in RFFE2. Board dependent bit meaning
0xA31	uint8	Fault register of the HS2 controller in RFFE2. Board dependent bit meaning
0xA32	uint8	Current of the HS2 controller in RFFE2. Board dependent scaling factor.
0xA33	uint8	Voltage of the HS2 controller in RFFE2. Board dependent scaling factor.
0xA34	uint8	Status register of the HS3 controller in RFFE2. Board dependent bit meaning
0xA35	uint8	Fault register of the HS3 controller in RFFE2. Board dependent bit meaning
0xA36	uint8	Current of the HS3 controller in RFFE2. Board dependent scaling factor.
0xA38	int16	RFFE2 temperature, scaling factor 0.0625 for [degC].
0xA37	uint8	Voltage of the HS3 controller in RFFE2. Board dependent scaling factor.
0xA38	int16	RFFE2 temperature, scaling factor 0.0625 for [degC].

0xA3A	uint8	BoardID – unique model number of the RFFE2 board
0xA41	uint8	Bit[0] – RFFE3 present
0xA42	uint8	RFFE3 error number: 0 – no error 1 – I2C bus timeout 3 – Invalid descriptor in EEPROM 5 – Not supported RFFE board ID 7 – To many hot swap controllers
0xA43	uint8	Bit[0] – RFFE3 power good
0xA44	char[8]	RFFE3 serial number string
0xA4C	uint8	Status register of the HS1 controller in RFFE3. Board dependent bits meaning
0xA4D	uint8	Fault register of the HS1 controller in RFFE3. Board dependent bits meaning
0xA4E	uint8	Current of the HS1 controller in RFFE3. Board dependent scaling factor.
0xA4F	uint8	Voltage of the HS1 controller in RFFE3. Board dependent scaling factor.
0xA50	uint8	Status register of the HS2 controller in RFFE3. Board dependent bits meaning
0xA51	uint8	Fault register of the HS2 controller in RFFE3. Board dependent bits meaning
0xA52	uint8	Current of the HS2 controller in RFFE3. Board dependent scaling factor.
0xA53	uint8	Voltage of the HS2 controller in RFFE3. Board dependent scaling factor.
0xA54	uint8	Status register of the HS3 controller in RFFE3. Board dependent bit meaning
0xA55	uint8	Fault register of the HS3 controller in RFFE3. Board dependent bit meaning
0xA56	uint8	Current of the HS3 controller in RFFE3. Board dependent scaling factor.
0xA57	uint8	Voltage of the HS3 controller in RFFE3. Board dependent scaling factor.
0xA58	int16	RFFE3 temperature, scaling factor 0.0625 for [degC].
0xA5A	uint8	BoardID – unique model number of the RFFE3 board
0xA61	uint8	Bit[0] – RFFE4 present
0xA62	uint8	RFFE4 error number: 0 – no error 1 – I2C bus timeout 3 – Invalid descriptor in EEPROM 5 – Not supported RFFE board ID 7 – To many hot swap controllers
0xA63	uint8	Bit[0] – RFFE4 power good
0xA64	char[8]	RFFE4 serial number string
0xA6C	uint8	Status register of the HS1 controller in RFFE4. Board dependent bits meaning
0xA6D	uint8	Fault register of the HS1 controller in RFFE4. Board dependent bits meaning
0xA6E	uint8	Current of the HS1 controller in RFFE4. Board dependent scaling factor.
0xA6F	uint8	Voltage of the HS1 controller in RFFE4. Board dependent scaling factor.
0xA70	uint8	Status register of the HS2 controller in RFFE4. Board dependent bit meaning
0xA71	uint8	Fault register of the HS2 controller in RFFE4. Board dependent bit meaning

0xA72	uint8	Current of the HS2 controller in RFFE4. Board dependent scaling factor.
0xA73	uint8	Voltage of the HS2 controller in RFFE4. Board dependent scaling factor.
0xA74	uint8	Status register of the HS3 controller in RFFE4. Board dependent bit meaning
0xA75	uint8	Fault register of the HS3 controller in RFFE4. Board dependent bit meaning
0xA76	uint8	Current of the HS3 controller in RFFE4. Board dependent scaling factor.
0xA77	uint8	Voltage of the HS3 controller in RFFE4. Board dependent scaling factor.
0xA78	int16	RFFE4 temperature, scaling factor 0.0625 for [degC].
0xA7A	uint8	BoardID – unique model number of the RFFE4 board
0xAA1	uint8	Bit[0] – DIO board present
0xAA2	uint8	DIO board error number: 0 – no error 1 – I2C bus timeout 3 – Invalid descriptor in EEPROM 5 – Not supported RFFE board ID 7 – To many hot swap controllers
0xAA3	uint8	Bit[0] – DIO board power good
0xAA4	char[8]	DIO board serial number string
0xAAC	uint8	Status register of the HS1 controller in DIO board. Board dependent bits meaning
0xAAD	uint8	Fault register of the HS1 controller in DIO board. Board dependent bits meaning
0xAAE	uint8	Current of the HS1 controller in DIO board. Board dependent scaling factor.
0xAAF	uint8	Voltage of the HS1 controller in DIO board. Board dependent scaling factor.
0xAB0	uint8	Status register of the HS2 controller in DIO board. Board dependent bit meaning
0xAB1	uint8	Fault register of the HS2 controller in DIO board. Board dependent bit meaning
0xAB2	uint8	Current of the HS2 controller in DIO board. Board dependent scaling factor.
0xAB3	uint8	Voltage of the HS2 controller in DIO board. Board dependent scaling factor.
0xAB4	uint8	Status register of the HS3 controller in DIO board. Board dependent bit meaning
0xAB5	uint8	Fault register of the HS3 controller in DIO board. Board dependent bit meaning
0xAB6	uint8	Current of the HS3 controller in DIO board. Board dependent scaling factor.
0xAB7	uint8	Voltage of the HS3 controller in DIO board. Board dependent scaling factor.
0xAB8	int16	DIO board temperature, scaling factor 0.0625 for [degC].
0xABA	uint8	BoardID – unique model number of the DIO board
0xAC1	uint8	Bit[0] – COM board present
0xAC2	uint8	COM board error number: 0 – no error 1 – I2C bus timeout

		3 – Invalid descriptor in EEPROM 5 – Not supported RFFE board ID 7 – To many hot swap controllers
0xAC3	uint8	Bit[0] – COM board power good
0xAC4	char[8]	COM board serial number string
0xACC	uint8	Status register of the HS1 controller in COM board. Board dependent bits meaning
0xACD	uint8	Fault register of the HS1 controller in COM board. Board dependent bits meaning
0xACE	uint8	Current of the HS1 controller in COM board. Board dependent scaling factor.
0xACF	uint8	Voltage of the HS1 controller in COM board. Board dependent scaling factor.
0xAD0	uint8	Status register of the HS2 controller in COM board. Board dependent bit meaning
0xAD1	uint8	Fault register of the HS2 controller in COM board. Board dependent bit meaning
0xAD2	uint8	Current of the HS2 controller in COM board. Board dependent scaling factor.
0xAD3	uint8	Voltage of the HS2 controller in COM board. Board dependent scaling factor.
0xAD4	uint8	Status register of the HS3 controller in COM board. Board dependent bit meaning
0xAD5	uint8	Fault register of the HS3 controller in COM board. Board dependent bit meaning
0xAD6	uint8	Current of the HS3 controller in COM board. Board dependent scaling factor.
0xAD7	uint8	Voltage of the HS3 controller in COM board. Board dependent scaling factor.
0xAD8	int16	COM board temperature, scaling factor 0.0625 for [degC].
0xADA	uint8	BoardID – unique model number of the COM board
0xB00	char[6]	MMC2 version string
0xB06	char[6]	MMC2 MAC
0xB0C	int16	MMC temperature readout in [degC]. Scaling factor 0.00390625.
0xB0E	uint8	MMC2 power supply failure register: Bit [0] – power supply 1 failure Bit [1] – power supply 2 failure
0xB10	char[8]	MMC2 S/N
0xB20	char[8]	Power module S/N
0xC00	char[4]	MMC2 firmware version
0xC04	char[4]	MMC2 software version
0xC08	uint16	Reserved
0xC0A	uint16	MMC2 firmware status. Bits 13:0 are the input bits read from the I2C gpio IC (Read-only): 0.5V power monitor alert_b 1.3.3V power monitor alert_b 2.12V supply 1 alert_b 3.12V supply 2 alert_b 4.+12V power monitor alert_b

		5.-12V power monitor alert_b 6.12V oring switch 1 fault_b 7.12V oring switch 2 fault_b 8.Heater 1 alert_b 9.Heater 2 alert_b 10. Temperature alert 11. FAN tray alert 12. Power meter alert 13. Elapsed time counter alert Bit 14 is the flag USE_SUPPLY2 that controls which power supply is enabled at power-up (Read-write). Bit 15 is the flag FORCE_POWERDOWN that forces both power supplies to switch off (Read-write).
0xC0C	uint32	MMC2 firmware status. Bits 12:0 are the output bits written to the I2C gpio IC: 0.Not used 1.Front panel FW led 2.Oled reset_n (hardwired to 1) 3.Front panel HW led 4.Front panel remote led (hardwired to 1) 5.Fan controller 1 reset 6.Fan controller 2 reset 7.Fan controller 1 fault (hardwired to 0) 8.Fan controller 2 fault (hardwired to 0) 9.Master reset 10. Spe_b 11. Heater powerdown (active low) 12. FPGA's VPUMP ON (hardwired to 1) Bits 23:16 reflect the status of the FPGA's input pins: 16. Front panel on switch 17. Fan present (active low) 18. Slave power enable 19. Watchdog 20. V1 power good 21. V2 power good 22. V1 power fail 23. V2 power fail Bits 29:25 reflect the status of the FPGA's output pins: 25. HSC5 alert 26. V1 remote enable 27. V2 remote enable 28. V1 switch off V2 switch off
0xC10	int16	Front fans outlet temperature in [degC]. Scaling factor 0.0625
0xC12	int16	Rear fans outlet temperature in [degC]. Scaling factor 0.0625
0xC14	int16	Fans inlet temperature in [degC]. Scaling factor 0.0625
0xC16	int16	Power board temperature in [degC]. Scaling factor 0.0625
0xC18	int16	Hit sink temperature in [degC]. No scaling
0xC1A	uint16	Readout of heater DAC output
0xC1C	uint8[4]	MMC2 IP address. Each byte is one segment of the IP address

0xC20	uint32	Reserved
0xC24	uint32	Reserved
0xC28	single	Oring 1 power in [W], precision 2
0xC2C	single	Oring 1 current in [mA], precision 0
0xC30	single	Oring 1 input voltage in [V], precision 2
0xC34	single	Oring 1 output voltage in [V], precision 2
0xC38	single	Oring 2 power in [W], precision 2
0xC3C	single	Oring 2 current in [mA], precision 0
0xC40	single	Oring 2 input voltage in [V], precision 2
0xC44	single	Oring 2 output voltage in [V], precision 2
0xC48	single	Regulator 3V3 power in [W], precision 2
0xC4C	single	Regulator 3V3 current in [mA], precision 0
0xC50	single	Regulator 3V3 input voltage in [V], precision 2
0xC54	single	Regulator 3V3 output voltage in [V], precision 2
0xC58	single	Regulator 5V0 power in [W], precision 2
0xC5C	single	Regulator 5V0 current in [mA], precision 0
0xC60	single	Regulator 5V0 input voltage in [V], precision 2
0xC64	single	Regulator 5V0 output voltage in [V], precision 2
0xC68	single	Regulator +12V0 power in [W], precision 2
0xC6C	single	Regulator +12V0 current in [mA], precision 0
0xC70	single	Regulator +12V0 input voltage in [V], precision 2
0xC74	single	Regulator +12V0 output voltage in [V], precision 2
0xC78	single	Regulator -12V0 power in [W], precision 2
0xC7C	single	Regulator -12V0 current in [mA], precision 0
0xC80	single	Regulator -12V0 input voltage in [V], precision 2
0xC84	single	Regulator -12V0 output voltage in [V], precision 2
0xC88	single	Power distribution module 1 – RMS current in [A], precision 2
0xC8C	single	Power distribution module 1 – RMS voltage in [V], precision 2
0xC90	single	Power distribution module 1 – average current in [A], precision 2
0xC94	single	Power distribution module 2 – RMS current in [A], precision 2
0xC98	single	Power distribution module 2 – RMS voltage in [V], precision 2
0xC9C	single	Power distribution module 2 – average current in [A], precision 2
0xCA0	uint32	Fans controller 1 status word. See MAX31785, table 17 for details
0xCA4	uint32	Fans controller 1 MFR mode. See MAX31785, table 22 for details
0xCA8	uint32	Fans controller 1 lifetime in hours.
0xCAC	int16	Reserved
0xCAE	int16	Fans controller 1 temperature readout in [degC]. Scacling factor 0.01.
0xCB0	uint32	Controller 1 fan 1 configuration (see MAX31785 for details)
0xCB4	uint32	Controller 1 fan 1 MFR config register (see MAX31785 for details)
0xCB8	uint32	Controller 1 fan 1 MFR response register (see MAX31785 for details)
0xCBC	uint32	Controller 1 fan 1 status register (see MAX31785 for details)
0xCC0	uint32	Controller 1 fan 1 command register (see MAX31785 for details)
0xCC4	uint32	Controller 1 fan 1 speed in [RPM]
0xCC8	uint32	Controller 1 fan 1 lifetime in days
0xCCC	uint32	Controller 1 fan 1 PWM read (see MAX31785 for details)
0xCD0	uint32	Controller 1 fan 1 PWM average (see MAX31785 for details)
0xCD4	uint32	Controller 1 fan 2 configuration (see MAX31785 for details)
0xCD8	uint32	Controller 1 fan 2 MFR config register (see MAX31785 for details)

0xCDC	uint32	Controller 1 fan 2 MFR response register (see MAX31785 for details)
0xCE0	uint32	Controller 1 fan 2 status register (see MAX31785 for details)
0xCE4	uint32	Controller 1 fan 2 command register (see MAX31785 for details)
0xCE8	uint32	Controller 1 fan 2 speed in [RPM]
0xCEC	uint32	Controller 1 fan 2 lifetime in days
0xCF0	uint32	Controller 1 fan 2 PWM read (see MAX31785 for details)
0xCF4	uint32	Controller 1 fan 2 PWM average (see MAX31785 for details)
0xCF8	uint32	Controller 1 fan 3 configuration (see MAX31785 for details)
0xCFC	uint32	Controller 1 fan 3 MFR config register (see MAX31785 for details)
0xD00	uint32	Controller 1 fan 3 MFR response register (see MAX31785 for details)
0xD04	uint32	Controller 1 fan 3 status register (see MAX31785 for details)
0xD08	uint32	Controller 1 fan 3 command register (see MAX31785 for details)
0xD0C	uint32	Controller 1 fan 3 speed in [RPM]
0xD10	uint32	Controller 1 fan 3 lifetime in days
0xD14	uint32	Controller 1 fan 3 PWM read (see MAX31785 for details)
0xD18	uint32	Controller 1 fan 3 PWM average (see MAX31785 for details)
0xD1C	uint32	Controller 1 fan 4 configuration (see MAX31785 for details)
0xD20	uint32	Controller 1 fan 4 MFR config register (see MAX31785 for details)
0xD24	uint32	Controller 1 fan 4 MFR response register (see MAX31785 for details)
0xD28	uint32	Controller 1 fan 4 status register (see MAX31785 for details)
0xD2C	uint32	Controller 1 fan 4 command register (see MAX31785 for details)
0xD30	uint32	Controller 1 fan 4 speed in [RPM]
0xD34	uint32	Controller 1 fan 4 lifetime in days
0xD38	uint32	Controller 1 fan 4 PWM read (see MAX31785 for details)
0xD3C	uint32	Controller 1 fan 4 PWM average (see MAX31785 for details)
0xD40	uint32	Fans controller 2 status word. See MAX31785, table 17 for details
0xD44	uint32	Fans controller 2 MFR mode. See MAX31785, table 22 for details
0xD48	uint32	Fans controller 2 lifetime in hours.
0xD4C	int16	Reserved
0xD4E	int16	Fans controller 2 temperature readout in [degC]. Scacling factor 0.01.
0xD50	uint32	Controller 2 fan 1 configuration (see MAX31785 for details)
0xD54	uint32	Controller 2 fan 1 MFR config register (see MAX31785 for details)
0xD58	uint32	Controller 2 fan 1 MFR response register (see MAX31785 for details)
0xD5C	uint32	Controller 2 fan 1 status register (see MAX31785 for details)
0xD60	uint32	Controller 2 fan 1 command register (see MAX31785 for details)
0xD64	uint32	Controller 2 fan 1 speed in [RPM]
0xD68	uint32	Controller 2 fan 1 lifetime in days
0xD6C	uint32	Controller 2 fan 1 PWM read (see MAX31785 for details)
0xD70	uint32	Controller 2 fan 1 PWM average (see MAX31785 for details)
0xD74	uint32	Controller 2 fan 2 configuration (see MAX31785 for details)
0xD78	uint32	Controller 2 fan 2 MFR config register (see MAX31785 for details)
0xD7C	uint32	Controller 2 fan 2 MFR response register (see MAX31785 for details)
0xD80	uint32	Controller 2 fan 2 status register (see MAX31785 for details)
0xD84	uint32	Controller 2 fan 2 command register (see MAX31785 for details)
0xD88	uint32	Controller 2 fan 2 speed in [RPM]
0xD8C	uint32	Controller 2 fan 2 lifetime in days
0xD90	uint32	Controller 2 fan 2 PWM read (see MAX31785 for details)
0xD94	uint32	Controller 2 fan 2 PWM average (see MAX31785 for details)

0xD98	uint32	Controller 2 fan 3 configuration (see MAX31785 for details)
0xD9C	uint32	Controller 2 fan 3 MFR config register (see MAX31785 for details)
0xDA0	uint32	Controller 2 fan 3 MFR response register (see MAX31785 for details)
0xDA4	uint32	Controller 2 fan 3 status register (see MAX31785 for details)
0xDA8	uint32	Controller 2 fan 3 command register (see MAX31785 for details)
0xDAC	uint32	Controller 2 fan 3 speed in [RPM]
0xDB0	uint32	Controller 2 fan 3 lifetime in days
0xDB4	uint32	Controller 2 fan 3 PWM read (see MAX31785 for details)
0xDB8	uint32	Controller 2 fan 3 PWM average (see MAX31785 for details)
0xDBC	uint32	Controller 2 fan 4 configuration (see MAX31785 for details)
0xDC0	uint32	Controller 2 fan 4 MFR config register (see MAX31785 for details)
0xDC4	uint32	Controller 2 fan 4 MFR response register (see MAX31785 for details)
0xDC8	uint32	Controller 2 fan 4 status register (see MAX31785 for details)
0xDCC	uint32	Controller 2 fan 4 command register (see MAX31785 for details)
0xDD0	uint32	Controller 2 fan 4 speed in [RPM]
0xDD4	uint32	Controller 2 fan 4 lifetime in days
0xDD8	uint32	Controller 2 fan 4 PWM read (see MAX31785 for details)
0xDDC	uint32	Controller 2 fan 4 PWM average (see MAX31785 for details)
0x1E0	char[8]	String with front panel version
0x1E8	char[8]	String with backplane version
0x1F0	char[8]	MBU crate serial number
0x1F8	uint16	Return code of the firmware 0 update procedure
0x1FA	uint16	Return code of the firmware 1 update procedure
0x1FC	uint16	Return code of the software 0 update procedure
0x1FE	uint16	Return code of the software 1 update procedure

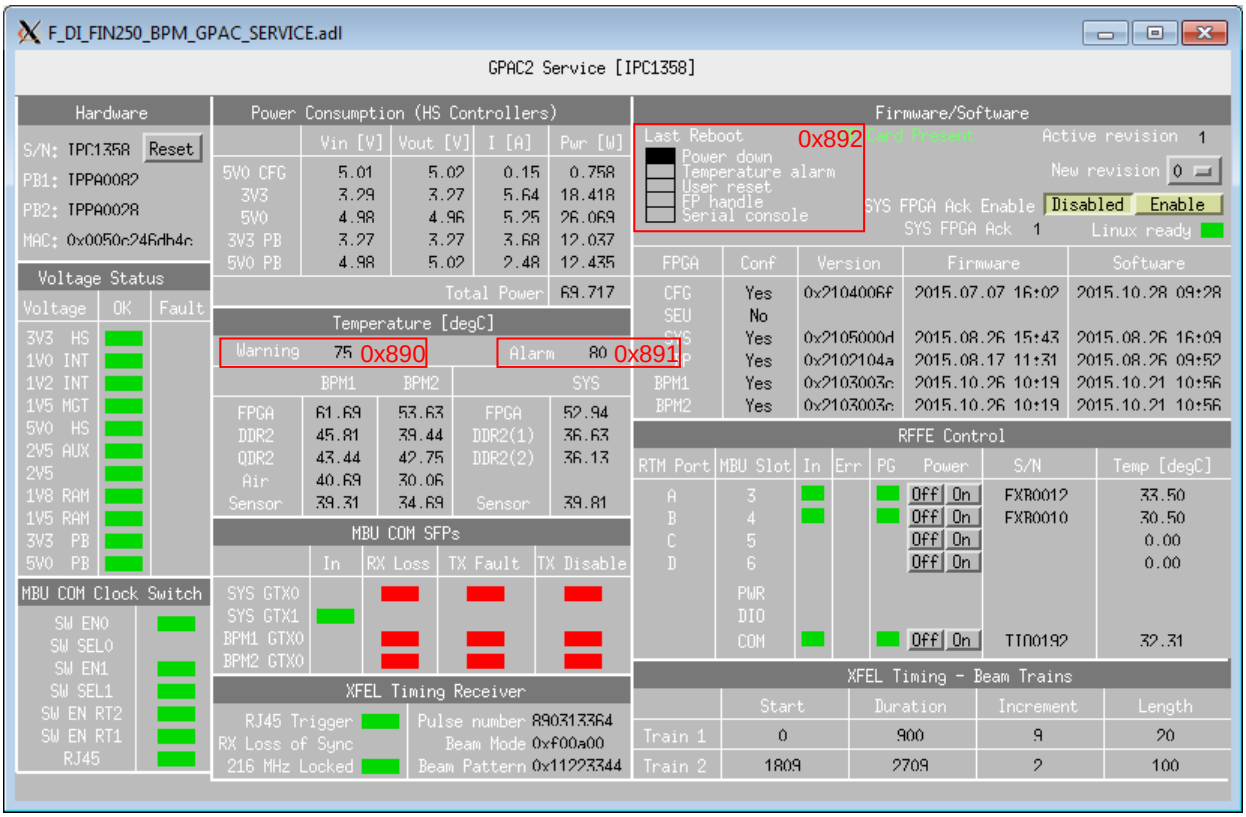
2.3 Write Memory Map

Address	Size	Description
0x000	uint32	GPAC hardware reset. Writing anything to this address causes hard reset of the GPAC board
0x080	uint32	Reserved. Do not write anything to this address.
0x084	uint32	SystemACE revision number write register. Write value from 0 to 2 to select ACE file revision by next reboot of GPAC. Note: Use this address to write new value to 1-Wire EEPROM in GPAC, but this register does not reflect the current value after reboot.
0x088	uint32	Linux is ready. This address is written by Linux when the booting process is finished. Read this address to check if Linux has finished booting. Do not write anything to this address.
0x08C	uint32	Configure if CFG FPGA checks whether Linux has booted correctly: 0 – no check 1 – check enabled Note: Use this address to write new value to 1-Wire EEPROM in GPAC, but this register does not reflect the current value after reboot. Use address 0x88C to read actual state of the 1-Wire EEPROM value.
0x090	uint32	Set board ID in 1-Wire EEPROM of a piggyback [31:16] – magic word

		[15:8] – piggyback number 0 or 1 [7:0] - reserved
0x094	char[8]	Piggyback serial number string for programming with address 0x09C
0x09C	uint32	Write serial number from address 0x094 to 1-Wire EEPROM of piggyback [31:16] – magic word [15:8] – piggyback number 0 or 1 [7:0] - reserved
0x0A0	uint32	New frequency for adjustable oscillator 0 in [Hz]
0x0A4	uint32	Programming register 1 for adjustable oscillator 0 [31:24] – register 7 [23:16] – register 8 [15:8] – register 9 [7:0] – register 10
0x0A8	uint32	Programming register 2 for adjustable oscillator 0 [31:24] – register 11 [23:16] – register 12 [15:10] – reserved [9] – write 1-Wire EEPROM [8] – configure oscillator [7:0] – magic byte 0xAB Write operation to this register triggers the action in CFG FPGA
0x0AC	uint32	New frequency for adjustable oscillator 1 in [Hz]
0x0B0	uint32	Programming register 1 for adjustable oscillator 1 [31:24] – register 7 [23:16] – register 8 [15:8] – register 9 [7:0] – register 10
0x0B4	uint32	Programming register 2 for adjustable oscillator 1 [31:24] – register 11 [23:16] – register 12 [15:10] – reserved [9] – write 1-Wire EEPROM [8] – configure oscillator [7:0] – magic byte 0xAB Write operation to this register triggers the action in CFG FPGA
0x0B8	uint32	Write one byte to I2C device on MBU power module. The whole uint32 word has to be written at a time. The bit meaning is: [31:24] – 8-bit I2C address [32:16] – register address [15:8] – data byte [7:0] – magic byte, must be 0xAB
0x0BC	uint32	Write non-zero value to disable periodic readout by CFG FPGA from MBU. This feature is used in conjunction with MMC2 programming
0x200	uint32	Writing anything to this address causes power switch on in RFFE1
0x204	uint32	Writing anything to this address causes power switch off power in RFFE1
0x208	uint32	RFFE1 LED ready control Bit[0] – red LED on/off Bit[1] – green LED on/off
0x220	uint32	Writing anything to this address causes power switch on in RFFE2
0x224	uint32	Writing anything to this address causes power switch off power in RFFE2

0x228	uint32	RFFE2 LED ready control Bit[0] – red LED on/off Bit[1] – green LED on/off
0x240	uint32	Writing anything to this address causes power switch on in RFFE3
0x244	uint32	Writing anything to this address causes power switch off power in RFFE3
0x248	uint32	RFFE3 LED ready control Bit[0] – red LED on/off Bit[1] – green LED on/off
0x260	uint32	Writing anything to this address causes power switch on in RFFE4
0x264	uint32	Writing anything to this address causes power switch off power in RFFE4
0x268	uint32	RFFE4 LED ready control Bit[0] – red LED on/off Bit[1] – green LED on/off
0x2C0	uint32	Writing anything to this address causes power switch on in COM board
0x2C4	uint32	Writing anything to this address causes power switch off power in COM board

3 User Interface



4 GPAC Booting Process

4.1 Firmware booting

The CFG FPGA firmware is responsible for booting process of the application FPGA chips present on the GPAC board. The application FPGA chips form a JTAG chain connected to CFG FPGA as presented in Fig. 4.1.

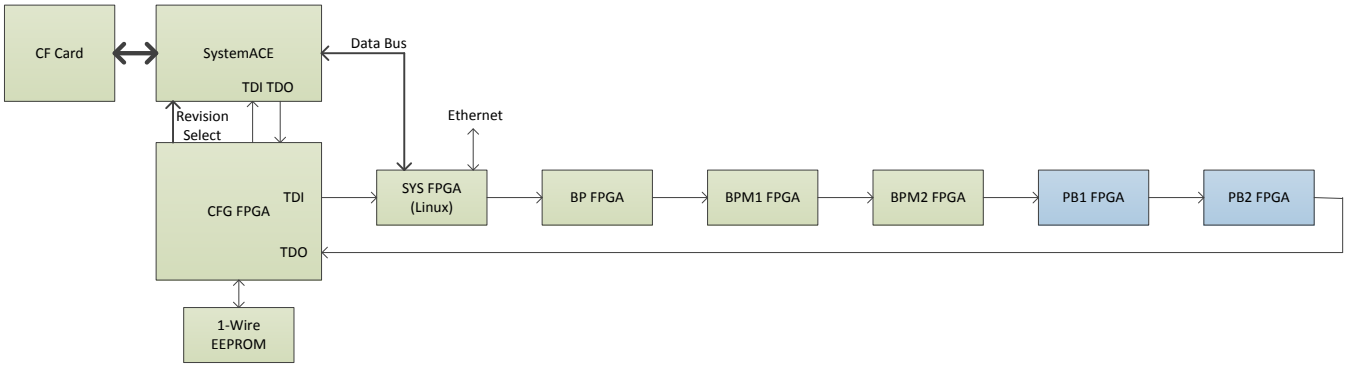


Figure 4.1. JTAG chain of FPGA chips on GPAC board

The blue FPGA chips PB1 and PB2 FPGA are optional and are located on the mezzanine cards mounted on 500-pin connectors. The FPGA chips are programmed by Xilinx SystemACE chip using JTAG interface. The SystemACE loads FPGA configuration from ACE file located on the Compact Flash (CF) card connected to the SystemACE. The CF card can contain several configuration files and the SystemACE can manage up to eight revisions. The revision number which is used by SystemACE is managed by CFG FPGA firmware. Currently the CFG FPGA firmware uses three revisions which allows for management of firmware updates and emergency configuration in case the firmware update failed. The revision number which is used by CFG FPGA during booting process is stored in 1-Wire EEPROM connected to CFG FPGA. The three configurations are organized in a folder and file structure on the CF card as presented in table 4.1. The content of the CF card can be updated remotely by FTP server running on SYS FPGA.

Table 4.1. Firmware revision folder structure

/mnt/cf/	Root folder of the CF card mounted in PetaLinux
xilinx.sys	Xilinx configuration file for SystemACE – do not edit this file
fpga/	Folder with three revisions
golden/	Revision 0 folder
golden.ace	Golden configuration which is a backup solution if prod1 and prod2 revision does not work. Never update this file remotely.
prod1/	Revision 1 folder
<project>.ace	Project dependent configuration file.
prod2/	Revision 2 folder
<project>.ace	Project dependent configuration file.

For regular operation the CFG FPGA should configure the GPAC board using prod1 or prod2 revision. The prod1 and prod2 revisions are interchangeable and they are used for

firmware update. If one revision is currently used the other one can be updated remotely. When the corresponding control software is ready for the new revision, the control software should change the revision number and it will be used after next reboot.

In case the new revision does not work, the CFG FPGA loads the golden image from revision 0. This file must not be updated remotely so that it can never be corrupted. The golden image contains configuration only for SYS FPGA with limited Linux functionality giving access to CF card from remote host over FTP server running on SYS FPGA.

When the FPGA configuration is successfully loaded the CFG FPGA tells the SYS FPGA the revision number and the SYS FPGA loads corresponding image file of the Linux. After successful boot of the Linux the SYS FPGA sends acknowledge to the CFG FPGA that the Linux is ready. If the acknowledge does not arrive to the CFG FPGA within 6 minutes the CFG FPGA loads golden image. The boot algorithm of CFG FPGA is presented in figure 4.

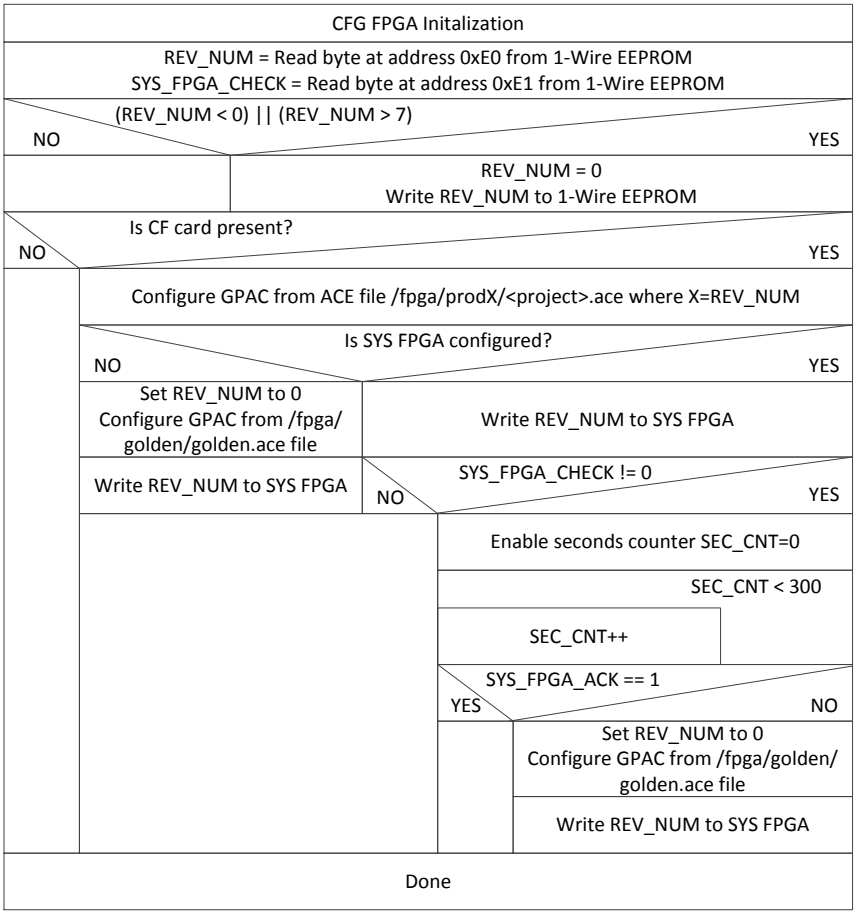


Figure 4.2. Booting algorithm running in CFG FPGA.

4.2 Proposal for complementary mechanism for firmware booting and updates in DOOCS server.

4.2.1 Firmware version check

After the firmware has started the corresponding DOOCS servers will start communication with GPAC board. It is very important for the DOOCS server to check which firmware revision is currently loaded in order to start the right version of the DOOCS server. Otherwise the behavior

of the DOOCS server and the firmware may be unpredictable. Therefore the DOOCS server should start at the very beginning only the part communicating with the CFG FPGA and it should check the actually loaded firmware revision number under address 0x884 (see section 2.2). If the revision number is 0 (the golden image) the DOOCS server must not start any BPM server because there is no BPM firmware in BPM1 and BPM2 FPGA. If the revision number is 1 or 2, then the DOOCS server may start the corresponding BPM servers.

4.2.2 Firmware and DOOCS server update

Firmware update can be done by using revision 1 (prod1) and revision 2 (prod2). It is very important that the firmware and DOOCS server updates are done at the same time in order to keep consistency of the firmware and the control software. For example the running revision is number 1 with corresponding DOOCS server. When PSI makes firmware update then PSI checks which revision is currently running and makes update of the other one (in this case revision 2). Then PSI informs DESY about the firmware update and provides corresponding documentation with implemented changes. Then DESY implements the necessary changes in DOOCS server. When DOOCS server is ready then DESY decides when the update should be applied. During update DESY selects new revision (in this case revision 2) for the next boot by programming address 0x084 register in CFG FPGA (see section 2.3) and prepares new DOOCS server for operation. Then DESY reboots GPAC boards and simultaneously restarts DOOCS server. If the firmware revision 2 was successfully loaded the DOOCS server starts the corresponding new BPM DOOCS server. If the revision 2 was not loaded successfully then the CFG FPGA will load revision 0 (golden image) and the DOOCS server can set back revision 1 in CFG FPGA to keep the BPM running. Then the update procedure can be safely repeated.