IBFB Kicker Attenuator Fan Controller

Ibfb_kick_cool_mon
Revision 1.1

Firmware Data Sheet

PSI, 14.07.2016

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Introduction

The E-XFEL IBFB system controls the beam position by means of kickers. Each kicker's output is connected to an attenuator, so that the signal has a level small enough to be measured with ordinary instruments. The attenuators are cooled by means of an *ebmpapst DV4112/NP-201* fan (cfr. [1]). Each fan has a power on wire, a PWM wire to control its speed and a TACHO output to monitor its speed. These wires are accessible via a RJ45 connector (one per fan). The IBFB kicker cooler monitor component (IKCM) can control and monitor up to 8 independent RJ45 interfaces. The core is meant to be instantiated in the BP FPGA of a GPAC2 board [2]. It is controlled via PLB bus and each serial interface is connected to the board's P2 connector and, through this, to a Rear Transition Module (RTMG_8SFP_8RJ [3]) that provides up to 8 RJ45 connectors. The interconnection of the various components is shown in

Figure 1.

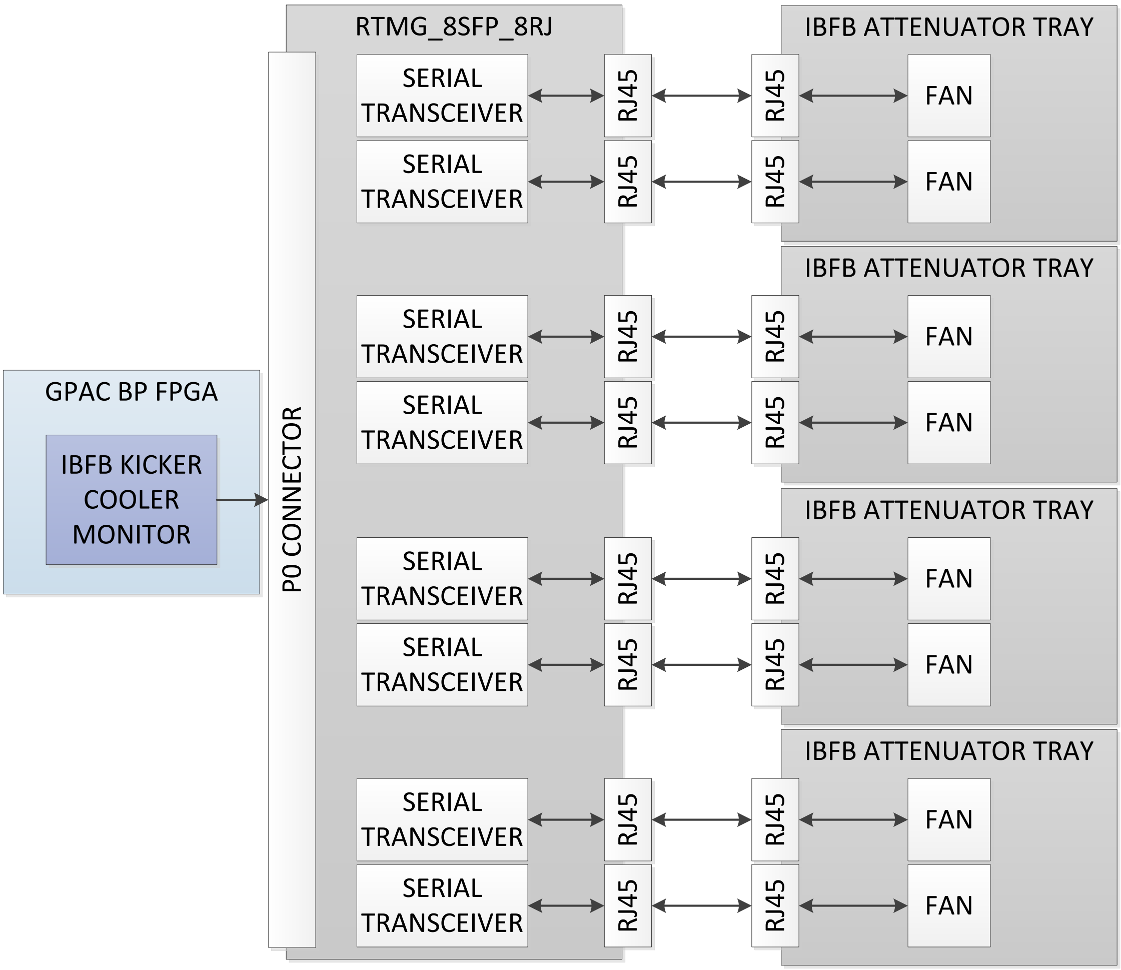

Figure 1 - Interconnection between the IKCM controller and the fan trays.

1.1 Features

The IKCM has the following properties:

- PLB register interface for command and control
- Tested up to 62.5 MHz PLB clock frequency
- Control up to 8 fans via 2kHz PWM.

- Monitor TACHO signal for up to 8 fans

1.2 Definitions, acronyms, and abbreviations

FPGA	Field Programmable Gate Array
IKCM	IBFB Kicker Cooler Monitor
PLB	Processor Local Bus (by IBM)
GPAC	Generic PSI ADC Carrier

1.3 References

[1] "DV4112/2NP-201", *Product Data Sheet,* 05.07.2012, ebmPapst.
[2] "Generic PSI ADC Carrier, VME64x FPGA Carrier Board for High Speed Mezzanines", *Datasheet*, Board Rev. 2.1, 12.07.2013.
[3] "RTMG_8SFP_8RJ", *Hardware Design Description*, Rev.1, 06.08.2015.
[4] "LTC2847 Software-Selectable multi protocol transceiver", Datasheet, Linear Technology.

1.4 History

Revision	Date	Author	Description
1.0	15.07.2016	A. Malatesta	First release
1.1	19.07.2016	A. Malatesta	Corrected error in Table 3 (RPM computation)

2 Firmware Description

The IKCM was implemented in pure VHDL. It does not contain any device specific primitive, therefore its portability is high. The IKCM component is wrapped in a Xilinx EDK pcore with slave PLB interface, but its core logic is also available as an independent VHDL component.

2.1 Architecture

The pcore consists of a parallel bank of controllers (the number of channels is selectable with a parameter). A PLB slave controller allows the access to a register bank for command and control. The block diagram is shown in Figure 2.

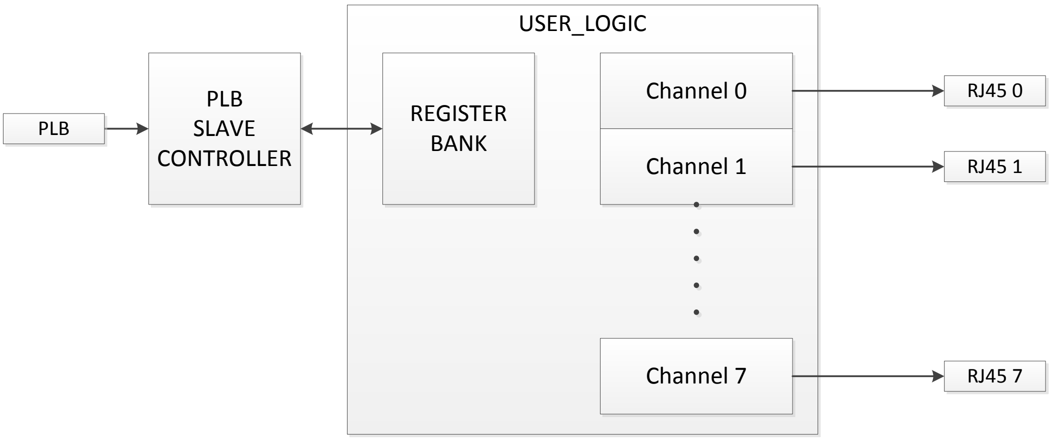

Figure 2 - Block diagram of the IKCM firmware

2.2 Ports and Attributes

Figure 3 contains component overview with ports and attributes. The table 1 and 2 describe the meaning of port and attributes.

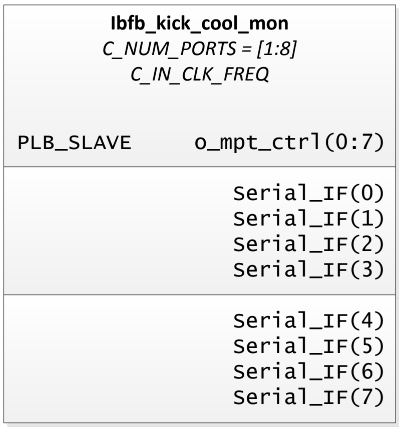

Figure 3 - Top entity of the ibfb_kick_cool_mon component.

Table 1 - Port description of ibfb_kick_cool_mon

Port name	In/Out	Type	Description
PLB_SLAVE	in	BUS	PLB slave bus (non bursting) used to access local register bank for command and control purposes. PLB bus clock is used to drive all the logic in the core.
Following signals are repeated for each channel			
o_if_m	out	std_logic_vector(2:0)	Mode bits for the multi-protocol transceiver chip [4] on the rear-transition-module [3]. Hardwired to “000” to select V.11 mode.
o_if_dce	out	std_logic	DCE bit for the multi-protocol transceiver chip [4] on the rear-transition-module [3]. Hardwired to ‘1’ to set the transceiver to use 3 TX lines and 1 RX line.
o_if_pull_src	out	std_logic	RJ45 interface: fan enable signal. Hardwired to 1.
o_if_pwm	out	std_logic	RJ45 interface: fan speed control (2 kHz PWM). The duty cycle is controllable via PLB register.
o_if_d3	out	std_logic	RJ45 interface: transceiver’s unused input pin. Hardwired to 0.
i_if_tacho	in	std_logic	RJ45 interface: TACHO signal from FAN.

Table 2 - Attribute list.

Attribute Name	Type	Description
C_NUM_PORTS	Integer	Number of RJ45 interfaces to be controlled. Allowed range 1 to 8.
C_IN_CLK_FREQ_HZ	Integer	Frequency of the PLB clock, expressed in Hz. Used to count time and generate correct PWM frequencies.

2.3 PLB Register map

The PLB register map is shown in Table 3 below. Each register is 32-bit wide. Addressing is bytewise. Parameters are read-write unless specified as read-only.

Table 3 - PLB register map

PLB Address offset	Bit range	Description
0x0	27:0	FW_VERSION: Firmware version (currently 0x3). Read-only.
0x0	31:28	N_PORTS: Number of channels available (same as parameter C_NUM_PORTS). Read-only.
0x4	31:0	CLK_FREQ_HZ: PLB clock frequency in Hz. Same as parameter C_IN_CLK_FREQ_HZ. Read only.
Channel N		
(N*0x8)+0x8	0	CHANNEL RESET. Level-sensitive: when ‘1’ channel is kept under reset.
(N*0x8)+0x8	14:8	CHANNEL PWM. PWM duty cycle expressed in percent. Allowed range 0 to 100 (unsigned integer).
(N*0x8)+0xC	31:0	CHANNEL TACHO PERIOD. Time needed for a whole fan revolution. Expressed in PLB clock cycles. Revolutions Per Minute (RPM) for fan <n> is calculated as: *RPM(n) = 60*CLK_FREQ_HZ/TACHO_PERIOD(n)*

2.4 Functional description

The core is meant to be used to control the speed of up to 8 fans connected via RJ45 cable. The PWM can be set independently for each fan. Each channel interface is implemented as an independent component and has the structure shown in Figure 4.

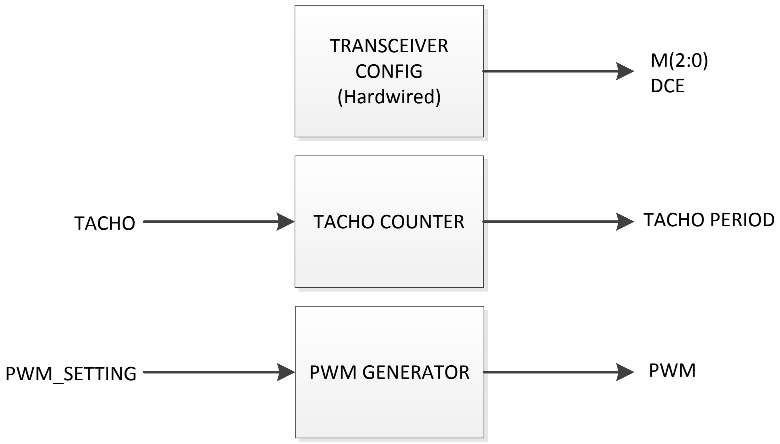

Figure 4 - Architecture of the controller for a single channel.

Each channel sets its transceiver to a fixed configuration (Single ended V.28 with 2 transmitters and 2 receivers).

The TACHO COUNTER measures the time between rising edges in the TACHO signal. The value is then multiplied by 2 (since the TACHO generates 2 pulses per revolution) and output as the TACHO PERIOD. If no edge is detected for more than 250 ms, the TACHO PERIOD value is forced to 0xFFFFFFFF.

The PWM generator produces a variable duty cycle 2 kHz periodic signal. This is done using 2 counters: the Percent Counter and the Duty-Cycle Counter The Percent Counter measures 1/100 of the 2 kHz period (500 µs / 100 = 1 µs). The Duty-Cycle Counter is incremented every time the Percent Counter expires, and counts from 1 to 100. The PWM signal is set high when the Duty-Cycle Counter is less than the set PWM, and low otherwise.

2.5 FPGA Resources

Table 4 - Resources use

Version	Flip Flops	LUTs	LUTRAMs	BRAM
Virtex-5, 8 channels (with PLB Slave)	2141	2183	0	0

2.6 Design constraints

The core has no specific constraints.