European XFEL Intra-train Beam Based Feedback Manual

Revision 1.1
PSI, Villigen, 06.09.2016

Content

1 Introduction

The E-XFEL IBFB…

1.1 Purpose

The aim of this document is to provide a global overview of the measurement technique and to describe the user interface to the GPAC firmware and software.

1.2 Scope

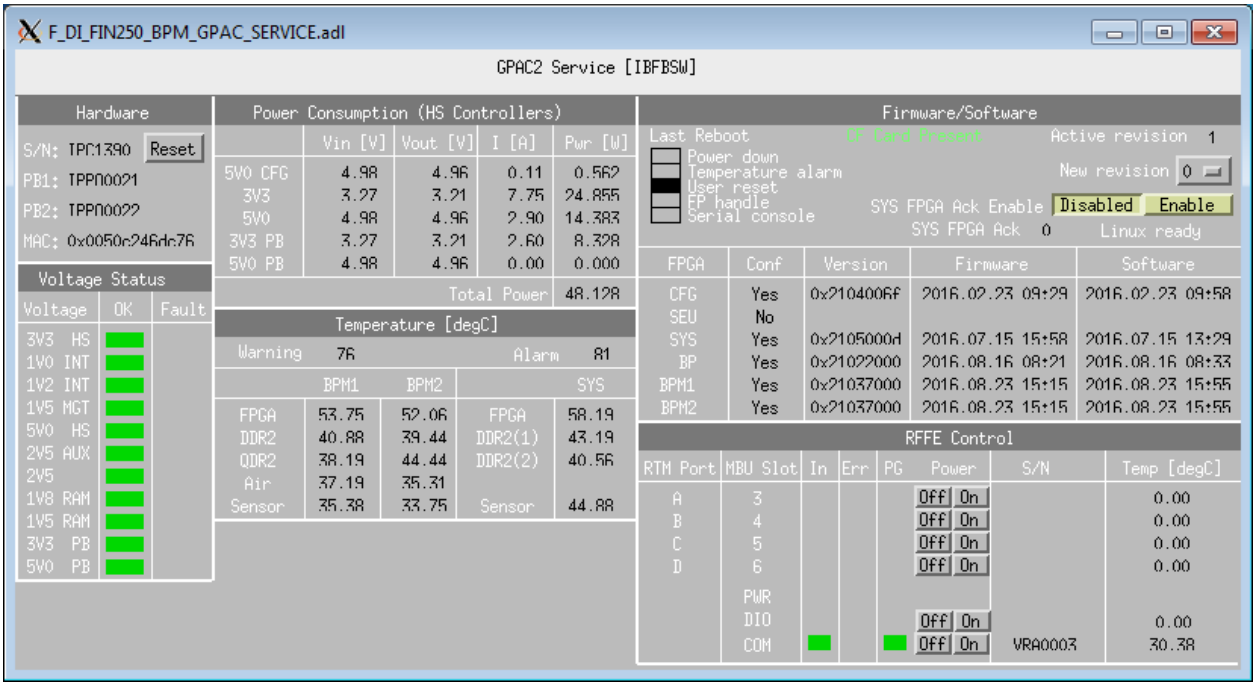
This document provides a global overview of the IBFB system and specifies the user interface. This document is a starting point which links to the detail information in the implementation in hardware, firmware and/or software.

1.3 History

Revision	Date	Author	Description
1.0	04.01.2016	W. Koprek	DAC16HL console operation
1.1	06.09.2016	W. Koprek	EPICS records description

1.4 Firmware and Software Version

This document is valid for the firmware and software version presented in the screen shot in Fig 1.1.



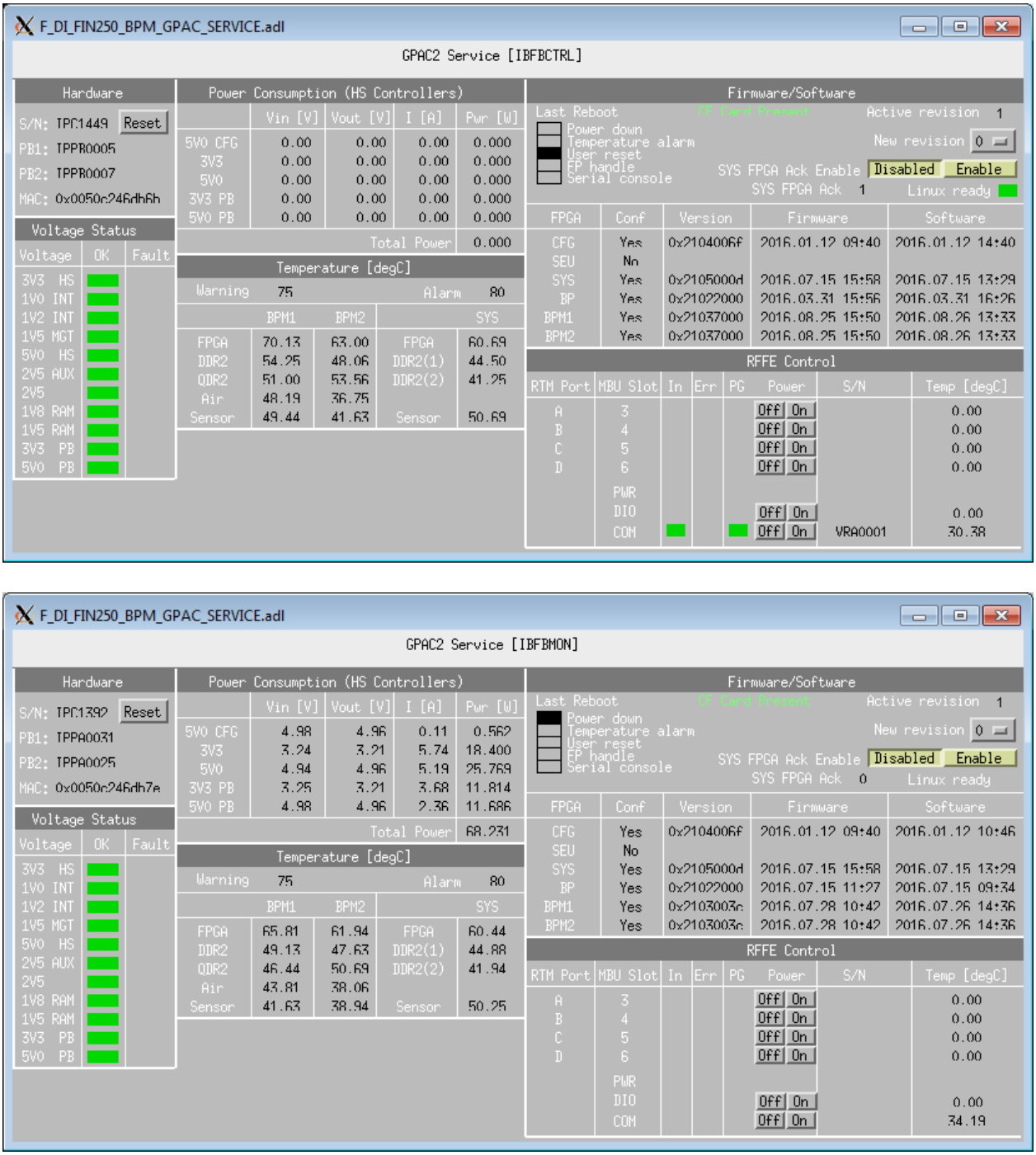


Figure 1.1. Screen shot of the EPICS panel with firmware and software version.

1.5 Definitions, acronyms, and abbreviations

This document is based on the “IEEE Recommended Practice for Software Requirements Specifications” [1].

ADC	Analog Digital Converter.
ADC12FL	GPAC piggyback with eight 12-bit ADCs
BPM	Beam Position Monitor. Usually measures the transversal beam bunch position and the bunch charge.

DAC16HL	GPAC piggyback with four 16-bit DACs
FPGA	Field Programmable Gate Array. Programmable logic device.
I2C	see IIC
IIC	IIC or I²C (Inter Integrated Circuit bus) is a multi-master serial bus defined / specified by Philips.
MPLB	PLB Master
PLB	IBM Processor Local Bus
PPC	PowerPC (Performance optimization with enhanced risc Performance Computing) is a RISC architecture created by an alliance of big companies Apple/IBM/Motorola.
QSFP	GPAC piggyback with quad SFP cage.
RTM	Rear transition card. Sometimes called “Transition Card”
RTMG	Rear transition card for GPAC.
SFP	Small form-Factor Pluggable is a compact, hot-pluggable multi-gigabit optical or/and electrical transceiver interface.
SPLB	PLB Slave

1.6 References

[1] “BPM packet router for IBFB” – Firmware Data Sheet, ibfb_bpm_router, Revision 1.0
[2] “IBFB Switch” – Firmware Data Sheet, ibfb_switch, Revision 2.1
[3] “IBFB Kicker Attenuator Fan Controller” – Firmware Data Sheet, ibfb_kick_cool_mon, Revision 1.1
[4] “European XFEL Timing System Receiver” – Firmware Data Sheet, xfel_timing, Revision 2.0
[5] “CFG FPGA Firmware in GPAC 2.1” – Firmware Data Sheet, Revision 1.8
[6] “IBFB packet player” – Firmware Data Sheet, ibfb_player, Revision 1.0
[7] “European X-Ray FEL Transverse Intra Bunch Train Feedback System” – Conceptual and Technical Design Report

1.7 Bytes and Bits Indexing Convention

The convention for indexing bytes and bits within a 32-bit word is as presented in Fig. 2. This convention is valid for the whole document.

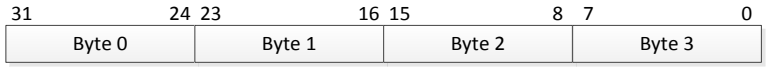


Figure 1.2. Byte and bit convention

2 System Overview

2.1 Hardware Overview

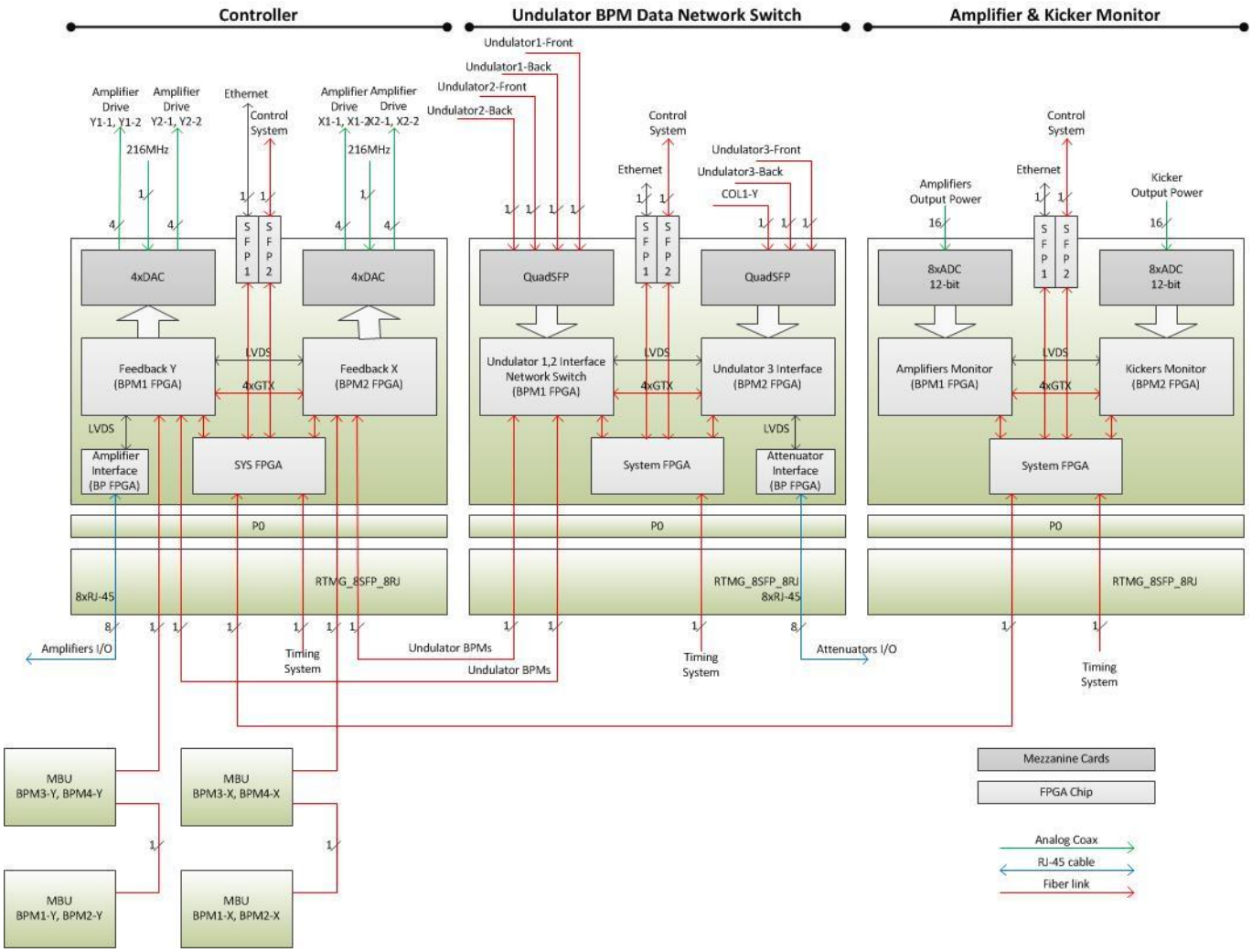


Figure 2.1: Block diagram of the IBFB hardware

2.1.1 GPAC Configurations and Interfaces

The IBFB hardware consists of the following components:

- three GPAC boards each in different piggyback configuration
- two piggybacks with four 16-bit DACs (DAC16HL)
- two piggybacks with eight 12-bit ADCs (ADC12FL)
- two quad SFP piggybacks (QSFP)
- three rear transition modules for GPAC (RTMG)

The three pairs of the piggybacks are installed on three GPAC boards. The GPAC configuration with two DAC16HL piggybacks is called IBFB controller. The configuration with two QSFP piggybacks is called IBFB switch, and the GPAC with two ADC12FL is called IBFB monitor. Each GPAC board has corresponding RTMG which provides eight interfaces for optical links and eight RJ45 connectors for electrical interfaces. Each GPAC configuration is described in the following subsections.

2.1.1.1 Common Interfaces

There are three common interfaces which are present in every GPAC configuration:

- Ethernet – this interface is connected to the SFP1 cage on the front panel of the GPAC. It uses copper SFP for connecting a patch cable. The Ethernet interface is used by Linux running on GPAC and it is used as a maintenance interface.
- DOOCS interface is a fiber link connected to SFP2 cage on the front panel of the GPAC. This interface is used to operate GPAC function from DOOCS control system. This is the main interface used for operation.
- Timing interface is a fiber link connected to E-XFEL timing system. This interfaces works only as a receiver of the timing stream. It is connected to RTMG to port SYS-1.

2.1.1.2 IBFB Controller

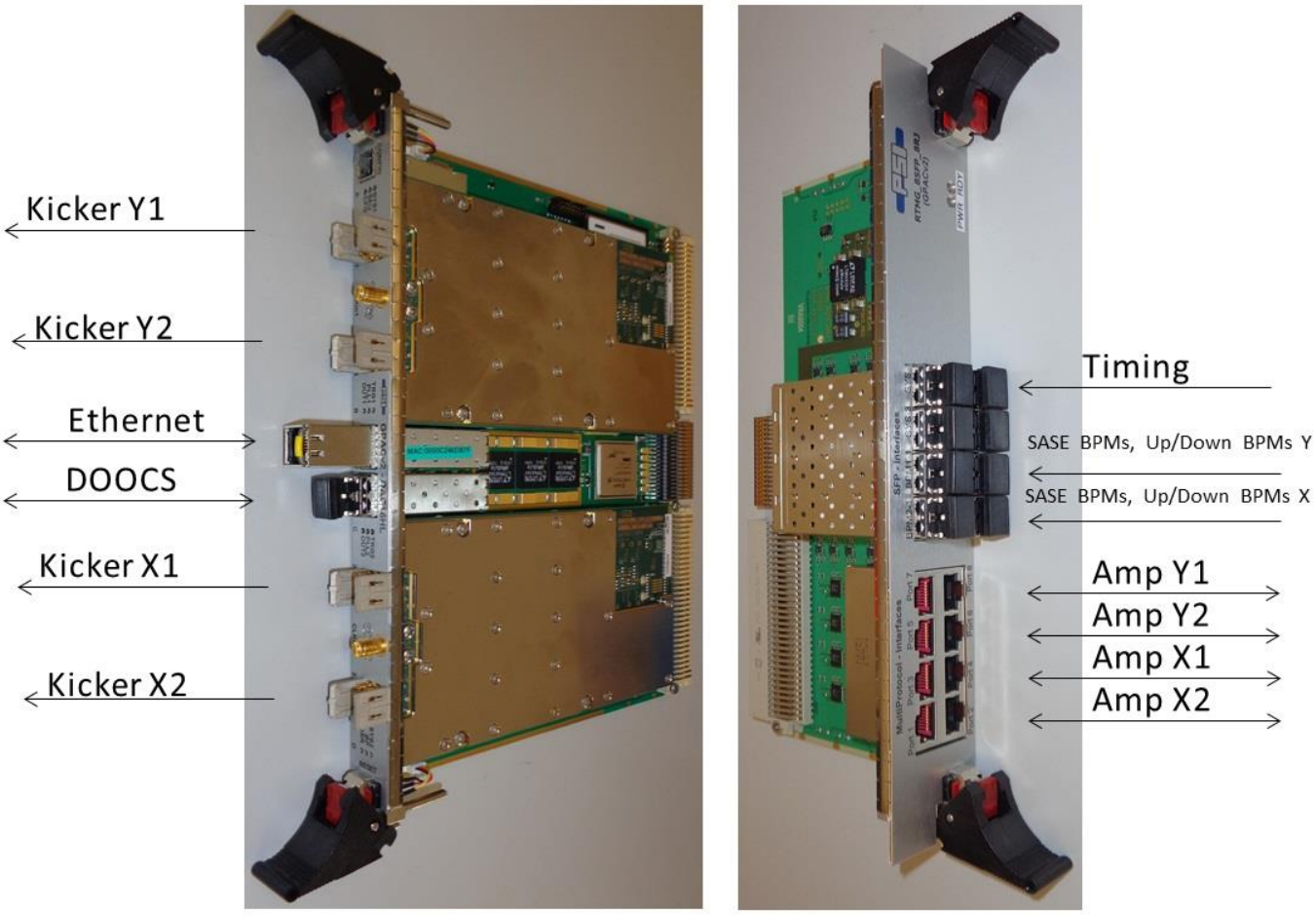


Figure 2.2: GPAC with two DAC16HL piggybacks and an RTMG

2.1.1.3 IBFB Undulator Network Switch

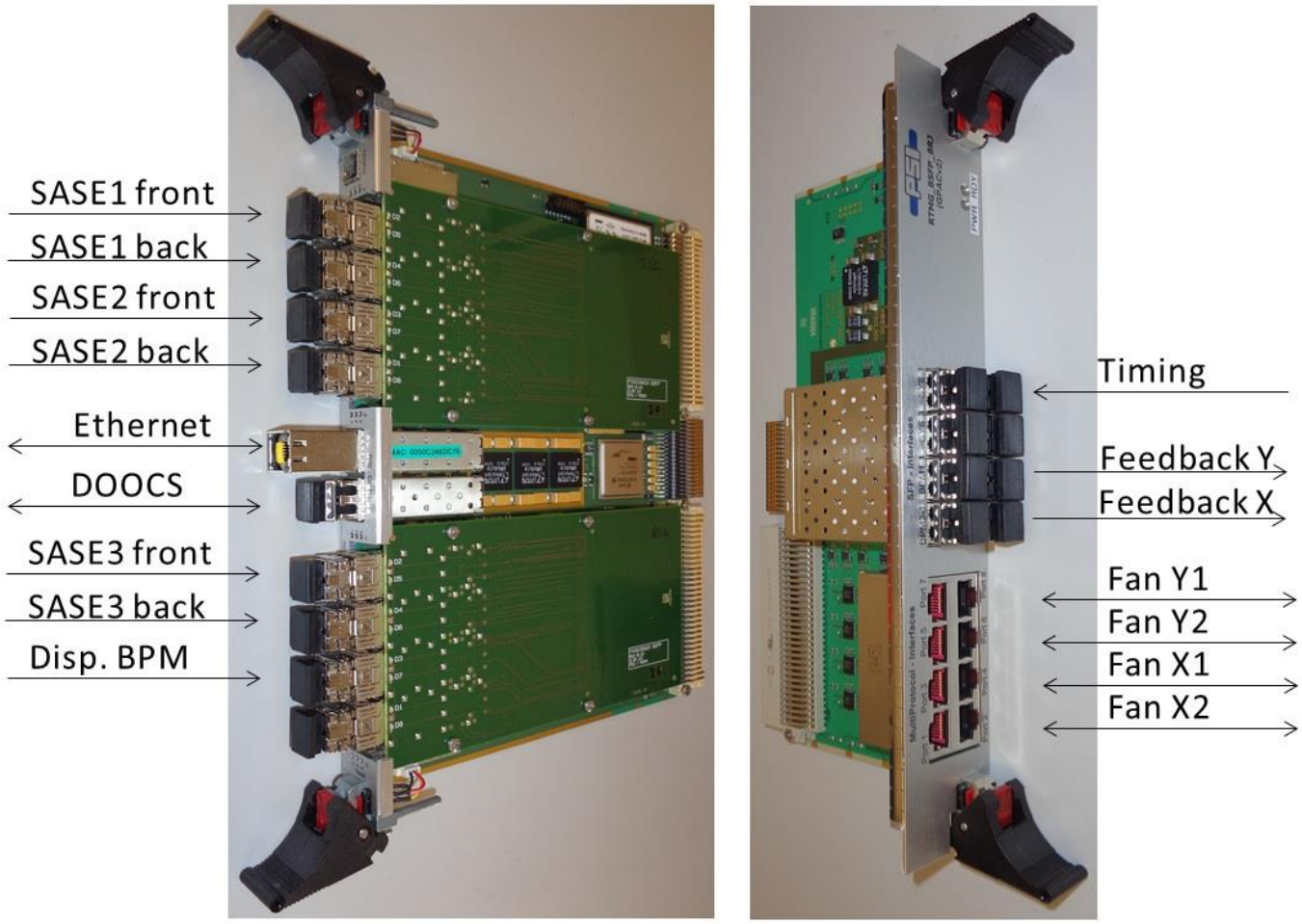


Figure 2.3: GPAC with two QSFP piggybacks and an RTMG

2.1.1.4 IBFB Monitoring

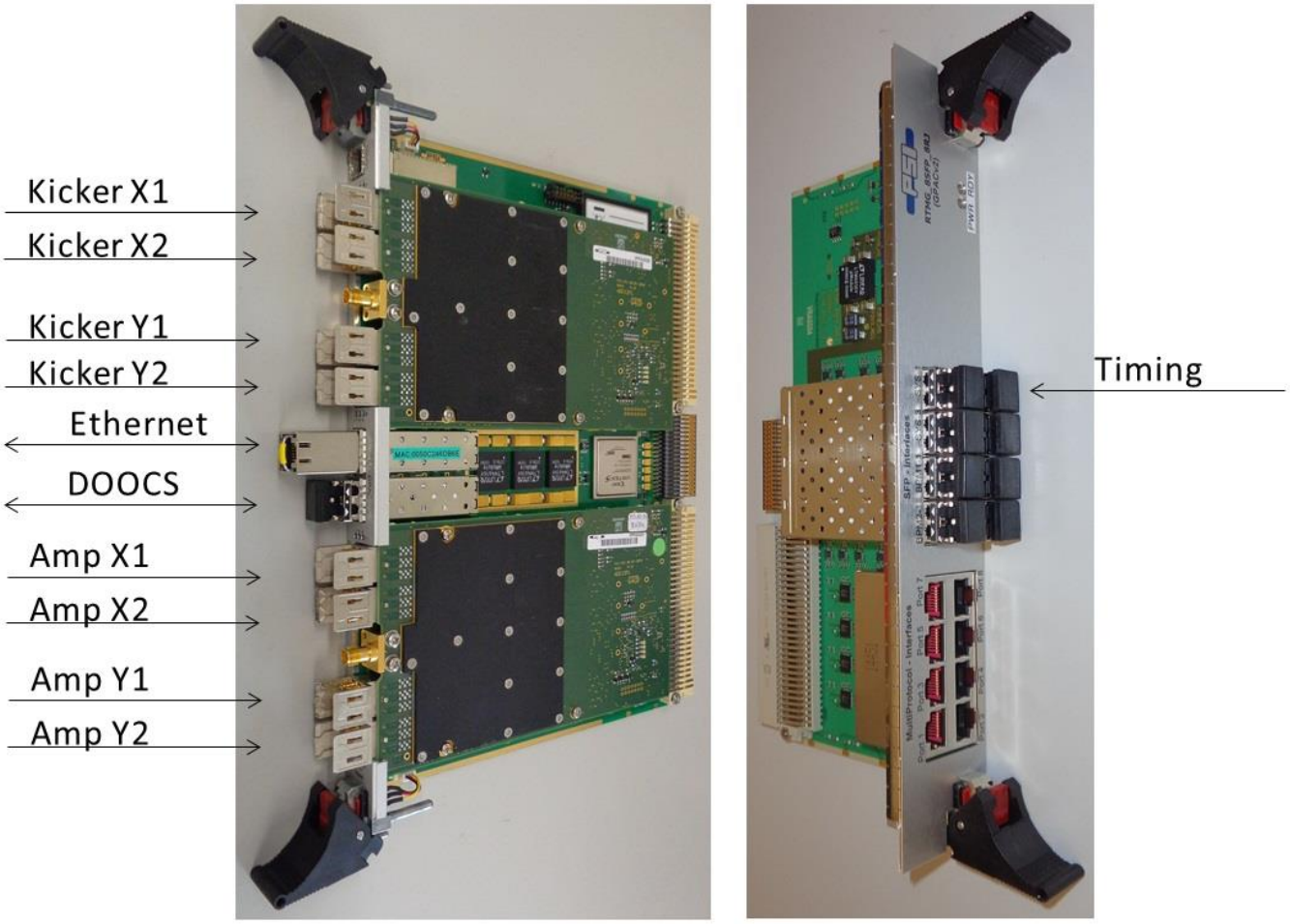


Figure 2.4: GPAC with two ADC12FL piggybacks and an RTMG

2.1.2 IBFB Installation in a VME Crate

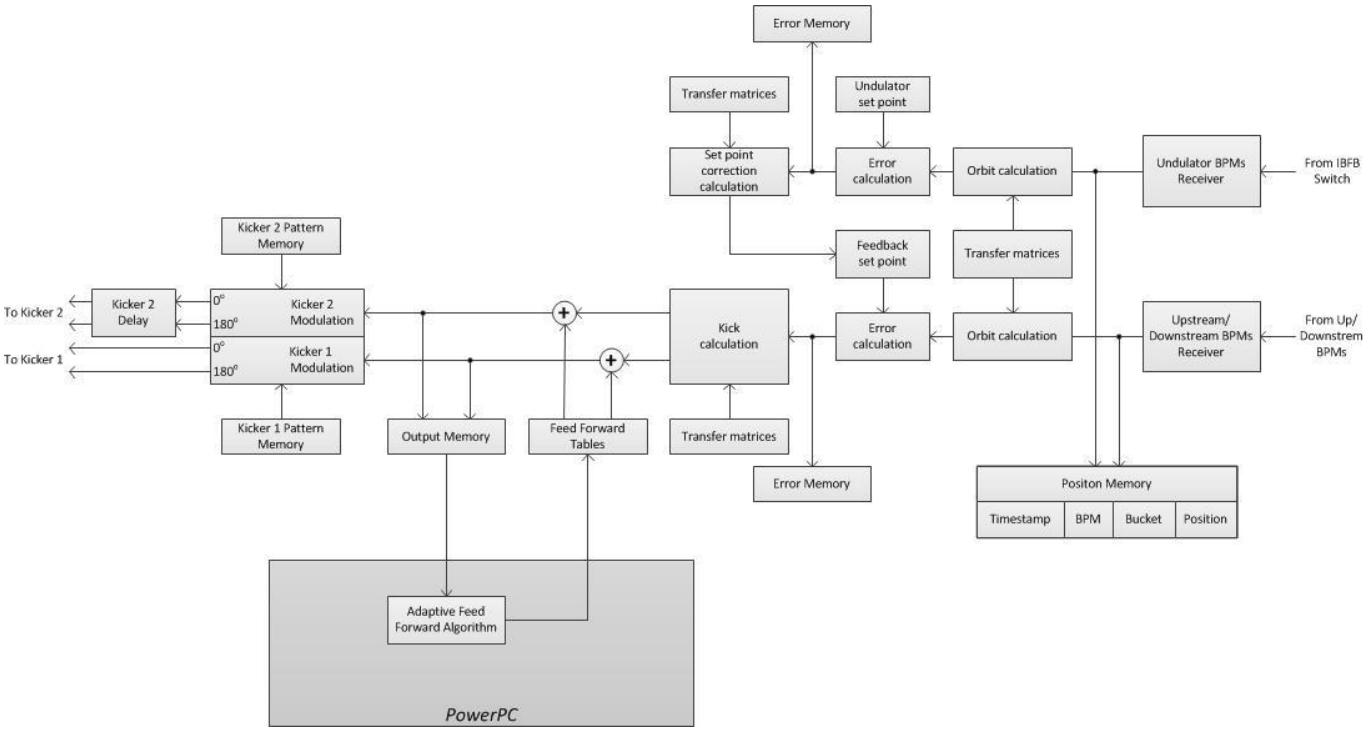
Figure 2.5: IBFB hardware installed in a VME crate – front side

Figure 2.6: IBFB hardware installed in a VME crate – rear side

2.2 Firmware Overview

3 IBFB Controller

3.1 Firmware Overview



3.2 Orbit calculation

The following formula calculates beam orbit based on position measurement from two BPMs. The beam orbit at location of these BPMs is $B_1 = \begin{bmatrix} b_1 \\ b_1' \end{bmatrix}$, and $B_2 = \begin{bmatrix} b_2 \\ b_2' \end{bmatrix}$ and known transfer matrix between these two BPMs, $M_{B1B2} = \begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix}$.

The relation between orbits at these two BPMs is

$$\begin{bmatrix} b_2 \\ b_2' \end{bmatrix} = M_{B1B2} * \begin{bmatrix} b_1 \\ b_1' \end{bmatrix} \quad (3.1.1)$$

We know the M_{B1B2} from the machine lattice, and the $b_1$and b_2 are measured. In order to calculate b_1' and b_2' we need to transform the equation (3.1.1) to

$$\begin{bmatrix} b_1' \\ b_2' \end{bmatrix} = M^o_{B1B2} * \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}$$

where matrix M^o_{b1b2} has the following coefficients

$$M^o_{b1b2} = \begin{bmatrix} -\frac{m_{11}}{m_{12}} & \frac{1}{m_{12}} \\ \frac{m_{12}*m_{21}-m_{22}*m_{11}}{m_{12}} & \frac{m_{22}}{m_{12}} \end{bmatrix}$$

The above formulas are valid both for x and y planes. The coefficients of the matrix $M^o_{b1b2}$are constant for given beam energy and can be calculated in software. The beam orbit at given location requires two multiplications and one addition per location.

3.3 Correction Algorithm

3.4 Case Studies

3.4.1 Case 1: Downstream BPMs. All components in drift space

The simplest case when all IBFB components are in a drift space. The feedback uses downstream BPMs and the set point orbit is defined at BPM2.

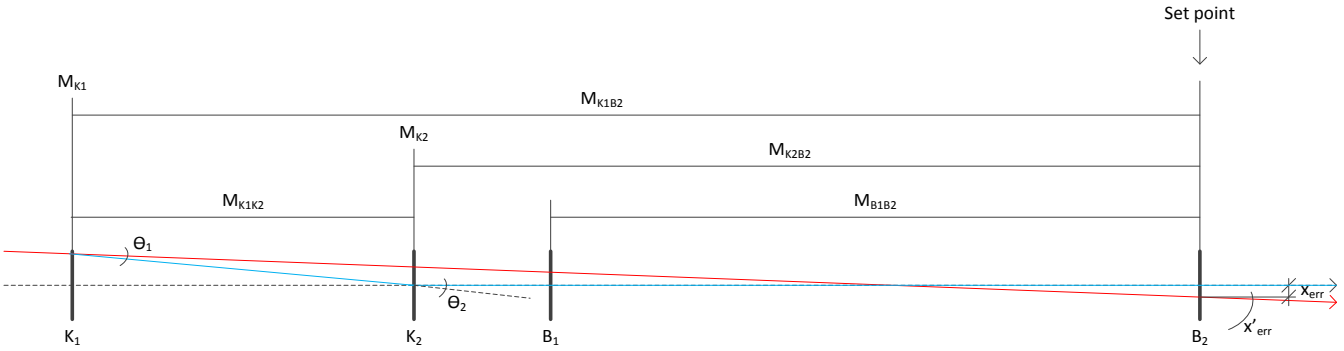


Figure 3.1 Schematic representation of IBFB components with marked transfer matrices

The generic transport matrix for drift space is $M_{s0s1} = \begin{bmatrix} 1 & L \\ 0 & 1 \end{bmatrix}$ where L is a distance between s_0 and s_1. Hence the transfer matrices necessary for further calculations are the transfer matrix from the first kicker to the second one

$$K_{2U} = M_{K1K2} * K_{1D}$$
$$\begin{bmatrix} k_{2U} \\ k'_{2U} \end{bmatrix} = \begin{bmatrix} 1 & L_{K1K2} \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} k_{1D} \\ k'_{1D} \end{bmatrix}$$

and from the second kicker to BPM B_2

$$B_2 = M_{K2B2} * K_{2D}$$
$$\begin{bmatrix} b_2 \\ b'_2 \end{bmatrix} = \begin{bmatrix} 1 & L_{K2B2} \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} k_{2D} \\ k'_{2D} \end{bmatrix}$$

where $\begin{bmatrix} k_{2U} \\ k'_{2U} \end{bmatrix}$ is the orbit at the upstream side of the second kicker, and $\begin{bmatrix} k_{1D} \\ k'_{1D} \end{bmatrix}$, $\begin{bmatrix} k_{2D} \\ k'_{2D} \end{bmatrix}$ are the orbits at the downstream side of the kicker one and two.

Assuming the kicker is a perfect device, which only changes the beam angle then its transfer matrix looks like

$$K = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & m_{23} \\ 0 & 0 & 1 \end{bmatrix}$$

where $m_{23} = \theta_K$ and it is the beam angle change caused by the kicker. The third row and column in this matrix was added for simplification of the matrix calculations.

In case when kickers are off the total transfer matrix from the upstream side of kicker one to the second downstream BPM is

$$B_2 = M_{K1K2} * M_{K2B2} * K_{1U} \qquad (3.3.1.1)$$

which is

$$B_2 = \begin{bmatrix} b_2 \\ b_2' \end{bmatrix} = \begin{bmatrix} 1 & L_{K2B2} \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & L_{K1K2} \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} k_{1U} \\ k_{1U}' \end{bmatrix} = \begin{bmatrix} k_{1U} + k_{1U}' * (L_{K1K2} + L_{K2B2}) \\ k_{1U}' \end{bmatrix} \quad (3.3.1.2)$$

When the kickers are on the total transfer matrix is extended by two kicker transfer matrices

$$B_2 = M_{K1} * M_{K1K2} * M_{K2} * M_{K2B2} * K_{1U} \qquad (3.3.1.3)$$

which is

$$B_2 = \begin{bmatrix} b_2 \\ b_2' \\ 1 \end{bmatrix} = \begin{bmatrix} 1 & L_{K2B2} & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & \theta_{K2} \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & L_{K1K2} & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & \theta_{K1} \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} k_{1U} \\ k_{1U}' \\ 1 \end{bmatrix}$$

and after matrix multiplication we obtain

$$B_2 = \begin{bmatrix} \theta_{K1} * (L_{K1K2} + L_{K2B2}) + \theta_{K2} * L_{K2B2} + k_{1U} + k_{1U}' * (L_{K1K2} + L_{K2B2}) \\ \theta_{K1} + \theta_{K2} + k_{1U}' \end{bmatrix} \quad (3.3.1.4)$$

If the $B_2 = B_{2M}$ from equation 3.1.1.2 is the measured beam orbit without correction and the $B_2 = B_{2SP}$ from equation 3.1.1.4 is the set point orbit achieved by active kickers then the difference of both gives the orbit error

$$B_{2ERR} = B_{2SP} - B_{2M}$$

then the difference of these two matrices gives

$$B_{2ERR} = \begin{bmatrix} b_{2ERR} \\ b_{2ERR}' \end{bmatrix} = \begin{bmatrix} \theta_{K1} * (L_{K1K2} + L_{K2B2}) + \theta_{K2} * L_{K2B2} \\ \theta_{K1} + \theta_{K2} \end{bmatrix} = \begin{bmatrix} L_{K1K2} + L_{K2B2} & L_{K2B2} \\ 1 & 1 \end{bmatrix} * \begin{bmatrix} \theta_{K1} \\ \theta_{K2} \end{bmatrix}$$

$$\begin{bmatrix} b_{2ERR} \\ b_{2ERR}' \end{bmatrix} = M_{corr} * \begin{bmatrix} \theta_{K1} \\ \theta_{K2} \end{bmatrix}$$

From this equation we can calculate the required kick angle for both kickers which gives

$$\begin{bmatrix} \theta_{K1} \\ \theta_{K2} \end{bmatrix} = M_{corr}^{-1} * \begin{bmatrix} b_{2ERR} \\ b_{2ERR}' \end{bmatrix} = \begin{bmatrix} \frac{1}{L_{K1K2}} & -\frac{L_{K2B2}}{L_{K1K2}} \\ -\frac{1}{L_{K1K2}} & \frac{L_{K1K2} + L_{K2B2}}{L_{K1K2}} \end{bmatrix} * \begin{bmatrix} b_{2ERR} \\ b_{2ERR}' \end{bmatrix}$$

where

$$M_{corr}^{-1} = \begin{bmatrix} \frac{1}{L_{K1K2}} & -\frac{L_{K2B2}}{L_{K1K2}} \\ -\frac{1}{L_{K1K2}} & \frac{L_{K1K2}+L_{K2B2}}{L_{K1K2}} \end{bmatrix} \qquad (3.3.1.5)$$

The inversed correction matrix M_{corr}^{-1} consists of constant values for given beam energy. Hence the firmware implementation of the correction kick consists of two multiplications and one addition per kicker.

3.4.2 Case 2: Downstream BPMs. Applied real transfer matrices between feedback components.

This case is based on the case 1. The two transfer matrices M_{K1K2} and M_{K2B2} do not represent drift spaces but real matrices calculated from the accelerator lattice. The coefficients of the matrices use the following symbols

$$M_{K1K2} = \begin{bmatrix} kk_{11} & kk_{12} \\ kk_{21} & kk_{22} \end{bmatrix}$$

$$M_{K2B2} = \begin{bmatrix} kb_{11} & kb_{12} \\ kb_{21} & kb_{22} \end{bmatrix}$$

Applying the above matrices to equation (3.1.1.1) to calculate the transfer matrix from upstream side of the kicker one to BPM2 we obtain

$$M_{K1B2} = \begin{bmatrix} kb_{11} * kk_{11} + kb_{12} * kk_{21} & kb_{11} * kk_{12} + kb_{12} * kk_{22} & 0 \\ kb_{21} * kk_{11} + kb_{22} * kk_{21} & kb_{21} * kk_{12} + kb_{22} * kk_{22} & 0 \end{bmatrix}$$

$$M_{K1B2} = \begin{bmatrix} kb_{11} * kk_{11} + kb_{12} * kk_{21} & kb_{11} * kk_{12} + kb_{12} * kk_{22} & \theta_{K1} * (kb_{11} * kk_{12} + kb_{12} * kk_{22}) + \theta_{K1} * kb_{12} \\ kb_{21} * kk_{11} + kb_{22} * kk_{21} & kb_{21} * kk_{12} + kb_{22} * kk_{22} & \theta_{K1} * (kb_{21} * kk_{12} + kb_{22} * kk_{22}) + \theta_{K1} * kb_{22} \end{bmatrix}$$

Subtracting both matrices and extracting the correction angles we obtain the correction matrix

$$M_{corr} = \begin{bmatrix} kb_{11} * kk_{12} + kb_{12} * kk_{22} & kb_{12} \\ kb_{21} * kk_{12} + kb_{22} * kk_{22} & kb_{22} \end{bmatrix}$$

and the inversed correction matrix

$$M_{corr}^{-1} = \begin{bmatrix} \frac{kb_{22}}{kb_{11}*kb_{22}*kk_{12} - kb_{12}*kb_{21}*kk_{12}} & -\frac{kb_{12}}{kb_{11}*kb_{22}*kk_{12} - kb_{12}*kb_{21}*kk_{12}} \\ -\frac{kb_{21}*kk_{12} + kb_{22}*kk_{22}}{kb_{11}*kb_{22}*kk_{12} - kb_{12}*kb_{21}*kk_{12}} & \frac{kb_{11}*kk_{12} + kb_{12}*kk_{22}}{kb_{11}*kb_{22}*kk_{12} - kb_{12}*kb_{21}*kk_{12}} \end{bmatrix} \quad (3.3.2.1)$$

And again all coefficients are constant for given beam energy and can be calculated in software. Hence the firmware implementation of the correction kick consists of two multiplications and one addition per kicker.

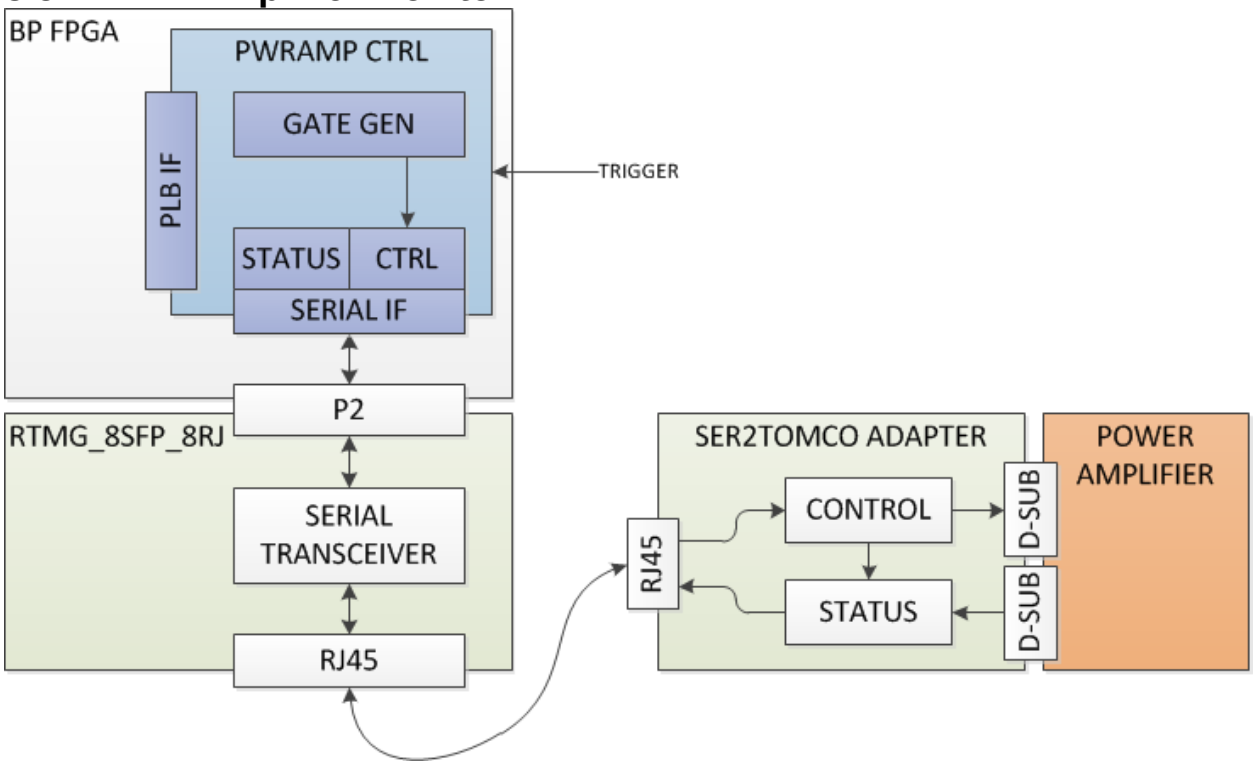
3.4.3 Case 3: Downstream BPMs. Transfer matrix from lattice. Beam energy deviation.

In this case the conditions from case 2 are considered but the transfer matrix of the kickers contains components related to energy deviation.

3.5 Firmware implementation

3.5.1 IBFB Controller

3.5.2 IBFB Amplifier Monitor



3.5.3 DAC16HL Monitor and Control

3.5.3.1 GPAC Console configuration

- Connect debug box to GPAC and to USB port in a PC.
- Check in the 'Device Manager' which COM ports were assigned to the GPAC serial ports.
- Connect with Putty to the higher number COM port. The COM parameters are 9600, 8, 1, None, XON/XOFF.
- Type in the Putty console 'u' to select FPGA chip. Select '2' for BPM1 FPGA.
- Connect with Putth to the lower number COM port. The COM parameters are 9600, 8, 1, None, XON/XOFF.

3.5.3.2 IBFB BPM FPGA Console Manual

Type 'help' for list of commands.

```
dac16hl <switch> [parameters]

switches:
v           - read back the PLL registers and verify against the
              selected configuration. Only registers with different
              content are displayed.
```

```
t           - print DAC temperatures
c <conf>    - configure PLL with configuration number <conf>. Currently
              allowed configurations are 0 and 1
w <addr> <value> - write value to selected register in PLL. Example:
              dac16hl w 0x0000 0x90
r <addr>    - read selected register from PLL
d           - reset DCMs
```

3.5.4 IBFB Controller Register Map

Address	Type	R/W	Description	MEDM
			SYS FPGA	
0x00000000	SYS FPGA Service Component			
0x000000FF				
0x00000100	XFEL Timing System Receiver (Registers) – see documentation [4] for details.			
0x000001FF				
0x00003000	CFG FPGA Access Memory – see CFG FPGA documentation for details [5].			
0x00003FFF				
0x00008000	XFEL Timing System Receiver (Memory) – see documentation [4] for details.			
0x0000FFFF				
			BP FPGA	
0x00100500	uint32	RW	Amplifiers control - reset loss of synchronization indicator. Write anything to this register to reset the indicators	203
0x00100504	uint32	RO	Amplifier status register 1 for KICK-Y1-N: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100508	uint32	RO	Amplifier status register 2 for KICK-Y1-N: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010050C	uint32	RW	Reserved. Do not write anything to this register	
0x00100510	uint32	RO	Amplifier status register 3 for KICK-Y1-N: Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator) Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	 211 216 217 218 215 214 212 213 219 220 221 222 223
0x00100514	uint32	RO	Amplifier status register 1 for KICK-Y1-P: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100518	uint32	RO	Amplifier status register 2 for KICK-Y1-P: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010051C	uint32	RW	Reserved. Do not write anything to this register	
0x00100520	uint32	RO	Amplifier status register 3 for KICK-Y1-P:	

			Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator) Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	211 216 217 218 215 214 212 213 219 220 221 222 223
0x00100524	uint32	RO	Amplifier status register 1 for KICK-Y2-N: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100528	uint32	RO	Amplifier status register 2 for KICK-Y2-N: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010052C	uint32	RW	Reserved. Do not write anything to this register	
0x00100530	uint32	RO	Amplifier status register 3 for KICK-Y2-N: Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator) Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	 211 216 217 218 215 214 212 213 219 220 221 222 223
0x00100534	uint32	RO	Amplifier status register 1 for KICK-Y2-P: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100538	uint32	RO	Amplifier status register 2 for KICK-Y2-P: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010053C	uint32	RW	Reserved. Do not write anything to this register	
0x00100540	uint32	RO	Amplifier status register 3 for KICK-Y2-P: Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator)	 211 216 217 218 215 214 212 213 219 220

			Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	221 222 223
0x00100544	uint32	RO	Amplifier status register 1 for KICK-X1-N: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100548	uint32	RO	Amplifier status register 2 for KICK-X1-N: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010054C	uint32	RW	Reserved. Do not write anything to this register	
0x00100550	uint32	RO	Amplifier status register 3 for KICK-X1-N: Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator) Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	 211 216 217 218 215 214 212 213 219 220 221 222 223
0x00100554	uint32	RO	Amplifier status register 1 for KICK-X1-P: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100558	uint32	RO	Amplifier status register 2 for KICK-X1-P: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010055C	uint32	RW	Reserved. Do not write anything to this register	
0x00100560	uint32	RO	Amplifier status register 3 for KICK-X1-P: Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator) Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	 211 216 217 218 215 214 212 213 219 220 221 222 223
0x00100564	uint32	RO	Amplifier status register 1 for KICK-X2-N: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100568	uint32	RO	Amplifier status register 2 for KICK-X2-N: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010056C	uint32	RW	Reserved. Do not write anything to this register	

0x00100570	uint32	RO	Amplifier status register 3 for KICK-X2-N: Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator) Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	 211 216 217 218 215 214 212 213 219 220 221 222 223
0x00100574	uint32	RO	Amplifier status register 1 for KICK-X2-P: Bit 29:9 – gate delay in [us]. Scaling factor is 0.016. Bit 8 – when high then gate enabled (green indicator) Bit 7:0 – link speed in [MHz]. Scaling factor 62.5/(2*(val+1))	 205 206 207
0x00100578	uint32	RO	Amplifier status register 2 for KICK-X2-P: Bit 31 – when high then loss of synchronization detected (red indicator) Bit 25:9 – gate length in [us]. Scaling factor is 0.016 Bit 8 – when high then the amplifier is connected (green indicator) Bit 7:0 – link delay expressed in clock cycles of clock 62.5MHz	 208 209 204 210
0x0010057C	uint32	RW	Reserved. Do not write anything to this register	
0x00100580	uint32	RO	Amplifier status register 3 for KICK-X2-P: Bit 31 – when high then DC power is OK (red/green indicator) Bit 30 – when high there is forward power at the amplifier output (green indicator Bit 29 – when high then there amplifier has to high temperature (green indicator) Bit 28 – when high then there was over duty in the last pulse (red indicator) Bit 25 – when high the amplifier has fault (red indicator) Bit 24 – when high the amplifier is shut down (red indicator) Bit 23 – when high then the amplifier is selected (blue indicator) Bit 22 – when high then the amplifier is enabled (green indicator) Bit 21 – when high then the amplifier was overdriven (red indicator) Bit 20 – when high then power supply 1 status is OK (green indicator) Bit 19 – when high then power supply 2 status is OK (green indicator) Bit 17 – when high then amplifier 1 status is OK (green indicator) Bit 16 – when high then amplifier 2 status is OK (green indicator)	 211 216 217 218 215 214 212 213 219 220 221 222 223
0x00104004	uint8	RW	PB1 DAC0 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00104005	uint8	RW	PB1 DAC1 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00104006	uint8	RW	PB1 DAC2 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00104007	uint8	RW	PB1 DAC3 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00104008	uint8	RW	PB1 DAC0 enable. When ‘1’ then the amplifier is enabled.	509
0x00104009	uint8	RW	PB1 DAC1 enable. When ‘1’ then the amplifier is enabled.	509
0x0010400A	uint8	RW	PB1 DAC2 enable. When ‘1’ then the amplifier is enabled.	509
0x0010400B	uint8	RW	PB1 DAC3 enable. When ‘1’ then the amplifier is enabled.	509
0x00104018	uint8	RO	External clock present (green/red indicator): =0 – missing clock <>0 – clock present	435
0x00104040	int32	RW	PB1 DAC0 amplifier common mode voltage in bits.	510
0x00104044	int32	RW	PB1 DAC1 amplifier common mode voltage in bits.	510
0x00104048	int32	RW	PB1 DAC2 amplifier common mode voltage in bits.	510
0x0010404C	int32	RW	PB1 DAC3 amplifier common mode voltage in bits.	510
0x00104050	int32	RW	PB1 DAC0 comparator reference voltage in bits.	511
0x00104054	int32	RW	PB1 DAC1 comparator reference voltage in bits.	511
0x00104058	int32	RW	PB1 DAC2 comparator reference voltage in bits.	511
0x0010405C	int32	RW	PB1 DAC3 comparator reference voltage in bits.	511
0x00104010	uint32	RO	PB1 DAC external clock level detection (red indicator): 0 – clock present 1 – no clock connected	500

0x00104018	uint32	RO	PB1 DAC PLL 1 locked (green indicator): 0 – not locked not zero – locked	501
0x0010401C	uint32	RO	PB1 DAC PLL 2 locked (green indicator): 0 – not locked not zero – locked	502
0x00106000	int32	RO	PB1 DAC0 temperature in degC. Scaling factor is 0.00390625	503
0x00106010	int32	RO	PB1 DAC1 temperature in degC. Scaling factor is 0.00390625	503
0x00106020	int32	RO	PB1 DAC2 temperature in degC. Scaling factor is 0.00390625	503
0x00106030	int32	RO	PB1 DAC3 temperature in degC. Scaling factor is 0.00390625	503
0x00108004	uint8	RW	PB2 DAC0 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00108005	uint8	RW	PB2 DAC1 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00108006	uint8	RW	PB2 DAC2 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00108007	uint8	RW	PB2 DAC3 amplifier enable. When ‘1’ then the amplifier is enabled.	508
0x00108008	uint8	RW	PB2 DAC0 enable. When ‘1’ then the amplifier is enabled.	509
0x00108009	uint8	RW	PB2 DAC1 enable. When ‘1’ then the amplifier is enabled.	509
0x0010800A	uint8	RW	PB2 DAC2 enable. When ‘1’ then the amplifier is enabled.	509
0x0010800B	uint8	RW	PB2 DAC3 enable. When ‘1’ then the amplifier is enabled.	509
0x00108018	uint8	RO	PB2 DAC External clock present (green/red indicator): =0 – missing clock <>0 – clock present	435
0x00108040	int32	RW	PB2 DAC0 amplifier common mode voltage in bits.	510
0x00108044	int32	RW	PB2 DAC1 amplifier common mode voltage in bits.	510
0x00108048	int32	RW	PB2 DAC2 amplifier common mode voltage in bits.	510
0x0010804C	int32	RW	PB2 DAC3 amplifier common mode voltage in bits.	510
0x00108050	int32	RW	PB2 DAC0 comparator reference voltage in bits.	511
0x00108054	int32	RW	PB2 DAC1 comparator reference voltage in bits.	511
0x00108058	int32	RW	PB2 DAC2 comparator reference voltage in bits.	511
0x0010805C	int32	RW	PB2 DAC3 comparator reference voltage in bits.	511
0x00108010	uint32	RO	PB2 DAC external clock level detection (red indicator): 0 – clock present 1 – no clock connected	500
0x00108018	uint32	RO	PB2 DAC PLL 1 locked (green indicator): 0 – not locked not zero – locked	501
0x0010801C	uint32	RO	PB2 DAC PLL 2 locked (green indicator): 0 – not locked not zero – locked	502
0x0010A000	int32	RO	PB2 DAC0 temperature in degC. Scaling factor is 0.00390625	503
0x0010A010	int32	RO	PB2 DAC1 temperature in degC. Scaling factor is 0.00390625	503
0x0010A020	int32	RO	PB2 DAC2 temperature in degC. Scaling factor is 0.00390625	503
0x0010A030	int32	RO	PB2 DAC3 temperature in degC. Scaling factor is 0.00390625	503
BPM1 FPGA				
0x00A00104	int8	RO	PB1 DAC0 output N comparator state	504
0x00A00105	int8	RO	PB1 DAC1 output N comparator state	504
0x00A00106	int8	RO	PB1 DAC2 output N comparator state	504
0x00A00107	int8	RO	PB1 DAC3 output N comparator state	504
0x00A00108	int8	RO	PB1 DAC0 output P comparator state	505
0x00A00109	int8	RO	PB1 DAC1 output P comparator state	505
0x00A0010A	int8	RO	PB1 DAC2 output P comparator state	505
0x00A0010B	int8	RO	PB1 DAC3 output P comparator state	505
0x00A0010C	uint8	RO	PB1 DAC0 DCM locked 0 – not locked 1 - locked	507
0x00A0010D	uint8	RO	PB1 DAC1 DCM locked 0 – not locked 1 - locked	507
0x00A0010E	uint8	RO	PB1 DAC2 DCM locked 0 – not locked 1 - locked	507
0x00A0010F	uint8	RO	PB1 DAC3 DCM locked 0 – not locked 1 - locked	507
0x00A00114	uint32	RO	PB1 DAC0 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506

0x00A00118	uint32	RO	PB1 DAC1 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506
0x00A0011C	uint32	RO	PB1 DAC2 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506
0x00A00120	uint32	RO	PB1 DAC3 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506
0x00A00124	uint32	RO	PB1 DAC0 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x00A00128	uint32	RO	PB1 DAC1 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x00A0012C	uint32	RO	PB1 DAC2 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x00A00130	uint32	RO	PB1 DAC3 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x00A00138	uint8	RO	PB1 DAC0 DCM phase shifter step from 0 to 255	516
0x00A00139	uint8	RO	PB1 DAC1 DCM phase shifter step from 0 to 255	516
0x00A0013A	uint8	RO	PB1 DAC2 DCM phase shifter step from 0 to 255	516
0x00A0013B	uint8	RO	PB1 DAC3 DCM phase shifter step from 0 to 255	516
0x00A00257	uint8	RO	External trigger missing (red indicator): =0 – trigger detected <>0 – missing trigger	417
0x00A01004	uint8	RW	Trigger source: 0 – Signal 1 – Machine trigger 2 – Auto trigger (2 s) 3 – Auto trigger (1 s) 4 – Auto trigger (0.5 s) 5 – Auto trigger (0.2 s) 6 – Auto trigger (0.1 s)	412
0x00A01005	uint8	RW	Trigger mode: 0 – Continuous 1 – Single	413
0x00A01008	uint32	RW	Delay of the first bunch with respect to the pulse trigger. Measured in clock cycles.	414
0x00A0100C	uint16	RW	Number of bunches. Now has to be set manually. Later the value comes from timing system.	415
0x00A0100E	uint16	RW	Bunch spacing in ADC clock cycles. Now has to be set manually. Later the value comes from the timing system.	416
0x00A01010	uint8	RW	PB1 DAC0 operation mode: 0 – DAC off 1 – Constant level 2 – Sinewave 3 - Squarewave 4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	512
0x00A01011	uint8	RW	PB1 DAC1 operation mode: 0 – DAC off 1 – Constant level 2 – Sinewave 3 - Squarewave 4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	512
0x00A01012	uint8	RW	PB1 DAC2 operation mode: 0 – DAC off	512

			1 – Constant level 2 – Sinewave 3 - Squarewave 4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	
0x00A01013	uint8	RW	PB1 DAC3 operation mode: 0 – DAC off 1 – Constant level 2 – Sinewave 3 - Squarewave 4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	512
0x00A01018	single	RW	PB1 DAC0 constant/waveform amplitude in [V]. Range 0-1V.	513
0x00A0101C	single	RW	PB1 DAC1 constant/waveform amplitude in [V]. Range 0-1V.	513
0x00A01020	single	RW	PB1 DAC2 constant/waveform amplitude in [V]. Range 0-1V.	513
0x00A01024	single	RW	PB1 DAC3 constant/waveform amplitude in [V]. Range 0-1V.	513
0x00A01028	single	RW	PB1 DAC0 waveform frequency in [MHz].	514
0x00A0102C	single	RW	PB1 DAC1 waveform frequency in [MHz].	514
0x00A01030	single	RW	PB1 DAC2 waveform frequency in [MHz].	514
0x00A01034	single	RW	PB1 DAC3 waveform frequency in [MHz].	514
0x00A01038	single	RW	PB1 DAC0 waveform phase in [deg] in range from -180 to 180.	515
0x00A0103C	single	RW	PB1 DAC1 waveform phase in [deg] in range from -180 to 180.	515
0x00A01040	single	RW	PB1 DAC2 waveform phase in [deg] in range from -180 to 180.	515
0x00A01044	single	RW	PB1 DAC3 waveform phase in [deg] in range from -180 to 180.	515
0x00A0105C	uint8	RW	PB1 DAC0 DCM command. The following values cause actions: 1 – increment phase by one 2 – set phase shifter to 0 steps	517
0x00A0105D	uint8	RW	PB1 DAC1 DCM command. The following values cause actions: 1 – increment phase by one 2 – set phase shifter to 0 steps	517
0x00A0105E	uint8	RW	PB1 DAC2 DCM command. The following values cause actions: 1 – increment phase by one 2 – set phase shifter to 0 steps	517
0x00A0105F	uint8	RW	PB1 DAC3 DCM command. The following values cause actions: 1 – increment phase by one step 2 – set phase shifter to 0 steps	517
BPM2 FPGA				
0x01200104	int8	RO	PB2 DAC0 output N comparator state	504
0x01200105	int8	RO	PB2 DAC1 output N comparator state	504
0x01200106	int8	RO	PB2 DAC2 output N comparator state	504
0x01200107	int8	RO	PB2 DAC3 output N comparator state	504
0x01200108	int8	RO	PB2 DAC0 output P comparator state	505
0x01200109	int8	RO	PB2 DAC1 output P comparator state	505
0x0120010A	int8	RO	PB2 DAC2 output P comparator state	505
0x0120010B	int8	RO	PB2 DAC3 output P comparator state	505
0x0120010C	uint8	RO	PB2 DAC0 DCM locked 0 – not locked 1 - locked	507
0x0120010D	uint8	RO	PB2 DAC1 DCM locked 0 – not locked 1 - locked	507
0x0120010E	uint8	RO	PB2 DAC2 DCM locked 0 – not locked 1 - locked	507
0x0120010F	uint8	RO	PB2 DAC3 DCM locked 0 – not locked 1 - locked	507

0x01200114	uint32	RO	PB2 DAC0 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506
0x01200118	uint32	RO	PB2 DAC1 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506
0x0120011C	uint32	RO	PB2 DAC2 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506
0x01200120	uint32	RO	PB2 DAC3 DCM output frequency measurement in [MHz]. Scaling factor is 0.000001	506
0x01200124	uint32	RO	PB2 DAC0 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x01200128	uint32	RO	PB2 DAC1 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x0120012C	uint32	RO	PB2 DAC2 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x01200130	uint32	RO	PB2 DAC3 DCM phase shifter state: 0x0 – phase shifter OK 0x10000 – phase shifter overflow	518
0x01200138	uint8	RO	PB2 DAC0 DCM phase shifter step from 0 to 255	516
0x01200139	uint8	RO	PB2 DAC1 DCM phase shifter step from 0 to 255	516
0x0120013A	uint8	RO	PB2 DAC2 DCM phase shifter step from 0 to 255	516
0x0120013B	uint8	RO	PB2 DAC3 DCM phase shifter step from 0 to 255	516
0x01200257	uint8	RO	External trigger missing (red indicator): =0 – trigger detected <>0 – missing trigger	422
0x01201004	uint8	RW	Trigger source: 0 – Signal 1 – Machine trigger 2 – Auto trigger (2 s) 3 – Auto trigger (1 s) 4 – Auto trigger (0.5 s) 5 – Auto trigger (0.2 s) 6 – Auto trigger (0.1 s)	417
0x01201005	uint8	RW	Trigger mode: 0 – Continuous 1 – Single	418
0x01201008	uint32	RW	Delay of the first bunch with respect to the pulse trigger. Measured in clock cycles.	419
0x0120100C	uint16	RW	Number of bunches. Now has to be set manually. Later the value comes from timing system.	420
0x0120100E	uint16	RW	Bunch spacing in ADC clock cycles. Now has to be set manually. Later the value comes from the timing system.	421
0x01201010	uint8	RW	PB2 DAC0 operation mode: 0 – DAC off 1 – Constant level 2 – Sinewave 3 - Squarewave 4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	512
0x01201011	uint8	RW	PB2 DAC1 operation mode: 0 – DAC off 1 – Constant level 2 – Sinewave 3 - Squarewave	512

			4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	
0x01201012	uint8	RW	PB2 DAC2 operation mode: 0 – DAC off 1 – Constant level 2 – Sinewave 3 - Squarewave 4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	512
0x01201013	uint8	RW	PB2 DAC3 operation mode: 0 – DAC off 1 – Constant level 2 – Sinewave 3 - Squarewave 4 - Noise 5 - Saw 6 – Doublet 7 – User pattern 8 – IBFB 9 – Test phase shift	512
0x01201018	single	RW	PB2 DAC0 constant/waveform amplitude in [V]. Range 0-1V.	513
0x0120101C	single	RW	PB2 DAC1 constant/waveform amplitude in [V]. Range 0-1V.	513
0x01201020	single	RW	PB2 DAC2 constant/waveform amplitude in [V]. Range 0-1V.	513
0x01201024	single	RW	PB2 DAC3 constant/waveform amplitude in [V]. Range 0-1V.	513
0x01201028	single	RW	PB2 DAC0 waveform frequency in [MHz].	514
0x0120102C	single	RW	PB2 DAC1 waveform frequency in [MHz].	514
0x01201030	single	RW	PB2 DAC2 waveform frequency in [MHz].	514
0x01201034	single	RW	PB2 DAC3 waveform frequency in [MHz].	514
0x01201038	single	RW	PB2 DAC0 waveform phase in [deg] in range from -180 to 180.	515
0x0120103C	single	RW	PB2 DAC1 waveform phase in [deg] in range from -180 to 180.	515
0x01201040	single	RW	PB2 DAC2 waveform phase in [deg] in range from -180 to 180.	515
0x01201044	single	RW	PB2 DAC3 waveform phase in [deg] in range from -180 to 180.	515
0x0120105C	uint8	RW	PB2 DAC0 DCM command. The following values cause actions: 1 – increment phase by one 2 – set phase shifter to 0 steps	517
0x0120105D	uint8	RW	PB2 DAC1 DCM command. The following values cause actions: 1 – increment phase by one 2 – set phase shifter to 0 steps	517
0x0120105E	uint8	RW	PB2 DAC2 DCM command. The following values cause actions: 1 – increment phase by one 2 – set phase shifter to 0 steps	517
0x0120105F	uint8	RW	PB2 DAC3 DCM command. The following values cause actions: 1 – increment phase by one step 2 – set phase shifter to 0 steps	517

4 IBFB Switch and IBFB Network

4.1 Undulators Network

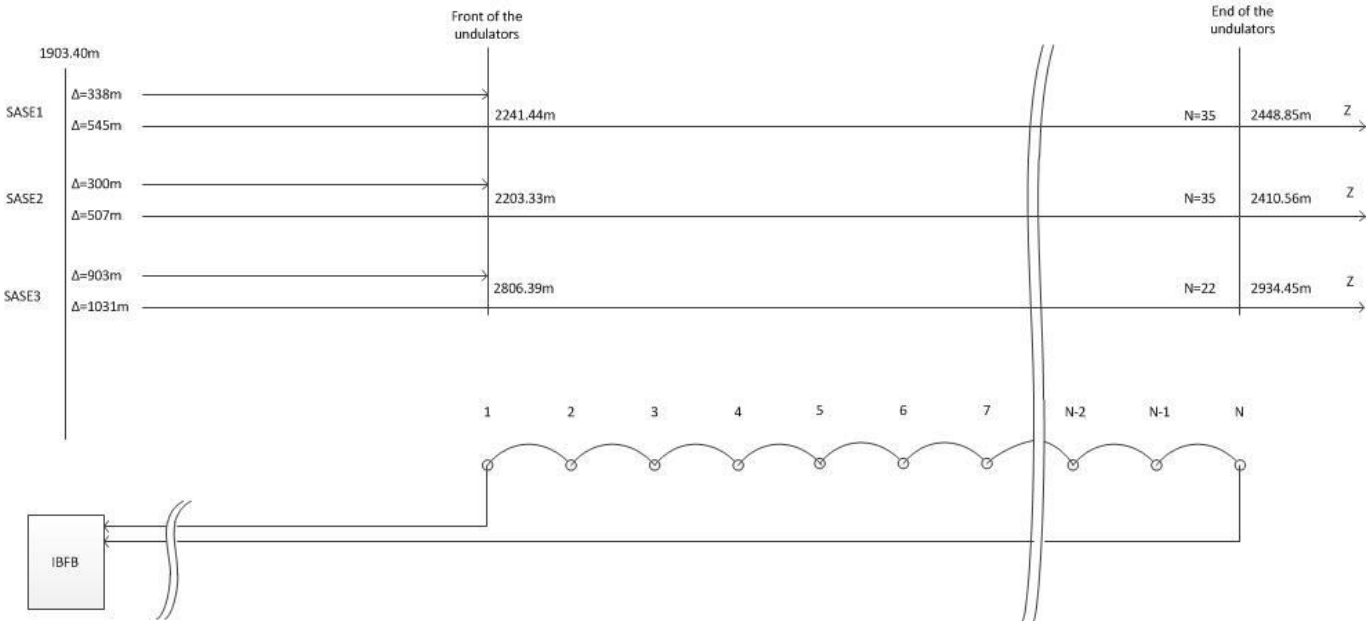


Figure 4.1: Physical location of undulators

4.2 IBFB Network Protocol

0	SOF
	Control Byte
	BPM Number
	Bucket Number Byte 0
	Bucket Number Byte 1
	Pos X Byte 0
	Pos X Byte 1
	Pos X Byte 2
	Pos X Byte 3
	Pos Y Byte 0
	Pos Y Byte 1
	Pos Y Byte 2
	Pos Y Byte 3
	CRC 8
14	EOF

Figure 4.2: Frame content of the network packet

4.3 Downstream and Upstream BPMs Network

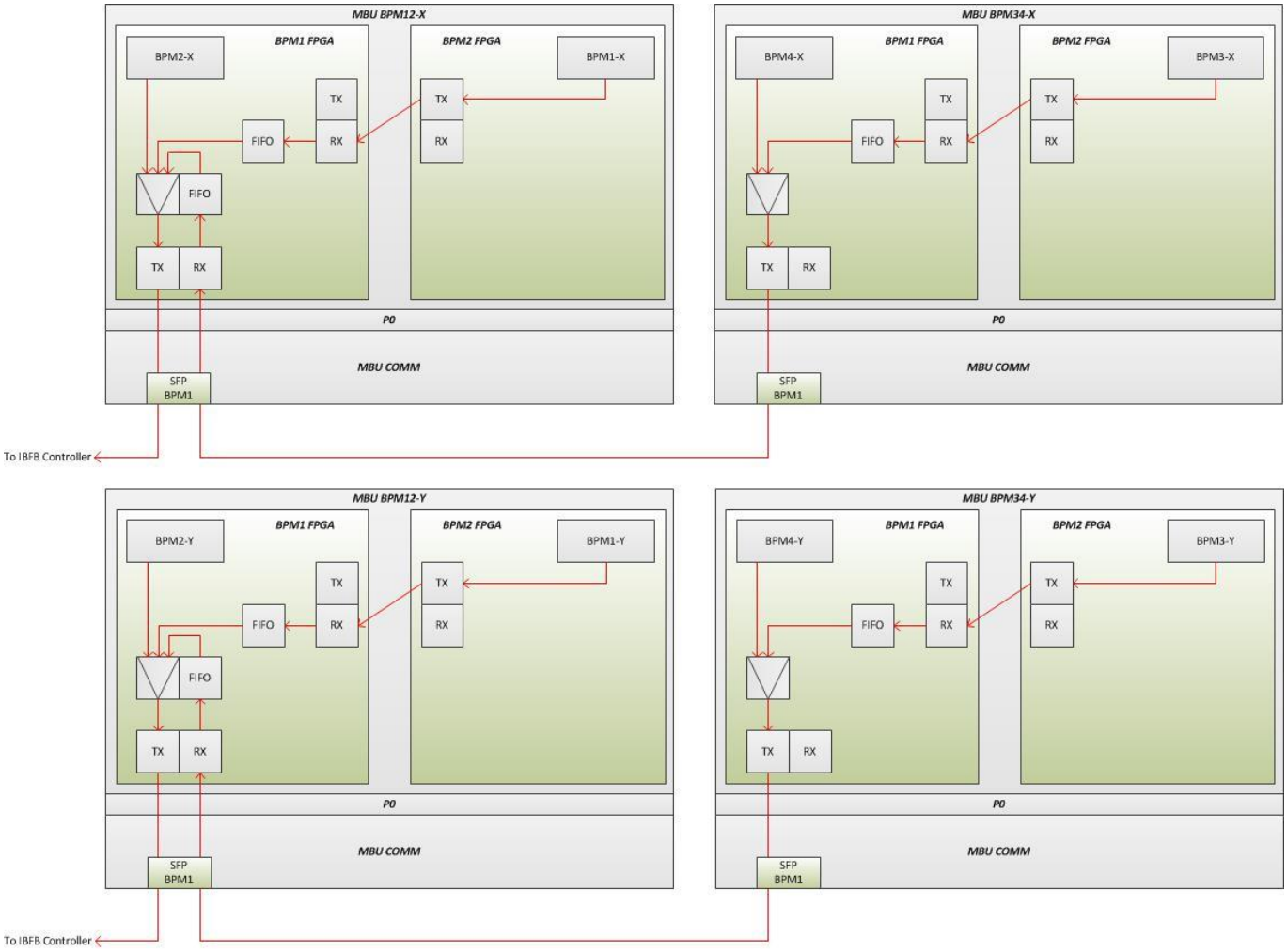


Figure 4.3: Connection of downstream and upstream BPMs to IBFB controller

4.4 IBFB Switch Firmware

4.4.1 IBFB Filter and Router

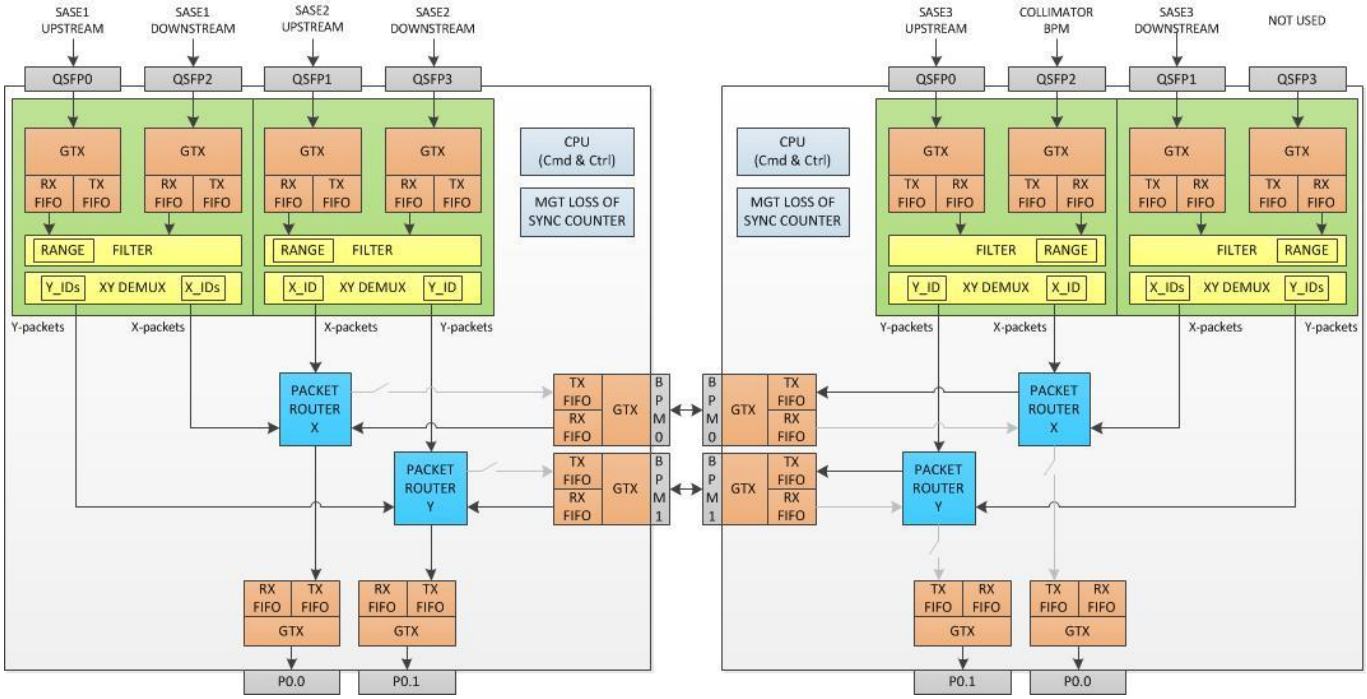


Fig 4.4 Block diagram of the firmware for IBFB switch

4.4.2 Kicker Attenuator Fans Control

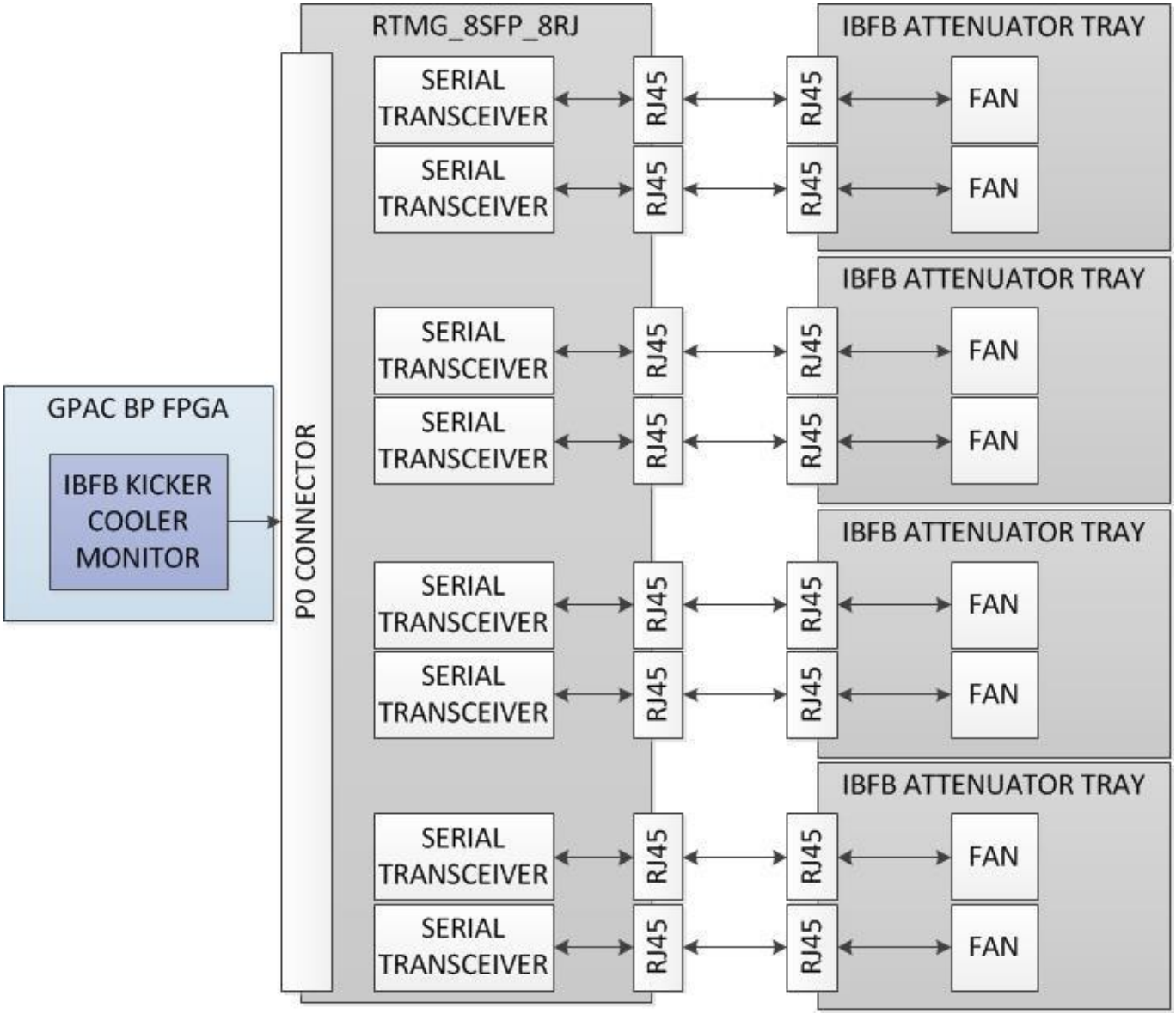


Figure 4.5: Hardware block diagram of the kicker attenuator fan control

4.4.3 IBFB Switch Register Map

All addresses in this table have absolute values. The additional columns indicates in which FPGA is located each register.

Address	Type	R/W	Description	MEDM
SYS FPGA				
0x00000000	SYS FPGA Service Component			
0x000000FF				
0x00000100	XFEL Timing System Receiver (Registers) – see documentation [4] for details.			
0x000001FF				
0x00003000	CFG FPGA Access Memory – see CFG FPGA documentation for details [5].			
0x00003FFF				
0x00008000	XFEL Timing System Receiver (Memory) – see documentation [4] for details.			
0x0000FFFF				
BP FPGA				
0x00100300	uint8	RO	The SFP of port QSFP1_0 sees no light – SASE1 upstream 0 – no light (red indicator) 1 – SFP RX sees light	300
0x00100301	uint8	RO	The SFP of port QSFP1_1 sees no light – SASE2 upstream	300

			0 – no light (red indicator) 1 – SFP RX sees light	
0x00100302	uint8	RO	The SFP of port QSFP1_2 sees no light – SASE1 downstream 0 – no light (red indicator) 1 – SFP RX sees light	300
0x00100303	uint8	RO	The SFP of port QSFP1_3 sees no light – SASE2 downstream 0 – no light (red indicator) 1 – SFP RX sees light	300
0x0010030C	uint8	RO	The SFP of port QSFP1_0 is in – SASE1 upstream 0 – SFP not in 1 – SFP plugged in the cage (green indicator)	301
0x0010030D	uint8	RO	The SFP of port QSFP1_1 is in – SASE2 upstream 0 – SFP not in 1 – SFP plugged in the cage (green indicator)	301
0x0010030E	uint8	RO	The SFP of port QSFP1_2 is in – SASE1 downstream 0 – SFP not in 1 – SFP plugged in the cage (green indicator)	301
0x0010030F	uint8	RO	The SFP of port QSFP1_3 is in – SASE2 downstream 0 – SFP not in 1 – SFP plugged in the cage (green indicator)	301
0x00100310	uint8	RO	The SFP of port QSFP2_0 sees no light – SASE3 upstream 0 – no light (red indicator) 1 – SFP RX sees light	302
0x00100311	uint8	RO	The SFP of port QSFP2_1 sees no light – Collimator BPM 0 – no light (red indicator) 1 – SFP RX sees light	302
0x00100312	uint8	RO	The SFP of port QSFP2_2 sees no light – SASE3 downstream 0 – no light (red indicator) 1 – SFP RX sees light	302
0x0010031C	uint8	RO	The SFP of port QSFP1_0 is in – SASE3 upstream 0 – SFP not in 1 – SFP plugged in the cage (green indicator)	303
0x0010031D	uint8	RO	The SFP of port QSFP1_1 is in – Collimator BPM 0 – SFP not in 1 – SFP plugged in the cage (green indicator)	303
0x0010031E	uint8	RO	The SFP of port QSFP1_2 is in – SASE3 downstream 0 – SFP not in 1 – SFP plugged in the cage (green indicator)	303
0x00100408	uint8	RO	RTMG, SFP BPM1-0 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is not plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	304, 108, 109
0x00100409	uint8	RO	RTMG, SFP BPM1-1 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	304, 108, 109
0x0010040A	uint8	RO	RTMG, SFP BPM2-0 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	304, 108
0x0010040B	uint8	RO	RTMG, SFP BPM2-1 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010040C	uint8	RO	RTMG, SFP SYS-0 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010040D	uint8	RO	RTMG, SFP SYS-1 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage	108, 109

			Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	
0x0010040E	uint8	RO	RTMG, SFP SYS-2 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010040F	uint8	RO	RTMG, SFP SYS-3 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010060A	uint8	RW	Set fan KICK-Y1-N speed in percentage.	201
0x0010060B	uint8	RW	Reset fan KICK-Y1-N. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x0010060C	uint32	RO	Tachometer of the fan KICK-Y1-N	202
0x00100612	uint8	RW	Set fan KICK-Y1-P speed in percentage.	201
0x00100613	uint8	RW	Reset fan KICK-Y1-P. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x00100614	uint32	RO	Tachometer of the fan KICK-Y1-P	202
0x0010061A	uint8	RW	Set fan KICK-Y2-N speed in percentage.	201
0x0010061B	uint8	RW	Reset fan KICK-Y2-N. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x0010061C	uint32	RO	Tachometer of the fan KICK-Y2-N	202
0x00100622	uint8	RW	Set fan KICK-Y2-P speed in percentage.	201
0x00100623	uint8	RW	Reset fan KICK-Y2-P. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x00100624	uint32	RO	Tachometer of the fan KICK-Y2-P	202
0x0010062A	uint8	RW	Set fan KICK-X1-N speed in percentage.	201
0x0010062B	uint8	RW	Reset fan KICK-X1-N. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x0010062C	uint32	RO	Tachometer of the fan KICK-X1-N	202
0x00100632	uint8	RW	Set fan KICK-X1-P speed in percentage.	201
0x00100633	uint8	RW	Reset fan KICK-X1-P. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x00100634	uint32	RO	Tachometer of the fan KICK-X1-P	202
0x0010063A	uint8	RW	Set fan KICK-X2-N speed in percentage.	201
0x0010063B	uint8	RW	Reset fan KICK-X2-N. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x0010063C	uint32	RO	Tachometer of the fan KICK-X2-N	202
0x00100642	uint8	RW	Set fan KICK-X2-P speed in percentage.	201
0x00100643	uint8	RW	Reset fan KICK-X2-P. Level sensitive reset: 0 – normal operation 1 – reset state	200
0x00100644	uint32	RO	Tachometer of the fan KICK-X2-P	202
BPM1 FPGA				
0x00A00800	uint32	RW	Reset loss of sync counters. It is level sensitive: - write 0x00000000 to disable reset - write 0x0FF00000 to keep the counters in reset state	305
0x00A00808	uint8	RO	Status of enabled router outputs: Bit0-3 – not used always zero Bit4 – enabled BPM1 GTX output Bit5 – enabled MBU COM BPM1-0 output Bit6 – enabled BPM0 GTX output Bit7 – enabled MBU COM BPM1-1 output	328
0x00A0080D	uint8	RO	Status of the BPM01 GTX: Bit 7 – loss of synchronization for BPM1 GTX Bit 5 – loss of synchronization for BPM0 GTX	306

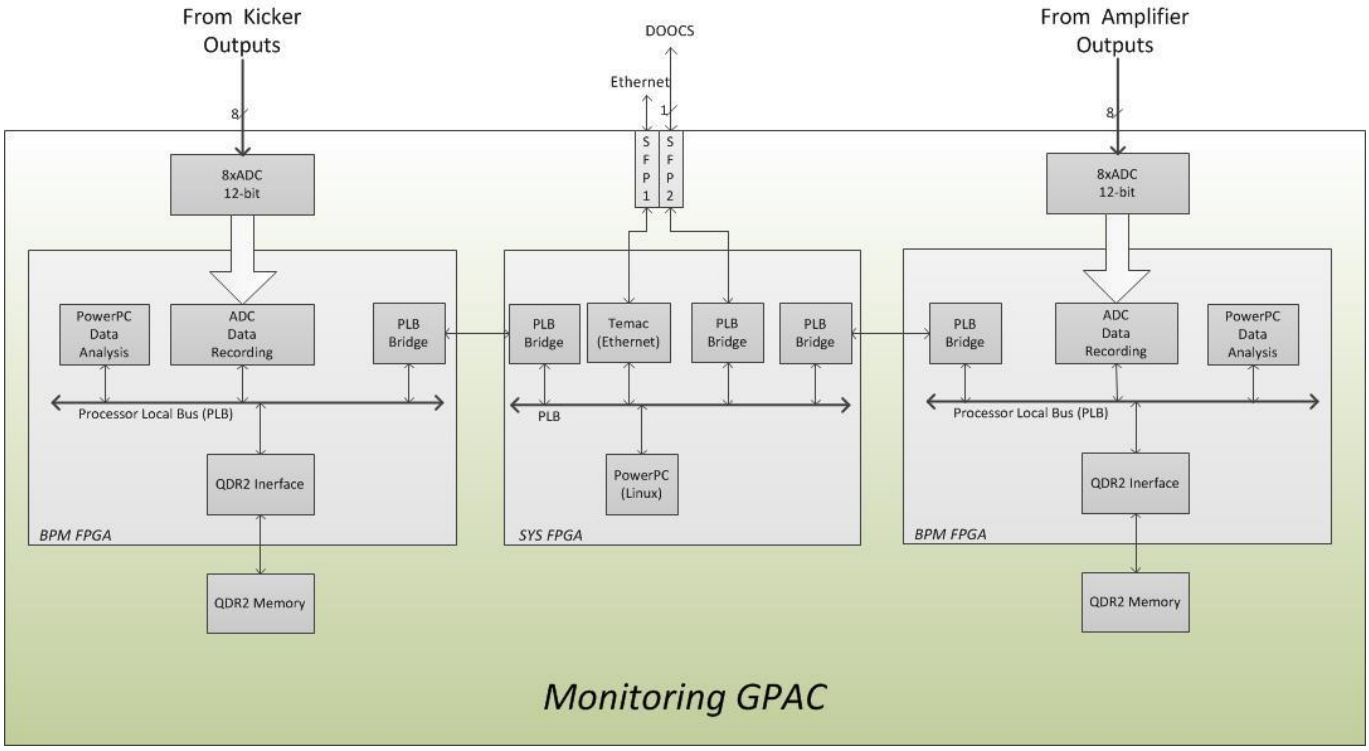
0x00A0080E	uint8	RO	Status of the QSFP02 GTX: Bit 7 – loss of synchronization for QSFP0 GTX – SASE1 upstream Bit 5 – loss of synchronization for QSFP2 GTX – SASE2 downstream	307
0x00A0080F	uint8	RO	Status of the QSFP13 GTX: Bit 7 – loss of synchronization for QSFP1 GTX – SASE2 upstream Bit 5 – loss of synchronization for QSFP3 GTX – SASE2 downstream	307
0x00A00813	uint8	RO	Status of the MBU COM GTX: Bit 7 – loss of synchronization for MBU COM GTX0 – IBFB controller Y Bit 5 – loss of synchronization for MBU COM GTX1 – IBFB controller X	308
0x00A0081C	uint8	RW	BPM1 ID for SASE2, Y plane	309
0x00A0081D	uint8	RW	BPM2 ID for SASE2, Y plane	309
0x00A0081E	uint8	RW	BPM1 ID for SASE2, X plane	309
0x00A0081F	uint8	RW	BPM2 ID for SASE2, X plane	309
0x00A00820	uint8	RW	BPM1 ID for SASE1, Y plane	309
0x00A00821	uint8	RW	BPM2 ID for SASE1, Y plane	309
0x00A00822	uint8	RW	BPM1 ID for SASE1, X plane	309
0x00A00823	uint8	RW	BPM2 ID for SASE1, X plane	309
0x00A00824	uint16	RO	Loss counter for QSFP1 – SASE2 upstream	310
0x00A00826	uint16	RO	Loss counter for QSFP0 – SASE1 upstream	310
0x00A00828	uint16	RO	Loss counter for QSFP3 – SASE2 downstream	310
0x00A0082A	uint16	RO	Loss counter for QSFP2 – SASE1 downstream	310
0x00A0082C	uint16	RO	Loss counter for BPM1 GTX	312
0x00A0082E	uint16	RO	Loss counter for BPM0 GTX	311
0x00A00834	uint16	RO	Loss counter for MBU COM GTX0 – IBFB controller Y	313
0x00A00836	uint16	RO	Loss counter for MBU COM GTX1 – IBFB controller X	313
0x00A00853	uint8	RO	External trigger missing	400
0x00A00854	uint16	RO	Packet counter for SASE1 upstream	314
0x00A00856	uint16	RO	Packet counter for SASE1 downstream	314
0x00A00858	uint16	RO	Packet counter for SASE2 upstream	314
0x00A0085A	uint16	RO	Packet counter for SASE2 downstream	314
0x00A0085C	uint16	RO	Discarded packets for SASE1	315
0x00A00860	uint16	RO	Discarded packets for SASE2	315
0x00A00864	uint8	RO	Invalid BPM ID for SASE1. When bigger than 0 then an invalid BPM send data	316
0x00A00866	uint8	RO	Invalid BPM ID for SASE2. When bigger than 0 then an invalid BPM send data	316
0x00A00868	uint16	RO	Passed packets for SASE1 plane X	317
0x00A0086A	uint16	RO	Passed packets for SASE1 plane Y	317
0x00A0086C	uint16	RO	Passed packets for SASE2 plane X	317
0x00A0086E	uint16	RO	Passed packets for SASE2 plane Y	317
0x00A00870	uint16	RO	SASE1 filter – star bucket number	318
0x00A00872	uint16	RO	SASE1 filter – stop bucket number	318
0x00A00874	uint16	RO	SASE2 filter – star bucket number	318
0x00A00876	uint16	RO	SASE2 filter – stop bucket number	318
0x00A00880	uint8	RW	Enable ping packet for SASE1 upstream chain	
0x00A00881	uint8	RW	Enable ping packet for SASE2 upstream chain	
0x00A00882	uint8	RW	Enable ping packet for SASE1 downstream chain	
0x00A00883	uint8	RW	Enable ping packet for SASE2 downstream chain	
0x00A00884	uint8	RO	Received ping packet for SASE1 upstream chain	
0x00A00885	uint8	RO	Received ping packet for SASE2 upstream chain	
0x00A00886	uint8	RO	Received ping packet for SASE1 downstream chain	
0x00A00887	uint8	RO	Received ping packet for SASE2 downstream chain	
0x00A00888	uint32	RO	Ping packet delay for SASE1 upstream chain	
0x00A0088C	uint32	RO	Ping packet delay for SASE2 upstream chain	
0x00A00890	uint32	RO	Ping packet delay for SASE1 downstream chain	
0x00A00894	uint32	RO	Ping packet delay for SASE2 downstream chain	
0x00A01004	uint8	RW	Trigger source: 0 – Signal 1 – Machine trigger 2 – Auto trigger (2 s) 3 – Auto trigger (1 s) 4 – Auto trigger (0.5 s) 5 – Auto trigger (0.2 s) 6 – Auto trigger (0.1 s)	401
0x00A01005	uint8	RW	Trigger mode: 0 – Continuous 1 – Single	402

0x00A01008	uint32	RW	Delay of the first bunch with respect to the pulse trigger. Measured in clock cycles.	403
0x00A0100C	uint16	RW	Number of buckets. Now has to be set manually. Later the value comes from timing system.	404
0x00A0100E	uint16	RW	Bucket spacing in ADC clock cycles. Now has to be set manually. Later the value comes from the timing system.	405
BPM2 FPGA				
0x01200800	uint32	RW	Reset loss of sync counters. It is level sensitive: - write 0x00000000 to disable reset - write 0x0FF00000 to keep the counters in reset state	319
0x01200808	uint8	RO	Status of enabled router outputs: Bit0-3 – not used always zero Bit4 – enabled BPM1 GTX output Bit5 – enabled MBU COM BPM1-0 output Bit6 – enabled BPM0 GTX output Bit7 – enabled MBU COM BPM1-1 output	329
0x0120080E	uint8	RO	Status of the QSFP02 GTX: Bit 7 – loss of synchronization for QSFP0 GTX – SASE1 upstream Bit 5 – loss of synchronization for QSFP2 GTX – SASE2 downstream	320
0x0120080F	uint8	RO	Status of the QSFP13 GTX: Bit 7 – loss of synchronization for QSFP1 GTX – SASE2 upstream Bit 5 – loss of synchronization for QSFP3 GTX – SASE2 downstream	320
0x0120081C	uint8	RW	BPM1 ID for SASE3, Y plane	321
0x0120081D	uint8	RW	BPM2 ID for SASE3, Y plane	321
0x0120081E	uint8	RW	BPM1 ID for SASE3, X plane	321
0x0120081F	uint8	RW	BPM2 ID for SASE3, X plane	321
0x01200820	uint8	RW	BPM1 ID for Collimator BPM, Y plane	321
0x01200824	uint16	RO	Loss counter for QSFP1 – Collimator BPM	322
0x01200826	uint16	RO	Loss counter for QSFP0 – SASE3 upstream	322
0x01200828	uint16	RO	Reserved	
0x0120082A	uint16	RO	Loss counter for QSFP2 – SASE3 downstream	322
0x01200853	uint8	RO	External trigger missing	406
0x01200854	uint16	RO	Packet counter for SASE3 upstream	323
0x01200856	uint16	RO	Packet counter for SASE3 downstream	323
0x01200858	uint16	RO	Packet counter Collimator BPM	323
0x0120085A	uint16	RO	Reserved	
0x0120085C	uint16	RO	Discarded packets for SASE3	324
0x01200860	uint16	RO	Discarded packets for Collimator BPM	324
0x01200864	uint8	RO	Invalid BPM ID for SASE3. When bigger than 0 then an invalid BPM send data	325
0x01200866	uint8	RO	Invalid BPM ID for Collimator BPM. When bigger than 0 then an invalid BPM send data	325
0x01200868	uint16	RO	Passed packets for SASE3 plane X	326
0x0120086A	uint16	RO	Passed packets for SASE3 plane Y	326
0x0120086C	uint16	RO	Passed packets for Collimator BPM	326
0x0120086E	uint16	RO	Reserved	
0x01200870	uint16	RO	SASE3 filter – star bucket number	327
0x01200872	uint16	RO	SASE3 filter – stop bucket number	327
0x01200880	uint8	RW	Enable ping packet for SASE1 upstream chain	
0x01200881	uint8	RW	Enable ping packet for SASE2 upstream chain	
0x01200882	uint8	RW	Enable ping packet for SASE1 downstream chain	
0x01200883	uint8	RW	Enable ping packet for SASE2 downstream chain	
0x01200884	uint8	RO	Received ping packet for SASE1 upstream chain	
0x01200885	uint8	RO	Received ping packet for SASE2 upstream chain	
0x01200886	uint8	RO	Received ping packet for SASE1 downstream chain	
0x01200887	uint8	RO	Received ping packet for SASE2 downstream chain	
0x01200888	uint32	RO	Ping packet delay for SASE1 upstream chain	
0x0120088C	uint32	RO	Ping packet delay for SASE2 upstream chain	
0x01200890	uint32	RO	Ping packet delay for SASE1 downstream chain	
0x01200894	uint32	RO	Ping packet delay for SASE2 downstream chain	
0x01201004	uint8	RW	Trigger source: 0 – Signal 1 – Machine trigger 2 – Auto trigger (2 s) 3 – Auto trigger (1 s) 4 – Auto trigger (0.5 s)	407

			5 – Auto trigger (0.2 s) 6 – Auto trigger (0.1 s)	
0x01201005	uint8	RW	Trigger mode: 0 – Continuous 1 – Single	408
0x01201008	uint32	RW	Delay of the first bunch with respect to the pulse trigger. Measured in clock cycles.	409
0x0120100C	uint16	RW	Number of buckets. Now has to be set manually. Later the value comes from timing system.	410
0x0120100E	uint16	RW	Bucket spacing in ADC clock cycles. Now has to be set manually. Later the value comes from the timing system.	411

5 IBFB Monitoring

5.1 IBFB Monitoring Firmware



5.1.1 IBFB Monitor Register Map

Address	Type	R/W	Description	MEDM
SYS FPGA				
0x00000000	SYS FPGA Service Component			
0x000000FF				
0x00000100	XFEL Timing System Receiver (Registers) – see documentation [4] for details.			
0x000001FF				
0x00003000	CFG FPGA Access Memory – see CFG FPGA documentation for details [5].			
0x00003FFF				
0x00008000	XFEL Timing System Receiver (Memory) – see documentation [4] for details.			
0x0000FFFF				
BP FPGA				

0x00100408	uint8	RO	RTMG, SFP BPM1-0 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is not plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	304, 108, 109
0x00100409	uint8	RO	RTMG, SFP BPM1-1 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	304, 108, 109
0x0010040A	uint8	RO	RTMG, SFP BPM2-0 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	304, 108
0x0010040B	uint8	RO	RTMG, SFP BPM2-1 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010040C	uint8	RO	RTMG, SFP SYS-0 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010040D	uint8	RO	RTMG, SFP SYS-1 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010040E	uint8	RO	RTMG, SFP SYS-2 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
0x0010040F	uint8	RO	RTMG, SFP SYS-3 status: Bit 0 – when high no light received by SFP Bit 1 – when high the SFP is plugged in the cage Bit 2 – when high the transmitter is disabled Bit 3 – when high the transmitter has fault	108, 109
BPM1 FPGA				
0x00A00154	uint8	RO	External trigger missing (red indicator): =0 – trigger detected <>0 – missing trigger	428
0x00A0050E	uint16	RO	Number of samples stored in QDR2 memory	608
0x00A01004	uint8	RW	Trigger source: 0 – Signal 1 – Machine trigger 2 – Auto trigger (2 s) 3 – Auto trigger (1 s) 4 – Auto trigger (0.5 s) 5 – Auto trigger (0.2 s) 6 – Auto trigger (0.1 s)	423
0x00A01005	uint8	RW	Trigger mode: 0 – Continuous 1 – Single	424
0x00A01008	uint32	RW	Delay of the first bunch with respect to the pulse trigger. Measured in clock cycles.	425
0x00A0100C	uint16	RW	Number of bunches. Now has to be set manually. Later the value comes from timing system.	426
0x00A0100E	uint16	RW	Bunch spacing in ADC clock cycles. Now has to be set manually. Later the value comes from the timing system.	427
0x00B00000	int16 (2048)	RO	Amplifier output monitor for KICK-Y1-N. It is a waveform of 2048 samples in range of +/- 32767	600
0x00B20000	int16	RO	Amplifier output monitor for KICK-Y1-P. It is a waveform of 2048 samples in	601

	(2048)		range of +/- 32767	
0x00B40000	int16 (2048)	RO	Amplifier output monitor for KICK-Y2-N. It is a waveform of 2048 samples in range of +/- 32767	602
0x00B60000	int16 (2048)	RO	Amplifier output monitor for KICK-Y2-P. It is a waveform of 2048 samples in range of +/- 32767	603
0x00B80000	int16 (2048)	RO	Amplifier output monitor for KICK-Y1-N. It is a waveform of 2048 samples in range of +/- 32767	604
0x00BA0000	int16 (2048)	RO	Amplifier output monitor for KICK-Y1-P. It is a waveform of 2048 samples in range of +/- 32767	605
0x00BC0000	int16 (2048)	RO	Amplifier output monitor for KICK-Y2-N. It is a waveform of 2048 samples in range of +/- 32767	606
0x00BE0000	int16 (2048)	RO	Amplifier output monitor for KICK-Y2-P. It is a waveform of 2048 samples in range of +/- 32767	607
BPM2 FPGA				
0x01200154	uint8	RO	External trigger missing (red indicator): =0 – trigger detected <>0 – missing trigger	434
0x0120050E	uint16	RO	Number of samples stored in QDR2 memory	708
0x01201004	uint8	RW	Trigger source: 0 – Signal 1 – Machine trigger 2 – Auto trigger (2 s) 3 – Auto trigger (1 s) 4 – Auto trigger (0.5 s) 5 – Auto trigger (0.2 s) 6 – Auto trigger (0.1 s)	429
0x01201005	uint8	RW	Trigger mode: 0 – Continuous 1 – Single	430
0x01201008	uint32	RW	Delay of the first bunch with respect to the pulse trigger. Measured in clock cycles.	431
0x0120100C	uint16	RW	Number of bunches. Now has to be set manually. Later the value comes from timing system.	432
0x0120100E	uint16	RW	Bunch spacing in ADC clock cycles. Now has to be set manually. Later the value comes from the timing system.	433
0x01300000	int16 (2048)	RO	Kicker output monitor for KICK-Y1-N. It is a waveform of 2048 samples in range of +/- 32767	700
0x01320000	int16 (2048)	RO	Kicker output monitor for KICK-Y1-P. It is a waveform of 2048 samples in range of +/- 32767	701
0x01340000	int16 (2048)	RO	Kicker output monitor for KICK-Y2-N. It is a waveform of 2048 samples in range of +/- 32767	702
0x01360000	int16 (2048)	RO	Kicker output monitor for KICK-Y2-P. It is a waveform of 2048 samples in range of +/- 32767	703
0x01380000	int16 (2048)	RO	Kicker output monitor for KICK-Y1-N. It is a waveform of 2048 samples in range of +/- 32767	704
0x013A0000	int16 (2048)	RO	Kicker output monitor for KICK-Y1-P. It is a waveform of 2048 samples in range of +/- 32767	705
0x013C0000	int16 (2048)	RO	Kicker output monitor for KICK-Y2-N. It is a waveform of 2048 samples in range of +/- 32767	706
0x013E0000	int16 (2048)	RO	Kicker output monitor for KICK-Y2-P. It is a waveform of 2048 samples in range of +/- 32767	707

6 Cavity BPM Extension for IBFB

The IBFB uses as sensors the Cavity BPMs located in various locations. The position measured by the Cavity BPMs is sent over fiber link connected to MBU COM board. The transmission protocol described in section 4.2 is involved to deliver the position data to the IBFB electronics.

The block diagram of the firmware extension is presented in Fig. 6.1. Each MBU is connected by two fiber cables. A series of MBUs connected in the same way create two chains. The ends of both chains are connected to the IBFB controller.
The firmware extension is implemented in both BPM1 and BPM2 FPGA. The firmware is symmetric and performs the following functions:

- Transmission of the position from local BPM
- Transmission of the position from the BPM in another BPM FPGA in the same MBU
- Forwarding of the packets sent by other MBUs

In addition the firmware has the following features:

- Present status of the fiber connection such as loss of signal, loss of synchronization, loss of synchronization counter
- Disable/enable transmission from local BPM
- BPM ID register for unique identification of the packets in the IBFB network.

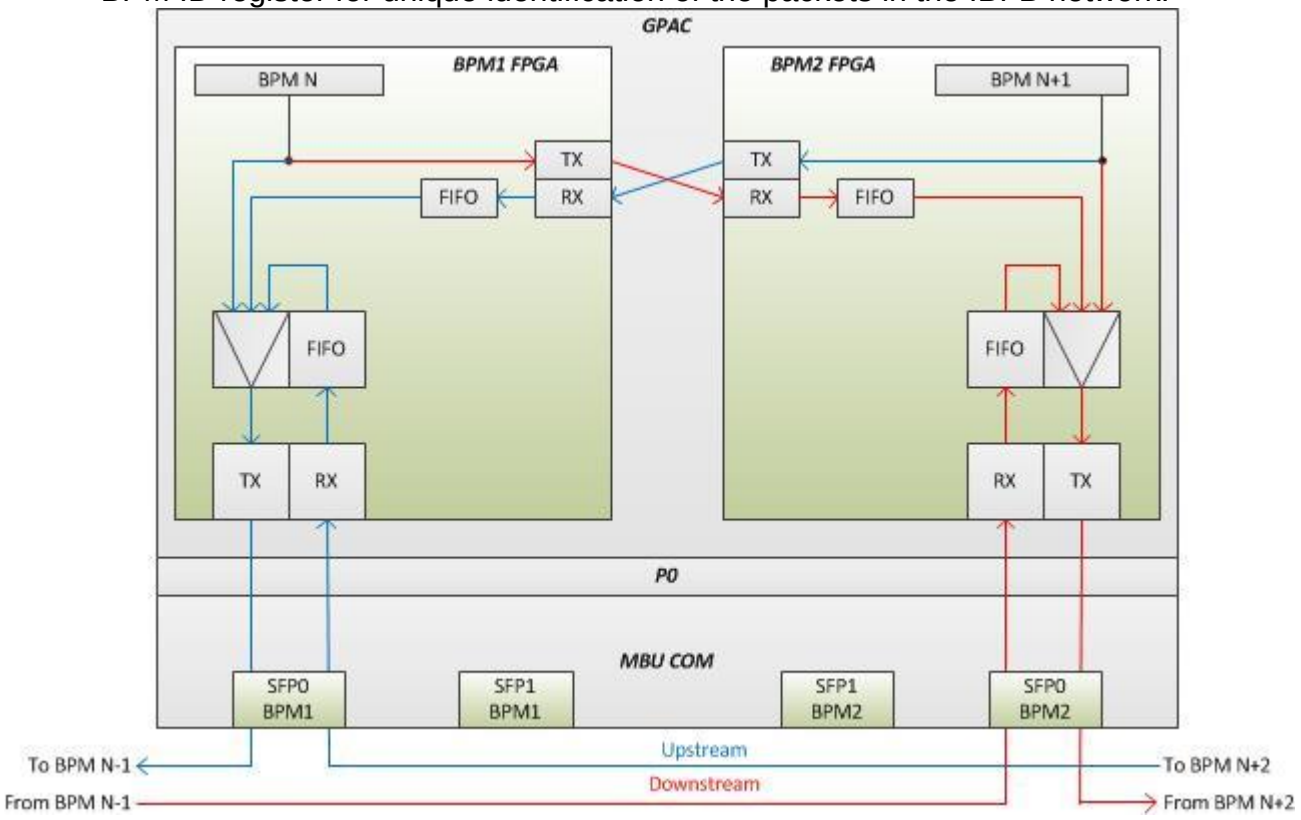


Figure 6.1: Block diagram of the firmware extension for Cavity BPM.

The Cavity BPM extension is used for all BPMs connected to the IBFB system and these are:

- four MBUs in rack 1899 with IBFB upstream and downstream BPMs
- 35 BPMs in undulator 1
- 35 BPMs in undulator 2
- 20 BPMs in undulator 3
- one collimator BPM

6.1 Register Map

The address offset is 0x00000400 with respect to base address of the BPM FPGA which means:

- 0x00800400 for Cavity BPM1
- 0x01000400 for Cavity BPM2

Address	Type	R/W	Description	MEDM
0x0000	uint32	RW	Reserved. Always write 0.	
0x0004	uint8	RW	BPM identification field. This field is used to configure the unique BPM number which is sent by the IBFB feedback protocol	
0x0005	uint8	RW	Reserved. Always write 0 to this register	
0x0006	uint8	RW	Reserved. Always write 0 to this register	
0x0007	uint8	RW	Reserved. Always write 0 to this register	
0x0008	uint8	RO	Reserved.	
0x0009	uint8	RO	Reserved.	
0x000A	uint8	RO	Status of GTX0 and GTX1 between BPM1 FPGA and BPM2 FPGA: Bit 7 – GTX1 loss of synchronization Bit 5 – GTX0 loss of synchronization Bit 2 – GTX1 reset done Bit 1 – GTX 0 reset done Bit 0 – GTX PLL locked	
0x000B	uint8	RO	Status of GTX0 and GTX1 on the MBU COM board: Bit 7 – GTX1 loss of synchronization Bit 5 – GTX0 loss of synchronization Bit 2 – GTX1 reset done Bit 1 – GTX 0 reset done Bit 0 – GTX PLL locked	
0x000C	uint16	RO	MBU COM board GTX1 loss of sync counter	
0x000E	uint16	RO	MBU COM board GTX0 loss of sync counter	
0x0010	uint16	RO	BPM1 FPGA to BPM2 FPGA GTX0 loss of sync counter	
0x0012	uint16	RO	BPM1 FPGA to BPM2 FPGA GTX0 loss of sync counter	
0x0014	uint32	RO	Reserved	
0x0018	uint32	RO	Reserved	
0x001C	uint32	RO	Reserved	
0x0020	uint32	RO	Reserved	
0x0024	uint32	RW	Enable BPM to transmit position to IBFB network 0 – disabled 1 – enabled	

7 IBFB Player

7.1 IBFB Player Firmware

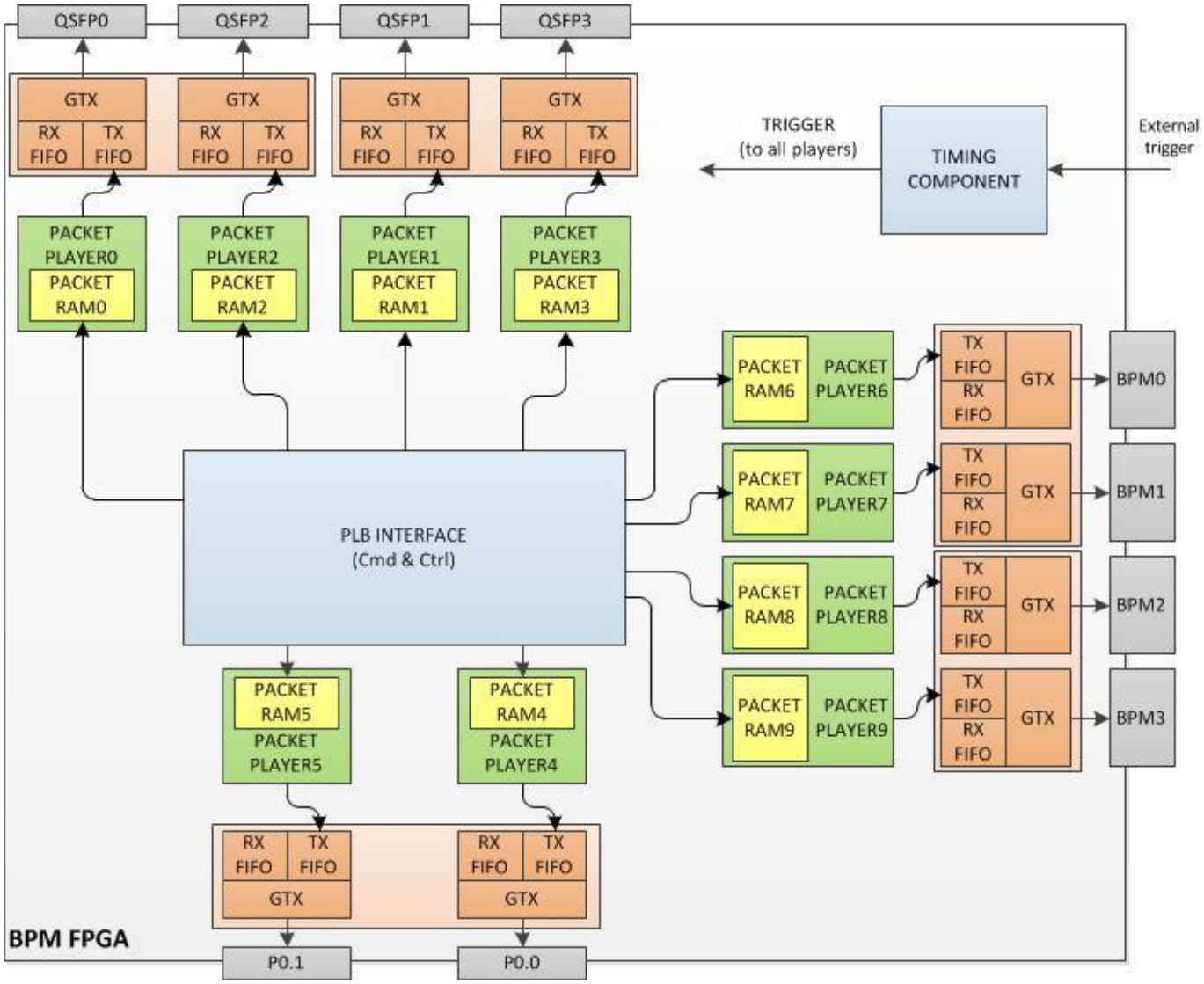


Figure 7.1: IBFB player firmware block diagram

7.2 Test Setup

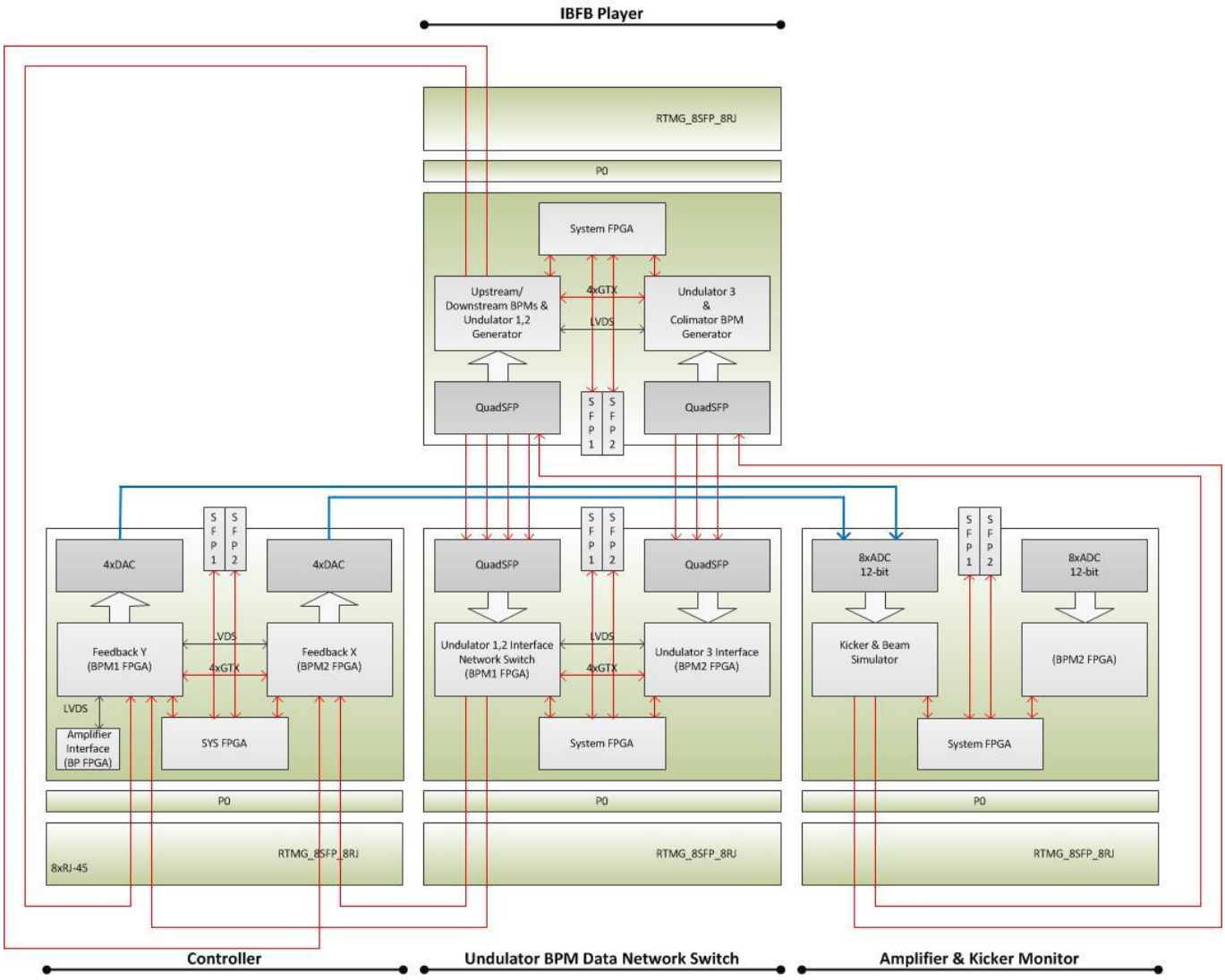


Figure 7.2: Block diagram of the test setup if IBFB electronics and IBFB player

8 Appendix

8.1 EPICS Screenshots

The following screenshot have blue labels referring to address map tables in the previous chapters.

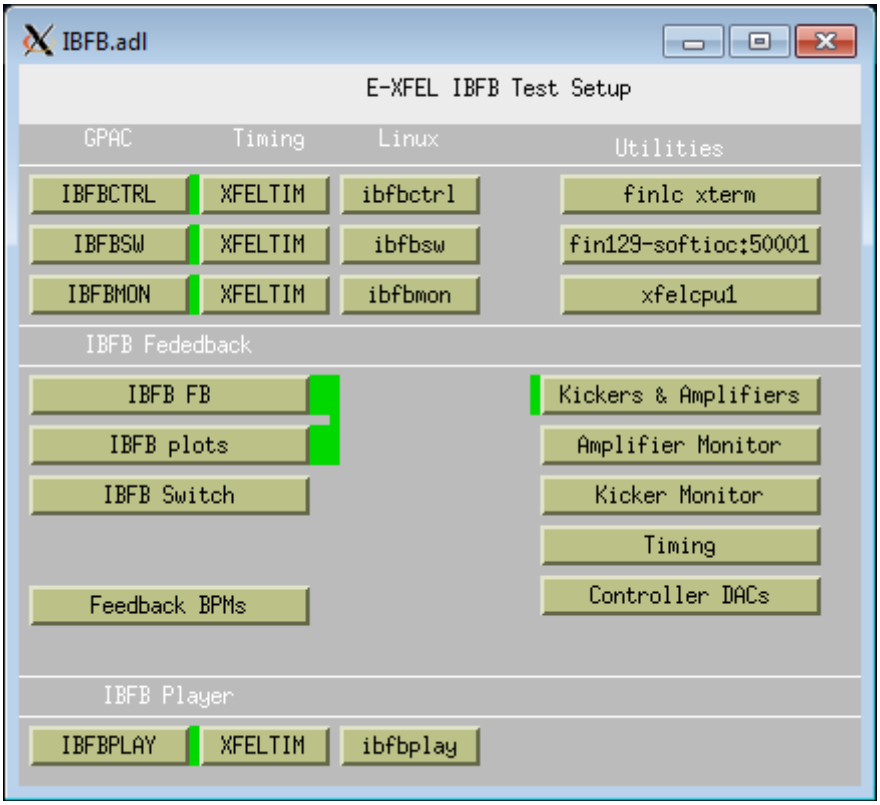


Figure 8.1: Main EPICS panel for IBFB

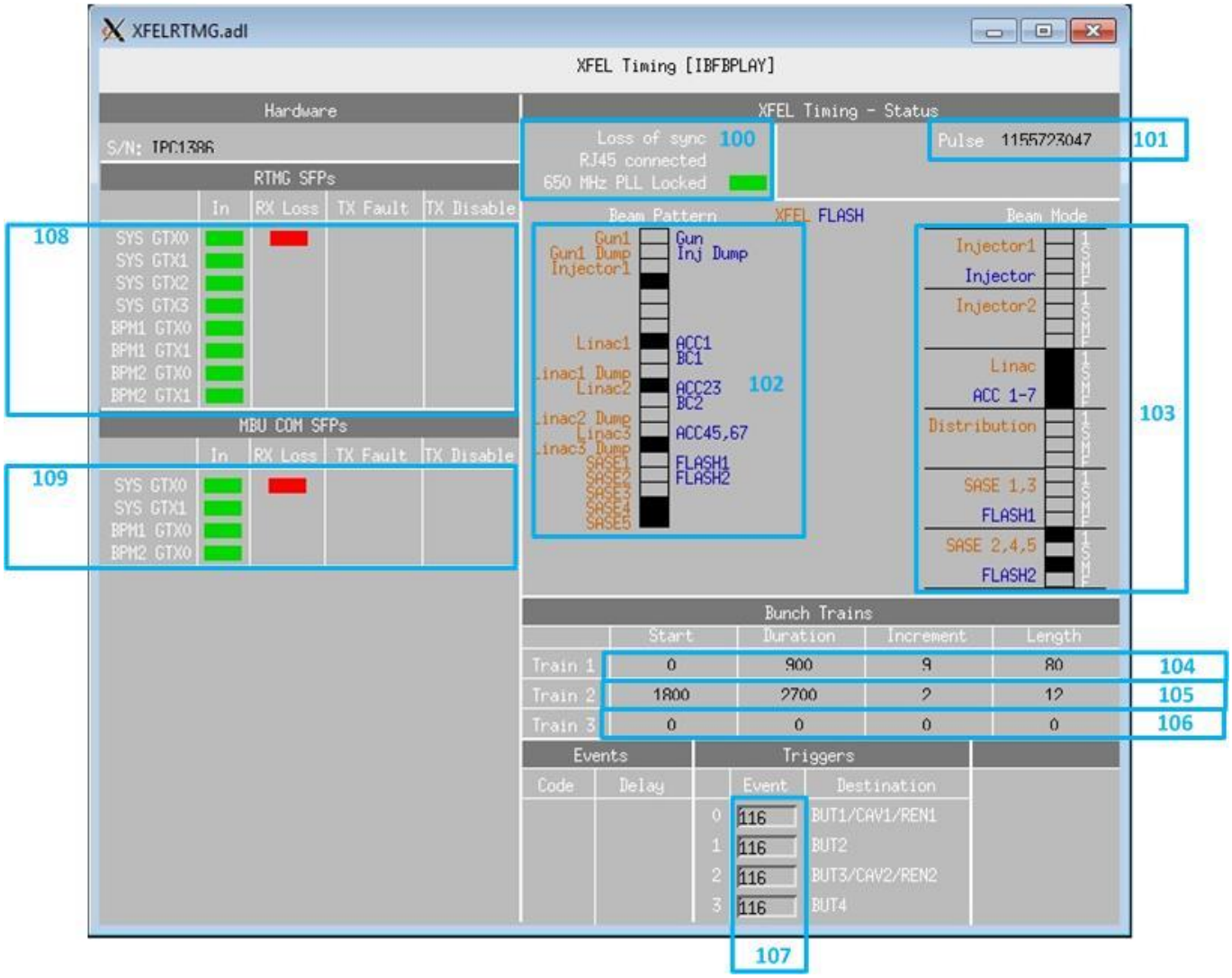


Figure 8.2: PSI timing receiver for E-XFEL uTCA timing system

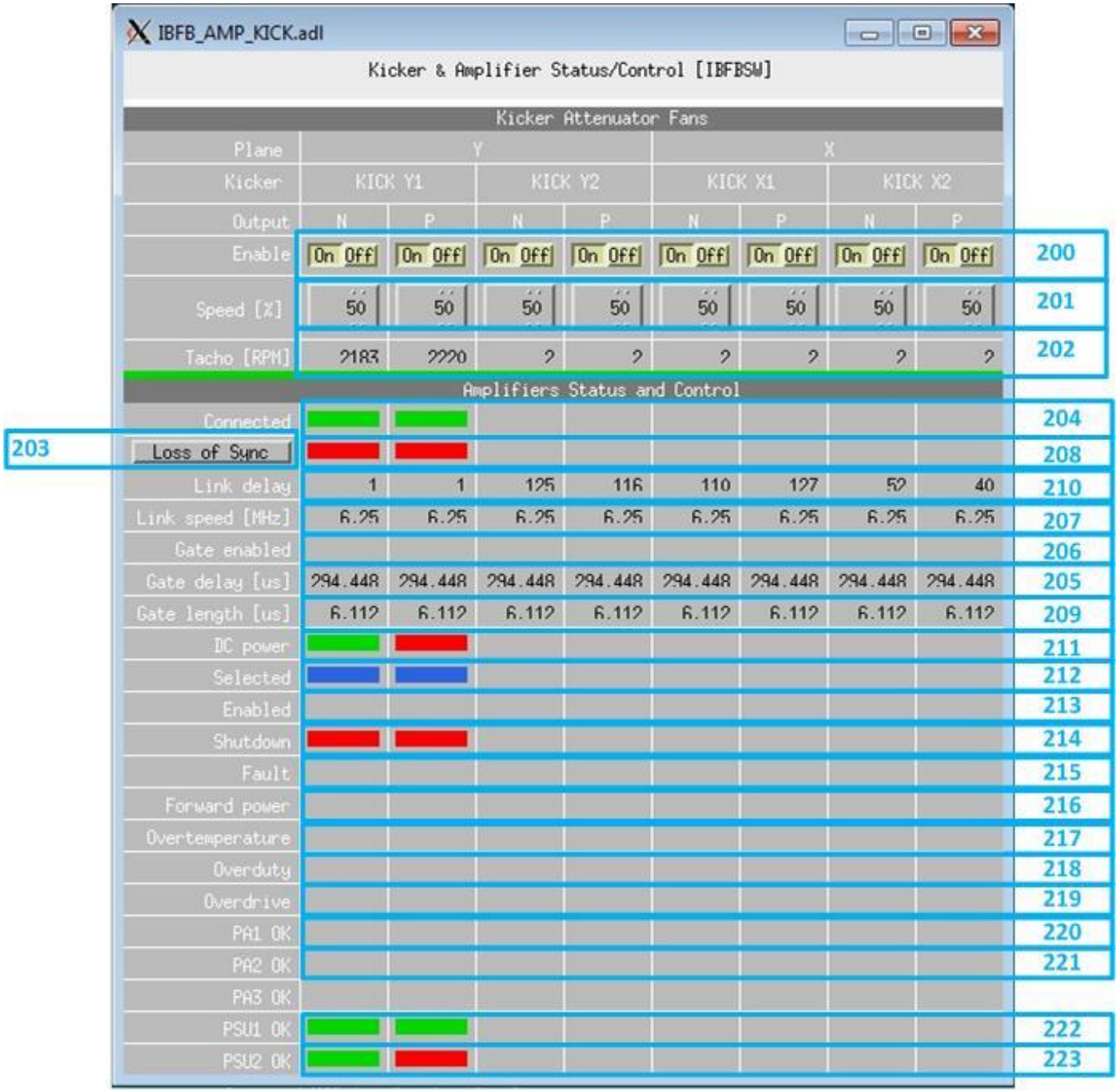


Figure 8.3: Amplifiers status and control

Figure 8.4: IBFB switch control and status

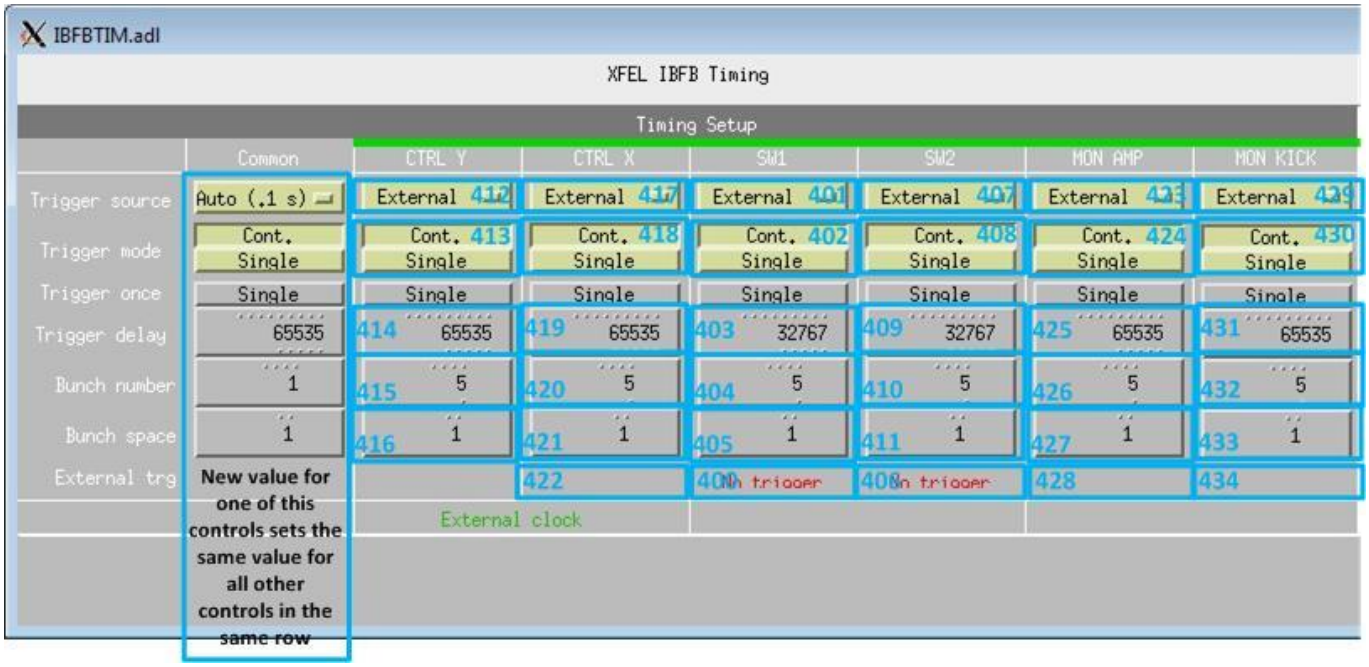


Figure 8.5: IBFB timing settings

Figure 8.6 DAC status and control

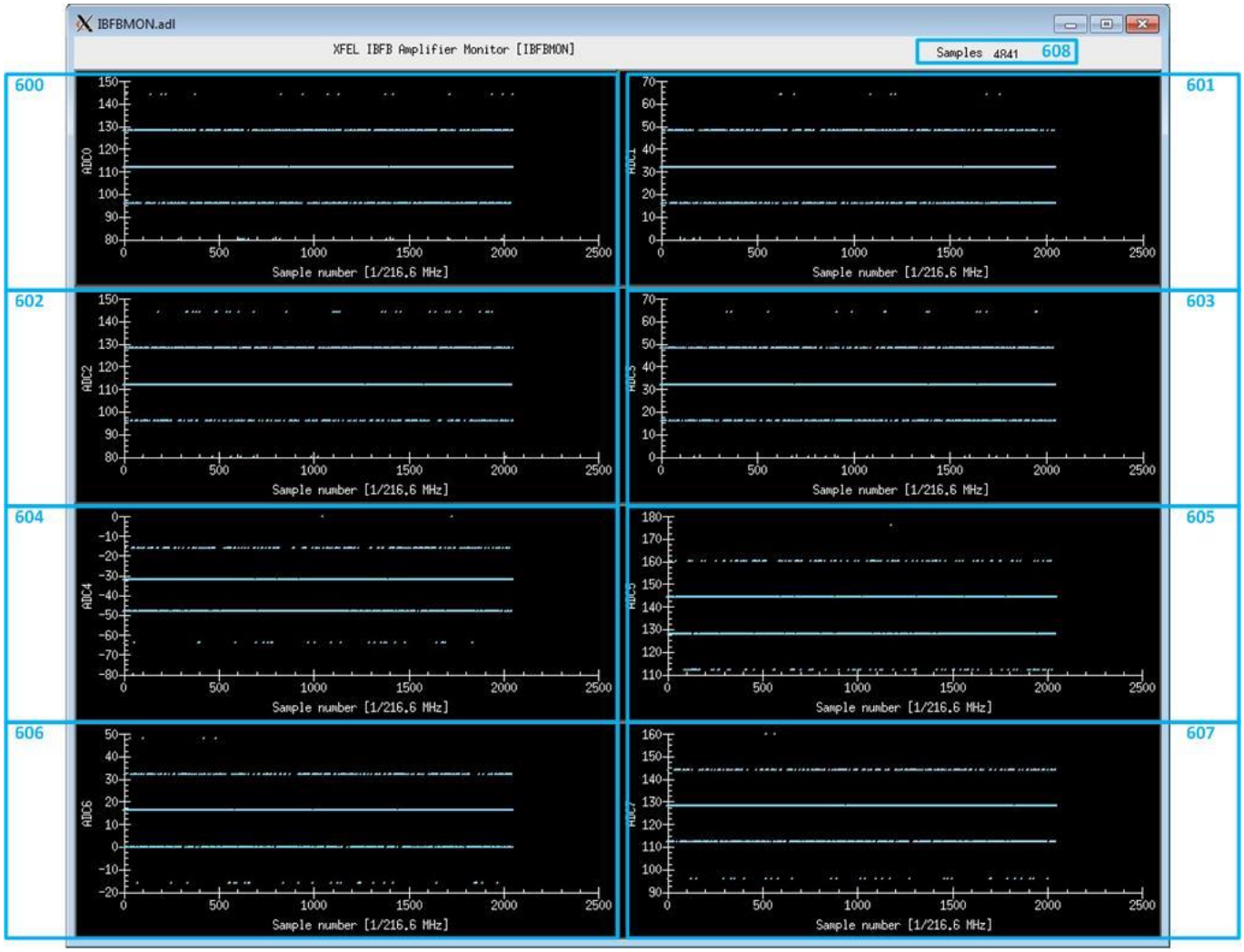


Figure 8.7: IBFB amplifier output monitor

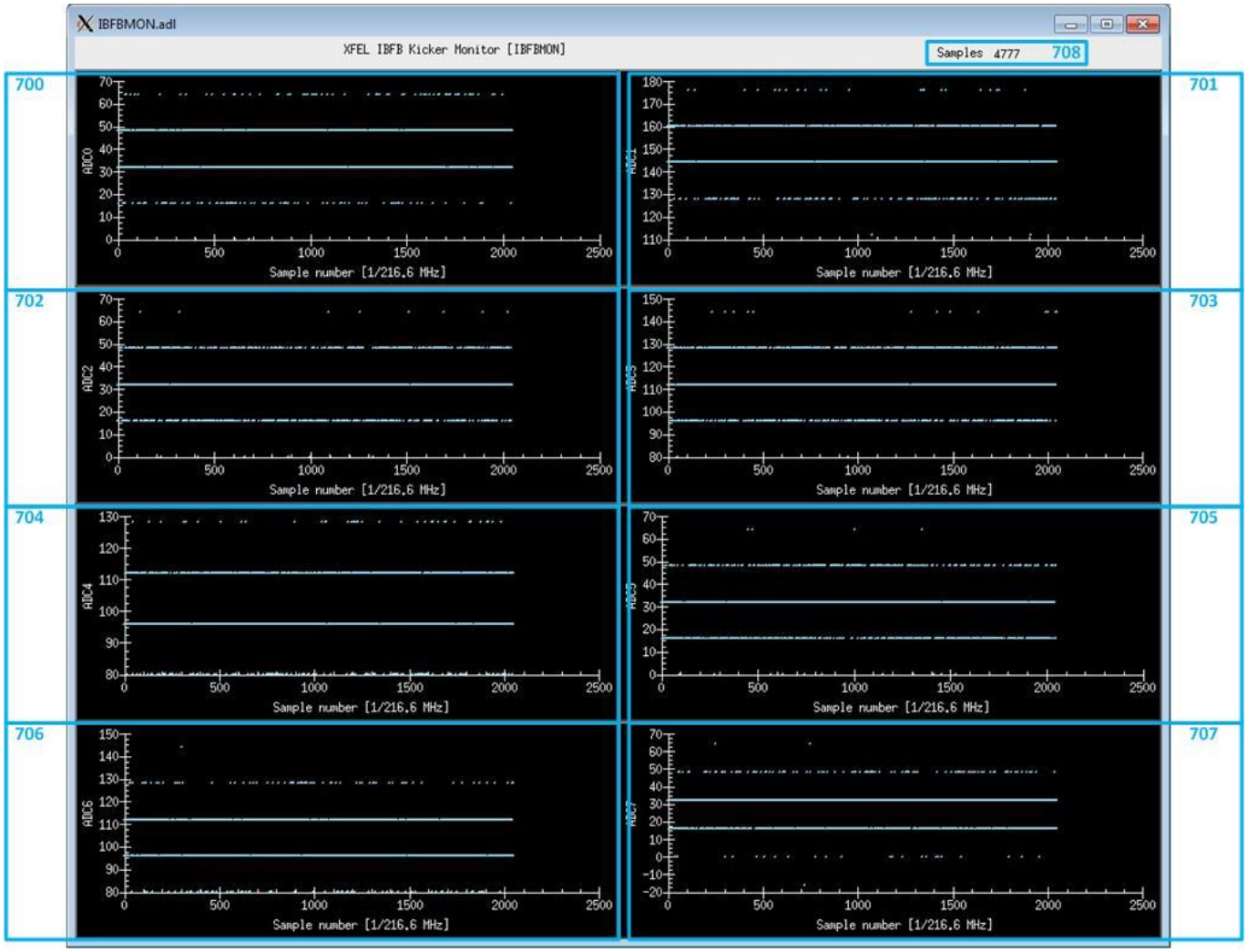


Figure 8.8: IBFB kicker output monitor

8.2 Latency Analysis and Measurement

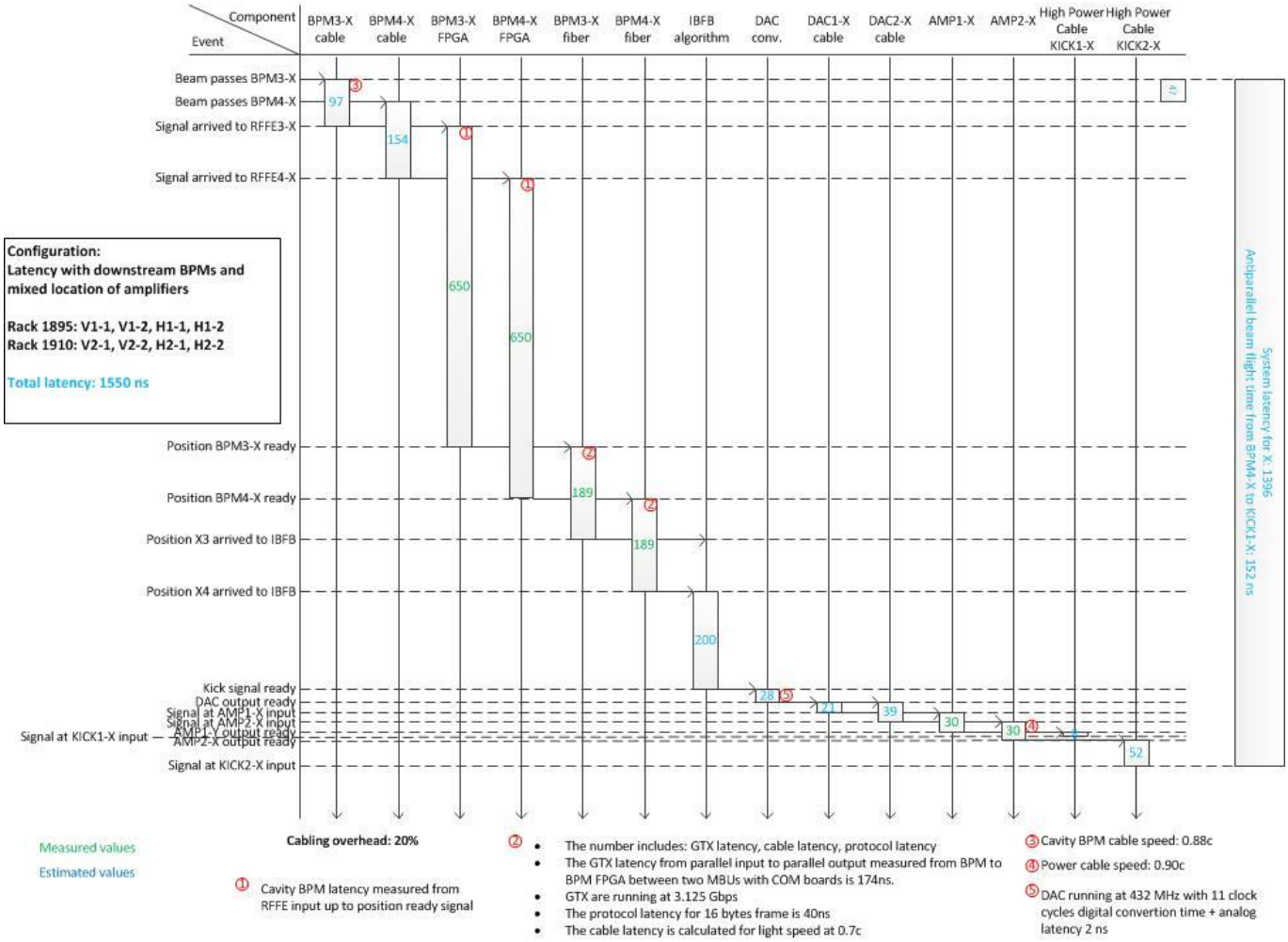


Fig 8.1 X Plane

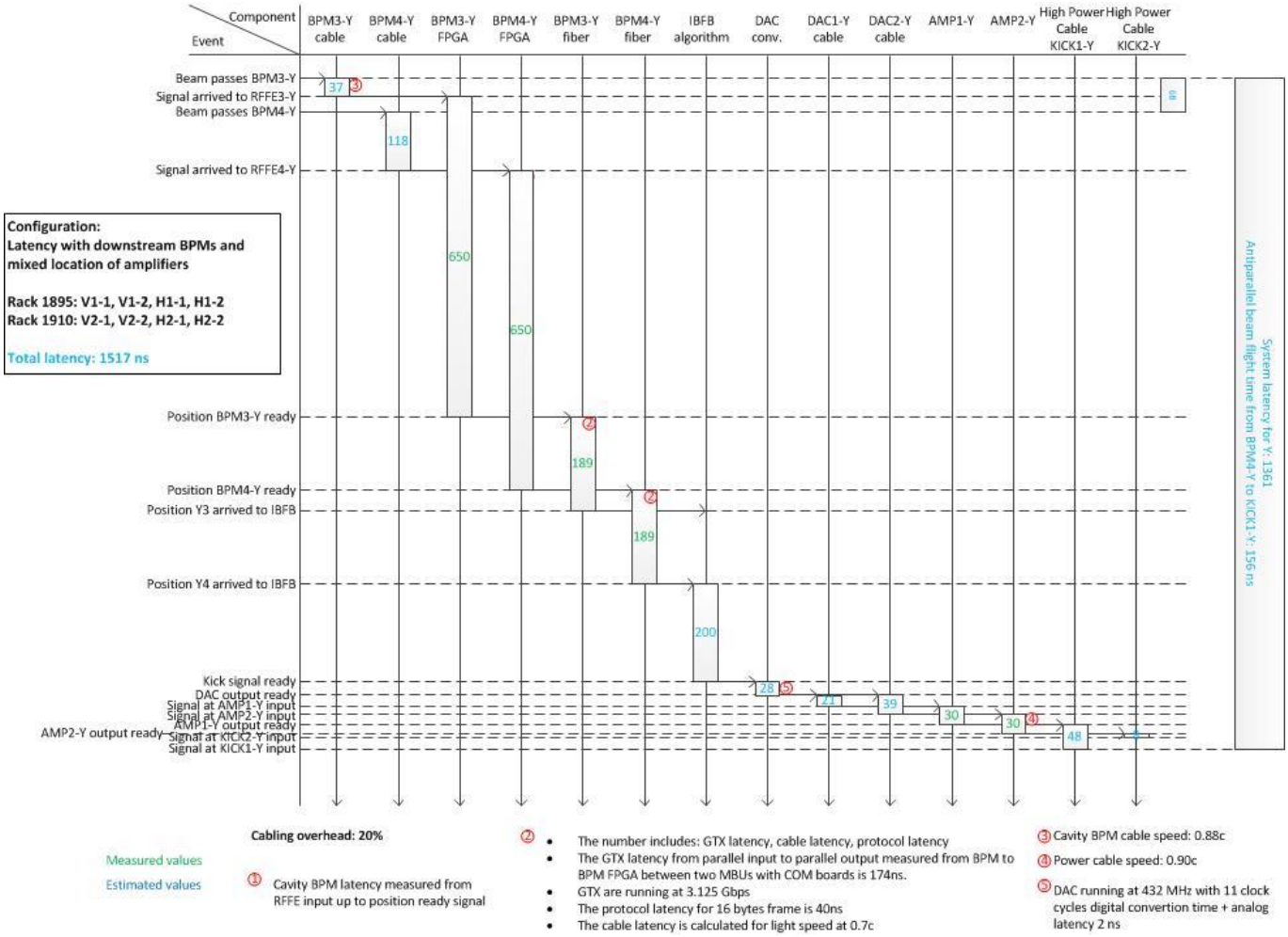


Fig 8.2 Y Plane

SASE1					
Device	Location [m]	Distance [m]	Latency [ns]	Latency in vacuum [ns]	Total Latency [ns]
BPME.2241.SA1	2247	0	189		
BPME.2241.SA1	2241	6			
IBFB Rack	1900	341	1652	1156	2997

SASE2					
Device	Location [m]	Distance [m]	Latency [ns]	Latency in vacuum [ns]	Total Latency [ns]
BPME.2209.SA2	2209	0	189		
BPME.2203.SA2	2203	6			
IBFB Rack	1900	309	1471	1030	2690

SASE3					
Device	Location [m]	Distance [m]	Latency in fiber [ns]	Latency in vacuum [ns]	Total Latency [ns]
BPME.2812.SA3	2812	0	189		
BPME.2806.SA3	2806	6			
IBFB Rack	1900	906	4342	3040	7571

Fig 8.3 Undulator Latencies

8.3 Auxiliary calculations

We measure the beam position at $B_2 = (x_{B2},\ x'_{B2})$. The set point at this position is $B_{2SP} = (x_{SP}, s'_{SP})$. and after transformation of the set point from position B_2 to position K_2 we obtain

$$K_{2SP} = M^{-1}_{K2B2} * B_{2SP}$$

which of course gives $K_{2SP} = (0, 0)$, and after transforming measured position B_{2M} to K_{2M} using equation

$$K_{2M} = M^{-1}_{K2B2} * B_{2M}$$

$$\begin{bmatrix} k_{2M} \\ k'_{2M} \end{bmatrix} = \begin{bmatrix} 1 & -L_{K2B2} \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} b_{2M} \\ b'_{2M} \end{bmatrix}$$

The beam position in front of the first kicker K_{1U} is transformed to the position after the second kicker K_{2D} with the transfer matrix $M_{K1K2} = \begin{bmatrix} 1 & L_{K1K2} \\ 0 & 1 \end{bmatrix}$ where L_{K1K2} is the distance between the first kicker and the second. And the transformation equation looks like

$$K_{2D} = M_{K1K2} * K_{1U}$$

In case of the active kickers additional two matrices have to be added to this equation

$$K_{2D} = M_{K2} * M_{K1K2} * M_{K1} * K_{1U} \quad (3.3.1.1)$$

Putting the matrix coefficients in equation 3.3.1.1 we obtain

$$\begin{bmatrix} k_{2D} \\ k'_{2D} \\ 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & \theta_{K2} \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & L_{K1K2} & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & \theta_{K1} \\ 0 & 0 & 1 \end{bmatrix} * \begin{bmatrix} k_{1U} \\ k'_{1U} \\ 1 \end{bmatrix}$$

which gives finally after matrix multiplication

$$\begin{bmatrix} k_{2D} \\ k'_{2D} \\ 1 \end{bmatrix} = \begin{bmatrix} k_{1U} + (k'_{1U} + \theta_{K1}) * L_{K1K2} \\ k'_{1U} + \theta_{K1} + \theta_{K2} \\ 1 \end{bmatrix}$$

When compare now the position of the beam after the kicker two with the desired set point at kicker two

$$K_{2SP} = K_{2D} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

then we can quickly calculate the required kick angle for both kickers

$$\begin{bmatrix} \theta_1 \\ \theta_2 \end{bmatrix} = \begin{bmatrix} -k'_{1U} - \dfrac{k_{1U}}{L_{K1K2}} \\ \dfrac{k_{1U}}{L_{K1K2}} \end{bmatrix}$$