European XFEL Timing System Receiver

xfel_timing
Revision 2_00_a

Firmware Data Sheet

Revision 1.0
PSI, Villigen, 30.08.2016

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1 Introduction

The European XFEL timing system receiver is a firmware component which was implemented by PSI on GPAC board in order to synchronize BPMs and IBFB with the uTCA timing system.

1.1 Purpose

The purpose of this document is to describe functionality of the EDK IP core.

1.2 History

Revision	Date	Author	Description
1.0	30.08.2016	W. Koprek	First version.

1.3 Features

The *xfel_timing_v2_00_a* has the following properties:

- SPLB46 interface with
  - configuration registers
  - receiver memory with timing data
- connects to MBU COM board or to RTMG
- decodes all messages send by uTCA timing system
- generates four configurable triggers from received events
- generates reset pulse
- generates 108MHz and 216MHz with reproducible phase to MO

1.4 Scope

Tbd.

1.5 Definitions, acronyms, and abbreviations

This document is based on the IEEE Recommended Practice for Software Requirements Specifications [1].

FPGA	Field Programmable Gate Array
Reg	Register. Mathematically z^-1

1.6 References

1. XFEL Timing System Specification, Version 2.3, 01.10.2013

2 Functional Overview

2.1 Firmware description

The component consists of gigabit link GTX which receives timing stream from uTCA system. The parallel data bytes together with the parallel recovered clock 130 MHz are connected to command decoder. The command decoder checks for the incoming commands and compares with the command table. The command table is configurable and contains list of commands which should be decoded by the command decoder. The data included in the commands are stored in the dual port memory under addresses defined by the command table. All data stored in the dual port memory are immediately accessible through the PLB Slave interface.

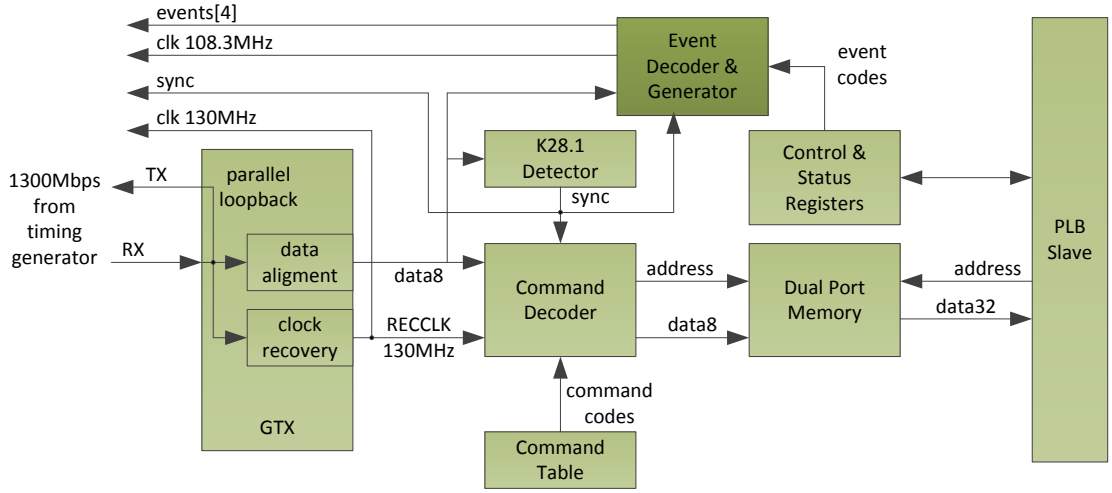


Figure 1. Block diagram of the firmware

The Event Decoder & Generator component detects only events coming from GTX. This component synthesizes 108 MHz clock to measure the event delay and to generate corresponding trigger. The component can generate up to 4 triggers which can be generated on any event configured in the control registers.
The K28.1 Detector is used to detect the special K-character which is used to synchronize components and clock dividers.

2.1.1 Clock generation

The clocks needed locally in the GPAC board can be synthesized from the 1.3 GHz stream in the fiber link. The Figure 2 shows how the clocks are synthesized in the FPGA.

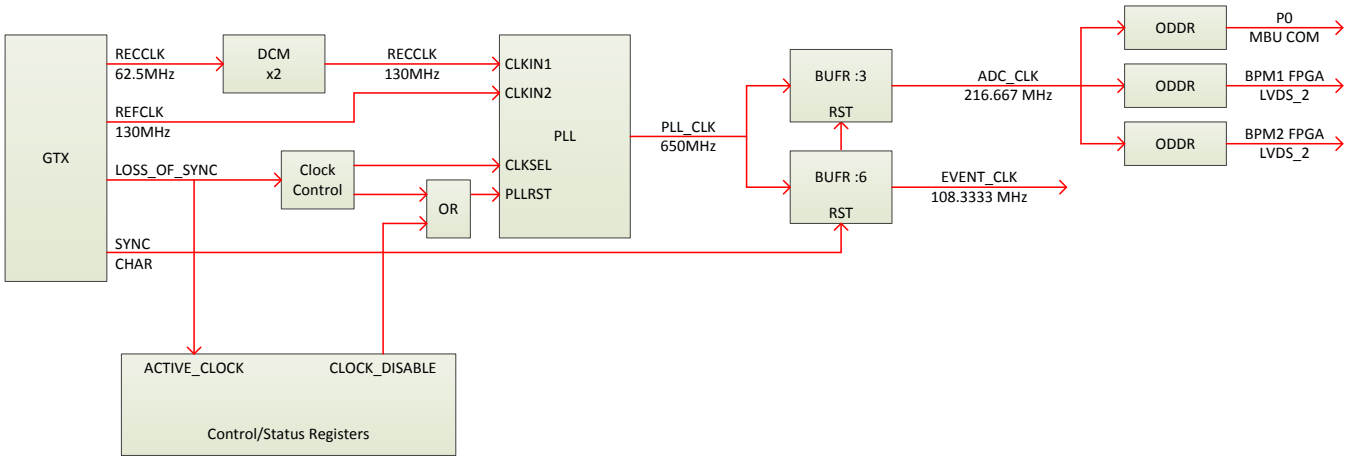


Figure 2. Clock synthesis from 1.3GHz serial stream

Since the GTX component has 16-bit parallel interface the recovered clock is a 1.3 GHz divided by 20 (20 is two bytes in 8/10 bit encoding) which gives 62.5 MHz. Then this clock is multiplied in a DCM by two and connected to one of the PLL clock inputs. The second PLL clock input is connected to reference clock REFCLK which is 130 MHz and comes from local free running oscillator. The input clock is selected automatically by the component. If the LOSS_OF_SYNC signal is active it means that the timing signal is not received correctly. In this case the PLL select REFCLK. If the timing stream is correctly received by GTX and LOSS_OF_SYNC signal is low then the PLL switches automatically to RECCLK. The PLL multiplies the input 130 MHz clock and generates 650 MHz. The 650 MHz clock is connected to two regional buffers BUFR in the FPGA which have built-in dividers. One BUFR delivers 216.667 MHz clock, the other one delivers 108.333 MHz clock. The dividers are reset by the synchronization character 28.1 in order to achieve reproducible phase with respect to the master oscillator. The 108 MHz clock is used to generate triggers from events and measure the trigger delays. The 216 MHz clock is used for the ADC clock on the GPAC piggybacks.

2.2 Config parameters

Param name	Type	Description
C_TIM_ENA_EVENTS	uint8	0 – do not compile trigger generator 1 – compile trigger generator

2.3 Ports

Port name	Type	Description
I_GTX_REFCLK_IN	std_logic	Reference clock for the GTX – 260 MHz.
I_GTX_RX_N I_GTX_RX_P	std_logic_vector(1 downto 0)	RX pins of the GTX tile. Connect timing to GTX1 on GPAC
I_GTX_TX_N I_GTX_TX_P	std_logic_vector(1 downto 0)	TX pins of the GTX tile. Connect timing to GTX1 on GPAC
I_TIM_TRG_EXT	std_logic	TTL trigger input on MBU COM board connected either to LEMO input or to RJ45 input. In case of RJ45 this is trigger input 1
O_TIM_108M_EVENTS	std_logic_vector(3 downto 0)	Four trigger generated by the trigger generator
O_TIM_216M_CLK_P0	std_logic	216 MHz clock output going to the SMA output on the MBU COM board
O_TIM_216M_CLK_BPM1	std_logic	216 MHz clock output going to BPM1 FPGA

O_TIM_216M_CLK_BPM2	std_logic	216 MHz clock output going to BPM2 FPGA
O_REFCLKOUT	std_logic	Reference clock output used to measure the frequency
O_TIM_130M_CLK	std_logic	130 MHz parallel clock recovered from the 1.3 GHz serial stream
O_TIM_130M_SYNC	std_logic	Reset pulse generated by the 28.1 character decoder. It is synchronous to the 130 MHz clock
O_TIM_108M_CLK	std_logic	108 MHz clock. The triggers are synchronizes to this clock

2.4 Register map

The registers are used to configure and monitor the EXFEL timing receiver component.

Address offset is 0x00000100

Addr	Type	Access	Description	Panel
0x0000	uint8	RO	GTX loss of synchronization: 0 – the GTX is synchronized and received timing stream 1 – GTX not synchronized	100
0x0001	uint8	RO	RJ45 cable connected. When is high it means that the RJ45 cable is connected to the MBU COM board. This bits detects presence of the 5 volts on the RJ45 connector.	100
0x0002	uint8	RO	Reserved	
0x0003	uint8	RO	The 650 MHz PLL locked	100
0x0004	uint8	RW	Event code for the trigger 0	107
0x0005	uint8	RW	Event code for the trigger 1	107
0x0006	uint8	RW	Event code for the trigger 2	107
0x0007	uint8	RW	Event code for the trigger 3	107
0x0008	uint32	RW	GTX configuration. Do not write to this register.	
0x000C	uint8	RW	Trigger source: 0 – trigger from optical fiber 1 – trigger from RFJ45 or LEMO input	
0x000D	uint8	RW	Reserved	
0x000E	uint8	RW	Reserved	
0x000F	uint8	RW	Disable clock synchronization by K28.1: 0 – enabled 1 - disabled	
0x0010	uint32	RO	GTX status: Bit 16 – GTX loss of synchronization Other bits are reserved	
0x0014	uint16	RO	Reserved	
0x0016	uint16	RO	Number of command per pulse received from the XFEL timing system	
0x0018	uint16	RO	Reserved	
0x001A	uint16	RO	GTX loss of synchronization counter	
0x001C	uint16	RO	Reserved	
0x001E	uint16	RO	Number of events per pulse received from the EXFEL timing system	

2.5 Memory map

The memory contains data received from the uTCA timing generator. The payload data decoded in the Command Decoder are stored in this memory. The decoded data is stored byte by byte in the memory in the same order as they are sent. For detailed description of each command content see the XFEL Timing System Specification document.

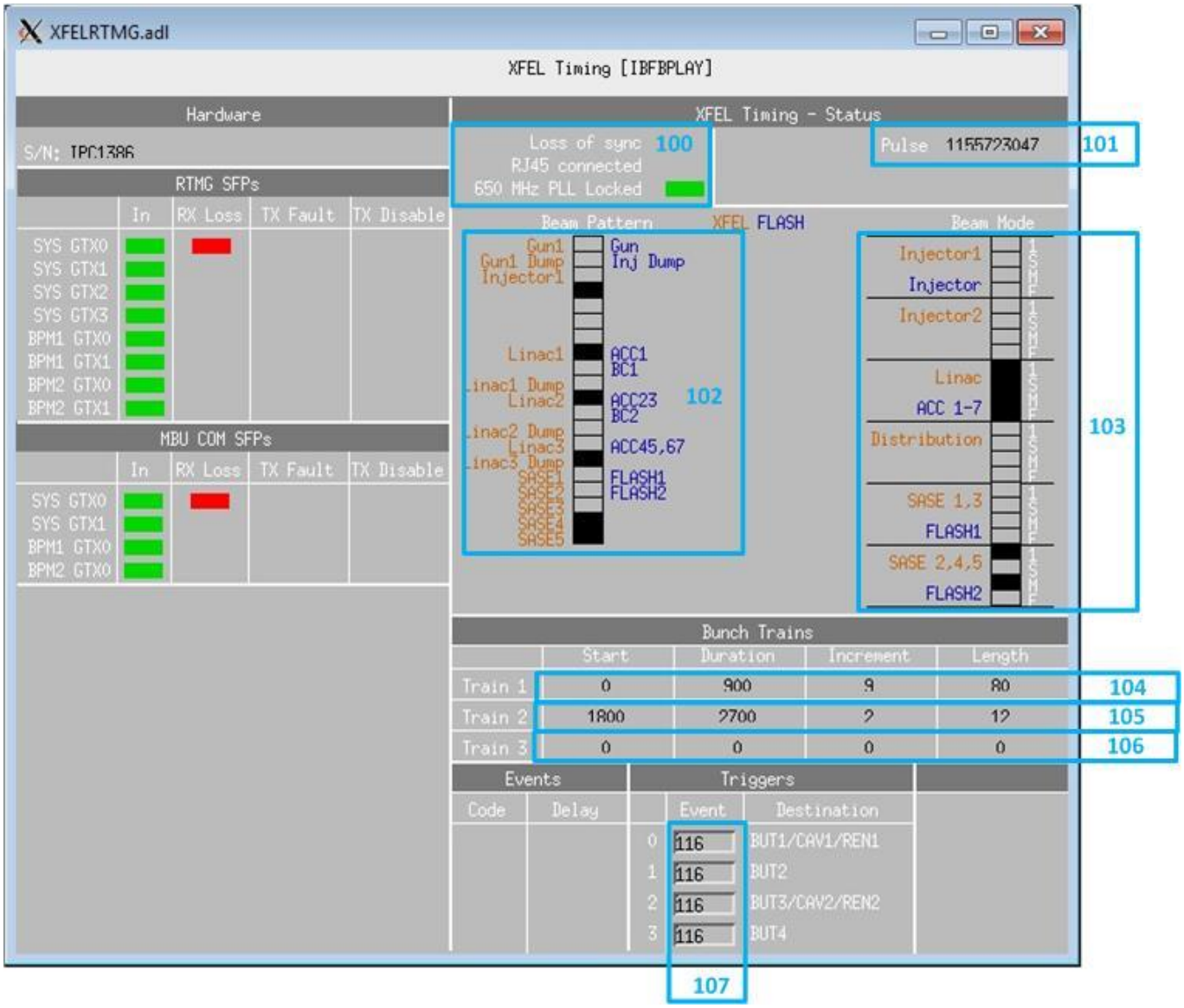
Address offset is 0x00008000

Addr	Type	Description	Panel
0x0000	uint64	Pulse number. Check XFEL Timing System Specification for details.	101
0x0008	double	Date and time. Check XFEL Timing System Specification for details.	
0x0010	uint32	Beam mode. Check XFEL Timing System Specification for details.	103
0x0014	uint32	Section pattern. Check XFEL Timing System Specification for details.	104
0x0018	uint8	Event 0 code	
0x0019	uint32	Event 0 delay	
0x001D	uint8	Event 1 code	
0x001E	uint32	Event 1 delay	
…	…	…	
0x00DB	uint8	Event 39 code	
0x00DC	uint32	Event 39 delay	
0x00E0	uint32	Train 1 start bucket	104
0x00E4	uint32	Train 1 start duration	104
0x00E8	uint32	Train 1 start bunch spacing	104
0x00EC	uint32	Train 1 start bunch number	104
0x00F0	uint32	Train 2 start bucket	105
0x00F4	uint32	Train 2 start duration	105
0x00F8	uint32	Train 2 start bunch spacing	105
0x00FC	uint32	Train 2 start bunch number	105
0x0100	uint32	Train 3 start bucket	106
0x0104	uint32	Train 3 start duration	106
0x0108	uint32	Train 3 start bunch spacing	106
0x010C	uint32	Train 3 start bunch number	106
0x0110	uint32	Bucket 0 of full bunch patter. Check XFEL Timing System Specification for details.	
…	…	…	
0x71E8	uint32	Bucket 7221 of full bunch patter.	

2.6 FPGA Resources

Version	Flip Flops	LUTs	BRAM36
C_TIMING_ENA_EVENTS = 1	1226	1236	8

2.7 MEDM Panel



2.8 Design constraints

The design is structural and hence bound to the Xilix® Virtex5 FPGA.