TITLE :

IFC_1210 User's Guide

KEY WORD :	ACCESS CODE :
IOxOS Quality System, P2020, HSID, PCI Express resources description,	IOxOS Confidential

SUMMARY :

This document provides detailed informations for programmer and scientific users of the IFC210 equipment includes static options, external connectors assignment, visual indicators, PCI Express resources mapped in the CONFIGURATION Space, IO Space and MEMORY Space.
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PROJECT REFERENCES

DOCUMENT REFERENCE No:	INTERNAL_1 :	INTERNAL_2 :

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Table of Contents

15

Index of Tables

Illustration Index

1. Introduction

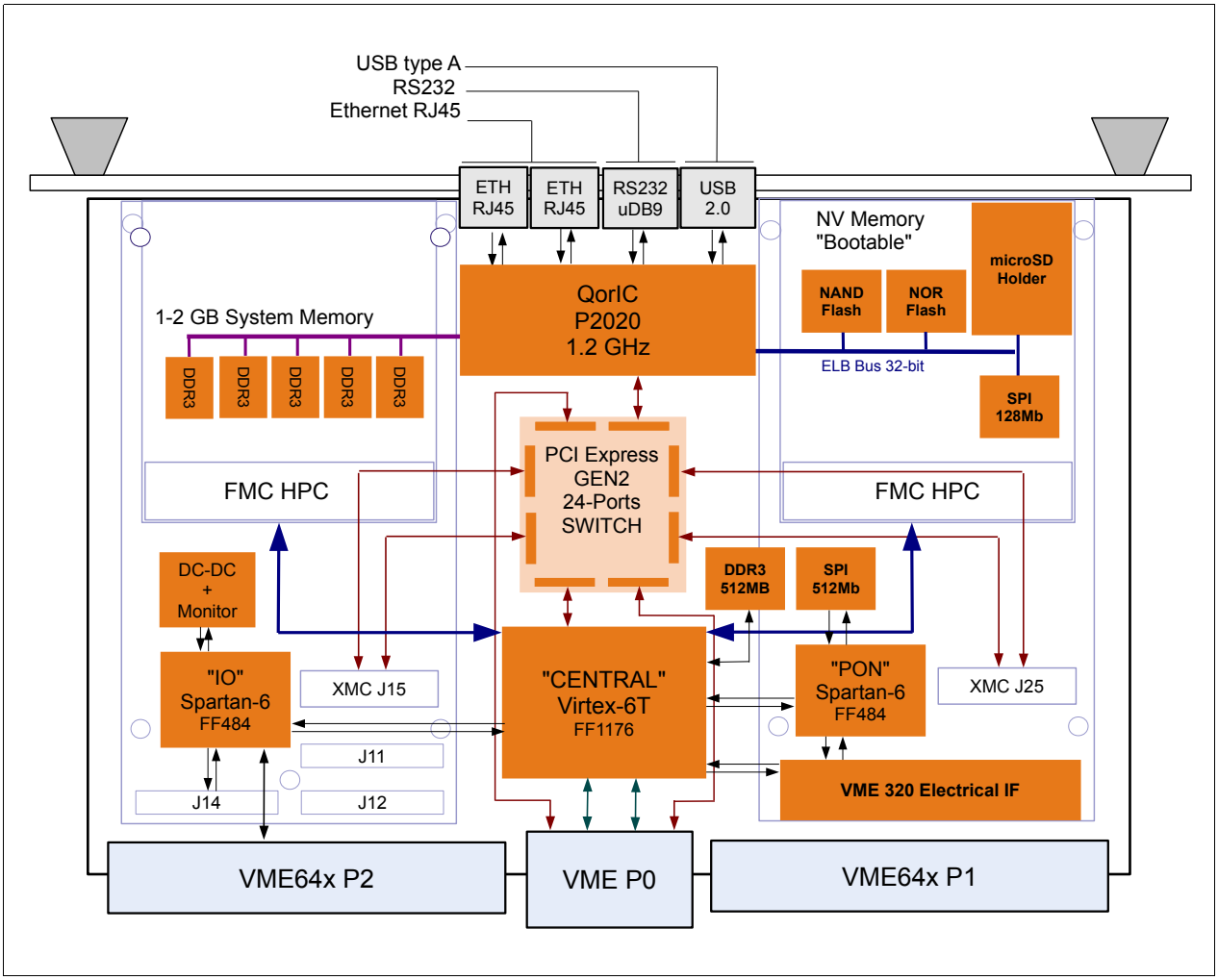

Illustration 1 : IFC_1210 Functional Diagram

Overview

IOxOS Technologies introduces the IFC_1210, a 6U VME64X highly configurable Single Board Computer with embedded FPGA capability and VITA 42.3 XMC, IEEE1386.1 PMC, VITA57 FMC. The IFC_1210 is built around a high performance switched PCI Express GEN2 providing low latency and high bandwidth extension capability.

The IFC_1210 is general purpose high capacity FPGA platform associated with a high performance computing dual-core PowerPC. It is well adapted for complex real-time applications and sophisticated data acquisition.

The IFC_1210 integrates the latest generation of Freescale PowerPC QorIQ processors. The P2020 provides dual-core capability running at 1.2 GHz with low power operation (< 8[W] Typ.). It is implemented with large System Memory (up to 2 GBytes), non volatile memory NOR, NAND and multiple IO capabilities as dual Gigabit Base-T Ethernet .

The on-board Xilinx Virtex-6T FPGA implements a high performance PCI Express centric Network on Chip

(NoC) switched interconnection. This NoC architecture provides a non-blocking, controlled low-latency and high-throughput bandwidth interface between the data producer and consumer.

The VME64x interface, which is also integrated in the FPGA, is implemented with a direct transparent low latency PCI Express / VME64X Bridge. It supports all Master/Slave VME64x modes of operation with Slot_1 System Controller.

The IFC_1210 user's application are supported by a complete FPGA design kit “TOSCA II”.

Main Features

- 6U VME64x Single Board Computer
- Freescale PowerPC P2020 computing core
  - QorIQ P2020 1.2 GHz
  - 1 or 2 GBytes DDR3 System Memory with ECC
  - NAND Flash, NOR Flash
  - Dual 10/100/1000 BaseT Ethernet
  - Single RS232
  - USB 2.0 Host Controller
- High performance PCI Express G2 24-ports switch
  - Multiple NTB ports
  - Multicast support
  - SSC / CFC clocking
- Dual VITA 42.3 XMC Mezzanine
- Single IEEE P1386.1 PMC Mezzanine
- Dual VITA57 HPC FMC Mezzanine
- UHM P0 extension (7 Gb/s)
- VME64x Master/Slave with 2eSST support
- Multi-board time synchronization
- Thermal and Power supplies monitoring
- Xilinx Virtex-6T/FF1156 CENTRAL FPGA
- Xilinx Spartan-6/ FF484 IO FPGA
- Complete FPGA Design Kit “TOSCA II”
- Linux / VxWorks BSP
- Target applications:
  - Upgrade of legacy VME64x based real-time control systems
  - Aerospace integration RIG systems, flight simulators & test equipment with advance IO capabilities

Introduction

The IFC_1210 platform has been designed to support high performance computing in scientific and aerospace real-time applications. The key main was to provides the key items to support these high demanding applications

- Multi-core PowerPC (P2020) with RT OS support.
- High performance Xilinx Virtex-6T FPGA with DSP computing support.
- Standard application customization with XMC, PMC and FMC (VITA57) Mezzanine slots.
- Standard real-time interconnect infrastructure of several GBytes/s. (PCI Express GEN2)
- External expansion capability for large system built

The IFC_1210 carrier is ready to be equipped with any available Virtex-6T device in FF1156 pins package.

- LX130T, LX195T, LX240T, LX365T
- SX315T, SX475T

PCI Express Centric Architecture

The IFC_1210 is built around the latest generation of PCI Express GEN1/GEN2 non-blocking switch IDT PES32NT24AG2 providing eight (8) PCI Express x4 GEN1/GEN2 Ports.

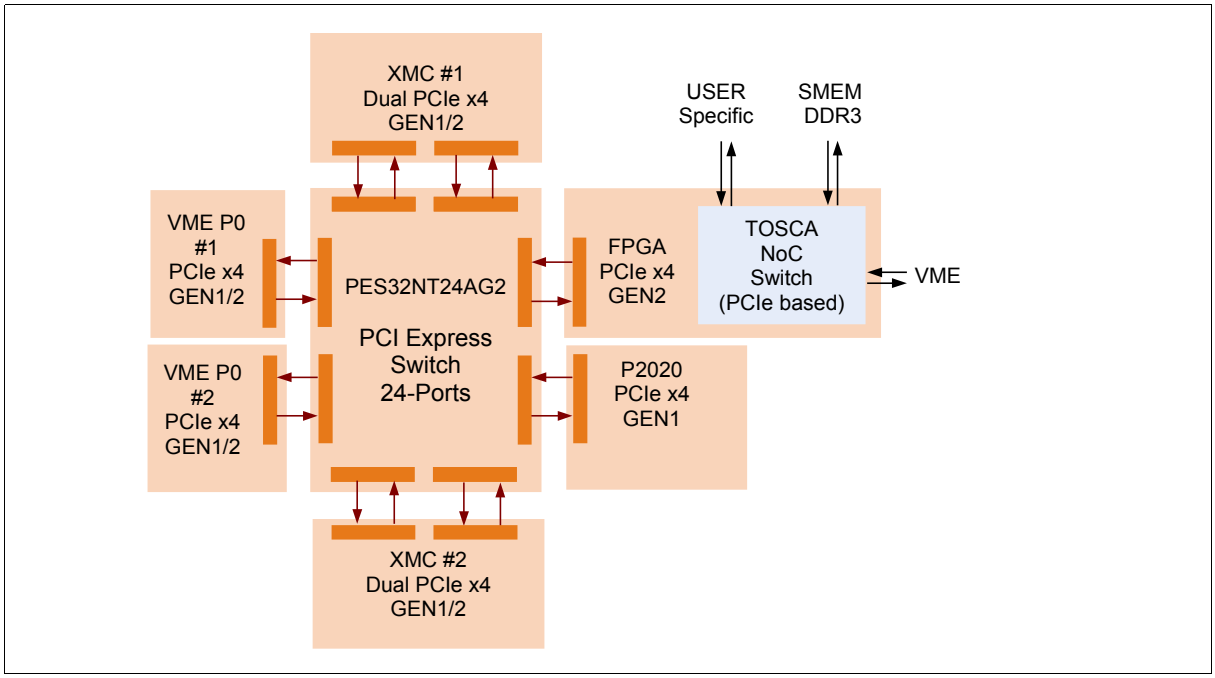

Illustration 2 : IFC_1210 PCI Express Infrastructure

The PCI Express topology is naturally extended inside the FPGA fabric by means of TOSCA II 's native Network on Chip (NoC) switch. This provides an unified PCI Express centric architecture.

IDT PES32NT24AG2

The IDT PES32NT24AG2 non-blocking PCI Express switch supports advanced modes of operation as:

- PCI Express 2.1 compliant (2.5 Gb/s or 5.0 Gb/s)
- 256 Gbps aggregate switching capacity
- Low latency cut-through architecture with advanced QoS support
- Up to eight(8) NT endpoint with 6 BARs per NT
- Multicast capability over the twenty-four(24) ports, including the NT
- Dynamic port reconfiguration (Upstream, Downstream and NT Bridge)
- Integrated multiple DMA controllers with link list capability
- Per lane SERDES configuration (De-emphasis, Receive equalization and Drive strength)
- Automatic lane reversal and link width negotiation
- Flexible port clocking mode SSC/CFC

IDT External PCI Express Expansion

The internal IFC_1210 PCI Express network can be expended externally thanks to following IO capabilities.

- XMC VITA 42.3. Four(4) PCI Express x4 External Cabling (XMC_3105)
- VME P0 UHM connector. Two(2) PCI Express x4 External Cabling or CX4 copper/optical.

This expansion capability allows to built a local high performance, memory mapped sub micro-second real-time network interconnecting multiple IFC_1210 together or high performance multi-core based workstations.

QorIQ P2020 Computing core

The PowerPC P2020 microprocessor is supported by the following memory resources. All non-volatile resources can be statically selected as Bootable.

- 1 or 2 GBytes DDR2-600 System Memory
- 256 MBytes NAND Flash Memory with ECC
- 16 MBytes NOR Flash Memory
- 128 Mbit SPI Serial Flash Memory

The P2020 PCI Express port can be configured as Root Complex (RC, which manages the local PCI Express enumeration) or as End Point (EP).

P2020 IO Resources

The P2020 provides the following IO on the front panel:

- Two RJ45, Ethernet 10/100/1000 Base-T
- One µDB9, RS232
- One type A USB 2.0 Host Adapter
- JTAG COP debugging socket (on-board access only)

Others Resources

- Quad frequency Programmable VCXO (IDT 8N4QV01)
- Dual Hot swap controller (MAX5970)
- PCI Express – PCI Bridge (PLX PEX8112)

VME64x Legacy Interface

The "CENTRAL" Virtex-6T FPGA embeds a proprietary IP core providing a complete Master/Slave VME64x interface. The electrical interfacing is based on VME320 ETL technology, supporting full speed 2eSST and 2eVME protocols.

The Master/Slave VME64x IP core is part of the TOSCA II FPGA Design Kit infrastructure and therefore provides transparent bridging capability such as PCI Express to VME64x.

The VME Slave interface implements the legacy VME/VME64 addressing configuration with static switches and/or VME64x CR/CSR. The VME Slave handles all addressing modes and is fully programmable through an in-going scatter-gather.

The VME Master interface, driven by the internal FPGA infrastructure supports also all VME addressing mode including 2eVME and 2eSST.

In addition, the VME Master integrates a complete VME Slot-1 function, Interrupt Generator/Handler and a global time synchronization distribution over the back-plane.

Additional capabilities as VME Master Read Modify Write (RMW) , LOCK with ADOH addressing and Auto-ID are also integrated in standard VME IP core.

VME64x P2 User IO

The VME P2 User IO (rows A & C / 64 signals 32+32) and the (rows D & Z / 48 signals 32+16) are directly wired to the Spartan-6 IO FPGA. The VME P2 IO signalling is legacy LVTTL.

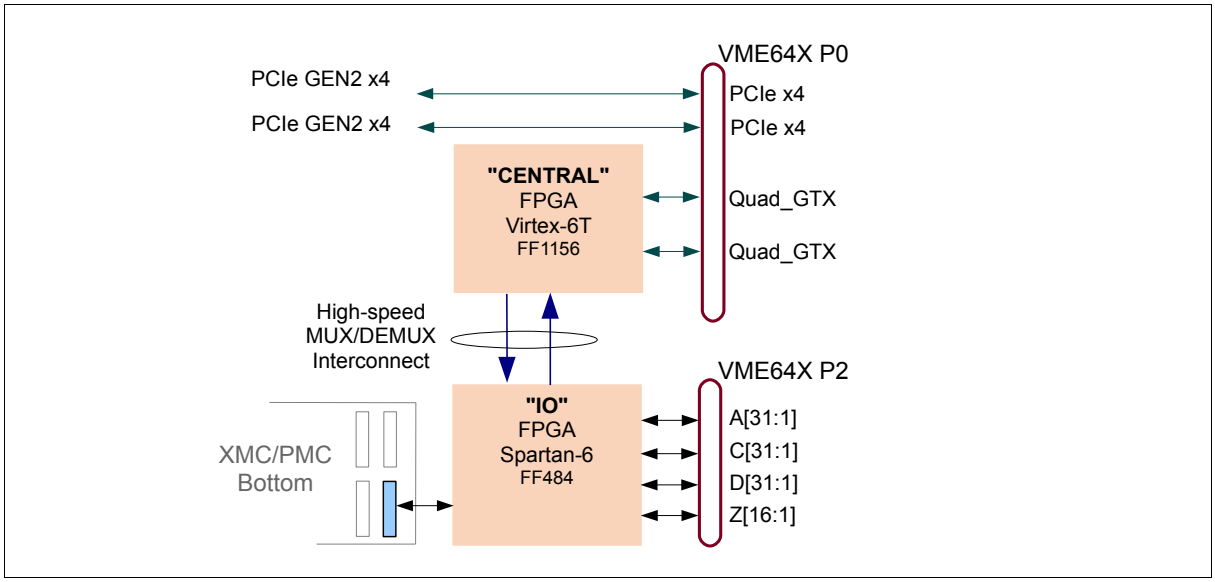

Illustration 3 : IFC_1210 VME64x P2 User IO

VME64x P0 High-speed Extension

The IFC_1210 VME64X P0 is implemented with new 3M UHM connector generation, supporting multiple >5 GBit/s interfaces. Through theses connections, the internal PCI Express GEN2 and the Virtex-6T GTX transceiver can be used on the rear IO extension.

- Two(2) PCI Express x4 GEN2
- Two(2) Virtex-6T Quad_GTX
- 16 GPIO wired to the IO FPGA Spartan-6

The MPR_1260 rear_IO extender unit,can extend the P0 Gbit connections over external cabling (PCI Express External cable or CX4 copper/optical)

XMC VITA 42.1

The IFC_1210 provides two VITA42.3 XMC Mezzanine sites with fully configurable PCI Express interfaces (Single PCIe x8, Dual PCIe x4, Quad PCIe x2 or Octal PCIe x1

PMC IEEE1386.1

The IFC_1210 provides one IEEE1386.1 PMC Mezzanine site with 32-bit PCI 3.0 interface (33/66 MHz). The User's IO connector (Jn14), common for PMC#1 and XMC#1 is directly wired to the „IO“ FPGA acting as user configurable User IO router with VME P2 and „CENTRAL“ FPGA.

FMC VITA 57.1

The IFC_1210 provides two VITA57.1-R2010 FMC Mezzanine sites, with High Pin Count (HPC) interfaces. The two FMC interfaces are diretly wired to the Virtex-6T “CENTRAL“ FPGA.

High Speed GTX Transceivers

The XILINX Virtex-6T FF1136 device provides up to 20 GTX low power Gigabit transceivers. These physical interfaces, running up to 6,5 Gb/s are dedicated to high speed serial communications such as PCI Express GEN1/GEN2, SRIO, 10G Ethernet, and USB 3.0 among others.

The TOSCA II FPGA Design Kit integrates direct support for PCI Express GEN2 EP. The IFC_1210 physically supports PCI Express through the Virtex-6T GTX transceivers, therefore PCI Express can be supported through the MPF IO Expansion connectors and/or the new high-speed VME64x P0 connector.

PCI Express GEN2 can be supported through copper “External Cabling” and/or optical CX4 plug-in adapter.

Virtex-6T "CENTRAL" FPGA Support

The Virtex-6T “CENTRAL” FPGA is organized in a hierarchy level composed of two main blocks:

- The IFC_1210 IP core integrating the basic carrier board infrastructure as NoC Switch, PCI Express EP, VME64x Master/Slave, the DDR3 shared memories controller with IDMA and the Interrupt controller
- Two USER blocks, one for each MPF IO connector, fully configurable by the end user

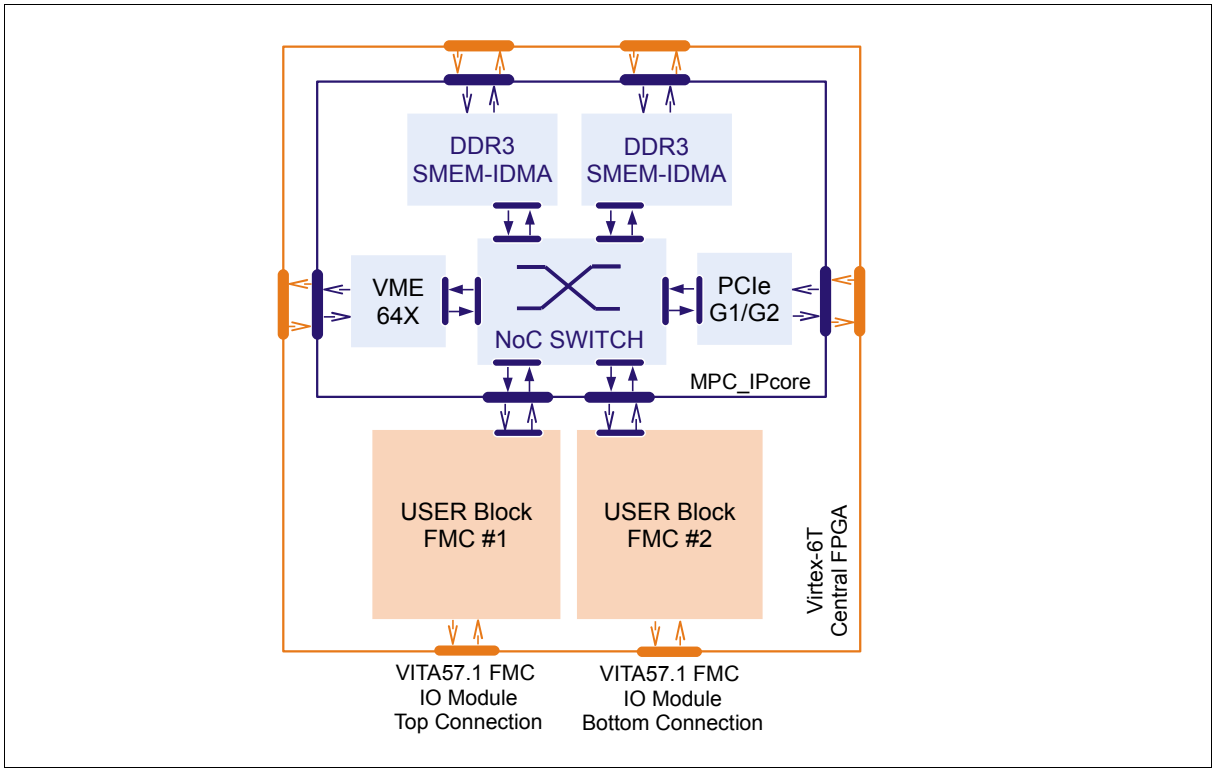

Illustration 4 : IFC_1210 TOSCA II Implementation

The IFC_1210 TOSCA II is released in binary format (NGC) or in source format (VHDL), along with generic USER Block examples and all needed files for the implementation of fully functional FPGA ("CENTRAL and "IO") for the IFC_1210.

TOSCA II FPGA Design Kit

Conventional design kits offer a set of IP cores along with implementation examples. IOxOS Technologies goes one step further releasing the TOSCA II FPGA Design Kit, a comprehensive system design environment that covers all the path, from the SW application to the FPGA user code.

The TOSCA II FPGA Design Kit is delivered with full VHDL source code together with a set of test-benches and Bus Functional Models (BFM) to set up a complete VHDL simulation environment for functional verification purposes. This simulation environment is supported by the main HDL simulation tool vendors. (Model*Sim*)

The TOSCA II architecture is based on a PCI Express switch centric structure implementing a memory mapped model with segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane).

The TOSCA II FPGA Design Kit enhances the versatility of the IFC_1210 solution, providing the user with a powerful tool for implementation and integration of custom applications within the IFC_1210 on-board Virtex-6T "CENTRAL" FPGA.

Software Support

The TOSCA II FPGA Design Kit is supported with the following software items:

- LINUX device drivers (PCI Express & VME64x)
- User library with examples

- IFC_1210 specific library
- XprsMON and FPGA Built utilities

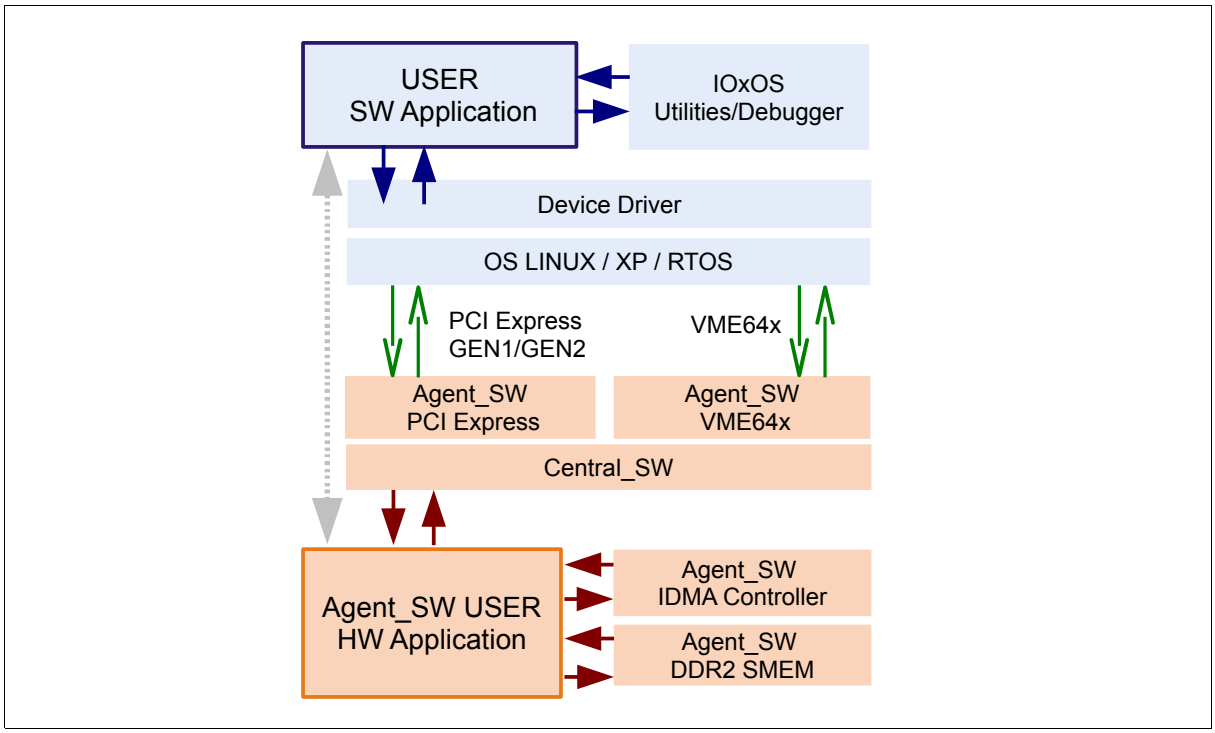

Illustration 5 : IFC_1210 TOSCA 2 SW Integration

XprsMON is a Linux application linked with the TOSCA II user library which allows the user to interactively perform a set of commands to operate the TOSCA II infrastructure :

- Patch, Examine, Deposit & Display operations on Memory and I/O Space references
- Patch, Examine, Deposit & Display operations on VME64x references
- Exercise Interrupts, Global_Time and DMA
- Flash Memory programming (FPGA bit stream download

Debugging & Integration Support

The IFC_1210 unit integrates a local JTAG chain connecting all on-board FPGA. A standard XILINX TAP port provide direct access from the XILINX ISE Design Suite (ChipScope PRO and iMPACT).

Additionally specific software tools are provided to upgrade the FPGA bit-streams in the Serial FLASH devices from the VME64x or PCI Express interfaces.

1.1 IFC_1210 Accessories

The IFC_1210 is supported with following complements products.

1.1.1 MPR_1260

VME64x Rear IO unit connected through the VME P2 USER IO and the VME P0 UHM. The unit provides high-speed extension as dual PCI Express x4 External Cabling connectors and dual CX4 connectors.

→ Refer to MPR_1260 data-sheet

1.1.2 FMC_3106

Single width FMC unit equipped with a XILINX Spartan-6 XC6SLX45-2-FFG484 FPGA. The FMC front panel provides direct access to four(4) SMA connectors and to the dedicated XILINX TAP port.

→ Refer to FMC_3106 data-sheet

1.2 Acronyms and Abbreviation

Following table sums up specific abbreviation and acronyms used in this document.

ABBREVIATION	MEANING
ADC	Analogue to Digital converter
BFM	Bus Functional Model (VHDL related)
DAC	Digital to Analogue converter
DAQ	Data Acquisition
DUT	Device Under Test
FPGA	Field Programmable Gate Array
HRS	Hardware Requirements Specification document. List of precisely and labelled specification items
MPF	IFC_1210 front end module
SIMENV	Simulation Environment (VHDL related)
PCI Express / PCIe	Serial based PCI Interface
PLL	Phase Locked Loop
RMW	Read Modify Write
TOSCA II	IOxOS Technologies FPGA Design Kit based on NoC technology.
VHDL	Hardware description language

Table 1.1 : List of Acronyms and Abbreviation

1.3 TOSCA II Documentation

The TOSCA II documentation is organized around seven(7) user's guide, summarized in following table :

#	Document	Comments
1	Tosca2_Architecture_UG	General TOSCA II user's guide. Provide detailed technical description of the architecture and its implementation.
2	Tosca2_Implementation_UG	TOSCA II Example implementation guide.
3	Tosca2_AgentSW_PCIe_EP_UG	TOSCA II PCI Express Agent_SW description
4	Tosca2_AgentSW_VME64_UG	TOSCA II VME64x Master/Slave Agent_SW description
5	TOSCA2_AgentSW_SMEMIDMA_UG	TOSCA II DDR2 Memory Controller and Integrated DMA Agent_SW description.
6	Tosca2_AgentSW_USER_UG	TOSCA II USER Block Agent_SW description.
7	Tosca2_SUSER_UG	TOSCA II “Simple USER” Block description

Table 1.2 : TOSCA II Documentation Architecture

1.4 Technical References

Following table sums up the related technical references from third parties supplier used on the IFC_1210. Theses documentations could be required for user specific software/firmware support. Some of them are only available under NDA.

REF	Component	Documentation	Source
{20}	FPGA Virtex-6T	DS153 Virtex-6 Family overview DS152 Virtex-6 Data Sheet DS153 Virtex-6 CXT Family Data Sheet UG360 Virtex-6 FPGA Configuration UG361 Virtex-6 FPGA SelectIO resources UG362 Virtex-6 FPGA Clocking Resources UG363 Virtex-6 FPGA Memory Resources UG364 Virtex-6 FPGA Configurable Logic Block UG366 Virtex-6 FPGA GTX Transceiver UG370 Virtex-6 FPGA System Monitor UG517 Virtex-6 FPGA Integrated Block for PCI Express + ... Others user specific	XILINX
{21}	FPGA Spartan-6	DS160 Spartan-6 Family overview DS162 Spartan-6 Data Sheet UG380 Spartan-6 FPGA Configuration UG381 Spartan-6 FPGA SelectIO resources UG382 Spartan-6 FPGA Clocking Resources UG383 Spartan-6 FPGA Memory Resources UG384 Spartan-6 FPGA Configurable Logic Block + ... Others user specific	XILINX
{22}	QorIQ P2020	P2020 QorIQ Integrated Processor Hardware Specifications P2020 QorIQ Integrated Processor Reference Manual P2020 QorIQ Integrated Processor Chip Errata (NDA required)	Freescale
{23}	PES32NT8AG2 PES32NT24AG2	IDT PES32NT8AG2 Data Sheet IDT PES32NT8AG2 Preliminary User Manual (NDA required) IDT PES32NT24AG2 Data Sheet IDT PES32NT24AG2 Preliminary User Manual(NDA required)	IDT

REF	Component	Documentation	Source
{24}	PEX8112	PEX8112 User Manual	PLX
{25}	S25SFL129	S25FL129P Data Sheet	SPANSION
{26}	KSZ9021RN	KSZ9021GN Data Sheet	MICREL
{27}	IDT8N4Q001	IDT8N4Q001 Data Sheet RevG (NDA required)	IDT
{28}	MAX5970	MAX5970 Dual Hit-Swap Controller with 10-bit Current and Voltage Monitor Data Sheet	Maxim
{29}	BMR 463	BMR 463 Digital PoL Regulator Technical Specification PMBus Specification Part_I PMBus Specification Part_II	Ericsson
{30}	LM95235	LM95235 precision Remote Diode Temperature sensor with SMBus Interface Data Sheet	NS
{31}	CDCLDV110A	CDCLDV110A Data Sheet	TI
{32}	CDCLDV2104	CDCLDV2104 Data Sheet	TI
{33}	SY89574A	2:1 Multiplexer LVDS for	MICREL
{34}	AT24C256	Serial Flash EEPROM	ATMEL
{35}	S29GL128P11TFI010	NOR 16-bit Flash EPROM	SPANSION
{36}	HY27F082G2B	NAND 8-bit Flash EPROM	HYNIX
{37}	DS1339U-33	RTC Real Time Clock	MAXIM
{38}	SP3232EEY-L	RS232 Transceiver	EXAR
{39}	USB3300	USB 2.0 PHY	SMSC

Table 1.3 : IFC_1210 Technical Documents

1.5 General Information

1.5.1 Ordering Informations

Reference	"CENTRAL" FPGA	DDR3	VME_P0	IDT 8N4QV01	Environmental
IFC1210-A0	LX130T	512M	UHM	YES	0 - 50 [°C]
IFC1210-A1	LX130T	512M	Legacy	YES	0 - 50 [°C]
IFC1210-B0	LX240T	512M	UHM	YES	0 - 50 [°C]
IFC1210-B1	LX240T	512M	Legacy	YES	0 - 50 [°C]

Table 1.4 : IFC_1210 Options & Ordering Informations

Note *For others IFC_1210 board configuration, and environmental contact directly IOxOS Technologies*

1.5.2 Environmental

The IFC_1210 is available in Commercial temperature grade (0 - 50 [°C]) and Industrial temperature grade (-25 - 55 [°C])

1.5.3 Power Requirement

To Be Completed

1.6 Environmental and Regulations

The IFC_1210 is designed to operate and fulfil following environmental conditions

- Storage Temperature -55 to 105 [°C]
- Commercial operating Temperature 0 to 55[°C] (with 200LFM forced air cooling)
- Industrial operating Temperature -25 to 55[°C] (with 400LFM forced air cooling)
- Safety regulation IEC/EN/UL60950
- EMI/RFI regulations EN50022

The IFC_1210 maximal operating temperature is also conditioned by the several parameters as FPGA type installed, the FPGA firmware, the MPF section, … To characterize the maximal operating temperature, several thermal sensors are implemented on the critical sections of the IFC_1210. (FPGA die temperature, high current DCDC, ...)

To satisfy the safety regulations, all IFC_1210 power sources incorporate short circuit protections and

over temperature protections .

- + 5[V] VME power supply → protected with MAX5970
- + 3.3[V] VME power supply → protected with MAX5970
- + 12[V] / -12[V] VME power supplies → protected with fuses
- Ericsson BMR463 internal DC-DC for 1.0[V] and 1.5[V]

1.6.1 ESD Protection EMI/RFI Filter

The IFC_1210 front panel IO connections are protected against ESD as follow

- Ethernet 10/100/1000 Base-T → embedded in the RJ45 JUMBO BELFUSE 0875-1G2T-E3 (2260 V_{DC})
- RS232 → SIPEX SP3232 with ±15kV Human Body Model
- USB 2.0 Host → External TVS diode array (D801) SEMTEC ECLAMP0504P
- microSD Holder → SEMTEC ECLAMP2357N ESD protection to IEC 61000-4-2 (ESD) Level4, ±15kV (air), ±8kV (contact)

2. IFC_1210 Hardware Description

2.1 IFC_1210 Block Diagram

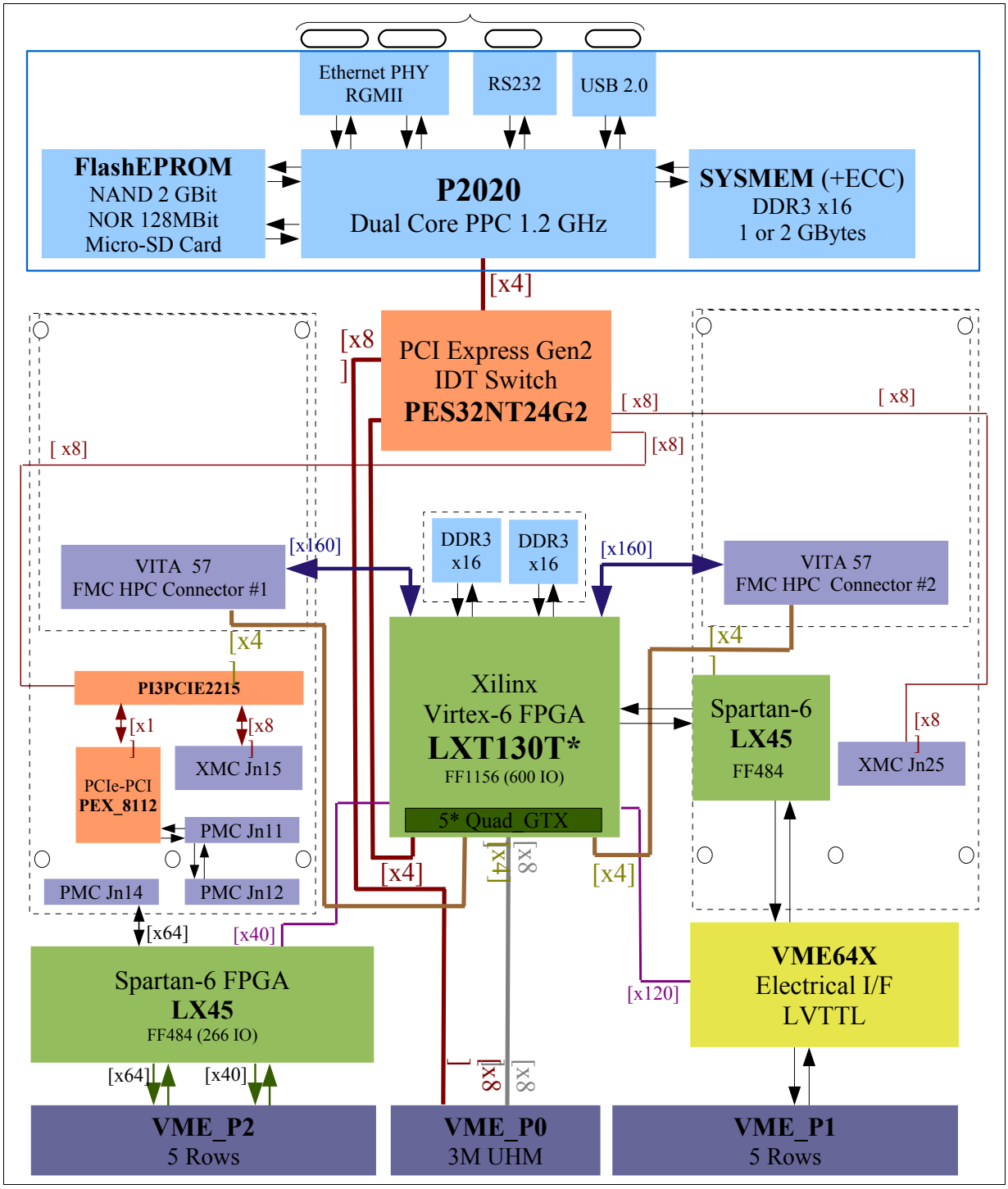

Illustration 6 : IFC_1210 Block Diagram

2.2 Mechanical Informations

The IFC_1210 is a full height 6U VME 64xboard with intermediate edge to edge connectors. It is designed to be equipped with a front-end section (named MPF) to form a full VME64x board with 160[mm] depth

- 6U VME64x board 233[mm] x 75[mm]
- 160 pins 5 rows VME P1 & P2
- 95 UHS pins P0 (High speed P0 (> 5 Gbit/s) compatible with legacy VME64x connector)
- 14 layers PCB

Note *The mechanical CAD files (AutoCAD) of the MPF front-end sections (Single width and dual width) are available under request.*

2.2.1 PMC IEEE1386.1

- IEEE1386.1 CMC/PMC (P11, P12, P14)

2.2.2 XMC VITA42.3

- IEEE1386.1 CMC
- VITA42.3-2010 XMC (P15, P25)

2.2.3 FMC VITA57.1

- VITA57.1-2008 (R2010) FMC with HPC connector (P400, P401)

2.2.4 IFC_1210 Picture

Following picture represents the top side of the IFC_1210 with key components labelled.

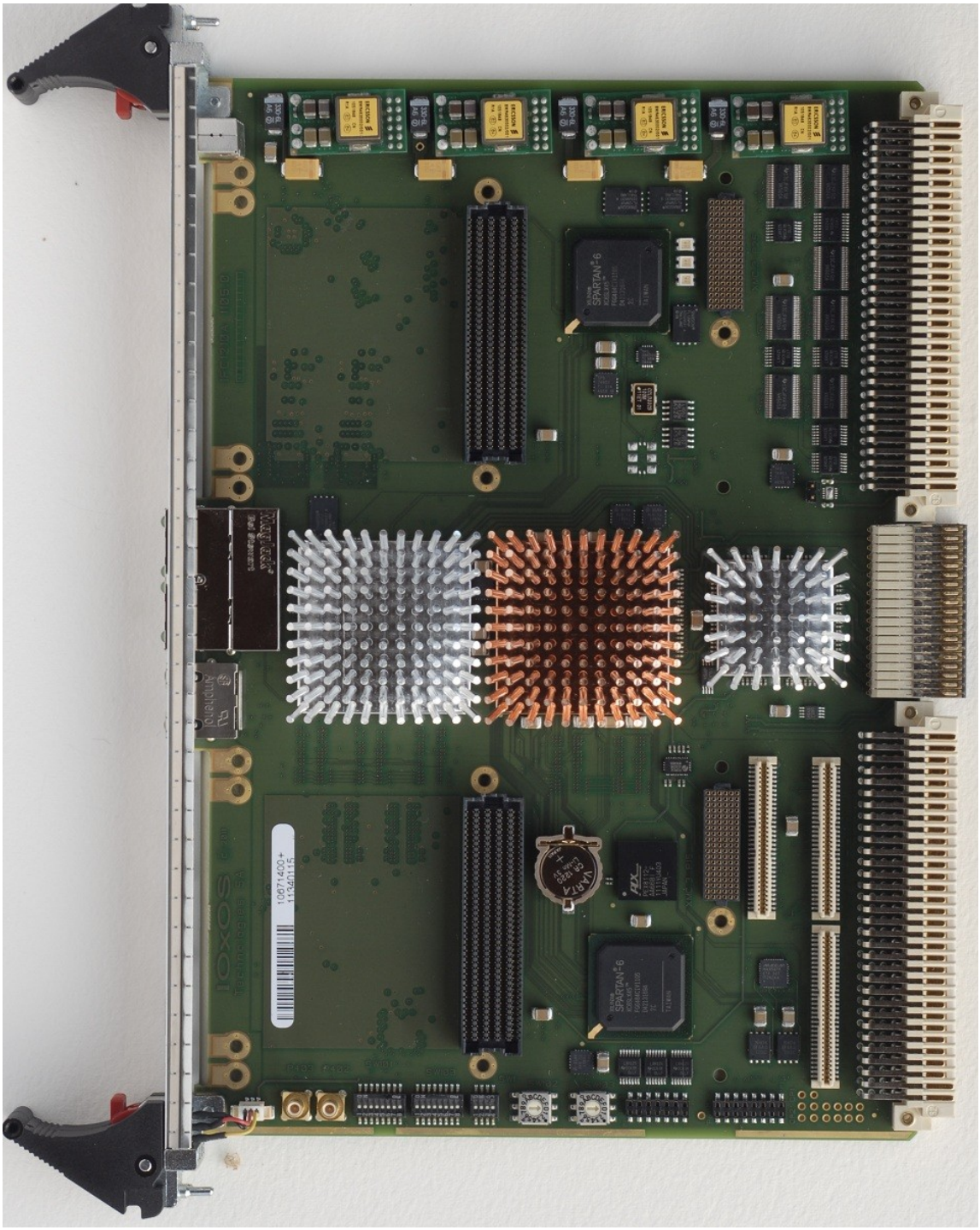

Illustration 7 : IFC_1210 Top Side Picture

2.2.5 IFC_1210 Top Side

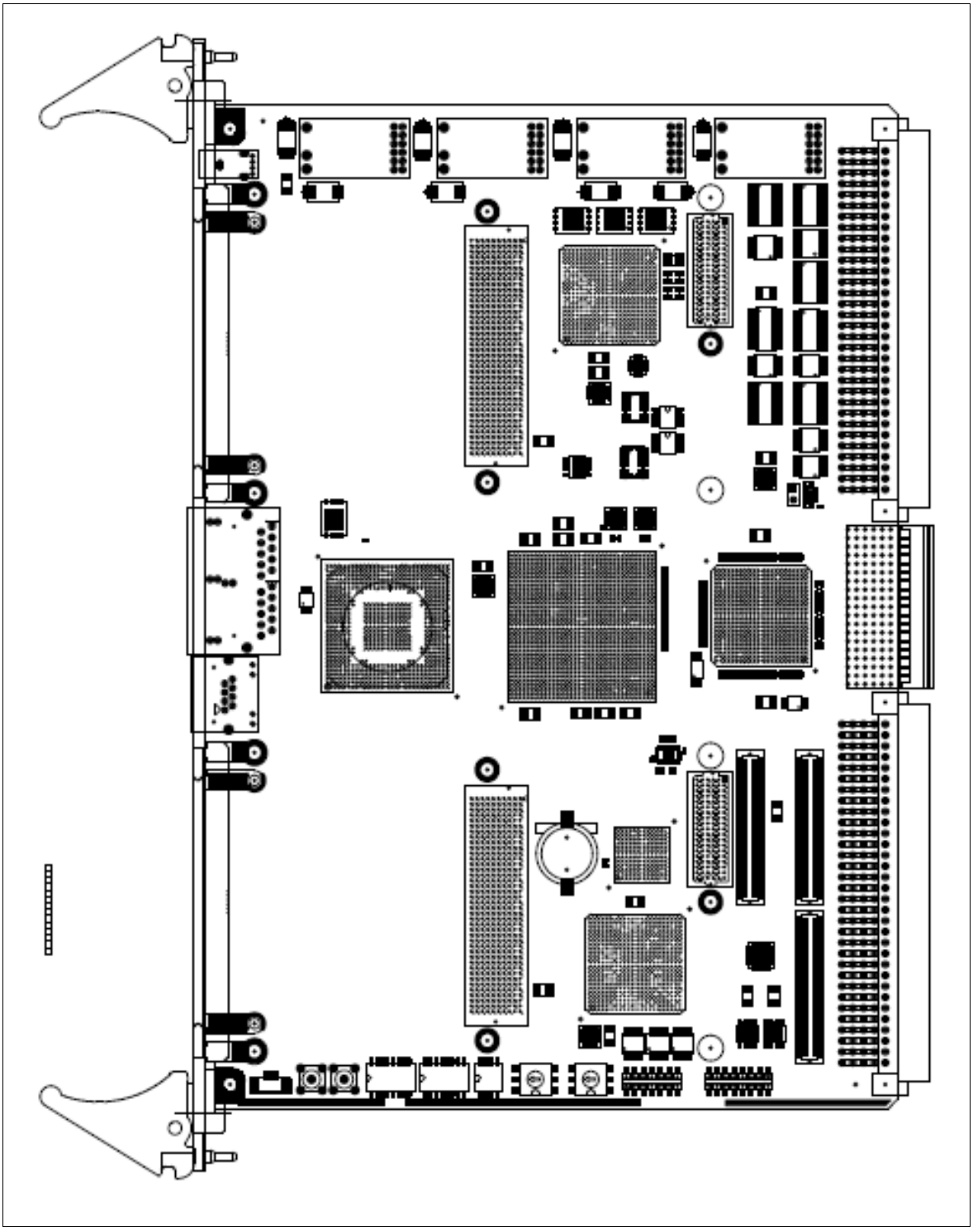

Illustration 8 : IFC_1210 Top Component Side

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2.2.6 IFC_1210 Bottom Side

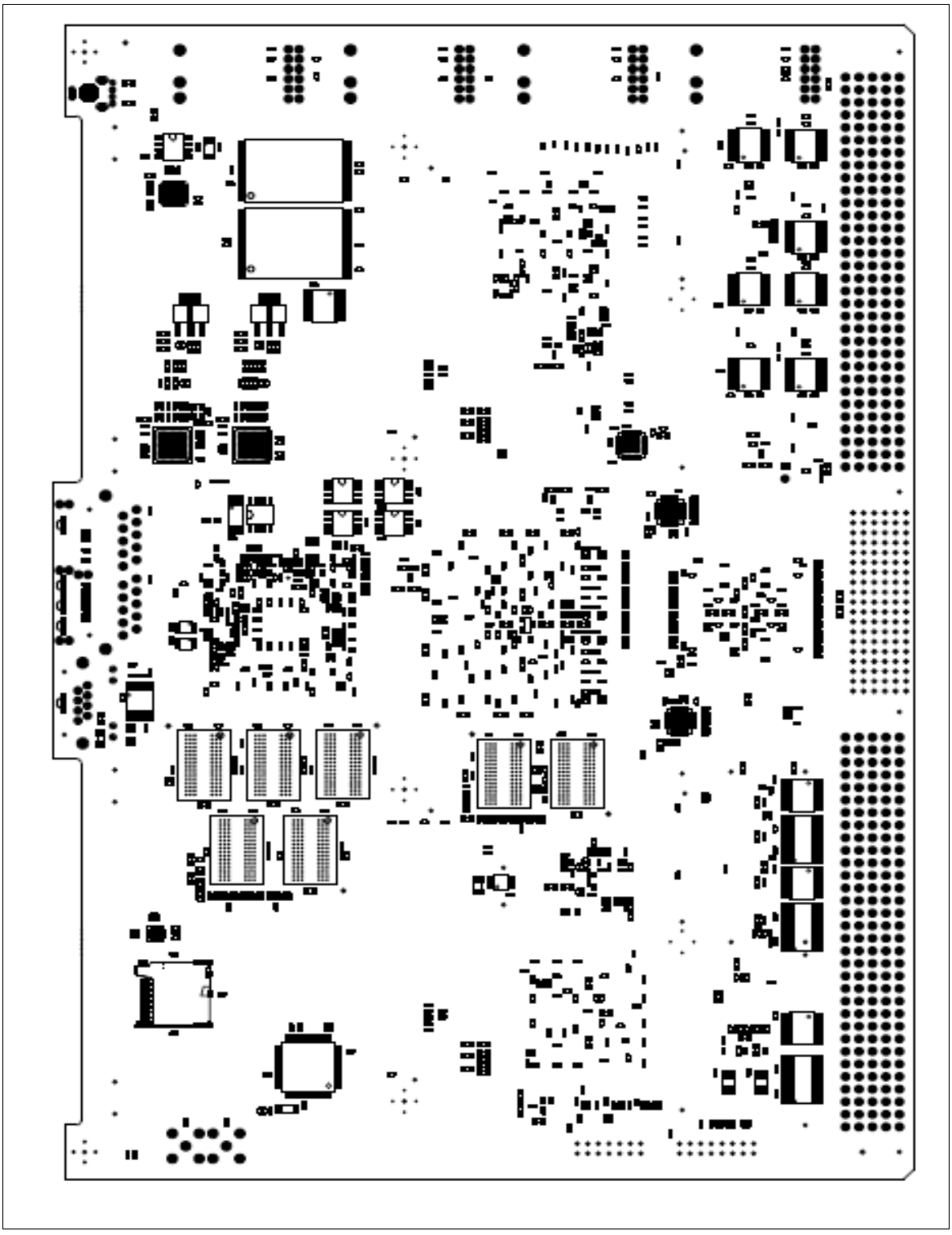

Illustration 9 : IFC_1210 Bottom Component Side

2.3 IFC_1210 STATIC Options

The IFC_1210 static options are divided into three groups :

- Two(2) 8 positions mini DIP switches (SW100, SW101)
- One(1) 4 positions mini DIP switches (SW1)
- Two (2) Hex Rotary selectors (SW102, SW103)
- Six(6) 2.54 Jumpers
- Two(2) TAP connectors

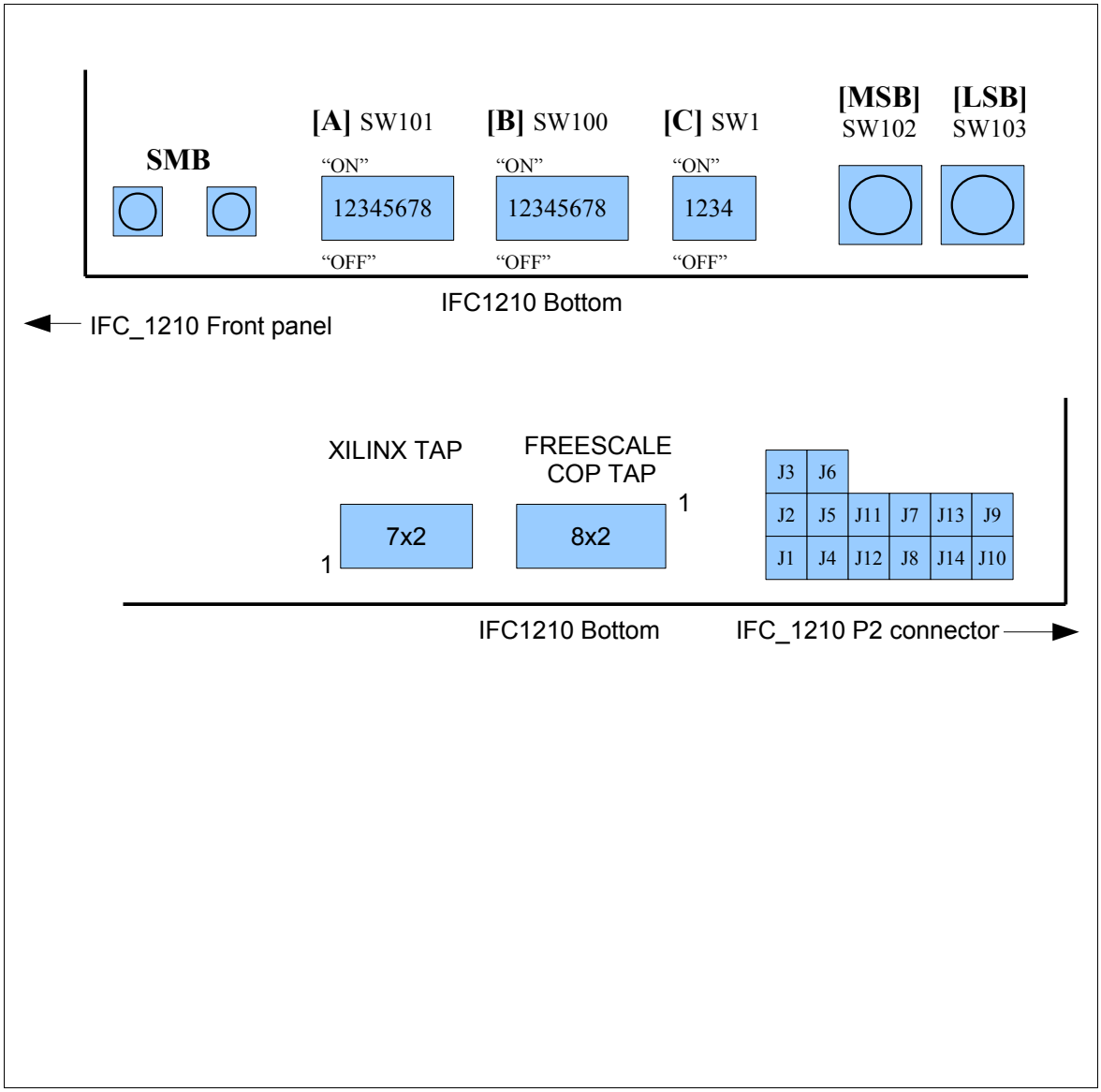

Illustration 10 : IFC_1210 Static options PCB location

All static options (DIP switches and Hex Rotary switches) are located on the bottom of the
345 IFC_1210 (PCB bottom side), with full availability while the PMC#1, XMC#1 or FMC#1 are installed.

2.3.1 Mini DIP SWITCH A (SW101)

The SW1 “SWITCH_A” provides general VME64x options

Position	Description		Comments
SW1-1 SW1-2	vme_MODE[1:0]	VME Slave Mode 00 VME64x, with CR/CSR Mapping 01 CR/CSR field mapped in a fixed A24 512 K window defined with HEX Rotary switch 10 Condensed 64K field mapped in the A24 space defined with HEX Rotary switch 11 VME64x Auto_ID	Define the way how the VME CSR area is mapped. In any case the VME Slave mapping of the IFC_1210 Memory Space is dynamically defined with adequate register.
SW1-3	vme_SLOT_1	Enable VME Slot_1 function (manual) in case of VME_Mode ≠ “00 If VME_Mode = “00”, the VME Slot_1 is enable with f(GA[5:0]) (VME64x Mode)	Refer to VME64x Specification.
SW1-4	vme_RxSYSRST	Enable VME64x SYSRESET action . While enabled on-board logic is RESET. 0 VME SYSRESET assertion only RESET the VME64x Interface 1 VME SYSRESET assertion force a IFC_1210 Cold_RESET action	
SW1-5 SW1-6	P2020 Boot Mode	P2020 Boot Selection. 00 MicroSD Memory 01 NOR Flash Memory 10 SPI Flash Memory 11 No BOOT. Keep the P2020 in RESET Mode	
SW1-7	vme_TxSYSRST	Enable VME Tx SYSRESET generation. 0 VME SYSRESET never asserted by the IFC_1210 1 VME SYSRESET asseted only while VME Slot_1	
SW1-8	Reserved	Reserved for IOxOS future upgrade	

Table 2.1 : IFC_1210 SW1 “SWITCH A” static options

2.3.2 Mini DIP SWITCH B (SW100)

The SW2 provides general PCI Express related options

Position	Description		Comments
SW2-1 SW2-2	FPGA Config[1:0]	This two static options selects the FPGA bit-stream number used by default at power-up. 00 Back-up bit-stream, 01 1st FPGA bit-stream 10 2nd FPGA bit-stream 11 3rd FPGA bit-stream	The back-up bit-stream should be updated very carefully. In case of back-up bit-stream corruption, the SPI Flash shall be reloaded with specific XILINX Tool
SW2-3	JTAG_Config	This static allows to disable the power on XILINX FPGA auto-configuration. • "ON" FPGA Configuration process through XILINX TAP connector • "OFF" FPGA Configuration process automatic at power-up	While XILINX embedded ChipScope_PRO tool is used, this static shall be positioned "ON".
SW2-4	Cold_RESET_Mode	This static selects the Cold_RESET Mode. • "OFF" Autonomous • "ON" P2020 Control	Refer to chapter X.X
SW2-5	PONFSM_Enable	This static allows to enable/disable the PON_FSM controller execution. • "ON" PON_FSM Enabled • "OFF" PON_FSM Disabled	Refer to chapter 2.21.3
SW2-6	PONFSM_Mode	This static allows to define the PON_FSM microcode offset in the SPI Flash EPROM #1. • "ON" PON_FSM independent for each FPGA bit-stream • "OFF" PON_FSM unified for all FPGA bit-streams.	Refer to chapter 2.21.3
SW2-7 SW2-8	SWITCH_Mode[1:0]	Cold RESET PES32NT24AG2 Switch Mode. This static field condition the PCI Express Switch Mode of operation. 00 Single partition 01 Single partition with reduced latency 10 Single partition with Serial EEPROM Initialization with reduced latency 11 Reserved, User defined in "PON" FPGA	Refer to chapter 2.10.4

Table 2.2 : IFC_1210 SW2 "SWITCH B" Static options

2.3.3 Mini DIP SWITCH C (SW3)

The SW2 provides general PCI Express related options

Position	Description		Comments
SW3-1 SW3-2 SW3-3 SW3-4	user_TBD[4:1]	Reserved for user customisation. Supplied to the USER Agent_SW blocks and to the "IO" FPGA.	

Table 2.3 : IFC_1210 SW3 "SWITCH C" Static options

2.3.4 HEX Rotary Encoder (SW102, SW103)

The IFC_1210 provides two Hex rotary encoder, used to define statically the VME CSR base address in the VME A24 Space. This 8-bit field (2* 4-bit) are used as :

- SW102 → VME64x Base Address A[23:20]
- SW103 → VME64x Base Address A[19:16]

If the IFC_1210 maps its CR/CSR Space with VME64x mode, the base address is determined by the VME64 GA[4:0] information supplied by the backplane. In this case the Hex Rotary information is no more used by the VME Slave controller an therefore can be refurbished for alternate usage.

2.3.5 SMB Debugging Support (P402, P403)

The IFC_1210 provides two SMB connectors (vertical mount) dedicated for FPGA user VHDL code debugging. These connectors are located inside the VME board (close to the front panel) and are not directly available on the VME front panel.

- SMB_1 → "CENTRAL" FPGA IO_Bank_24 pin "G23"
- SMB_2 → "CENTRAL" FPGA IO_Bank_24 pin "AB23"

Because these connectors are not dedicated to external connection, no ESD protection nor EMI/RFI practice are implemented. The SMB signal are directly connected to the "CENTRAL" FPGA IO_Bank 24.

Note *The SMB signalling can be configured as INPUT or OUTPUT in the "CENTRAL" FPGA.*

2.3.6 Rear_IO Power Supplies (J1 - J14)

The IFC_1210 implement a collection of 2.54 jumpers to control VME P2 specific usage of User IO. Six of these IO can be used for power supplies and therefore can not be used as generic IO controlled by the "IO" FPGA.

VME_P2	Jumpers	Selection	Comments
C31	J3,J2,J1	J3-J2 → IOC31 "IO" FPGA.	User_IO / VCC12VPOS

		J1-J2 → VCC12VPOS	
A31	J6,J5,J4	J6-J5 → IOC31 "IO" FPGA. J4-J5 → VCC12VNEG	User_IO / VCC12VNEG
C28	J8,J7	J8-J7→ VCC3V3	User_IO / VCC3V3
C30	J10,J9	J10-J9 → VCC3V3	User_IO / VCC3V3
D28	J12,J11	J12-J11 → VCC3V3	User_IO / VCC3V3
D30	J14,J13	J14-J13 → VCC3V3	User_IO / VCC3V3

Table 2.4 : 2.54 Jumpers options

2.3.7 TAP Debugging Support

The IFC_1210 provides two(2) JTAG TAP located to the bottom side of the IFC_1210.

- Xilinx TAP receptacle connector (P100) 2x7 14-pin 2[mm] dedicated to XILINX ChipScope PRO and iMPACT.
- P2020 COPS receptacle connector (P800) 2x8 16-pin 2[mm] dedicated to FREESCALE CodeWARRIOR.

The P2020 COPS interface requires an external adaptor to fit default connector CodeWARRIOR connector. (16-pin 2.54[mm])

2.4 IFC_1210 Visual Indicators

The IFC_1210 incorporates eight(8) gewneral purpose Bi-colour LED indicators. Additionnaly the front panel RJ45 connectors (Ethernet + RS232) also provide two LED indicator with each connector.

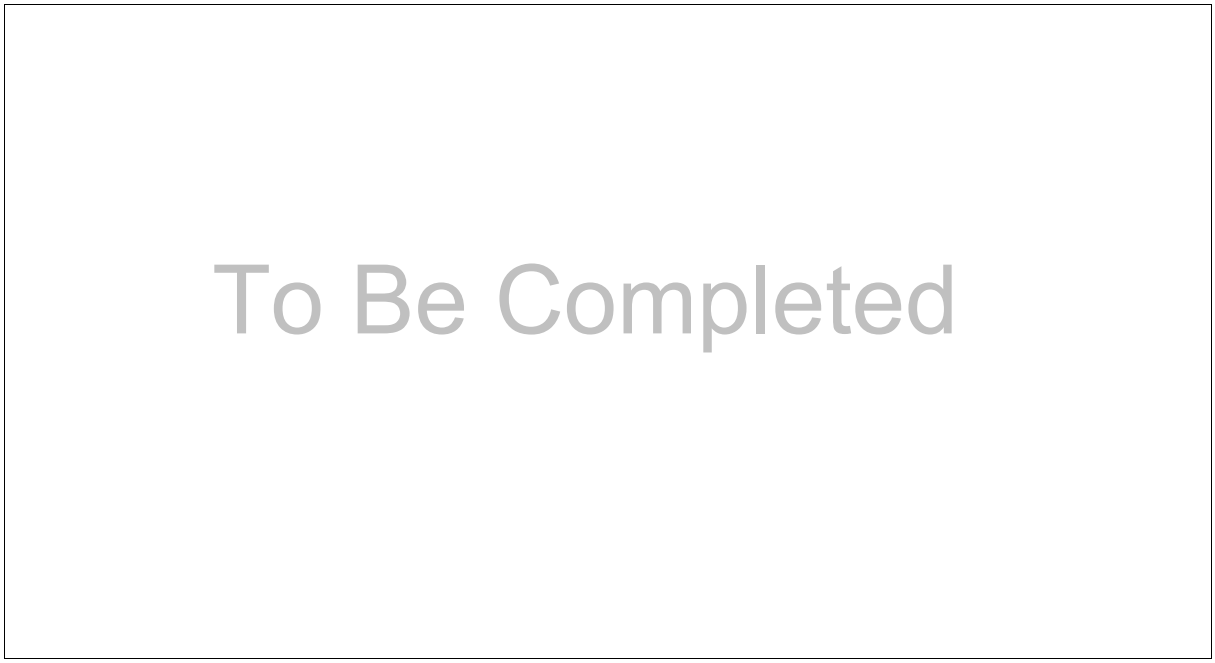

Illustration 11 : IFC_1210 Visual Indicators location.

2.4.1 On-board LED Indicators

Three(3) Bi-colour LEDs are implemented directly on the IFC_1210 PCB top side, providing general status informations. These LED indicators are not visible from the VME front panel.

LED#	Color	Information	Comments
LED_103	Green	“PON” FPGA controlled TBD	To Be defined
	Amber	“PON” FPGA controlled TBD	To Be defined
	Red	“PON” FPGA controlled TBD	To Be defined
LED_104	Green	“IO” & “CENTRAL” FPGA configured OK	OK Configured with selected bit-stream number (#0, #1, #2 or #3)
	Amber	“IO” & “CENTRAL” FPGA configured with back-up bit-streams	WARNING, the configured with back-up stream #0
	Red	“IO” & “CENTRAL” FPGA configuration FAIL	ERROR, FPGA are not configured
LED_105	Green	“PON” FPGA Configured	Light-on while the Spartan-6 “PON” FPGA is auto-configured at power-up from the dedicated SPI Flash EPROM.

Table 2.5 : IFC_1210 Top PCB side LED Indicators

2.4.2 Front Panel LED Indicators

Five(5) Bi-colour LEDs are implemented on the VME front panel directly attached to the “PON” FPGA Spartan-6 and the “CENTRAL” FPGA Virtex-6.

LED#	Color	Information	Comments
LED_401 “FMC1”	Green	“CENTRAL” FPGA controlled	“CENTRAL” FPGA FMC_1 User function defined.
	Amber	“CENTRAL” FPGA controlled	
	Red	“CENTRAL” FPGA controlled	
LED_102 “VME”	Green	TOSCA II VME Slave access	Stretched 0.3 [s]
	Amber	TOSCA II VME Master access	Stretched 0.3 [s]
	Red	TOSCA II VME Error detected (BERR)	Stretched 0.3 [s]
LED_101 “S1”	Green	TOSCA II VME Slot_1 Enable	IFC_1210 incorporates a complete VME Slot_1 function.
	Red	MAX5970 LI controller FAULT	When light on, a power supply major failure occurred. Refer to MAXIM Semiconductors MAX5970 data-sheet
LED_400 “CENTRAL”	Green	“CENTRAL” FPGA OK	“CENTRAL” FPGA Operation status
	Amber	“CENTRAL” FPGA TBD	
	Red	“CENTRAL” FPGA ERROR	
LED_402 “FMC2”	Green	“CENTRAL” FPGA controlled	“CENTRAL” FPGA FMC_2 User function defined.
	Amber	“CENTRAL” FPGA controlled	
	Red	“CENTRAL” FPGA controlled	

Table 2.6 : IFC_1210 Front Panel LED Indicators

2.4.3 Front Panel RS232 RJ45 LED Indicators

The RJ45 dedicated to the RS232 interface integrates two LED indicators (Green and Yellow).

These two LED are controlled by the "PON" FPGA as follow :

LED#		Information	Comments
GREEN	OFF	Power OFF	Provides RESET FSM status informations. Allow to track P2020 + FPGA Configuration process.
	Pulsed	Cold_RESET active	
	Toggle FAST	PCIe SWITCH Configured	
	Toggle SLOW	P2020 Running	
	ON	READY, In Operation	
YELLOW	OFF	To Be Defined	
	Pulsed	To Be Defined	
	Toggle FAST	To Be Defined	
	Toggle SLOW	To Be Defined	
	ON	To Be Defined	

Table 2.7 : IFC_1210 Front Panel RJ45 LED Indicators

405 ***Note*** *Refer to the HDL source code in "ifc1210_PON_A0.vhd"*

2.4.4 Front Panel 10/100/1000BaseT LED Indicators

The two(2) Ethernet RJ45 COMBO incorporate two(2) LED providing operation status on the Ethernet 10/100/1000 Base-T port. (Tx / Rx / Linked)

410

These four LED indicators are directly controlled by the Ethernet PHY KSZ9021RN (U826, U828)

2.5 Thermal Monitoring

The IFC_1210 integrates two (2) LM95235, on-board temperature monitoring, connected to a
415 dedicated I2C Bus.

- LM95235 #1 (U700) is located in the middle of the front section.
- LM95235 #2 (U701) is located in the middle of the rear section.

The 1st one is also connected to the temperature sensing diode (DXP:Anode – DXN:Cathode) of the FREESCALE P2020 die temperature.

420 The XILINX Virtex-6T “CENTRAL” FPGA System Monitor is able to monitor its die temperature.

The two LM95235 (U700, U701) are able to issue an interrupt “TCRITn” on software programmable conditions. This can be used for automatic action in case of over temperature detection.

2.6 Power Supplies

The IFC_1210 implements a specific cicuitry on the incoming VME64x power supplies. This circuitry allows to monitor dynamically (voltage and current level) the VME power supplies and protect the IFC_1210 against short circuit and current surge.

This circuitry is implemented with a "Dual Hot-Swap Controller" MAX5970 (U702), isolating the high capability VME 3.3[V] and 5.0[V].

The IFC_1210 motherboard does not use the +/- 12[V] power supplies. These two high voltage power supplies are fed from the VME backplane to the FMC/XMC and PMC sites through :

- -12[V] SMD 0805 1[A] fuse (F701)
- +12[V] NIS5132(U715) Electronic Fuse

The IFC_1210 follows the VITA 1.7 specification, supporting up to 1.25[A] per power supply pin on VME P1 and P2 connectors. (Up to 11.25[A] on 5.0[V] and up to 11.25[A] on 3.3[V]

The "high-current" local power supplies are implemented with latest generation Ericsson BMR 463. These DCDC can be synchronized together allowing to support phasing control reducing the noise generated by the DCDC switchers.

The control register ELB_BMRCTL allows to set-up the SYNC frequency (320 -> 640[KHz]) or inactive.

The "low-current" local power supplies are implemented with LDO TI TPS74901.

The following table sums up the IFC_1210 power supplies infrastructure.

Power	V	Imax	V_{SRC}	Load	
IVCC_5V0	5.0[V]	11.2[A]	VME64x	PMC, XMC, FMC BMR 463 DCDC	VME64x 5.0[V] backplane isolated with MAX5970 (U702)
IVCC_3V3	3.3[V]	11.2[A]	VME64x	VME Transceiver PMC, XMC, FMC Spartan-6 "IO"	VME64x 3.3[V] backplane isolated with MAX5970 (U702)
IVCC_12POS	12.0[V]	1[A]	VME64x	PMC, XMC, FMC	SMD 0805 Fuse protection 1[A] (F701)
IVCC_12NEG	-12.0[V]	1[A]	VME64x	PMC, XMC	Electronic Fuse protection NIS5132 (U715)
VCC_1V0	1.05[V]	20[A] (40[A])	IVCC_5V0	Virtex-6T "CENTRAL" P2020, PES32NT8AG2	Single / (optionnaly dual) BMR 463 (U704, U705). Can be mounted in // for 40[A] support.
VCC_1V5	1.5[V]	20[A]	IVCC_5V0	DDR3, VCC_IO, LDO,	Single BMR 463 (U706).
FMC_VADJ	2.5[V] - 1.5[V]	20[A]	IVCC_5V0	Both FMC VADJ Virtex-6T "CENTRAL" Spartan-6 "PON" Spartan-6 "IO"	Single BMR 463 (U707). The two FMC slots VADJ power supplies are isolated through a controllable CMOS switch SiR404 (Q702).
VCC_2V6A	2.6[V]	3[A]	IVCC_3V3	Virtex-6T "CENTRAL" Spartan-6 "PON" Spartan-6 "IO" PES32NT8AG2	TPS74901 (U709) General purpose 2.6[V]
VCC_2V5B	2.5[V]	3[A]	IVCC_3V3	P2020 + Companion	TPS74901 (U710) General purpose 2.6[V]
VCC_1V2A	1.2[V]	3[A]	VCC_1V5	Spartan-6 "PON"	TPS74901 (U711) Top section 1.2[V]

VCC_1V2B	1.2[V]	3[A]	VCC_1V5	Spartan-6 “IO“	TPS74901 (U712) Bottom section 1.2[V]
VCC_1V2C	1.2[V]	3[A]	VCC_1V5	Virtex-6T GTX	TPS74901 (U714) dedicated to GTX (TPS74401 low noise version optional)
VCC_1V0C	1.05V]	3[A]	VCC_1V5	Virtex-6T GTX	TPS74901 (U713) dedicated to GTX (TPS74401 low noise version optional)

Table 2.8 : IFC_1210 Power Supplies Infrastructure

445 Following table provides the IFC_1210 power consumption estimation.

	IVCC_5V0	IVCC_3V3	VCC_1V0	VCC_1V5	FMC_VADJ	Notes
P2020 DDR System Memory				2.00		
P2020		0.3 (Note_2)	5.00	0.60		
P2020 IO Resources NAND NOR microSD		0.10				
Ethernet 1000BaseT		0.10		1.0 (Note_1)		
USB 2.0 Host						
PES32NT32AG2		0.20 (Note_2)	4.50			
CENTRAL FPGA DDR3				0.40		
CENTRAL FPGA Virtex-6 VCC_Core + VCC_IO		0.60 (Note_2)	8.00	0.40	1.00	Estimation
CENTRAL FPGA Virtex-6 VCC_MGT				2.00 (Note_1)		
IO FPGA		0.4		1.0 (Note_1)	0.25	
PON FPGA		0.3		1.0 (Note_1)	0.25	
PCI Bridge PEX8112	0.01	0.02		0.20 (Note_1)		
VME Interface	0.01	0.40				
Clock Infrastructure		0.50 (Note_2)				
Others (Marginal)	0.05	0.10				
Budget Current/Power MAX	~0.06[A] ~0.3[W]	~2.90[A] ~9.5[W]	~17.50[A] ~17.50[W]	~9.60[A] ~14.40[W]	~1.50[A] ~3.70[W]	
Estimated typical PW (66%)	~0.2[W]	~6.2[W]	~12.50[W]	~10.00[W]	~2.50[W]	Σ = ~31W]
Reported to VCCI	~25.0[W]	~6.2[W]				
Note_1 *LDO TPS74901 connected to VCC_1V5* ***Note_2*** *LDO TPS74901 connected to VCC_3V3*						

Table 2.9 : IFC_1210 Power Budget

Note *The IFC_1210 carrier board estimated power ~30[W]*

Note *Estimation for XMC/FMC/FMC Mezzanine card ~20[W]*

2.6.1 System Power Management MAX5970

The IFC_1210 is equipped with one MAX5970 (U702) integrated power controller device monitoring continuous the VME power supplies 3.3[V] and 5.0[V].

The MAX5970 (U702) incorporates a I2C remote control interface allowing to monitor all key parameters related to the on-board power supplies (V_{CC} Max/Min I_{CC} Max/Min for both VME power inputs. To support the measurements the MAX5970 integrates a 10-bit ADC .

This device provides following IFC_1210 power management facilities :

- Electronic Circuit Breaker with programmable over-current
- Power supplies dV/dt control
- Under-voltage lockout (UVLO)
- Power-Good PG and Power-Fault signalling
- Complete remote monitoring

2.6.2 Power_ON Controller TPS38600

The key internal power supplies are monitored by a dedicated quad-voltage supervisory circuitry TI TPS38600 (U703). This devices monitors the following IFC_1210 power supplies as :

- VME +5[V] input power supply
- VME +3.3[V] input power supply
- 1.5[V], supplying the low voltage LDO TPS74901 and majority of IO interconnection. (HSTL)
- 1.0[V], supplying the Virtex-6 FPGA core, the P2020 and the PES32NT8AG2 / PES32NT24AG2

The Power-up RESET Management is controlled through manual RESET input or Static Enabled VME SYSRESET# assertion.

The TI TPS38600 (U703) controls directly the configuration process of the “PON” FPGA Spartan-6 . The TPS38600 (U703) RESET is directly assigned to the “cfg_PROGRAMn” signal.

Until all power supplies are OK, or in case of a power supplies failure, the PON_RESET signal is asserted.

The TI TPS38600 (U703) also integrates a watch-dog timer function. This watch-dog is clear periodically by the FSM located in the “PON” FPGA while the complete IFC_1210 system is alive.

2.6.3 High Current DCDC BMR 463

The IFC_1210 is equipped with latest generation high efficiency DCDC converter ERICSSON BMR463, able to supply up to 20[A]. This new DCDC generation provides key features as :

- High efficiency, typ. 97.1%
- Configuration and Monitoring via PMBus
- Synchronization & Phase spreading
- Current sharing, Voltage Tracking & Voltage margining
- Input under voltage shut-down

- Over temperature protection
- Output short-circuit & Output over voltage protection
- MTBF >20 Mh

These new generation of DCDC provide very high efficiency and integrate a I2C Interface (PMBus) allowing to monitor and control them remotely. Through the PMBus, it is also possible to adjust the Voltate Output level (+ 10% / - 100%).

The three(3) (optionnaly four(4)) BMR463 (U704, U705, U706, U707) can be synchronized together with programmable de-phasing. The phase set-up can be tuned under SW control for optimal noise distribution.

The SYNC pins of the three(3) (optionnaly four(4)) BMR463 (U704, U705, U706, U707) are connected together and can be also controller by the „PON“ FPGA. The control register ELB_BMRCTL allows to set-up the SYNC frequency (320 -> 640[KHz]) or inactive.

Thanks to new current sharing capability, two BMR 463 (U704, U705) can be wired in // with dynamic current balancing.

The BMR463 DCDC are used to built locally following IFC_1210 internal power supplies :

- 1.0[V], supplying the XILINX Virtex-6 FPGA (U400), IDT PES32NT8AG2 / PES32NT24AG2 (u200) PCI Express Switch and the PowerPC processor P2020 (U800).
- 1.5[V], supplying the DDR3, IO_Bank for HSTL and low voltage LDO
- 1.5[V] – 2.5[V], supplying the FMC VADJ ans specific FPGA IO_bank (See next chapter)

The three(3) (optionnaly four(4)) BMR 463 can be synchronized together with programmable de-phasing. The phase set-up can be tuned under SW control for optimal noise distribution. The synchronization signal can also be driven by to the “PON“ FPGA.

The three(3) (optionnaly four(4)) BMR 463 suppliing the 1.0[V] and 1.5[V] are enabled immediatly at power-up with Power_GOOD information issued by the LI controller MAX5970.

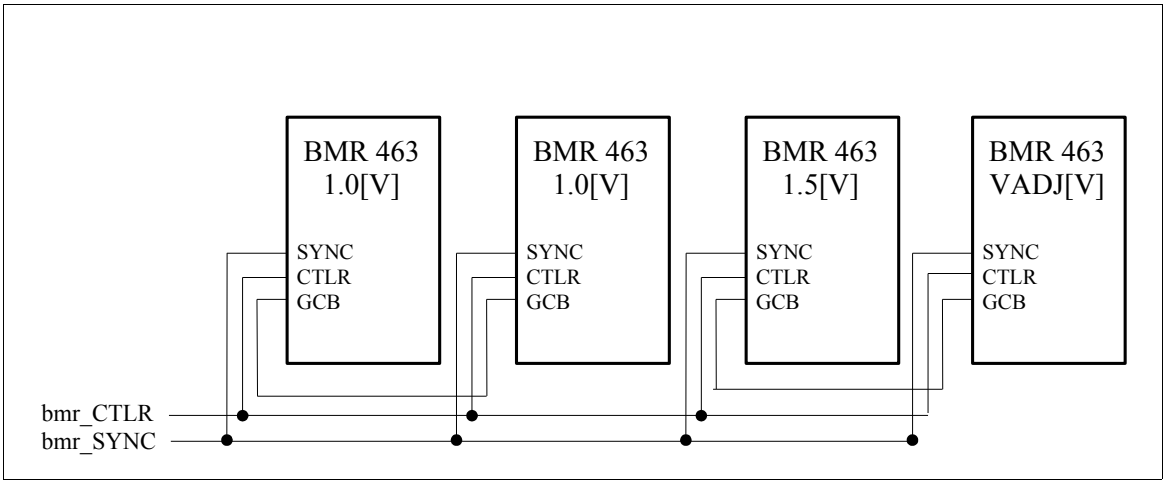

Illustration 12 : IFC_1210 BMR 463 DCDC Implementation

2.6.4 DCDC FMC VADJ Power Supply

The FMC VITA57.1-R2010 VADJ is selectable from1.5[V] up to 2.5[V]. The VADJ voltage level is conditioned by the FMC mezzanine installed on the sites. The BMR 463 (U707) dedicated to VADJ is conditioned by start-up R_{SET} value fixed to 2.5[V].

The three on-board FPFA “CENTRAL, “IO” and “PON” own a IO_Bank powered with this power supply VADJ. After power-up. With VADJ set-up to 2.5[V], the P2020 can, under software control, modify this value from 1.5[V] to 2.5[V].

The VADJ connected to the FMC sites is isolated with a N-Channel MOSFET transistor (Q702) (VISHAY SiR404DP) The gate of this transistor is controlled by the “PON” FPGA allowing to enable/disable under software control the FPC VADJ power.

The VADJ level requirement shall be available in the FMC Mezzanine EEPROM interfaced to the SMBus. (Refer to VITA57.1-R2010 specification Rule 5.98)

The IFC_1210 shall implement a dedicated software routine, (P2020) implementing following sequence. This software routine shall be executed before the FMC communication is activated.

1. I2C Read FMC#2 mezzanine EEPROM to extract the VADJ requirement
2. I2C Read FMC#1 mezzanine EEPROM to extract the VADJ requirement
3. Consolidate VADJ requirements for both FMC.
4. Determine VADJ maximum level (if inconsistent set to lowest voltage level)
5. Initialize the BMR463 VADJ with adequate value through its PMBus
6. Enable the FMC VADJ power supply by controlling the SiR404DP gate

After sequence initialization, the FMC VADJ power supplies is active, with voltage level set-up in accordance with intalled FMC.

During the above descibed process, the VADJ voltage can be changed from initial power-up value set at 2.5[V] to lower value down to 1.5[V]. The VADJ voltage modification should be executed smoothly without disturbing the communication between the “CENTRAL“ FPGA and the “PON“ FPGA.

Note *In case od unexpected behaviour while the VADJ is modified, the communication between the “CENTRAL“ FPGA and the “PON“ FPGA can be temporary suspended for the required time.*

Note *The FMC VADJ power supply is monitored by the Virtex-6 “CENTRAL“ FPGA System Monitor block, providing real-time voltage value measurement.*

2.6.5 High/Low Current LDO TPS74901

Six(6) TI TPS74901 LDO devices are used for generation of on-board low voltage power supplies (2.5[V], 1.2[V] and 1.0[V]) The TPS74901 is able to provide low output voltage with a minimal drop out (< 120[mV])

- TI TPS74901 (U709) 2.6[V] / 3.0[A] VME64x internal + general purpose
- TI TPS74901 (U710) 2.5[V] / 3.0[A] general purpose
- TI TPS74901 (U711) 1.2[V] / 3.0[A] for the “PON“ FPGA Spartan-6 XC6SL45

- TI TPS74901 (U712) 1.2[V] / 3.0 A] for the “IO“ FPGA Spartan-6 XC6SL45
- TI TPS74901 (U713) 1.2[V] / 1.5[A] for the MGTAVTT and MGTAVTTRCAL (GTX transceivers)
- TI TPS74901 (U714) 1.05[V] / 1.2[A] for the MGTAVCC (GTX transceivers)

The twenty(20) available GTX transceivers are all powered from two (low noise) TPS74901 LDO regulators. From this voltage sources, the north and south sections are connected together and powered through ferrite/inductor filter. Suggested PCB implementation with the capacitor decoupling requirements is described in XILINX “Virtex-6 UG364”, Board Design Guideline.

Note *TI TPS74401 (1% accuracy, 16[uV$_{RMS}$) → TI TPS74901 (2% accuracy, 25[uV$_{RMS}$)*

2.7 Clock Distribution

The IFC_1210 implements two primary low jitter clock reference

- Fixed 100MHz +/- 50 ppm low jitter oscillator LVDS (U110)
- SW Programmable oscillator IDT8N4Q001 LVDS (U108)

These two clock references are than distributed over the IFC_1210 resources through differential low jitter clock drivers (TI CDCLVD2104 repeater without PLL/DLL logic). Following drawing represents the IFC_1210 clock distribution schema.

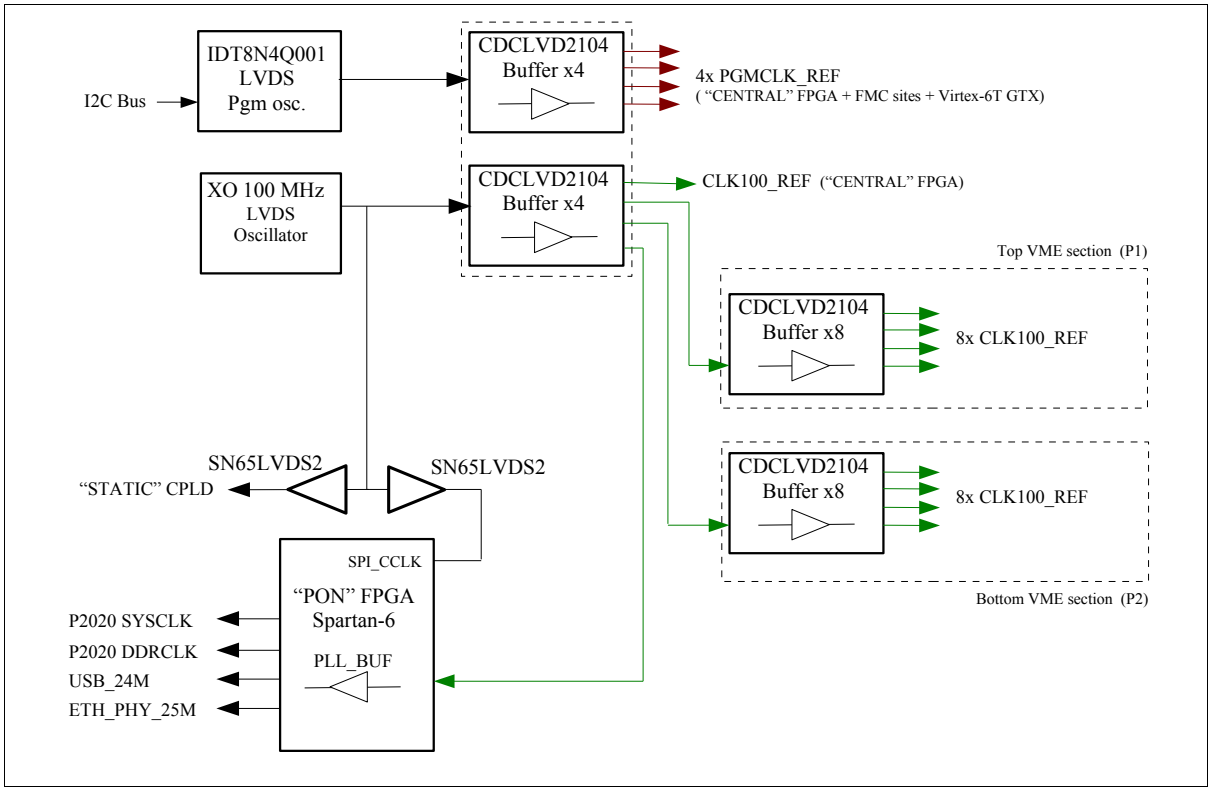

Illustration 13 : IFC_1210 Clock Distribution

The 100 MHz clock distribution is implemented in LVDS with a two stage clock buffer. The 1st stage uses a ½ CDCLDV2104 (U107) and the 2nd stage two CDCLDV2104 (U109, U112). The final clock segment is AC coupled (only while required) terminated with a 100 ohms resistors.

Two LVDS → LVTTL translators SN65LVDS2 (U111, U113) are used to feed the “PON” FPGA

Spartan-6 CCLK and the “STATIC” CPLD global clock. The “PON” FPGA Spartan-6 CCLK running at 100 MHz speed-up Cold_RESET SPI configuration process and guarantee a deterministic configuration wake-up

The PGMCLK, sourced by the IDT8N4Q001 (U108), is distributed with a ½ CDCLDV2104(U107) It is also AC coupled and terminated with a 100 ohms resistors.

The following tables sum up the IFC_1210 clock distribution.

Destination	Load	Destination	Source	AC	Comments
“CENTRAL” FPGA Virtex-6T	3	GC IO_Bank_34 MGT_GTX_113 MGT_GTX_114	CDCLDV2104$_{1B}$ CDCLDV2104$_{2}$ CDCLDV2104$_{2}$	N Y Y	***Note*** Adjacent MGT group can share the CLKREF0 CLKREF1
“IO” FPGA Spartan-6	1	GC IO_Bank_XX	CDCLDV2104$_{3}$	N	
“PON” FPGA Spartan-6	1	GC IO_Bank_XX	CDCLDV2104$_{1A}$	N	
“PON” FPGA Spartan-6	1	_CCLK	SN65LVDS2	N	LVTTL (SPI Configuration Mode)
“STATIC” CPLD CoolRunner II	1	GCK_0	SN65LVDS2	N	LVTTL global clock
XMC Site #1	1	DP18	CDCLDV2104$_{23}$	N	***Note*** *High impedance if XMC not present*
XMC Site #2	1	DP18	CDCLDV2104$_{2}$	N	***Note*** *High impedance if XMC not present*
FMC Site #1	1	CLK3_BIDIR	CDCLDV2104$_{3}$	N	***Note*** *Isolated with high-impedance LVDS repeater DS90LV001 controlled with FMC CLK_DIR signal*
FMC Site #2	1	CLK3_BIDIR	CDCLDV2104$_{2}$	N	
PES32NT8AG2 / PES32NT24AG2	2	GCLK0, GCLK1	CDCLDV2104$_{3}$	Y	
PEX8112	1	PCLK	CDCLDV2104$_{3}$	Y	
UHM P0	4	UHM_PCLK_0 UHM_PCLK_1 UHM_PCLK_2 UHM_PCLK_3	CDCLDV2104$_{2}$ CDCLDV2104$_{2}$ CDCLDV2104$_{3}$ CDCLDV2104$_{3}$	Y Y Y Y	PCI Express Extension Tx_CLK ***Note*** *High impedance control from “PON” FPGA*
P2020 SERDES	1	P2020	CDCLDV2104$_{2}$	Y	Independent clock reference for PCIe
P2020 SYSCLK	1		“PON” FPGA	N	PLL based generation 100 MHz
P2020 DDRCLK	1		“PON” FPGA	N	PLL based generation 66/100 MHz
USB 24 MHz	1		“PON” FPGA	N	PLL based generation 24 MHz Provision for local crystal 24 MHz
ETH PHY 25 MHz	2		“PON” FPGA	N	PLL based generation 25 MHz Provision for local crystal 25 MHz

Table 2.10 : IFC_1210 100 MHz + derived Clock Distribution

Destination	Load	Destination	Source	AC	Comments
“CENTRAL” FPGA Virtex-6T	3	GC IO_Bank_34 MGT_GTX_112 MGT_GTX_115	CDCLDV2104$_{1A}$ CDCLDV2104$_{1A}$ CDCLDV2104$_{1A}$	N Y Y	***Note*** *Adjacent MGT group can share the CLKREF0 CLKREF1*

FMC Site #1	1/2	CLK2_BIDIR	CDCLDV2104$_{1A}$ + DS90LV001	N	***Note*** *Isolated with high-impedance LVDS repeater DS90LV001*
FMC Site #2	1/2	CLK2_BIDIR	CDCLDV2104$_{1A}$ + DS90LV001	N	

Table 2.11 : IFC_1210 IDT8N4Q001 PGM Clock Distribution

The others on-board IFC_1210 synchronous resources are controlled as :

- P2020 SYSCLK is driven by the the “PON” FPGA and derived from the CLK_100REF. (1:1)
- Ethernet PHY clock 25 MHz (MICREL KSZ9021RN) are supplied by the “PON” FPGA and derived from the CLK_100REF. (1:4)
- USB PHY clock 24 MHz (SMSC USB3300) is supplied by the “PON” FPGA and derived from the CLK_100REF
- System Memory DDR3 clocks are driven directly by the P2020
- PCI (PMC) clock 33 MHz is supplied by the PEX_8112 or alternatively by the “PON” FPGA derived from the CLK_100REF
- VME SYSCLK is supplied by the “PON” FPGA and derived from the CLK_100REF

2.7.1.1 FMC VITA57-1 Clocking

Refer to chapter 2.16.4

2.7.1.2 VME64x P0 Clocking

Refer to chapter 2.2.6

2.7.1.3 Virtex-6T GTX Clocking

Refer to chapter 2.11.4

2.7.2 Programmable XO (VCXO) IDT8N4QV01

To support flexible clocking support, the programmable XO IDT8N4Q001 (U108) is implemented to provide :

- A modular frequency generator
- Programmable spread spectrum (+/- 600 ppm)

The IDT8N4Q001 (U108) device is a programmable VCXO oscillator exhibiting very low RMS jitter (< 0.5 [ps]) and excellent phase noise performance (< 0.3 [ps]). Beside the four default power-up frequencies, the IDT8N4Q001 (U108) can be programmed via a I2C Bus interface from 15.476 [KHz] to 866.67[MHz] and from 975[MHz] to 1'300[MHz] with frequency step of 436 Hz.

The IDT8N4Q001 (U108) is attached to the “PON” FPGA Spartan-6 for I2C interfacing (LVTTL) and issue a clock reference in LVDS.. IDT8N4Q001 keys features are :

- Clock generation programmable from 15.476 [KHz] to 866.67[MHz] and from 975[MHz] to 1'300[MHz]

- Frequency programming resolution is 436 [Hz]
- I2C Interface for clock frequency, APR and PLL control registers
- APR programmable from +/- 2.5[ppm] and +/- 727.5[ppm]
- RMS phase jitter @ 155.52MHz, (12kHz - 20MHz): 0.5ps (typical)

The IDT8N4Q001 (U108) static operation mode is selectable through the register. Refer to IDT8N4Q001 data sheet

2.8 Power_UP/Cold_RESET Sequence

The IFC_1210 supports two basic Cold_RESET options, selected with the static switch SW2-4 "Cold_RESET_Mode"

- Mode_0 : Autonomous
- Move_1 : P2020 control

While configured in Mode_0, the on-board hardware FSM (located in the "PON" FPGA) configures completely the IFC_1210 before releasing the on-board RESET signals. In Mode_1, the final on-board hardware configuration is deported to the P2020 microprocessor and than shall be integrated in its bootstrap software.

Following diagram shows the IFC_1210 Cold RESET sequence :

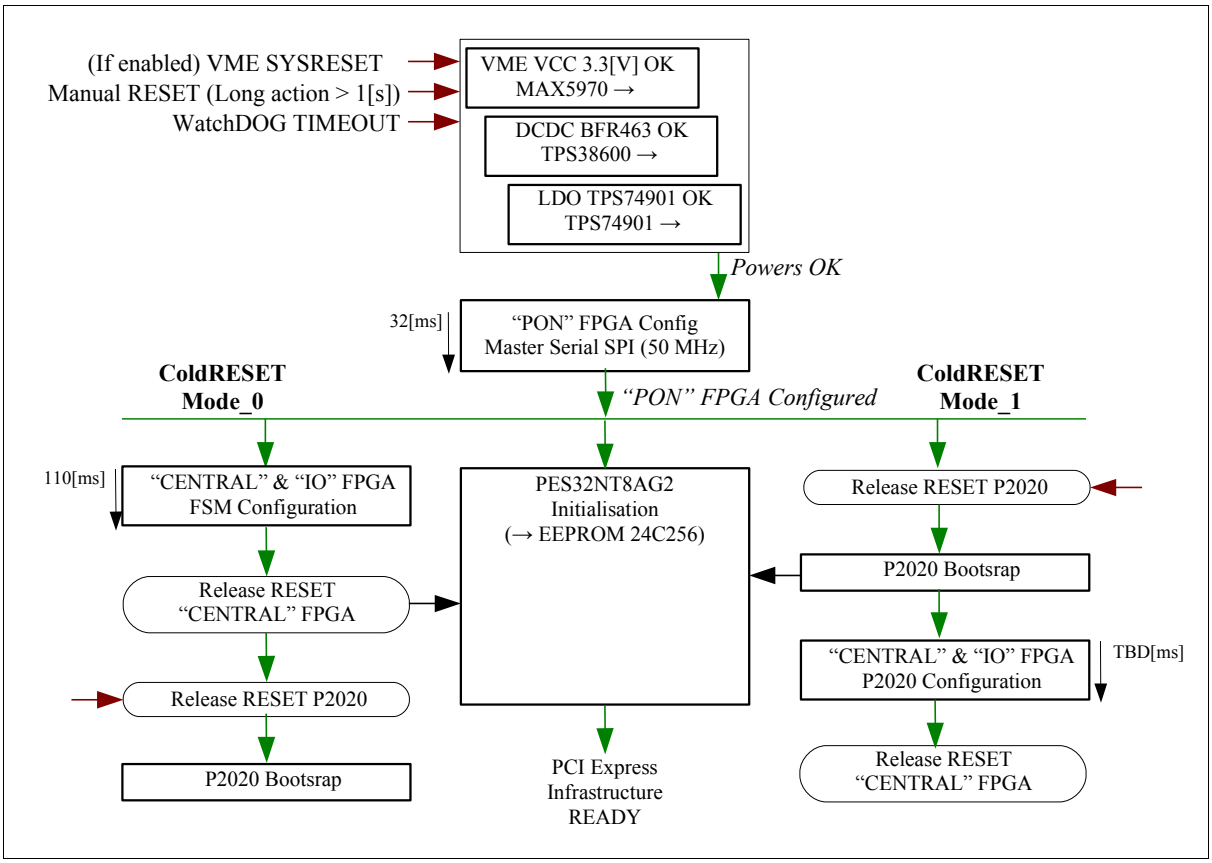

Illustration 14 : IFC_1210 Power_UP/Cold_RESET Sequence

The sequence steps are described bellow :

1. Discrete logic monitors on-board power supplies states determining when the IFC_1210 is ready for start-up sequence. Following power sources are monitored through :
   - The VME power inputs (+3.3[V] and +5.0[V]) are monitored by the LI Controller MAX5970 (U702).
   - The BMR 463 DCDC outputs (1.0[V], 1.5[V] and FMC_VADJ) are monitored by a dedicated circuit TI TPS38600 (U703).
   - The TPS74901 LDOs are monitored through there PG signals (wired OR)

2. The “PON” FPGA is configured autonomously through its Master Serial SPI. The attached SPI Flash EPROM is read-out in Quad-bit mode @ 50 MHz. The “PON” FPGA is configured in less than 40[ms]
3. The PCI Express Switch PES32NT8AG2 / PES32NT24AG2 (U200) RESET is released with “SWMODE[3:0]” defined by the static options SW2-[8:7]. The PES32NT8AG2 / PES32NT24AG2 “Boot Configuration Vector” is supplied by the “PON” FPGA.
    - PES32NT8AG2 / PES32NT24AG2 Initialization is fetched from the attached Serial EEPROM (24C256)

At this point the Cold RESET sequence execution can be selected between Mode_0 or Mode_1 with the static option SW2-4.

While Mode_0 is enabled (SW2-4 = “OFF”) the “PON” FPGA embedded logic continues the configuration process as :

4. The “CENTRAL” FPGA and the “IO” FPGA are configured under control of two dedicated FSM, extracting the FPGA bit-stream from the SPI Serial Flash EPROM. The two FPGA are configured in parallel.
    - The “IO” FPGA Spartan-6 is configured in Slave Serial Mode @ 200 Mbit/s. (For a XC6SLX25 → 32[ms])
    - The “CENTRAL” FPGA Virtex-6T is configured in Slave SelectMAP Mode @ ~400 Mbit/s. (For a XC6VLX130T → 110[ms])
5. The on-board RESET is released to the “IO” FPGA and “CENTRAL” FPGA
6. The on-board RESET is released to the processor P2020, starting-up its boot code.

While Mode_1 is enabled (SW2-4 = “ON”) the RESET is released to the processor P2020, starting-up its boot code. From this point it is under the responsibility of the P2020 to configure the “IO” & “CENTRAL” FPGA. The configuration resources (control & status) are located in the “PON” FPGA and mapped on the P2020 ELB Bus.

7. The on-board RESET is released to the processor P2020, starting-up its boot code.
8. The “CENTRAL” FPGA and the “IO” FPGA are configured under control of the P2020.
9. The on-board RESET is released to the “IO” FPGA and “CENTRAL” FPGA

2.8.1 Front panel RESET action

The IFC_1210 uses the "Ergonomic IEEE Hot-swap Injector/Ejector Handle" (ELMA 81-096) with Micro-switch (ELMA 81-088-1) to implement the front panel RESET action. Action on the switch is interpreted as :

- SHORT action (< 1[s]) Activate only the CPU P2020 Hardware RESET
- LONG action (> 1[s]) Complete “Cold_RESET” (Refer to previous chapter)

The micro-switch denouncing logic and the short/long interpretation is implemented in the “PON” FPGA.

2.9 QorIQ P2020 Computing Core

The IFC_1210 P2020 computing core follows the FREESCALE reference design implementation, limiting the SW effort for OS porting. (LINUX and VxWorks)

The P2020 computing core is fully operational without “CENTRAL” and “IO” FPGA configured. This allows to have a fully functional environment under OS, connected on the Ethernet Local Network, with PMC/XMC mezzanine operational. In this case, the “CENTRAL” and “IO” FPGA configuration process can be left under control of the P2020. (.bit/.mcs files downloaded from the Network)

The IFC_1210 computer core implementation take provisions for future upgrade to P2040, P2041 version.

2.9.1 P2020 Processor Unit Generalities

The IFC_1210 central microprocessor QorIQ P2020 (U800) is implemented with following configuration options.

- 1.2 GHz core frequency
- DDR3 600 MHz clock (½ core frequency)
- Single PCI Express GEN1 configurable as Root Complex (RC) or End Point (EP)
- Boot Mode selectable with static DIP switch SW1-[6:5]
  - = “00” → microSD
  - = “01” → NOR Flash EPROM
  - = “10” → SPI Flash EPROM
  - = “11” → No BOOT (Reserved for boot through eLBC in GPGM mode)
- ELB Bus 2.5[V] / 3.3[V] running at 75 MHz.

2.9.1.1 RESET and Power-up options

To Be Updated

2.9.1.2 U-BOOT Support

To Be Updated

2.9.1.3 COP Support

The IFC_1210 provides a COP interface (P2020 JTAG ports + side band signalling) dedicated to FREESCALE CodeWARRIOR tool.

- P2020 COPS receptacle connector (P800) 2x8 16-pin 2[mm]

2.9.2 DDR3 System Memory

The IFC_1210 P2020 System Memory is implemented with five(5) DDR3 running at 600 MHz. The ECC is fully supported.

- 1 GBytes
- 4 DDR3 x16 2 Gbit devices (U830, U831, U832, U833) (DATA) → 1 GBytes
- 1 DDR3 x16 2 Gbit devices (U834) (ECC Hamming code syndrome)
- 600 MHz DDR3
- Ready for 2 GBytes by using up-coming 4Gb DDR3 devices

Note *The DDR3 System Memory Controller can be also configured to operate in asynchronous mode with clocking operation up to 1066 MHz.*

2.9.3 NOR Flash

The IFC_1210 implements a 16-bit wide NOR Flash Memory interfaced on the P2020 Enhanced Local Bus. This non-volatile device can be defined for P2020 ColdRESET boot.

- 128 Mbit SPANSION S29GL128TFI010 (U815)

The NOR Flash can be (re-)programmed directly with the Freescale "CodeWarrior" tool or with utilities supplied in U-BOOT.

2.9.4 NAND Flash

The IFC_1210 implements a 8-bit wide NAND Flash Memory interfaced on the P2020 Enhanced Local Bus. This non-volatile device can be defined for P2020 boot.

- 2Gbit HYNIX HY27UF082G2B (U813)
- Upgrade path (pin compatible) to 4, 8, 16 and 32 Gbit.

The NAND Flash can be (re-)programmed with utilities supplied in U-BOOT.

Note *The IFC_1210 can be equipped under request with larger NAND Flash device. Consult IOxOS.*

2.9.5 SPI Flash Memory

The IFC_1210 implements a SPI Serial Flash Memory connected to the P2020 SPI interface.This non-volatile device can be defined for P2020 boot.

- 128 Mbit SPANSION S25FL128P0 (U824)

The NAND Flash can be (re-)programmed with utilities supplied in U-BOOT.

Note *Same devices type are used for FPGA bit-streams configuration storage.*

2.9.6 EEPROM Memory

The IFC_1210 implements two(2) I2C EEPROM Memory interfaced with the P2020 I2C#1 and I2C#2 Bus controllers. These NV memories are used for the P2020 “Board Signature” and “BOOT Sequencer”

- 8Kbit ATMEL 24C08 (U817) for “Board Signature”
  - I2C#1 Address = 50H)
- 256Kbit ATMEL 24C256 (U819) for “BOOT Sequencer”
  - I2C#2 Address = 68H

Note *ATMEL 24C256 is also used by the PCI Express Switch IDT PES32NT24AG2*

2.9.7 RTC

The IFC_1210 implements one Real Time Clock with a local 32.768 Khz crystal. The RTC is interfaced with the P2020 I2C#1 controller.

- MAXIM DS1339U-33 (U823)
  - I2C#2 Address = 50H
- Local CRYSTAL 32.768 KHz (Y100)

A CR1220 battery holder (BT800) provides back-up capability while IFC_1210 power is removed.

2.9.8 MicroSD Card Holder

The IFC_1210 implements one microSD holder (socket). This non-volatile device can be defined for P2020 boot.

- microSD compatible storage up to 32 GBytes. (J803)

The microSD card can be (re-)programmed with utilities supplied in U-BOOT.

Note *The microSD is able to hold a complete LINUX system*

2.9.9 RS232 Interface

The IFC_1210 implements one RS232C Serial line, available on the front.

- RS232C available on standard RJ45 (Following PSI pin assignment) (J802)

RJ45 pin#	Function
1	Not used (DCD)
2	Not used (RTS)
3	GNDC

4	TXD
5	RXD
6	GNDC
7	Not used (CTS)
8	Not used (DTR)

- Electrical IF implemented with EXAR SP3232EEY-L (U802)

2.9.10 USB Host Interface

The IFC_1210 implements one Host USB 2.0, available on the front panel.

- PHY SMSC 3300 (U820)
- Type A USB 2.0 connector vertical mount (P801)
- 24 MHz clock reference built in the “PON” FPGA from the CLK100_REF

USB storage device can also be used as bootable media under control of U-BOOT

Note *The USB storage device is able to hold a complete LINUX system*

2.9.11 10/100/1000 BaseT Ethernet

The IFC_1210 implements two 10/100/1000 Base-T Ethernet available on the front panel.

- Standard RJ45 connectors with embedded magnetics (J801)
- Dual PHY MICREL KSZ9021RN (U826, U828)
- 25 MHz clock reference built in the “PON” FPGA from the CLK100_REF

ETH Port	MAC Address			Comments
	MAC Address IFC_1210			
	[47:11]	[10:1]	[0]	
ETH0	7C DD 10 01 08	Serial NB	0	IOxOS MAC Address (Front IPane #0l
ETH1	7C DD 10 01 08	Serial NB	1	IOxOS MAC Address (Front Panel #1)

Table 2.12.: IFC_1210 Ethernet MAC Address assignation

2.9.12 P2020 ELB Interface ("PON" FPGA)

The P2020 ELB (GPCM mode 8-bit Data + 16-bit Address + Control signals) is connected to the “PON” FPGA. This simple interface allows to map up to 64K 8-bit registers dedicated to key FPGA control & status information supporting on-board FPGA configuration (or re-configuration) directly from the P2020 computing core.

- Status of IFC_1210 static options. (DIP Switch & Hex-ROT)
- Power and Clocking Management
- Control & Status for “CENTRAL” FPGA configuration process
- Control & Status for “IO” FPGA configuration process
- Programming of SPI Flash EPROM storing the IFC_1210 on-board FPGA bit-streams
- 1[ms] ColdRESET Timer
- P2020 Programmable RESET management
- IDT PES32NT24AG2 PCI Express Switch management
- 8 KBytes Scratch SRAM

Refer to chapter *4.2 ELB PON FPGA Resources* for a complete description of the implemented functions.

Note *Additional user function can be easily added in the “PON“ FPGA device, providing application specific support.*

2.9.13 PCI Express Interface

The P2020 PCI Express interface is the main IO connection to the IFC_1210 infrastructure. The P2020 is connected to the PCI Express Switch PES32NT24AG2 Port_0.

- Single PCI Express port (#1) activated
- Configured as GEN1 x4
- By default Root Complex mode (RC)

Note *The P2020 PCI Express could be defined as End-Point for specific application.*

2.10 PCI Express GEN2 Infrastructure

The PCI Express GEN2 Switch IDTPES32NT24AG2 (U200) is the IFC_1210 central communication component.

Following drawing represents the IFC_1210 PES32NT24AG2 (U200) implementation.

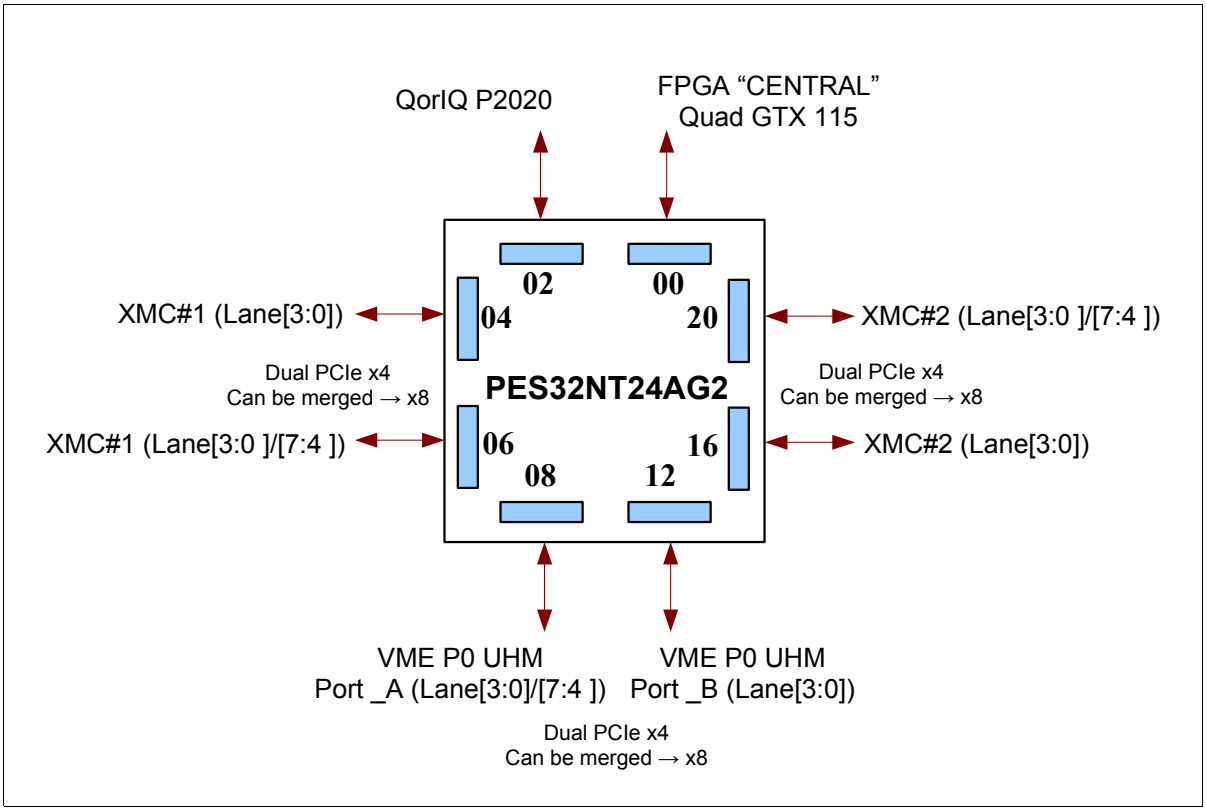

Illustration 15 : IFC_1210 IDT PCI Express Switch Implementation

The following table provides the IDT PES32NT24AG2 Ports assignment with its associated capabilities

Port	Link Partner	UP	DWN	NTB	DMA	SSC	Comments
00	P2020 (U800)	Y	Y	Y	Y	N	The P2020 PCIe x4 Port can be statically defined as RC (Root Complex) or EP (End Point)
02	"CENTRAL" FPGA (U400)	N	Y	N	--	N	Virtex-6T IP core PCIe x4 Port EP (End Point)
04 05	XMC#1A	Y	Y	Y	--	Y	Standard is Dual PCIex4 Can be merged → PCIe x8 Can be splitted → Quad PCIe x2 Iso serve the PCIe-PCI Bridge PEX8112 (U202) SSC supported only when single PCIe x8 is used
06 07	XMC#1B	Y	Y	Y	--	N	
08 09 10 11	VME P0 UHM Port_B	Y	Y	Y	Y	Y	Standard is Dual PCIex4 Can be merged → PCIe x8 Can be splitted → Quad PCIe x2 Can be splitted → Octal PCIe x1 SSC supported only when single PCIe x8 is used
12 13	VME P0 UHM Port_A	Y	Y	Y	--	--	

14 15							
16 17 18 19	XMC#2A	Y	Y	Y	--	Y	Standard is Dual PCIex4 Can be merged → PCIe x8 Can be splitted → Quad PCIe x2 Can be splitted → Octal PCIe x1
20 21 22 23	XMC#2B	Y	Y	Y	--	--	SSC supported only when single PCIe x8 is used

Table 2.13 : IFC_1210 PES32NT8AG2 / PES32NT24AG2 Port Assignation

2.10.1 IDT LOGAN Switch

The IDT PES32NT24AG2 (U200) is a member of latest PCI Express GEN2 generation, optimized for embedded applications. This new switch generation provides capabilities for real-time and high performance data acquisition system.

IDT PES32NT24AG2 key features

- Switching capability of 32 GBytes/s
- Eight Ports PCI Express x4 GEN2/GEN1
- Two adjacent x4 Ports can be merged to form a single PCI Express x8 GEN2/GEN1
- Programmable Tx De-emphasis, Rx Equalization and Tx Drive strengh
- Low latency cut-through architecture
- Switch partitioning with dynamic reconfiguration
- Non Transparent Bridge capability available on the eight Ports
- Multicast with up to 64 multicast group
- Dual channel DMA controller with linked list descriptors
- Flexible clocking Mode (CFC Common, CFC Non-common, SSC)
- Hot-Plug on all Downstream Ports

Two adjacent PCI Express x4 Port can be merged together to form a single PCI Express x8 Port. In this case the Port 06, 12, and 20 are used for highest PCI Express lanes [7:4]. This merging capability is supported on following IFC_1210 sections :

- Ports {04:06} → XMC#1 (Bottom VME P2)
- Ports {16:20} → XMC#2 (Top VME P1)
- Ports {08:12} → VME P0 UHM

2.10.2 PCI Express GEN2 Clock Distribution

The IDT PES32NT24AG2 (U200) PCI Express Switch clocking infrastructure is set-up with a modular schema, accommodating several modes of operation :

- CFC Common clock with link partner
- CFC Non-common clock with link partner
- SSC clock Common with link partner

The clocking operation mode can be selected by Port through following PES32NT8AG2 / PES32NT24AG2's registers :

- PxxCLKMODE[1:0] {PCLKMODE} = Global or Local Clock Mode
- SCLK {PCIELSTS} = Common/Non-common clock with link partner

Following table sums up the PES32NT8AG2 / PES32NT24AG2 Port clocking configuration :

PES32NT8AG2 / PES32NT24AG2	CLK Source	Port	Comments
GCLK0 GCLK1	CLK100REF CLK100REF	PES32NT8AG2	Global Reference clock. 100 MHz +/- 50[ppm]
P00CLK	'0'		Fixed to '0' with Global CLOCK
P02CLK	'0'		
P04CLK	XMC1_RxCLK0	XMC#1 (Bottom P2)	Clock source selectable between the on-board CLK100_REF100 MHz +/- 50[ppm] and a clock reference supplied by the XMC1. Selection through P04CLKMODE[1:0] & P06CLKMODE[1:0]
P06CLK	XMC1_RxCLK1	XMC#1 (Bottom P2)	
P08CLK	UHM_RxCLKA	VME P0 UHM Port_B	Clock source selectable between the on-board CLK100_REF100 MHz +/- 50[ppm] and a clock reference supplied by the VME P0 UHM. Selection through P08CLKMODE[1:0] & P12CLKMODE[1:0]
P12CLK	UHM_RxCLKB	VME P0 UHM Port_A	
P16CLK	XMC2_RxCLK0	XMC#2 (Top P1)	Clock source selectable between the on-board CLK100_REF100 MHz +/- 50[ppm] and a clock reference supplied by the XMC2. Selection through P16CLKMODE[1:0] & P20CLKMODE[1:0]
P22CLK	XMC2_RxCLK1	XMC#2 (Top P1)	

Table 2.14 : IFC_1210 IDT PES32NT24AG2 Clock Support

The PES32NT8AG2 / PES32NT24AG2 (U200) P04CLK/P06CLK for Ports {06:08} are driven with the same clock source with two loads. (The two signal pairs are very close). The 100 ohms terminators are located at far end.

The selection of the external PCI Express clock reference is required while the Link partner is running with SSC (Spread Spectrum Clocking) mode.

Only a single PCI Express Port, configured in x4 or x8, located on XMC#1,XMC#2 or VME P0 UHM can support SSC mode.

2.10.3 PES32NT24AG2 PCI Express Naming

The PCI Express Lane naming (Tx → Rx) and (Rx → Tx) is defined referenced to the PES32NTXXAG2 with following convention.

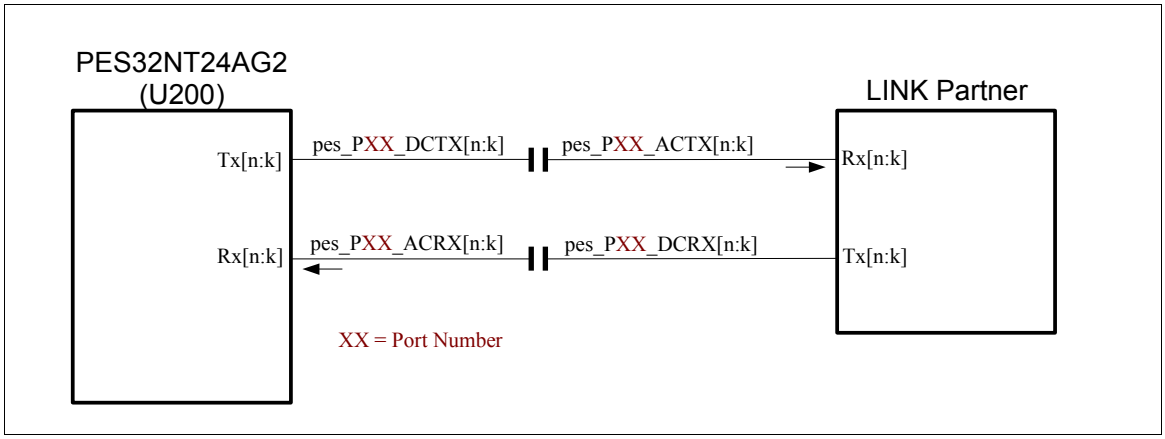

Illustration 16 : IFC_1210 PCI Express Naming Convention

2.10.4 PES32NT24AG2 Static Configuration

The PES32NT24AG2 is configured at power-up through three path

- Pin strapping (static option)
- Attached SPI EEPROM 24C256
- SMBus Slave port controlled by the TOSCA II I2C Master Controller or ELB I2C Master Controller

The PES32NT24AG2 static configuration is based on pin strapping. Value found on these specific pins during RESET de-assertion are memorized and used as default options.

Several of these power-up options can also be overridden with the Serial Flash EEPROM (24C256) or from the SMBus Slave port.

Following table sums up the PES32NT24AG2 PIN strapping options.

Signal	Override	IFC_1210 Setup	Name & Description
GCLKFSEL	N	'0'	Global Clock Frequency Select. Fixed to '0' → 100 MHz
CLKMODE[1:0]	Y	"PON" FPGA	Clock Mode Refer to PES32NT24AG2 User's Manual Table 2.4
RSTHALT	Y	"PON" FPGA	Reset Halt Refer to PES32NT24AG2 User's Manual Table 3.2
SSMBADDR[2:1]	N	"01"	SMBus Slave Address
SWMODE[3:0]	Y	"PON" FPGA	Switch Mode Refer to PES32NT24AG2 User's Manual Table 3.8 At Cold_RESET the SWMODE[3:0] is conditioned by SW2-[8:7] as : **SW2-[8:7]** / **Switch Mode** 00 / Single partition

			01 Single partition with reduced latency 10 Single partition with Serial EEPROM Initialization with reduced latency 11 Reserved, User defined in "PON" FPGA
STK0CFG[1:0]	Y	"01"	Stack 0 Configuration (P2020 + "CENTRAL" FPGA" → Port_0 = PCI Express x4, → Port_1 = PCI Express x4
STK1CFG[1:0]	Y	"PON" FPGA STK1CFG[1:0]	Stack 1 Configuration (XMC#1) = "00" → Port_4 + Port_6 = PCI Express x8 = "01" → Port_4, Port_6 = PCI Express x4 = "11" → Port_4, Port_5, Port_6, Port_7 = PCI Express x2
STK2CFG[4:0]	Y	"PON" FPGA STK2CFG[4:0]	Stack 2 Configuration (VME P0 UHM) Refer to PES32NT24AG2 User's Manual
STK3CFG[4:0]	Y	"PON" FPGA STK3CFG[1:0]	Stack 3 Configuration (XMC#2) = "00" → Port_16 + Port_20 = PCI Express x8 = "01" → Port_16, Port_20 = PCI Express x4 = "11" → Port_16, Port_18, Port_20, Port_22 = PCI Express x2 ***Note*** *Can also be defined in Octal PCIe x1*

Table 2.15 : IFC_1210 PES32NT24AG2 Static Options ("Boot Configuration Vector")

The PES32NT24AG2 "Boot Configuration Vector" and the "Reset" are supplied by the "PON" FPGA. Exception of SWMODE[3:0], the "Boot Configuration Vector" value is hard coded in the "PON" FPGA. The SWMODE[3:0] determines the N+1 initialization process of the PES32NT24AG2. The mode is than determined by the "PON" FPGA, related to the static option SW2-8:7.

PES32NT24AG2 Stack	PES32NT24AG2 Ports	CFG[k:n]	PCIe CFG	Comments
Stack_0	0,2	STK0CFG[0]	x4	P2020 + FPGA
Stack_1	4,5,6,7	STK1CFG[1:0]	x8, x4, x2	XMC #1
Stack_2	8,9,10,11,12,13,14,15	STK2CFG[4:0]	x8, x4, x2, x1	VME P0 UHM
Stack_3	16,18,20,11 (17,19,21,23)	STK3CFG[1:0]	x8, x4, x2, (x1)	XMC #2

Table 2.16 : IFC_1210 PES32NT24AG2 Stack Configuration

A Serial EEPROM 24C256 is directly attached to the PES32NT24AG2. This non-volatile device can store the initialization sequence. A complete description of the EEPROM format is supplied in the PES32NT24AG2 User's Manual (Refer to Chapter 12.2) The Serial EEPROM 24C256 can be re-programmed (1st programmed) from the RC (Root Complex) or

The PES32NT24AG2 can also be initialized through its SMBus Slave port. In this case an external SMBus Master can be used to initialize the PES32NT24AG2. All SW resources of the Switch are accessible through its SMBus Slave port. The IFC_1210 "CENTRAL" FPGA and the ELB PON FPGA Resources "Refer to chapter *4.2*" integrates a SMBus controller (I2C) which is used to control the PES32NT24AG2 SMBus Slave port.

Thanks to the PON_FSM, supplied in the IFC_1210 "CENTRAL" FPGA, the PES32NT24AG2 initialization can be handled autonomously while the "CENTRAL" FPGA is configured.

2.10.5 VME P0 UHM PCI Express Expansion

The VME P0 connector (UHM) provides eight(8) PCI Express Lane. These eight(8) lanes can be configured as :

- Single Port PCI Express x8 GEN2
- Dual Port PCI Express x4 GEN2
- Quad Port PCI Express x2 GEN2
- Eight Port PCI Express x1 GEN2

To provide DC coupling protection, all PCI Express lanes (Tx and Rx) are AC coupled (100[nF] on the IFC_1210 board. (PCI Express specification recommends to insert the AC coupling close to the Tx section. The fact to have two(2) AC coupled inserted on the Rx lane will not impact the PCI Express functionality)

Following table sums up the PCI Express extension capability wired to VME P0

VME UHM P0 Signal Name	VME UHM P0 pin#	PES32NT24AG2 Lanes	PCI Express Port			
			x8	x4	x2	x1
P0_A_TxRx[0]	A[18,19] - D[18,19]	PE8[0]				
P0_A_TxRx[1]	B[18,19] - E[18,19]	PE9[0]				
P0_A_TxRx[2]	A[16,17] - D[16,17]	PE10[0]				
P0_A_TxRx[3]	B[16,17] - E[16,17]	PE11[0]				
P0_B_TxRx[0]	A[14,15] - D[14,15]	PE12[0]				
P0_B_TxRx[1]	B[14,15] - E[14,15]	PE13[0]				
P0_B_TxRx[2]	A[12,13] - D[12,13]	PE14[0]				
P0_B_TxRx[3]	B[12,13] - E[12,13]	PE15[0]				

Table 2.17 : IFC_1210 VME P0 UHM PCI Express Expansion capability

The VME P0 UHM implement Tx and Rx PCI Express clock reference (100 MHz) for each PCI Express x4 Port (Port_A and Port_B)

- CLK_100REF (Local 100 MHz) supplied (P0_A_TxCLK and P0_B_TxCLK)
- External 100 MHz (CFC or SSC) connected to the PCI Express Switch PES32NT24AG2 Local clock
  - P0_A_RxCLK → P08CLK
  - P0_B_RxCLK → P12CLK

In case of the VME P0 UHM PCI Express extension is configured as four(4) PCI Express x2 ports or eight(8) PCI Express x1 ports, the port group 08 and 12 shall remain coherent.

The PCI Express External Cabling side-band signalingshall beimplemented across the VME P0 UHM GPIO[11:0] signals, connected directly to the “CENTRAL” FPGA or in dedicated control logic embedded in the Read_IO (I.e MPR_1260)

Only two(2) PCI Express NT ports can be enabled on the VME P0 UHM PCI Express extension. In case of four(4) PCI Express x2 ports or eight(8) PCI Express x1 ports mode of operation, only two(2) ports can be configured as NT.

Only a single embedded DMA controller can be allocated to the VME P0 UHM PCI Express extension.

2.10.6 VITA42.3 XMC PCI Express Expansion

The VITA42.3 XMC sites provides eight(8) PCI Express Lane. These eight(8) lanes can be configured as :

- Single Port PCI Express x8 GEN2
- Dual Port PCI Express x4 GEN2
- Quad Port PCI Express x2 GEN2
- Octal Port PCI Express x1 GEN2 (optionnaly on XMC#2)

Following table sums up the PCI Express extension capability wired to XMC VITA42.3

XMC Signal Name	XMC pin#	PES32NT24AG2 Lanes		PCI Express Port		
		XMC#1	XMC#2	x8	x4	x2
PER0k0/PET0k0	AB01 / AB11	PE4[0]	PE16[0]			
PER0k1/PET0k1	DE01 / AB11	PE4[1]	PE17[0]			
PER0k2/PET0k2	AB03 / AB13	PE5[0]	PE18[0]			
PER0k3/PET0k3	DE03 / AB13	PE5[1]	PE19[0]			
PER0k4/PET0k4	AB05 / AB15	PE6[0]	PE20[0]			
PER0k5/PET0k5	DE05 / AB15	PE6[1]	PE21[0]			
PER0k6/PET0k6	AB07 / AB17	PE7[0]	PE22[0]			
PER0k7/PET0k7	DE07 / AB17	PE7[1]	PE23[0]			

Table 2.18 : IFC_1210 XMC VITA42.3 PCI Express Expansion capability

Following the VITA 42.3-R2010 specification, he AC coupling capacitors are implemented only on the Tx lanes (PES32NT24AG2 → XMC connector)

Multiple PCI Express ports available on the XMC mezzanine allows to use the XMC as PCI Express Expension. XMC_3105 provides Dual PCI Express x4 External Cabling sockets. XMC expension for Quad x2 or Octal x1 can be supported.

2.11 “STATIC” CPLD

The IFC-1210 implements a small CoolRunner II XC2C64A 44-pin VQFP CPLD “STATIC” (U105) used to reduce the number of PCB traces running from the static options DIP switch located on the bottom of the board to the “PON” FPGA. This 44-pin VQFP device is located close to the IFC_1210 DIP switch selectors.

- Implement a 32 → 1 multiplexer for static option concentrator.

2.12 "PON" FPGA Spartan_6

The “PON” FPGA Spartan-6 (U100) implements IFC_1210 power-up critical functions. This FPGA Spartan-6 XC6SLX25 FG484 pins device configures itself from its SPI Flash EPROM (U103) at Power_UP even.

Following functions are integrated in the “PON” FPGA

a) RESET Management and DCDC monitoring

b) “IO” FPGA and “CENTRAL” FPGA configuration

c) Serial interface with the “CENTRAL” FPGA for slow signals. This proprietary interface allows to reduce significantly the IO budget of the “CENTRAL” FPGA Virtex-6T

- Tx → Static options as DIP Switches, HexROT, VME64x Geographical
- Rx ← LED indicators, ...

d) ELB 8-bit Slave supporting control of the FPGA configuration under control of the P2020

e) Remote SPI control path. Support SPI Flash EPROM access from the “CENTRAL” FPGA infrastructure

f) I2C 8-port router. Support of the “I2C Master Controller” embedded in the “CENTRAL” FPGA infrastructure

g) IDT8N4Q001 control PGMCLK_REF

h) VME64x side-band 3.3[V] signalling deported from the “CENTRAL” FPGA infrastructure

i) PES32NT24AG2 “Boot Configuration Vector”

j) P2020 Power-up “Static Configuration”

2.12.1 “PON” FPGA IO_Bank Assignation

Following table sums up Spartan-6 IO_Bank attribution

- IO_Bank_0 used for high-speed interface with VCC_IO = VADJ
- IO_Bank_0 requires a VREF_0 = VADJ:2[V]

Bank_IO	VCC_IO	Max_IO		Comments
0	VADJ 1.5-2.5[V]	46	• V6 Configuration • V6 Serial scanning • FPGA RESET • STATIC CPLD Interface • LED indicators	High speed Bank with VREF_0 at VADJ : 2[V]
1	2.5[V]	62	• General • Clock References • P2020 ELB Interface • P2020 Configuration • IDT8N4Q001 Control	
2	3.3[V]	80	• VME64x remote support	Bank_IO_2 used for Config.

			• SPI#1 • SPI#2, SPI#3	VME64x direct signalling
3	2.5[V]	64	• XMC, PMC side-band signals • PES Boot vector • I2C Bridge • FMC side-band signals	

Table 2.19 : IFC_1210 "PON" FPGA IO_Bank Assignation

2.12.2 Interconnection "CENTRAL" ↔ "PON" FPGA

To support the communication between the "IO" FPGA (U400) and the "CENTRAL "FPGA" (U406) dedicated signaling is implemented. This synchronous communication is supported from "PON" FPGA IO_Bank_0 and "CENTRAL" FPGA IO_Bank_24, both IO_Bank are powered with VADJ (1.5[V] – 2.5[V].

- Serial stream "IO" → "CENTRAL" for static options
- Serial stream "CENTRAL" → "IO" for control and command
- High speed serial stream "IO" ↔ "CENTRAL" supporting VME64x arbitration
- SPI and I2C Bridge "IO" ↔ "CENTRAL"

The bi-directional serial streaming between the "PON" FPGA and the "CENTRAL" FPGA is implemented through following HDL files instantiated :

- "tosca2_serial_scan_hsvme1_s6.vhd" → "PON" FPGA
- "tosca2_serial_scan_hsvme1_v6.vhd" → "CENTRAL" FPGA
- "tosca2_serial_scan_ls1_s6.vhd" → "PON" FPGA
- "tosca2_serial_scan_ls1_v6.vhd" → "CENTRAL" FPGA

2.12.3 On-board FPGA Configuration

The three on-board FPGA (Virtex-6T and Spartan-6) are SRAM based devices requiring configuration at power-up. This configuration process can be handled with :

- Automatically at power-on with bit-stream(s) stored in the SPI Flash EPROM
- Under control of the ISE iMPACT software through the dedicated JTAG TAP
- Under control of the P2020 processor (Virtex-6T only)

Through dedicated JTAG TAP connector (P100), the XILINX ISE iMPACT tool can configure (program) the on-board FPGA and can also program the SPI#1 Serial Flash (U104). (Red path) This connection is also used while XILINX ChipScopePRO is used.

Under normal operation, the IFC_1210 is fully configured in less than 200[ms]. Further P2020 boot process can extend this availability time.

The following functional diagram shows the IFC_1210 FPGA configuration sub-system.

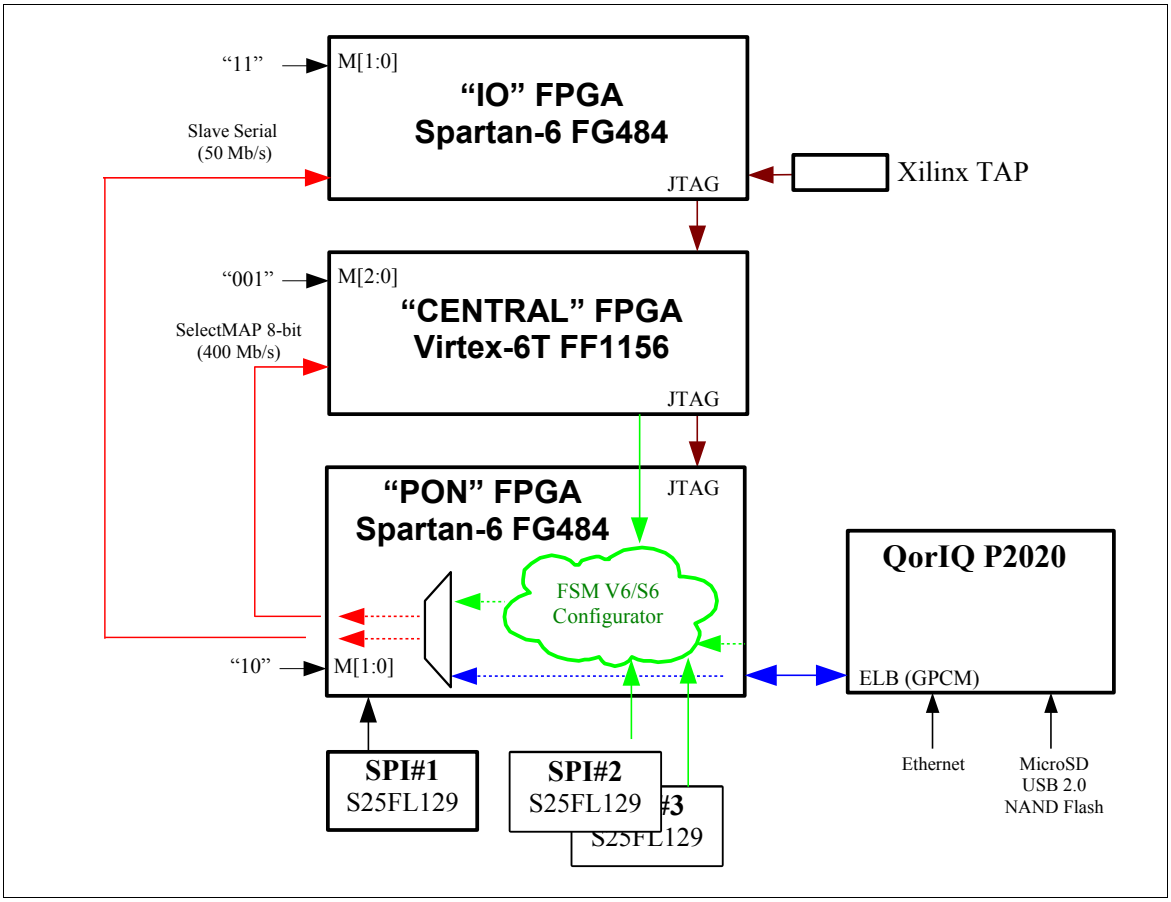

Illustration 17 : IFC_1210 FPGA Configuration Functional Diagram

The IFC_1210 FPGA configuration procedure is controlled by three static options as :

Static	Description		Comments
SW2-1 SW2-2	FPGA Config [1:0]	This two static options selects the "CENTRAL" FPGA and "IO" FPGA bit-stream number used by default at power-up. 00 Back-up bit-stream, 01 1st FPGA bit-stream 10 2nd FPGA bit-stream 11 3rd FPGA bit-stream	The back-up bit-stream #0 should be updated very carefully. In case of back-up bit-stream corruption, the SPI Flash shall be reloaded with specific iMPACT XILINX tool.
SW2-3	JTAG_Config	This static allows to disable the power on XILINX FPGA auto configuration. • "ON" FPGA Configuration process through XILINX TAP connector • "OFF" FPGA Configuration process autonomous at power-up.	This stati option shall be positionned "ON" while the FPGA are configured with the XILINX iMPACT tool

Table 2.20 : IFC_1210 FPGA Configuration static option

Remote configuration commands , issued by the "CENTRAL" FPGA infrastructure can also trigger the "FSM V6/S6 Configurator" to re-trigger the "CENTRAL" FPGA and "IO" FPGA configuration

process with programmable bit-stream.

Under P2020 control, through its ELB Bus, the “CENTRAL” FPGA and “IO” FPGA can be (re-)configured with two selectable modes :

1. Trigger the “FSM V6/S6 Configurator” with selectable bit-stream number. In this case the FPGA bit-stream are fetched from the SPI Flash EPROM (U105, U106) devices.
2. Load the complete bit-stream images through its ELB interface. In this case the bit-streams shall be supplied by the P2020 non-volatile memories (NAND, NOR, microSD) or directly from a FTP server through the Ethernet.

The two control registers “ELB_FPGA_CFGCTL” and “ELB_FPGA_CFGDAT” mapped on the P2020 ELB Bus interface are used to configure the FPGA. (Refer to chapter 4.2.4)

2.12.3.1 “PON” FPGA Spartan-6 Configuration

The “PON” FPGA (U100) Spartan-6 (XC6SLX45) is configured automatically at power-up or under other “PON_Reset” condition from the attached SPI#1 Serial Flash Device (U103). To do so, the Spartan-6 configuration mode is fixed with M[1:0] = 01 → “Master Serial/SPI” mode.

The SPI#1 device (Spansion S25FL129P) is interfaced to the Spartan-6 with “Quad SPI” mode, supplying 4-bit at every clock cycle.

For optimal (and deterministic) configuration latency, the “PON” FPGA Spartan-6 CCLK input is driven by an external 100 MHz clock reference (LVTTL), divided internally by 2, providing sustained 200 Mbit/s configuration rate (Spartan-6 XC6SLX45 configured in less than 65 [ms])

The “PON” FPGA Spartan-6 can be configured only with a single bit-stream image stored in the SPI Flash EPROM #1 device (U103).

2.12.3.2 “IO” FPGA Spartan-6 Configuration

The “IO” FPGA (U406) Spartan-6 can be configured or re-configured in two different mode of operation using the “Slave Serial” configuration mode.

- Under control of a controller logic “FSM S6 Configurator” located in the “PON” FPGA
- Under control of the P2020 processor through its dedicated ELB 8-bit Interface. (Refer to chapter 4.2.4)

With the “FSM S6 Configurator”, the “IO” FPGA Spartan-6 XC6SLX45 is configured in Slave Serial at 50 Mbit/s (Spartan-6 XC6SLX45 configured in less than 250 [ms])

The four(4) bit-stream images are stored in the SPI#1 Flash EPROM (U103). The 2-bit static option (SW2[2:1]) selects the bit-stream number to be used. In case of configuration error detected, the bit-stream #0 is used as back-up and the configuration process is re-executed.

While configured by the P2020, the bit-stream is provided by any source as local non-volatile memory of directly across the Ethernet Network. The configuration performance is this case is related to the P2020 execution.

Status informations attached to the “FSM S6 Configurator” is supplied to the TOSCA II infrastructure and also directly to P2020 local processor through ELB status register “ “ELB_FPGA_CFGCTL”.

2.12.3.3 “CENTRAL” FPGA Virtex-6T Configuration

The “CENTRAL” FPGA (U400) Virtex-6T can be configured or re-configured in two different mode of operation using the “Slave SelectMAP x8” (parallel) configuration mode.

- Under control of a controller logic “FSM V6 Configurator” located in the “PON” FPGA
- Under control of the P2020 processor through dedicated ELB 8-bit Interface. (Refer to chapter 4.2.4)

With the “FSM S6 Configurator”, thanks to the use of the “Slave Select_MAP”, running at 50 MHz (400 Mbit/s), the “CENTRAL” FPGA Virtex-6T is configured at optimal speed. (Virtex-6T XC6LX130T configured in less than 120 [ms])

The four(4) bit-stream images are stored in the two SPI Flash EPROM #2 and #3 (U101, U102), each one storing a 4-bit nibble. The 2-bit static option (SW2[2:1]) allows to select the bit-stream number to be used. In case of configuration error detected, the bit-stream #0 is used as back-up and the configuration process is re-executed.

Status informations attached to the “FSM V6 Configurator” is supplied to the TOSCA II infrastructure and also to P2020 local processor through ELB status register “ “ELB_FPGA_CFGCTL”.

While configured by the P2020, through its ELB 8-bit Interface, the bit-stream is provided by any source as local non-volatile memory of directly across the Ethernet Network. The configuration performance is this case is related to the P2020 execution.

The “CENTRAL” FPGA Virtex-6 dedicated configuration signalling is refurbished during runtime for communication between the “PON” and “CENTRAL” FPGA.

2.12.4 SPI Flash Resources

The IFC_1210 implements three non-volatile memory SPI Flash EPROM devices dedicated to store FPGA bit-streams and related signature. The three SPI Flash EPROM are wired to the “PON” FPGA with Quad_Bit interface.

All three devices can be (re-)programmed and read-back through the PCI Express infrastructure (P2020 Processor / External PCI Express Cable), directly from the VME64x Interface or through the P2020 ELB Interface.

Additionally the The SPI#1 128Mbit device (SPANSION S25FL129P) can also be (re-)programmed with the XILINX ISE iMPACT tool.

SPI#	Type	Size	Storage	Comments
1	SPANSION S25FL129P (or EoN EN25Q128) (U103)	64Mb	“PON” FPGA Spartan-6 bit-stream (8Mb) “IO” FPGA Spartan-6 bit-stream (32Mb) PON_FSM Microcode (16Mb) IFC_1210 Board Signature (8Mb)	Spartan-6 bit-stream size : XC6SLX25 ~ 6.5 Mb XC6SLX45 ~ 11.8 Mb
2	SPANSION S25FL129P (or EoN EN25Q128) (U101)	128Mb	“CENTRAL” FPGA Virtex-6T bit-stream (lower nibble) Storage for four(4) or two(2) bit-streams image, depending on the FPGA type. • 4x → LX130T / LX195T • 2x → LX240T and bigger	Virtex-6T bit-stream size : LX130T ~ 47 Mb LX195T ~ 58 Mb LX240T ~ 72 Mb
3	SPANSION S25FL129P (or EoN EN25Q128) (U102)	128Mb	“CENTRAL”FPGA Virtex-6T bit-stream (higher nibble)	

Table 2.21 : IFC_1210 SPI Flash EPROM

Warning *Due to their Flash EPROM technology, the SPI device programming can take several seconds, mainly related to the erase process.*

Note *Software utilities are supplied for SPI device programming.*

The two following table sum up the SPI Flash EPROM mapping allocation.

SPI#1 Mapping	SPI#1 Content	Comments
0xFE'0000 -0xFF'FFFF	"IO" FPGA Signature #3	Programming file generated by the MCS2BIN utility include the FPGA signature
0xE0'0000 -0xFD'FFFF	"IO" FPGA Bit-stream #3	
0xDE'0000 -0xDF'FFFF	"IO" FPGA Signature #1	
0xC0'0000 -0xCD'FFFF	"IO" FPGA Bit-stream #1	
0xBE'0000 -0xBF'FFFF	"IO" FPGA Signature #1	
0xA0'0000 -0xBD'FFFF	"IO" FPGA Bit-stream #1	
0x9E'0000 -0x9F'FFFF	"IO" FPGA Signature #0	
0x80'0000 -0x9D'FFFF	"IO" FPGA Bit-stream #0	
0x70'0000 -0x7F'FFFF	PONFSM Microcode #3	PON_FSM Microcode. If SW2-6 is "ON", PONFSM_Mode = '1' only 1st PON_FSM Microcode (unified) is activated.
0x60'0000 -0x6F'FFFF	PONFSM Microcode #2	
0x50'0000 -0x5F'FFFF	PONFSM Microcode #1	
0x40'0000 -0x4F'FFFF	PONFSM Microcode #0	
0x20'0000 -0x3F'FFFF	IFC_1210 Board Signature	Contents to be defined
0x1F'0000 -0x1F'FFFF	"PON" FPGA Signature	Single image for "PON" FPGA. Can be updated with the iMPACT tool
0x00'0000 -0x17'FFFF	"PON" FPGA Bit-stream 12	

Table 2.22 : IFC_1210 SPI#1 Mapping content

SPI#2/3 Mapping	SPI#2/3 Content	Comments
0xFE'0000 -0xFF'FFFF	"CENTRAL" FPGA Signature #3	Programming file generated by the MCS2BIN utility include the FPGA signature
0xC0'0000 -0xFD'FFFF	"CENTRAL" FPGA Bit-stream #3	
0xBE'0000 -0xBF'FFFF	"CENTRAL" FPGA Signature #1	
0x80'0000 -0xBD'FFFF	"CENTRAL" FPGA Bit-stream #1	
0x7E'0000 -0x7F'FFFF	"CENTRAL" FPGA Signature #1	
0x40'0000 -0x7D'FFFF	"CENTRAL" FPGA Bit-stream #1	
0x3E'0000 -0x3F'FFFF	"CENTRAL" FPGA Signature #0	
0x00'0000 -0x3D'FFFF	"CENTRAL" FPGA Bit-stream #0	

Table 2.23 : IFC_1210 SPI#2-3 Mapping content

2.12.5 Remote SPI Control Register

An embedded SPI Master controller, located in the PCIE_EP Agent_SW provides following facilities :

- Read / Write(program) the three on-board SPI Flash_EPROM devices.
- Issue remote configuration command for the FPGA Configuration Controller located in the companion Spartan_6 FPGA

For SPI controller description refer to the “Tosca2_AgentSW_PCIe_EP_UG” document.

2.12.6 VME64x Support

The “PON” FPGA Spartan-6 controls the non time-critical LVTTL VME64x signals, primary to reduce the IO pin count of the “CENTRAL” FPGA Virtex-6T. Refer to chapter 2.19

2.13 "CENTRAL" FPGA Virtex_6

The "CENTRAL" FPGA is implemented with a high performance XILINX Virtex-6T device packaged in FFG1156 pins (31x31 array). The IFC_1210 is ready to be populated with a wide selection of Virtex-6T device. Consult IOxOS Technologies for FPGA type availability.

To support this wide selection, the on-board power supplies 1.0[V] and 1.5[V] are built with high current capable DCDC Ericsson BMR463 (up to 20[A])

Following table sums-up the possible selection. Complementary information are available in the XILINX DS150 data-sheet.

Type	LUT array	BRAM 36 (Kb)	Comments
XC6VLX130T	128'000	264	Default IFC_1210
XC6VLX195T	199'680	344	Consult IOxOS Technologies
XC6VLX240T	241'152	416	Consult IOxOS Technologies
XC6VLX365T	364'032	416	Consult IOxOS Technologies
XC6VSX315T	314'880	704	Consult IOxOS Technologies
XC6VSX475T	476'160	1064	Consult IOxOS Technologies

Table 2.24 : "CENTRAL" Virtex-6 FPGA selection

The FMC#2 signalling is attributed to the IO_Bank_12/13 and IO_Bank_22/23 with local clocking assigned to support multi banks IO clocks. The FMC#2 signalling is attributed to the IO_Bank_15/16 and IO_Bank_25/26. The IO_Bank 12,13,14 15,16, 22, 23, 24, 25 and 26 are all powered with VADJ 1.5[V] → 2.5[V]. (also common with both FMC)

The general facilities as “PON” FPGA interconnect and clock references are attributed to IO_Bank_24 and IO_Bank_34.

The high-speed interconnect with the “IO” FPGA is attributed to IO_Bank_14, VCC_IO powered with VADJ 1.5[V] → 2.5[V].

The DDR3 devices assigned to the TOSCA II SMEM Agent_SW are attributed to IO_Bank_35 and IO_Bank_36, with VCC_IO powered with 1.5[V]. Refer to section 4.4

The VME64x electrical interface is connected to the IO_Bank_32, IO_Bank_33 and IO_Bank_34 with VCC_IO powered with 2.6[V]. Intermediate CMOS level shifter are used to interface with the VME64x LVTTL transceiver powered with 3.3[V].

The VME P0 GPIO[11:0] is directly connected to the IO_Bank_32 and IO_Bank_33 with VCC_IO powered with 2.6[V]. If these signals are interfaced with LVTTL drivers, an intermediate CMOS level shifter shall be used externally (V_{IH} max < 2.6[V])

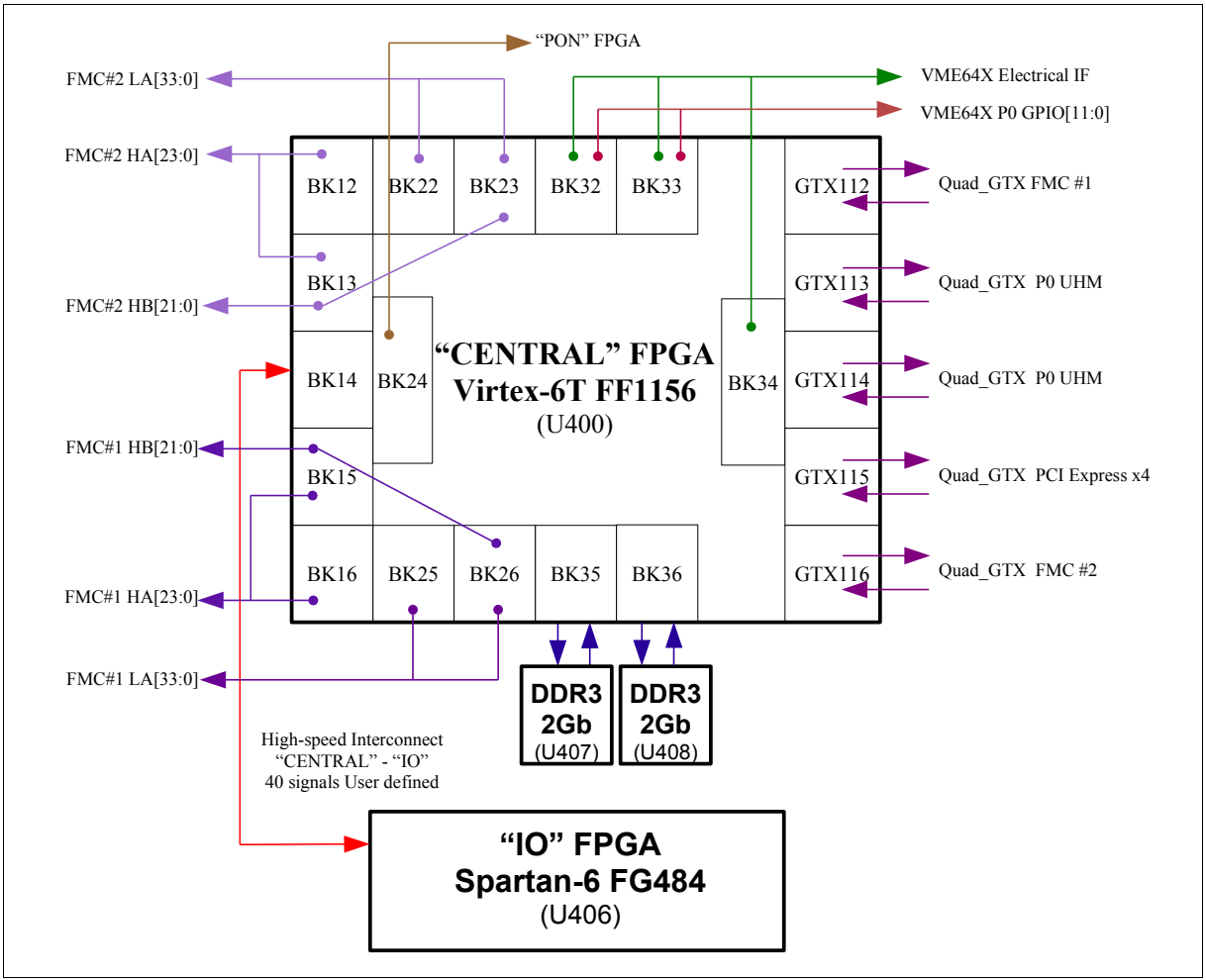

Illustration 18 : IFC_1210 "CENTRAL" FPGA Implementation

Bank_IO	VCC_IO	VRN/P	Max_IO	Description	
12	VADJ		40	FMC#2	
13	VADJ		40	FMC#2	
14	VADJ	VADJ	38	"IO" FPGA HS Interface	
15	VADJ		40	FMC#1	
16	VADJ		40	FMC#1	
22	VADJ		40	FMC#2	
23	VADJ		40	FMC#2	
24	VADJ	VADJ	38	FMC Clocks + "PON" FPGA Interface	
25	VADJ		40	FMC#2	
26	VADJ		40	FMC#2	
32	2V6		40	VME Interface + P0 GPIO[11:0]	
33	2V6	2V6	38	VME Interface + P0 GPIO[11:0]	

34	2V6		40	VME Interface + Divers	
35	1V5	1V5	38	DDR3 Control + General Clock	
36	1V5		40	DDR3 Data Port + DQS	

Table 2.25 : IFC_1210 "IO" FPGA IO_Bank Assignation

2.13.1 Interconnection "CENTRAL" ↔ "IO"

Refer to chapter 2.14.2

2.13.2 Global Clock "CENTRAL"

The "CENTRAL" FPGA " MMCM clocking inputs are assigned as follow.

Virtex-6T IO	pin		Comments
GC_25a	H28, H29	Not used	Not available because used for FMC#1 LA[3]
GC_25b	B31, A31	Not used	Not available because used for FMC#1 LA[7]
GC_24a	L23, M22	fmc1_CLK_M2C(0)	Primary FMC#1/2 Mezzanine to Carrier Clock. Compensated IBUFG within the MMCM.
GC_24b	K24, K23	fmc2_CLK_M2C(0)	
MRCC_24a	J25, J24	fmc1_CLK_M2C(1)	Secondary FMC#1/2 Mezzanine to Carrier Clock. Non compensated BUFR within the MMCM.
MRCC_24b	U23, V23	fmc2_CLK_M2C(1)	
GC_34a	J9, H9	CLK100_REF	IFC_1210 100 MHz reference clock
GC_34b	A10, B10	PGMCLK_REF	IDT8N4Q001 Programmable XO
GC_35a	K13, K12	Not used	Not available because used for ddr_bk12_A3,A5
GC_35b	D11, E11	Not used	Not available because used for ddr_bk12_A1,A10

Table 2.26 : IFC_1210 "CENTRAL" Virtex-6 FPGA Clock Assignment

2.13.3 GTX (MGT) Clocking "CENTRAL"

The QTX (Quad) clocking (MGTREFCLK) are assigned as follow on the IFC_1210. Internally, each MGT Quad can select its clock reference from eight source as :

- Directly from its assigned CLKREF0 and CLKREF1
- From the above MGT CLKREF0 and CLKREF1 (North)
- From the bellow MGT CLKREF0 and CLKREF1 (South)

MGT Quad_#	CLKREF_0	CLKREF_1	Assignment
MGT Quad_112	GBTCLK0_M2C	PGM_CLKREF	FMC#2 multi-gigabit Interface
MGT Quad_113	CLK100_REF	GTX_113_RxCLK	P0 Gigabit Interface #1
MGT Quad_114	TBD	GTX_114_RxCLK	P0 Gigabit Interface #2
MGT Quad_115	CLK100_REF	PGM_CLKREF	PCI Express EP FPFA
MGT Quad_116	GBTCLK0_M2C	TBD	FMC#1 multi-gigabit Interface

Table 2.27 : IFC_1210 "CENTRAL" Virtex-6 FPGA GTX Clock Reference

2.13.4 PCI Express EP IP core

The IFC_1210 PCI Express EP IPcore is built on top of on XILINX Version 2.3

- "v6_pcie_ep_v2_3"

The VHDL source "axi_basic_rx_pipeline.vhd" has been modified/patched according XILINX AR 40866.

At power-up, the IPcore is reconfigured to full-fill the IOxOS configurable parameters. This IPcore reconfiguration is handled through its Management Interface Port (Refer to XILINX UG671) The reconfiguration FSM is located in the VHDL source file "tosca2_tcsr_pcieepg2.vhd". (block:lpcie_mgt)

Following IPV_1210 IPcore parameters is updated :

- BAR_0 / BAR_1 Prefetchable MEMORY → Mask Width, A32/A64, Enable/Disable
- BAR_2 Non-Prefetchable MEMORY → Mask Width
- BAR_3 Non-Prefetchable MEMORY → Enable/Disable
- BAR_3 IO → Mask Width

2.14 "IO" FPGA Spartan_6

The “IO” FPGA (U406) Spartan-6 (XC6SLX45 FG484 pins device) is dedicated to the VME P2 User IO andPPMC#1 User IO interconnection management. This programmable device allows user to define its own mapping interconnect between following IO infrastructure :

- PMC#1 (Jn14) User IO (64)
- VME64x (P2) Row_A(32) and Row_C(32)
- VME64x (P2) Row_D(30) and Row_Z(16)
- High-speed user defined interconnection with the “CENTRAL” FPGA

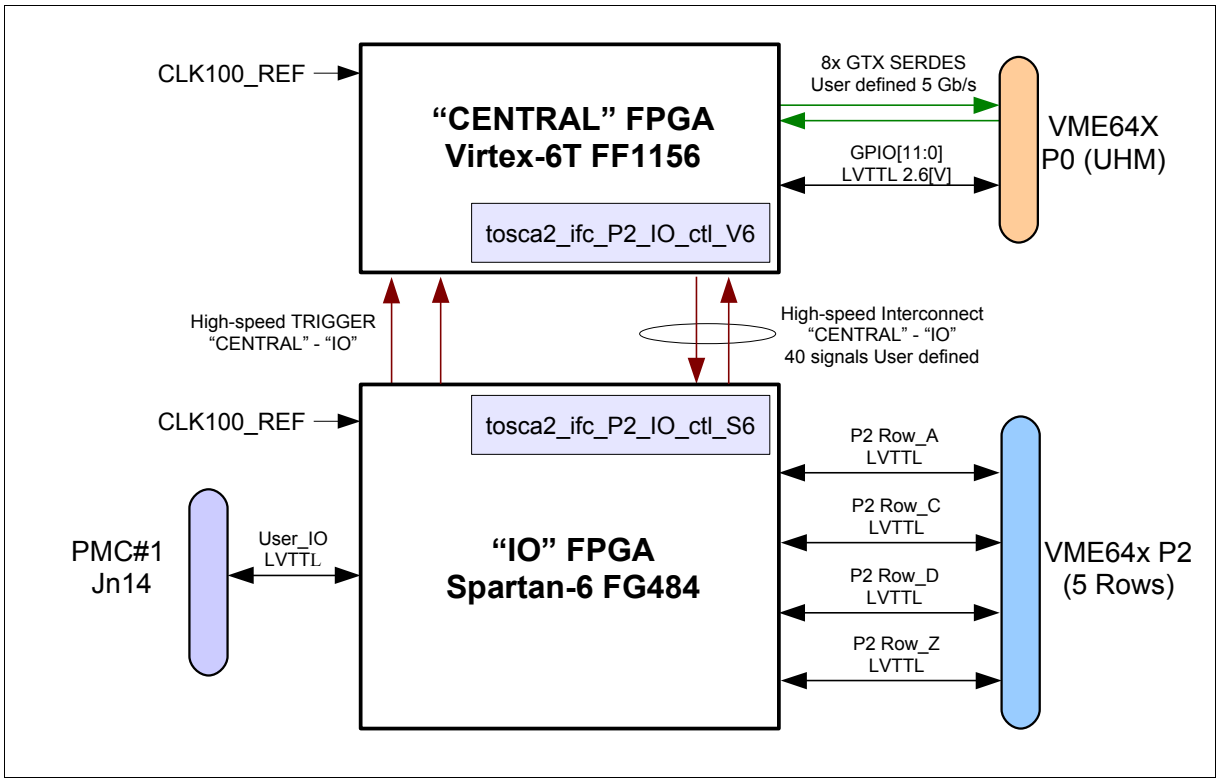

Illustration 19 : IFC_1210 “IO” FPGA Implementation

The PMC#2 Jn24 User's IO are interfaced with 3.3[V] LVTTL compatible level.

The VME P2 (Row_A, Row_C, Row_D and Row_Z) are interfaced with 3.3[V] LVTTL compatible level.

The Spartan-6 FPGA devices support LVTTL/LVCMOS33 driving up to 24[mA]. Additional driving options are available to optimize the electrical interface to P2. (SLEW, DRIVE, PULLUP, …)

The Spartan-6 IO are IO tolerant up to 4.1[V] (DC)

2.14.1 “IO” FPGA IO_Bank Assignation

Following table sums up “IO” FPGA (U406) Spartan-6 IO_Bank attribution

- IO_Bank_0 used for high-speed interface with VCC_IO = VADJ

- IO_Bank_0 requires a VREF_0 = VADJ:2[V]
- IO_Bank_2 used for configuration → ! 3.3[V] interface

Bank_IO	VCC_IO	Max_IO		Comments
0	VADJ 1.5-2.5[V]	46	• Virtex-6 HSI Interconnect • Fast TRIGGER	Need a VREF_0 = VCC_IO/2
1	3.3[V]	64	• VME P2 Top section • A[1:16], C[1:16], D[1:16], Z[1:8] • RESET	
2	3.3[V]	80	• PMC User's IO • Configuration Interface • General LVDS33 Clocking	Bank_IO_2 also used for FPGA device configuration.
3	3.3[V]	64	• VME P2 Bottom section • A[17:32], C[17:32], D[17:32], Z[9:16]	

Table 2.28 : IFC_1210 "IO" FPGA IO_Bank Assignation

2.14.2 Interconnection "CENTRAL" ↔ "IO"

To support IO communication between the "CENTRAL" FPGA and the VME64x P2, and PMC#1 Jn14, a high-speed interface is assigned for this function. This interface is defined with following key topics

- VADJ 2.5[V]-1.5[V] VCC_IO (Support for unipolar and differential) with VREF assigned for high-speed unipolar signalling.
- Bidirectional Source Synchronous Interface
- Ready for ISERDES/OSERDES on both side (Spartan-6 and Virtex-6T)
- Fast TRIGGER signal ("IO" → "CENTRAL")
- Dedicated IO_Bank (Spartan-6 and Virtex-6T)
- DCI support on Virtex-6T IO_Bank

Thirty eight (38) signals, all located in the same IO_Bank are dedicated to this high speed interface . Following table sums up the signal assignment.

Signal Name	"CENTRAL"	"IO"	
pad_HSI_CFG[1:0]	OUT	IN	Single ended Remote Configuration selection. This two bit field allows to select the "IO" FPGA operating mode.
pad_HSI_V2S_MODE[1:0]	OUT	IN	Single ended communication synchronisation.
pad_HSI_V2S_CLKp pad_HSI_V2S_CLKn	OUT	IN	Differential source synchronous clock "CENTRAL"→ "IO" data path.
pad_HSI_V2S_DAT	OUT	IN	Single ended CENTRAL"→ "IO" data path.
pad_HSI_S2V_CLKp pad_HSI_S2V_CLKn	IN	OUT	Differential source synchronous clock for "IO" → "CENTRAL" data path.
pad_HSI_S2V_DAT[15:0]	IN	OUT	Single ended "IO" → "CENTRAL" data path.

Table 2.29 : IFC_1210 "IO" ↔ "CENTRAL" FPGA Interconnect

Note *Refer to .UCF files for "IO" and "CENTRAL" FPGA pin assignment.*

Time multiplexing are used for data communication between the two FPGA

- 8:1 for "CENTRAL" → "IO" FPGA
- 4:1 for "IO" → "CENTRAL" FPGA

Note *The default implementation is running with a conservative 31.5 MHz (125 MHz : 4) "pad_HSI_V2S_CLKp" reference clock, (→8[ns] per data with SERDES 4:1) Higher frequency implementaion is supported up to 50 MHz. (→5[ns] per data with SERDES)*

Default controllers for each FPGA (Spartan-6 and Virtex-6T), are supplied in VHDL format, providing full control of the User IO resources on VME64x P2, and PMC#1 Jn14 from the TOSCA II infrastructure located in the "CENTRAL" FPGA. These two source files are available in the TOSCA II distribution folder.

- "tosca2_ifc_suser_P2_IO_ctl_V6.vhd"
- "tosca2_ifc_suser_P2_IO_ctl_S6.vhd"

2.14.3 Default Implementation

The IFC_1210 implements a default "IO" FPGA with support to exercize its User IO capabilility (VME P2 rows A, C, D Z and PMC#1 Jn24. This "IO" FPGA basic implementation is supplied in the VHDL source files :

- "ifc1210_top_IO_a0.vhd"
- "ifc1210_top_IO_a0.ucf"

In the "CENTRAL" FPGA, the USER#1 Agent_SW block is implemented with specific resources (control and status registers) allowing to control the IFC_1210 User IO capabilility. Following VHDL source files are used to support this functionality :

- "tosca2_ifc_suser_ex2b_agsw.vhd"
- "tosca2_ifc_suser_tcsr.vhd"
- "tosca2_ifc_suser_tmem.vhd"
- "tosca2_ifc_suser_P2_IO_V6.vhd"

Following resources dedicated to control the"IO" FPGA are provided in the USER#1 Agent_SW block. All these resources are mapped over the TOSCA II IO_Bus infrastructure. Following table sum-up the resources dedicated for

IO_Bus	Resource		Description
0x1000	Register_00	R	32-bit Read only = X"12345678"
0x1004	Register_01	RW	32-bit Read/Write 32-bit register

0x1008	Register_02	RW	16-bit Interrupt Mode (Edge or Level) "suser_INT_MOD[15:0]"	
0x100C	Register_03	RW	16-bit Interrupt Request "suser_INT_REQ[15:0]"	
0x1010	Register_04	RW	32-bit VME_P2_row_A Input	
0x1014	Register_05	RW	32-bit VME_P2_row_A Output	
0x1018	Register_06	RW	32-bit VME_P2_row_A Direction ('1' = OUTPUT, '0' = INPUT)	
0x101C	Register_07	RW	32-bit VME_P2_row_C Input	
0x1020	Register_08	RW	32-bit VME_P2_row_C Output	
0x1024	Register_09	RW	32-bit VME_P2_row_C Direction ('1' = OUTPUT, '0' = INPUT)	
0x1028	Register_0A	RW	32-bit VME_P2_row_D Input	
0x102C	Register_0B	RW	32-bit VME_P2_row_D Output	
0x1030	Register_0C	RW	32-bit VME_P2_row_D Direction ('1' = OUTPUT, '0' = INPUT)	
0x1034	Register_0D	RW	16-bit VME_P2_row_Z Input	
0x1038	Register_0E	RW	16-bit VME_P2_row_Z Output	
0x103C	Register_0F	RW	16-bit VME_P2_row_Z Direction ('1' = OUTPUT, '0' = INPUT)	
	....	RW	Resources used for FMC#1 control. Refer to section.	
0x1080	Register_20	RW	ITC16 IACK	TOSCA II Interrupt Controller. These four(4) locations are used to support Interrupt handling of the User Agent_SW.
0x1084	Register_21	RW	ITC16 CSR	
0x1088	Register_22	RW	ITC_IMC	
0x108C	Register_23	RW	ITC_IMS	
0x1090	Register_24	RW	High Speed VME P2 SERDES Control & Status Register. "CENTRAL" FPGA ↔ "IO" FPGA High speed link management	

Table 2.30 : IFC_1210 "IO" ↔ "CENTRAL" Control Resources

Note *The Register_XX bit assignment is made with its natural numbering. i.e bit<0> -> P2_row_A_IN[1].*

2.14.3.1 VME P2 SERDES CSR Register

The Register_24 resource, mapped at IO_Bus 0x1090 control the "CENTRAL" ↔ "IO" FPGA interconnection.

VME_P2_CSR IO_Bus : 0x1090-1093				VME P2 SERDES Control CSR	
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[1:0]	P2_MODE[1:0]	RW	00	FPGA "CENTRAL" Virtex-6T → FPGA "IO" Spartan-6 synchronisation control. This 2-bit field allows to set-up dynamically the SERDES connections . **P2_Mode[1:0]** | 00 | RESET State. The Inter-connect is not operational 01 | Enable Virtex-6 → Spartan-6 SERDES connection. 10 | Enable Spartan-6 → Virtex-6 SERDES connection.	

VME_P2_CSR IO_Bus : 0x1090-1093				VME P2 SERDES Control CSR	
				11 — Enable Spartan-6 → Virtex-6 SERDES connection. The Virtex-6 – Spartan-6 synchronisation mechanism shall be handled sequentially with : • "00" →" 01" → "10"/"11" While P2_MODE[1:0] = 10/11, the status field P2_Link_FSMSTA[1:0] provides the current Virtex-6 - Spartan-6 operation.	
[3:2]	IO_CFG[1:0]	RW	00	This two bit field select the "IO" FPGA Configuration IO_CFG[1:0]: 00 — VME P2 Row AC remote control; 01 — VME P2 Row AC PMC#1 Jn14 control; 10 — PMC#1 Jn14 control remote control; 11 — USER defiined	
[7:4]	SWITCH_C[4:1]	R	0x0	Status SWITCH_C	
[11:8]	Remote_STA[3:0]	R	X'0'	Remote Status_ID	
[13:12]	Reserved	R	00	Not implemented	
[15:14]	P2_Link_FSMSTA	R	"00"	This 2-bit field reflects the current state of the FSM managing the interconnection between the central Virtex-6 FPGA and the remote Spartan-6 FPGA "IO". FSMSTA[1:0]: 00 — RESET State. The Inter-connect is not operational; 01 — PLL locking and remote FPGA acknowledge protocol is in in progress; 10 — P2 Link interconnect is operational; 11 — P2 Link interconnect detects a protocol error. The Inter-connect is not operational.	
[23:16]	Reserved		X'00'	Not used	
[27:24]	P2_IO_SeqID	R	X'0'	This 4-bit field reflect the 4-bit binary counter embedded in the inter FPGA link. Value is incremented at every de-mux state	
[29:28]	Reserved	R	"00"	Not used	
[30]	P2_MMCM_Locked	R	'0'	Local PLL MMCM is locked.	
[31]	P2_IO_Ready	R	'0'	Remote Spartan-6 FPGA "IO" link status Ready. While set, the remote Spartan6 FPGA is ready.	

Table 2.31.: VME_P2 SERDES CSR Register

2.14.3.2 "IO" FPGA Configuration Mode

The default "IO" FPGA provides three basic configuration schema, selected with the control signal "`pad_HSI_CFG[1:0]`" driven by the "CENTRAL" FPGA. These three mode of operation are operating as follow :

CFG = "00" : VME P2 IO ↔ "CENTRAL" FPGA
The VME P2 rows A, C, D and Z can be defined as INPUT or OUTPUT and fully controlled from the "CENTRAL" FPGA FPGA.

CFG = "01" : VME P2 A-C ↔ PMC Jn14
The PMC#1 Jn24 IO can be connected to the VME P2 rows A, C. The signal direction can be controlled from the "CENTRAL" FPGA FPGA. The VME P2 rows D and Z can be defined as INPUT or OUTPUT and fully controlled from the "CENTRAL" FPGA FPGA.

CFG = "10" : PMC Jn14 ↔ "CENTRAL" FPGA
The PMC#1 Jn24 IO can be defined as INPUT or OUTPUT and fully controlled from the "CENTRAL" FPGA FPGA. The VME P2 rows D and Z can be defined as INPUT or OUTPUT and fully controlled from the "CENTRAL" FPGA.

CFG = "11" : USER Defined
This configuration is not implemented by default and left available for application specific. The selection can be refurbished by modifiing the VHDL source "`ifc1210_top_IO_a0.vhd`".

Following table provides the resource allocation for each ogf the configuraion selected.

Register#	CFG = "00"	CFG = "01"	CFG = "10"
Register_04	VME_P2_row_AIN[32:1]	Jn14_EVEN_IN[64:2]	Jn14_EVEN_IN[64:2]
Register_05	VME_P2_row_AOUT[32:1]	Jn14_EVEN_DIR[64:2]	Jn14_EVEN_OUT[64:2]
Register_06	VME_P2_row_ADIR[32:1]	VME_P2_row_ADIR[32:1]	Jn14_EVEN_DIR[64:2]
Register_07	VME_P2_row_CIN[32:1.]	Jn14_ODD_IN[63:1]	Jn14_ODD_IN[63:1]
Register_08	VME_P2_row_COUT[32:1]	Jn14_ODD_DIR[63:1]	Jn14_ODD_OUT[63:1]
Register_09	VME_P2_row_CDIR[32:1]	VME_P2_row_CDIR[32:1]	Jn14_ODD_DIR[63:1]
Register_0A	VME_P2_row_DIN[30:1]	VME_P2_row_DIN[30:1]	VME_P2_row_DIN[30:1]
Register_0B	VME_P2_row_DOUT[30:1]	VME_P2_row_DOUT[30:1]	VME_P2_row_DOUT[30:1]
Register_0C	VME_P2_row_DDIR[30:1]	VME_P2_row_DDIR[30:1]	VME_P2_row_DDIR[30:1]
Register_0D	VME_P2_row_ZIN[16:1]	VME_P2_row_ZIN[16:1]	VME_P2_row_ZIN[16:1]
Register_0E	VME_P2_row_ZOUT[16:1]	VME_P2_row_ZOUT[16:1]	VME_P2_row_ZOUT[16:1]
Register_0F	VME_P2_row_DIR[16:1]	VME_P2_row_DIR[16:1]	VME_P2_row_DIR[16:1]
Note *xxxDIR : '1' = OUTPUT, '0' = INPUT* ***Note*** *xxxEVEN = 2,4,6, ...62, 64, xxxODD = 1,3,5, ... 61, 63*			

Table 2.32 : IFC_1210 "IO" FPFA Configuration resources allocation

Warning The IFC_1210 VME P2 pins A31, C28, C30, D28, D30 and C31, can be assigned with static jumpers J1- J14 to supply power supplies (+3.3[V], +12[V] and -12[V] to the VME Rear_IO. These static options are provided for backward compatibility. Refer to chapter 2.3.6 "Rear_IO Power Supplies".

2.15 DDR3 Shared Memory

The IFC_1210 implements two(2) DDR3 devices (U407, U408), directly connected to the Virtex-6 "CENTRAL" FPGA. These two memory devices are organized in x16 and managed by specific TOSCA II IP core as independent memory array. The TOSCA II updated IP core is optimized for DDR3 and also integrates tightly coupled DMA controllers, optimized for DDR3 transactions.

The DDR3 SDRAM memory device is an improved version of DDR2 with 1.5[V] power supply.

The two DDR3 devices are connected to the FPGA in such way that the SDRAM array can be controlled by TOSCA II SMEM-IDMA as :

- Dual independent Memory blocks running at 200 MHz (2x 1.6 GBytes/s burst rate).

2.15.1 DDR3 Clocking Support

Following drawing shows the DDR3 clocking infrastructure. The IFC_1210 implements a DDR3 controller running at 400 MHz (DDR800). To achieve operation at this frequency a dedicated MMCM is dedicated for this purpose.

- DDR3 Memory Write are issued synchronous with the internal clock reference
- DDR3 Memory Read are issued synchronous with the internal clock reference but data on DQ lines from the DDR3 is catched with the DQS lines.

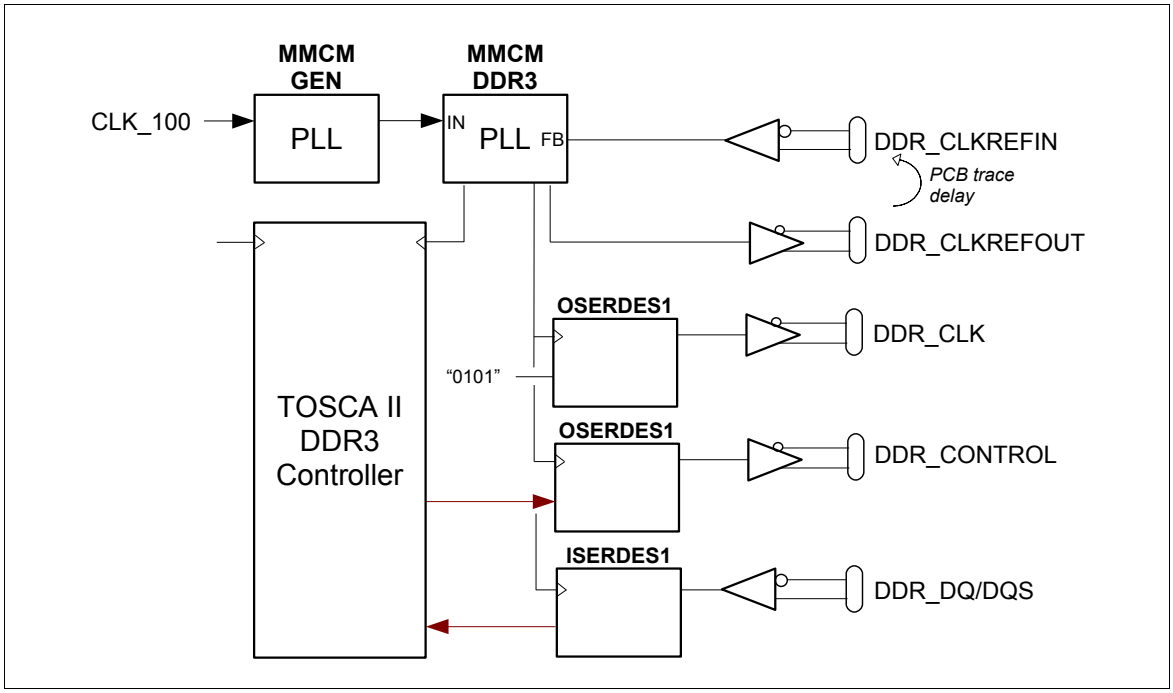

Illustration 20 : IFC_1210 DDR3 Clocking Infrastructure

2.16 IEEE1386.1 PMC

The IFC_1210 provides one IEEE1386.1 PMC site (JN11, JN12, JN14) with PCI 32-bit 33/66MHz interface. The PMC site also supports the VITA32-2003 PrPMC (Processor PMC) signalling.

The PMC PCI Interface is built with a PCI Express PCI bridge PLX Technology PEX8112 (U202) able

to operate in FORWARD or REVERSE mode.

The PEX8112 PCI Express PCI bridge is interfaced through a single PCI Express lane shared with the XMC#1 PCI Express. A high speed (PCI Express GEN2 compatible) 2:1 Mux/DeMux Switch is used for selecting the PCI Express End Point. The selection is made automatically under control of the "xmc1_PRESENTn" side-band signal.

The IEEE1386.1 PMC related control and status information are available in the register "ELB_FMCXMC_CTL" Refer to chapter 4.2.3.4

Following table sums up the IEEE1386.1 PMC side band signalling controlled by the "PON" FPGA.

Signals	Direction	Function	Comments
pci_RESETn	IN	PCI + PEX8112 RESET	Issued under control of the PCI Express – PCI Bridge.
pci_CLKO	IN	PCI + PEX8112 segment clock	33/66 MHz clock driven by the "PON" FPGA
pmc1_MONARCHn	IN	PMC PrPMC	
pmc1_EREADY	OUT	PMC PrPMC	
pmc1_M66EN	OUT	66 MHz Capable	
pmc1_RSTOUTn	OUT	Remote PCI Command	Not supported
pcipcie_FORWARD	IN	PCIE – PCI Bridge PEX_8112 Mode	
pcipcie_BAR0ENB	IN	PCIE – PCI Bridge PEX_8112 Mode	
pcipcie_PERSTn	INOUT	PCIE – PCI Bridge PEX_8112	
pcipcie_PCIRSTn	INOUT	PCIE – PCI Bridge PEX_8112	

Table 2.33 : IFC_1210 PMC IEEE1386.1 Side-band Signalling

Warning While populated, the VITA57.1 FMC HPC carrier connectors (Height = 6.5 [mm]) can be in conflict with the PMC Mezzanine mechanical envelope.

2.16.1 PCI Express PCI Bridge PEX8112

The PLX technology PEX8112 (U202) is a legacy PCI Express x1 - PCI Bridge following the PCISIG specification. The function is fully transparent for the PCI enumeration.

To support VITA32-2003 PrPMC, the PEX8112 can also be configured in FORWARD (PCI Express → PCI) or in REVERSE (PCI → PCI Express) Mode.

- Specific clocking schema f(FORWARD / REVERSE)
- Specific RESET schema f(FORWARD / REVERSE)

2.16.2 PMC User's IO

The IEEE1386.1 PMC JN4 provides 64 User IO. These 64 signals are directly wired to the Spartan-6 "IO" FPGA. This Spartan-6 IO are LVTTL compatible and tolerant up to 4.1[V] (DC)

The IEEE1386.1 PMC JN4 can also be used as User IO for the VITA42.3 XMC#1 Mezzanine.

2.17 XMC VITA42.3

The IFC_1210 provides two VITA42.3-2010 XMC sites. These two Mezzanine site are interfaced with single PCI Express Gen2 x8, dual PCI Express Gen2 x4 or quad PCI Express Gen2 x2. (XMC#2 also support Octal PCI Express Gen2 x1). The PCI Express 'Number of ports' is selectable in the IDT PES32NT24AG2 Switch.

Two PCI Express Port on each VITA42.3-2010 XMC site can be defined in Non Transparent (NT) mode and one PES32NT24AG2 embedded DMA can be assigned on each VITA42.3-2010 XMC site.

The two VITA42.3-2010 XMC site supports side-band signalling as :

- SMBus controlled by the TOSCA II I2C Master Controller or directly with the ELB mapped I2C Master Controller. Refer to chapter 4.2.6
- PCI Express specific ROOTn and WAKEn
- PRESENTn and MBISTn status
- RESET control MRSTIn, MRSTOn

The VITA42.3-2010 XMC related control and status informations are available in the register “ELB_FMCXMC_CTL” Refer to chapter 4.2.3.4

In complement to the above VITA42.3 standards signals, additional facilities has been added on the Reserved IO

- Two independent Rx REFCLK 100 MHz x2 (for non-common clock mode) wired to the PCLKn PES32NT24AG2
- SPARE[3:2] wired to the “PON” FPGA supporting “PCI Express External Cabling” side band signalling.

Following table sums up the XMC side band signalling

Signals	Direction	Function	Comments
xmc1_PRESENTn xmc2_PRESENTn	OUT	Define when a XMC mezzanine is plugged on the IFC_1210 carrier	Used for PMC#1/XMC#1 selection controlling the PCI Express switch selection.
xmc1_SDA xmc2_SDA	INOUT	SMBus Data	Standard SMBus (I2C) Can be controlled by the TOSCA2 I2C master Controller.
xmc1_SCL xmc2_SCL	IN	SMBus Clock	
xmc1_MRSTIn xmc2_MRSTIn	IN	XMC RESET control. Uses as PCI Express PERSTn	Could be common for both XMC sites
xmc1_MRSTOn xmc2_MRSTOn	OUT	XMC RESET Output. Minimum 10[ms] pulse.	Not supported
xmc1_MBISTn xmc2_MBISTn	OUT	Built-in Self test status	Available in the “PON” FPGA.
xmc12_MVMROn	IN	Non volatile “Write Inhibit”	Common for both mezzanine
xmc1_WAKEn xmc2_WAKEn	OUT	PCI Express “WAKE#”	PCI Express specific
xmc1_ROOTn xmc2_ROOTn	IN	PCI Express mode definition = 0 : End Point (EP) = 1 : Root Complex (RC)	PCI Express specific

xmc1_SPARE2 xmc2_SPARE2	TBD	Reserved for IOxOS PCI Express External Cabling side-band signalling	Serial interface between the XMC logic and the “PON” FPGA.
xmc1_SPARE3 xmc2_SPARE3	TBD		

Table 2.34 : IFC_1210 XMC VITA42.3 side-band signalling

Warning While populated, the FMC HPC carrier connectors (Height = 6.5 [mm]) can be in conflict with the XMC Mezzanine mechanical envelope.

1360

Note Refer to chapter 2.10.6 for PCI Express configuration mode supported on XMC#1 and XMC#2.

2.18 FMC VITA57.1

The IFC_1210 provides two ANSI/VITA57.1-2008(R2010) FMC sites. The FMC IO signals are directly wired to the “CENTRAL” FPGA (XILINX Virtex-6T) and to the “PON” FPGA (XILINX Spartan-6).

These two Mezzanine sites (P400, P401) are dedicated for high-speed analog interface (ADC, TDC, DAC) To reduce noise induced by the carrier board, following precaution have been implemented.

- Ferrite serial isolation on power supplies (L407-L411, L402-L406)
- Ground plane bellow the two FMC sites.

Moreover, The IFC_1210 FMC carrier, provides a full height (10[mm]) envelope for the installed FMC mezzanines (No components are located on the carrier board bellow the FMC mezzanine). This provides enough available height to equip critical components on the FMC mezzanine with adequate heat-sink.

2.18.1 FMC VITA57.1 Power Supplies

The two ANSI/VITA57.1 FMC sites (P400, P401) are powered by the IFC_1210 carrier board. These power supplies implements specific filter (bed ferrite) and isolated GND plane reference.

The VADJ power supply voltage is programmable (1.5[V] – 2.5[V]) in the DCDC BMR463 (U707) and effective connection to each FMC is isolated with two FET switch (Q702, Q703) gated with control bits “FMC12_VADJ_ENA“ located in the register “ELB_FMCXMC_CTL“. Refer to chapter 4.2.3.4.

Following table sums up the VITA FMC power supplies capability.

FMC Signalling	Voltage	Current Max	Comments
3P3V (x4)	3.3[V]	3[A]	Directly supplied by the VME64x backplane power supply through the Hot-Swap Controller MAX5970 (U702) Power monitoring and short circuit protection.
12P0V (x2)	12.0[V]	1[A]	Directly supplied by the VME64x backplane power supply through the electronic fuse NIS5132 (U715) Max durrent can be also limited by the VME64x power supply.
3P3VAUX	3.3[V]		Hard wired with 3V3
VADJ(x4)	1.5[V] → 2.5[V]	4[A]	Power suppliy built with a DCDC BMR463 (U707) Isolation with a FET switch (Q702, Q703) supporting SW ON/OFF. Voltage level is SW programmable in the BMR463
VIO_B_M2C(x2)	User defined	-	Not used by the IFC_1210 Carrier
VREF_A_M2C	User defined	-	Not used by the IFC_1210 Carrier
VREF_B_M2C	User defined	-	Not used by the IFC_1210 Carrier
PG_C2M	LVTTL	-	Carrier Power Good . Control bit available in the register “ELB_FMCXMC_CTL“
PG_M2C	LVTTL	-	Mezzanine Power Good . Status bit available in the register “ELB_FMCXMC_CTL“

Table 2.35 : IFC_1210 VITA57 FMC Power Supplies

2.18.2 FMC VITA57.1 GTP Signalling

The two ANSI/VITA57.1 FMC multi-gigabit interface are interfaced to the “CENTRAL” FPGA Virtex-6T Quad GTX blocks GTX_112 and GTX_114. Only a single Quad GTX block is dedicated for each FMC site, providing x4 native interface :

- FMC#2 (P400 top) site → Quad GTX_112
- FMC#1 (P401 bottom) site → Quad GTX_116

These multi-gigabit interface allows to implements SERDES based communication as XILINX proprietary “Aurora”, PCI Express x4, Serial RapidIO, ...

As defined by the VITA57.1 specification, all AC coupling capacitors shall be located on the FMC Mezzanine, so no AC coupling capacitors are implemented on the Virtex-6T GTX Tx/Rx lanes.

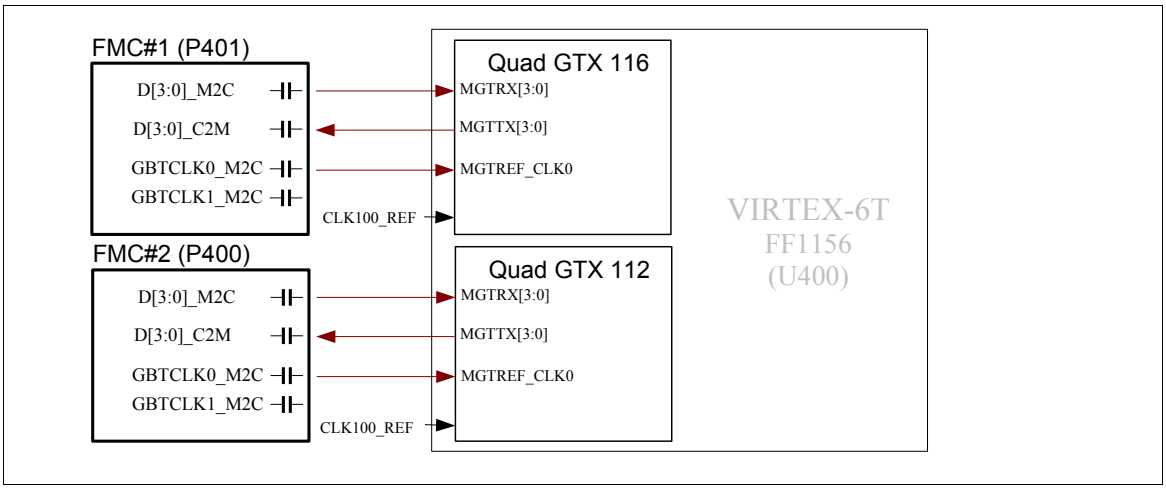

Illustration 21 : IFC_1210 ANSI/VITA57.1 FMC Multi-gigabit Interface with Virtex-6T GTX

The IFC_1210 FMC multi-gigabit clocking schema allows to synchronize the MGT SERDES operation.

- GBTCLK0_M2C is directly connected to the Quad GTX “MGTREFCLK0”
- GBTCLK1_M2C is not used (Left unconnected)

Note *Refer to chapter 2.13.3 for complete Quad GTX clocking schema.*

2.18.3 FMC VITA57.1 Side band signalling

The ANSI/VITA57.1 FMC implements a number of side band signaling, controlled/monitored by the IFC_1210 Carrier through the “PON“ FPGA.

The FMC Geographic addressing signals “GA1“ & “GA0“ are hardwired on the IFC_1210 Carrier as :

- GA1, GA0 = “10“ for FMC#2 (P400 Top)
- GA1, GA0 = “01“ for FMC#1 (P401 Bottom)

The SMBus, implemented with SDC and SDA signals are directly controlled by the IFC_1210 I2C Controller. Refer to chapter 4.2.6. or in TOSCA2 User's guide „Tosca2_AgentSW_PCIe_EP_UG“

chapter 4.2.20.

The FMC status informations as “PRSNT_M2C“ and “PG_M2C“ are connected to the “PON“ FPGA and made available in ELB mapped register ELB_FMCXMC_CTL. Refer to chapter 4.2.3.4

2.18.4 FMC VITA57.1 Clocking Schema

The IFC_1210 implements following clocking support to/from the ANSI/VITA57.1-R2010 FMC sites. Implementation is conditionned by the XILINX Virtex-6T architecture.

For both FMC sites (P400, P401) the C2M clocks are assigned as follow :

- “CLK3_BIDIR” driven by 100 MHz reference clock while CLK_DIR = High, otherwise high impedence (not used)
- “CLK2_BIDIR” driven by a programmable clock supplied by the “Quad frequency Programmable XO“ IDT8N4Q001 REV G while CLK_DIR = High, otherwise high impedence (not used)

The “CLK3_BIDIR” and “CLK2_BIDIR” clock signal are controlled with external LVDS buffer with high impedance capability DS90LV001 (U402, U403, U404, U405) . The high impedance is controlled directly with the “CLK_DIR“ signal supplied by the FMC mezzanine.

The M2C clock signals are connected individually to the “CENTRAL“ FPGA Virtex-6T Global Clock Inputs located in the IO_bank 24.

- FMC#2 CLK0_M2C → IO_Bank 24 _GC
- FMC#2 CLK1_M2C → IO_Bank 24 _MRCC (TBD)
- FMC#1 CLK0_M2C → IO_Bank 24 _GC
- FMC#1 CLK1_M2C → IO_Bank 24 _MRCC (TBD)

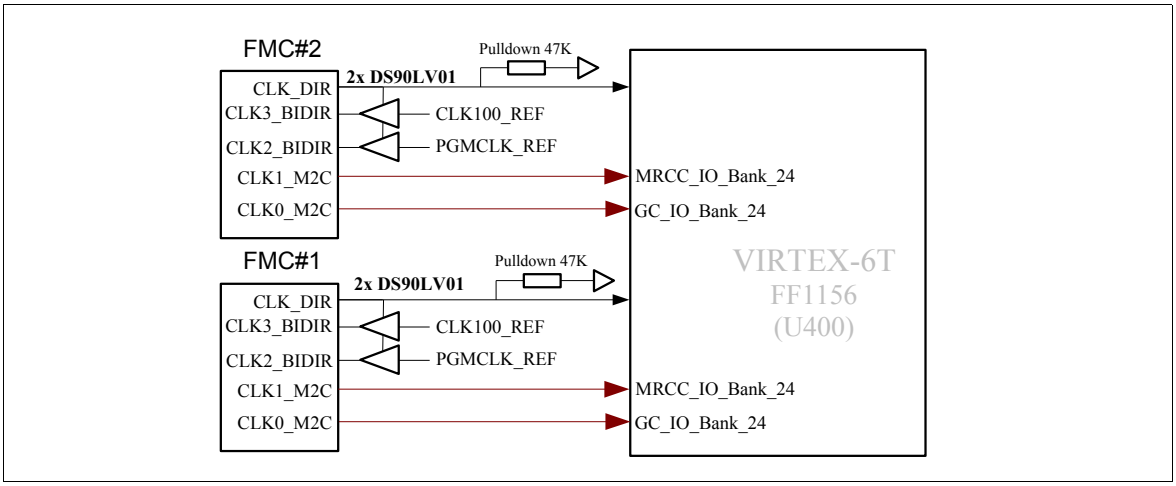

Illustration 22 : IFC_1210 FMC → VITA57.1-2010 Clocking Support

Note *Any FPGA IO connected to LA, HA or HB Interface is able to suppy clock reference to the FMC Mezzanine.*

2.18.5 FMC VITA57.1 → "CENTRAL" FPGA

The following drawing represents the IO connection between the FMC sites and the "CENTRAL" FPGA. The XILINX Virtex-6T provide common clocking support (through MRCC IO type) for adjacent IO_Banks as {15:16}, {25:26}, {13:12} and {23:22}.

The IO Bank assignation of the LA[33:0], HA[23:0] and HB[21:0] FMC signal groups has been selected in such way to optimize the PCB layout and provide maximal flexibility in the FPGA interface.

- IO_Bank {23:22} and {15:16} are assigned as primary for the LA[33:0] group. IO_Banks {23:22} and {15:16} can share common IO clocks resources.
- IO_Bank {12:13} and {25:26} are assigned as primary for the HA[23:0] group. IO_Banks {12:13} and {25:26} can share common IO clocks resources.
- The FMC signals with "_CC" suffix are connected to Virtex-6T MRCC and LRCC IO pins

  LA00, LA17 → MRCC, LA01, LA18 → LRCC

  HA00, HA17 → MRCC, HA01 → LRCC

  HB00, HB17 → MRCC, HB06 → LRCC

  HB00, HB17 → MRCC, HB06 → LRCC

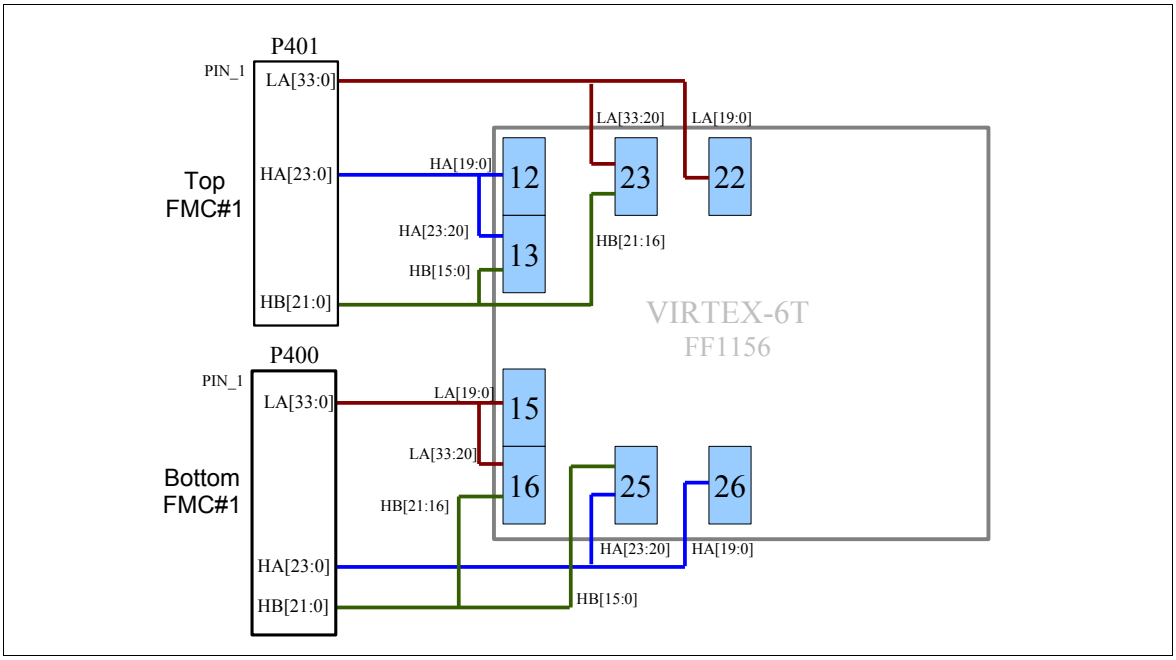

Illustration 23 : IFC_1210 FMC → Virtex-6T/FF1156 IO Bank Assignation

2.18.6 FMC VITA57.1 Electrical Signalling

Following table sums up the FMC electrical interface

FMC#1/#2 Signalling	FPGA	IO_Bank	VCC_IO	Comments
fmcX_LA[19:00] fmcX_LA[33:00]	"CENTRAL"		PGM 1V5 – 1V8 - 2V5	(Note_1)
fmcX_HA[19:00]	"CENTRAL"		PGM	(Note_1)

fmcX_HA[23:20]			1V5 – 1V8 - 2V5	
fmcX_HB[19:00] fmcX_HB[21:20]	"CENTRAL"		PGM1V5 – 1V8 - 2V5	(Note_1)
fmcX_CLK2_BIDIR			2V5(LVDS)	Driven from 100 MHz clock source
fmcX_CLK0_M2C	"CENTRAL"		2V5(LVDS)	Must be connected to Virtex-6 GC pins
fmcX_CLK3_BIDIR			2V5(LVDS)	Driven from IDT8N4Q001 REV G clock source
fmcX_CLK0_M2C	"CENTRAL"		2V5(LVDS)	Connected to Virtex-6 GC pins
fmcX_D[3:0]_M2C	"CENTRAL"		CML AC	Virtex-6T Quad GTX Rx
fmcX_D[3:0]_C2M	"CENTRAL"		CML AC	Virtex-6T Quad GTX Tx
fmcX_GBTCLK0_M2C	"CENTRAL"		CML AC	Virtex-6T Quad GTX CLKREF0
fmcX_GBTCLK1_M2C	"CENTRAL"		CML AC	Not used
fmcX_3P3V	-	-	-	General 3V3 power supply (ferrite isolation)
fmcX_3P3VAUX	-	-	-	General 3V3 power supply (ferrite isolation)
fmcX_12P0V	-	-	-	General 12V0 power supply (ferrite isolation)
fmcX_VADJ	-	-	-	IO signalling Power. Selectable on the IFC_1210 between 1.5[V] → 2.5[V]
fmcX_VREF_A_M2C	-	-	-	Not supported (Note_2)
fmcX_VREF_B_M2C	-	-	-	Not supported (Note_2)
fmcX_VIO_B_M2C	-	-	-	Not used (Note_3)
fmcX_GA[1:0]			LVTTL	Hard-wired to "01" / "10" (FMC#1 / FMC#2)
fmcX_PRSNT_M2C_L	"PON"		LVTTL	Wired to the "PON" Spartan-6
fmcX_PG_C2M	"PON"		LVTTL	Power-up management wired to the "PON" Spartan-6. Pull-down resistor added
fmcX_PG_M2C	"PON"		LVTTL	
fmcX_SCL	"PON"		LVTTL	Wired to the "PON" Spartan-6
fmcX_SDA	"PON"		LVTTL	Wired to the "PON" Spartan-6
fmcX_RES0	"PON"		LVTTL	Wired to the "PON" FPGA Spartan-6
fmcX_TDI fmcX_TDO fmcX_TMS fmcX_TCK fmcX_TRST_L			LVTTL	Reserved, not implemented on IFC_1210

Note_1 *PGM → Selectable 1.5[V] – 1.8[V] – 2.5[V] through programmable*
Note_2 *The FPGA banks assigned in input can not use IO standards requiring an external VREF*
Note_3 *The FPGA banks interfacing the HB signalling do not use*

Table 2.36 : IFC_1210 FMC HPC Electrical Signalling

2.18.7 FMC VITA57.1 Derogations and Limitations

Due to IFC_1210 implementation, following exceptions shall be considered for the FMC Mezzanine utilization :

- The power signal **VIO_B_M2C** supplied by the mezzanine used to fill the "CENTRAL" FPGA corresponding VCC_IO. (limitation on the FPGA pin count) All FPGA IO Bank interfacing the FMC are powered with **VADJ** (programmable from 1.5[V] → 2.5[V].
- The FMC JTAG port are not implemented
- The FMC signals **VREF_A_M2C** and **VREF_A_M2C** are not used. The FPGA inputs do not

support IO standard requiring external voltage reference. The Virtex-6T devices are capable to built internally a VREF derived from the IO_Bank VCC_IO. (= VCC_IO / 2)

2.18.8 FMC VITA57.1 VHDL Examples

A basic VITA57.1 FMC controller interface is supplied in example. This example is instantiated twice (FMC#1, FMC#2) and allows to control the FMC signals.

- "tosca2_ifc_suser_ex2b_agsw.vhd"
- "tosca2_ifc_suser_tcsr.vhd"
- "tosca2_ifc_suser_tmem.vhd"
- "tosca2_ifc_suser_ex2b.vhd"

For optimal PCB layout, the differential polarity (N and P) are inverted on some signals. These signal polarity inversion are defined in the "ifc1210_phy_glb_pkg.vhd".

```
FMC1_LA_POL_1105_0 := B"00_01011011_11100001_11110100_11100000";
FMC1_HA_POL_1105_0 := B"11101000_11100001_01111000";
FMC1_HB_POL_1105_0 := B"000001_10100100_00110100";
FMC2_LA_POL_1105_0 := B"00_11011111_00100001_00001101_11111100";
FMC2_HA_POL_1105_0 := B"01000000_00000000_00100000";
FMC2_HB_POL_1105_0 := B"110001_01100110_00001100";
```

Use of Differential signalling has a strong impact on the FPGA power dissipation., so the use of them shall be limited as far as possible. The Xilinx tool "XPower Analyzer" provides modeling support

2.19 VME64x Electrical Interface

The TOSCA II VME Agent_SW IP core implements the logical protocol with FSMs clocked at 166 MHz. The IP core also integrates fast DPRAM used for intermediate buffering in 2eSST mode of operation.

The Virtex-6 FPGA device does not support natively 3.3[V] electrical interface. To interface with external LVTTL VME ETL transceivers, level translators (TI SN74CB3T3245) based on CMOS switch are intercalate between the Virtex-6 IO and the VME ETL transceivers.

To get optimal margin, VCC_IOBANK dedicated to the VME64x interface (IO Bank 32, 33 and 34) are powered with 2.6[V], directly derived from the internal 3.2[V] used for the VME ETL transceivers.

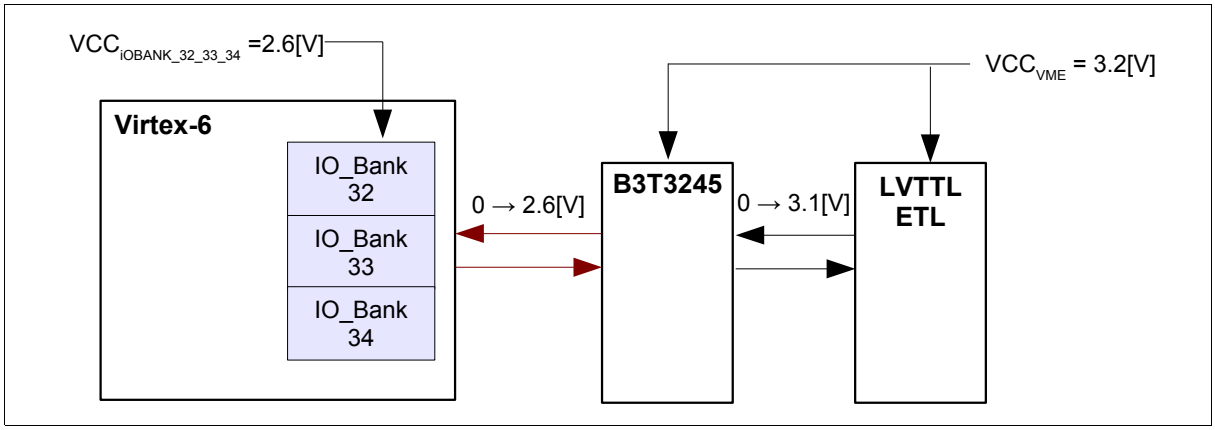

Illustration 24 : IFC_1210 VME64x Electrical Interface

The complete electrical VME64x Interface is supported with following circuitry :

- 10* SN74VMEH22501A VME320 compatible. (U21, U22, U23, U24, U25, U26 U27, U28, U29, U30)
- 5* SN74LVTH125 (U31, U32, U33, U35, U36)

The 2.6[V] level translation is implemented with

- 11* SN74CB3T3245 (U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U34
- Signalling with Spartan-6 "PON"FPGA does not require such level translation. Because this device is natively 4.1[V] tolerant.

2.19.1 VME64x Functions in Spartan-6 "PON" FPGA

A number of VME64x sub-functions are exported to the companion "PON" FPGA Spartan-6. The Spartan-6 devices are LVTTL tolerant and than can interface directly with the VME ETL transceivers.

Two serial interfaces (running at 200 MHz) are used to exchange informations between the Spartan-6 "PON" FPGA and the Virtex-6 "CENTRAL" FPGA.

Following VME signals informations are deported in the FPGA Spartan-6 "MPC_S1AA".

- VME related static options (Jumpers and Hex Rotary Switch)
- VME IRQ[7:1] Management Tx/Rx
- VME Geographic addressing GA[5:0], GAP
- VME side-band signalling as SYSCLK, SYSRESET#, ACFAIL#, SYSFAIL#
- VME Rx_BGIN[3:0]
- VME Tx_BGOUT[3:0]
- VME Rx_BREQ[3:0], Tx_BREQ[3:0]
- VME Rx_SYSFAIL, Tx_SYSFAIL
- VME Rx_BCLR, Tx_ BCLR

2.19.2 VME P2 User's IO Support

To assure backward compatibility with legacy VME64x IO, the IFC_1210 implements a fully compliant LVTTL interface on VME P2. The VME P2 interface is managed by one Spartan-6 XC6SLX45 device (FF484 pins package) named “IO” FPGA.

The IFC_1210 VME P2 connectors can be equipped with 3 or 5 rows connectors

- Row A and C, legacy VME 3 rows → 64 GPIO or VSB Interface
- Row D and Z, VME64x Extension 5 rows → 48 GPIO

2.19.3 VME P0 User's IO Support

The IFC_1210 provides a VME P0 connector based on 3M UHM technology.

The new 3M Ultra Hard Metric UHM connector technology makes possible to use the VME64x P0 legacy connector with high-speed SERDES protocols (PCI Express GEN1/GEN2, Serial RapidIO, USB 3.0 or Custom point to point protocols as AURORA).

The following tables shows how the pin-out organization :

Row	Group Allocation					Comments
	a	b	c	d	e	
1						FPGA Virtex-6 GTX_113 transceivers 1 group of 4 GTX (PCI Express x4, 10G Ethernet, …) 8 differential pairs, up to 7.0 Gb/s + TxCLK / RxCLK
2						
3						
4						
5						FPGA Virtex-6 GTX_114 transceivers 1 group of 4 GTX (PCI Express x4, 10G Ethernet, …) 8 differential pairs, up to 7.0 Gb/s + TxCLK / RxCLK
6						
7						
8						
9						"IO" FPGA 12x GPIO + 3.3[V]/2.5[V] Power supplies
10						
11						
12						IDT PES32NT24AG2 → Port_12 1 PCI Express GEN2 x4 8 differential pairs, up to 7.0 Gb/s + TxCLK / RxCLK
13						
14						
15						
16						IDT PES32NT24AG2 → Port_08 1 PCI Express GEN2 x4 8 differential pairs, up to 7.0 Gb/s + TxCLK / RxCLK
17						
18						
19						

Table 2.37 : IFC_1210 VME UHM P0

- Ten(10) Differential pairs to the IDT PES32NT24AG2 PCI Express x4
- Ten(10) Differential pairs to the IDT PES32NT24AG2 PCI Express x4
- Twenty(20) Differential pairs dedicated to the FPGA GTX Transceivers
- Twelve(12) single ended from "IO" FPGA Spartan-6
- Three(3) power supplies as 3.3[V], 2.5[V] and GND

#	Row_A	Row_B	Row_C	Row_D	Row_E
1	GTX_113_Rx_0P	GTX_113_Rx_1P	GTX_113_RxCLK_P	GTX_113_Tx_0P	GTX_113_Tx_1P
2	GTX_113_Rx_0N	GTX_113_Rx_1N	GTX_113_RxCLK_N	GTX_113_Tx_0N	GTX_113_Tx_1N
3	GTX_113_Rx_2P	GTX_113_Rx_3P	GTX_113_TxCLK_P	GTX_113_Tx_2P	GTX_113_Tx_3P
4	GTX_113_Rx_2N	GTX_113_Rx_3N	GTX_113_TxCLK_N	GTX_113_Tx_2N	GTX_113_Tx_3N
5	GTX_114_Rx_0P	GTX_114_Rx_1P	GTX_114_RxCLK_P	GTX_114_Tx_0P	GTX_114_Tx_1P
6	GTX_114_Rx_0N	GTX_114_Rx_1N	GTX_114_RxCLK_N	GTX_114_Tx_0N	GTX_114_Tx_1N
7	GTX_114_Rx_2P	GTX_114_Rx_3P	GTX_114_TxCLK_P	GTX_114_Tx_2P	GTX_114_Tx_3P
8	GTX_114_Rx_2N	GTX_114_Rx_3N	GTX_114_TxCLK_N	GTX_114_Tx_2N	GTX_114_Tx_3N
9	GPIO_6	GPIO_9	VCC2V5	GPIO_3	GPIO_0
10	GPIO_7	GPIO_10	GND	GPIO_4	GPIO_1
11	GPIO_8	GPIO_11	VCC3V3	GPIO_5	GPIO_2
12	P0_A_Rx_2P	P0_A_Rx_3P	P0_A_TxCLK_P	P0_A_Tx_2P	P0_A_Tx3P
13	P0_A_Rx_2N	P0_A_Rx_3N	P0_A_TxCLK_N	P0_A_Tx_2N	P0_A_Tx_3N
14	P0_A_Rx_0P	P0_A_Rx_1P	P0_A_RxCLK_P	P0_A_Tx_0P	P0_A_Tx_1P
15	P0_A_Rx_0N	P0_A_Rx_1N	P0_A_RxCLK_N	P0_A_Tx_0N	P0_A_Tx_1N
16	P0_B_Rx_2P	P0_B_Rx_3P	P0_B_TxCLK_P	P0_B_Tx_2P	P0_B_Tx_3P
17	P0_B_Rx_2N	P0_B_Rx_3N	P0_B_TxCLK_N	P0_B_Tx_2N	P0_B_Tx_3N
18	P0_B_Rx_0P	P0_B_Rx_1P	P0_B_RxCLK_P	P0_B_Tx_0P	P0_B_Tx_1P
19	P0_B_Rx_0N	P0_B_Rx_1N	P0_B_RxCLK_N	P0_B_Tx_0N	P0_B_Tx_1N
	P0_Input P0_Output				

Table 2.38 : IFC_1210 VME UHM P0 VME64x UHM P0 pin assignment.

Note *GPIO_0 ... GPIO_15 are all routed to the "CENTRAL" FPGA Virtex-6T IO Bank 34*

Warning *GPIO on P0 shall not exceed 2.5V because they are directly connected to Virtex-6T IO Bank 2.5[V].*

The high-speed differential allocated to the "CENTRAL" FPGA Virtex-6 MGT group GTX_113 and GTX114 are AC coupled on the IFC_1210.

The high-speed differential signals connected to the PCI Express switch PES32NT8AG2 / PES32NT24AG2 are AC coupled on the IFC_1210.

2.20 High-Speed GTX

The Virtex-6 "CENTRAL" FPGA implements twenty(20) {only 16 on CXT version} GTX Transceiver running up to 6 Gb/s {3.2 on CXT version). These high speed SerDes interfaces are optimized for modern communication protocols as PCI Express, Serial_RIO, 10G Ethernet, SATA I/II, USB 3.0, …

The five Quad GTX Inteface are allocated as :

- GTX_112 → FMC#2 Gigabit Interface
- GTX_113 → VME P0
- GTX_114 → VME P0
- GTX_115 → PCI Express EP (connected to PES32NT24AG2)
- GTX_116 → FMC#1 Gigabit Interface

2.20.1 GTX Power Supplies

The twenty(20) available GTX transceivers are all powered from two (low noise) LDO regulators (TI TPS74901 (2% accuracy, 25[uV_{RMS})). From this voltage sources, the North and South sections are connected together and powered through ferrite/inductor filter.

GTX Power	V	IMAX	Comments
MGTAVCC_N MGTAVCC_S	1.0[V] 1.0[V]	1.2[A]	U713 LDO TI 74901 from 1.5[V] with V_{BIAS} 5.0[V]
MGTAVTT_N MGTAVTT_S	1.2[V] 1.2[V]	1.2[A]	U714 LDO TI 74901 from 1.5[V] with V_{BIAS} 5.0[V]
MGTAVTTRCAL	1.2[V]	0.1[A]	

Table 2.39 : Virtex-6 GTX Power Supplies

2.20.2 GTX PCI Express LogiCORE

The Virtex-6 "CENTRAL" FPGA, integrates two(2) PCI Express LogiCORE. These Hardware IP cores occupy specific position on the die and therefore the wiring to/from the GTX Transceiver and the IP core can be more/less optimal.

Following table provides PCI Express GTX allocation as suggested by XILINX. Refer to XILINX "Virtex-6 UG517".

PCI Express	Preferred	Alternate	Comments
PCIe Core #1 (X0Y0)	Lane_0 → X0Y7 Lane_1 → X0Y6 Lane_2 → X0Y5 Lane_3 → X0Y4 (Quad_113)	Lane_0 → X0Y3 Lane_1 → X0Y2 Lane_2 → X0Y1 Lane_3 → X0Y0 (Quad_112)	• Quad_112 is wired to MPF Top • Quad_113 is wired to VME64x P0
PCIe Core #2 (X0Y1)	Lane_0 → X0Y11 Lane_1 → X0Y10 Lane_2 → X0Y9 Lane_3 → X0Y8 (Quad_114)	Lane_0 → X0Y15 Lane_1 → X0Y14 Lane_2 → X0Y13 Lane_3 → X0Y12 (Quad_115)	• Quad_115 is wired to VME64x P0 • Quad_114 is wired to MPF Top/Bottom

Table 2.40 : Virtex-6 PCI Express LogiCORE → GTX Allocation

2.21 Others

This section provides technical information on miscellaneous IFC_1210 functions.

2.21.1 FUSE Protections

The VME +12[] and -12[V] power supplies are directly wired to the VITA57.1 FMC connectors. Two fuses on specific holders are implemented to protect the IFC_1210 circuitry against short-circuit or over current.

- -12[V] Fuse Type USF0603 2A/63V (F701)
- +12[V] Fuse Type USF0603 2A/63V (F701)

The +12[V] Fuse can be replaced with an active fuse NIS5132MN1TXG (U715). Consult IOxOS Technologies for availability.

Others on-board IFC_1210 powers supplies are protected against over-current and over-temperature with embedded electronic circuit breaker.

- LI Controller MAX5970 (U701) → VME +3.3[V] and 5.0[V
- DCDC Ericsson BMR453 (U704, U705, U706 and U707) → 1.0[V] , 1.5[V] and VCC_ADJ
- LDO TI TPS74901 (U709, U710, U711, U712, U713 and U714) → Internal 2.6[V], 1.5[V], 1.2[V] MGT and 1.0[V] GTX

2.21.2 XILINX Interface Tool

The IFC_1210 implements a 2[mm] 14-pin connector (P100) dedicated to the XILINX programming/ debugging tool Platform USB II. For full description of this tool refer to XILINX DS593 document.

This connector (P100) is located on bottom of the VME board and used for :

- IFC_1210 FPGA Virtex-6/Spartan-6 XILINX ChipScope PRO tool.
- IFC_1210 FPGA Virtex-6/Spartan-6 Configuration with XILINX iMPACT tool

Signal allocation	TAP P6		Signal allocation
VREF	1	2	GND
SS/TMS	3	4	GND
SCK/TCK	5	6	GND
MISO/TDO	7	8	GND
MOSI/TDI	9	10	GND
NC1	11	12	GND
NC2 (TRSTn)	13	14	GND

Table 2.41 : IFC_1210 XILINX TAP Programming Port P4

The IFC_1210 JTAG chain incorporate only XILINX FPGA/CPLD devices, in following daisy-chain order :

1. Coolrunneer_II = “STATIC“ CPLD
2. Spartan-6 XC6SL45 = “IO“ FPGA
3. Virtex-6 XC6LVX130T = “CENTRAL“ FPGA
4. Spartan-6 XC6SL45 = “PON“ FPGA

To use the P100 connector with the XILINX programming tool Platform USB II to download the FPGA from the XILINX ISE iMPACT tool, the mini-switch SW2-3 shall be “ON”.

While SW2-3 is “ON”, the FPGA are not configured automatically at power-up with a bit-stream stored in the SPI Serial Flash_EPROM, but wait for a configuration bit-stream supplied through the XILINX TAP connector P100 connection

To support remote debugging with Chip-scope_PRO tool, the mini-switch SW2-3 shall be “ON” and the FPGA configuration shall be therefore downloaded with the ISE iMPACT tool.

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2.21.3 PON_FSM Controller

The IFC_1210 incorporates a micro-programmable function named PON_FSM allowing to self initialize the IFC_1210 board without any support from external computing support.

The PON_FSM is an autonomous sequencer involved at power up. If not disable by external static option (DIP switch implementation specific, ...) , This IO_Master controller executes a start-up microcode stored in the SPI Serial Flash EPROM.

An external switch option (SW2-5) allows to select a unified PON_FSM microcode at TBD offset or independent PON_FSM microcode for each of the N possible FPGA bit-stream number.

- Unified PON_FSM microcode → Max 256K instructions
- Independent PON_FSM microcode → Max 64K instructions

Each PON_FSM Instruction is built within a 64-bit word, occupying eight consecutive Bytes in the SPI Serial Flash_EPROM. Each microcode instruction is executed in ~ 5.4 [us].

The PON_FSM execution can be monitored in the status register ILOC_PONFSM located in the PCI Express EP Agent_SW. (Refer to Tosca2_AgentSW_PCIE_UG)

Three basic PON_FSM Instructions are supported as :

1. IOBUS_WRITE, allowing to initiate IO_Bus Write transactions and therefore initialize all IFC_1210 internal resources mapped over the IO_Bus.
2. WAIT, allowing to implements a fixed wait
3. STOP, terminating the FSM_PON execution .

Following table provides the PON_FSM instruction format :

DWORD_1 Instruction Coding			
[31:24]	Instruction Code	8-bit field encoding the Instruction Code. 0x45 = IOBUS_WRITE 0x34 = WAIT 0x22 = STOP Others = ILLEGAL	Only code 0x45, 0x34 and 0x22 are interpreted as valid PON_FSM Instructions. Any other code stops immediately the FSM_PON execution with illegal case.
[23:16]	Instruction Reserved	Not used	
[15:0]	Instruction Extension	16-bit field specifying the Instruction Extension. IO_Bus Address or Wait time in 1[us] step. (up to 65[ms])	The IO_Bus Address is encoded as follow : [1:0] : Not used. [9:2] : IO_Bus Slave resource selection in LWORD. [14:12] : IO_Bus number selection. (0,1,2,3,4,5,6,7) [15] : Reserved fore future extension
DWORD_2 Associated Data			
[31:0]	Instruction Data	32-bit field used to IOBUS_WRITE	Natural 32-bit LWORD format. Not used for WAIT Instruction.

Table 2.42 : PON_FSM Instruction Format

A specific SW environment is provided to built the PON_FSM microcode and to store it in the SPI Serial Flash EPROM associated with concerned FPGA bit-stream.

The PON_FSM controller is conditioned by two static options as

- PONFSM_Enable, Enabling/Disabling PON_FSM at power-up
- PONFSM_Mode, selecting PON_FSM microcode offset in the SPI Flash EPROM #1.

Note *The PON_FSM execution provides status informations in the "ILOC_PONFSM" register.*

3. IFC_1210 FPGA Implementation

3.1 TOSCA II FPGA Architecture

The IFC_1210's FPGA implements a TOSCA II infrastructure in its “CENTRAL” FPGA.

For complete description refer to “Tosca2_Architecture_UG” document.

The TOSCA II architecture approach has been driven by a number of new technology trends

- FPGA devices is becoming bigger and bigger at every new silicon technology, providing capability to integrates complete system in a single FPGA device. Those devices are now available at reasonable cost for high end application. (No more limited to ASIC prototypes) Moreover doe to their structure, new FPGA generation are directly in phase with the silicon technology (today is 40[nm] with migration visibility to 32[nm] (→ 2012) and 22[nm] (→ 2014))
- Wide availability of these new FPGA requires a new design methodology approach with intensive use of 3rd party IP core. These approach is today widely used for the ASIC market but with a cost model not directly applicable. FPGA utilisation is mainly focused on small and medium volume application
- In the past we built system application by assembling chip together or board level product together. Standards interfaces were defined to interconnect the different elements (VME, PCI, ...) Since thirty years this approach have been very successful, allowing to built embedded system with “standard” components. To support system built inside a single FPGA device a functional similar methodology need to be applied.

The standard “Shared Bus Architecture” widely used since years, are all based on Master/Slave interactions. A “Master” read or writes a “Slave” resources, which can be IO registers or/and Memory locations. Several new trends have been introduced as Cache Memory, optimized burst transactions, split transactions with un-compelled request and completion, … but without modifying fundamentally the initial principle. These standard shared Buses have two main inconvenient

- The physical media interconnecting the Masters with the Slaves shall be shared. An arbitration mechanism shall be used to allocate the media to the Masters. This has a direct impact on the Latency and the Bandwidth performance.
- The physical media size (number of pins) is limited in construction. It is difficult to built interfaces with thousands of IO.

The TOSCA II architecture has been defined to support the widely used “Shared Bus Architecture” but with optimal latency and bandwidth performance for implementation in new high performance FPGA. The interconnection between the Masters and the Slaves are no more implemented with a shared media but with a full mesh switch where each Master owns a direct connection to every Slaves. Thanks to this approach we have following advantages.

- Due to point to point connection the bandwidth performance is not shared and can be specifically defined by the Master and the Slave implementation.
- Due to individual connection between the Masters and the Slave, the latency is fully under control of the Slave and no more related to the media sharing.

The TOSCA “Network On Chip” NoC approach is possible by the fact that the targeted FPGA have enough resources (DPRAM and LE) and there is no limitation in the number of connections inside the FPGA routing. The TOSCA II “Network On Chip” NoC elements ("CENTRAL" switch and agents are described in following sub-sections)

3.2 TOSCA II Interconnect Infrastructure

The above diagram represents the IFC_1210 TOSCA II internal interconnect infrastructure.

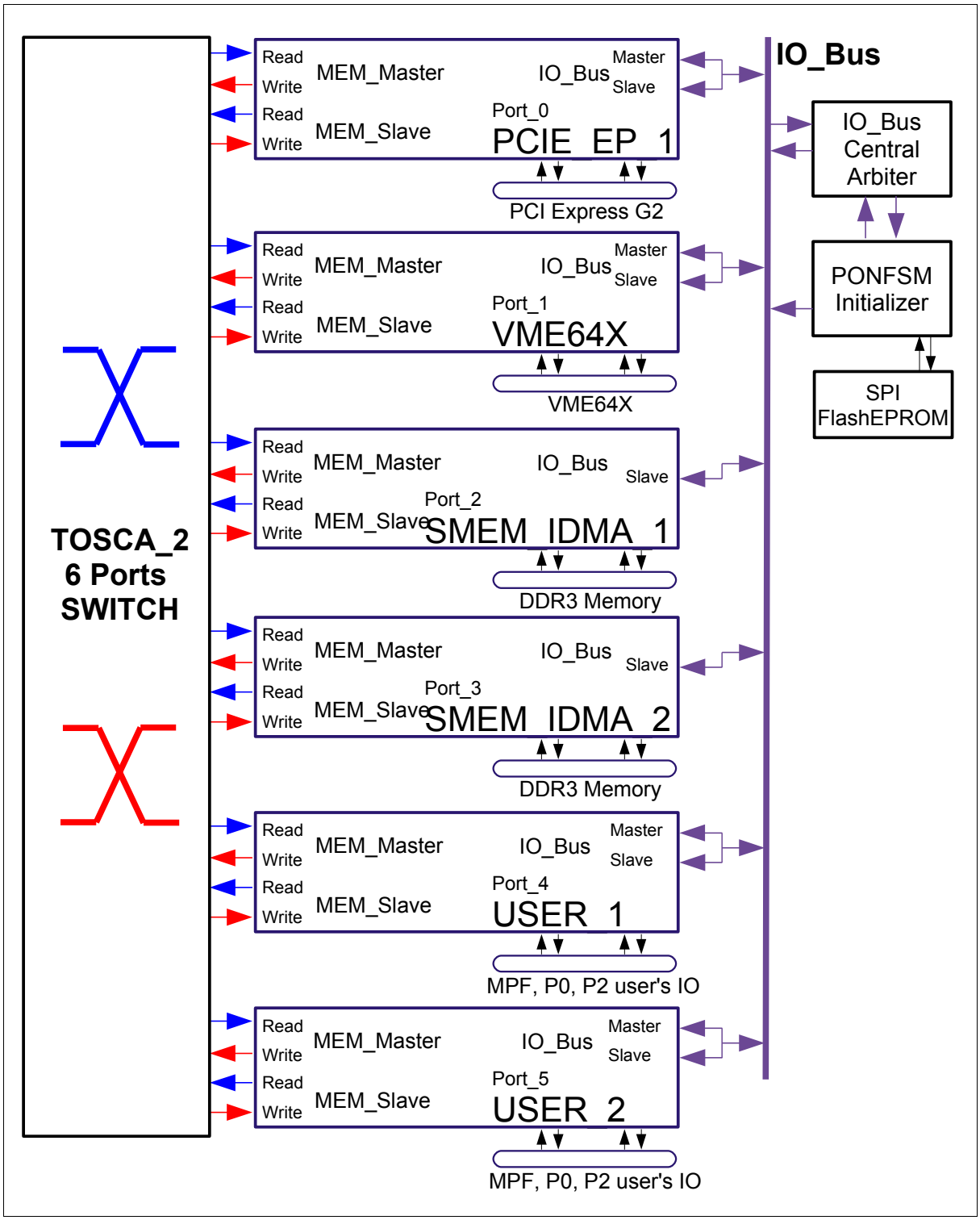

Illustration 25 : IFC_1210 TOSCA II Interconnection

The above diagram represents the default TOSCA II system with six(6) Agent Switch (Agent_SW) interconnected together.

- Port_0 : Agent_SW PCIE_EP1, PCI Express End Point
- Port_1 : Agent_SW VME64x Master/Slave + Slot_1
- Port_2 : Agent_SW SMEM_IDMA #1, Shared DDR3 Memory
- Port_3 : Agent_SW SMEM_IDMA #2, Shared DDR3 Memory
- Port_4 : Agent_SW USER #1, User's specific HDL controlling the MPF Top connector
- Port_5 : Agent_SW USER #1, User's specific HDL controlling the MPF Bottom connector

An implementation with eight(8) Agent_SW is also achievable. In this case, additional ports are assigned as follow :

- Port_6 : USER_3, A third USER's block
- Port_7 : PCIE_EP, as a second PCI Express EP /RC

The TOSCA II infrastructure implements a separate “Control Plane” to map IO type resources as command and status registers as well as the event/interrupt management.

The TOSCA II infrastructure keep and extends this segregation to its internal interconnection by differentiating physically the IO and the MEMORY transactions through independent CONTROL _Plane (IO) and DATA _Plane (MEMORY)

- The CONTROL_Plane is implemented through a standard shared parallel bus, named IO_Bus. An IO_Bus Master can Read/Write a selected IO_Bus Slave. Only single beat Read or Write transactions are supported. (No burst capability) The IO_Bus access is managed by a central arbiter providing grant access through a Round Robin priority algorithm.
- The DATA_Plane is implemented through the Central_SW, with non-blocking full mesh capability. This interconnection provides independent Read/Write paths for Master and Slave ports. It is optimized to provide maximal bandwidth with minimal latency between Master and Slave agent.

To save FPGA routing resource, the IO_Bus is implemented with 8-bit Address/Data multiplexed path.

3.2.1 IO_Bus (Control Plane)

The IFC_1210 IO_Bus infrastructure in implemented through a 6(8) KBytes area, assigning 1 KBytes for each IO_Bus device.

IO_Bus Device	Master	Slave	Description
PCIE_EP1	Y	Y	PCI Express IO_Bus Extension → IO_Bus Master bridged from PCIe IO space. → IO_Bus Slave also incorporate general resources
VME64x	Y	Y	VME64x CRCSR window (512K/64K) → IO_Bus Master bridged from PCIe IO space. → IO_Bus Slave VME resource
SMEM_IDMA#1	N	Y	

SMEM_IDMA#2	N	Y	Only IO_Bus Slave
USER#1	Y	Y	User defined functionality. Ready to support IO_bus Master/Slave
USER#2	Y	Y	
USER#3	(Y)	(Y)	
PCIE_EP2	(Y)	(Y)	Idem as for PCIE_EP1
PON_FSM	Y	N	Power ON initialization of IO_bus resources → IO_Bus Master under control of a micro-programmable sequence stored in SPI Flash memory

Table 3.1 : IFC_1210 IO_Bus Master/Slave Device support

3.2.1.1 IO_Bus Master

The TOSCA II IO_Bus central arbiter controls a router (simple multiplexer) providing grant Bus mastership up to the seven(7) IO_Bus Master. This arbiter implements round-robin arbitration protocol, and serves only a single Bus cycle at the time. Each IO_Bus master address a 8 KBytes area, mapping the eight (8) IO_Bus Slave. (1 KBytes each)
In the IFC_1210 implementation, the following eight potential IO_Bus Master are :

1. PON_FSM, Autonomous FSM Sequencer started at power-up, allowing to issues IO_Bus Write, directly fetched from the on-board SPI Flash EPROM. Up to 65K instruction can be stored in the SPI Flash EPROM #1 and executed sequentially before releasing the internal RESET. The PON_FSM allows to initialize completely the unit without any external software boot process. The SPI Flash EPROM #1 can be programmed with local support.

2. PCI_Express port. The IO_Bus is fully mapped in the PCI_Express IO Space. This occupies a total of 4 KBytes area in the PCI Express IO Space, set-up by the appropriate BAR(x) configuration register.

3. VME64x port. The IO_Space is fully mapped in the VME64x CR/CSR area. The IFC_1210's internal resources can be fully addressable from the VME64x Bus.

4. USER Block #1 port. Provision is made for User's block access. In case of this block is filled with intelligent resources, an access path is reserved. Soft IP_core as MicroBlaze, ARM Cortex M1 or upcoming Hard IP PowerPC 440 (available only with upcoming Virtex-5 FX family) can be added in the IFC_1210's FPGA as on-chip IO co-processor.

5. USER Block #2 port. (idem as previous one)

The two SMEM_IDMA block do not incorporate any IO_Bus Master.

The two additional ports are reserved for third USER Block #3 and second PCI Express EP/RC (PCIE_EPRC2).

3.2.1.2 IO_Bus Slave

The TOSCA II IO_Bus infrastructure maps eight(8) IO_Bus Slave. Each IO_Bus Slave occupies a fixed 1 KBytes space (256* D32 registers). Some of the IO_Bus Slave block also incorporates a 2nd local Bus access port. This 2nd port access is arbitrated internally with the IO_Bus access.
In the MPC_1100 implementations, eight (8) IO_Bus Slave are mapped.

1. PCIE_EP1, PCI Express EP and General IFC_1210 resources. This IO_Bus Slave owns all PCIe_EP/Local general registers resources.

2. VME64x. This IO_Bus Slave owns the VME64x CR/CSR Configuration resources. The concerned resources are also directly mapped with the VME Slave CR/CSR controller, providing a low latency path without potential dead-lock.

3. Shared Memory & IDMAC #1. This IO_Bus Slave owns all related registers controlling the DDR2 Shared Memory and IDMAC.

4. Shared Memory & IDMAC #2. (idem as previous one)

5. USER Block #1. This IO_Bus Slave owns TBD user's related registers and resources.

6. USER Block #2. (idem as previous one)

7. USER Block #3. (Reserved for extension)

8. PCIE_EP2. (Reserved for 2nd PCI Express EP)

3.2.2 MEMORY Bus (Data plane)

The TOSCA II Central_SW (Central Switch) provides full mesh independent data flows. Each flow is scheduled independently from the others and therefore implements simultaneous transactions on all of them. By providing up to 2*6*2 GBytes/s= 24 GBytes/s, a 6-ports Central_SW is ready to support multiple full speed PCI_Express x8, Revision 1.1 or PCI_Express x4, Revision 2.0.

The two independent full mesh interconnection support following transaction type as :

- The WRITE Posting & READ_Request , 64-bit - @200-(250 MHz), N independent path.
- The READ_Response, 64-bit - @200-(250 MHz), N independent path.

By default, the TOSCA II Central_SW supports data packets transactions up to 512 Bytes. Provision is made to support larger data packet. (1 KBytes and 2 KBytes) The packet size is directly derived from the DPRAM resource available in each back-end interface.

The IFC_1210 TOSCA Central_SW is composed of six(6) or optionally eight(8) independent back-end ports, each supporting Master/Slave / Read/Write independent channel access.

- 1x (2x) PCI Express Agent_SW, directly attached to the Virtex-6 PCI Express EP/RC
- 1x VME64x Agent_SW
- 2x DDR3 Shared Memory – IDMAC Agent_SW
- 2x (3x) USER Block Agent_SW

The following diagram represents, for better understanding, a simplified 4-ports TOSCA II switch. The blue section represents the Request flow (Write and Read) and the Orange section represents the Response flow (Read)

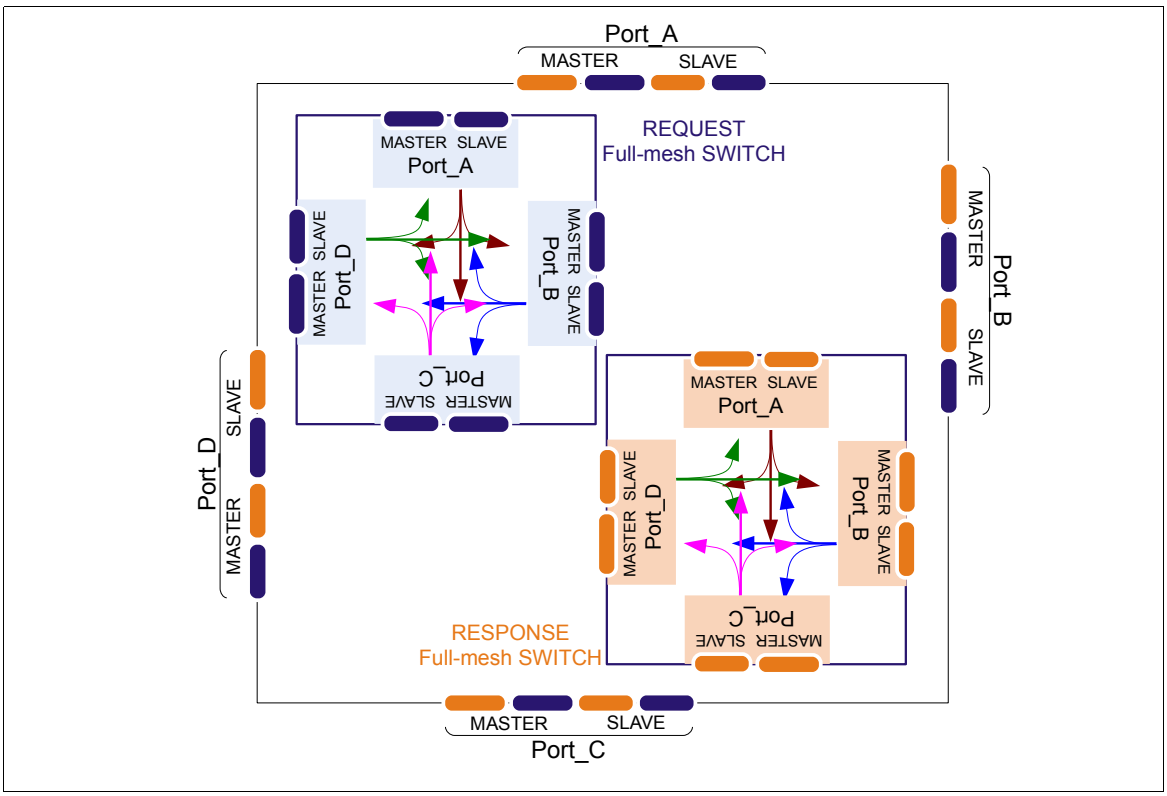

Illustration 26 : TOSCA II Simplified Central_SW Implementation

The Central_SW implements two full mesh interconnection between the four ports. Packet buffering is implemented at Source and at Destination section, this independently for each type of transaction. The above diagram represents in blue the four data flow for a transaction type (i.e WRITE Posting & READ_Request). The 2nd full mesh (orange), implements the READ_Response data flow...

Each Agent_SW port, integrates four interfaces types with specific buffering. The following table sums up the interface implementation.

Interface	Description	Buffering	Comments
WPOST_RDRQ_MAS	Write_Posting and READ_Request. The back-end Master controller generates the packets	6* [512+64] Bytes + 6* [64] Bytes	Two independent buffer queue segregating the Write_Posting and the READ_Request. Specific control logic for the Write-read ordering.
WPOST_RDRQ_SLV	Write_Posting and READ_Request. The back-end Slave controller consumes the packets and executes them.	3*4* [512+64] Bytes + 3*4* [64] Bytes	Independent buffer queue assigned for each sources
RDRS_MAS	Read Response with Data. The back-end Master controller, (initiator of the Read-Request) consumes the	6* [512+64] Bytes	Provision made for "Write Status Response" in case of the Central-SW shall supports others protocol (i.e Rapid-IO or Specific)

Interface	Description	Buffering	Comments
	received data packet.		
RDRS_SLV	Read Response with Data.. The The back-end Slave controller load the response data packet.	6* [512+64] Bytes	Common buffering for the three Read Responder sources.

Table 3.2 : Agent_SW TOSCA II Back-end Interfaces

1815

Note The standard IFC_1210 implementation of the TOSCA II Central_SW (6-ports, 512 Bytes data packet) consumes thirty-six(36) (6* 6) 36K Block RAM.

3.3 General Local Resources

Due to legacy implementation (IOxOS PEV_1100), the IFC_1210 general resources are all located with the PCIE_EP1 Agent_SW. Following general resources are implemented

- Eight channel I2C Controller
- SPI Controller
- PON_FSM Controller
- General Status of the MPC1200 board as Configuration, Signature
- Virtex-6 System Monitor

For complete description of the above resources, refer to the “Tosca2_AgentSW_PCIe_EP_UG” document.

3.3.1 I2C Controller.

The IFC_1210 PCI Express EP Agent_SW integrates a I2C Controller controlling eight I2C Buses, assigned in the 1PC_1210 to follow resources :

- Port_0 → On-board temperature monitor LM95235 + PCA9502
- Port_1 → Reserved
- Port_2 → BMR43 DC-DC + MAX5970 LI Controller
- Port_3 → VME P0 wired
- Port_4 → XMC#1/ FMC#1connector SMBus
- Port_5 → XMC#2 / FMC#2 connector SMBus
- Port_6 → PCI Express Switch IDT PES32NT24AG2
- Port_7 → Programmable clock generator IDT8N4Q001

The I2C Master controller is interfaced with four control registers “I2C_CTL”, “I2C_CMD”, “I2C_DATW” and “I2C_DATR”.

→ Refer to the “Tosca2_AgentSW_PCIe_EP_UG” chapters 2.6 and 4.2.20

3.3.2 SPI Controller.

The IFC_1210 incorporates three(3) 128 MBit Serial Flash EPROM (Spansion, Windbond/ eON) used to store in non-volatile device the FPGA bit-stream and its associated PON_FSM micro-code. These non volatile memory device can be access from two different ports.

- FPGA S1AA handling the power-up FPGA configuration.
- SPI specific control register “ILOC_SPI”

The SPI Serial Flash Device is fully accessible in run time and can than be reprogrammed from the

Host controller with specific utilities. XprsMON command are provided to support new FPGA bit-stream programming (update).

The SPI Serial Flash are organized in different different mapping, fixed with option related to the bit-stream size of the on-board populated FPGA type.

The SPI Master controller is interfaced with the register “I2C_DATR”.

→ Refer to the “Tosca2_AgentSW_PCIe_EP_UG” chapters 2.7 and 4.2.5

3.3.3 PON_FSM Controller.

Already described in previous chapter

→ Refer to the “Tosca2_AgentSW_PCIe_EP_UG” chapter 4.2.4

3.3.4 XILINX VIRTEX-6 System Monitor

The XILINX Virtex-6 FPGA incorporates a System Monitor with 10-bit ADC, allowing to implement analog monitoring on specific parameters. By default, internal parameters as VCC_{CORE} and die temperature are continuously evaluated.

The XILINX System Monitor technical description is provided in XILINX UG370 document “Virtex-6 System Monitor User's guide”.

On the IFC_1210, only the pin couple VP /VP (Bank_0) are connected through a voltage divider (1.2:3.0) to VCC_2V5.

An external electronic voltage reference, Burr-Brown REF3012, provides the precise 0.2% 1.25[V] voltage reference to the System Monitor.

The System Monitor controller is controlled trough “V6_SMON_ADDPT” , “V6_SMON_DAT” and “V6_SMON_STA”registers.

→ Refer to the “Tosca2_AgentSW_PCIe_EP_UG” chapter 4.2.11 – 4.2.13

3.4 PCI Express EP1 Agent_SW

The IFC_1210 provides a complete PCI Express x4 EP Interface. This interface can be physically connected with :

- MPR_1260 (across VME P0 UHM Connector)
- MPF_1222 (across MPF SAMTEC Connectors)

The IFC_1210 “CENTRAL” FPGA Virtex-6 owns two PCI Express LogiCORE. Each one can be connected to specific Quad_GTX transceiver.

For complete description refer to “Tosca2_AgentSW_PCIe_EP_UG” document.

3.4.1 IFC_1210 Specific TOSCA II Implementation

→ Refer to the “Tosca2_IFC1210_Implementation_UG” document.

3.5 VME64x Agent_SW

The IFC_1210 provides a complete VME64x Master/Slave Interface with Slot_1 function. The following sections provide an overview of the implemented VME sub-functions. For complete VME Bus understanding please refer to the VITA specification with addendum.

The IFC_1210 is ready to operate in VME64x 5-rows backplane as well in legacy VME64 3-row backplane. The IFC_1210 is designed to use directly the 3.3[V] from the VME backplane (only available in 5-rows connector). While plugged in legacy VME 3-rows backplane, a local DCDC is used to built the on-board 3.3[V] poser supply

Static option SW1-3 determines the mode of operation related to the CR/CSR mapping support.

Refer to “Tosca2_AgentSW_VME64X_UG” document.

3.5.1 IFC_1210 Specific TOSCA II Implementation

→ Refer to the “Tosca2_IFC1210_Implementation_UG” document.

3.6 SMEM Shared Memory

The IFC_1210 instantiates two independent DDR3 SMEM Memory Controllers.

Each controller controls independently two(2) DDR3 16-bit devices running in QDR mode with a native clock frequency between 200 to 250 MHz. This mode support 64-bit data every clock cycle → 1.6 to 2.0 GBytes/s. (The two SMEM instantiation provides a total of 6.4 – 8.0 GBytes/s)

The two independent array provide independent SMEM DIRECT interfaces. These direct path are made available to the USER Agent_SW.

The IFC_1210 implements four(4) DDR3 devices organized in x16 providing 512, 1024 or 2048 MBytes on-board shared memory. The two bit field “ddr3_SIZE” located in the “SMEM_DDR3_CSR” register provides information on populated devices.

ddr3_SIZE =	“01”	1024MBit	= 4* 128 MBytes (optional)
	“10”	2048MBit	= 4* 256 MBytes (default)
	“11”	4096MBit	= 4* 512 Future upgrade while available

Refer to “Tosca2_AgentSW_SMEMIDMA_UG” document.

3.6.1 IFC_1210 Specific TOSCA II Implementation

→ Refer to the “Tosca2_IFC1210_Implementation_UG” document.

3.7 IDMA Embedded Controller

The IFC_1210 implements multi-channel (4) DMA controller, especially designed to support high efficient data movement between the DDR3 Shared Memory and others TOSCA II Agent_SW (PCI Express EP Agent_SW, VME64x Bus Agent_SW, USER blocks Agent_SW.

The number of instantiated IDMA Read_Engines (0, 1 or 2), Read_Engines (0, 1 or 2) can be defined while the "CENTRAL" FPGA Virtex-6 is built.

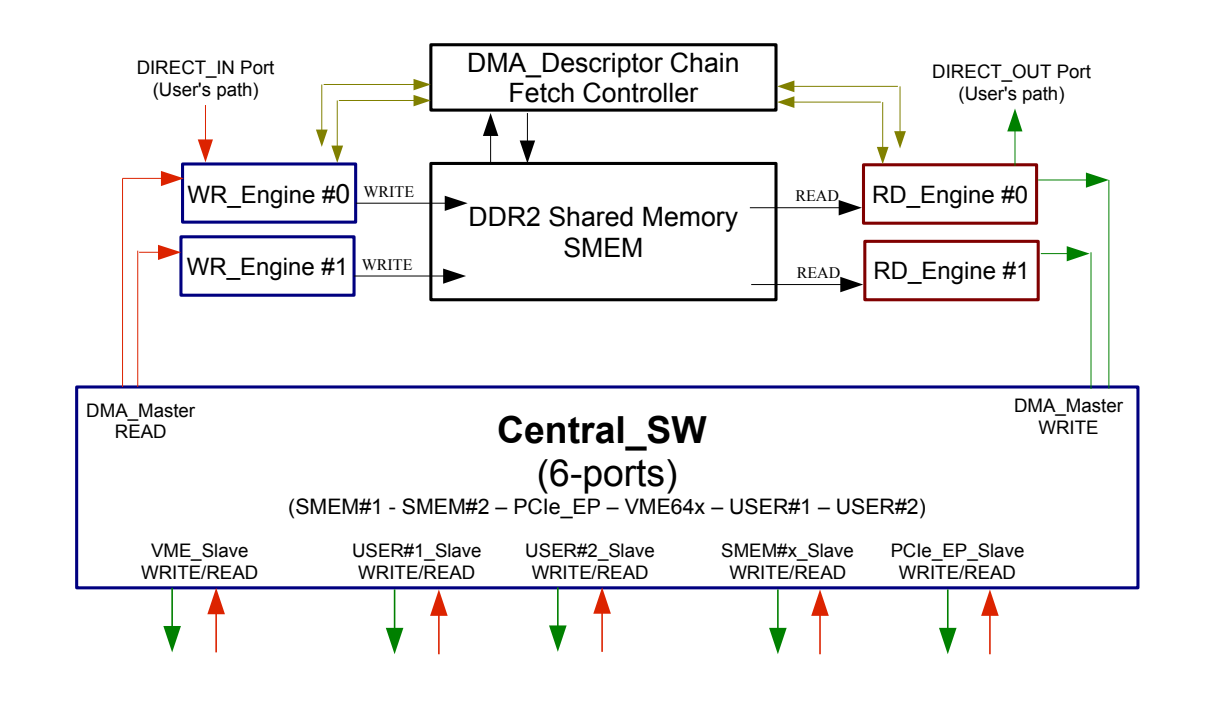

Illustration 27 : IFC_1210 Embedded IDMA Controllers

The above drawing represents a simplified functional diagram of the IDMAC implementation. The IDMAC is directly attached to the SMEM block and therefore optimized to get maximum performance from the DDR3 devices. (burst size, page management, DPRAM caches, ...)

- The IFC_1210 IDMAC system, is implemented with independent READ and WRITE IDMA Engine. Each engine can process its own chain of DMA_Descriptor.
- The DMA_Descriptor chaining shall be located in the local DDR3 SMEM. The DMA_Descriptor shall be first built by the application before any DMA process. To provide maximum performance, a cache memory (DPRAM) stores 64 consecutive DMA_Descriptor per channel.
- The IDMA SMEM DDR2 access (Read and Write) are optimized for block/burst transactions, supporting maximal bandwidth (up to 1.6 GBytes/s @ 200 MHz (DDR400)
- The IDMA WRITE_Engine(s) is dedicated for DMA transfer to the SMEM (→ DDR3 Write ...). Data source comes from any of the Central_SW Agent (PCIe_EP, VME64x, USER#1, USER#2 or SMEM#x) or from the DIRECT_IN Port.

- The READ_Engine(s) are dedicated for DMA transfer from the SMEM (→ DDR3 Read ...). to any of the Central_SW Agent (PCIe_EP, VME64x, USER#1, USER#2 or SMEM#x) or from the DIRECT_OUT Port.
- All IDMA Engines can be programmed with selectable “Start_of_Operation” Trigger facilities as End of operation of another IDMA Engine, User's specific event, Global Time, ... Each DMA Engine can issue local Trigger on Start or End of a DMA_Descriptor execution.
- Each IDMA Engine can issue Interrupt on the Start/End of a DMA_Descriptor execution. Reported Error can also issue specific interrupt.
- DIRECT Port_IN/OUT are provided for on-chip DMA facilities to dedicated user's hardware as DAQ queues, autonomous communication engine, data servers

Refer to “Tosca2_AgentSW_SMEMIDMA_UG” document.

3.7.1 IFC_1210 Specific TOSCA II Implementation

→ Refer to the “Tosca2_IFC1210_Implementation_UG” document.

3.8 Interrupt Infrastructure

The IFC_1210 implements a complete Interrupt infrastructure with dispatching to the PCI Express Host Controller or to the local VME INTG . The PCI Express MSI generator, manages the MSI generation, on request from the attached ITC16.

The IFC_1210 instantiates six(6) ITC16 blocks providing management for up to 96 local interrupts. The six(6) ITC16 issues a unique PCI Express MSI. The PCI Express MSI parameters are defined through the PCI Express System Configuration. (Refer to PCI Express specification)

Due to LINUX limitation, only single vector MSI is supported. To work-around this system integration issue, a dedicated hardware FSM has been implemented to support the six(6) on chip ITC serviced through a single MSI message.

Provision is made to extend the interrupt infrastructure up to eight(8) ITC16.

Refer to “Tosca2_Architecture_UG” document.

3.8.1 IFC_1210 Specific TOSCA II Implementation

→ Refer to the “Tosca2_IFC1210_Implementation_UG” document.

4. IFC_1210 HSID

Following chapters provides the IFC_1210 's Hardware-Software Interface Data (HSID).

4.1 QorIQ P2020 Mapping

The P2020 resource mapping is assigned ...

To Be Completed

P2020 Address Range	Ressources	Comments
0x0000'0000-0x3FFF'FFFF	System Memory	1st GBytes
0x4000'0000-0x7FFF'FFFF	System Memory Extension	2nd GBytes
0x4000'0000-0xBFFF'FFFF	PCI Express #1	
0x0000'0000-0x0000'0000	...	
0x0000'0000-0x0000'0000	...	
0xFFB0'0000-0xFFB0'FFFF	“PON“ FPGA ELB Resources	
0x0000'0000-0x0000'0000	NOR Flash Memory	
0x0000'0000-0x0000'0000	P2020 Control Register	

Table 4.1 : P2020 Resources Mapping

Note Above address reference are valid for U-BOOT set-up. Because the P2020 provides dynamic resource mapping capability, the OS mapping can be different

4.2 ELB "PON" FPGA Resources

The „PON“ FPGA integrates dedicated resources directly connected to the P2020 ELB interface and fully available even while the „CENTRAL“ FPGA and the „IO“ FPGA are not configured.

This capability allows to leave the IFC_1210 configuration sequence under control of the P2020. The P2020 computing core can fully boot an OS without „CENTRAL“ FPGA and the „IO“ FPGA configured.

Following IFC_1210 functions are directly supported in the „PON“ FPGA through the ELB interface.

- General IFC_1210 control and status
- Power management and Programmable clock
- SPI Master controller, supporting Read and Write access to the three SPI Flash memory storing the FPGA bit-streams and the Signature area.
- I2C Master controller, providing direct access to the IFC_1210 I2C resources
- PES32NT24AG2 configuration control (RESET + HALT)

- FPGA SW controlled configurator. The „CENTRAL“ FPGA and the „IO“ FPGA can be configured directly from the P2020.

The „PON“ FPGA implement a 8-bit ELB interface running at 75 MHz.

- CS#6 (Configured with P2020 OR6/BR6)
- 8-bit Data Bus (R/W performance 120 [ns]/cycle -> ~ 6 MBytes/s)
- 16-bit Address Bus (64 KBytes area reserved)
- 75 MHz elb_LCLK

4.2.1 ELB Resource mapping

The following table sums up the resources mapped over the ELB Bus Device #6.

ELB Offset	Register	Comments
+ 0x0000	ELB_VendDev_ID	Vendor_ID + Device_ID = 0x7357_1210
+ 0x0004	ELB_Static_SW	Status of the IFC_1210 static options. (Switches & Hex_ROT)
+ 0x0008	ELB_VME_CTL	VME64x related
+ 0x000C	ELB_FMCXMC_CTL	Mezzanine card control FMC, XMC, PMC
+ 0x0010	ELB_GENERAL_CTL	Power Supplies + Clock Management
+ 0x0014	ELB_PCIESW	PCI Express Switch Strapping
+ 0x0018	ELB_RWTST1	32-bit RW Register (Cleared while Short RESET)
+ 0x001C	ELB_Sign	32-bit signature word. Defined in the VHDL source code
+ 0x0020	ELB_FPGA_CFGCTL	FPGA Configuration control
+ 0x0024	ELB_FPGA_CFGDAT	FPGA Configuration data port (32-bit)
+ 0x0028	ELB_SPI_CTL	SPI Master Controller
+ 0x002C	ELB_PGMRST_CTL	PGM RST Sequencing
+ 0x0030	ELB_I2C_CTL	I2C Master Controller
+ 0x0034	ELB_I2C_CMD	I2C Master Controller
+ 0x0038	ELB_I2C_DATW	I2C Master Controller
+ 0x003C	ELB_I2C_DATR	I2C Master Controller
+ 0x0040	ELB_BMRCTL	BMR463 SYNC Control
+ 0x0044 ... + 0xDFFF	Not Implemented	Reserved for further user defined resources
+ 0xE000 + 0xFFFF	ELB_SRAM	8 KBytes SRAM area

Table 4.2 : P2020 ELB “PON“ Resources Mapping

4.2.2 SRAM

A 8 KBytes SRAM area is instantiated at the top of the decoded area. This SRAM area can be used for temporary data storage, independent from Cold_RESET.

4.2.3 General Control & Status

4.2.3.1 ELB_VendDev_ID

Provides HDL related Vendor_ID + Device_ID information.

ELB_VendDev_ID ELB : 0x0000 - 0x0003		"PON" Vendor_ID + Device_ID Signature			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[31:0]	VendDev_ID[31:0]	R	Value	Fixed Value = 0x7357_1210	

4.2.3.2 ELB_Static_SW

Provides status information of the IFC_1210 static options

ELB_Static_SW ELB : 0x0004 - 0x0007		"PON" Static Switch Status			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[31:28]	Hex_ROT[7:4]	R		HexROT Switch SW103	Refer to chapter 2.3.4
[27:24]	Hex_ROT[3:0]	R		HexROT Switch SW102	
[23:16]	Reserved	R	0x00	Reserved	
[15:8]	Switch_B[8:1]	R		Mini DIP Switch SW100	Refer to chapter 2.3.2
[7:0]	Switch_A[8:1]	R		Mini DIP Switch SW101	Refer to chapter 2.3.1

4.2.3.3 ELB_VME_CTL

Provides direct VME64x related control and status.

ELB_VME_CTL ELB : 0x0008 - 0x000B		VME Direct Control and Status			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[4:0]	Rx_GA	R		VME Geographic addressing	
[5]	Rx_GAP	R		VME Geographic addressing	
[6]	Rx_SLOT1	R		VME Slot-1 function enabled	
[7]	Rx_BBSY#	R		VME BBSY direct signal	! Active Low
[8]	Rx_ACFAIL#	R		VME direct ACFAIL signal	! Active Low
[15:9]	Rx_IRQ[7:1]#	R		VME direct INTERRUPT signal	! Active Low
[16]	Tx_SERDAT	RW	'0'	VME Serial Bus SW control	
[17]	Rx_SERDAT	R			

ELB_VME_CTL ELB : 0x0008 - 0x000B		VME Direct Control and Status			
[18]	Tx_SERDAT_OE	RW	'0'		
[19]	Reserved			Not used	
[20]	Tx_SERCLK	RW	'0'	VME Serial Bus SW control	
[21]	Rx_SERCLK	R			
[22]	Tx_SERCLK_OE	RW	'0'		
[23]	Reserved			Not used	
[27:24]	Reserved			Not used	
[28]	Rx_SYSRESET#	R		VME direct SYSRESET signal	! Active Low
[29]	Rx_SYSFAIL#	R		VME direct SYSFAIL signal	! Active Low
[30]	Tx_SYSRESET	RW	'0'	VME control SYSRESET signal (Masked with SW1-7 static)	
[31]	Tx_SYSFAIL	RW	'0'	VME control SYSFAIL signal	

4.2.3.4 ELB_FMCXMC_CTL

Provides direct Mezzanine (PMC, XMC, FMC) related control and status.

ELB_FMCXMC_CTL ELB : 0x000C - 0x000F		Mezzanine Direct Control and Status			
Bit[]	**Function**	**R/W**	**Res**	**Description**	**Comments**
[0]	XMC1_PRESENTn	R		XMC Mezzanine present status	! Active Low
[1]	XMC2_PRESENTn	R			
[2]	XMX12_MWMRO	RW	'0'	XMC Memory Write protect	
[7:3]	Reserved	R		Not used	
[1]	PMC_BMODE_1	R		PMC Slot status information	
[8]	PMC_MONARQUEn	R		PMC Slot status information	! Active Low
[10]	PMC_EREADYn	R		PMC Slot status information	! Active Low
[11]	PMC_M66EN	R		PMC Slot status information	
[12]	8112_WAKE_INn	R		PES8112 PCIe-PCI Bridge direct status	! Active Low
[13]	8112_GPIO_0	R		PES8112 PCIe-PCI Bridge direct status	
[14]	8112_BAR0ENB	RW	'0'	PES8112 PCIe-PCI Bridge static option	
[15]	8112_FORWARD	RW	'0'	PES8112 PCIe-PCI Bridge static option	
[16]	FMC1_RES0	R		FMC#1 direct status Reserved_0	
[17]	FMC1_PG_M2C	R		FMC#1 direct status Power Good	
[18]	FMC1_PRSTn	R		FMC#1 direct status Present	! Active Low
[19]	Reserved	R		Not used	
[20]	FMC1_RES0	R		FMC#2 direct status Reserved_0	
[21]	FMC1_PG_M2C	R		FMC#2 direct status Power Good	
[22]	FMC1_PRSTn	R		FMC#2 direct status Present	! Active Low

ELB_FMCXMC_CTL ELB : 0x000C - 0x000F		Mezzanine Direct Control and Status			
[23]	Reserved	R		Not used	
[29:24]	Reserved	R		Not used	
[30]	FMC12_PG_C2M	RW	'0'	FMC#12 Power Good	
[31]	FMC12_VADJ_ENA	RW	'0'	FMC#12 Enable VADJ power supply	

2030

4.2.3.5 ELB_GENERAL_CTL

Provides direct IDT Clock Generator and IDT PCI Express Switch related control and status.

ELB_GENERAL_CTL ELB : 0x0010- 0x0013		Power Supplies Direct Control and Status			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[1:0]	IDTCLK_SEL[1:0]	RW	00	IDT Programmable clock generator frequency selection	IDT 8N4Q01EG
[2]	IDTCLK_OE	RW	0	IDT Programmable clock generator Enable	
[3]	FUSE5132_ENA	RW	0	Enable +12[V] Solid state fuse	NIS5132MN1TXG
[4]	CDCLVD2104_DIS	RW	0	IDT Programmable clock on-board ditribution disable. 0 Enable 1 Disable	TI CDCLVD2104
[6:5]	Reserved	R		Not used	
[15:7]	PCIESW_GPIO[8:0]	R		PCI Express Switch IDT 32NT24 GPIO direct signalling (IN)	IDT PES32NT24AG2
[31:16]	PON_Timer[15:0]	R	0x0000	16-bit counter-timer 1KHz. This counter timer is reset at power-up or under action of Long_RESET detection	

The PON_Timer provides a boot time information with [ms] granularity. The PON_Timer is reset (forced to 0x0000) on detection of a “Cold_RESET“.

2035

“Cold_RESET“ is activated at power-up or while the "Ergonomic IEEE Hot-swap Injector/Ejector Handle" is opened for more than 1 second.

4.2.3.6 ELB_PCIESW_CTL

This control register provides control information to configure the PCI Express Switch PES32NT24AG2 at RESET. (Power-up and Programmed RESET)

2040

ELB_PCIESW_CTL ELB : 0x0014 - 0x0017		PCI Express Switch Control and Status			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**

<table>
<tr><th colspan="2">ELB_PCIESW_CTL
ELB : 0x0014 - 0x0017</th><th colspan="4">PCI Express Switch Control and Status</th></tr>
<tr><td>[1:0]</td><td>PCIESW_STK1CFC[1:0]</td><td>RW</td><td>HDL</td><td>PCIe Switch PES32NT24 Stack_1 Static Configuration. (XMC#1)
<table><tr><th>CFC[1:0]</th><th>PCI Express Lane assignation</th></tr><tr><td>00</td><td>x8</td></tr><tr><td>01</td><td>x4 – x4 (RESET default)</td></tr><tr><td>10</td><td>x2 – x2 -x4</td></tr><tr><td>11</td><td>x2 – x2 - x2 - x2</td></tr></table></td><td></td></tr>
<tr><td>[7:2]</td><td>Reserved</td><td>R</td><td></td><td>Not used</td><td></td></tr>
<tr><td>[12:8]</td><td>PCIESW_STK2CFC[4:0]</td><td>RW</td><td>HDL</td><td>PCIe Switch PES32NT24 Stack_2 Static Configuration. (VME_P0)
<table><tr><th>CFC[4:0]</th><th>PCI Express Lane assignation</th></tr><tr><td>0_0000</td><td>x8</td></tr><tr><td>0_0001</td><td>x4 - x4 (RESET default)</td></tr><tr><td>0_0010</td><td>x2 – x2 -x4</td></tr><tr><td>0_0011</td><td>x2 – x2 - x2 - x2</td></tr><tr><td>1_1011</td><td>x1 - x1 - x1 - x1 - x1 - x1 - x1 - x1</td></tr><tr><td>Others</td><td>Refer to IDT PES32NT24AG user' Manual Table 3.6</td></tr></table></td><td></td></tr>
<tr><td>[15:13]</td><td>Reserved</td><td>R</td><td></td><td>Not used</td><td></td></tr>
<tr><td>[17:16]</td><td>PCIESW_STK3CFC[1:0]</td><td>RW</td><td>HDL</td><td>PCIe Switch PES32NT24 Stack_2 Static Configuration. (XMC#2)
<table><tr><th>CFC[1:0]</th><th>PCI Express Lane assignation</th></tr><tr><td>00</td><td>x8</td></tr><tr><td>01</td><td>x4 - x4 (RESET default)</td></tr><tr><td>10</td><td>x2 – x2 -x4</td></tr><tr><td>11</td><td>x2 – x2 - x2 - x2</td></tr></table></td><td></td></tr>
<tr><td>[23:18]</td><td>Reserved</td><td>R</td><td></td><td>Not used</td><td></td></tr>
<tr><td>[27:24]</td><td>PCIESW_SWMODE[3:0]</td><td>RW</td><td>HDL</td><td>PCIe Switch PES32NT24 Static Configuration.
<table><tr><th>SWMOD [3:0]</th><th>Switch Mode of operation</th></tr><tr><td>0000</td><td>Single Partition</td></tr><tr><td>0001</td><td>Single Partition with reduced latency</td></tr><tr><td>0010</td><td>Single Partition with EEPROM init</td></tr><tr><td>0011</td><td>Single Partition with reduced latency annd EEPROM init</td></tr></table></td><td></td></tr>
</table>

ELB_PCIESW_CTL ELB : 0x0014 - 0x0017				PCI Express Switch Control and Status	
				Others: Refer to IDT PES32NT24AG user' Manual Table 3.8 The switch SW2-[8:7] select the power-up default setting as : SW2-[8:7] / PES32NT24AG Switch Mode: 00 – Single partition 01 – Single partition with reduced latency 10 – Single partition with Serial EEPROM Initialization with reduced latency 11 – Reserved, User defined in “PON” FPGA	
[29:28]	PCIESW_CLKMODE[1:0]	RW	HDL	PCIe Switch PES32NT24 Static Configuration. CLKMODE / PES32NT24AG Clock Mode: 00 – Global Clock Mode 01 – Local Clock Mode 1X – Reserved	
[30]	PCIESW_RSTHALT	RW	'0'	PCIe Switch PES32NT24 Static Configuration.	
[31]	Reserved	R		Not used	

4.2.3.7 ELB_TEST_1_REG

These two simple 32-bit Read-Write Registers allows to implement SW markers during boot sequencing. The ELB_TEST1_REG is cleared on assertion of FPSW_DET_SHORT. ("Ergonomic IEEE Hot-swap Injector/Ejector Handle" open for less than 1 second)

ELB_TEST1_REG ELB : 0x0018 - 0x001B		Simple RW Test Register			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[31:0]	TEST1[31:0]	RW	0x00000000	Basic 32-bit RW register. Cleared on detection of FPSW_DET_SHORT.	

4.2.3.8 ELB_Signature

Provides HDL related signature information.

ELB_Sign ELB : 0x001C - 0x001F		"PON" FPGA Signature			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[31:0]	RTL_Signature[31:0]	R	Value	This status field provides signature information specified in the "PON" FPGA VHDL. • **"PON_Signature"**	

4.2.4 ELB FPGA Configuration

Following control and status registers provides facility to configure the FPGA "CENTRAL" and "IO" directly from the P2020 processor. The IFC_1210 computing core can be fully operational while the "CENTRAL" and "IO" FPGA are not configured.

In this mode of operation is enabled, (SW2-4 = "ON" "**ColdRESET_Mode**") the IFC_1210 FPGA "CENTRAL" and "IO" shall be configured under the control of the P2020 processor.

4.2.4.1 ELB_FPGA_CFGCTL

This control & status register supports the FPGA configuration logic.

ELB_FPGA_CFGCTL ELB : 0x0020 - 0x0023		"PON" FPGA Configuration Control			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[0]	fpga_central_INITn	R		FPGA "CENTRAL" Virtex-6T **INIT** pin	
[1]	fpga_central_DONE	R		FPGA "CENTRAL" Virtex-6T **DONE** pin	
[2]	fpga_central_PROGn	RW	'1'	FPGA "CENTRAL" Virtex-6T **PROGRAM** pin	
[4:3]	Reserved	R		Not used	
[5]	fpga_central_CSIn	RW	1'	FPGA "CENTRAL" Virtex-6T **CSI** pin	
[6]	fpga_central_RDWRn	RW	'1'	FPGA "CENTRAL" Virtex-6T **RDWR** pin	
[7]	fpga_central_ENA	RW	'0'	FPGA "CENTRAL" Virtex-6T Enable Configuration	
[8]	fpga_io_INITn	R		FPGA "IO" Spartan-6 **INIT** pin	
[9]	fpga_io_DONE	R		FPGA "IO" Spartan-6 **DONE** pin	
[10]	fpga_io_PROGn	RW	'1'	FPGA "IO" Spartan-6 **PROGRAM** pin	
[14:11]	Reserved	R		Not used	
[15]	fpga_io_ENA	RW	'0'	FPGA "IO" Spartan-6 Enable Configuration	
[21:16]	Reserved	R	'0'	Not used.	
[22]	Seq_P2020_LRESET	W	'0'	While set, IFC-1210 Cold_RESET is activated. Equivalent to FPSW_DET_LONG.	
[23]	Seq_P2020_SRESET	W	'0'	While set, the P2020 is forced with HRESET activated. Equivalent to FPSW_DET_SHORT.	

ELB_FPGA_CFGCTL ELB : 0x0020 - 0x0023		"PON" FPGA Configuration Control			
[25:24]	fpga_CONF_BSTR[1:0]	R	"00"	FPGA Harware Configurator status FPGA bitstream number	
[27:26]	fpga_CONF_STATUS[1:0]	R	"00"	FPGA Harware Configurator status 00 Not Configured 01 Error 10 Configured OK 11 Configured BACKUP	
[29:28]	Seq_BSTR[1:0]	RW	"00"	FPGA Bitstream Number associated with command Seq_CONF_CMD	
[30]	Seq_CONF_CMD	RW	'0'	Force FPGA Configuration HW process with Seq_BSTR[1:0]	
[31]	Seq_RUN_CMD	RW	'0'	Force FPGA RESET release and issue a programmabel RESET . This control bit shall be forced to '1' after „CENTRAL" FPGA and „IO" FPGA have been configured by the P2020.	

4.2.4.2 ELB_FPGA_CFGDAT

This data register allows to load 32-bit at the time in the configuration logic

- Virtex-6T "CENTRAL" FPGA → 4 Bytes @ 50 MHz.
- Spartan-6 "IO" FPGA →16 bits @ 50 MHz.

ELB_FPGA_CFGDAT ELB : 0x0024 - 0x0027		"PON" FPGA Configuration Data			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[15:0]	FPGA Bit-stream[31:0]	W	0x0000	FPGA bit-stream low half-word common for „CENTRAL" and „IO" FPGA.	
[31:16]	FPGA Bit-stream[31:0]	W	0x0000	FPGA bit-stream high half-word only for „CENTRAL" FPGA.	

This register provides the FPGA configuration streaming support. Access to this register in 32-bit mode requires 480[ns] (Four(4) ELB transactions)

When fpga_central_ENA = '1' Everytime the ELB_FPGA_CFGDAT is written, the 32-bit is demultiplexed in 4 time 8-bit with 4 clock edges. This sequence is executed in 80[ns].

When fpga_io_ENA = '1', only the low 16-bit section is used. Everytime the ELB_FPGA_CFGDAT is written, the 16-bit is serialized with 16 clock edges. This sequence is executed in 320[ns].

4.2.5 SPI Master Interface

The three SPI Flash EPROM dedicated for the FPGA bit-stream non volatile storage can be

accessed through the P2020 ELB port.

- Read access for FPGA signature verification
- Write access for Flash EPROM programming (non volatile storage of FPGA bit-streams and PONFSM microcode)

SPI Master controller is implemented identical as in the TOSCA 2 infrastructure, providing backward software compatibility.

4.2.5.1 ELB_SPI Register

This register provides control&status information to support on-board SPI Flash EPROM programming.

The SPI interface protocol shall be completely controlled under software.

ELB_SPI IO_Bus : 0x028 - 0x02B		**SPI Flash EPROM programming**			
Bit[]	**Function**	**R/W**	**Res**	**Description**	**Comments**
[0]	pgm_SPICLK	W	'0'	SPI Clock calibrated pulse. While set a calibrated 32 [ns] pulse is automatically generated, with controlled set-up /hold time related to “pgm_SPIDO”	Need time accurate sequencing.
[1]	pgm_SPIDO	RW	'0'	SPI Data OUT direct pin control	
[2]	pgm_SPIDI	R	'0'	SPI Data IN direct pin status	
[3]	pgm_SPICS	RW	'0'	SPI Chip Select direct pin control. '1' for CS active.	
[5:4]	Reserved	R	--	Not implemented	
[7:6]	pgm_SPISEL[1:0]	RW	“00”	FC_1210 SPI Device selection. **pgm_SPISEL[1:0]** / **FPGA bit-stream Nb** 00 / No selection 01 / SPI Device#1 10 / SPI Device#2 11 / SPI Device#3	
[8]	pgm_REM_RELOAD	W	'0'	Remote Internal RESET with/without selected FPGA reconfiguration. This command is associated with FPGA bit-stream number defined with “pgm_SPISEL[1:0] “ **pgm_SPISEL[1:0]** / **FPGA bit-stream Nb** 00 / Bit-stream_#0 01 / Bit-stream_#1 10 / Bit-stream_#2 11 / Bit-stream_#3 The association of “pgm_SPIDO” and “pgm_SPICS” allows to qualify the FPGA reload operation as : **{pgm_SPICS, pgm_SPIDO}** / **FPGA bit-stream Number**	

ELB_SPI IO_Bus : 0x028 - 0x02B				SPI Flash EPROM programming	
				00 — No FPGA reload, only on-board RESET generation V1 + S2 01 — FPGA V1 reload + RESET 10 — FPGA V1 + S2 reload + RESET 11 — FPGA V1 + S2 reload + RESET	
[31:9]	Reserved	R	--	Not implemented	

4.2.6 Pgm RESET Control

This control register allows to issue an IFC_1210 RESET sequence under control of the P2020.

The Following sequence shall be used while the P2020 control is taking control of the IFC_1210 FPGA configuration process.

a) Download “IO” FPGA configuration bit-stream (from TFTP or local NV memory)
   - Configure the “IO” FPGA with the registers “ELB_FPGA_CFGCTL” & “ELB_FPGA_CFGDAT”

b) Download “CENTRAL” FPGA configuration bit-stream (from TFTP or local NV memory)
   - Configure the “CENTRAL” FPGA with the registers “ELB_FPGA_CFGCTL” & “ELB_FPGA_CFGDAT”

c) Set the control “Seq_CONF_CMD” located in the register “ELB_FPGA_CFGCTL”

d) Select the PCIe Switch PES32NT24AG2 options in register “ELB_PCIESW_CTL”

e) Generate a Programmed RESET with control bit “Seq_RUN_CMD” located in the register “ELB_FPGA_CFGCTL”

This control register can also be used to issue a programmable IFC_1210 RESET without configuring the FPGA with the field “PGM_RSTCMD[1:0]”

ELB_PGMRST ELB : 0x002C - 0x002F				ELB Programmable RESET	
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[1:0]	P2020_BMOD[1:0]	RW	00	Programmable RESET P2020 Boot Mode. Used only with “PGM_RSTCMD”. **P2020_BMOD** — **Boot Mode** 00 — NOR Flash 01 — NAND Flash 10 — Micro SD card 11 — Reserved	

ELB_PGMRST ELB : 0x002C - 0x002F		ELB Programmable RESET			
[29:2]	Reserved	R	--	Not implemented	
[31:30]	PGM_RSTCMD[1:0]	W	00	Programmable RESET Command. This 2-bit field define the process. RSTCMD[1:0] / RESET action 00 : No action 01 : No action, + Enable PES32NT24AG2 RESET 10 : P2020 RESET 11 : P2020 + PES32NT24AG2 RESET	

4.2.7 I2C Master Interface

Following four ELB mapped registers controls the I2C Master controller. The register mapping is identical as the one instantiated in the “CENTRAL” FPGA.
Following control & status registers provides interface support for eight(8) on-board I2C Serial Bus listed in following items :
The I2C is implemented through a register based interface with limited functionality to support MPC_1200 / IFC_1210 on-board device.

- Address + Command
- Address + K*Command + N*Data_Write (N = 1 to 4, K = 1 to 4)
- Address + N*Data_Read (N = 1 to 4)

4.2.8 ELB_I2C_CTL Register

The Control register provides all control and status related to the I2C cycle generation.

ELB_I2C_CTL ELB : 0x0030 - 0x0033		I2C Control			
Bit[]	Function	R/W	Reset	Description	Comments
[6:0]	I2C_ADD[6:0]	RW	0x00	I2C 7-bit Address field	
[7]	Reserved	R		Not Used	
[10:8]	I2C_ADD[9:7]	R	0x0	I2C 10-bit Address extension field	
[15:11]	Reserved	R		Not Used	
[17:16]	I2C_CMDSIZ[1:0]	RW	0b00	I2C Byte Count for CMD field (1 to 4) 00 : 1 Byte 01 : 2 Bytes 10 : 3 Bytes 11 : 4 Bytes	
[19:18]	I2C_DATSIZ[1:0]	RW	0b00	I2C Byte Count for DATW field (1 to 4)	
[21:20]	I2C_EXECSTA[1:0]	R	0b00	I2C Interface Cycle Execution Status 00 : I2C Idle 01 : I2C Cycle Running	

ELB_I2C_CTL ELB : 0x0030 - 0x0033		I2C Control			
				10 : I2C Cycle Executed without Error 11 : I2C Cycle Executed with Error (Aborted)	
[23:22]	I2C_TRIG[1:0]	W	0b00	I2C Bus Trigger Command. 01 : I2C Cycle ADD + n* CMD 10 : I2C Cycle ADD + n* CMD +n*DATW 11 : I2C Cycle ADD + n* DATR	
[25:24]	I2C_SPEED[1:0]	RW	0b00	I2C Bus Speed Selection 00 : Standard-mode Sm (100 kbit/s) 01 : Fast-mode **Fm** (400 kbit/s) 10 : Fast-mode Plus **Fm+** (1 Mbit/s) 11 : High-speed mode Plus **Hs** (3.4 Mbit/s)	Only mode Sm (100Kbit/s) and Fm(400Kbit/s) need to be supported on MPC1200
[26]	SMB_SPEED	RW	0b0	SMB Bus Speed Selection 0 : Slow-mode (10 kbit/s) 1 : Fast-mode (100 kbit/s)	
[27]	THERM_CRITn	R	0b0	LM95535 SMB Bus T_CRIT active low status (common for both sensors)	
[28]	THERM_ALERTn	R	0b0	BMR463 + MAX5970 SMB Bus interrupt active low status (common for all three devices)	
[31:29]	I2C_Port_SEL[2;1]	RW	0x0	On-board I2C Port Selection. 000 : On board LM95535 Thermometer 001 : Reserved 010 : BMR463 DCDC + MAX5970 011 : VME P0 SMBus 100 : XMC/FMC #1 101 : XMC/FMC #2 110 : IDT PES32NT24AG2 111 : IDT8N4QV01	Provision for three additional port

The following table sums-up the IFC_1210 I2C Address for the implemented devices

Device	I2C Port	I2C Address	Reference(s)
MAX5970 (LI controller + Electronic fuse)	“010”	“011 0000”	Maxim IC MAX5970 data sheet I2C Speed 400Kbit/s
DCDC BMR463 (1.0[V])	“010”	“101 0011”	Ericsson BMR463 Technical Spec. I2C (PMBus) Speed 320Kbit/s
DCDC BMR463 (1.0[V]) Option	“010”	“010 0100”	
DCDC BMR463 (1.5[V])	“010”	“101 1011”	
DCDC BMR463 (FMC_VADJ])	“010”	“011_0011”	
LM95255 (Thermometer #1)	“000”	“100 1100”	NS LM95235 data sheet I2C(SMBus) Speed 100Kbit/s
LM95255 (Thermometer #2)	“000”	“001 1100”	
PCA9502 (MGT Clock Management)	“000”	“100 1000”	NPX PCA9502 data sheet I2C Speed 400Kbit/s
IDT 8N4QV01 (Prog. VCXO)	“111”	“110 1110”	IDT 8N4QV01 data sheet I2C Speed 400Kbit/s
XMC/FMC #1 SMBus	“100”	“XXX_XXXX”	Refer to related XMC / FMC plugged units
XMC/FMC #2 SMBus	“101”	“XXX_XXXX”	
PES32NT24AG2	“110”	“111 0101”	IDT PCIe Switch I2C Bus Slave
VME P0	“011”	“XXX_XXXX”	

Table 4.3.: IFC_1210 implemented I2C Devices

4.2.8.1 ELB_I2C_CMD Register

The Command register holds up to four (4) Command Bytes, whose be used in the subsequent I2C transaction. The number of Command Bytes is defined in the field I2C_CMDSIZ[1:0] of the I2C_CTL register.

ELB_I2C_CMD ELB : 0x0034 - 0x0037		I2C Command			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[7:0]	I2CCMD_BYTE_0	RW	0x00	I2C Bus Command Byte #0	1st Byte
[15:8]	I2CCMD_BYTE_1	RW	0x00	I2C Bus Command Byte #1	2nd Byte
[23;16]	I2CCMD_BYTE_2	RW	0x00	I2C Bus Command Byte #2	3rd Byte
[31:24]	I2CCMD_BYTE_3	RW	0x00	I2C Bus Command Byte #3	4th Byte

4.2.8.2 ELB_I2C_DATW Register

The Data Write register holds up to four (4) Data Bytes, whose be used in the subsequent I2C Write transaction. The number of Data Bytes is defined in the field I2C_DATSIZ[1:0] of the I2C_CTL register.

ELB_I2C_DATW ELB : 0x0038 - 0x003B		I2C Data Write			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[7:0]	I2C_DATW_BYTE_0	RW	0x00	I2C Bus Data Write Byte #0	1st Byte
[15:8]	I2C_DATW_BYTE_1	RW	0x00	I2C Bus Data Write Byte #1	2nd Byte
[23;16]	I2C_DATW_BYTE_2	RW	0x00	I2C Bus Data Write Byte #2	3rd Byte
[31:24]	I2C_DATW_BYTE_3	RW	0x00	I2C Bus Data Write Byte #3	4th Byte

4.2.8.3 ELB_I2C_DATR Register

The Data Read register stores four (4) Data Bytes received from subsequent I2C Read transaction.

ELB_I2C_DATR ELB : 0x003C - 0x003F		I2C Data Read			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[7:0]	I2C_DATR_BYTE_0	R	0x00	I2C Bus Data Read Byte #0	1st Byte
[15:8]	I2C_DATR_BYTE_1	R	0x00	I2C Bus Data Read Byte #1	2nd Byte
[23;16]	I2C_DATR_BYTE_2	R	0x00	I2C Bus Data Read Byte #2	3rd Byte
[31:24]	I2C_DATR_BYTE_3	R	0x00	I2C Bus Data Read Byte #3	4th Byte

4.2.9 ELB_BMRCTLRegister

This Control register allows to supply a programmable synchronisation signal (SYNC) to the four(4) on-board BMR463.

- Programmable SYNC (195 – 769 [Khz]) with 20[ns] step .

ELB_BMRCTL ELB : 0x0040 - 0x0043		BMR463 Control Register			
Bit[]	**Function**	**R/W**	**Reset**	**Description**	**Comments**
[7:0]	BMR_SYNC_CNT[7:0]	RW	0x00	This eight bit field define the SYNC frequency supplied d to the BMR463 Value: BMR463 SYNC X"00": Fixed to '0' < X"40": High Impedance >= X"40": Period = 2*Value*10[ns])	Refer to BMR563 technical doc for valid limit.
[8]	BMR_SYNC_RUN	R		This status is positioned to '1' only if BMR_SYNC_CNT[7:0] >= 0x40	
[9]	BMR_POWER_ALERT	R		This status is positioned to '1' while one of the BMR463 activate its ALERTn statue	Wired-OR signal
[31:10]	Reserved	R	0x00	Not used	

4.3 PCI Express EP

The PCIE_EP#1 IO_Bus resources are mapped on a single-port IO_Bus interface

- IO_Bus 1 KBytes Device#0 (Offset + 0x0000-0x03FF)

The PCIE_EP#1 registers provide the facilities to control the PCI Express EP Interface and general IFC_1210 board status informations.

The following table sums-up the PCIe_EP register mapping.

Offset IBUS	Size	Register_Name	Description	UG Chapter
0x000 - 0x003	0x4	**ILOC_General**	External Static Information (micro-switch & strapping)	PCIe_EP 4.2.1
0x004 - 0x007	0x4	**ILOC_Cable_0**	Reserved for implementation specific	PCIe_EP 4.2.2
0x0008 - 0x000B	0x4	**ILOC_Cable_0**	Reserved for implementation specific	PCIe_EP 4.2.3
0x000C - 0x000F	0x4	**ILOC_PONFSM**	Power_ON FSM Sequencer Status	PCIe_EP 4.2.4
0x0010 - 0x0013	0x4	**ILOC_SPI**	SPI Flash EPROM Bit programming	PCIe_EP 4.2.5
0x0014 - 0x0017	0x4	**Reserved**		
0x0018 - 0x001B	0x4	**ILOC_SIGN**	Signature FPGA date of Creation 32-bit field	PCIe_EP 4.2.7
0x001C - 0x001F	0x4	**ILOC_GENCTL**	General Control Register	PCIe_EP 4.2.8
0x0020 - 0x0023	0x4	**PCIE_MMUADD**	PCI Express INgress MMU Address pointer.	PCIe_EP 4.2.9
0x0024 - 0x0027	0x4	**PCIE_MMUDAT**	PCI Express INgress MMU Data Register	PCIe_EP 4.2.10
0x0028 - 0x002B	0x4	**PCIE_EPSTA**	PCI Express EP Status (Reserved)	
0x002C - 0x0037	0x0C	**ILOC_Reserved**	Not used	
0x038 - 0x003B	0x4	**V6_PCIEP_DSN_L**	VIRTEX-6 PCI Express EP low word Device Serial Number	PCIe_EP 4.2.19.1

Offset IBUS	Size	Register_Name	Description	UG Chapter
0x003C - 0x003F	0x4	**V6_PCIEP_DSN_L**	VIRTEX-6 PCI Express EP high word Device Serial Number	PCIe_EP 4.2.19.2
0x0040 - 0x0043	0x4	**V6_SMON_ADDPT**	VIRTEX-6 System Monitor Address Pointer	PCIe_EP 4.2.11
0x0044 - 0x0047	0x4	**V6_SMON_DAT**	VIRTEX-6 System Monitor Data Register	PCIe_EP 4.2.12
0x0048 - 0x004B	0x4	**V6_SMON_STA**	VIRTEX-6 System Monitor Status	
0x004C - 0x005F	0x14	**V6_SMON_Reserved**		
0x0060 - 0x0063	0x4	**V6_PCIEP_ADDPT**	VIRTEX-6 PCI Express EP Address Pointer for DRP and PCIE CONFIG	PCIe_EP 4.2.14
0x0064 - 0x0067	0x4	**V6_PCIEP_DRP_DAT**	VIRTEX-6 PCI Express EP DRP Data Register	PCIe_EP 4.2.15
0x0068 - 0x006B	0x4	**V6_PCIEP_CFG_DAT**	VIRTEX-6 PCI Express EP DRP Data Register	PCIe_EP 4.2.16
0x006C - 0x006F	0x4	**V6_PCIE_LINK_STA**	VIRTEX-6 PCI Express EP Link Layer CSR	PCIe_EP 4.2.17
0x0070 - 0x0073	0x4	**V6_PCIE_CFG_STA1**	VIRTEX-6 PCI Express EP Status	PCIe_EP 4.2.18.1
0x0074 - 0x0077	0x4	**V6_PCIE_CFG_STA2**		PCIe_EP 4.2.18.2
0x0078 - 0x007B	0x4	**V6_PCIE_CFG_STA3**		PCIe_EP 4.2.18.3
0x007C - 0x007F	0x4	**V6_PCIE_CFG_STA4**		PCIe_EP 4.2.18.4
0x0080 - 0x0083	0x4	**PCIE_EP_ITC_IACK**	PCIE_BE Local ITC Interrupt Acknowledge	Archi. 2.4.2.1
0x0084 - 0x0087	0x4	**PCIE_EP_ITC_CSR**	PCIE_BE ITC Interrupt Pending + Control	Archi. 2.4.2.2
0x0088 - 0x008B	0x4	**PCIE_EP_ITC_IMC**	PCIE_BE ITC Mask CLEAR Control Register	Archi. 2.4.2.3
0x008C - 0x008F	0x4	**PCIE_EP_ITC_IMS**	PCIE_BE ITC Mask SET Control Register	Archi. 2.4.2.4
0x0090 - 0x00FF	0x04	**Reserved**		
0x0100 - 0x0103	0x4	**I2C_CTL**	I2C Controller Control Register	PCIe_EP 4.2.20.1
0x0104 - 0x0107	0x4	**I2C_CMD**	I2C Controller Command Register	PCIe_EP 4.2.20.2
0x0108 - 0x010B	0x4	**I2C_DATW**	I2C Controller Data Write Register	PCIe_EP 4.2.20.3
0x010C - 0x010F	0x4	**I2C_DATR**	I2C Controller Data Read Register	PCIe_EP 4.2.20.4
0x0110 - 0x037F	0x60	**Reserved**		
0x0380 - 0x03FF	0x80	**Signature_ROM**	Defined ROM area for implementation signature	

Table 4.4 : PCIe_EP Agent_SW IO_Bus Resources

4.3.1 PCIe_EP Resources (→ specific UG)

Refer to “Tosca2_AgentSW_PCIe_EP_UG” chapter X.X

4.4 VME64x

The VME64x CSR Resources are mapped through a true dual-port interface as :

- IO_Bus Device#1 (0x0400-00x7FF) 1 KBytes
- VME64x CR-CSR Space (512 KBytes), offset determined by VME Slave Interface VME64x Geographic address (GA[4:0] & GAP) or with static option Hex Rot switch while the VME64x mode is disabled.

The VME64x Private Registers PVME_XXX provides the facilities to configure the VME64x Master/Slave Interface from internal IO_Bus infrastructure.

The following tables sums up the VME64x Private Register Mapping.

Offset IO_Bus	Size	Register_Name	Description	UG Chapter
0x0400 - 0x0403	0x4	**PVME_SLOT1**	VME64x Slot-1 related functions as Arbiter, BTO and Static option switches status.	VME64x 4.2.1
0x0404 - 0x0407	0x4	**PVME_MASCSR**	VME64x Master Port related control and status	VME64x 4.2.2
0x0408 - 0x040B	0x4	**PVME_SLVCSR**	VME64x Slave Port related control and status	VME64x 4.2.3
0x040C - 0x040F	0x4	**PVME_INTG**	VME64x Interrupt Generator	VME64x 4.2.4
0x0410 - 0x0413	0x4	**PVME_MMUADD**	VME64x INgress MMU Address pointer.	VME64x 4.2.5
0x0414 - 0x0417	0x4	**PVME_MMUDAT**	VME64x INgress MMU Data Register	VME64x 4.2.6
0x0418 - 0x041B	0x4	**PVME_ADDERR**	VME64x Address Error Register	VME64x 4.2.7
0x041C - 0x041F	0x4	**PVME_ADDERR**	VME64x Status Error Register	VME64x 4.2.8
0x0420 - 0x0423	0x4	**PVME_LOCMON**	VME64x Location Monitor Address	VME64x 4.2.9
0x0424 - 0x0427	0x4	**PVME_LOCK**	VME64x ADOH/LOCK support	VME64x 4.2.10
0x0428 - 0x042B	0x4	**PVME_RMW_MODE**	VME64x RMW Operation control	VME64x 4.2.11
0x042C - 0x042F	0x4	**PVME_RMW_ADD**	VME64x RMW Address Pointer	
0x0430 - 0x0433	0x4	**PVME_RMW_DATCMP**	VME64x RMW Data Compare	
0x0434 - 0x0437	0x4	**PVME_RMW_DATUPT**	VME64x RMW Data Update	
0x0440 - 0x0443	0x4	**PVME_GLTIM_CSR**	Global Timer Control & Status Register	VME64x 4.2.12
0x0444 - 0x0447	0x4	**PVME_GLTIM_DBG**	Global Timer Debugging support	
0x0448 - 0x044B	0x4	**PVME_GLTIM_CNT2**	Global Timer Pre-scaler 17-bit	
0x044C - 0x044F	0x4	**PVME_GLTIM_CNT1**	Global Timer Main 32-bit counter (1 [ms]	
0x0480 - 0x0483	0x4	**VME64x_ITC_IACK**	VME64X Local ITC Interrupt Acknowledge	Archi. 2.4.2.1
0x0484 - 0x0487	0x4	**VME64x_ITC_CSR**	VME64X ITC Interrupt Pending + Control	Archi. 2.4.2.2
0x0488 - 0x048B	0x4	**VME64x_ITC_IMC**	VME64X ITC Mask CLEAR Control Register	Archi. 2.4.2.3

Offset IO_Bus	Size	Register_Name	Description	UG Chapter
0x048C - 0x048F	0x4	**VME64x_ITC_IMS**	VME64X ITC Mask SET Control Register	Archi. 2.4.2.4
0x0490 - 0x075F		**Reserved**	Reserved for additional facilities	
Following registers are also mapped on VME64x CR/CSR Space				
0x0560	0x1	**VMECSR_ADER0_3**	Address Space Relocation Register VME A32 MSB	VME64x 4.2.14
0x0564	0x1	**VMECSR_ADER0_2**	Address Space Relocation Register VME A32	
0x0568	0x1	**VMECSR_ADER0_1**	Address Space Relocation Register VME A32	
0x056C	0x1	**VMECSR_ADER0_0**	Address Space Relocation Register VME A32 LSB	
0x0570 - 0x05F0		**Reserved**	VME64x Agent_SW does not incorporate any CRAM resources.	
0x05F4	0x1	**VMECSR_BCR**	VME64x CR/CSR Bit Clear Register	VME64x 4.2.15
0x05F8	0x1	**VMECSR_BSR**	VME64x CR/CSR Bit Set Register	VME64x 4.2.16
0x05FC	0x1	**VMECSR_BAR**	VME64x CR/CSR Base Address Register	VME64x 4.2.17
0x0780 - 0x07FF	0x80	**Signature_ROM**	Defined ROM area for software signature	

Table 4.5 : VME64x Agent_SW IO_Bus Resources

The VME64x CR/CSR resources are accessible from two different path (IO_Bus Slave and VME64x Slave) The resource mapping is slightly different when addressed from the internal IO_Bus or from the VME64x CR/CSR Slave interface.

The VME64x CR/CSR is defined by the ANSI/VITA 1.0-1994 [2002] and complemented with ANSI/VITA 1.1-1997 [2003] specification.

The following tables sums up the VME64x CR/CSR Register Mapping (512 KBytes area). The register mapping is described in big-endian (VME64x natural endian)

Offset CR/CSR	Size	Register_Name	Description	UG Chapter
0x0'0000 - 0x0'0FFF	0x1000	**VME_CR**	VME64 0x80 Bytes, PROM Signature as defined by VME specification Fixed read only ROM space. Refer to ANSI/VITA 1-1994(R2000)Table 2-32	
0x01000 - 0x7'0FFF	....	**Reserved**	Not used	
0x7'0000 - 7'1FFF		**IO_Bus Bridge**	4 KBytes directly mapped to the internal IO_Bus infrastructure. **Base +** 0x0000-0x03FF = Local(PCIe) TCSR 0x0400-0x07FF = VME64x TCSR 0x0800-0x0BFF = SMEM_1 TCSR 0x0C00-0x0FFF = SMEM_2 TCSR 0x1000-0x13FF = USER _1 TCSR 0x1400-0x17FF = USER _1 TCSR	
0x7'2000 - 7'3FFF		**IO_Bus Extension**	Reserved for extended IO_Bus addressing	

Offset CR/CSR	Size	Register_Name	Description	UG Chapter
			range	
0x7'F000 - 7'F3FF		**Direct VME CTL**	(Refer to previous table)	
0x7'F400 - 7'FF5F		**Reserved**		
0x7'FF63	0x1	**VMECSR_ADER0_3**	Function_0 Address Mapping Registers. Only VME A32 Slave window is supported.	
0x7'FF67	0x1	**VMECSR_ADER0_2**	Function_0 Address Mapping Registers	
0x7'FF6B	0x1	**VMECSR_ADER0_1**	Idem	
0x7'FF6F	0x1	**VMECSR_ADER0_0**	Idem	
0x7'FF70 - 0x7'FFF6		**Reserved**	Not implemented The VME64x CRAM resources is not supported.	
0x7'FFF7	0x1	**VMECSR_BCR**	VME BIT Clear Register	
0x7'FFFB	0x1	**VMECSR_BSR**	VME BIT Set Register	
0x7'FFFF	0x1	**VMECSR_BAR**	VME Geographic Base Address Register. Read only register reflecting the VME64x GA[4:0] pins.	

Table 4.6 : VME64x Agent_SW CRCSR IO_Bus resources

4.4.1 VME64x Resources (→ specific UG)

Refer to “Tosca2_AgentSW_VME64x_UG” document

2170

4.5 SMEM_IDMA

The SMEM_IDMA #1 / #2 CSR Resources mapping are provided in following table. Address offset in () are related to SMEM_IDMA #2

The SMEM-IDMA CSR Resources mapping is provided in following table.

Offset IBUS	Size	Register_Name	Description	UG Chapter
0x0800 – 0x0803 (0x0C00 – 0x0C03)	0x4	**SMEM_DDR3_CSR**	Four port DDR3 Controller Control & Status	SMEM 4.2.1
0x0804 - 0x0807	0x4	**SMEM_DDR3_ERR**	DDR3 Addressing Error status	SMEM 4.2.2
0x0808 - 0x080B	0x4	**SMEM_DDR3_DELQ**	DDR3 Programmable Delay DQ	SMEM 4.2.3
0x0840 - 0x0843	0x4	**IDMA_GCSR**	IDMA Global CSR	SMEM 4.3.1
0x0850 - 0x085F	0x4	**IDMA_PCSR**	IDMA Pipeline CSR	SMEM 4.3.2
0x0880 - 0x0883	0x4	**IDMA_ITC_IACK**	SMEMIDMA Local ITC Interrupt Acknowledge	Archi. 2.4.2.1
0x0884 - 0x0887	0x4	**IDMA_ITC_CSR**	SMEMIDMA ITC Interrupt Pending + Control	Archi. 2.4.2.2
0x0888 - 0x088B	0x4	**IDMA_ITC_IMC**	SMEMIDMA ITC Mask CLEAR Control Register	Archi. 2.4.2.3
0x088C - 0x088F	0x4	**IDMA_ITC_IMS**	SMEMIDMA ITC Mask SET Control Register	Archi. 2.4.2.4
0x0900 - 0x0903	0x4	**IDMA_RD_0_CSR**	IDMA Read Engine #0 Control&Status	SMEM 4.3.3
0x0904 - 0x0907	0x4	**IDMA_RD_0_NDES**	IDMA Read Engine #0 Next DMA_Descriptor Pointer	SMEM 4.3.4
0x0908 - 0x090B	0x4	**IDMA_RD_0_CDES**	IDMA Read Engine #0 Current DMA_Descriptor Pointer	SMEM 4.3.5
0x090C - 0x090F	0x4	**IDMA_RD_0_WCNT**	IDMA Read Engine #0 Current DMA_Descriptor Pointer	SMEM 4.3.6
0x0940 - 0x094F	0x10	**IDMA_RD_1_XXX**	IDMA Read Engine #1 Registers	SMEM 4.3.3 - 4.3.6
0x0A00 - 0x0A03	0x4	**IDMA_WR_0_CSR**	IDMA Write Engine #0 Control&Status	SMEM 4.3.3
0x0A04 - 0x0A07	0x4	**IDMA_WR_0_NDES**	IDMA Write Engine #0 Next DMA_Descriptor Pointer	SMEM 4.3.4
0x0A08 - 0x0A0B	0x4	**IDMA_WR_0_CDES**	IDMA Write Engine #0 Current DMA_Descriptor Pointer	SMEM 4.3.5
0x0A0C - 0x0A0F	0x4	**IDMA_WR_0_WCNT**	IDMA Write Engine #0 Current DMA_Descriptor Pointer	SMEM 4.3.6
0x0A40 - 0x0A4F	0x10	**IDMA_WR_1_XXX**	IDMA Write Engine #1 Registers	SMEM 4.3.3 - 4.3.6
0x0B80 - 0x0BFF	0x20	**ROM_Signature**	Defined ROM area for software signature	

Table 4.7.: SMEM–IDMA Agent_SW IO_Bus Resources

4.5.1 SMEM-IDMA Resources (→ specific UG)

Refer to “Tosca2_AgentSW_SMEMIDMA_UG” document

4.6 USER Block(s)

The IFC_1210 provides two independent user Agent_SW. Following resources description is linked to default user's block supplied by default. The resource mapping associated with the VHDL source files provide a basic design reference for customized USER Agent_SW implementation.

These USER Agent_SW integrate following basic functions to control the users' IO.

- Programmable VME P2 User's IO (Rows, A, C, D and Z) Each IO can be individually controlled as INPUT, OUTPUT or Bidirectional.
- Programmable VME P0 GPIO. The VME P0 connectors integrates sixteen(16) GPIO in addition to the high-speed Gb/s connection supporting PCI Express,...
- Programmable FMC#1. Each IO can be individually controlled as INPUT, OUTPUT or Bidirectional.
- Programmable FMC#2. Each IO can be individually controlled as INPUT, OUTPUT or Bidirectional.

The default “CENTRAL” FPGA implements two instantiation of the SUSER Example_2B

The SMEM-IDMA CSR Resources mapping is provided in following table.

Offset IBUS	Size	Register_Name	Description	UG Chapter
FMC#1 Related (Full Support)				
0x1000 – 0x1003	0x4	FMC#1 Register_00	32-bit Read only = X”12340002”	SUSER 3.2.1.1
0x1004 – 0x1007	0x4	FMC#1 Register_01	32-bit Read/Write 32-bit register	SUSER 3.2.1.2
0x1008 – 0x100B	0x4	FMC#1 Register_02	16-bit Interrupt Mode	SUSER 3.2.1.3
0x100C – 0x100F	0x4	FMC#1 Register_03	16-bit Interrupt Request	SUSER 3.2.1.4
0x1010 – 0x1013	0x4	FMC#1 Register_04	32-bit VME_P2_row_A Input	SUSER 3.2.1.5
0x1014 – 0x1017	0x4	FMC#1 Register_05	32-bit VME_P2_row_A Output	
0x1018 – 0x101B	0x4	FMC#1 Register_06	32-bit VME_P2_row_A Direction	
0x101C – 0x101F	0x4	FMC#1 Register_07	32-bit VME_P2_row_C Input	SUSER 3.2.1.6
0x1020 – 0x1023	0x4	FMC#1 Register_08	32-bit VME_P2_row_C Output	
0x1024 – 0x1027	0x4	FMC#1 Register_09	32-bit VME_P2_row_C Direction	
0x1028 – 0x102B	0x4	FMC#1 Register_0A	32-bit VME_P2_row_D Input	SUSER 3.2.1.7
0x102C – 0x102F	0x4	FMC#1 Register_0B	32-bit VME_P2_row_D Output	
0x1030 – 0x1033	0x4	FMC#1 Register_0C	32-bit VME_P2_row_D Direction	
0x1034 – 0x1037	0x4	FMC#1 Register_0D	16-bit VME_P2_row_Z Input	SUSER 3.2.1.8
0x1038 – 0x103B	0x4	FMC#1 Register_0E	16-bit VME_P2_row_Z Output	
0x103C – 0x103F	0x4	FMC#1 Register_0F	16-bit VME_P2_row_Z Direction	
0x1040 – 0x1043	0x4	FMC#1 Register_10	32-bit FRONTIO[31:0] Input	SUSER 3.2.1.9
0x1044 – 0x1047	0x4	FMC#1 Register_11	32-bit FRONTIO[63:32] Input	
0x1048 – 0x104B	0x4	FMC#1 Register_12	16-bit FRONTIO[79:64] Input	
0x104C – 0x104F	0x4	FMC#1 Register_13	32-bit FRONTIO[31:0] Output	

Offset IBUS	Size	Register_Name	Description	UG Chapter
0x1050 – 0x1053	0x4	FMC#1 Register_14	32-bit FRONTIO[63:32] Output	
0x1054 – 0x1057	0x4	FMC#1 Register_15	16-bit FRONTIO[79:64] Output	
0x1058 – 0x105B	0x4	FMC#1 Register_16	32-bit FRONTIO[31:0] Direction	
0x105C – 0x105F	0x4	FMC#1 Register_17	32-bit FRONTIO[63:32] Direction	
0x1060 – 0x1063	0x4	FMC#1 Register_18	16-bit FRONTIO[79:64] Direction + FMC add-on signals	
0x1064 – 0x1067	0x4	FMC#1 Register_19	GPIO VME_P0	SUSER 3.2.1.10
0x1080 – 0x108f	0x10	FMC#1 Register_20 … FMC#1 Register_23	ITC_16 Interrupt Controller	SUSER 3.2.1.11 - SUSER 3.2.1.14
0x1090 – 0x1093	0x4	FMC#1 Register_24	VME_P2 External V6-S6 Serializer/De-serializer	SUSER 3.2.1.15
FMC#2 Related (Only VITA57-1 FMC related				
0x1400 – 0x1403	0x4	FMC#2 Register_00	32-bit Read only = X"12340002"	SUSER 3.2.1.1
0x1404 – 0x1407	0x4	FMC#2 Register_01	32-bit Read/Write 32-bit register	SUSER 3.2.1.2
0x1408 – 0x140B	0x4	FMC#2 Register_02	16-bit Interrupt Mode	SUSER 3.2.1.3
0x140C – 0x140F	0x4	FMC#2 Register_03	16-bit Interrupt Request	SUSER 3.2.1.4
0x1440 – 0x1443	0x4	FMC#2 Register_10	32-bit FRONTIO[31:0] Input	SUSER 3.2.1.9
0x1444 – 0x1447	0x4	FMC#2 Register_11	32-bit FRONTIO[63:32] Input	
0x1448 – 0x144B	0x4	FMC#2 Register_12	16-bit FRONTIO[79:64] Input	
0x144C – 0x144F	0x4	FMC#2 Register_13	32-bit FRONTIO[31:0] Output	
0x1450 – 0x1453	0x4	FMC#2 Register_14	32-bit FRONTIO[63:32] Output	
0x1454 – 0x1457	0x4	FMC#2 Register_15	16-bit FRONTIO[79:64] Output	
0x1458 – 0x145B	0x4	FMC#2 Register_16	32-bit FRONTIO[31:0] Direction	
0x145C – 0x145F	0x4	FMC#2 Register_17	32-bit FRONTIO[63:32] Direction	
0x1460 – 0x1463	0x4	FMC#2 Register_18	16-bit FRONTIO[79:64] Direction + FMC add-on signals	
0x1480 – 0x148f	0x10	FMC#1 Register_20 … FMC#1 Register_23	ITC_16 Interrupt Controller	SUSER 3.2.1.11 - SUSER 3.2.1.14

Table 4.8.: SUSER Example 2B Agent_SW IO_Bus Resources

4.6.1 SUSER Example_2B Resources (→ specific UG)

Refer to "Tosca2_IFC_SUSER_UG" document.

4.7 ITC Controllers

The ITC16 Interrupt controllers owns four control registers. The IFC_1210 instantiates six(6) ITC16, as one in each Agent_SW.

Following table sums up the ITC16 resource mapping.

ITC Register	Local/PCIe	VME64x	SMEM#1	SMEM#2	USER#1	USER#2
IACK	0x0080	0x0480	0x0880	0x0C80	0x1080	0x1480
CSR	0x0084	0x0484	0x0884	0x0C84	0x1084	0x1484
IMC	0x0088	0x0488	0x0888	0x0C88	0x1088	0x1488
IMS	0x008c	0x048c	0x088c	0x0C8c	0x108c	0x148c

Table 4.9 : ITC Register IO_Bus mapping

In normal operation, only IACK#0 register is used. The “PCI Express MSI Generator” manages under hardware control the selection of the appropriate ITC IACK Register.

4.7.1 ITC Resources (→ specific UG)

Refer to “Tosca2_Architecture_UG” document

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