1.0 PURPOSE

The purpose of this technical specification is to define from a functional stand point all the characteristics, properties and operation of the Aquarius I computer console.

Component tolerances mentioned here are for reference only, the appropriate component spec should be used for qualification of parts.

Aquarius Home Computer System is shown in Appendix B.

2.0 RELATED DOCUMENTS

Aquarius electrical schematic	5931-9229
Z80 CPU Spec	5931-0020
PLA 1 CRT Controller Spec	5931-0060
PLA 2 Software lock & Bidirectional Buss Driver	5931-0070

3.0 DESIGN REQUIREMENTS

3.1 Physical Requirements

3.1.1	Size	13" X 6" X 1 3/4"
3.1.2	Keyboard	
3.1.2.1	Actuator Type	Rubber - Tactile
3.1.2.2	Actuator	Peak Force: 65g @ .8mm-Contact @-1mm
3.1.2.3	# of I/O Mapped Keys	48 (6x8 Matrix)
3.1.2.4	Reset Key	Hardwired (Protected from Accidental Actuation)
3.1.2.5	Arrangement	QWERTY
3.1.2.6	Switch Type	Membrane
3.1.3	Switches & Indicators	
3.1.3.1	Power ON/OFF	Rocker (3P2T)-Right Side
3.1.3.2	Channel Selection	Slide (SPST)-Rear Panel
3.1.3.3	Power Indicator	LED, Front Panel (Green)

3.1.4 I/O Connectors		
	3.1.4.1 Cassette	5 pin DIN
	3.1.4.2 Printer	3.5mm Stereo Phone Jack
	3.1.4.3 TV	RCA Phone Jack
	3.1.4.4 Cartridge/Expansion	22 X 2 Edge Connector
3.2 Electrical Requirements		
3.2.1 Memory Capacity		
	3.2.1.1 RAM - On Board	4K (2K user; 1K color, 1K display)
	3.2.1.2 ROM - Basic & OP Sys	8K
	3.2.1.3 ROM - Character Set	2K
	3.2.1.4 RAM Expansion	Up to 48K in 16K Blocks
	3.2.1.4.1 Maximum User RAM	52K (Fully Expanded)
3.2.2 Display		
	3.2.2.1 Number of Colors	16 (8 + 8 Half Tones, background, foreground independent)
	3.2.2.2 Screen Format	40 columns X 24 rows
	3.2.2.3 Graphics Resolution	80 X 72
	3.2.2.4 PEL Size	4 X 3 / 4 X 2 / 4 X 3
3.2.3 Character Set		
	3.2.3.1 Number of Characters	256 (128 ASCII + 128 Graphics)
	3.2.3.2 Character Box	8 X 8
	3.2.3.3 Capitals	5 X 7
	3.2.3.4 Lower Case	5 X 5, 1 dot descender. 2 dot extender
3.2.4 Language		Microsoft 8K Basic
	3.2.4.1 Precision	6 digit

3.2.5	Keyboard	
	3.2.5.1 Language Support	Two Key (CTL + 1 additional key for basic commands - 42 commands possible)
3.2.6	Software Security	Proprietory, IC PLA-2
3.2.7	Television Interface	
	3.2.7.1 Modulation	NTSC - AM525 Lines, or PAL - 625 Lines
	3.2.7.2 Channel	3 or 4 - Switchable, or VHF Channel 36
	3.2.7.3 Output Z	75 OHMS
	3.2.7.4 Output Level	3mV RMS maximum
3.2.8	Printer Interface	
	3.2.8.1 Rate	1200 Baud
	3.2.8.2 Logic	RS 232 Serial, Data, CTS, +12V/-12V
3.2.9	Cassette Interface	
	3.2.9.1 Rate	600 Baud
	3.2.9.2 Tones	833 HZ, 1667 HZ
	3.2.9.3 Input Z	82 OHMS
	3.2.9.4 Output Z	2400 OHMS
	3.2.9.5 Output Level	$50m^{V}$ p.p.
3.2.10	Sound	
	3.2.10.1 Number of Channels	1
	3.2.10.2 Range	100HZ to 10,000 HZ
	3.2.10.3 Output	FM, Channel 3 or 4

3.2.11	Power Supply	
	3.2.11.1 Type	Linear
	3.2.11.2 Voltages (DC)	+12V ± 0.6V @ 150mA max. Typical 130mA
		-19V ± 3V @ 10mA max. Typical 0mA
		+5V ± 0.25V @ 1200mA max. Typical 420mA
	3.2.11.3 Peripheral Supply	+5V ± 0.25V @ 400mA max.
3.2.12	Extension Port	
	3.2.12.1 Logic	TTL Compatible
	3.2.12.2 Load Capability	Address - 1TTL load
		Data - 3TTL load
		Control - 1TTL load
	3.2.12.3 Lines Provided	44 Total
		- 16 Address
		- 8 Data
		- 16 Control
		- 1 Sound
		- +5V (one)
		- 2 Gnd

PIN NUMBER	PIN NAME	SYMBOL	DESCRIPTION
1	Composite Sync	$\overline{\text{CSYNC}}$	Output, active low. Video synchronization timing signal.
2	Sound	SOUND	Input/Output, active high. External sound input or internal sound output.
3	Interrupt Request	$\overline{\text{INT}}$	Input, active low. The INT signal is produced by I/O devices.
4	Bus Request	$\overline{\text{BUSRQ}}$	Input, active low. It is used to allow other devices to take control over the processor address bus, data bus and 3-state output control signals.
5	Reset	$\overline{\text{RESET}}$	Input/output, active low. When pull low, the Aquarius is reset. Interface may monitor or generate a reset
6	Machines Cycle one	$\overline{\text{M1}}$	Output, active low. M1 indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
7	Refresh	$\overline{\text{RFSH}}$	Output, active low. RFSH indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus.
8	Clock	$\overline{\text{Ø}}$	Output, active high. Standard 3.579545MHz microprocessor clock signal.
11	Chip Enable	$\overline{\text{CE}}$	Output, active low. Active when the computer addresses locations CØØØ-FFFF.
23,21,19,17 15,13,12,14 16,18,20,22 24,36,10,9	Address Bus	AØ-A15	3-State Output, active high. 16-bit address bus line.

PIN NUMBER	PIN NAME	SYMBOL	DESCRIPTION
26-33	Data Bus	DEØ-DE7	3-State input/output, active high. 8-bit, bidirectional data bus signals.
25	Power Supply	+5V	+5 Volts
35	Memory Read	$\overline{RD}$	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device.
37	Memory Write	$\overline{WR}$	3-State output, active low. The Memory Write signal indicates that the processor data bus is holding valid data to be stored in the addressed memory or I/O device.
38	Memory Request	$\overline{MREQ}$	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
39	Non-Maskable Interrupt	$\overline{NMI}$	Input, active low. $\overline{NMI}$ vectors the processor to subroutine at ØØ66.
40	Wait	$\overline{WAIT}$	Input/output, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. This pin has an internal 4.7K ohms pullup for wire-ORed Input. $\overline{WAIT}$ may also act as an output since it provides a 894.88KHz clock with 25% duty cycle.
41	Halt State	$\overline{HALT}$	Output, active low. The processor will execute NOP's while halted.
42	Bus Acknowledge	$\overline{BUSAK}$	Output, active low. $\overline{BUSAK}$ indicates to the requesting device the processor address bus, data bus and 3-state control bus signal have entered high impedance state.

PIN NUMBER	PIN NAME	SYMBOL	DESCRIPTION
43	Input/Output Request	$\overline{\text{IORQ}}$	3-State Output, active low. $\overline{\text{IORQ}}$ indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. It is also generated concurrently with M1 during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.
34, 44	Power GND	GND	System electrical ground.

4.0 FUNCTIONAL CHARACTERISTICS

4.1 Operating Systems

The Aquarius I can operate in the following two modes:

(i) 8K ROM BASIC

(ii) CP/M

4.1.1 Mode Switching

- Mode switching is accomplished by writing to bit zero of I/O location FD(HEX). Bit set indicates CP/M mode and bit reset indicates BASIC mode. The bit is not readable and is reset after power on.
  Set = Logic '1', Reset = Logic 'Ø'.

4.2 Memory Allocation

The Aquarius has 2 memory map modes, one is ROM BASIC mode (Fig. 4.1) another is CP/M mode Fig. 4.2).

4.3 System Configurations

The block diagram is shown in Fig. 4.3.

Refer to Schematics (RELATED DOCUMENTS 2.0) for the following descriptions.

4.3.1 Circuit Description

The Aquarius Computer is a Video based unit with a built-in keyboard. The video timing and CPU synchronization are generated by a custom gate array PLA-1 (U7). The master clock frequency of PLA-1 is 7.15909 MHz and it is divided internally in the PLA to provide the 3.579545 MHz CPU clock. The video scanning rate is one eight of the master clock frequency.

The CPU (U1) is linked directly to a 64K ROM (8K X 8) (U2) which contains the Basic Program and Service Routines. It is then linked indirectly to two 16K RAM's (2K X 8) (U3, U4) through buffers in PLA-1.

These RAM's are used for the operation of the Basic and also to store the video display. They are specially mapped so that the video information (screen and color data) are seen by the CPU as a continuous 2K memory starting from hex 3000 to hex 37FF. These two 1K video blocks are physcially apart so they can be scanned separately. The user program space extends from hex 3800 to hex 39FF in the base unit. User space can be expanded an additional 48K (Hex 4000 to FFFF) with the appropriate peripherals.

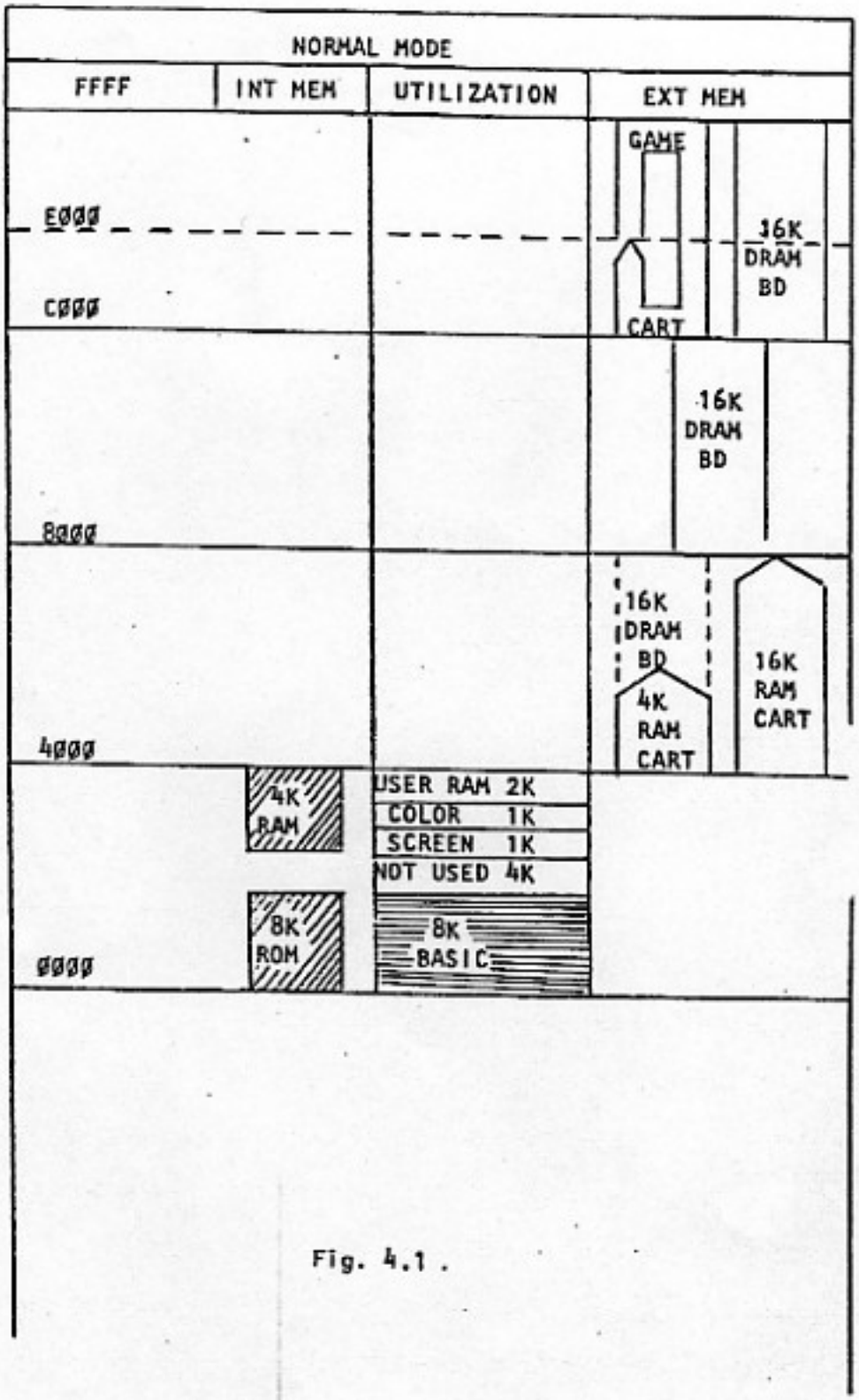
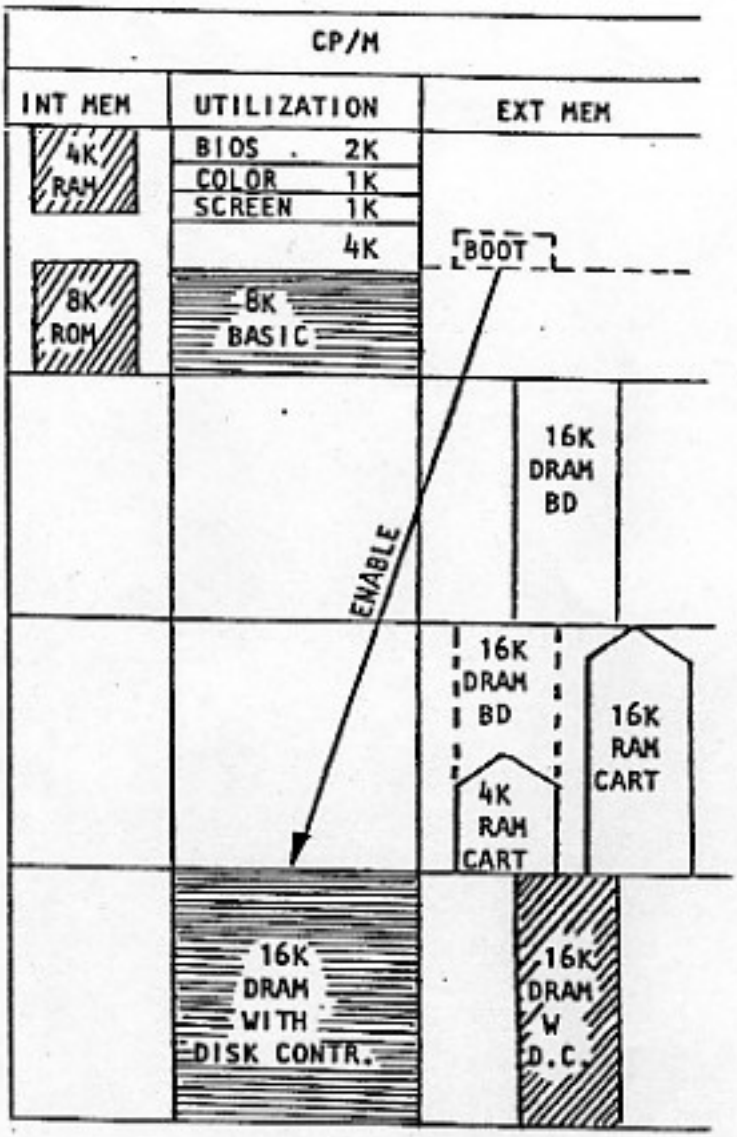

NORMAL MODE
FFFF
INT MEM
UTILIZATION
EXT MEM
GAME
CART
16K DRAM BD
E000
C000
16K DRAM BD
8000
16K DRAM BD
4K RAM CART
16K RAM CART
4000
4K RAM
USER RAM 2K
COLOR 1K
SCREEN 1K
NOT USED 4K
8K ROM
8K BASIC
0000

Fig. 4.1 .



. 8K BASIC ROM SHIFTED TO C000.

. ENABLE OF LOWER 16K MEMORY BLOCK CONTROLLED BY BOOT

Fig. 4.2

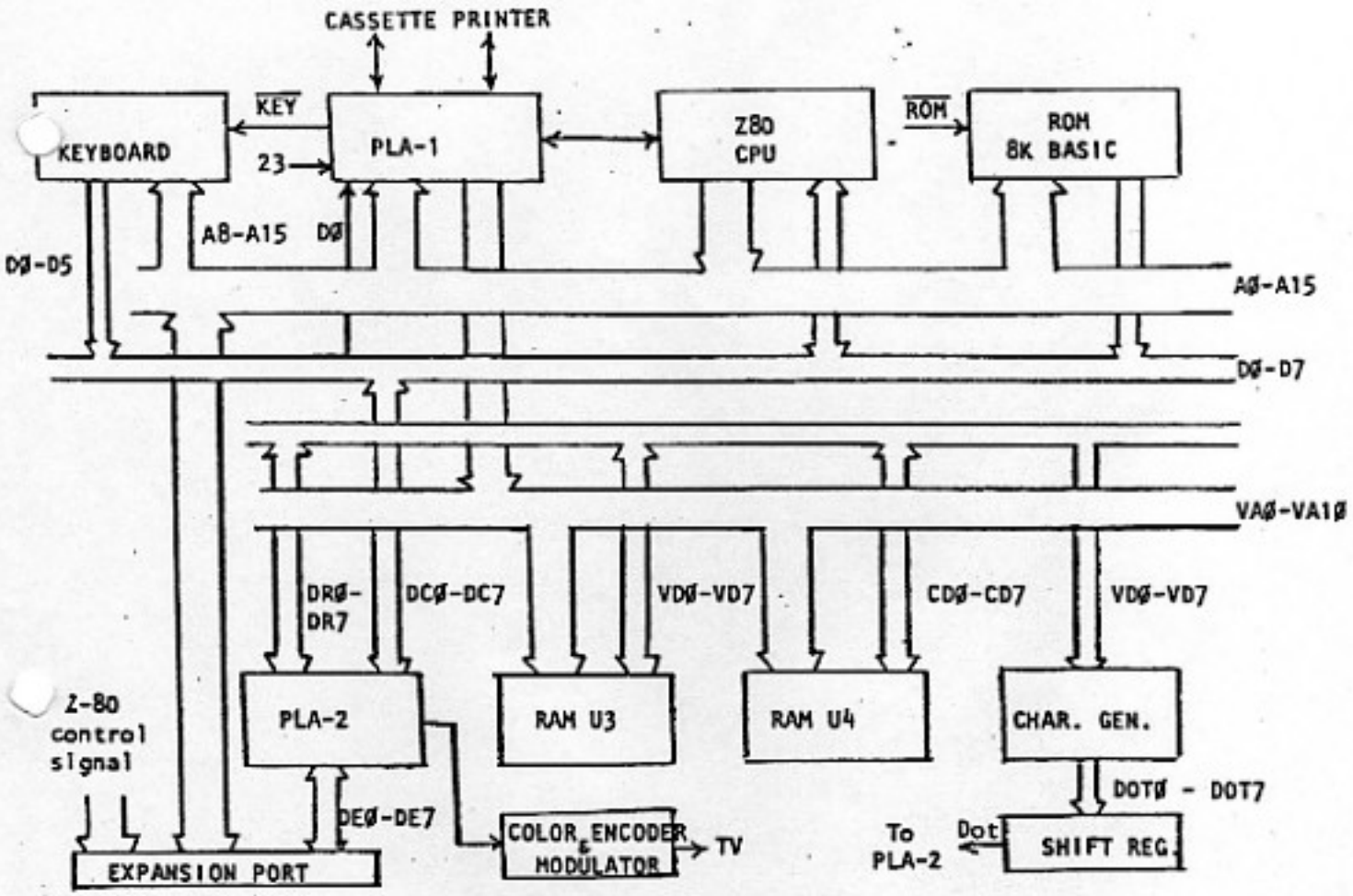


Fig. 4.3 Aquarius I System Block Diagram

4.3 System Configurations (continued)

The data output of the Screen RAM (U3) is routed to a character Generator (U5) stored in a 16K ROM (2K X 8). The output of the Character Generator is in turn connected to a shift register for video output.

Data from the color RAM (U4) is fed to another custom gate array PLA-2 (U8) which generates the R,G,B and INV signals. The PLA-2 also consists of a data scrambler or software lock for software protection.

The color encoder section consists of U12, U13, and U14 which produce a standard NTSC composite video for modulation.

4.4 PLA's

There are two custom LSI arrays in the Aquarius - PLA-1 and PLA-2.

4.4.1 PLA-1

The block diagram is shown in Fig. 4.4, which consists of:

- CRT Controller
- I/O Interface
- Address Buffers and Decoders

4.4.1.1 CRT Controller

The PLA-1 provides the timing and controls signals necessary for generating and displaying TV video information in the NTSC and PAL format. The PLA-1 accepts a single 7.1591 MHz input clock and generates various timing outputs including composite sync, composite blanking and color burst flag. Screen RAM address counters are also provided to give a 40 columns by 24 rows display. Alphanumeric and graphic characters are generated on an 8 X 8 matrix.

4.4.1.2 PLA-1 provides I/O interface logic to on-board I/O.

4.4.1.2.1 I/O Mapping

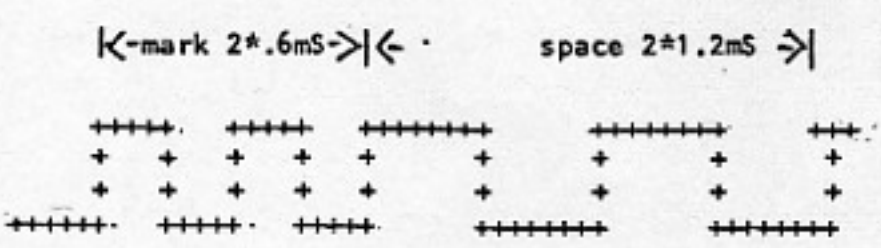
I/O Address (HEX)	Function
ØØ ↓ 7D	Not used
7E	Modem
7F	Modem
8Ø ↓ E7	Not used
E8 ↓ EA	Floppy disk interface
EB ↓ EF	Not used
FØ ↓ F7	Reserved for use in the entertainment module for addressing the sound-generation chip and the joy-sticks.
F8 ↓ FB	Not used

I/O Address (HEX)	Function	I/O bit(s)
FC	Cassette and sound port output	DØ (write)
	cassette port input	DØ (read)
FD	CP/M mode memory mapper	DØ (write)
	vertical sync signal	DØ (read)
FE	1200 bps serial printer	DØ (write)
	clear to send status	DØ (read)
FF	Software lock pattern	DØ-D7 (write)
	keyboard port	DØ-D5 (read)

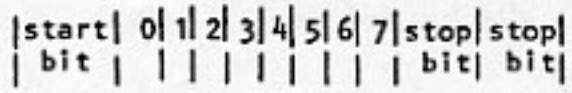
4.4.1.2.1.1 Cassette output (write)

The format employed is very similar to conventional serial interface format. One data byte on cassette consists of one start bit of 0, 8 data bits and 2 stop bits of 1. A mark is represented by 2 full cycles of square wave with period 0.6mS, a space also has 2 cycles but with a period of 1.2mS. In cassette interfacing we have to minimize problems due to DC offset thus square wave pattern was chosen. Prior to any data block transfer a group of sync bytes are sent for data recovery synchronization. In BASIC there are 16 sync bytes of FF and there must be 6 consecutive sync bytes to be read back for sync verification.

bit format



byte format



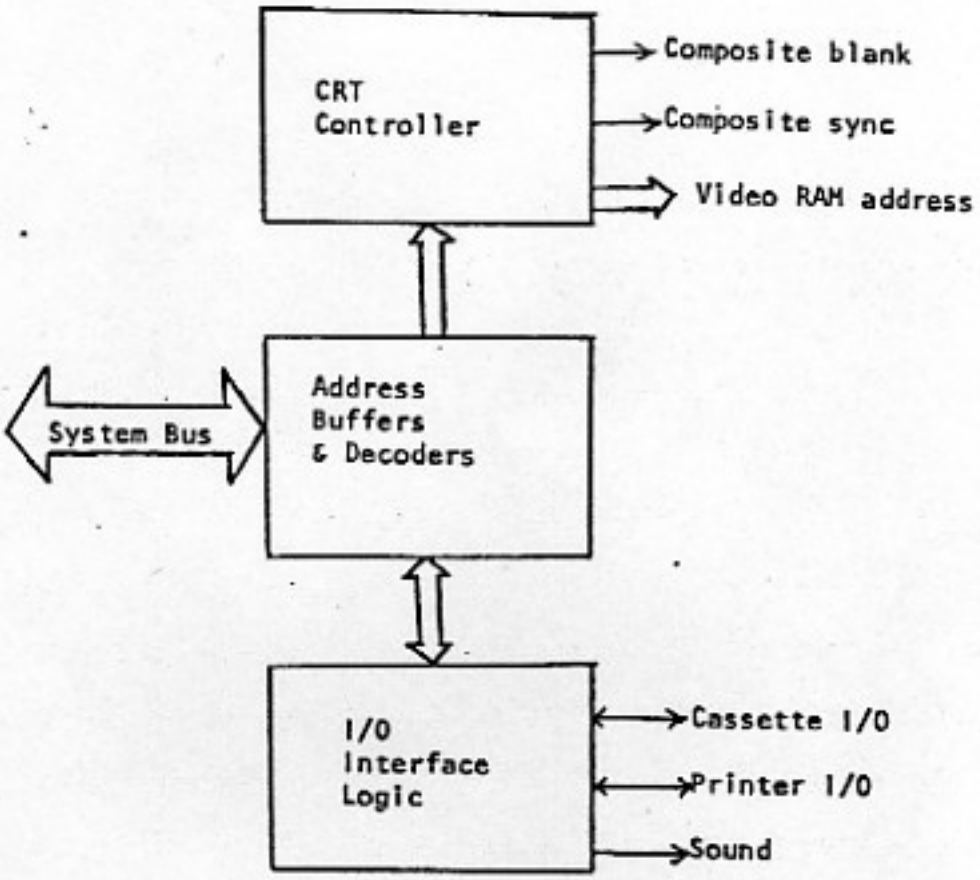


Fig. 4.4 PLA-1 Block Diagram

4.4.1.2.1.2 Cassette input (read)

To read stored data from cassette the program should look at bit zero of the cassette input port and measure the time difference between leading edges or trailing edges. This is to prevent DC level shifting from altering pulse width of data. The program should then look for sync bytes for data synchronization before data block transfer. If there is any task that must be performed during cassette loading, the maximum allowable time to do the job after reading one byte from cassette, must be less than 80% of the period of a mark cycle. Control must be returned at that time to the cassette routine in order to maintain data integrity.

4.4.1.2.1.3 Sound port (write)

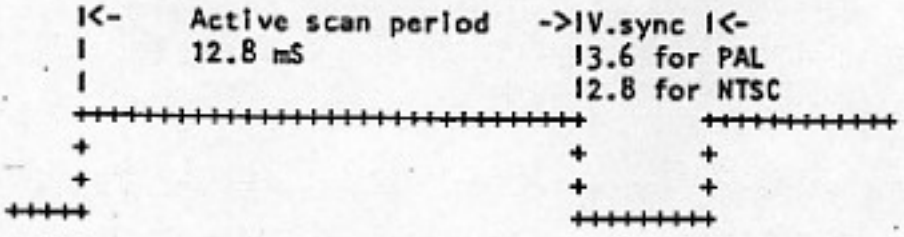
Sound and cassette use a common pin. Therefore signal to cassette will appear on audio output. Sound port is a simple one big I/O and therefore it must be toggled at a specific rate under software control.

4.4.1.2.1.4 Memory mapper (write)

Bit D0 of this port controls the swapping of the lower 16K block in the memory map with the upper 16K. A 1 in this bit indicates swapping. A 0 in this port means no swapping. This bit is reset after power up initialization.

4.4.1.2.1.5 Vertical sync (read)

The current state of the vertical sync will appear on bit 0 during a read of this port. The waveform and timing spec is shown as follows:



4.4.1.2.1.6 Printer port (write)

This is a single bit I/O at D0, it will perform as a serial output port under software control. Since timing is done by software therefore the baud rate is variable. In BASIC this is a 1200 baud printer port for the 40 column thermal printer.
CAUTION!!!
The printer output is initiallzed to logical zero by hardware reset. Therefore it must be written with a one under software control after power on reset.

4.4.1.2.1.7 Printer handshaking port (read)

Port FE when read, presents the clear to send status from PRNHASK pin at bit D0. A 1 indicates the printer is ready, 0 means not ready.

4.4.1.2.1.8 Software lock:

Writing this port with a 8 bit value will set the software scrambler pattern. The data that appears on the output side will be the result of the input bus EX-ORed with this pattern, bit by bit.

4.4.1.2.1.9 Keyboard port:

This port is 6 bits wide, when read, it returns the row data from the keyboard matrix.

The keyboard is usually scanned in the following manner:

The keyboard is a 6 row by 8 column matrix. The column is connected to the higher order address bus A15-A8. When Z80 executes its input instruction sets, either the current content of the accumulator (A) or the content of register (B) will go to the higher order address bus. Therefore the keyboard can be scanned by placing a specific scanning pattern in (A) or (B) and reading the result returned on rows.

4.4.1.2.2 Port Initialization Procedure

4.4.1.2.2.1 Cassette Port:

Needs no initialization

4.4.1.2.2.2 Memory Mapper:

Do not write to this bit unless block switching is desired for CP/M applications.

4.4.1.2.2.3 Printer Port:

MUST be initialized to logical 1 prior to printing.

4.4.1.2.2.4 Software Lock:

Depends on the desired function. Usually a game cartridge gains control from BASIC, at this point the lock is already prepared and does not need further intervention. Writing the software lock unintentionally simply means program crash.

4.4.1.3 Address Buffers and decoders

Buffered address bus lines (AØ - A1Ø) are provided for the two internal RAM's through PLA-1.

Memory and I/O mapping are allocated by decoders in PLA-1.

4.4.2 PLA-2

The block diagram for PLA-2 is shown in Fig. 4.5 which consists of a software lock and a multiplexer for color generation.

4.4.2.1 Software Lock

The software is a scrambler built between the CPU and external interface. The scrambling pattern is contained in port FFand is not readable.- CPU data output to external bus will be EX - ORed with this pattern in a bit by bit fashion to generate the real data on external bus. By the same mechanism,

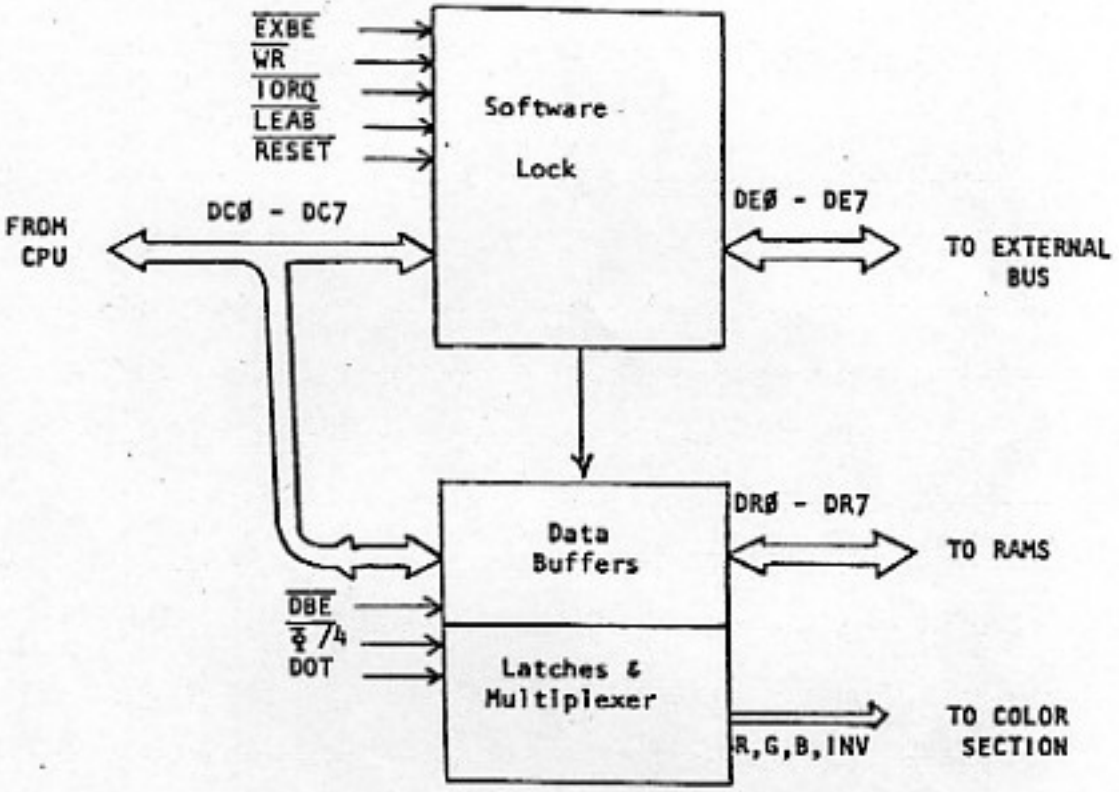


Fig. 4.5 PLA-2 Block Diagram

data from external bus is also EX-ORed with this pattern and read by CPU. Therefore if the external device is RAM, the software lock simply has no effect as long as the scrambling pattern remains unchanged. For I/O operation the pattern is gated to Ø and thus scrambling action is nullified. In BASIC operation the scrambling pattern is generated by a random number routine. For game cartridge, the lock pattern is generated from data in the game cartridge itself.

Internal and external space definition:
Any non-onboard element will be decoded as external.
Onboard elements are:

8K ROM
4K RAM
I/O location FC - FF

4.4.2.2 Color Generation

Data from the color section is fed to an 8-bit latch, where it is multiplexed for foreground and background color switching, as controlled by the output of the shift register.

4.4.3 Screen RAM

Text page starts from 3ØØØ (Hex) to 33FF in Basic mode and FØØØ to F3FF in CP/M mode.

Color page is offset by 1K, that is 34ØØ to 37FF for BASIC mode and F4ØØ to F7FF in CP/M mode.

4.4.3.1 Characters Format

The characters can be displayed on-screen in a matrix of 40 columns by 24 rows.

Characters are in ASCII plus graphic characters and special symbols. All characters are printable on screen but the (PUTCRT) routine in BASIC will filter out certain control characters such as return, linefeed, clear screen and backspace.

4.4.3.2 Color Format

The background and foreground colors of a single character on screen can be specified as follows:

bits

7 6 5 4	3 2 1 0
foreground	background

Bit 0 thru 2 and bit 4 thru 6 are chroma control bits and bit 3 and 7 are luminance control bits. If bit 3 or 7 is high the luminance of the corresponding field will be reduced by half, thus creating 8 colors and 8 half tone colors.

REMARKS: The first row of characters starts at 3028 or F028 (40 characters from the beginning of character RAM). The first RAM locations (3000 and 3400 or F000 and F400) control the frame background of the screen.

5.0 USER INTERFACE

5.1 Installing the Aquarius Computer

A. Make sure your computer is turned off.

B. Connect the computer to TV, plug in AC adaptor, set the Antenna Switch Unit to TV and determine that the set works correctly on broadcast stations.

C. Set the Antenna Switch Unit to COMPUTER. Insert the Cartridge (if any) into the Expansion port.

D. Turn your computer ON.

6.0 TESTING

This section describes the main test parameters for the AQUARIUS I COMPUTER. Detailed test specifications and procedures are covered in Functional Specification for Aquarius Port Test. (Appendix A)