Micro/Elf

Quick Reference Card

Register Summary

D	8-bit	Data Register
DF	1-bit	Data Flag (carry/borrow)
R	16x16-bit	General Register Array
P	4-bit	Program Pointer
X	4-bit	Data Pointer
N	4-bit	Low nybble of instruction byte
I	4-bit	High nybble of instruction byte
Q	1-bit	Output Flip-Flop
IE	1-bit	Interrupt Enable

Special Registers

R(0)	DMA Pointer
R(1)	Interrupt Vector
R(2)	Stack during interrupts

ASCII Codes

```
   0 1 2 3 4 5 6 7 8 9 A B C D E F
20   ! " # $ % & ' ( ) * + , - . /
30 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
40 @ A B C D E F G H I J K L M N O
50 P Q R S T U V W X Y Z [ \ ] ^ _
60 ` a b c d e f g h I j k l m n o
70 p q r s t u v w x y z { | } ~ del
```

State Codes

State	SC1	SC0
S0 Fetch	L	L
S1 Execute	L	H
S2 DMA	H	L
S3 Interrupt	H	H

Modes

Mode	Clear	Wait
Load	L	L
Reset	L	H
Pause	H	L
Run	H	H

Instruction Set

0N	LDN	Load via RN
4N	LDA	Load Advance via RN
F0	LDX	Load via RX
72	LDXA	Load Advance via RX
F8	LDI	Load Immediate
5N	STR	Store via RN
73	STXD	Store via RX and decrement
1N	INC	Increment
2N	DEC	Decrement
60	IRX	Increment RX
8N	GLO	Get Low register N
AN	PLO	Put Low register N
9N	GHI	Get High register N
BN	PHI	Put High register N
F1	OR	Logical OR
F9	ORI	OR Immediate
F3	XOR	Logical XOR
FB	XRI	XOR Immediate
F2	AND	Logical AND
FA	ANI	AND Immediate
F6	SHR	Shift Right
76	SHRC	Shift Right with Carry
FE	SHL	Shift Left
7E	SHLC	Shift Left with Carry
F4	ADD	Add
FC	ADI	Add Immediate
74	ADC	Add with Carry
7C	ADCI	Add with Carry Immediate
F5	SD	Subtract D
FD	SDI	Subtract D Immediate
75	SDB	Subtract D with Borrow
7D	SDBI	Subtract D with Borrow Immediate
F7	SM	Subtract Memory
FF	SMI	Subtract Memory Immediate
77	SMB	Subtract Memory with Borrow
7F	SMBI	Subtract Mem with Borrow Immed.
30	BR	Branch
38	NBR	No Branch
32	BZ	Branch on Zero
3A	BNZ	Branch on Non-Zero
33	BDF	Branch on DF=1
3B	BNF	Branch on DF=0
31	BQ	Branch on Q=1
39	BNQ	Branch on Q=0
34	B1	Branch on EF1=1
3C	BN1	Branch on EF1=0
35	B2	Branch on EF2=1
3D	BN2	Branch on EF2=0
36	B3	Branch on EF3=1
3E	BN3	Branch on EF3=0
37	B4	Branch on EF4=1
3F	BN4	Branch on EF4=0
C0	LBR	Long Branch
C8	NLBR	No Long Branch
C2	LBZ	Long Branch on Zero
CA	LBNZ	Long Branch on Non-Zero
C3	LBDF	Long Branch on DF=1
CB	LBNF	Long Branch on DF=0
C1	LBQ	Long Branch on Q=1
C9	LBNZ	Long Branch on Q=0
CE	LSZ	Long Skip on Zero
C6	LSNZ	Long Skip on Non-Zero
CF	LSDF	Long Skip on DF=1
C7	LSNF	Long Skip on DF=0
CD	LSQ	Long Skip on Q=1
C5	LSNQ	Long Skip on Q=0
CC	LSIE	Long Skip on IE=1
00	IDL	Idle
C4	NOP	No Operation
DN	SEP	Set P
EN	SEX	Set X
7B	SEQ	Set Q=1
7A	REQ	Set Q=0
78	SAV	Save T to Memory
79	MARK	Push X,P to stack
70	RET	Return, IE=1
71	DIS	Return, IE=0
61	OUT1	Output port 1
62	OUT2	Output port 2
63	OUT3	Output port 3
64	OUT4	Output port 4
65	OUT5	Output port 5
66	OUT6	Output port 6
67	OUT7	Output port 7
69	INP1	Input port 1
6A	INP2	Input port 2
6B	INP3	Input port 3
6C	INP4	Input port 4
6D	INP5	Input port 5
6E	INP6	Input port 6
6F	INP7	Input port 7

Opcode Table

	0	1	2	3	4	5	6	7
0	IDL	LDN	LDN	LDN	LDN	LDN	LDN	LDN
1	INC	INC	INC	INC	INC	INC	INC	INC
2	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC
3	BR	BQ	BZ	BDF	B1	B2	B3	B4
4	LDA	LDA	LDA	LDA	LDA	LDA	LDA	LDA
5	STR	STR	STR	STR	STR	STR	STR	STR
6	IRX	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
7	RET	DIS	LDXA	STXD	ADC	SDB	SHRC	SMB
8	GLO	GLO	GLO	GLO	GLO	GLO	GLO	GLO
9	GHI	GHI	GHI	GHI	GHI	GHI	GHI	GHI
A	PLO	PLO	PLO	PLO	PLO	PLO	PLO	PLO
B	PHI	PHI	PHI	PHI	PHI	PHI	PHI	PHI
C	LBR	LBQ	LBZ	LBDF	NOP	LSNQ	LSNZ	LSNF
D	SEP	SEP	SEP	SEP	SEP	SEP	SEP	SEP
E	SEX	SEX	SEX	SEX	SEX	SEX	SEX	SEX
F	LDX	OR	AND	XOR	ADD	SD	SHR	SM

8	9	A	B	C	D	E	F
LDN	LDN	LDN	LDN	LDN	LDN	LDN	LDN
INC	INC	INC	INC	INC	INC	INC	INC
DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC
NBR	BNQ	BNZ	BNF	BN1	BN2	BN3	BN4
LDA	LDA	LDA	LDA	LDA	LDA	LDA	LDA
STR	STR	STR	STR	STR	STR	STR	STR
	INP1	INP2	INP3	INP4	INP5	INP6	INP7
SAV	MARK	REQ	SEQ	ADCI	SDBI	SHLC	SMBI
GLO	GLO	GLO	GLO	GLO	GLO	GLO	GLO
GHI	GHI	GHI	GHI	GHI	GHI	GHI	GHI
PLO	PLO	PLO	PLO	PLO	PLO	PLO	PLO
PHI	PHI	PHI	PHI	PHI	PHI	PHI	PHI
NLBR	LBNQ	LBNZ	LBNF	LSIE	LSQ	LSZ	LSDF
SEP	SEP	SEP	SEP	SEP	SEP	SEP	SEP
SEX	SEX	SEX	SEX	SEX	SEX	SEX	SEX
LDI	ORI	ANI	XRI	ADI	SDI	SHL	SMI

Timing Diagrams