SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2513 is a high speed 2560-bit Static ROM organized as 64x8x5. A standard 7x5 dot matrix fits well in the 2513. The product uses +5V, -5V and -12V power supplies, TTL level interface signals and Tri-State Outputs for direct, low cost interfacing with TTL, DTL, CMOS and 2500 Series MOS.

FEATURES

- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR BUSSING CAPABILITY
- 2513/CM2140 ASCII FONT STANDARD (7 X 5)
- 24-PIN DIP
- P-MOS SILICON GATE TECHNOLOGY

APPLICATIONS

RASTER SCAN CRT DISPLAYS (ROW OUTPUT)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' P channel Silicon Gate Process allows the design and production of higher functional density and operating speed than other techniques.

SILICONE PACKAGING

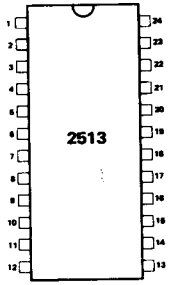
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers.

BIPOLAR COMPATIBILITY

All inputs of the 2513 can be driven directly by standard TTL voltage levels. The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)

N/I PACKAGE



1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.	Ground	15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

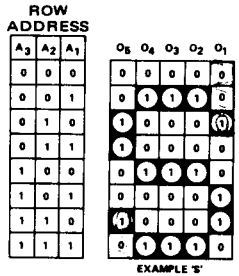
PART IDENTIFICATION TABLE

PART	ORGANIZATION	PROGRAMMING
2513N/I CM2140	64X8X5	ASCII Font
2513N/I CMXXXX	64X7X5 64X8X5	Custom

N PACKAGE = 24 PIN SILICONE DIP

I PACKAGE = 24 PIN CERAMIC DIP

CHARACTER FORMAT



CHARACTER ADDRESS

	A4	A5	A6	A7	A8	A9
ASCII CHARACTER	1	1	0	0	1	0

MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @T_A 70°C	730mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

NOTES

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = −5V ±5%; V_{GG} = −12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7)

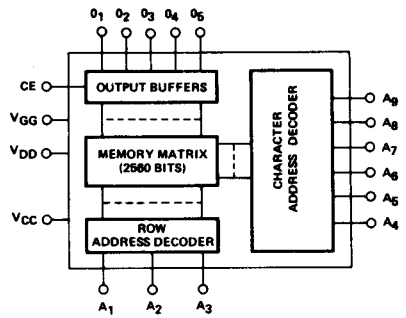
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C $V_{CE} = V_{CC}$
I_{DD}	V_{DD} Power Supply Current		12	15	mA	Outputs Open
I_{GG}	V_{GG} Power Supply Current		10	15	mA	Outputs Open $V_{CE} = V_{CC}$
V_{IL}	Input Logic "0"			+0.6	V	Note 8
V_{IH}	Input Logic "1"	+3.4		5.3	V	Note 8

AC CHARACTERISTICS

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$; $V_{DD} = -5V \pm 5\%$; $V_{GG} = -12V \pm 5\%$; unless otherwise noted.

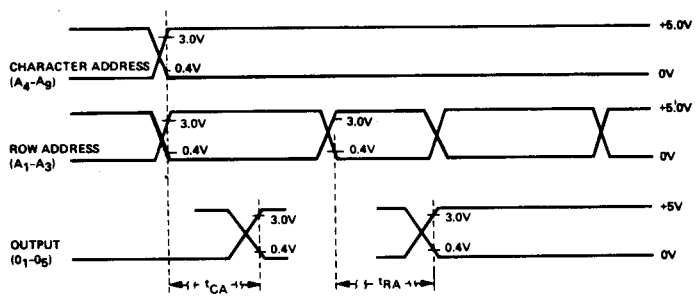
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		0.4	V	One TTL Load
V_{OH}	Output Logic "One"	3.0			V	One TTL Load
$^tCA_{(CM2140)}$	Character Access Time		500	600	ns	See AC Test Setup
^tRA	Row Access Time (A_1 - A_3)		450	500	ns	See AC Test Setup
^tCE	Chip Enable to Output		150		ns	
C_{IN}	Address Input Capacitance			10	pF	f = 1 MHz, V_{IH} = V_{CC}, 25mV p - p

BLOCK DIAGRAM



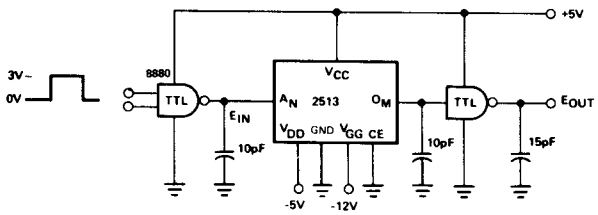
CE	OUTPUT
0	DATA
1	OPEN

TIMING DIAGRAM



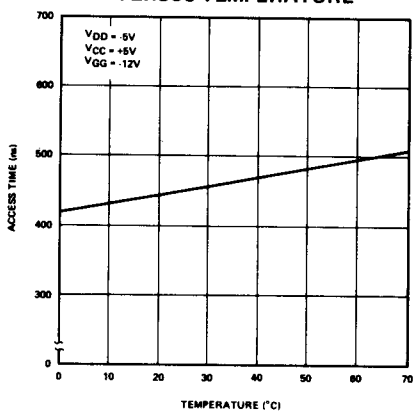
^tCA = Character Access Time
^tRA = Row Access Time

AC TEST SETUP

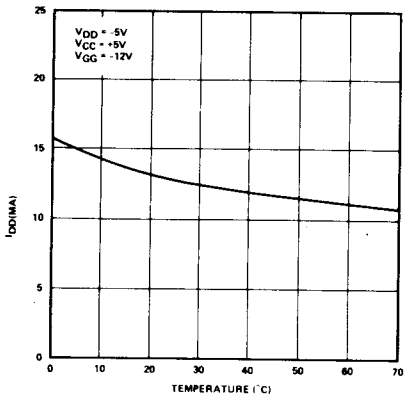


TYPICAL CHARACTERISTIC CURVES

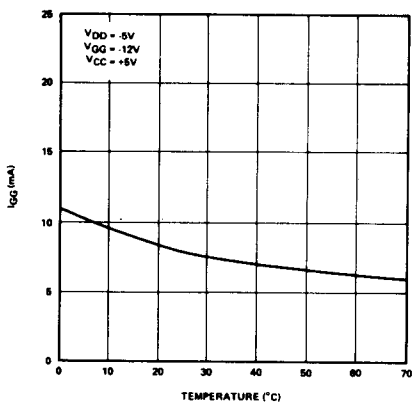
TYPICAL ACCESS TIME VERSUS TEMPERATURE



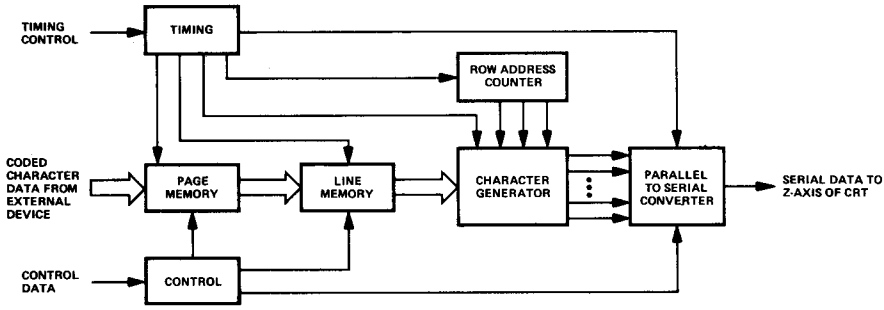
V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



APPLICATIONS INFORMATION



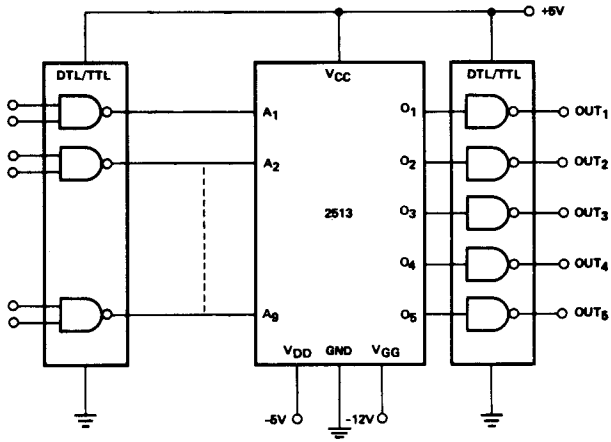
APPLICATION INFORMATION

CHARACTER GENERATOR: The 2513 IS DESIGNED TO PROVIDE THE INFORMATION NEEDED TO CONVERT THE CHARACTER CODES INTO A DOT MATRIX FOR DISPLAY.

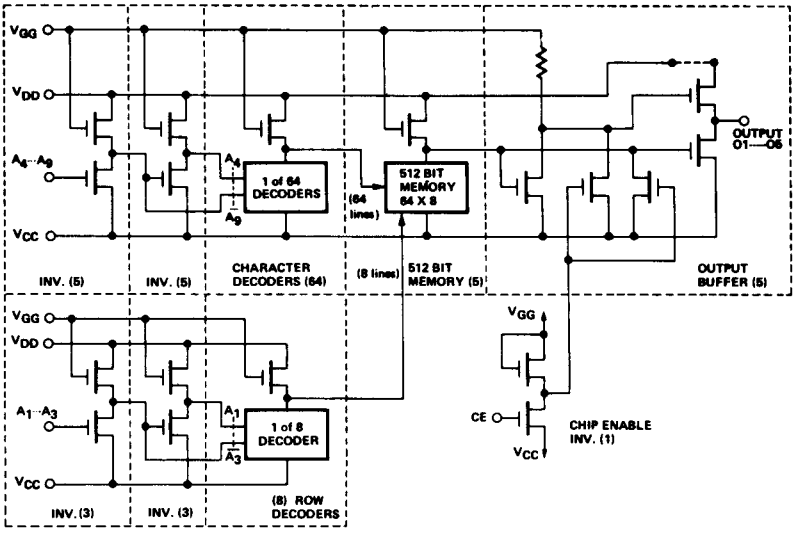
PAGE MEMORY: THIS MEMORY CONTAINS CHARACTER CODES. TYPICALLY, IT CONTAINS THE SAME NUMBER OF CHARACTER CODES AS THE NUMBER OF CHARACTERS ON A FULL SCREEN.

LINE MEMORY: THIS MEMORY CONTAINS THE CHARACTER CODES FOR ONE LINE OF THE CRT DISPLAY.

DTL/TTL INTERFACING

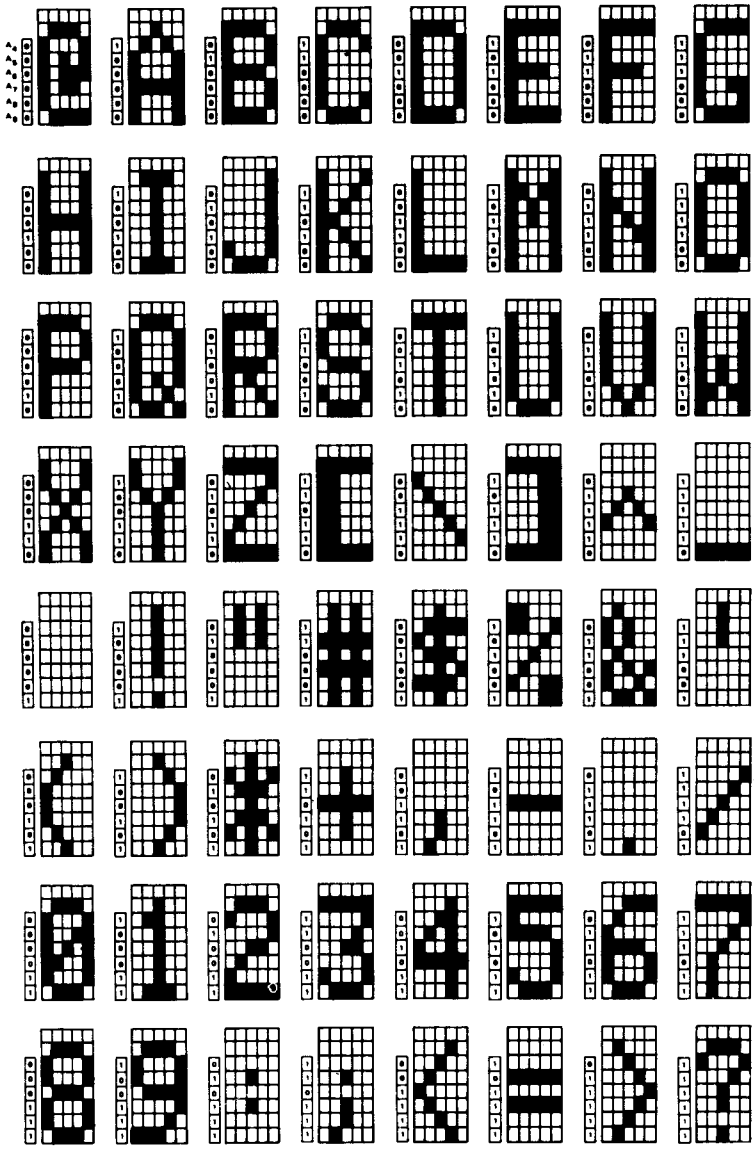


CIRCUIT CROSS-SECTION



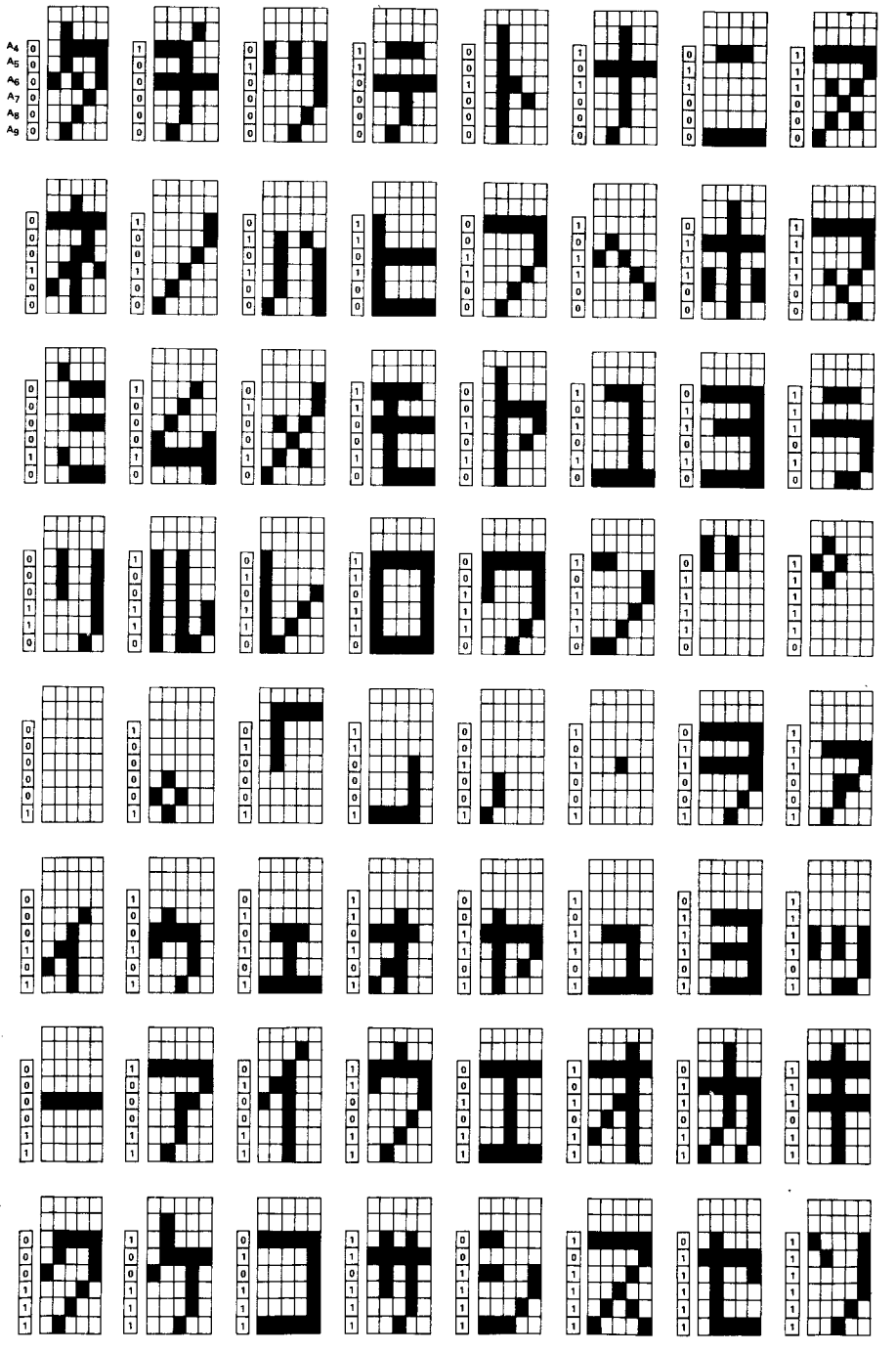
ASCII CHARACTER FONT

2513N/CM2140



JAPANESE KATAKANA FONT

2513N/CM4800



COMPANY_____

ADDRESS_____

CITY_____STATE_____ZIP____

TELEPHONE_____

AUTHORIZED SIGNATURE_____

DATE_____

CUSTOMER PRINT OR ID NO._____

PURCHASE ORDER NUMBER_____

DEVICE TYPE_____2513_____

CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS)_____

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A_4 through A_9) selects 1-of-64 matrix characters arranged 5 dots horizontally and 8 dots vertically. A three bit binary address code (A_1 through A_3) selects 1 of 8 rows. Five outputs display a complete row of the character matrix. See Figure 1. The devices may also be used in pairs to provide 9 X 7 and 10 X 8 vertical scan formats.

CHARACTER FORMAT

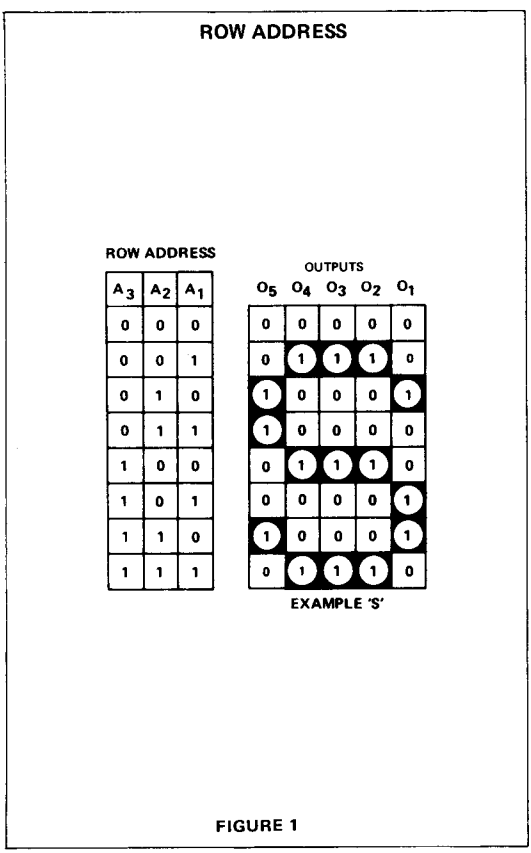


FIGURE 1

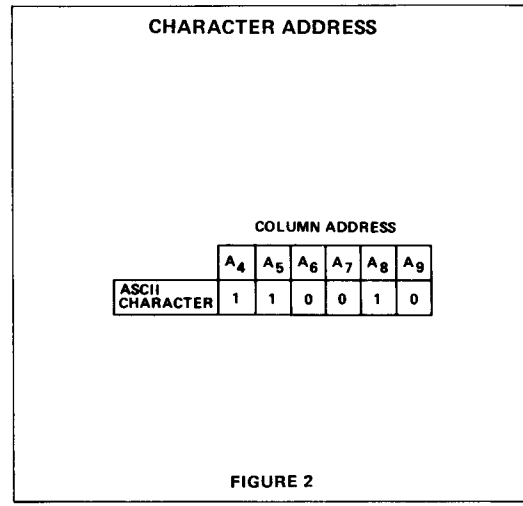


FIGURE 2

ORGANIZATION AS READ-ONLY MEMORY

For a straight 512 X 5 read-only memory, the five outputs will display any one of 512 5-bit stored words corresponding to a 9-bit address applied to A_1 through A_9.

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for a custom device will consist of the basic product type followed by a unique CM number assigned by Signetics. For example, "2513N/CM2141".

- **PROGRAMMING WITH PUNCHED CARDS**
  For maximum accuracy and minimum cost and turnaround time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.
- **PROGRAMMING WITH WRITTEN TRUTH TABLE**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. 3.2V minimum). Similarly, a "1" address input level is interpreted as 3.2V minimum.