UART 16550A - TX Logic

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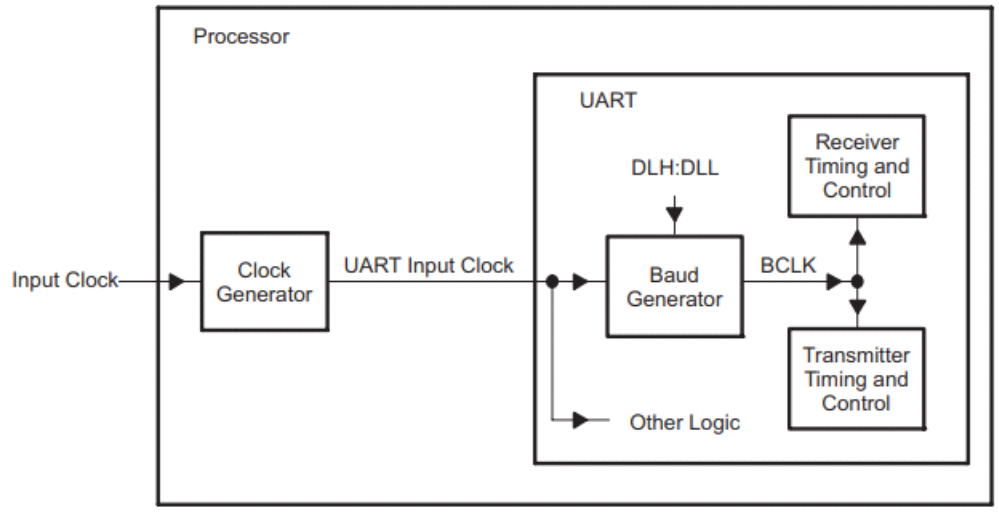
Sub Components

- Registers
- TX FIFO -> TX Logic
- RX FIFO <- RX Logic
- Baud Generator
- Interrupt Control (Omitted)
- DMA Logic (Omitted)
- Modem Control (Omitted)

- **Registers**
  - Can be used for data storage
    - THR - Hold data before applying to TX FIFO
    - RBR - Store received data
    - Scratchpad - Temporarily hold data
    - Control Registers
    - Status Registers
  - Address Bus Size is 3 bit => 8 unique addresses
  - Total Number of Registers is 10 so additional bits in the registers are used as addresses
- **FIFO**
  - UART 8550 can only store single byte in THR and RBR while 16500 can hold 16 bytes in FIFO
- **TX Logic**
  - Reading data from FIFO, add formatting bits and send the data serially using a shift register
- **RX Logic**
  - Collect data and store in FIFO

Oversampling - Reduce bit error in UART

Figure 2-1 UART Clock Generation Diagram



The 16× or 13× reference clock is selected by configuring the OSM_SEL bit in the mode definition register (MDR). The formula to calculate the divisor is:

$$\text{Divisor} = \frac{\text{UART Input Clock Frequency}}{\text{Desired Baud Rate} \times 16} \quad \text{[MDR.OSM\_SEL = 0]}$$

$$\text{Divisor} = \frac{\text{UART Input Clock Frequency}}{\text{Desired Baud Rate} \times 13} \quad \text{[MDR.OSM\_SEL = 1]}$$

The frequency of BCLK can be either of the two -

- Baud Rate * 16 => Received or transmitted bit lasts 16 BCLK cycles
  - Transmitter keeps the data static for 16 clock cycles
  - Bit is sampled in the 8th BCLK cycle
- Baud Rate * 13 => Received or transmitted bit lasts 13 BCLK cycles
  - Transmitter keeps the data static for 13 clock cycles
  - Bit is sampled in the 6th BCLK cycle

DLH and DLL registers decide the BCLK frequency and BCLK is sent to Transmitter and Receiver Timing and Control
OSM_SEL bit in Mode Definition Register is used to decide the oversampling factor

- If MDR.OSM_SEL == 0, then factor = 16 else factor = 13

DLL and DLH are loaded during initialization of the UART and writing to DLH/DLL results in two wait states being inserted during write access while the baud generator is loaded with the new value.

Table 3-1 UART Registers

Offset	Acronym	Register Description
0h	RBR	Receiver Buffer Register (read only)
0h	THR	Transmitter Holding Register (write only)
4h	IER	Interrupt Enable Register
8h	IIR	Interrupt Identification Register (read only)
8h	FCR	FIFO Control Register (write only)
Ch	LCR	Line Control Register
10h	MCR	Modem Control Register
14h	LSR	Line Status Register
18h	MSR	Modem Status Register
1Ch	SCR	Scratch Pad Register
20h	DLL	Divisor LSB Latch
24h	DLH	Divisor MSB Latch
28h	REVID1	Revision Identification Register 1
2Ch	REVID2	Revision Identification Register 2
30h	PWREMU_MGMT	Power and Emulation Management Register
34h	MDR	Mode Definition Register
End of Table 3-1		

Transmission

- Has Transmitter Hold Register (THR) and Transmitter Shift Register (TSR)
    - In FIFO mode, THR is a 16 byte FIFO
- Control is handled predominantly by Line Control Register (LCR), since interrupt control, DMA logic and modem control are absent. LCR decides the following parameters
    - 1 START bit
    - 5,6,7 or 8 data bits
    - 1 Parity Bit (Optional)
    - 1, 1.5 or 2 STOP bits

LCR has 8 bits

- Bit 31 to 8 are RESERVED
- Bit 7 => Divisor Latch Access Bit
    - DLAB == 0, allows access to the Receiver Buffer Register (RBR), Transmitter Holding Register (THR) and the interrupt enabled register. At the address shared by RBR, THR and DLL, the CPU can read from RBR and write to THR. At the address shared by IER and DLH, the CPU can read and write to the IER
    - DLAB == 1, allows access to the divisor latches of the baud generator during a read or write operation. At the address shared by RBR, THR and DLL, the CPU can read from and write to DLL. At the address shared by IER and DLH, the CPU can read from and write to the DLH
- Bit 6 => Break Control
    - BC == 0, break condition is disabled
    - BC == 1, Break condition is transmitted to the receiver
        - UARTn_TXD is forced to spacing (cleared) state
- Bit 5 => Stick Parity
    - SP == 0, stick parity is disabled
    - SP == 1, stick parity is enabled
    - If EPS == 0, parity bit(s) is transmitted and checked as set (1 is sent)
    - If EPS == 1, parity bit(s) is transmitted and checked as cleared (0 is sent
- Bit 4 => Even Parity Select
    - EPS == 1, even number of logic 1s is transmitted and checked

        - EPS == 0, odd number of logic 1s is transmitted and checked
    - Bit 3 => Parity Enable Bit
        - PEN == 0, no parity is disabled and not checked
        - PEN == 1, parity is enabled
    - Bit 2 => STB
        - Receiver clocks only the first STOP bit, regardless of the number selected
        - STB == 0, 1 STOP Bit is used
        - STB == 1, number of STOP bits depend on WLS
            - WLS == 0, 1.5 STOP bits transmitted
            - Else, 2 STOP bits are transmitted
    - Bit 1-0 => WLS
        - WLS == 0, 5 bits transmitted
        - WLS == 1, 6 bits transmitted
        - WLS == 2, 7 bits transmitted
        - WLS == 3, 8 bits transmitted

Table 3-9 Relationship Between ST, EPS, and PEN Bits in LCR

ST Bit	EPS Bit	PEN Bit	Parity Option
x	x	0	Parity disabled: No PARITY bit is transmitted or checked.
0	0	1	Odd parity selected: Odd number of logic 1s.
0	1	1	Even parity selected: Even number of logic 1s.
1	0	1	Stick parity selected with PARITY bit transmitted and checked as set.
1	1	1	Stick parity selected with PARITY bit transmitted and checked as cleared.
End of Table 3-9			

Table 3-10 Number of STOP Bits Generated

ST Bit	WLS Bit	Word Length Selected with WLS Bits	Number of STOP Bits Generated	Baud Clock (BCLK) Cycles
0	x	Any word length	1	16
1	0h	5 bits	1.5	24
1	1h	6 bits	2	32
1	2h	7 bits	2	32
1	3h	8 bits	2	32
End of Table 3-10				

Reference: KeyStone Architecture Literature Number: SPRUGP1 November 2010 Universal Asynchronous Receiver/Transmitter (UART) User Guide - Texas Instruments