


Z-Lite Block Diagram

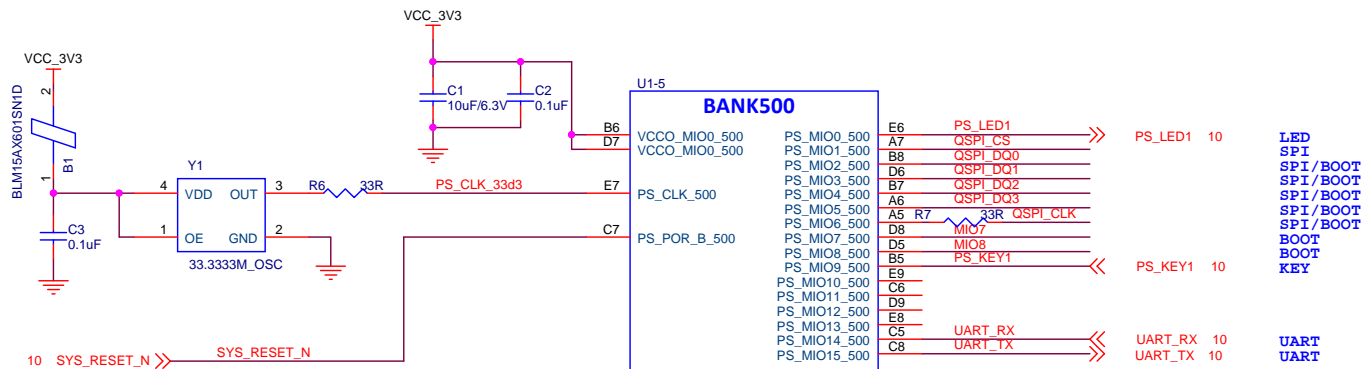
REV	DATE	PAGES	DESCRIPTION
1.0	24/04/2020	All	Rev 1.0 Release
1.1	29/05/2020	All	Rev 1.1 Release

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	PS BANK500&501
3	PS BANK502
4	PL BANK0&13
5	PL BANK34&35
6	ZYNQ Power
7	DDR3 RAM
8	ETHERNET
9	PS USB
10	PS UART SD KEY LED
11	HDMI TX
12	USB-JTAG
13	40Pin GPIO
14	Power
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	

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Title Mizar Board	
Size B	Document Number Block Diagram
Date: Monday, July 20, 2020	Rev 1.0
Sheet 1 of 14	



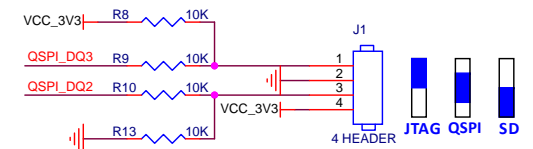
MIO[8] = 0 ----MIO bank1 voltage=3.3V

MIO[2] = 0 ----cascaded JTAG

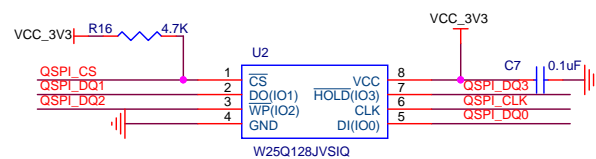
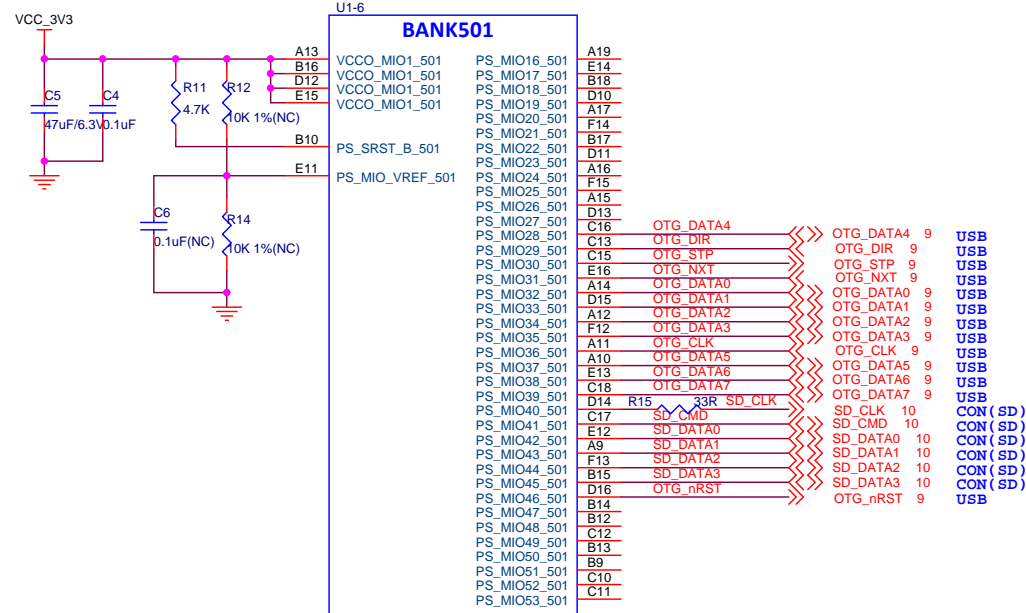
MIO[3] = 0 ----JTAG/NAND/Quad-SPI/SD

MIO[6] = 0 ----PLL used

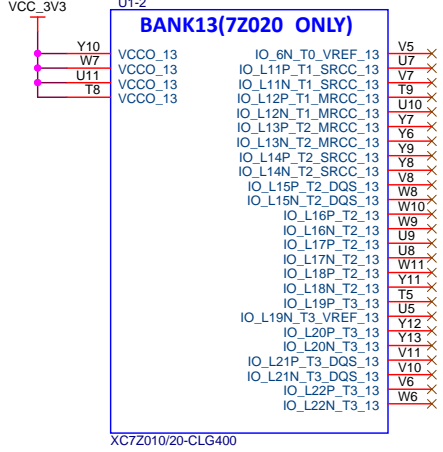
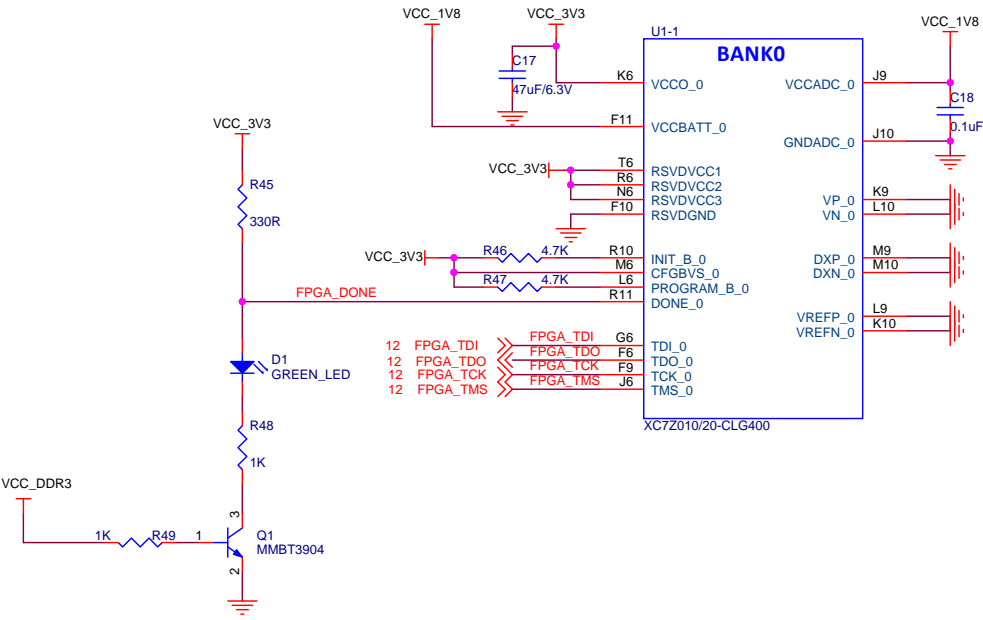
MIO[7] = 0 ----MIO bank0 voltage=3.3V



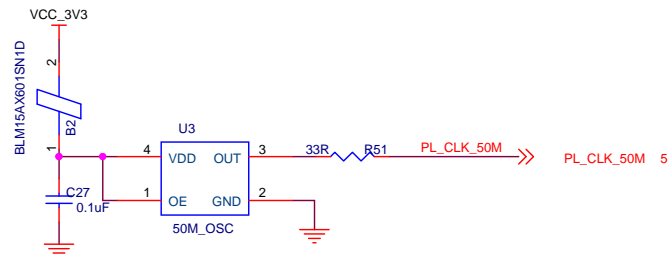
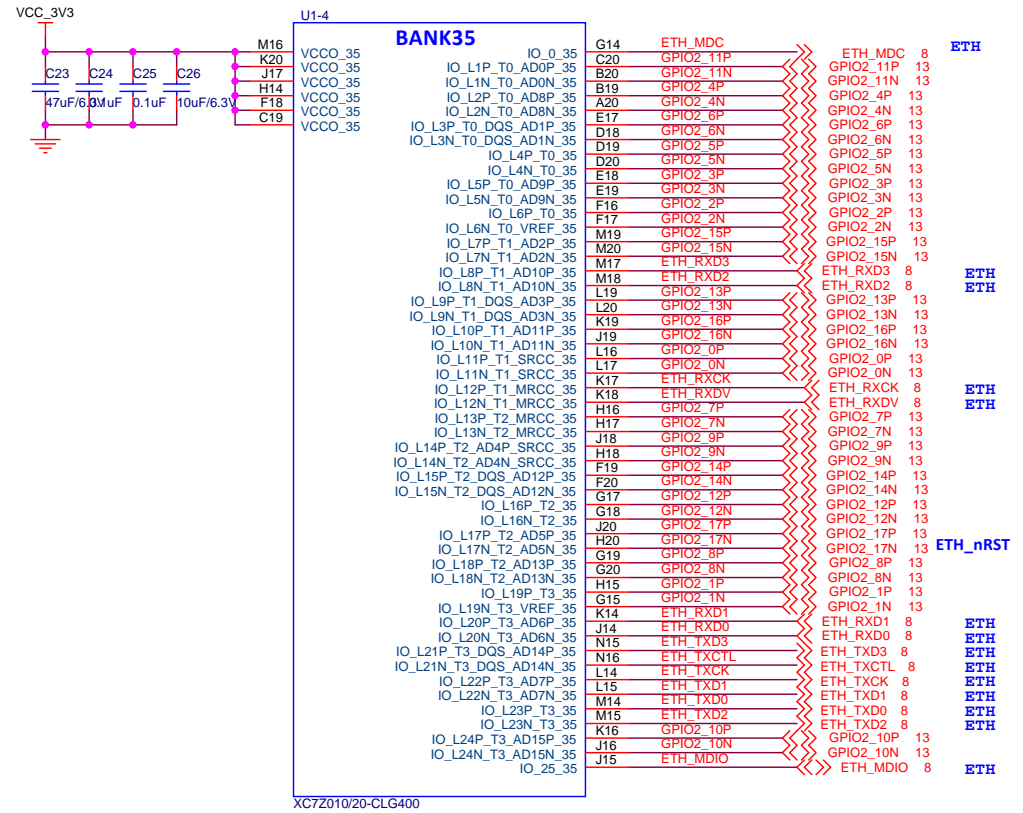
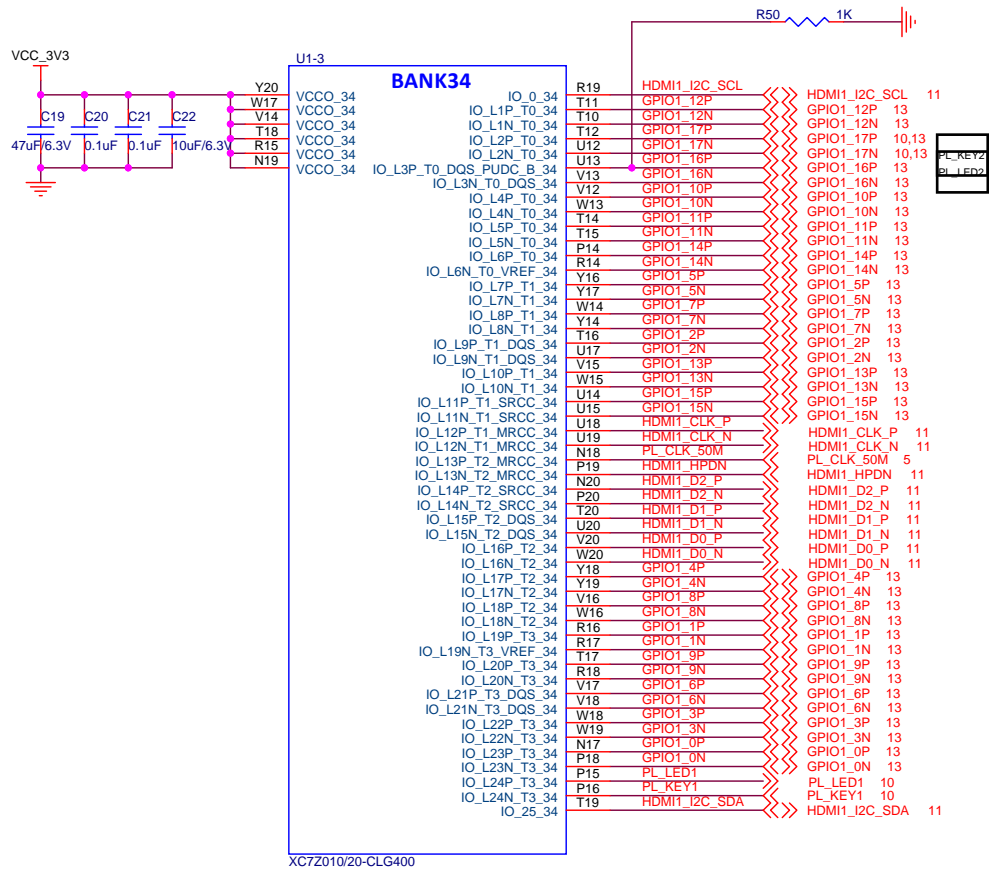
Boot Mode	MIO[5] (QSPI_DQ3)	MIO[4] (QSPI_DQ2)
JTAG	0	0
NAND	0	1
QSPI	1	0
SD Card	1	1

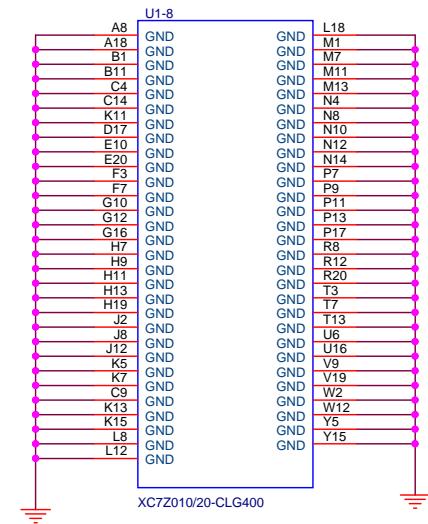
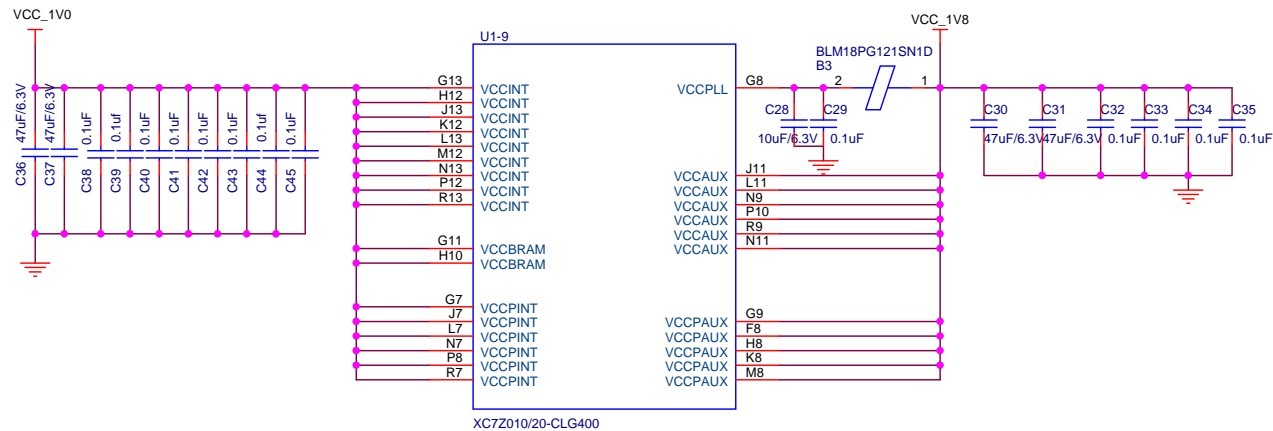


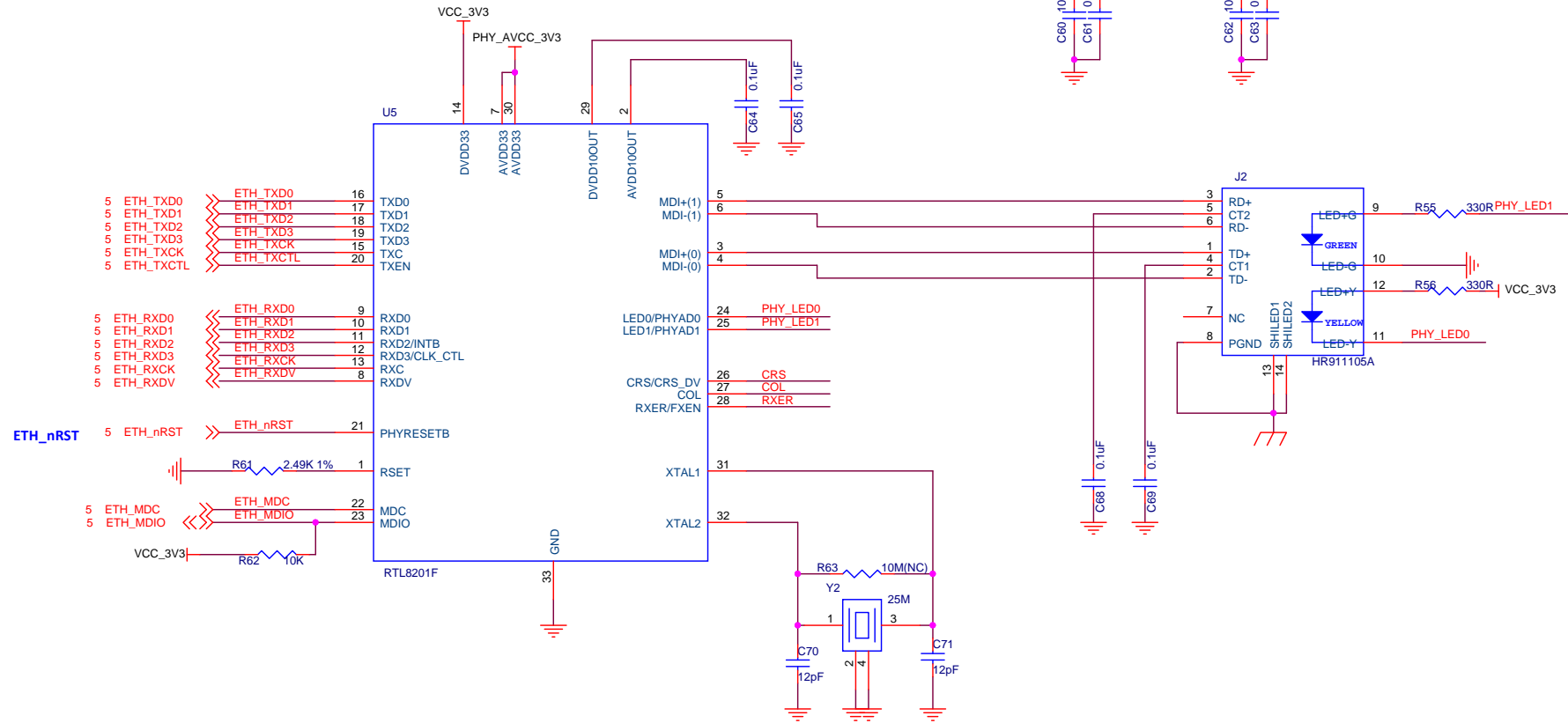
ZYNQ_CONFIG



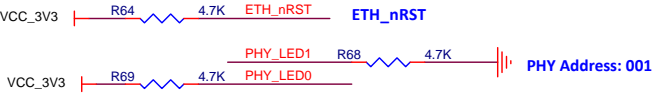
FPGA_PL



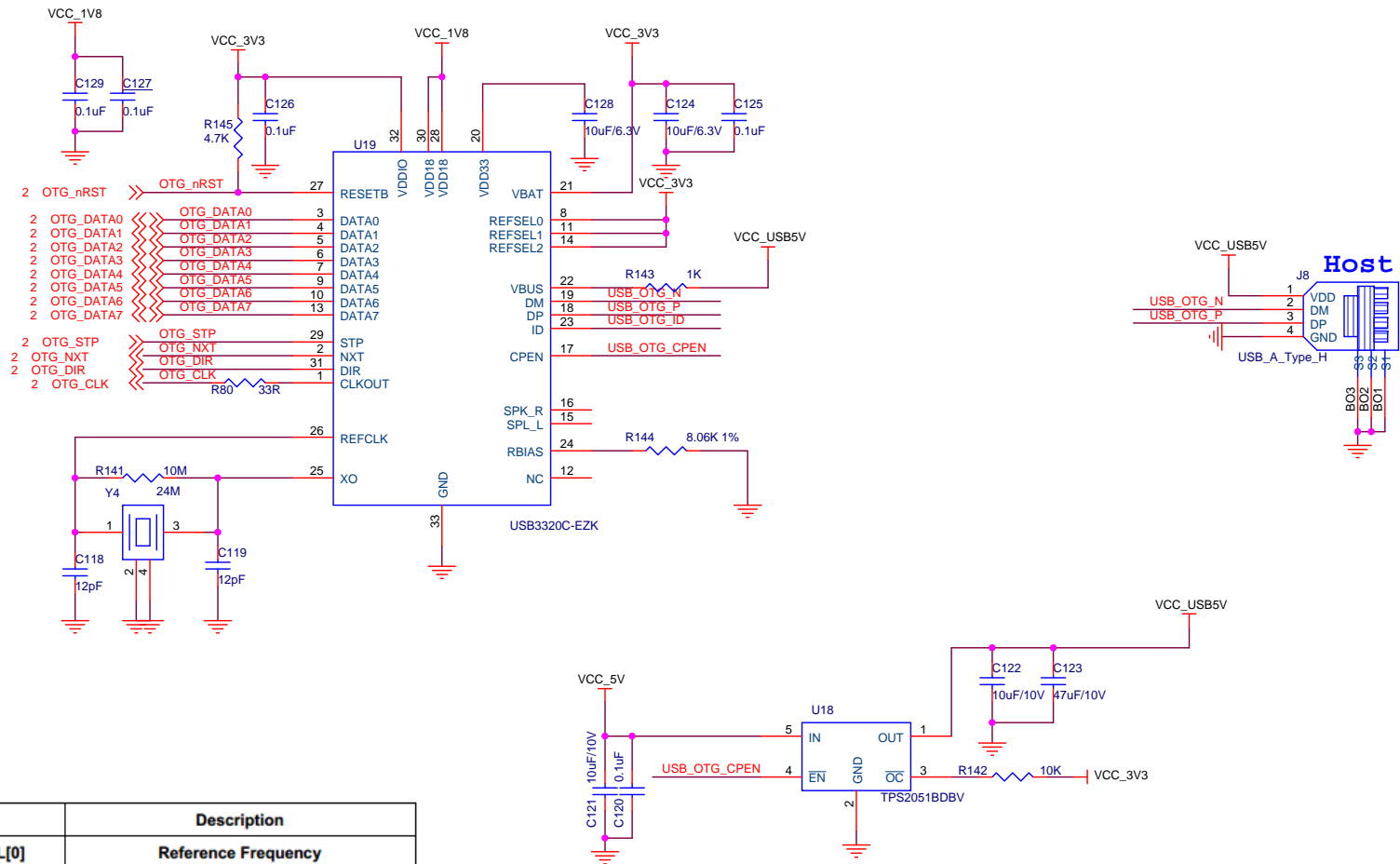




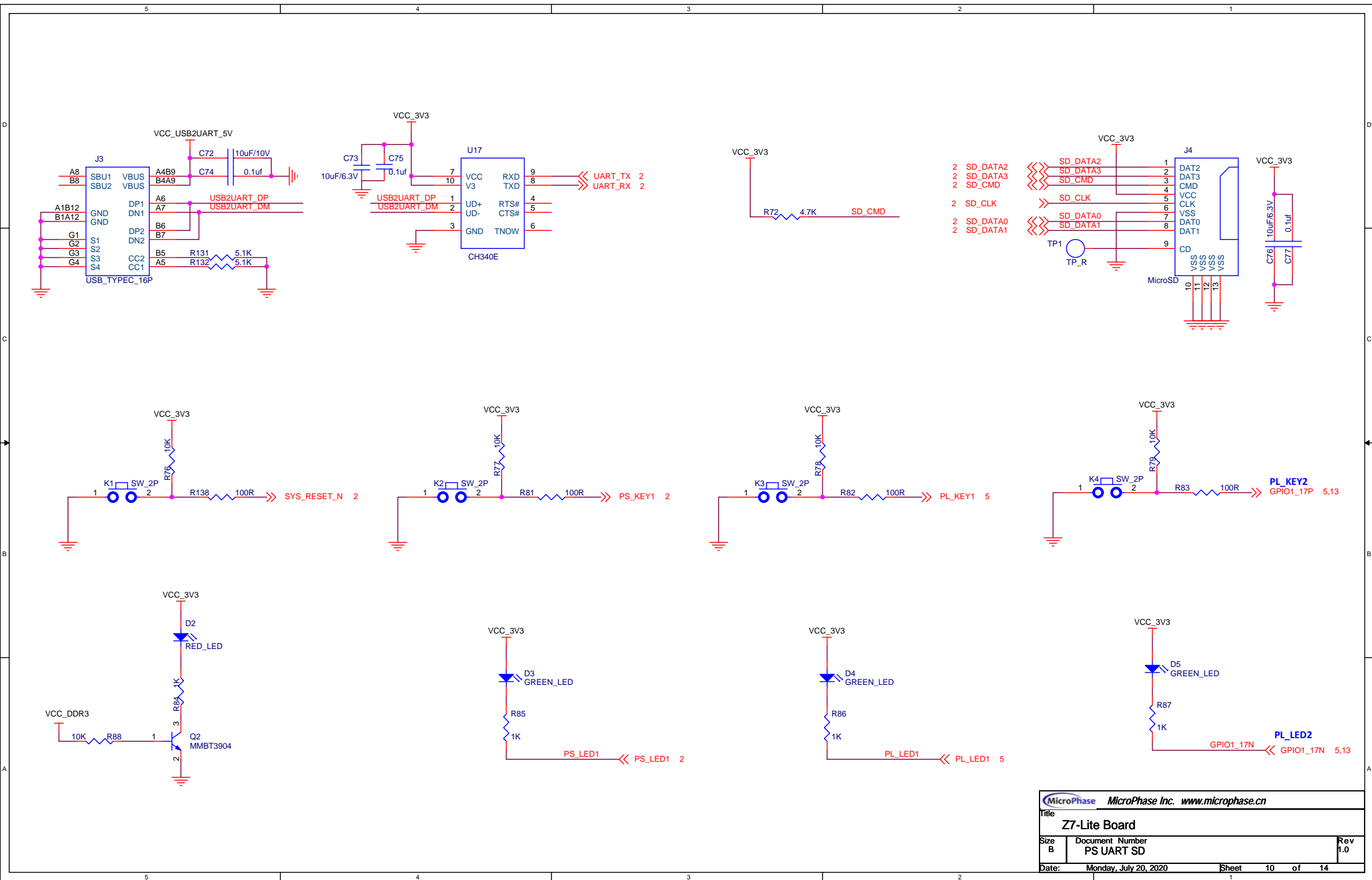
PHY Config

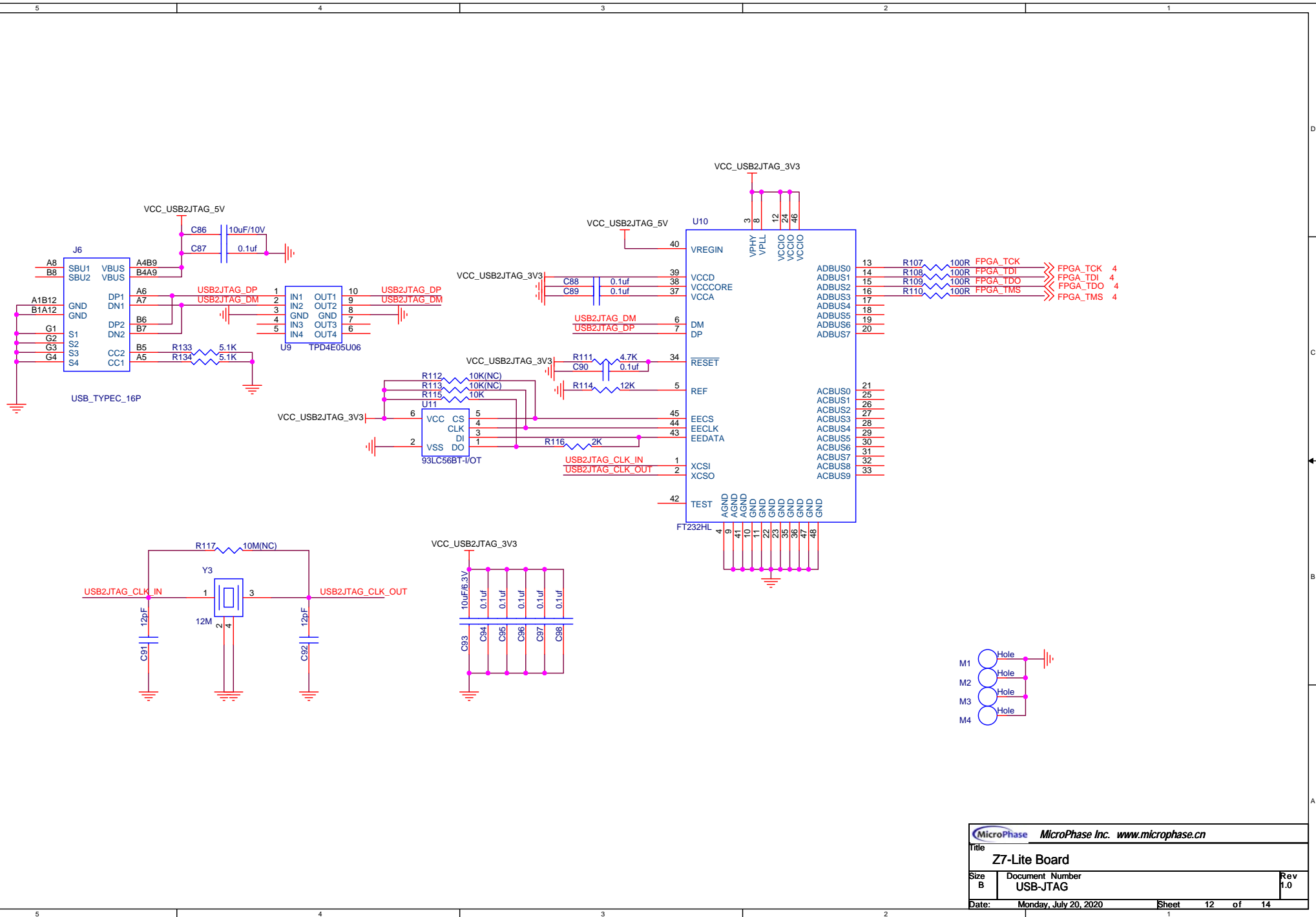


PS USB OTG

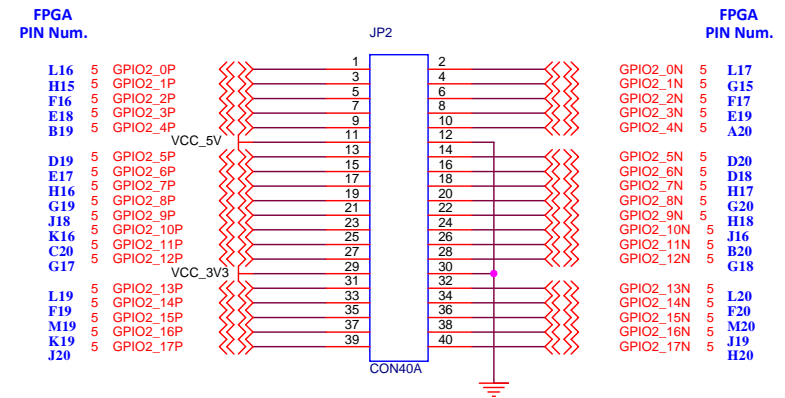
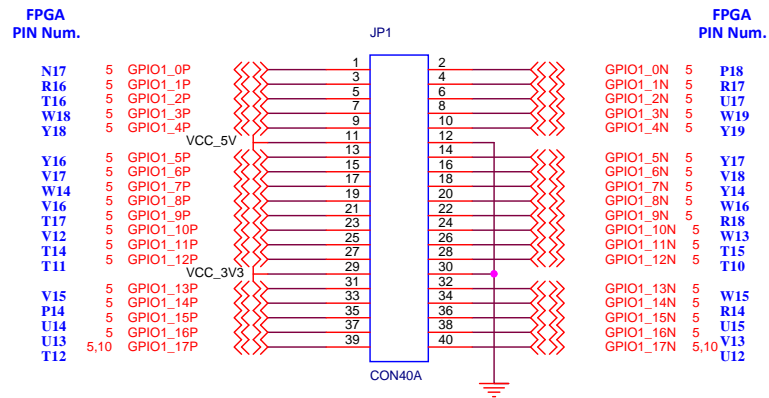


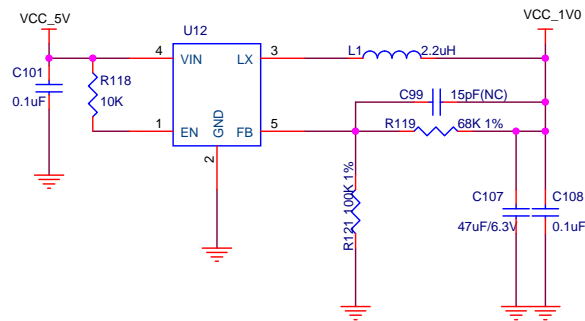
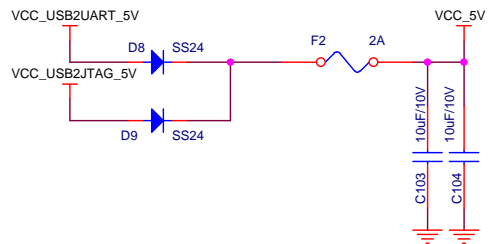
Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4 MHz
0	1	0	12 MHz
0	1	1	27 MHz
1	0	0	13 MHz
1	0	1	19.2 MHz
1	1	0	26 MHz
1	1	1	24 MHz



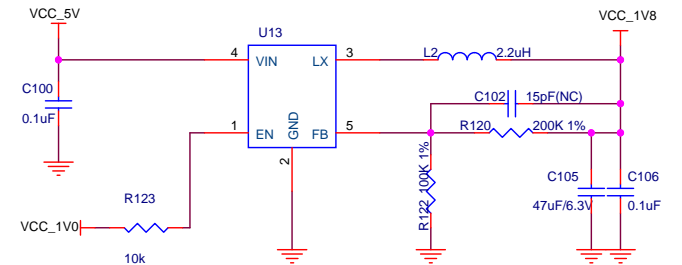


GPIO Interface

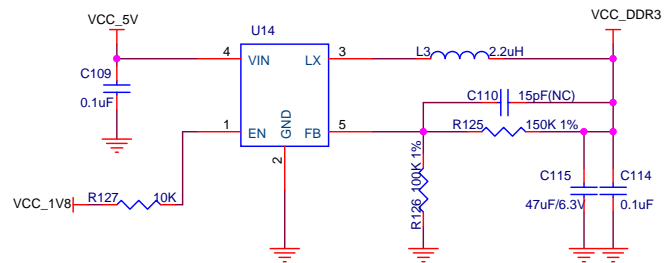




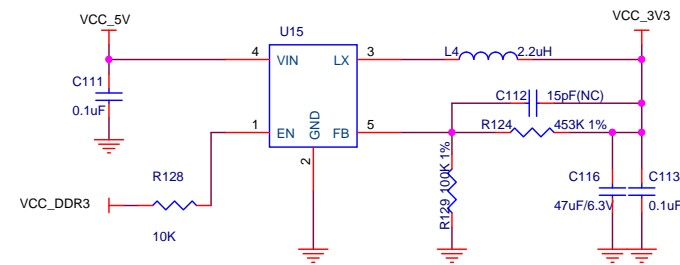
Vref = 0.6V VOUT = 1.0V



Vref = 0.6V VOUT = 1.8V



Vref = 0.6V VOUT = 1.5V



Vref = 0.6V VOUT = 3.3V