Title	***Housekeeping***		
Size: A3	Number: 1	Revision: 1.0	
Date: 19/02/2021	Time: 18:45:59	Sheet 1 of 4	
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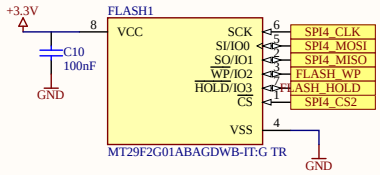
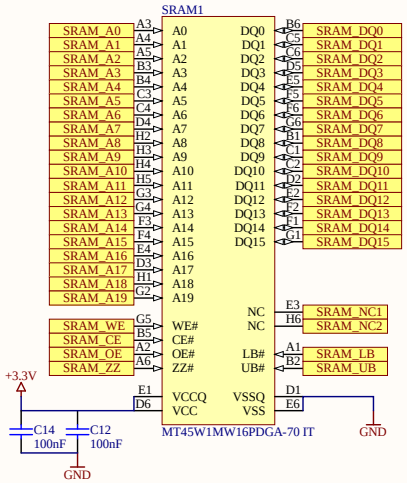
FLASH



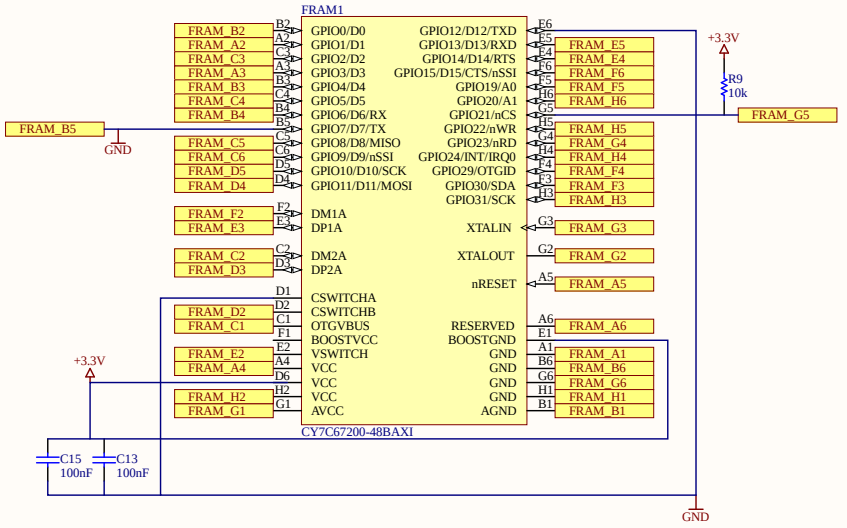
SRAM

Actual component: CY62157G/CY62157GE



FRAM

Actual component: FM22LD16



Title	**Core**		
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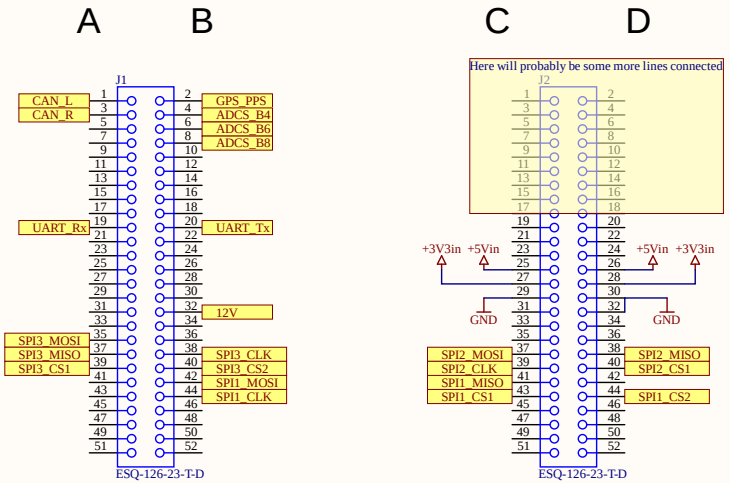
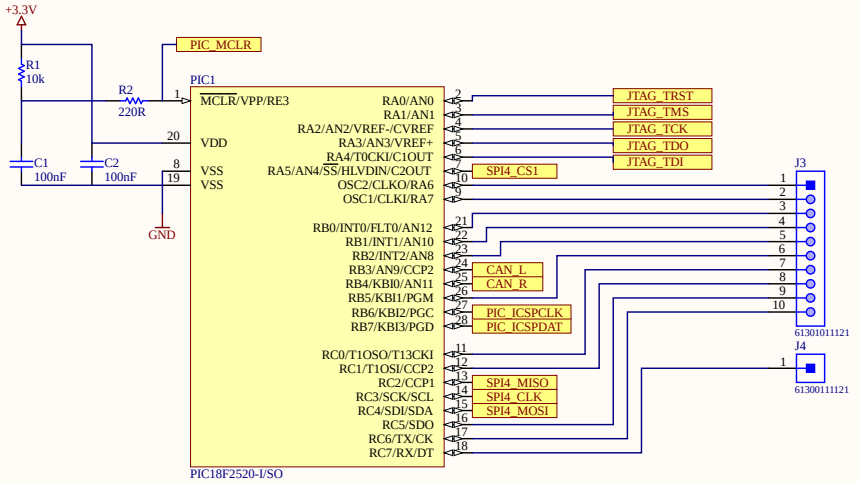
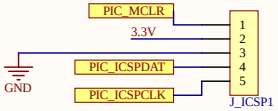
PC/104 Connector



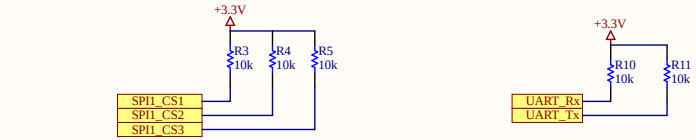
PIC (PIC18(L)F26K83)



PICKit connector



Pull-ups for SPI and UART



Title	***Interface***		
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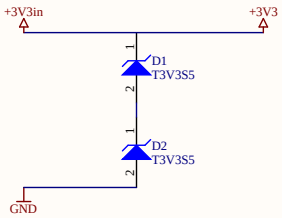
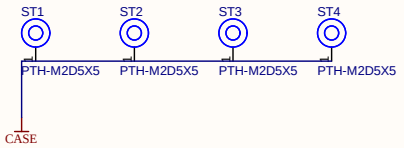
Date: 19/02/2021	Time: 18:45:59	Sheet 3 of 4	
File: C:\Users\pal\Dropbox\EPFL\Space_team\PCB\CHESSOBC_rev1\Interface.SchDoc			

Surge voltage protection



Over/under-voltage detection

Mechanical fixation points



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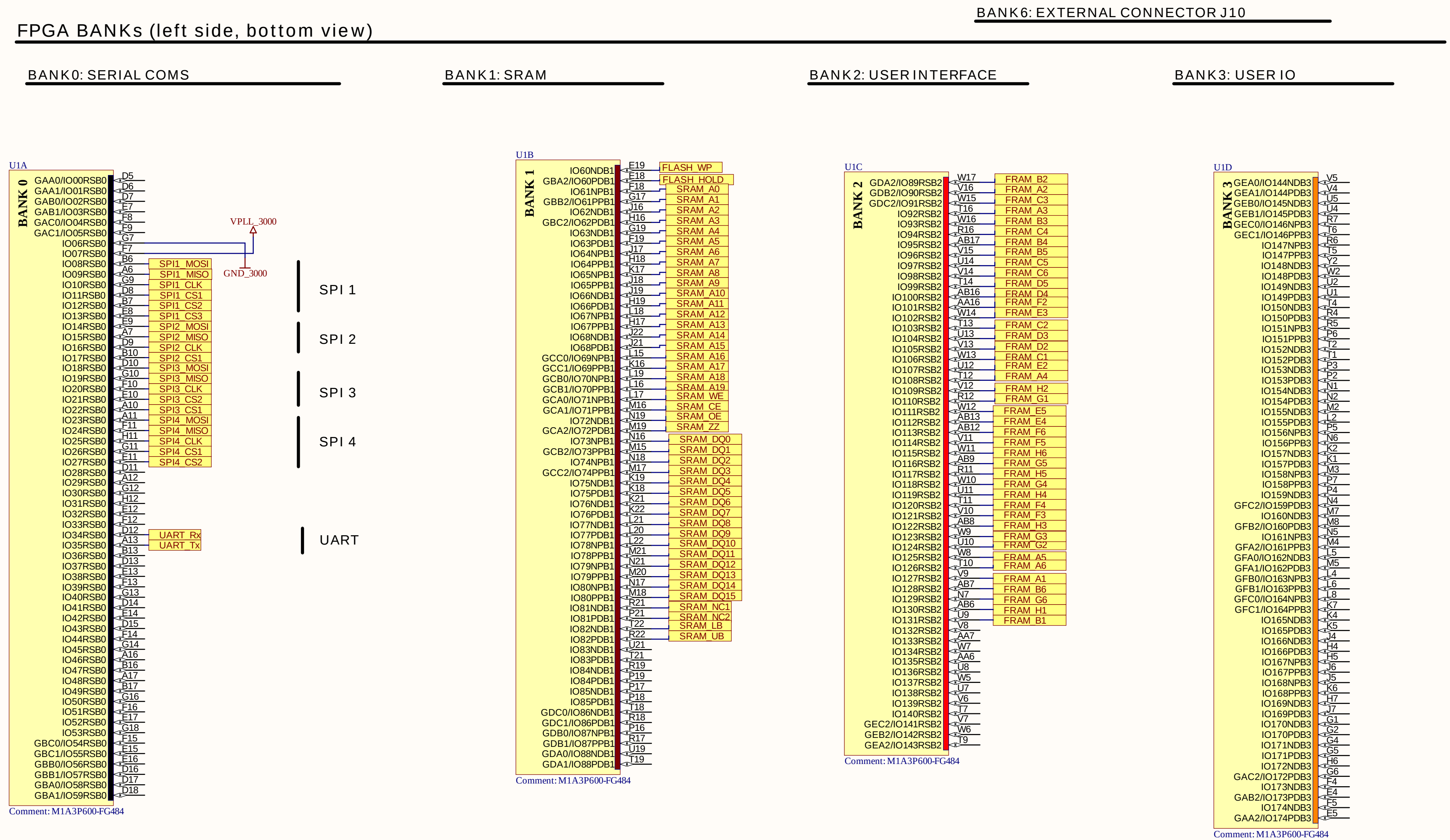
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG:	
DSN:	
CHK:	

REFERENCE DOCUMENTS
BOM:
ASSY DWG:
FAB DWG:
PCB DWG:

PROJECT
Altium
L3, 12a Rodborough Rd, Frenchs Forest, NSW, Australia 2086

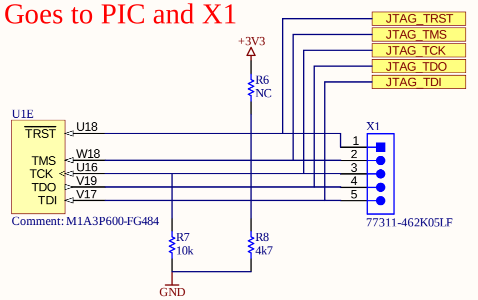
PROJECT REVISION: Not in version control
DOCUMENT REVISION: Not in version control
DESIGN ITEM:
TITLE

SIZE: A3
CAGE CODE
DWG NO.
REV
SCALE:
FILE NAME: FPGABanks.SchDoc
SHEET
OF

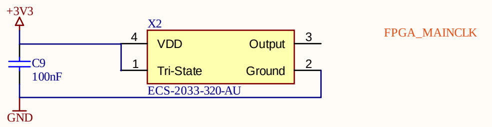
REVISION	DESCRIPTION	DATE	APPROVED

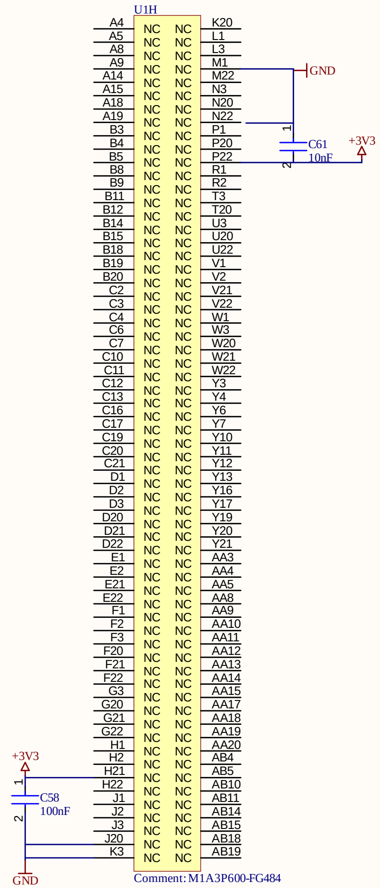
JTAG

Goes to PIC and X1



FPGA OSCILLATOR (MAIN CLOCK): Sapristi board uses 32 MHz, same as on OBC on Astrocard sat.





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FAB DWG:
PCB DWG:

PROJECT
Altium
L3, 12a Rodborough Rd, Frenchs Forest, NSW, Australia 2086
PROJECT REVISION: Not in version control
DOCUMENT REVISION: Not in version control
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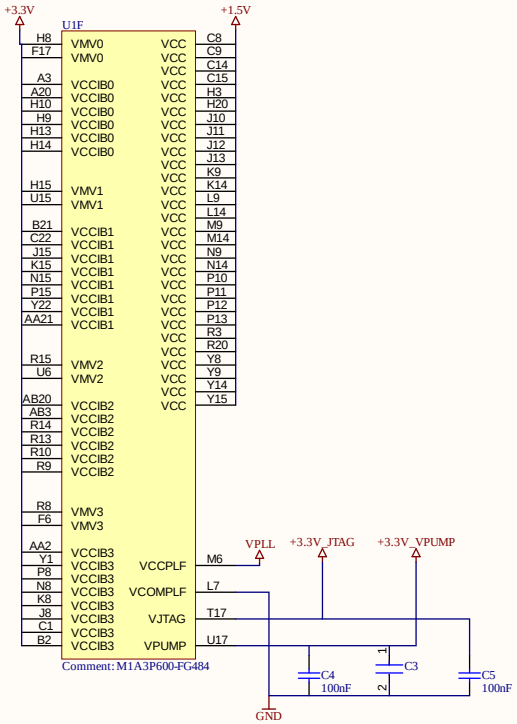
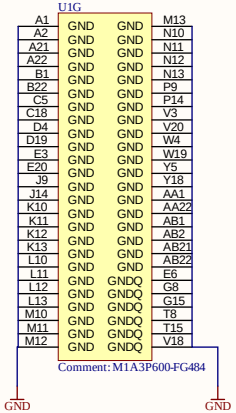
TITLE
SIZE A3 | CAGE CODE | DWG NO. | REV
SCALE: | FILE NAME FPGAMisc.SchDoc | SHEET | OF

REVISION	DESCRIPTION	DATE	APPROVED

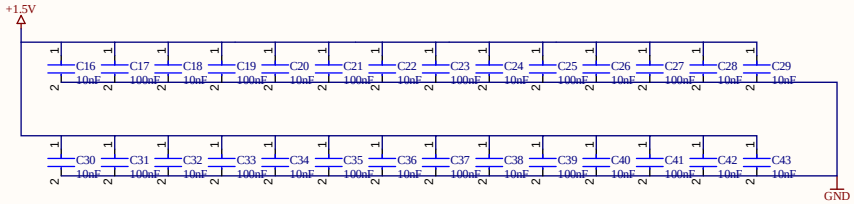
FPGA POWER

FPGA POWER PINS

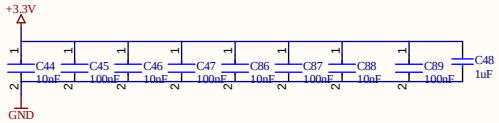




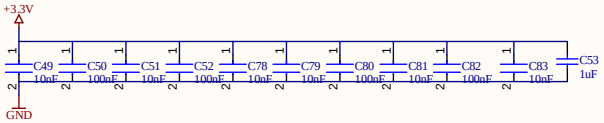
CORE DECOUPLING



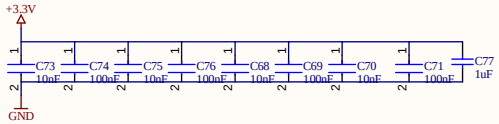
BANK0 DECOUPLING



BANK1 DECOUPLING



BANK2 DECOUPLING



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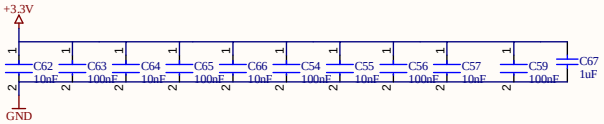
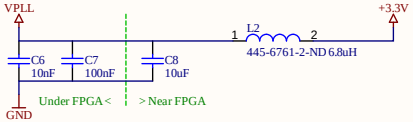


PLL DECOUPLING



SIZE	CAGE CODE	DWG NO.	REV
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