

1	2	3	4	5	6	7	8
A							A
B							B
C							C
D							D
1	2	3	4	5	6	7	8

Title <i>Housekeeping</i>				
Size: A3	Number: 1	Revision: 1.0		
Date: 19/02/2021	Time: 18:45:59	Sheet 1 of 4		
File: C:\Users\pal\Dropbox\EPFL\Space_team\PCB\CHESSOBC_rev1\Housekeeping.SchDoc				

A

B

C

D

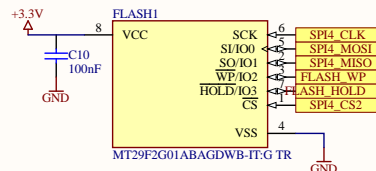
A

B

C

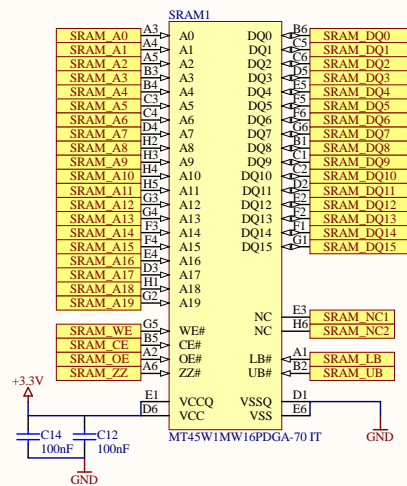
D

FLASH



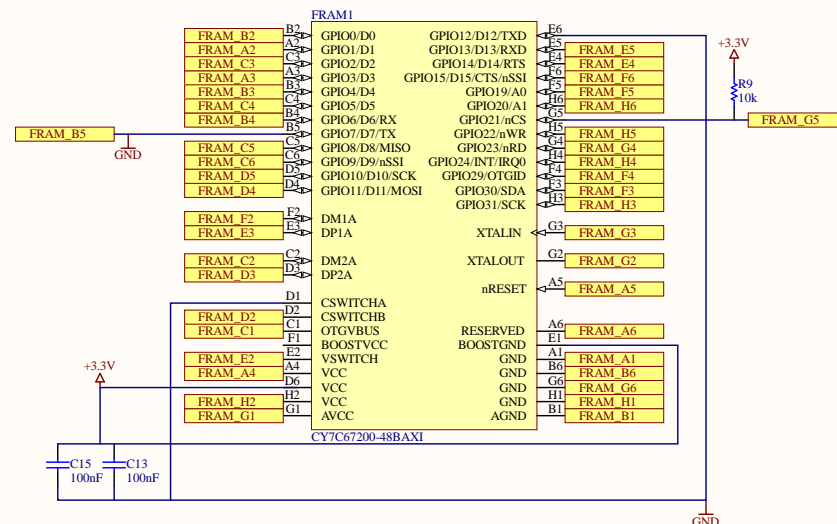
SRAM

Actual component: CY62157G/CY62157GE



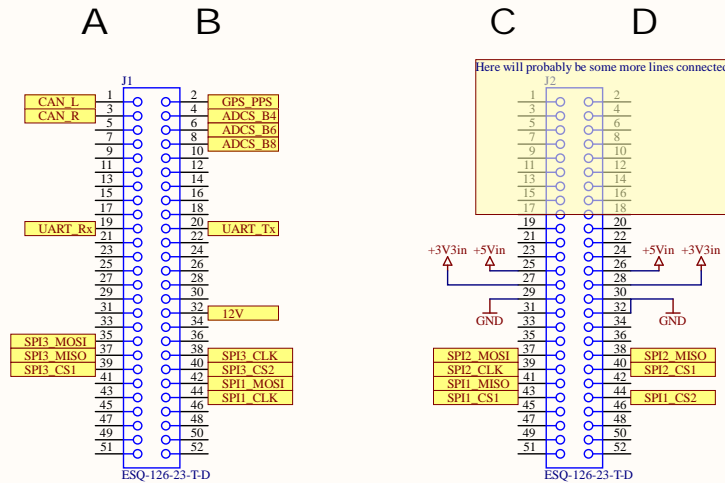
FRAM

Actual component: FM22LD16

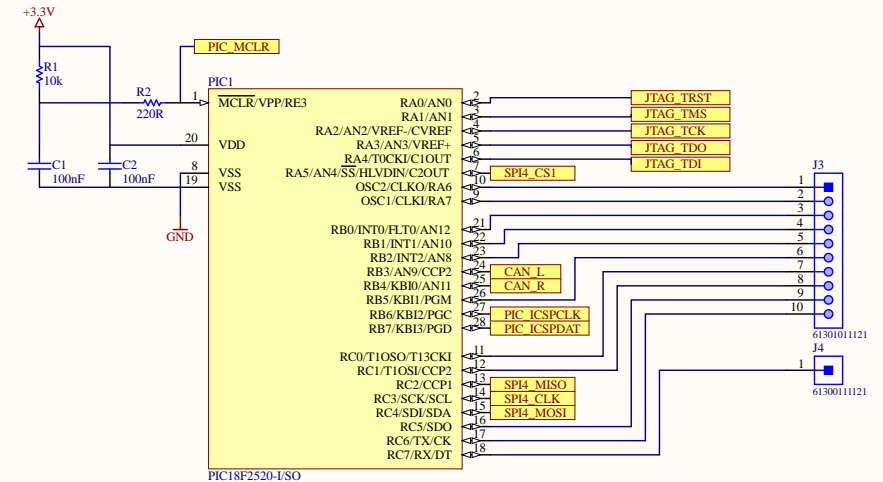


Title <i>Core</i>				
Size: A3	Number: 1	Revision: 1.0		
Date: 19/02/2021	Time: 18:45:59	Sheet 2 of 4		
File: C:\Users\pal\Dropbox\EPFL\Space team\PCB\CHESOB\rev1\Core.SchDoc				

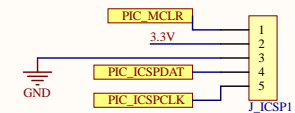
PC/104 Connector



PIC (PIC18(L)F26K83)



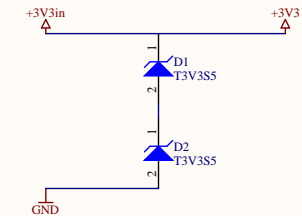
PICKit connector



Pull-ups for SPI and UART

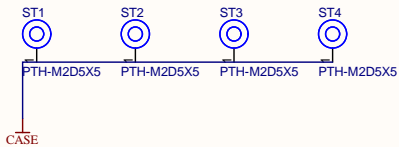


Surge voltage protection



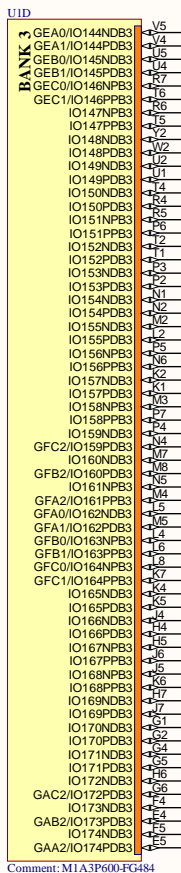
Over/under-voltage detection


Mechanical fixation points



Title: <i>Power and mechanical</i>				
Size: A3	Number: 1	Revision: 1.0		
Date: 19/02/2021	Time: 18:46:00	Sheet 4 of 4		
File: C:\Users\pal\Dropbox\EPFL\Space_team\PCB\CHESOBBC_rev1\Power.SchDoc				

BANK3: USER IO



APPROVALS		DATE		PROJECT		 13-14-Burrough Rd Forest NSW Cannell 2006					
ENG: .				PROJECT REVISION: . DOCUMENT REVISION: . DESIGN ITEM: . Not in version control Not in version control							
DSN: .											
CHK: .											
REFERENCE DOCUMENTS				TITLE							
BOM:											
ASSY DWG:				SIZE		CAGE CODE		DWG NO.		REV	
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										OF	

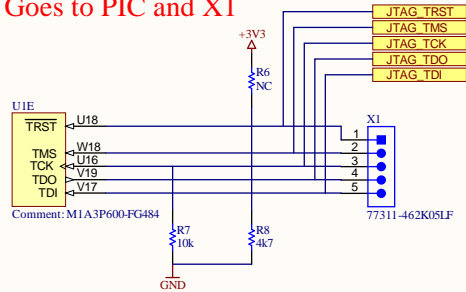
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DWG. NO. REV. 1/ST

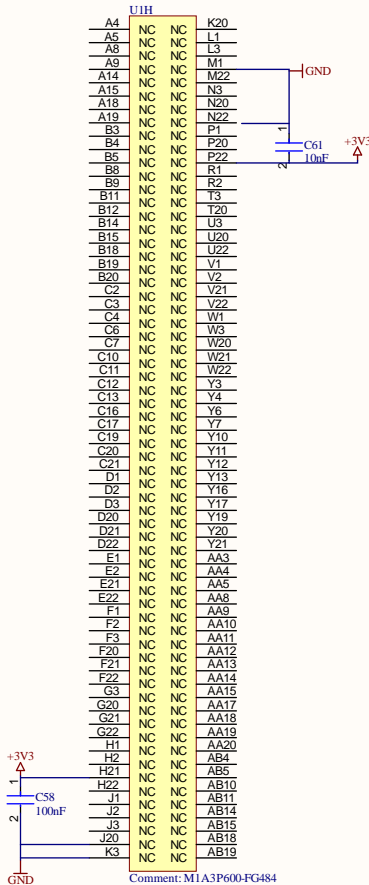
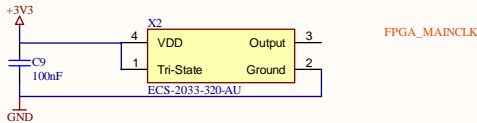
REVISION	DESCRIPTION	DATE	APPROVED

JTAG

Goes to PIC and X1



FPGA OSCILLATOR (MAIN CLOCK): Sapristj board uses 32 MHz, same as on OBC on Astrocard sat.

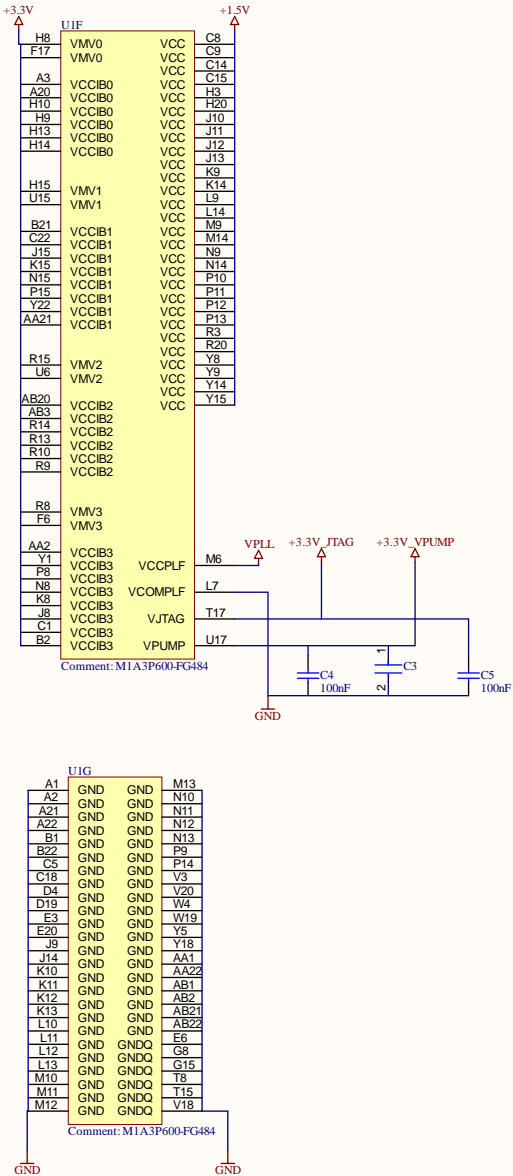


APPROVALS	DATE	PROJECT	PROJECT REVISION		DOCUMENT REVISION	DESIGN ITEM
ENG: -			Not in version control		Not in version control	
DSN: -			TITLE		TITLE	
CHK: -			REFERENCE DOCUMENTS		REFERENCE DOCUMENTS	
BOM:		SIZE		CAGE CODE	DWG NO.	REV
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FAB DWG:		SCALE:		FILE NAME	SHEET	OF
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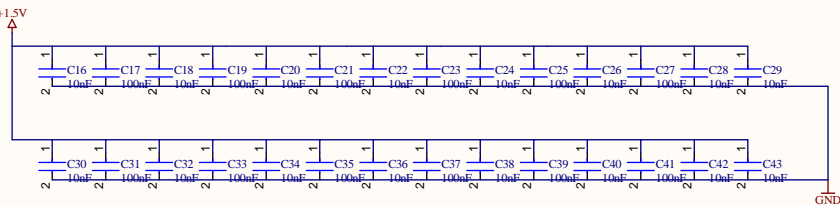
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FPGA POWER

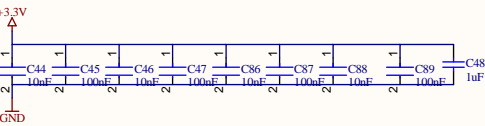
FPGA POWER PINS



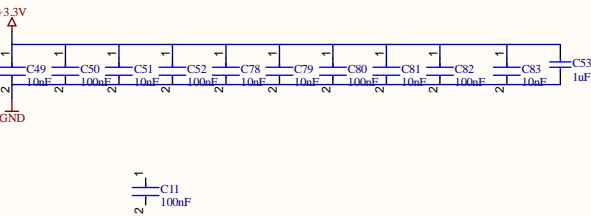
CORE DECOUPLING



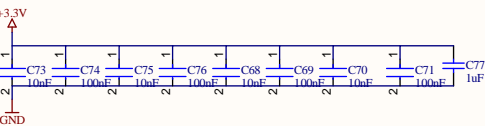
BANK0 DECOUPLING



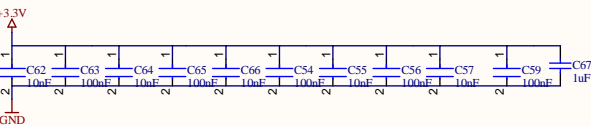
BANK1 DECOUPLING



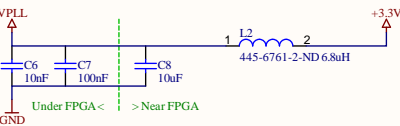
BANK2 DECOUPLING



BANK3 DECOUPLING



PLL DECOUPLING



SIZE	CAGE CODE		DWG NO.					REV	
A3									
SCALE:		FILE NAME					SHEET		OF
		FPGA Power.SchDoc							