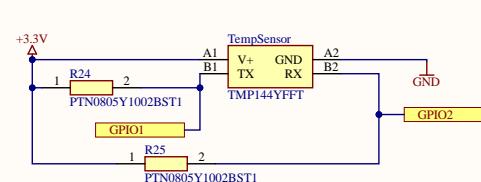
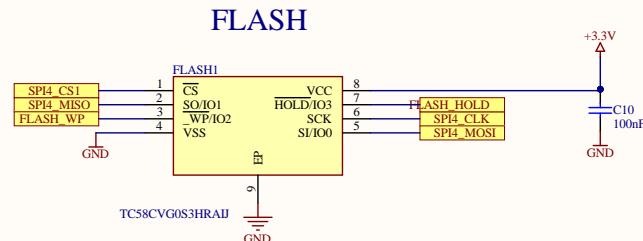
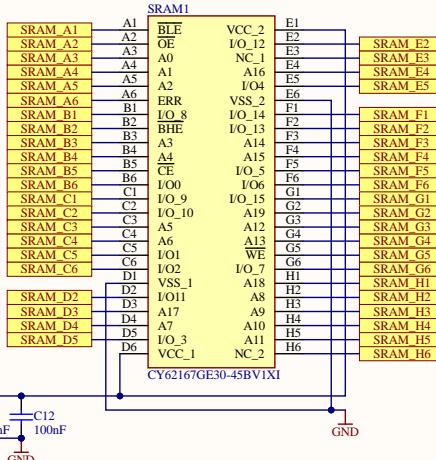


Temperature Sensor

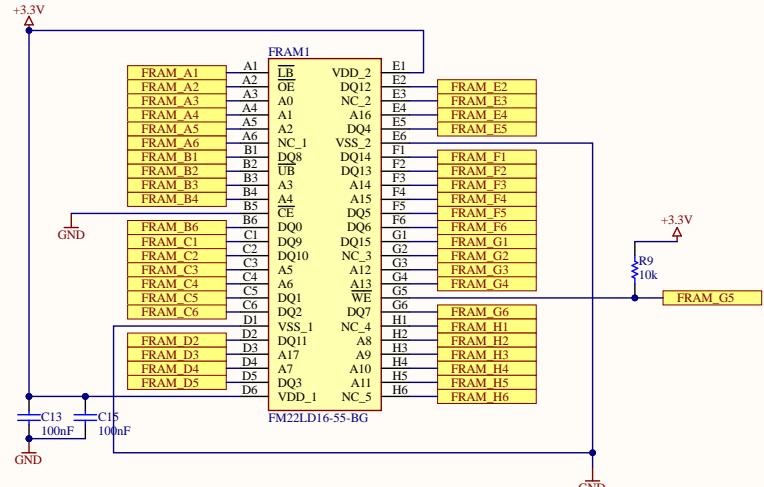


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Housekeeping		CHESS - OBC	
Size	Revision	File Name	EPFL SPACECRAFT TEAM
A3	1.0	Housekeeping_SchDoc	
Last updated 20/07/2021			EPFL Spacecraft Team EPFL Space Center PPH335 station 13 CH-1015 Lausanne
Page 1 of 8		Designers ML, PFA, EW	

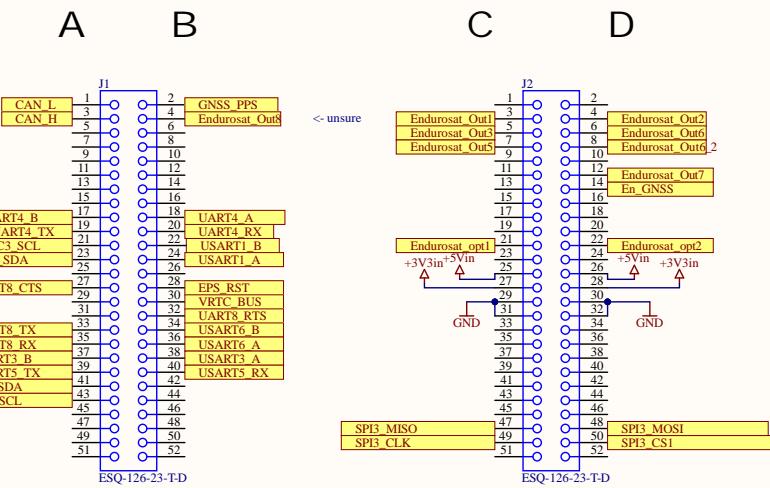
SRAM



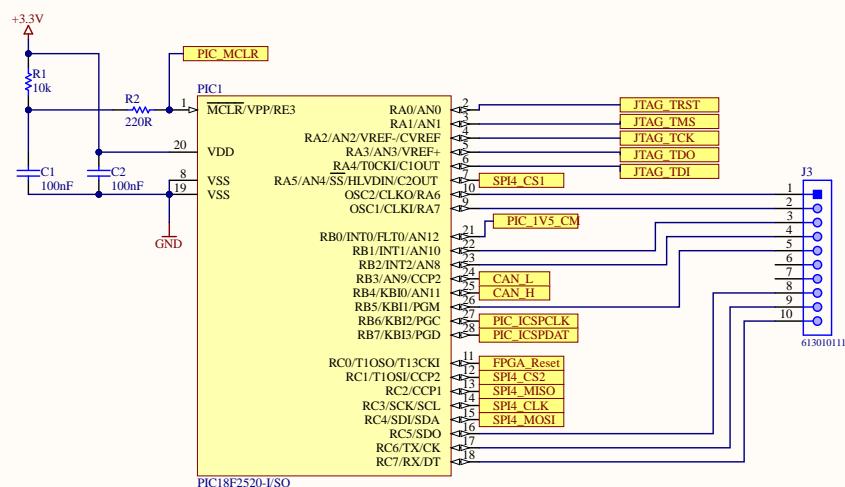
FRAM



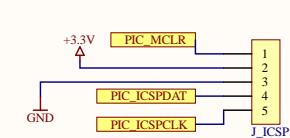
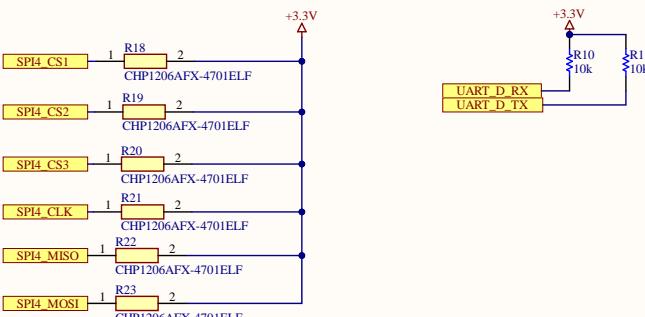
PC/104 Connector

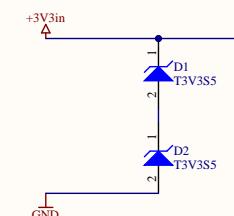
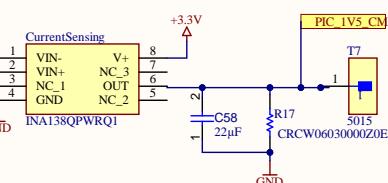
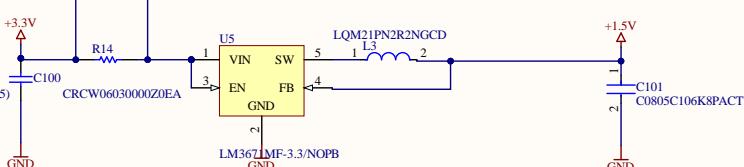
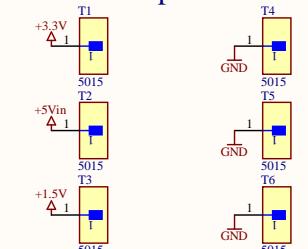
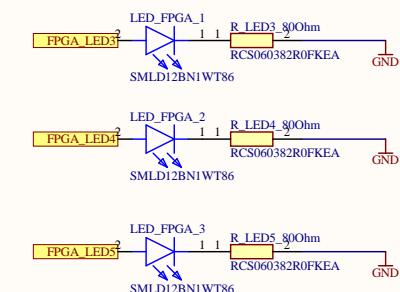
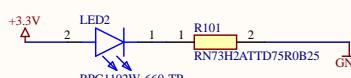
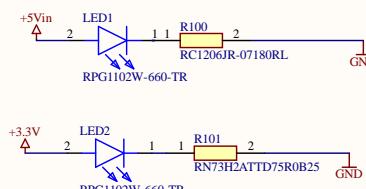
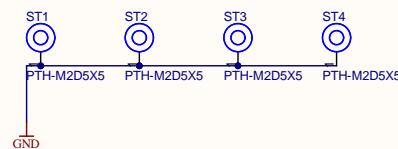


PIC (PIC18(L)F26K83)



Pull-ups for SPI and UART

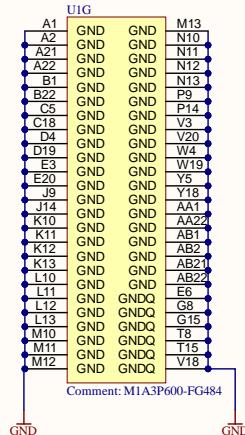
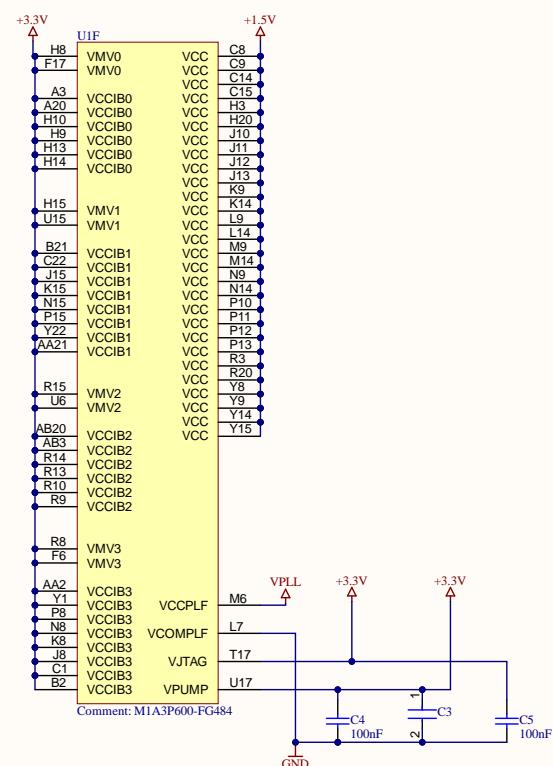


Surge voltage protectionOver/under-voltage detectionCurrent sensing1.5 V supply to FPGA coreTestpointsLEDsMechanical fixation points

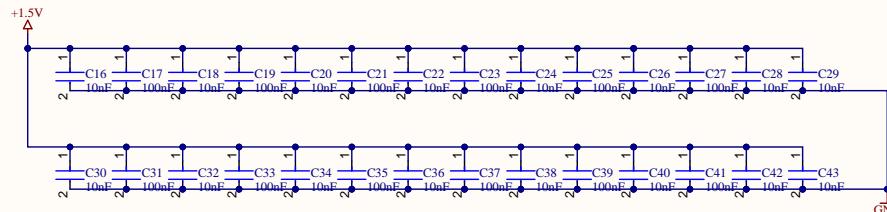
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A3	1.0	Power.SchDoc	EPFL
		Last updated 15/09/2021	SPACECRAFT
		Designers ML, PFA, EW	TEAM
			EPFL Spacecraft Team EPFL Space Center PPH335 station 13 CH-1015 Lausanne

FPGA POWER

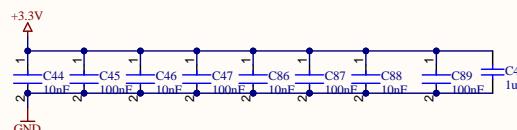
FPGA POWER PINS



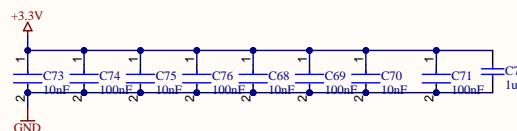
CORE DECOUPLING



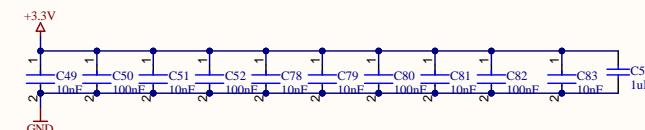
BANK0 DECOUPLING



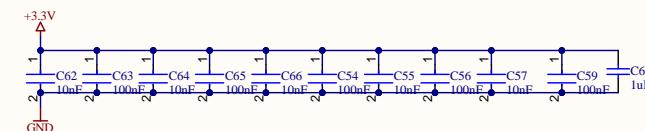
BANK2 DECOUPLING



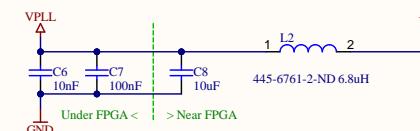
BANK1 DECOUPLING



BANK3 DECOUPLING

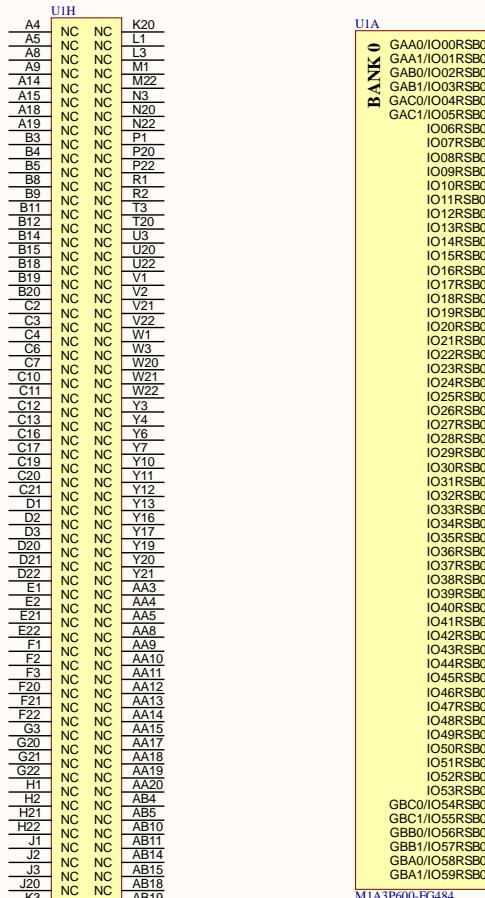


PLL DECOUPLING



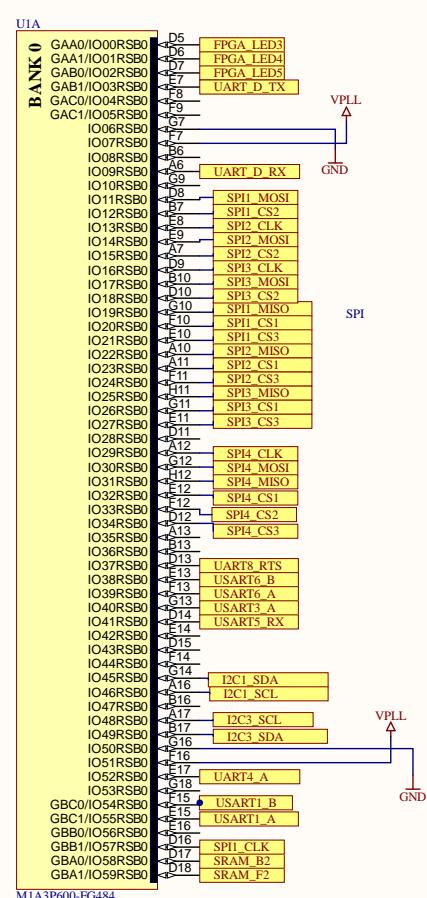
FPGA BANKs (left side, bottom view)

BANK0: SERIAL COMS



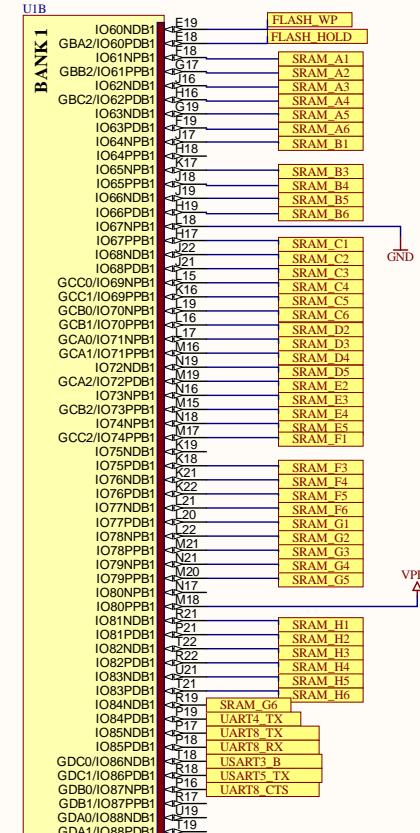
M1A3P600-FG484

BANK1: SRAM



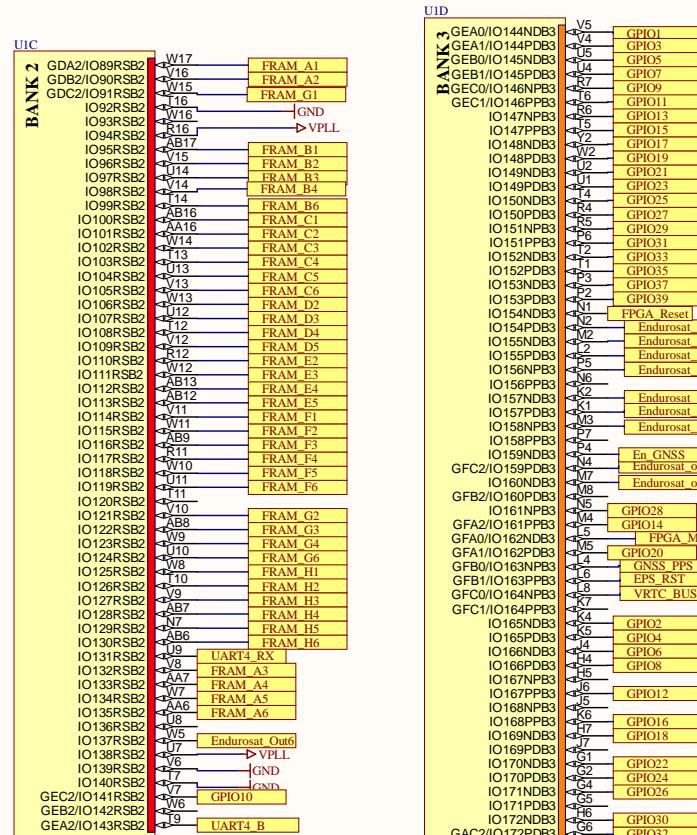
M1A3P600-EG48

BANK2: USER INTERFACE



Comment: M1A3B600_EG484

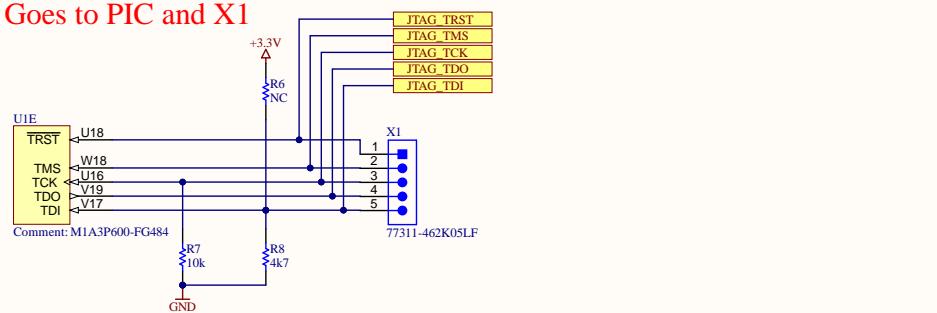
BANK3: USER IO



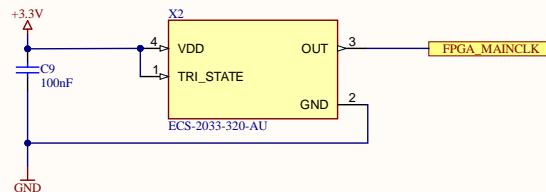
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JTAG

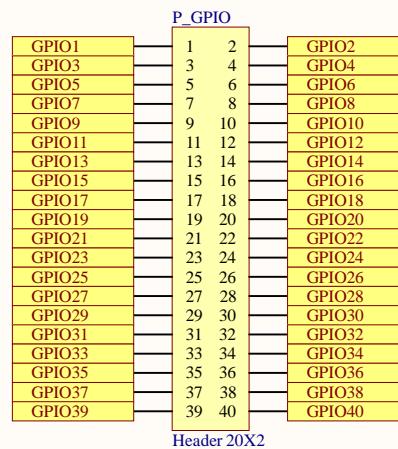
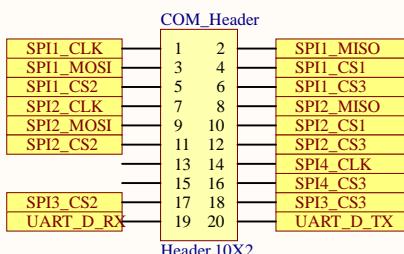
Goes to PIC and X1



FPGA OSCILLATOR (MAIN CLOCK): Sapristi board uses 32 MHz, same as on OBC on Astrocard sat.



Communication



Title Headers			Project CHESS - OBC		 EPFL
Size	Revision	File Name	Last updated	Designers	
A4	1.0	GPIO_Headers.SchDoc	10/07/2021	ML, PFA, EW	
Page 8 of 8					EPFL Spacecraft Team EPFL Space Center PPH335 station 13 CH-1015 Lausanne

