I) Purpose

The purpose of this assignment is to analyze and design the complete Differential Amplifier. In the 2nd, 3rd, and 4th reports the Improved High Swing Cascode Current Sink (figure 1), the Bootstrapped Current Source with Start-up Circuit (figure 2), and the Differential Pair Amplifier (figure 3) were analyzed and designed.

For this project another stage, the push pull amplifier, will be added to the Differential Pair Amplifier. Ideal components, such as biasing sources and current sources will be replaced with non-ideal their non-ideal counterpart, and deviations between the two will be compared. The Bootstrapped Current Source with Start-up Circuit will replace the ideal component in the Improved High Swing Cascode Current Sink. This Current Sink will be added to the Differential Pair Amplifier, replacing the ideal current source.

Finally, our design will be compared with another differential amplifier on the market, focusing on ultra-low power, and high speed.

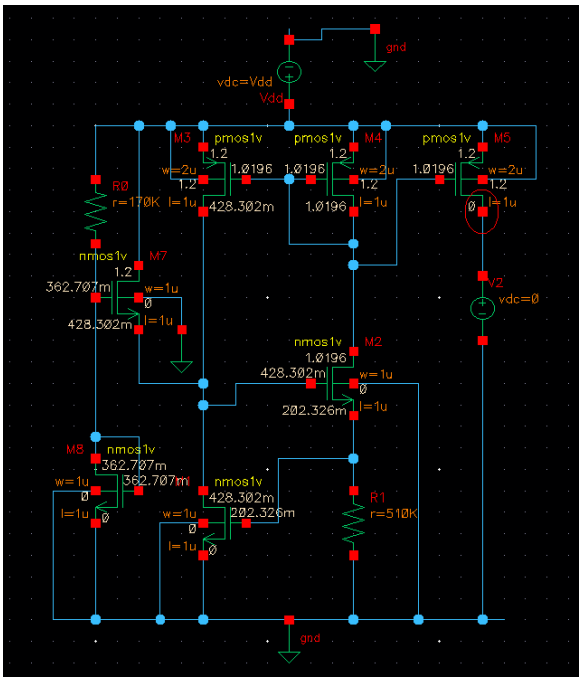

Figure 2: Bootstrapped Current Source with Start-up Circuit

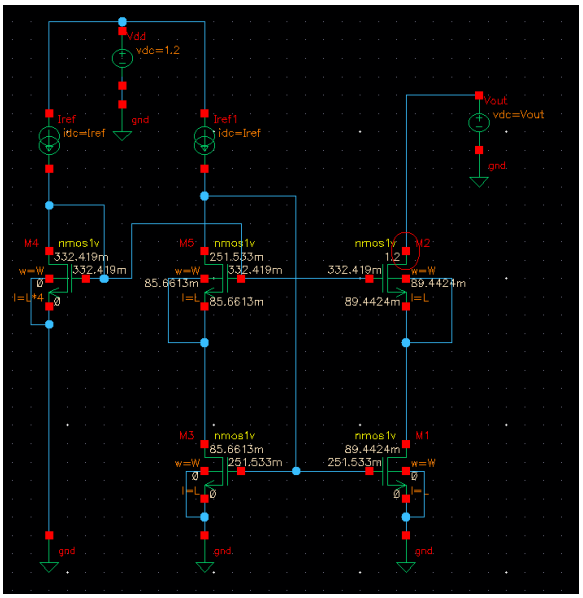

Figure 1: Improved High Swing Cascode Current Sink

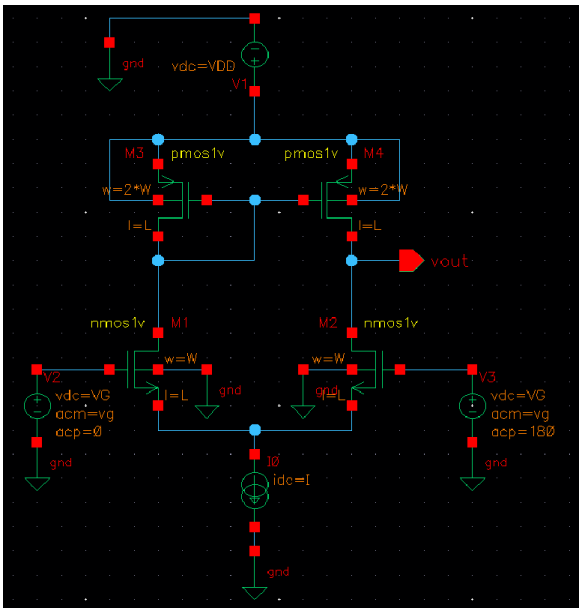

Figure 3: Differential Amplifier

II) Principle of Operation

In this section we will analyze the operating principles of the Push-Pull Amplifier (refer to figure 14). There are three main parts; the PMOS branch, the NMOS branch, and the output stage (figure 4).

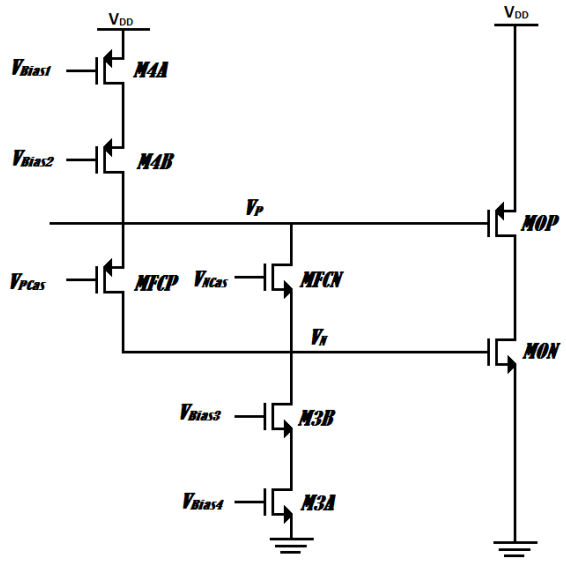

Figure 4: 2ND Stage, Push-Pull

II.1) PMOS Branch

The PMOS branch of the circuit, which includes transistors M4A, M4B, and MFCP is explained below, and includes equations (1.0 to 1.16)

The bias voltages of the PMOS branch are:

$$V_1 = V_2 = V_3 \tag{1.0}$$

The relationship of the currents through the PMOS branch for M4A, M4B, and MFCP are

$$I_1 = I_2 = \frac{I_3}{2} \tag{1.1}$$

respectively. It can be seen that M4A and M4B share the same current, while for MFCP the current is halved since a wire is connected in between M4B and MFCP (node V_P).

Now the bias voltages can be determined as:

$$V_{DD} - V_{bias1} = V_1 \tag{1.2}$$

$$V_H - V_{bias2} = V_2 \tag{1.3}$$

$$V_p - V_{pcas} = V_3 \tag{1.4}$$

Subtracting equations (1.2) and (1.3):

$$V_{DD} - V_H = V_{bias1} - V_{bias2} \tag{1.5}$$

Subtracting equations (1.3) and (1.4):

$$V_H - V_P = V_{bias2} - V_{pcas} \tag{1.6}$$

For the output stage, which consists of two transistors, MOP and MON, we can rearrange for the bias current:

$$I_{Out} = M * I_{bias} \rightarrow I_{bias} = \frac{I_{Out}}{M}$$

By design, we set the bias voltage for M4A equal to V_P so that the current can be controlled through the aspect ratio to create the factor of M.

$$V_{bias1} = V_p \tag{1.7}$$

Substituting (1.7) into equation (1.6), we can rearrange for another equation:

$$V_H - V_{bias1} = V_{bias2} - V_{pcas}$$

or (1.8)

$$V_H + V_{pcas} = V_{bias1} + V_{bias2}$$

Now, adding equations (1.5) with (1.8) will yields:

$$V_{bias1} = \frac{V_{DD} + V_{pcas}}{2} \tag{1.9}$$

And subtracting equations (1.8) with (1.5) yields:

$$2V_{TH} - V_{DD} + V_{pcas} = 2V_{bias2}$$

$$\rightarrow V_{Bias2} = V_H - \frac{V_{DD} - V_{pcas}}{2} \quad (1.10)$$

For MFCP, we can set the aspect ratio to one half, since current is split evenly in half through the branches. Thus, we can say:

$$I_{bias} = I_{SD} = 2\left(\frac{k}{2}\right)\left(\frac{W_p}{2L_p}\right)\left(V_p - V_{pcas} - |V_{TP}|\right)^2 \quad (1.11)$$

And defining Beta for the PMOS:

$$\beta_p = K\left(\frac{W_p}{L_p}\right) \quad (1.12)$$

Thus we can rearrange the bias current into another form by substituting equation (1.12) into (1.11):

$$I_{bias} = \frac{\beta_p}{2}\left(V_p - V_{pcas} - |V_{TH}|\right)^2 \quad (1.13)$$

We can now solve for V_{pcas} by rearranging equation (1.13):

$$V_{bias1} - V_{pcas} - |V_{TP}| = \sqrt{\frac{2I_{bias}}{\beta_p}}$$

$$V_{pcas} = \frac{V_{DD} + V_{pcas}}{2} - \sqrt{\frac{2I_{bias}}{\beta_p}} - |V_{TP}|$$

$$V_{pcas} = V_{DD} - 2\sqrt{\frac{2I_{bias}}{\beta_p}} - 2|V_{TP}| \quad (1.14)$$

There are 5 stages of transistors including M4A, M4B, MCFP, M3B, and M3A. Thus the voltage for the five stages can be partitioned five times by assigning:

$$V_{SDP} = V_{DSN} = \frac{V_{DD}}{5} \quad (1.15)$$

The condition for β_p selection can be derived using equation (1.15):

$$V_{DD} - V_H = \frac{V_{DD}}{5} \geq V_{ON} = \sqrt{\frac{2I_{bias}}{\beta_p}}$$

$$\beta_p \geq \frac{2I_{bias}}{\left(\frac{V_{DD}}{5}\right)^2} \quad (1.16)$$

II.2) NMOS Branch

The NMOS branch of the circuit, which includes transistors M3B, M3A, and MFCN is explained below, and includes equations (2.0 to 2.15).

The bias voltages of the NMOS branch are:

$$V_1 = V_2 = V_3 \quad (2.0)$$

The relationship of the currents through the NMOS branch for M3B, M3A, and MFCN are

$$I_1 = I_2 = \frac{I_3}{2} \quad (2.1)$$

respectively. It can be seen that M3B and M3A share the same current, while for MFCN the current is halved since a wire is connected in between M3B and MFCN (node V_N).

Now the bias voltages can be determined as:

$$V_{bias4} = V_1 \quad (2.2)$$

$$V_{bias3} - V_J = V_2 \quad (2.3)$$

$$V_{ncas} - V_N = V_3 \quad (2.4)$$

Subtracting equations (2.2) and (2.3):

$$V_{bias4} - V_{bias3} + V_J = 0 \quad (2.5)$$

Subtracting equations (2.3) and (2.4):

$$V_{bias3} - V_J - V_{ncas} + V_N = 0 \quad (2.6)$$

By design, we set the bias voltage for M3A equal to V_N so that the current can be controlled through the aspect ratio to create the factor of M.

$$V_{bias4} = V_N \tag{2.7}$$

Substituting (2.7) into equation (2.6):

$$V_{bias3} + V_{bias4} = V_J + V_{ncas} \tag{2.8}$$

Adding equations (2.5) with (2.8) will yields:

$$V_{bias4} = \frac{V_{ncas}}{2} \tag{2.9}$$

Subtracting equations (2.8) with (2.5) yields:

$$V_{bias3} - V_{bias4} + V_{bias4} + V_{bias3} - V_J = V_J + V_{ncas}$$

$$2V_{bias3} = 2V_J + V_{ncas}$$

$$V_{bias3} = V_J + \frac{V_{ncas}}{2} \tag{2.10}$$

For MFCN, we can set the aspect ratio to one half, since current is split evenly in half through the branches. Thus, we can say:

$$I_{bias} = \frac{I_{DS}}{2} =$$

$$\frac{1}{2} k \left(\frac{W_N}{2L_N}\right) (V_N - V_{ncas} - V_{TN})^2$$

$$I_{bias} = k \left(\frac{W_N}{2L_N}\right) (V_{GS} - V_{TN})^2 \tag{2.11}$$

And defining Beta for the NMOS:

$$\beta_N = K \left(\frac{W_N}{L_N}\right) \tag{2.12}$$

Substituting equation (2.12) into (2.11):

$$I_{bias} = \frac{\beta_N}{2} (V_N - V_{ncas} - V_{TN})^2 \tag{2.13}$$

We can now solve for V_{ncas} using (2.13):

$$V_{ncas} - V_{bias4} - V_{TN} = \sqrt{\frac{2I_{bias}}{\beta_N}}$$

$$\sqrt{\frac{2I_{bias}}{\beta_N}} = V_{ncas} - \frac{V_{ncas}}{2} - V_{TN}$$

$$\frac{1}{2} V_{ncas} = \sqrt{\frac{2I_{bias}}{\beta_N}} + V_{TN}$$

$$V_{ncas} = 2\sqrt{\frac{2I_{bias}}{\beta_N}} + 2V_{TN} \tag{2.14}$$

Referring to equation (1.15), which holds true for the NMOS branch as well, we can solve for the condition for β_N.

For M3A:

$$V_{DS} \geq V_{ON}$$

$$V_{ON} = V_{GS} - V_{TN}$$

$$V_{ON} = V_{bias4} - V_{TN}$$

From equation (2.9):

$$V_{ON} = \frac{1}{2} V_{ncas} - V_{TN}$$

From equation (2.14):

$$V_{ON} \geq \sqrt{\frac{2I_{bias}}{\beta_N}}$$

Using equation (1.15) and setting $V_{ON} = \frac{V_{DD}}{5}$, we can now proceed to solve for β_N:

$$\sqrt{\frac{2I_{bias}}{\beta_N}} \leq \frac{V_{DD}}{5}$$

$$\frac{2I_{bias}}{\beta_N} \leq \left(\frac{V_{DD}}{5}\right)^2$$

$$\beta_N \geq \frac{2I_{bias}}{\left(\frac{V_{DD}}{5}\right)^2} \tag{2.15}$$

III) Design Procedure

We wish to design an Active-Loaded MOS Differential Pair with ultra-low power, high bandwidth, and gain sustained at high frequencies; high speed. The goal will be to prioritize our design procedure for high speed applications (digital circuits) and high frequency applications (analog circuits) while maintaining a low current. The amplifier that we are using to compete with is a TI Ultra Low Power, Fully-Differential Amplifier, TSH4531.

III.1) Test-Bench: Determining μ_e for NMOS

To determine electron mobility, we can see from equation (2.15) we know that there is a lower bound for β_N, which is also equal to:

$$\beta_N = \mu_e C_{ox} \left(\frac{W}{L}\right)_n \qquad (3.0)$$

We can assume that $\mu_e C_{ox}$ is constant. We can determine it from a test bench consisting of a single MOSFET. From DC operating point analysis we can find BetaEff and since we know the aspect ratio of the transistor we are testing, the $\mu_e C_{ox}$ can be determined.

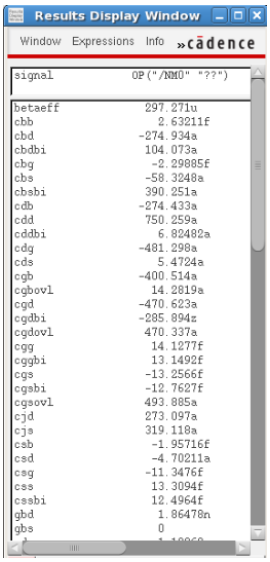

Figure 5: Results window for DC operating point of the test bench circuit

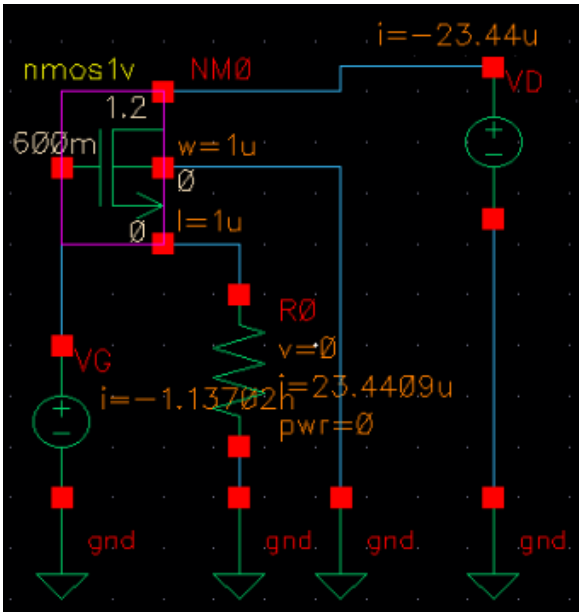

Figure 6: Test bench circuit for NMOS DC operating points

BetaEff (10^{-3})	Aspect Ratio	Vg (Volts)
3.3	0.1	1.2
4.1	0.1	0.6
4.3	0.1	0.3
4.3	0.1	0.2
0.223	1	1.2
0.297	1	0.6
0.313	1	0.2

Figure 7: Table for determining electron mobility

From this table, we can determine that the average value for electron mobility is around 300uA/V^2.

III.2) Test-Bench: Determining μ_p for PMOS

To determine the value for hole mobility of the PMOS, the same method from section III.1) can be used. The difference is that equation (1.16) is used determines the lower bound for β_P, which is also equal to:

$$\beta_P = \mu_p C_{ox} \left(\frac{W}{L}\right)_p \tag{3.1}$$

Similarly from step III.1) we have:

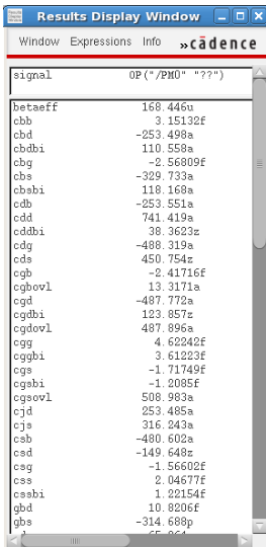

Figure 8: Results window for DC operating point of the test bench circuit

From a table similar to figure 7, we can determine that the average hole mobility has a value around 160uA/V^2.

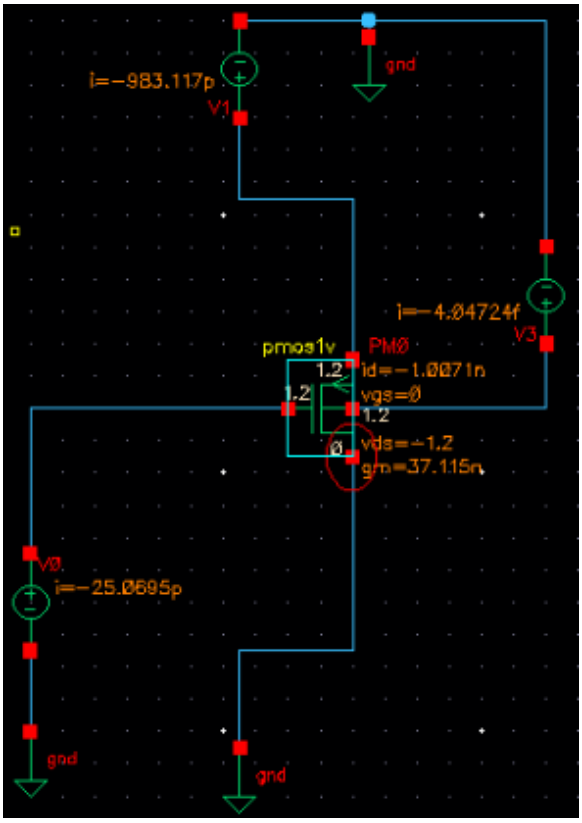

Figure 9: Test bench circuit for PMOS DC operating points

III.3) Determining the $\left(\frac{W}{L}\right)_N$

From equation (1.16), we can rearrange for the aspect ratio, since we know the $\mu_e C_{ox}$. Thus we can determine the lower bound of the NMOS aspect ratio:

$$\left(\frac{W}{L}\right)_N \geq \frac{2I_{bias}}{(\mu_e C_{ox})\left(\frac{V_{DD}}{5}\right)^2} \tag{3.2}$$

Since I_{bias} is the reference current of our output current, it is scaled down by a factor of M. From the TSH4531's data sheet our target output current I_{out} is 250 μA. Choosing M to be 32 we get:

$$I_{bias} = \frac{250\ \mu A}{32}$$

The resulting I_{bias} is equal to 7.81 μA. Plugging this into equation (3.2) will result in an upper bound for our NMOS aspect ratio:

$$\left(\frac{W}{L}\right)_N \geq \frac{2 * 7.81\mu}{(300\mu)\left(\frac{1.2}{5}\right)^2}$$

$$\left(\frac{W}{L}\right)_N \geq 0.9$$

For the NMOS aspect ratio we will choose $\left(\frac{W}{L}\right)_N = 1$.

III.4) Determining the $\left(\frac{W}{L}\right)_P$

Similarly for the PMOS, using equation (1.16) along with the determined I_{bias}:

$$\left(\frac{W}{L}\right)_P \geq \frac{2 * 7.81\mu}{(160\mu)\left(\frac{1.2}{5}\right)^2}$$

$$\left(\frac{W}{L}\right)_P \geq 1.70$$

For the PMOS $\left(\frac{W}{L}\right)_P = 2$ which satisfies our analysis, which is double the NMOS ratio which we determined previously.

III.5) Determining Lengths and Widths

Since we are looking to design a high-speed circuit we want to minimize the length of the transistors we are using. Smaller length leads to faster switching of the MOSFET. Since the unity-gain frequency is:

$$f_T = \frac{g_m}{s(C_{gs} + C_{gd})} \tag{3.3}$$

And C_{gs}, C_{gd} can be found according to

$$C_{gs} = \frac{2}{3} WLC_{ox} \tag{3.4}$$

$$C_{gd} = 0 \tag{3.5}$$

According to (3.4) in order to maximize the frequency of our amplifier (3.3) we need to minimize W, L and C_{ox}. Since we have the freedom to design L and W, we choose these values in conjunction with aspect ratios derived in sections ***III.4)*** and ***III.5).***

Choosing lengths of 100nm for our NMOS and PMOS leads to NMOS width = 100 nm and PMOS width = 200 nm, according to the derived aspect ratios.

III.6) Bias Voltage Design

In order to find a reasonable starting point for our push-pull stage we use the equations derived ***II) Principle of Operation***.

Beginning with equation (2.14), we can find V_{TN} from the DC operating point in Cadence:

$$V_{ncas} = 2\sqrt{\frac{2 * 7.81\mu}{300\mu * \frac{100n}{100n}}} + 2(260m)$$

$$V_{ncas} = 0.98\ [V] \tag{3.6}$$

From (2.9) we can find V_{bias4}:

$$V_{bias4} = \frac{0.98}{2}$$

$$V_{bias4} = 0.49\ [V] \tag{3.7}$$

The voltage V_J is across transistor M3A and is approximately equal to $V_{OV.}$ Since our power budget is determined by (1.15) to be 0.24 [V], V_J is also 0.24 [V] then we can determine V_{bias3} according to (2.10).

$$V_{bias3} = 0.24 + \frac{0.98}{2}$$

$$V_{bias3} = 0.73\ [V] \tag{3.8}$$

Using similar logic we can derive the PMOS bias voltages starting with V_{Pcas}. Since V_{TP} is determined by the DC operating point analysis to be around -220m volts and V_{DD} in this technology is 1.2 volts we can solve equation (1.14):

$$V_{pcas} = 1.2 - 2\sqrt{\frac{2 * 7.81\mu}{160\mu}} - 2|-220m|$$

$$V_{pcas} = 0.14\ [V] \qquad (3.9)$$

Next we determine V_{bias1} according to (1.9):

$$V_{bias1} = \frac{1.2 + 0.14}{2}$$

$$V_{bias1} = 0.67\ [V] \qquad (3.10)$$

And in a similar fashion to the NMOS case, the voltage across the source-drain of M4A, V_H, is equal to $V_{DD} - V_{OV}$, which equals to 0.96 volts. That is all we need to solve for V_{bias2} according to (1.10):

$$V_{bias2} = 0.96 - \frac{1.2 - 0.14}{2}$$

$$V_{bias2} = 0.43\ [V] \qquad (3.11)$$

Thus this concludes solving for all of the bias voltages we need to keep MFCN, MFCP, M3B, M3A, M4B, and M4A, respectively, in saturation. These voltages provide a starting point for our iterative analysis.

III.7) Output Stage Design

We require an output current on our design equal with the output current on the THS4531, which is 250 μA. We need to design the output stage in such a way to reflect our I_{bias} branch.

We have the equation$I_{Out} = M * I_{bias}$. In order to make this equation true, we need to **design** the circuit in such a way that the factor M is a multiple of the aspect ratios between:

$$\left(\frac{W}{L}\right)_P = M\left(\frac{W}{L}\right)_{P\_Out} \text{ and } \left(\frac{W}{L}\right)_N = M\left(\frac{W}{L}\right)_{N\_Out}$$

where $\left(\frac{W}{L}\right)_{P\_Out\ ,N\_Out}$ is the aspect ratios of the output transistors MOP and MON, respectively.

The design that allows for the use of this M factor will now be described. Because we designed the circuit using equations (1.7) and (2.7), V_{bias1} and V_{bias4} were assigned the voltages of V_P and V_N, respectively. This design decision results in the gate-source voltages of PMOS transistors M4A and MOP to be the same, i.e. $V_{SG\_M4A} = V_{SG\_MOP}$. Therefore the current through these transistors is now related through a factor M; the difference of the aspect ratios between them. With a similar logic the design of V_{bias4} to be equal to V_N fixes the gate-source voltages of transistors M3A and MON to be the same, i.e. $V_{GS\_M3A} = V_{GS\_MON}$. Therefore the current through the transistors is again related through a factor M of their aspect ratios. Finally this result can be elegantly summarized in:

$$I_{out} * M = I_{bias} \qquad (3.12)$$

Since in section ***III.3)*** we picked M = 32 and the NMOS aspect ratios were $\left(\frac{100nm}{100nm}\right)_N$ we can thus pick an aspect ratio for MON accordingly: $\left(\frac{3.2\mu m}{100nm}\right)_{N\_Out}$.

Similarly, for the PMOS pair since the aspect ratios picked in sections ***III.4)*** are in conjunction with ***III.5),*** which were $\left(\frac{200nm}{100nm}\right)_P$ we can then pick the MOP aspect ratio to be $\left(\frac{6.4\mu m}{100nm}\right)_{P\_Out}$.

III.8) Cādence Iterative Design Overview

As mentioned in the previous sections the calculated bias voltages simply provide a start to our design procedure. In Cādence we expect to slightly tweak these voltages to optimize the circuit.

We begin by replacing the ideal current source under the differential pair with a non-ideal current source designed in Assignments 2 and 3. Then inputting the theoretical voltages and doing DC operating point analysis.

The major goals here are matching V_{bias1} to V_P, V_{bias4} to V_N, and keeping the differential branch of the circuit (from Assignment 4) isolated from the new load stage (this means that no DC current is shared between the branches: I_{ref} only flows through M4A, M4B, MFCP||MFCN in parallel, M3B and M3A), power budgeting the $V_{DS,SD}$ which has a budget of 0.24 volts (shared between the 5 stages of cascaded transistors) and should approximately have a constant drop across all 5 stages, and we must evenly split the current in half across MFCN and MFCP transistors. Finally the ideal voltage sources must be replaced with non-ideal voltage sources CMOS voltage divider.

III.8.a) Non-ideal Current Source

In assignment 4 we used an ideal current source in our design. Now, to build a realistic amplifier, we must replace the ideal source with a non-ideal source created in assignment 2, and assignment 3.

In Assignment 3, we designed a Bootstrapped Current Source. The current source was designed to produce 1 μA of current (see figure 2 for the circuit topology). It was turned into a symbol and then inserted into Assignment 2.

Refer to the next figure which shows the bootstrapped current source inserted into the High Swing Cascode Current Source. Due to the fact that our current in Assignment 4 was designed for low power applications, we needed a total current supplied by our current source to be 16.4 μA. Thus a scaling factor of 16.4 in relation to our Bootstrapped source of 1 μA.

The scaling factor is implemented by widening the width of the transistors on the right side of the circuit in the diagram (M1, and M2). The resulting current was achieved and the circuit was transformed into a symbol which was used to replace the ideal current source in the differential pair.

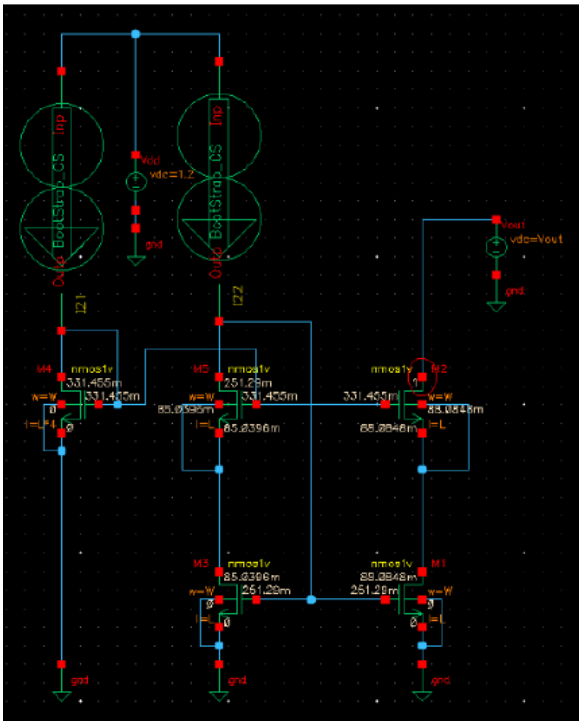

Figure 10: Bootstrapped Current source into the Improved-High Swing Cascode Current Source

III.8.b) Matching of Differential and Load stages

The first thing we noticed when we simulated the circuit is that the load stage of the circuit is leaking current into to the differential stage. This is a major concern since it results in a difference of current in our differential NMOS pair of assignment 4. This results in a severe drop of the CMRR. The solution to this is splitting the circuits up again, simulating and matching the voltages V_P, of our load stage to the output voltage V_{out} of our differential stage.

The easiest way to do this is by raising the width of the active-load (PMOS current mirror above

the differential pair). Eventually with a bit of adjusting, the voltages of V_P and V_{out} are equal and the circuits can be joined back together with nearly zero leakage current.

The result can be seen in the next diagram, notice the voltages 719.807m, in the left branch and 719.929m , in the right. The voltages in the two branches only differ by 0.122mV.

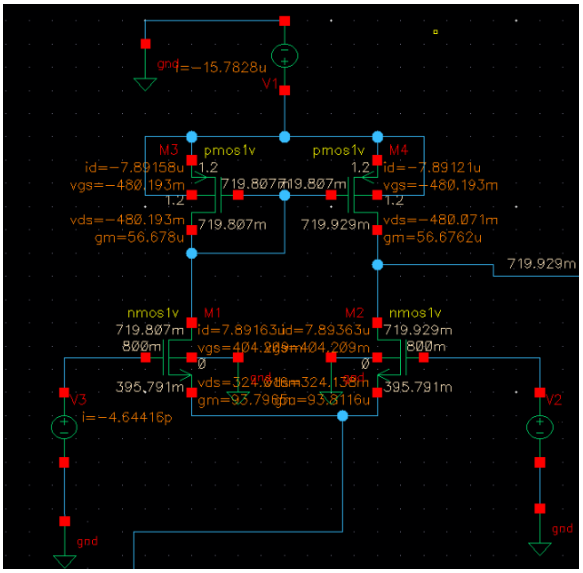

Figure 11: Perfectly Matched 1st and 2nd Circuit Stages

III.8.c) Calibrating Voltage Biases

The next task is to calibrate the voltage biases that we calculated previously in section ***III.6)***. In order to keep transistors M4A and M4B in saturation while maintaining the $V_P = V_{bias1}$ we must slowly raise or lower the bias voltages V_{bias1} and V_{bias2}. Note that these voltages also result in controlling the V_{SD} of the transistors which should be around 0.24 V.

By the same method, voltages V_{bias3} and V_{bias4} must be adjusted in order to keep their respective transistors in saturation, $V_N = V_{bias4}$, and $V_{DS} = 0.24$ V.

With some iterative analysis in Cādence we came up with the following voltages which are relatively close to our predicted voltages:

Bias Name	Final Voltage	Predicted Voltage
$\mathbf{V_{bias1}}$	686m	670m
$\mathbf{V_{bias2}}$	420m	430m
$\mathbf{V_{bias3}}$	650m	730m
$\mathbf{V_{bias4}}$	490m	490m

Table 1: Biasing for V1, V2, V3, V4; See figure 11

III.8.d) Balancing Split Current

The challenge here is that the current is in a parallel path through the 3rd stage of the transistors, MFCP and MFCN and would ideally split in two, but does not in practice. That is why the aspect ratios are designed in the following manner:

$$\left(\frac{W}{2L}\right)_N \; and \; \left(\frac{W}{2L}\right)_P$$

The NMOS and PMOS aspect ratios are divided by a factor of two since the current splits into two paths.

Unfortunately, in practice the current does not perfectly split in two, but this can be fine-tuned by the modification of V_{Pcas} and V_{Ncas} from the ideal voltages that were previously calculated in ***III.6).***The new voltages are summarized in the following table:

Bias Name	Final Voltage	Predicted Voltage
$\mathbf{V_{pcas}}$	220m	140m
$\mathbf{V_{ncas}}$	900m	980m

Table 2: V_{pcas} and V_{ncas} of final and predicted voltage see figure 11

The resulting current through the MFCP transistor was 4.058 μA and 3.910 μA in the MFCN branch, resulting in a difference of 0.148 μA or 1%.

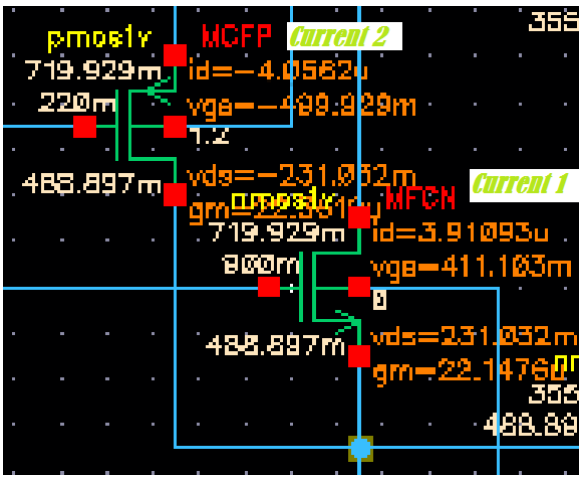

Figure 12: MFCP and MFCN Current Split

III.8.e) Overdrive Voltages

The total power budget of 1.2 V from V_{DD} is divided by the 5 stages. Thus V_{SD}=V_{DS}=0.24 V. This overdrive voltage was kept in mind with the designs of ***III.8.c)*** and ***III.8.d)***. The resulting $V_{DS,SD}$ values can be summarized:

V_{SD}, V_{DS} Name	Voltage
V_{SD_M4A}	275.57m
V_{SD_M4B}	204.501m
V_{SD_MFCP} / V_{DS_MFCN}	231.032m
V_{DS_M3B}	238.965m
V_{DS_M3A}	249.931m

Table 3: Overdrive voltages

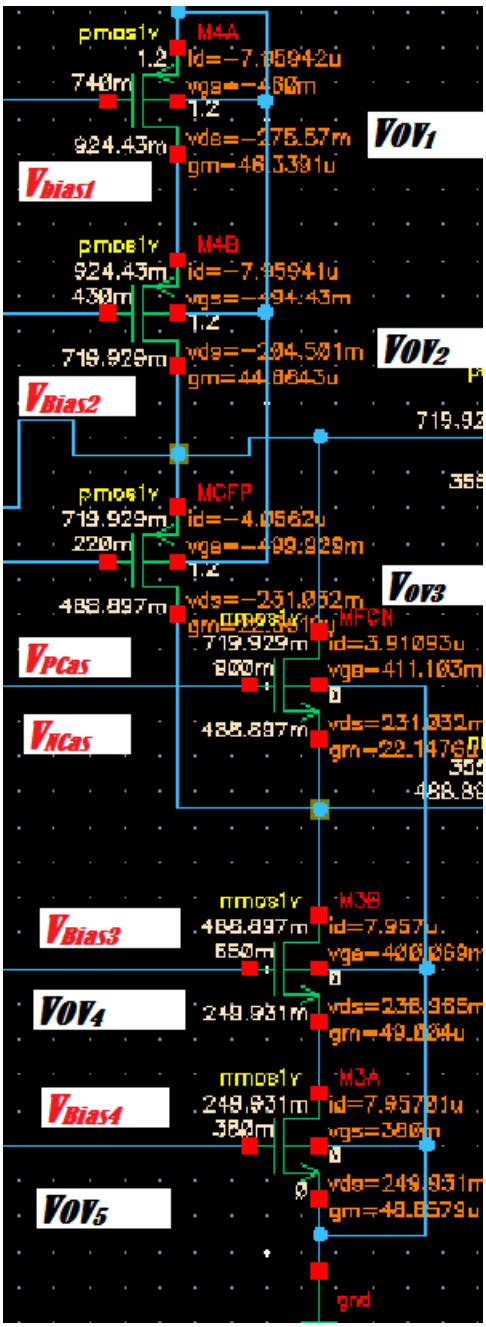

Figure 13: $V_{OV1\ ,\ 2,\ 3,\ 4,\ 5}$ and V_{Bias1}, V_{Bias2}, V_{NCas}, V_{PCas}, V_{Bias3}, V_{Bias4}

III.8.f) Non-ideal Voltage Sources

We must replace the ideal voltage sources with the non-ideal sources. This is the last step of the design. Here is the circuit element we use to replace the ideal voltage sources:

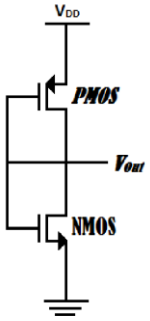

Figure 14: NMOS, PMOS Voltage Divider

The current equation through the NMOS is:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{TN})^2 \quad (3.13)$$

Since $V_{GS} = V_{Out} - 0$:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{Out} - V_{TN})^2 \quad (3.14)$$

The current equation through the PMOS is:

$$I_{SD} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - V_{Out} - |V_{TP}|)^2 \quad (3.15)$$

Since I_{DS} and I_{SD} are equal we can set equations (3.15) equal to (3.14).

$$\left(\frac{2W}{L}\right)_p (V_{Out} - V_{TN})^2 = \left(\frac{W}{L}\right)_N (V_{DD} - V_{Out} - |V_{TP}|)^2 \quad (3.16)$$

$$\sqrt{\left(\frac{2W}{L}\right)_p} * V_{Out} - \sqrt{\left(\frac{2W}{L}\right)_p} * V_{TN} = V_{Out}\left(\sqrt{\left(\frac{2W}{L}\right)_p} - \sqrt{\left(\frac{W}{L}\right)_N}\right) \quad (3.17)$$

Let $\beta_p = \left(\frac{2W}{L}\right)_p$ and Let $\beta_n = \left(\frac{W}{L}\right)_N$ and now we can rearrange for:

$$V_{Out}\left(\sqrt{\beta_P} + \sqrt{\beta_N}\right) = \sqrt{\beta_P} * V_{TN} + \sqrt{\beta_N}(V_{DD} - |V_{TP}|) \quad (3.18)$$

Isolating for V_{out}:

$$V_{Out} = \frac{\sqrt{\beta_P} * V_{TN} + \sqrt{\beta_N}(V_{DD} - |V_{TP}|)}{\sqrt{\beta_P} + \sqrt{\beta_N}} \quad (3.19)$$

Dividing top and bottom by $\sqrt{\beta_P}$ results our final equation:

$$V_{Out} = \frac{V_{TN} + \frac{\sqrt{\beta_N}}{\sqrt{\beta_P}}(V_{DD} - |V_{TP}|)}{1 + \frac{\sqrt{\beta_N}}{\sqrt{\beta_P}}} \quad (3.20)$$

Using DC Operating point analysis we can find the V_{TP} and V_{TN} values:

$$V_{TP} = -0.3$$

$$V_{TN} = 0.15$$

Using (3.20) and V_{TP} and V_{TN} values we can design the output voltage to be what we require from section ***III.8.c)*** and ***III.8.d)***. The circuit will be:

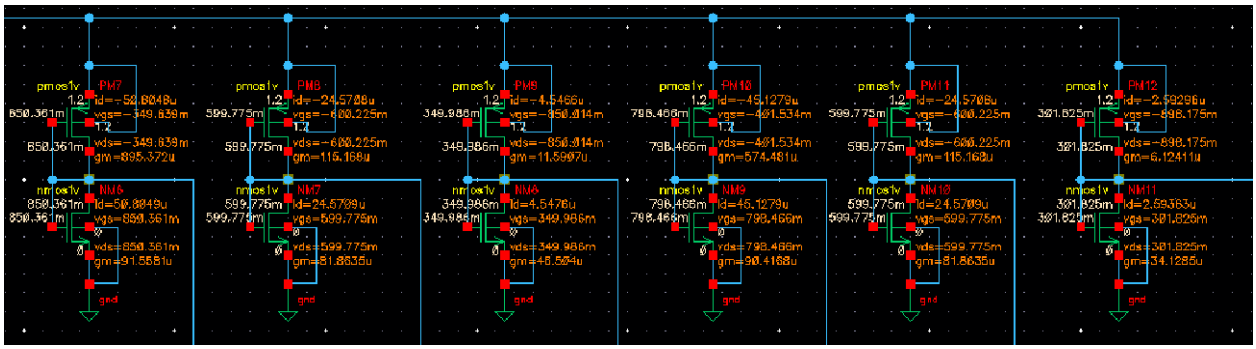

Figure 15: Non-ideal voltage sources

IV) Results and Discussion

Our goals are to design an ultra-low power, high gain and high frequency differential amplifier, made to compete with the Texas Instruments Ultra Low Power TSH4531 Fully Differential Amplifier. Below we will compare the two amplifiers.

	4EK4 Design	**TI TSH4531**
Gain (dB)	32	20
Bandwidth (Mhz)	68	2.7
Output Current (uA)	250	250
Voltage (V)	1.2	2.5-5.5
Slew Rate (V/usec)	200	200
Power Consumption (mW)	0.33	0.63 min, 1.38 max

Table 4: Comparison of our design to the TI TSH4531 (datasheet can be found here in reference [1])

From this table, we can see that our design surpasses the characteristics of the TI TSH4531. We can maintain a lower voltage, with the same slew rate and output current but have higher gain, and much faster bandwidth.

After adding the push-pull output stage of the amplifier, we have seen a significant drop in terms of the bandwidth, but the gain has increased. The drop in bandwidth makes sense because adding the output stage increases the capacitance of the amplifier.

Adding the non-ideal current source further decreases bandwidth because R_{out} is not infinite, this also decreases the CMRR.

When replacing the ideal voltage sources with the non-ideal voltage sources (CMOS voltage divider in figure 14), we noticed no significant bandwidth or drop in gain. This is expected, because the push-pull design is accurate enough to sustain the required voltages.

The resulting gain graph is shown below shows the gain and frequency bandwidth.

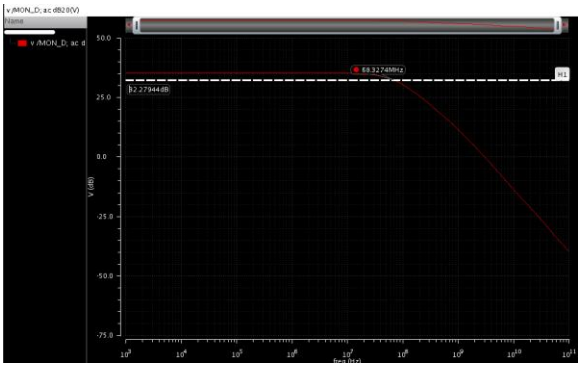

Figure 16: Gain and Frequency

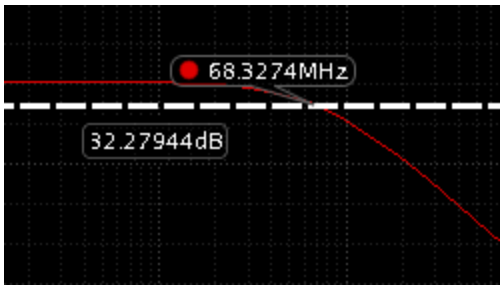

Figure 17: Zoomed image of figure 16

For the slew rate, it is chosen to be 200 V/usec, which is the same as the TSH4531.

$$SR = \frac{I_{Out}}{C_L}$$

SR and C_L can be verified with the above equation. Also, in Cādence we can do a transient analysis using a square wave generator (voltage source with a square wave), and determining the slope of the output waveform, according to these diagrams below.

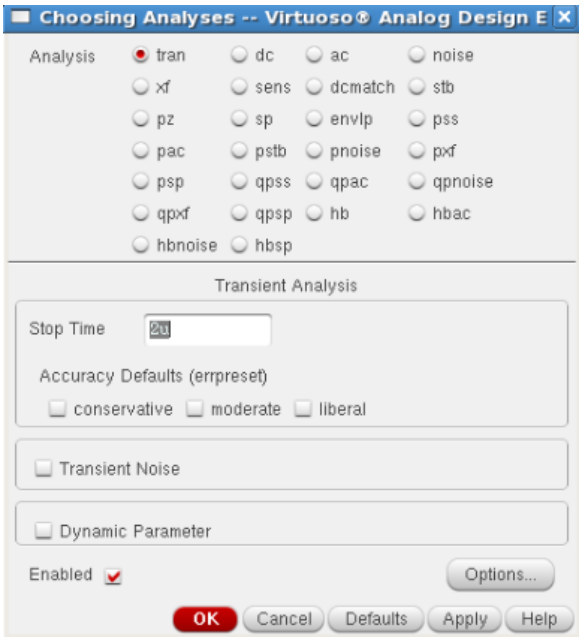

Figure 18: Choosing Analyses - Transient

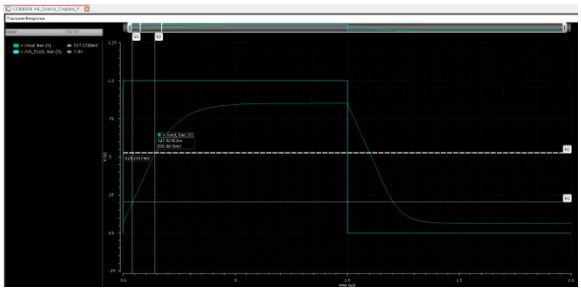

Figure 19: Transient Analysis for Slew Rate

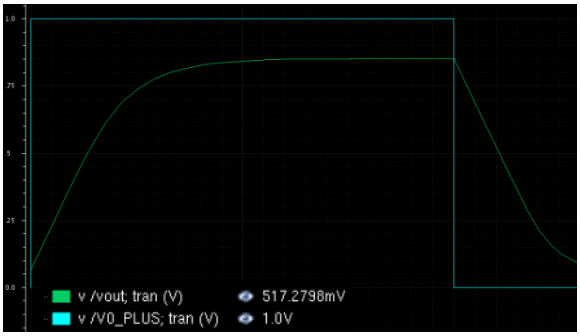

Figure 20: Zoomed image of figure 18

The phase margin can be calculated at the zero dB line, and drawing a vertical line intersecting with the phase curve.

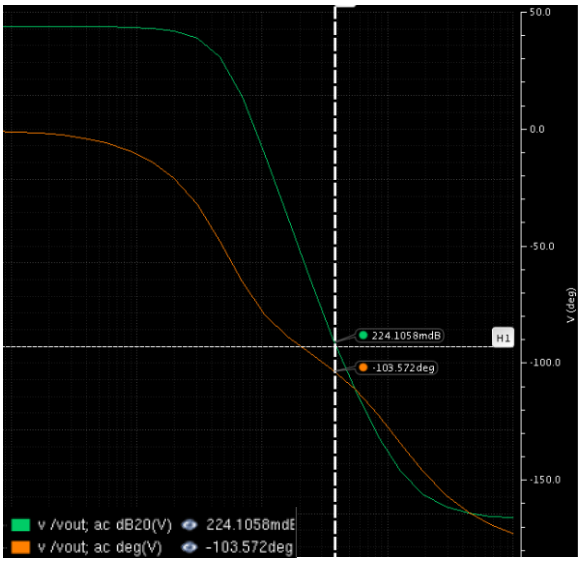

Figure 21: Phase, Magnitude Margin

The gain margin is shown below.

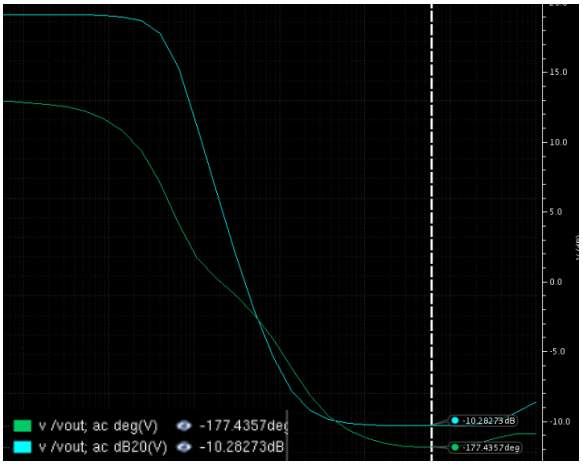

Figure 22: Gain Margin

To obtain CMRR, we need to get the common mode gain and the differential gain, and take the ratio of the two.

$$\text{CMRR} = \frac{\text{A}_\text{d}}{|A_{cm}|}$$

The CMRR is the differential amplifiers ability to reject unwanted input signals such as noise. A very good differential amplifier has very high CMRR, and in an ideal case it would have infinite CMRR.

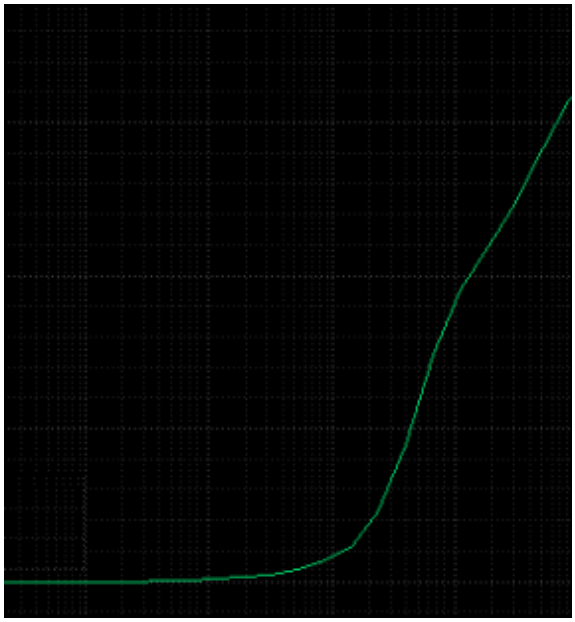

Figure 23: Common Mode Gain

We can see that the common-mode gain is rising when beyond a certain frequency, lowering our common-mode rejection ratio. For our operating frequency our CMRR is 91dB.

Our final design variables are:

Design Variables

	Name	Value
1	L	100n
2	W	350n
3	Ln	100n
4	Ln_out	100n
5	Lp	100n
6	Lp_out	100n
7	Vbias1	740m
8	Vbias2	430m
9	Vbias3	650m
10	Vbias4	380m
11	VnCas	900m
12	VpCas	220m
13	Wn	100n
14	Wn_out	3.2u
15	I	16.4u
16	VDD	1.2
17	VG	800m
18	l_nmos	100n
19	l_pmos	200n
20	vg	1
21	w_nmos	200n
22	w_pmos	400n
23	Wp_out	Wn_out*2
24	Wp	Wn*2

Figure 24: Design Variables

Discussing the push-pull amplifier, and why it is called that, by inspection and iteration. When i_{in} increases (a.k.a. ↑), charge accumulates, thus V_{SG} ↑, and MOP turns off, and then since V_{SG} ↑ and I_f ↑ then V_{ON} ↑, and MON turns on. When i_{in} decreases (a.k.a. ↓), the V_{SG} ↓, thus If ↓ and MOP turns on, and then since If ↓, I_{bias} must maintain its V_{min} to stay on, and pulls charge from MON. Thus V_{ON} ↓ and MON turns off.

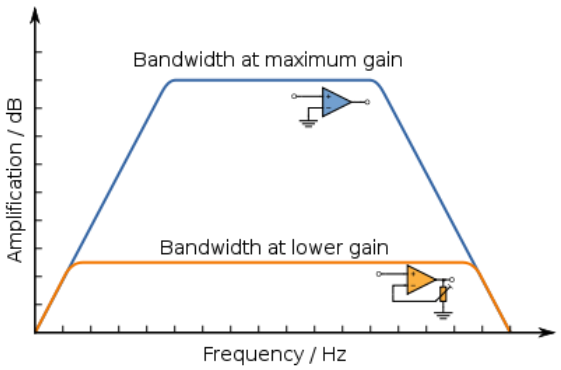

Figure 26: Trade-Offs [2]

Thus from our iterative design procedure, we can say that design trade-offs are a challenge to balance. Figure 25 on the left describe the trade-offs of having lower gain and higher bandwidth, and having higher gain and lower bandwidth. Another is increasing current, which increases power consumption, but leads to higher gain and bandwidth.

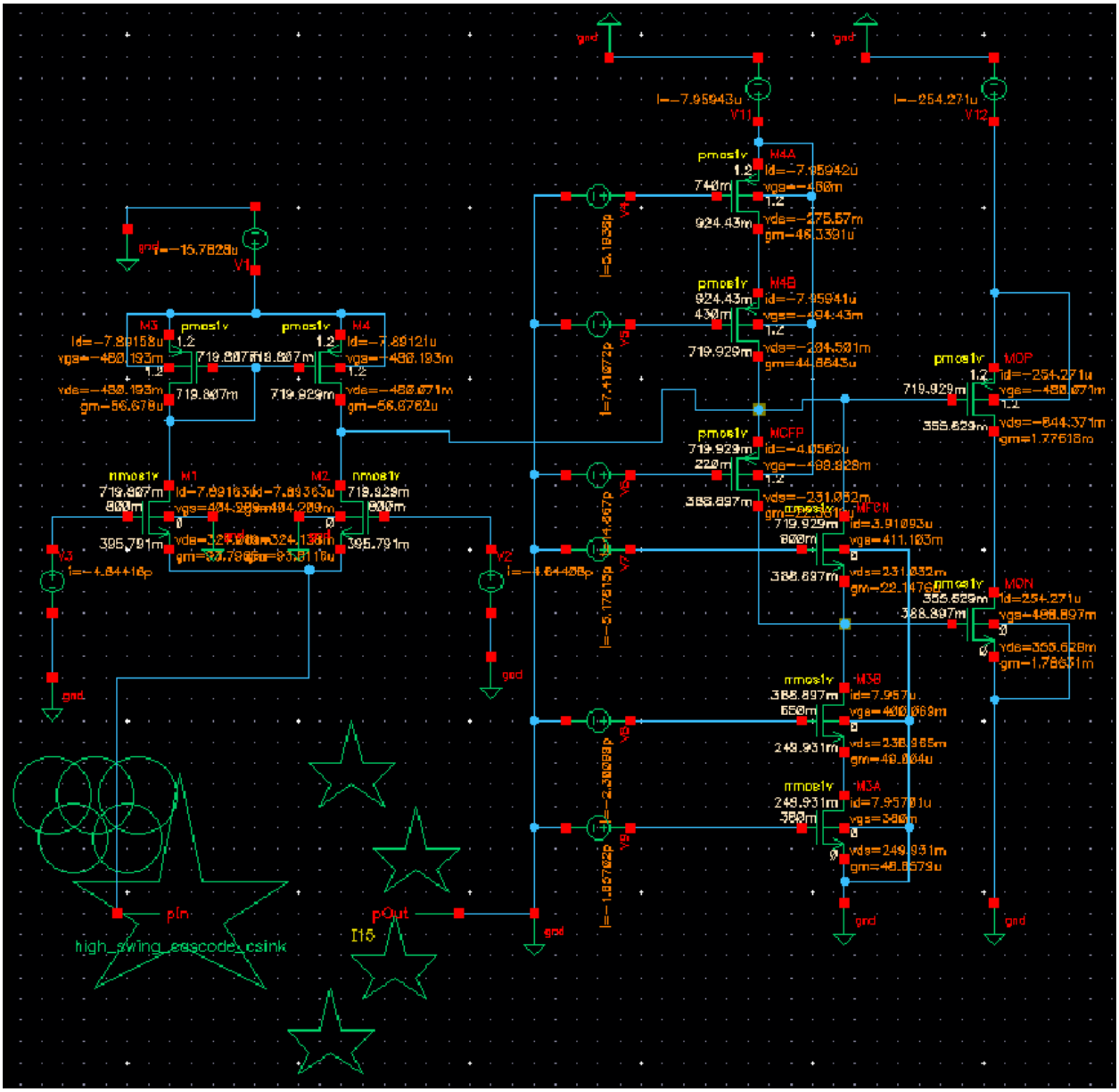

Figure 25: Overall Final Circuit with DC Operating Points

V) Conclusion

Thus our Differential Amplifier design discussed above meets our design goal of an ultra-low power amplifier, with an output current of 250 uA. Our design also features an excellent gain and bandwidth frequency for our application. Using design techniques learned in class we have achieved our design goal of surpassing a differential amplifier with the same design goals as us; the TI TSH4531.

Figure 24 can be referred to for the design variables, such as the aspect ratios, the I_{DS}, etc. Our power consumption is found through the current in the three branches, which would be 0.33mW.

The design can still be improved. This can be accomplished with further adjustments to the circuit such as changes to the aspect ratio, cascading, more precise voltage biasing, and more iterations etc. This would improve the gain, bandwidth, and potentially the slew rate.

This project was an interesting way to learn about microelectronics and amplifier design. We have developed an appreciation for the difficulty and non-trivial task of designing, where theoretical results do not always represent accurate physical models, but rather a good starting point. It was fun working with Cādence, and we learned a lot about the program. This class opened a new door of electrical and computer engineering.

Special thanks to our instructor Dr. Chen for giving us motivation and guidance throughout the project and the difficult times. As well, we would like to thank our TA his time and patience, for example coming into the lab outside of his working hours and the tough times dealing with McMaster security and letting in the lab when all hope was lost (Dec 28th).

We would also like to thank our body and mind for not deteriorating from lack of sleep, food, and physical and social activities during the semester. These thanks are also extended to family and friends (and/or girlfriend) who very understanding of our pain and were patient with us.

References

[1] "Ultra Low Power, Rail-to-Rail Output, Fully-Differential Amplifier". Texas Instruments, n.d. Web. 10 Dec. 2013. <www.ti.com/lit/ds/symlink/ths4531.pdf>.

[2] *Wikipedia*. Wikimedia Foundation, n.d. Web. 23 Dec. 2013. <http://en.wikipedia.org/wiki/File%3AGain-bandwidth_product.svg>.