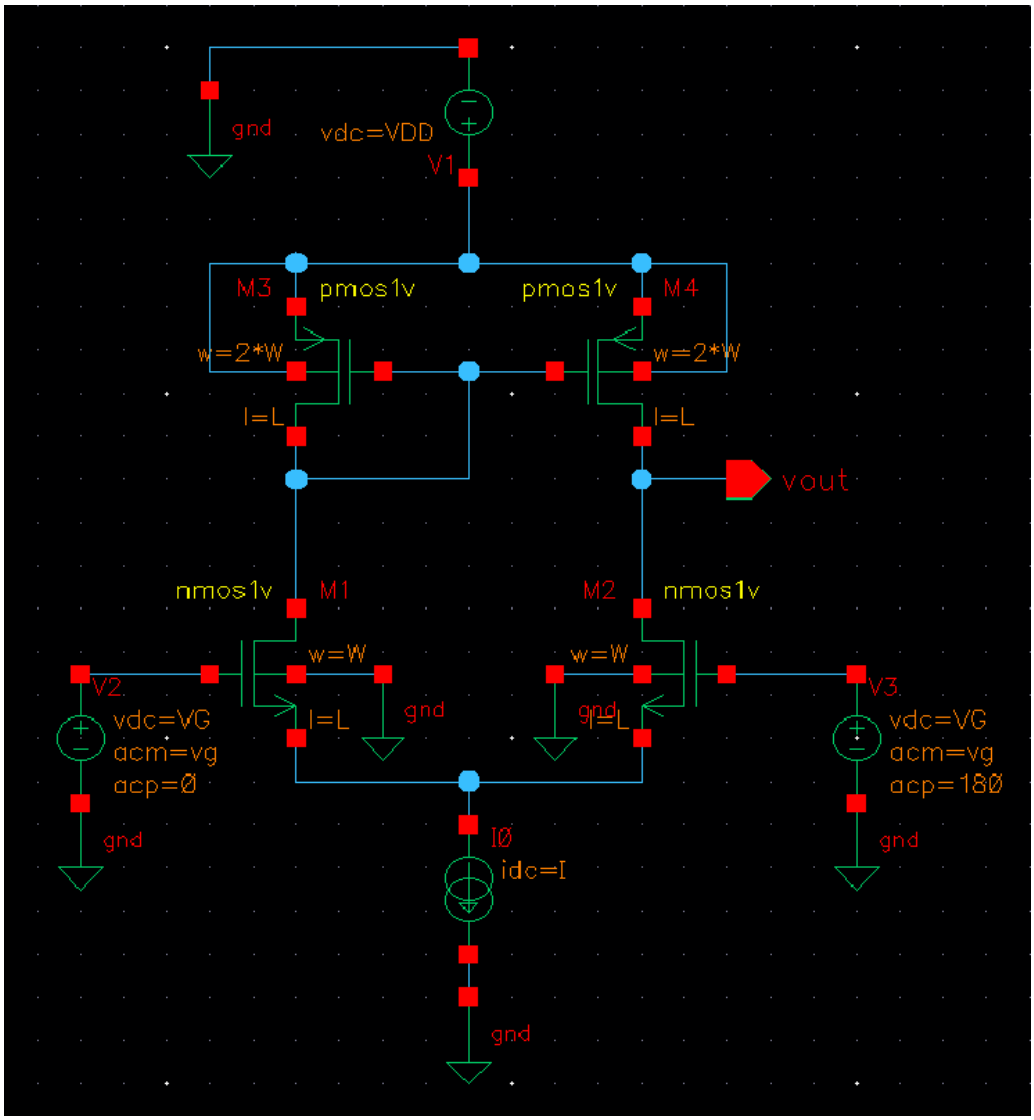
Purpose:

Our purpose is to design the first stage of a differential amplifier. We will be using a differential active-loaded MOS pair. First we will be analyzing the small signal of the differential and common gain of our configuration and the circuit's CMRR, see **Analysis** section. Then we will briefly talk about the higher frequency behaviour of MOS transistors and circuit. This will lead into the **Design** of the amplifier, talking about the design parameters we have and how to choose them. We will be going over the biasing conditions, length choices of M1 and M2, aspect ratios of the four transistors, maximum and minimum current restrictions, and dealing with gain/frequency tradeoffs.

Figure 1. Active-Loaded MOS Pair[1]



Analysis:

Large Signal:

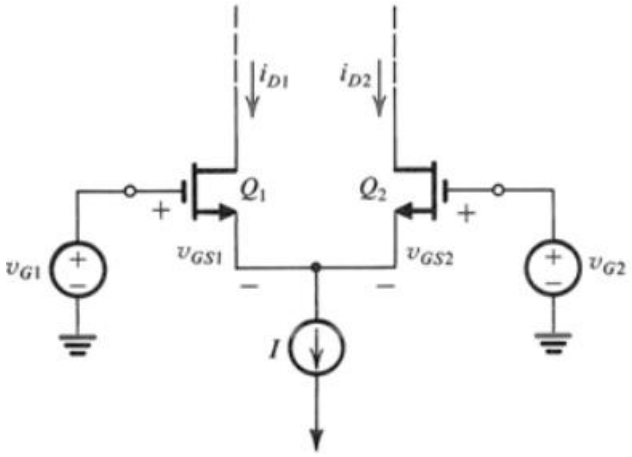


Figure 2. Large Signal Analysis

$$i_{D1} = \frac{1}{2}k_n'\frac{1}{2}(v_{GS1} - V_t)^2 \quad (1.0)$$

$$i_{D2} = \frac{1}{2}k_n'\frac{1}{2}(v_{GS2} - V_t)^2 \quad (1.1)$$

$$v_{GS1} - v_{GS2} = v_{G1} - v_{G2} = v_{id} \quad (1.2)$$

Equations (1.0) and (1.1) are our current equations for both branches. We can take the square root of both equations and substitute (1.2). This results in

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2}k_n'\frac{W}{L}}\, v_{id} \quad (1.3)$$

Since sum of i_{D1} and i_{D2} is equal to I, we can square both sides of (1.3), and substitute $i_{D2} = I - i_{D1}$. This leads to the solution of a quadratic equation, resulting in

$$i_{D1} = \frac{I}{2} \pm \sqrt{k_n'\frac{W}{L}I}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n'\frac{W}{L}}} \quad (1.4)$$

At the bias point, $v_{id} = 0$ this results in:

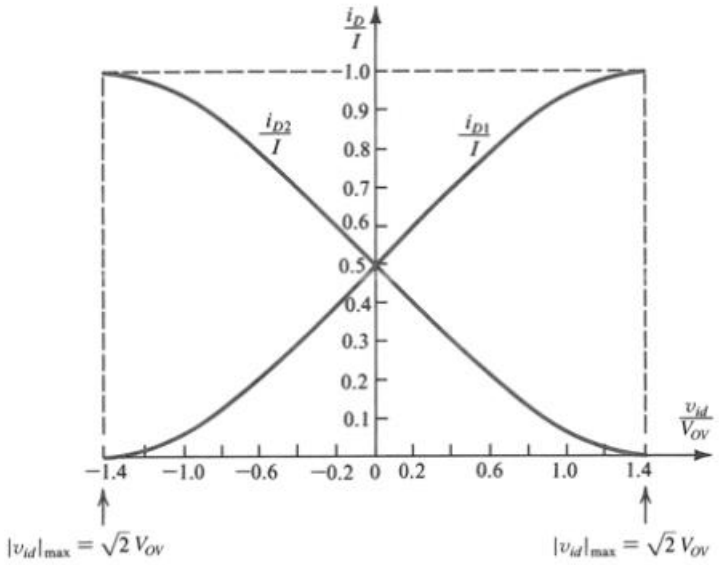
$$i_{D1} = i_{D2} = \frac{I}{2} \quad (1.5)$$

$$\frac{1}{2}k_n'\frac{1}{2}(V_{GS}-V_t)^2 = \frac{1}{2}k_n'\frac{1}{2}(V_{OV})^2 = \frac{I}{2} \quad (1.6)$$

$$i_{D1,D2} = \frac{I}{2} \pm \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2} \quad (1.7)$$

These equations can be plotted on a graph of $i_D \setminus I$ and $v_{id} \setminus V_{OV}$. It results in the following figure.

Figure 3[1]. Normalized plots of currents in MOS differential pair

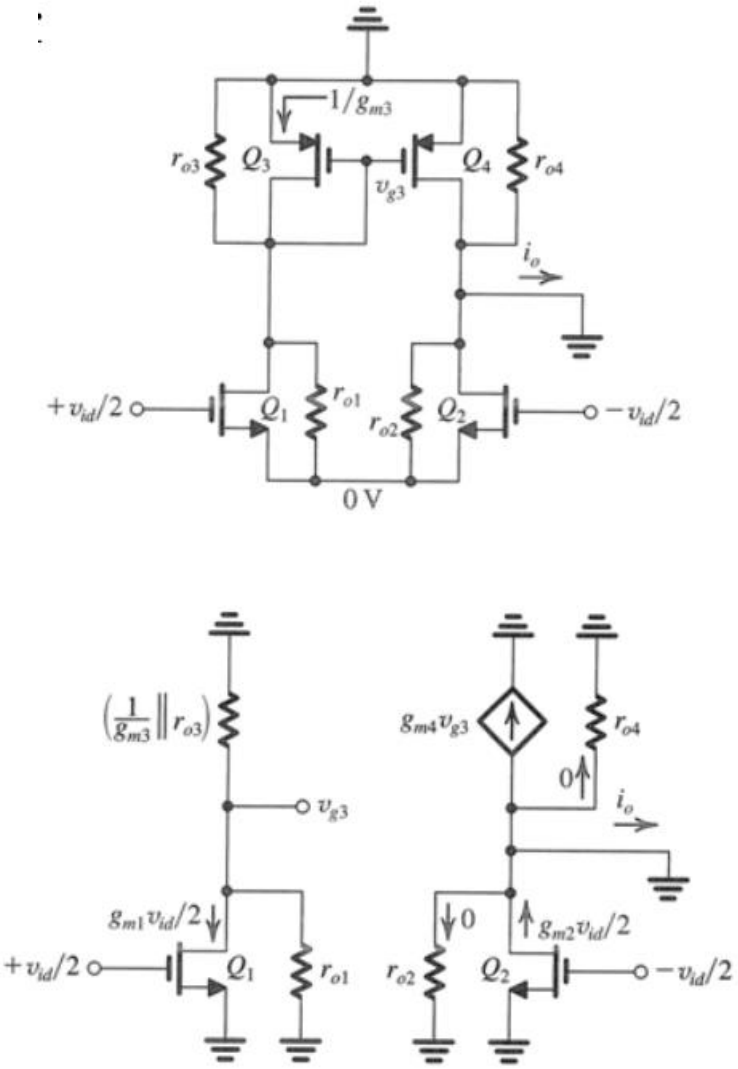


As well in the large signal we are responsible for biasing the two NMOS transistors in order to pick certain g_m values. This will be discussed in the **Design** section.

Small Signal:

There are two parameters of merit here, common mode gain and differential gain. These lead to defining the common mode rejection ratio (CMRR) for this amplifier configuration.

Figure 4[2]. Large and Small Signal Model for differential analysis



Differential Gain:

Differential voltage is defined by

$$v_{DI} = \frac{v_{I1} - v_{I2}}{2} \qquad (2.0)$$

The currents add at the output branch of the circuit according to

$$i_o = i_{d1} + i_{d2} = 2i_d \qquad (2.1)$$

The voltage at the output node is the current i_{out} multiplied by the parallel resistances of r_{ds2} and r_{ds4}.

$$v_{out} = i_{out}(r_{ds2}||r_{ds4}) \quad (2.2)$$

$$i_d = g_m \frac{v_{di}}{2} \quad (2.3)$$

Combining (2.1) into (2.3) and (2.2)

$$A_d = g_{m1,2}(r_{ds2}||r_{ds4}) \quad (2.4)$$

Common-Mode Gain:

We apply a common small signal to both input terminals. Due to the symmetry of the circuit we can say

$$V_{out} = \frac{-1}{g_{m3.}}(i_{c1}) \quad (2.5)$$

$$V_s = 2\, i_{c1}\, r_{tot} \quad (2.6)$$

Where r_{tot} is the resistance of the current source (Note: This isn't shown in **Figure 4**). We can make a loop equation using KVL

$$-\frac{v_{ci}}{2} + v_{gs1} + v_s = 0 \quad (2.7)$$

$$v_{gs1} = \frac{i_{c1}}{g_{m1}} \quad (2.8)$$

We can place (2.8) into (2.7) and (2.6) into (2.7). Then we can isolate for i_{c1} and replace i_{c1} with equation (2.5). We can then rearrange for $\frac{v_{out}}{v_{ci}} = A_{cm}$.

$$A_{cm} = \frac{-1}{4 \times g_{m3} \times r_{tot}} \quad (2.9)$$

Design:

In this circuit there are quite a few parameters we need to consider for our design. The design is driven by the need for our first stage of the amplifier to be able to accept and amplify our signal. Therefore we are mainly looking for high gain and high frequency application. When we will have to sacrifice we will be picking high frequency over gain though.

The parameters in the choice of the designer are the aspect ratios of all transistors M1, M2, M3 and M4, the current source I_{ss} and the gate voltages of the M1 and M2 transistors. We begin by a exploring the perfect biasing for out transistors.

i) NMOS Biasing Design:

We know the current source we will eventually use is not ideal, meaning it has some V_{min} we must obey. From assignment 3, the bootstrapped current source, was found to have a minimum voltage of around 180mV. This requires us to have $V_{s1,s2}$ > 180mV in order to keep our current source active, we will assume a voltage requirement greater than 200mV, for simplicity. V_{DD} is fixed at 1.2V, with our V_{min} constraint we now have a total voltage budget of: 1.2V – 0.2V = 1V over both the NMOS and PMOS transistors (M1 and M4).

In order to properly bias M1 we require it to be ON from this equation.

$$V_{GS1} \geq V_{th1} \qquad (3.0)$$

$$V_{G1} - V_{S1} \geq V_{th1} \qquad (3.1)$$

Equation (2.3) can be rearranged to get

$$V_{G1} \geq 0.2 + 0.2 \qquad (3.2)$$

With V_{th1} approximately equal to 0.2 V (see assignment 3), we now have a lower bound for V_{G1} = 0.4 volts.

Since our budget is 1V we must choose how we want to spread out the voltage. We would want the higher voltage drop to be across our PMOS since it is our active load, we want a high r_{ds4} since it would increase our gain from Equation (#.#). We choose to place a 0.4 V drop across V_{DS1} and therefore 0.6 V drop across V_{DS4}. This design leads to

$$V_{DS1} \geq V_{GS1} - V_{th1} \qquad (3.3)$$

$$0.4 \geq V_{G1} - 0.2 - 0.2 \qquad (3.4)$$

$$V_{G1} \leq 0.8 \qquad (3.5)$$

This now places an upper bound on our V_{G1}. This means our V_{G1} is bounded by

$$0.4 \leq V_{G1} \leq 0.8 \qquad (3.6)$$

From assignment one, we know that decreasing L will increase our gain and decrease our r_{ds} the following relationships were found from assignment one:

$$g_m \propto \frac{1}{L}, r_{ds} \propto L \qquad (3.7)$$

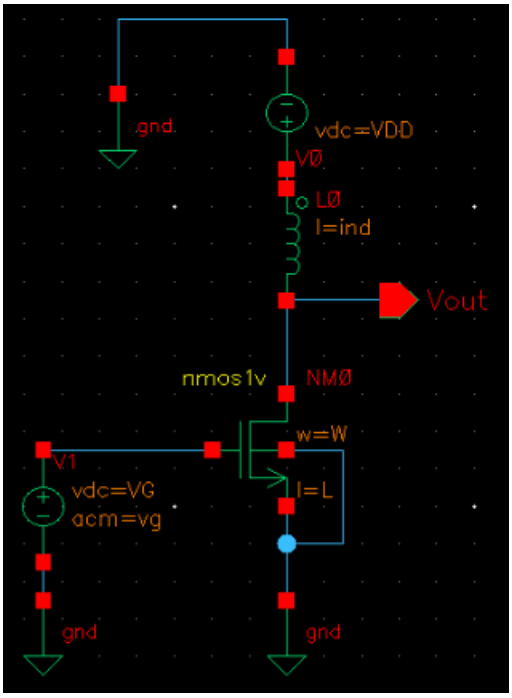
$$g_m \propto W, r_{ds} \propto \frac{1}{W} \qquad (3.8)$$

These conclusions would lead us to believe that we would want a high Width and low Length transistor M1, but we must keep in mind that we are not dealing with low frequency gain but would want to keep our gain at higher frequencies. The modern transistor has had its Length reduced to ~18 nm, dealing us to believe that high frequency would require smaller length transistor. Let's combine our V_{G1} bound equation (3.6) and explore the frequency response.

ii) NMOS Length Design:

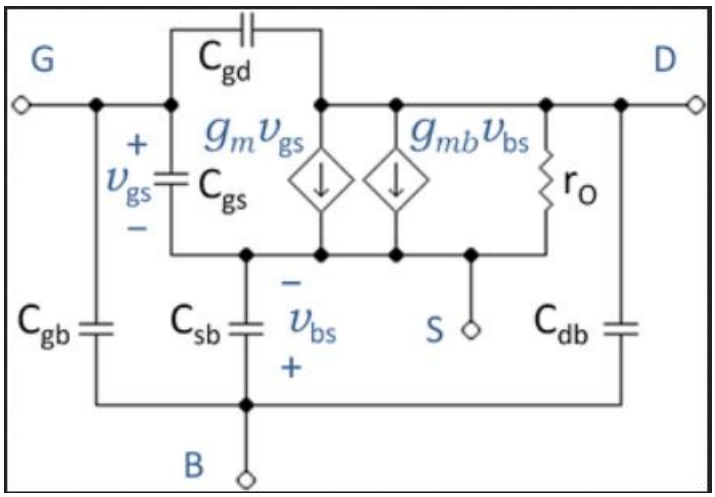
We are going to explore an isolated transistor to see how it behaves under a sweep of frequencies. We will need a DC biasing but will also need a direct output to V_{out} once we are in the AC domain. The circuit element which provides this is an inductor – it has 0 impedance at DC and infinite impedance at AC. Our V_{DD} voltage for this case will be 0.6 V since that is what our budget design dictates. The following circuit will be used for the frequency sweep in Cadence

Figure 5. Circuit setup for Gate Bias Test and Frequency Sweeps



In this circuit configuration we will use Cadence's AC analysis to find the optimal NMOS length. From circuit theory we know that there are internal capacitances in our MOSFET, between gate and drain, gate and source as well gate and body, source and body and finally base and drain. See the next figure

Figure 6. Internal Capacitors of a MOSFET



As frequency increases these capacitors will eventually become short circuits according to

$$Z = \frac{1}{jwC} \qquad (3.9)$$

When the C_{gs} capacitor shorts then we have a short circuit between gate and source making V_{gs} = 0, and in turn making our gain = 0.

So from that we know that eventually all MOSFETs will drop their gain. Again from circuit theory we know that charging a capacitor is easier when it is smaller

$$T_{charge} \propto L \qquad (3.10)$$

Therefore we are expecting a smaller length NMOS to be able to hold gain for a larger frequency and drop to 0 after a larger bandwidth. Cadence proves these theories. In the following diagram we will see that decreasing length of the NMOS the low frequency gain is dropping but the bandwidth is increasing for the shorter channel MOSFET

Figure 7. NMOS Length Design. Lengths of 100n to 1u.

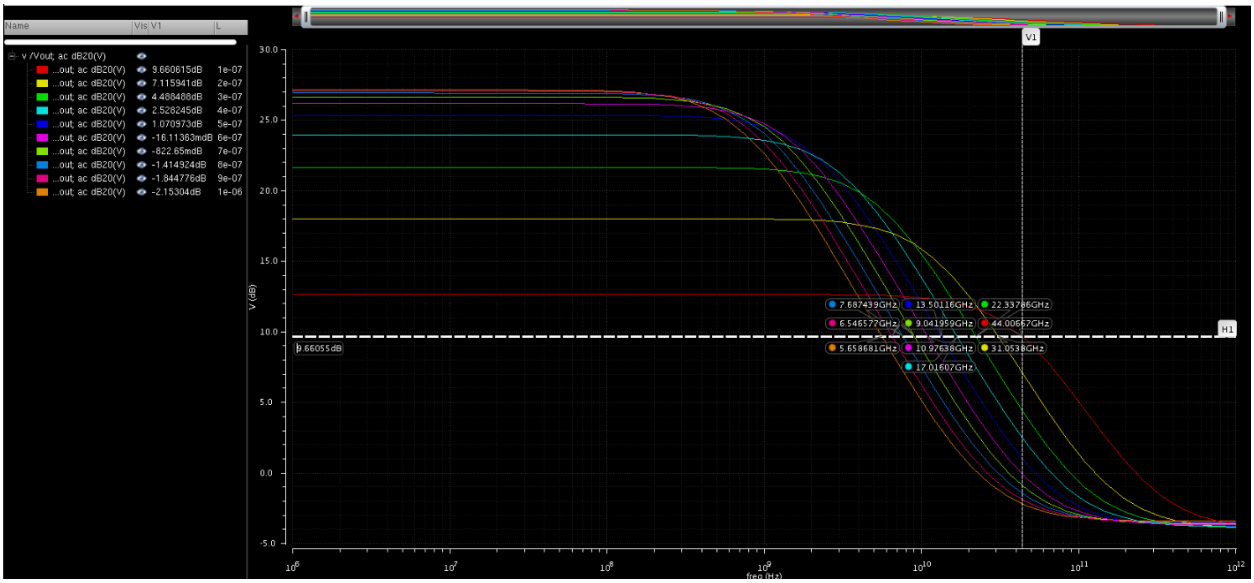
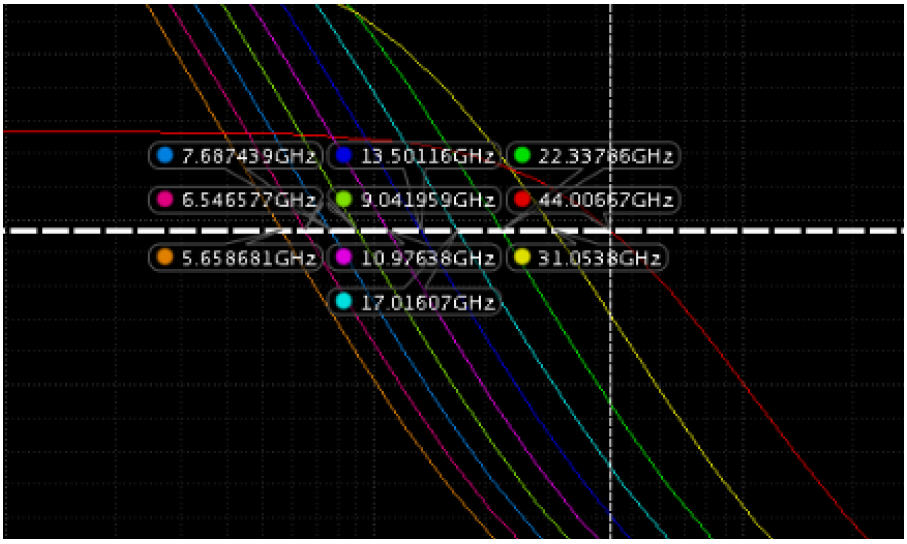


Figure 8. NMOS Length Design. Zoom on frequency bounds.

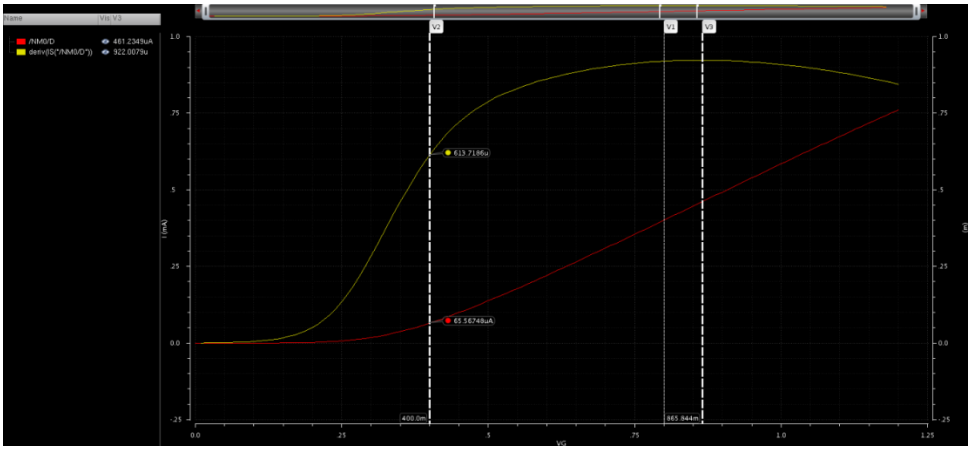


We want to design for high speed therefore we will pick the smallest transistor possible. In our test bench that would be 100nm. With this parameter chosen we can now go back to equation (3.6) and choose the appropriate gate biasing for our 100nm length NMOS transistor.

iii) NMOS Biasing Design Continued:

Now we have picked a certain length for our NMOS it's time to design the biasing voltage. From our equation (3.6) we know our V_{G1} has to be above 0.4V and below 0.8V, and we know $NMOS_{M1:L}$ = 100nm so we can do a DC sweep of V_{GS1} and look for an optimal value of V_{G1} that would give us the largest g_{m1} possible. We still use the circuit from Figure 5 and this is our output

Figure 9. Sweep of V_{GS}, with bounds 0.4V to 0.8V



We can see that the maximum is actually beyond our 0.8 V bound therefore we can only pick the value that has the highest g_m within our bounds, which occurs at 0.8 V.

From this result we can pick $V_{G1} = V_{G2} = 0.8V$. We want the pair to be perfectly matched therefore we pick the same length over both M1 and M2 NMOS transistors.

iv) Current Design:

$$\frac{I_{SS}}{2} = \frac{K}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (3.11)$$

$$V_{GS} - V_{th} = K\frac{W}{L}\sqrt{\frac{I_{SS}}{K\frac{W}{L}}} \quad (3.12)$$

$$g_m = \sqrt{K\frac{W}{L}I_{SS}} \quad (3.13)$$

Equation (3.11) is the current through a NMOS in saturation. In (3.12) we take square root of (3.11) and isolate. In (3.13) we place (3.12) into the derivative of

$$g_{m} = \frac{\partial I_{SS}}{\partial V_{GS}} \quad (3.14)$$

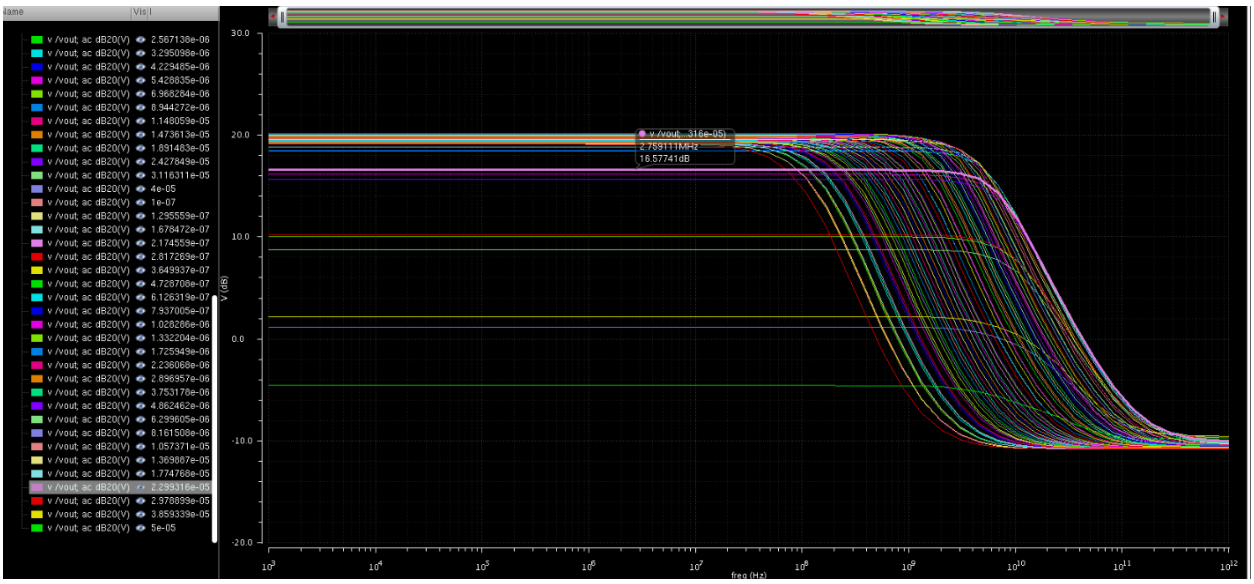
We see from (3.13) that g_m is proportional to $\sqrt{I_{SS}}$ and $\sqrt{W}$ and inversely proportional to $\sqrt{\frac{1}{L}}$.

As well as we increase current the voltage drop across our PMOS transistor (M4 and M3) would have to increase since

$$\frac{\boldsymbol{I_{SS}}}{2} = \frac{k_p'}{2}\frac{W}{L}\left(\boldsymbol{V_{SG}} - |V_{tp}|\right)^2 \quad (3.15)$$

In this equation if we keep increasing current I_{SS} - V_{SG} must also increase - since $V_S = V_{DD}$, V_G will have to go down. Since the circuit is symmetric $V_{G3,G4} = V_{D1,D2}$ and eventually V_D of the NMOS will go low enough for the transistor to leave saturation and enter triode region, at that point the circuit will break - we call this I_{SSMAX}. For our final circuit design this is about 40 uA. The following graph will show I_{SSMAX}, one can observe as I_{SS} increases beyond a certain threshold gain starts to drop; eventually it goes below 0 dB.

Figure 10. I_{SSMAX} exploration. I_{SS} threshold.



There is also a bound on the minimum current, I_{SSMIN}. As current decreases the gain also goes down, according to equation (3.13). The overall gain of the circuit cannot drop below unity, this also breaks our circuit and we call this I_{SSMIN}.

v) NMOS Width Design:

The main purpose the NMOS is to provide current gain. But since the gain of a single transistor is

$$A_v = r_{ds} \times g_m \quad (3.16)$$

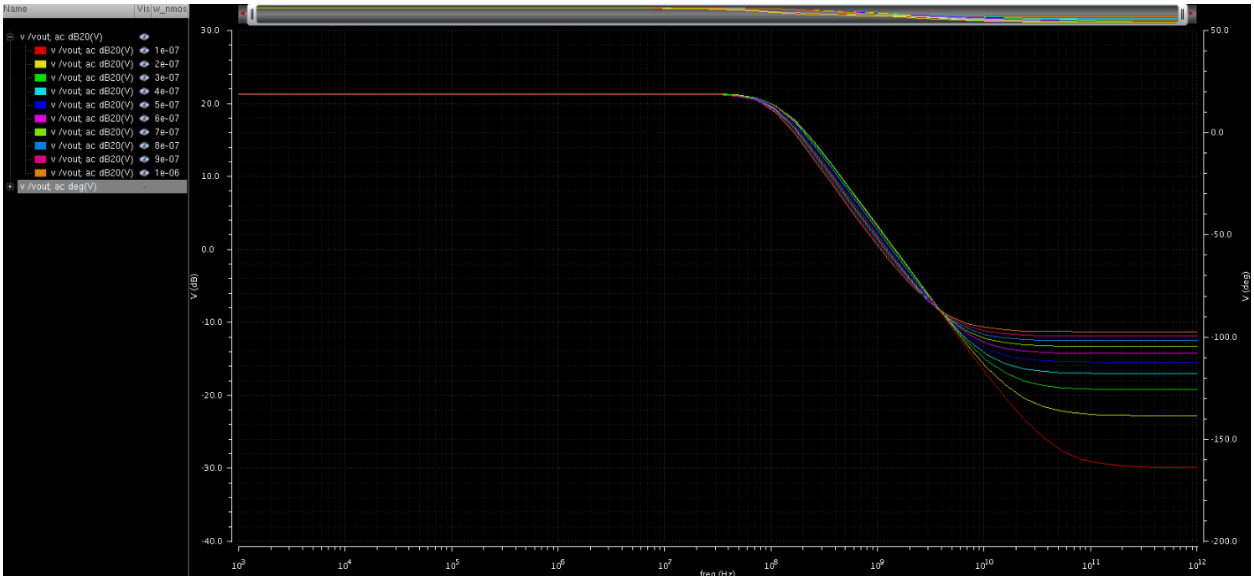
And according to equation (3.8) we see that increasing the width of the transistor *increases* g_m but decreases r_{ds}. Therefore we conclude that increasing or decreasing NMOS width has no effect on the overall gain of our circuit.

To pass a greater current through the transistor, increasing width balances the general current equation of a MOS in saturation (3.11). Increasing current and width *at the same time* will balance the equation. We can say

$$I_{SS} \propto W_{NMOS} \quad (3.17)$$

From this Cadence simulation we can see that increasing width has no effect on our overall gain. The width of the NMOS was therefore chosen to accommodate the V_{GS} value required

Figure 11. NMOS Width Design. Width sweep vs Frequency.



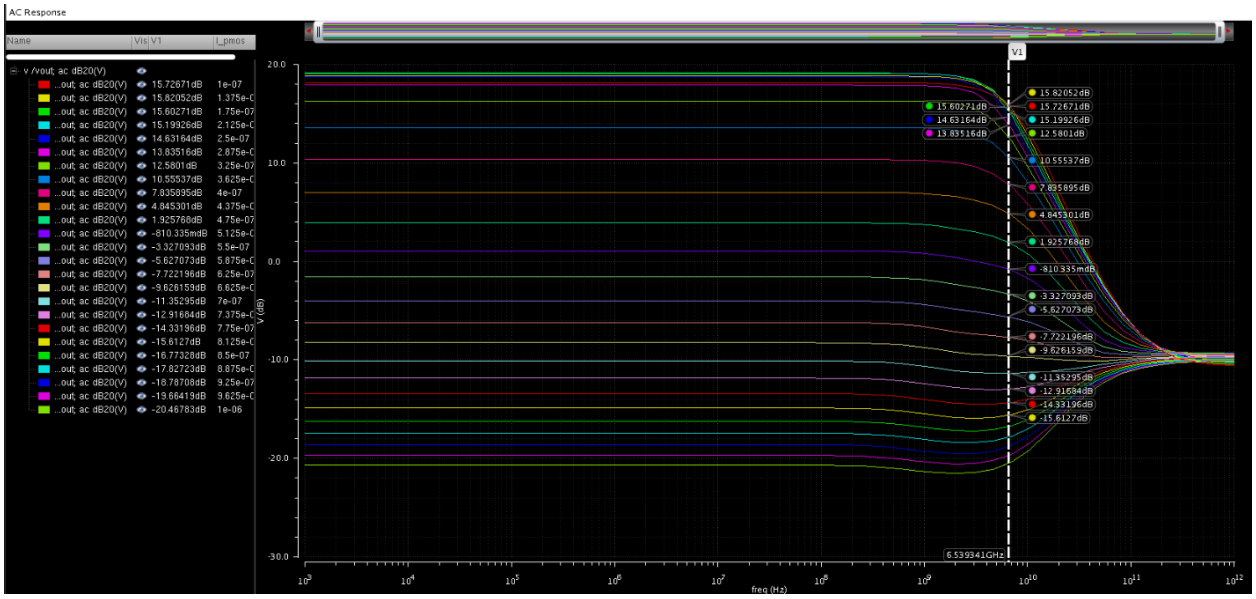
vi) PMOS Design:

The PMOS current mirror is acting as an active load for our amplifier's NMOS transistors. It copies the current from one branch to the other to deliver two times the differential current $2i_d$. We therefore want our PMOS to be able to respond to our fast NMOS design.

We know from small signal analysis that the resistance of the top branch looking into the drain of the PMOS is $\frac{1}{g_{m3,4}}$. But how high do we want our g_m we can determine from simulation, keeping frequency as a top priority.

Using the same analogies as we did with the NMOS length design we will sweep to find an optimal value for the length. Again we assume that smaller length will lead to larger gain. This is verified by the following simulation in Cadence, and our design choice was 200nm of Length.

Figure 12. PMOS Length Design.



For the width of the PMOS the arguments are the same as the NMOS case, we cannot increase the circuit gain by increasing or decreasing W. W can be used to regulate the voltage V_{SG} and keep it within circuit design bounds (we are coming back to our power budget of 1 V distribution amongst the NMOS and PMOS transistors). From the following Cadence simulation we can see that the width of the PMOS doesn't affect gain and therefore we pick it according to our need of V_{SG}. As well we can see a slight improvement in frequency response with smaller widths, therefore we pick 200nm.

Figure 13. PMOS Width Design.

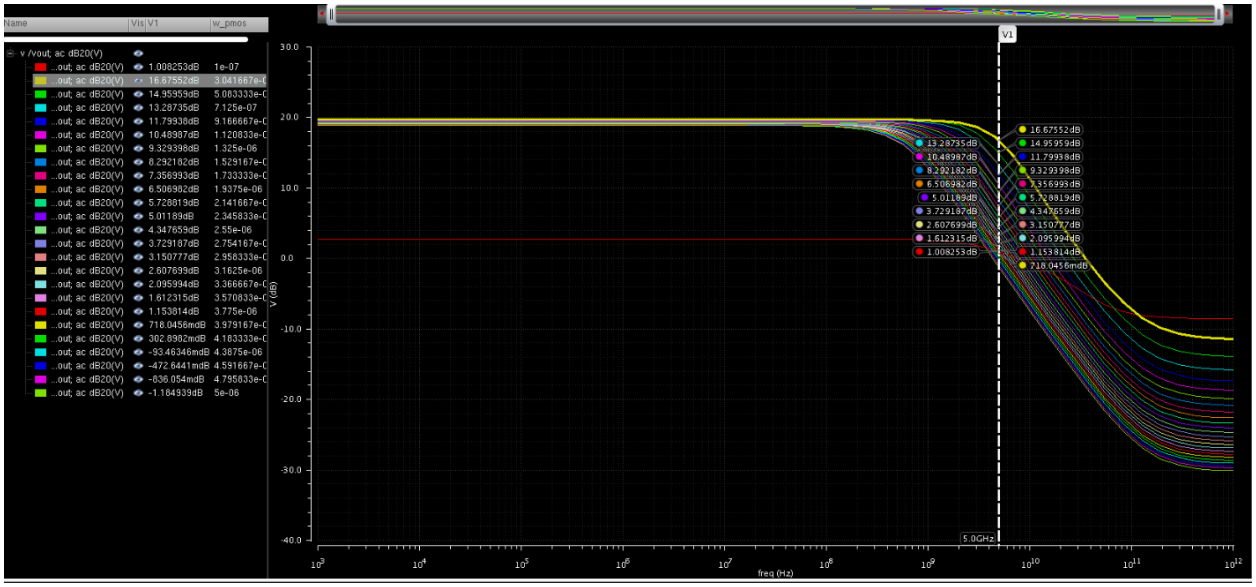
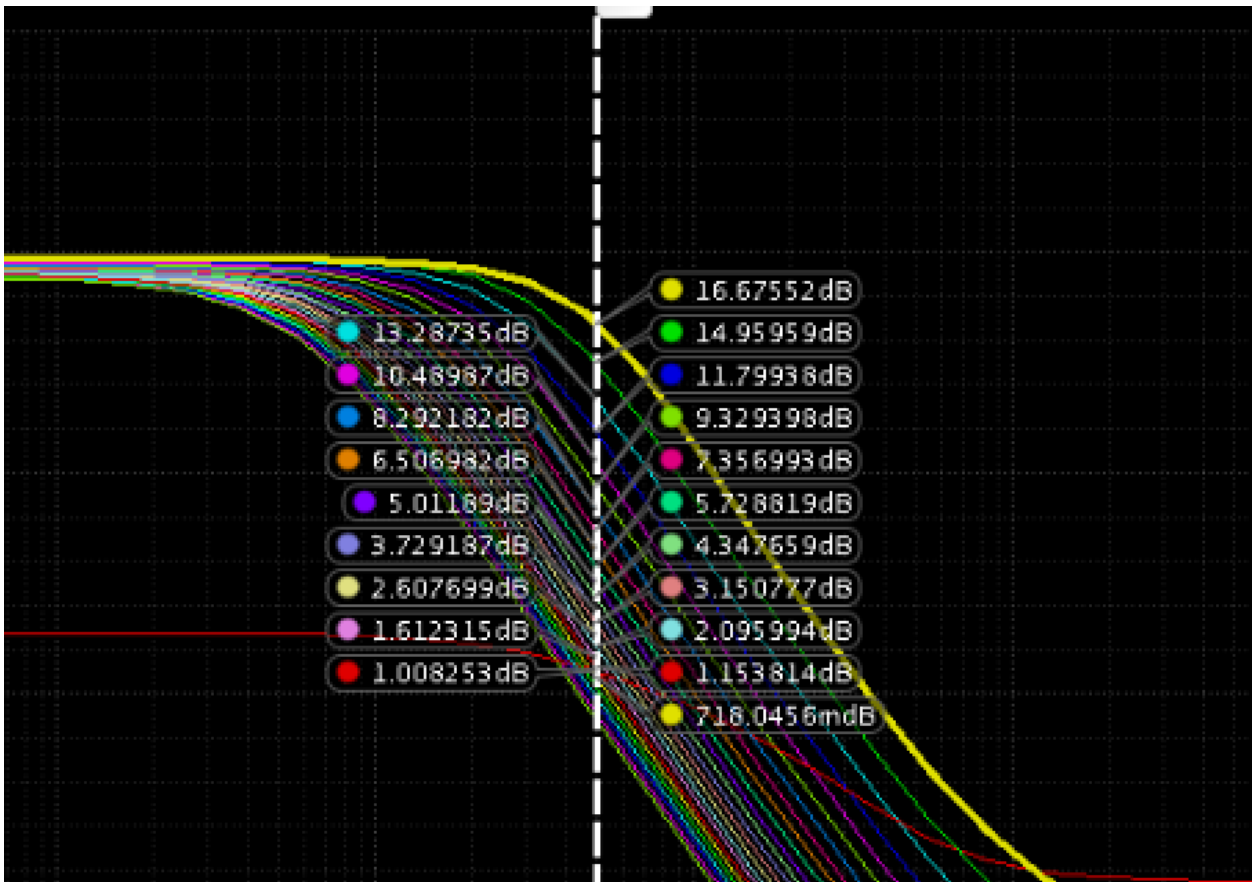


Figure 14. PMOS Width Design. Zoom in.



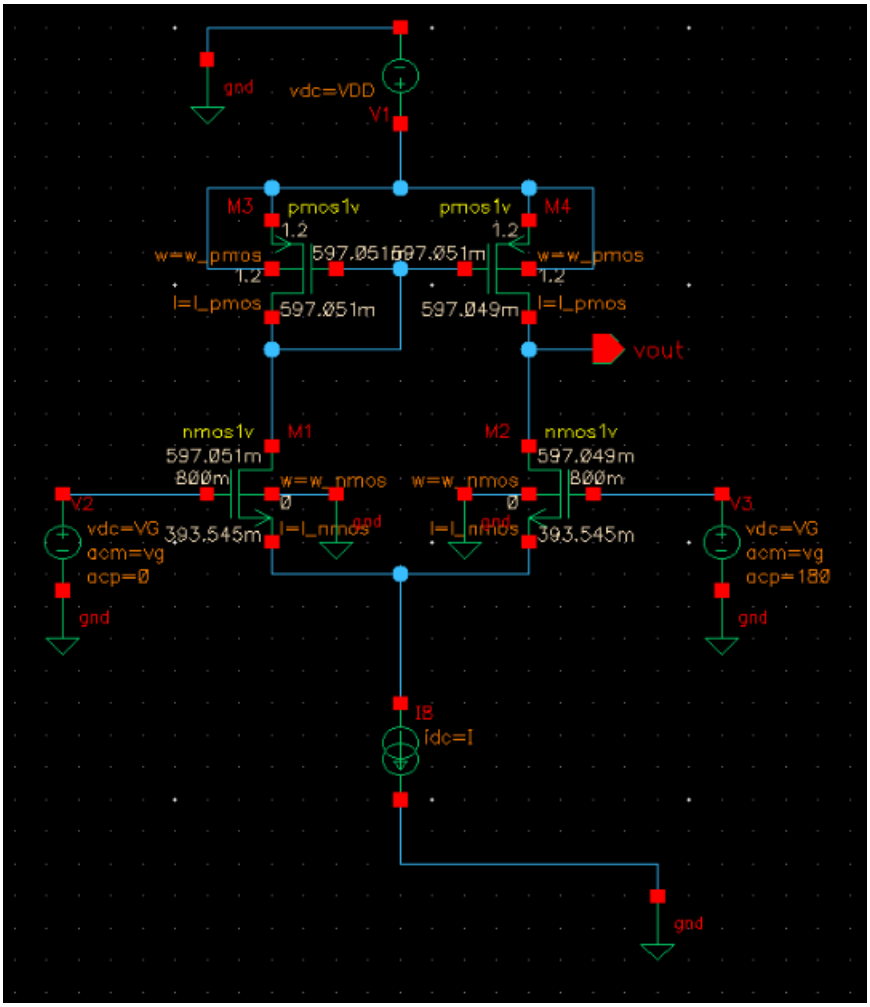
Conclusion:

After all the design steps we picked:

V_G = 0.8 V
L_{nmos} = 100 nm
W_{nmos} = 450 nm
L_{pmos} = 200 nm
W_{nmos} = 200 nm
I_{SS} = 15 uA

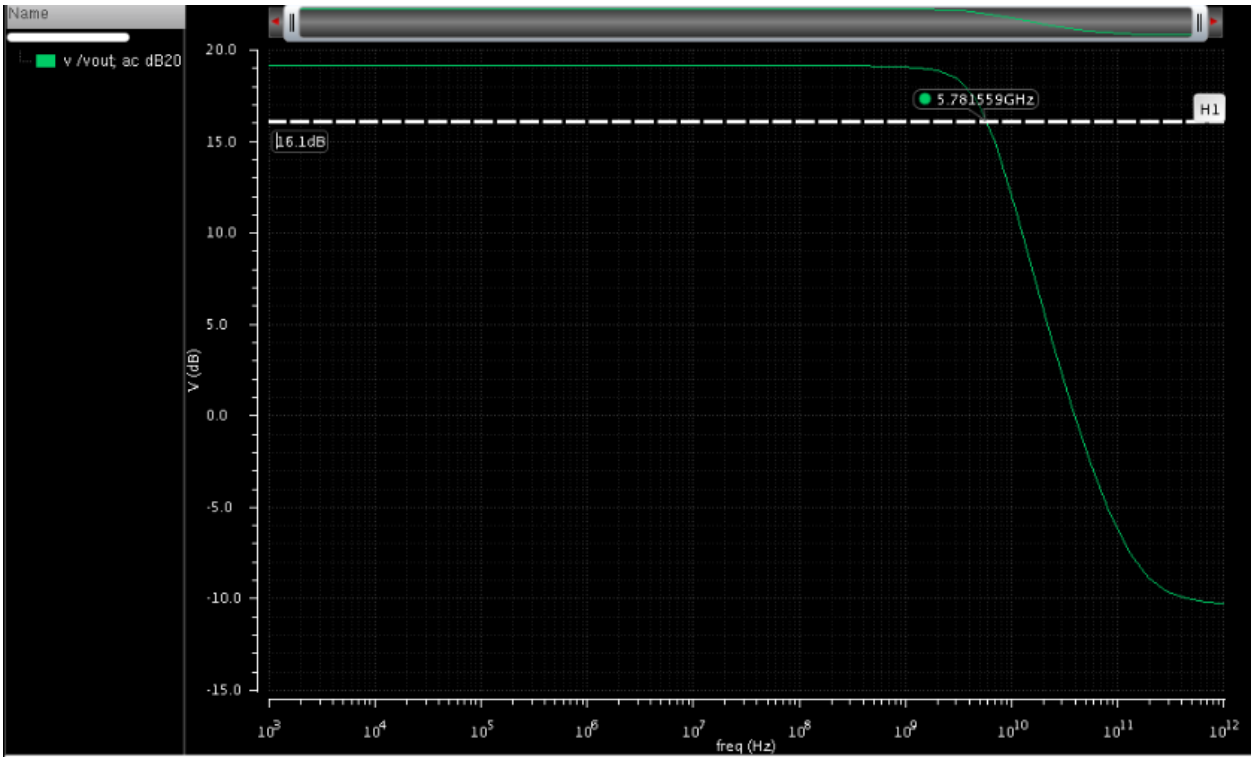
Here is a Cadence screenshot of the DC Operating points. Note we are using an ideal current source.

Figure 15. DC Operating Points in Circuit.



The overall gain of the circuit is 19.1 dB, with a 3-dB frequency of 5.78 GHz, and a phase margin of 76.5 degrees. CMRR is infinite, due to the use of our ideal current source.

Figure 16. 3-dB Plot. Cut-off at 5.78 GHz.



For the calculation of the phase margin we take the 0 dB of the magnitude plot and trace until we hit the phase. The phase margin is the difference between that number and 180 degrees. The following figure shows this process

Figure 17. Phase Margin calculation.

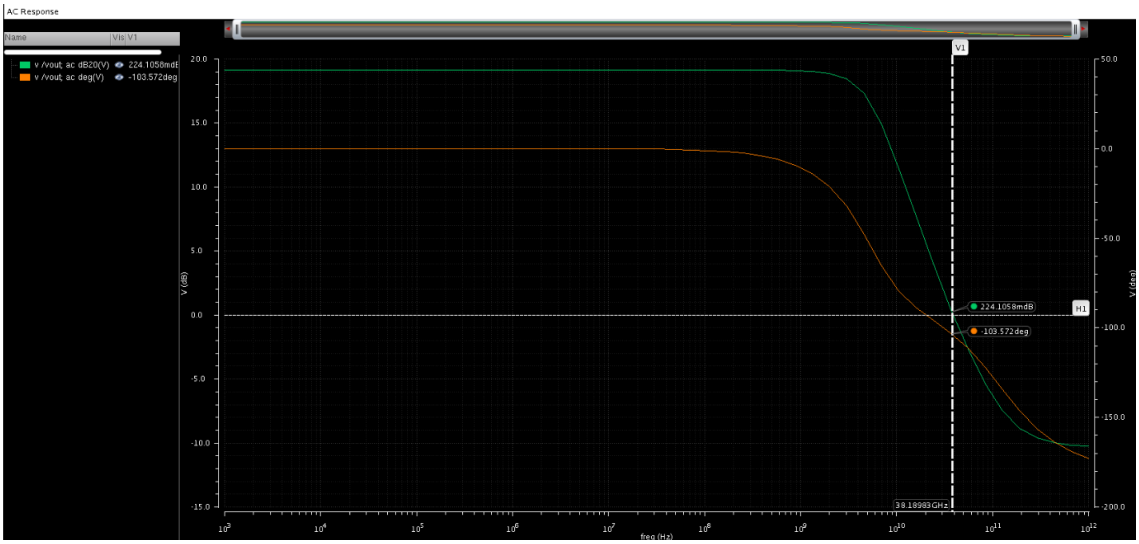


Figure 18. Phase margin. Zoomed in.

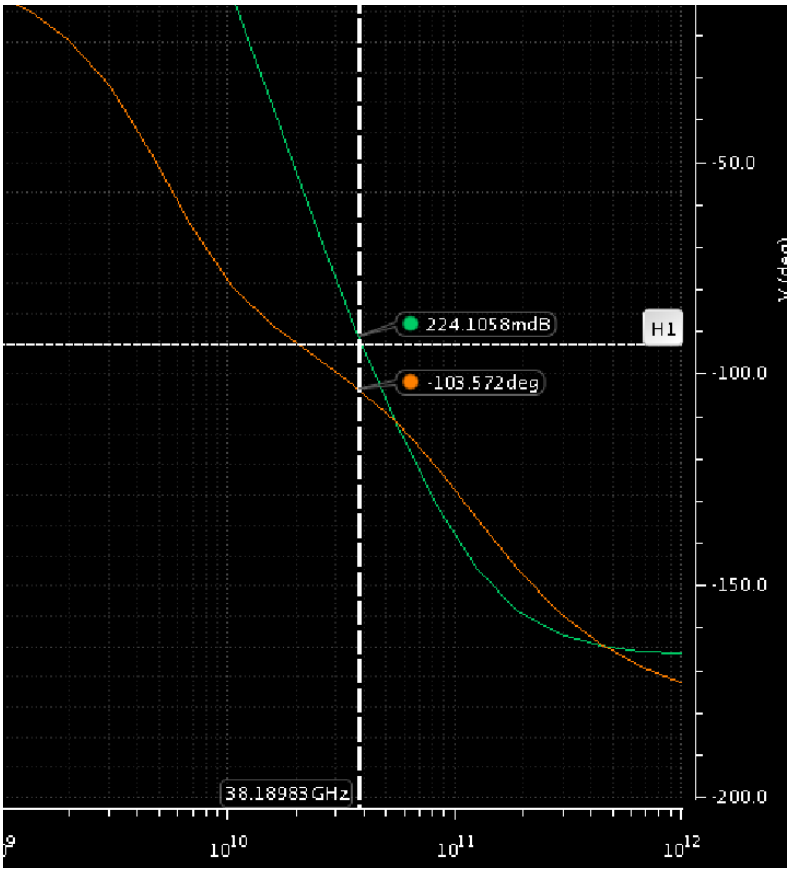
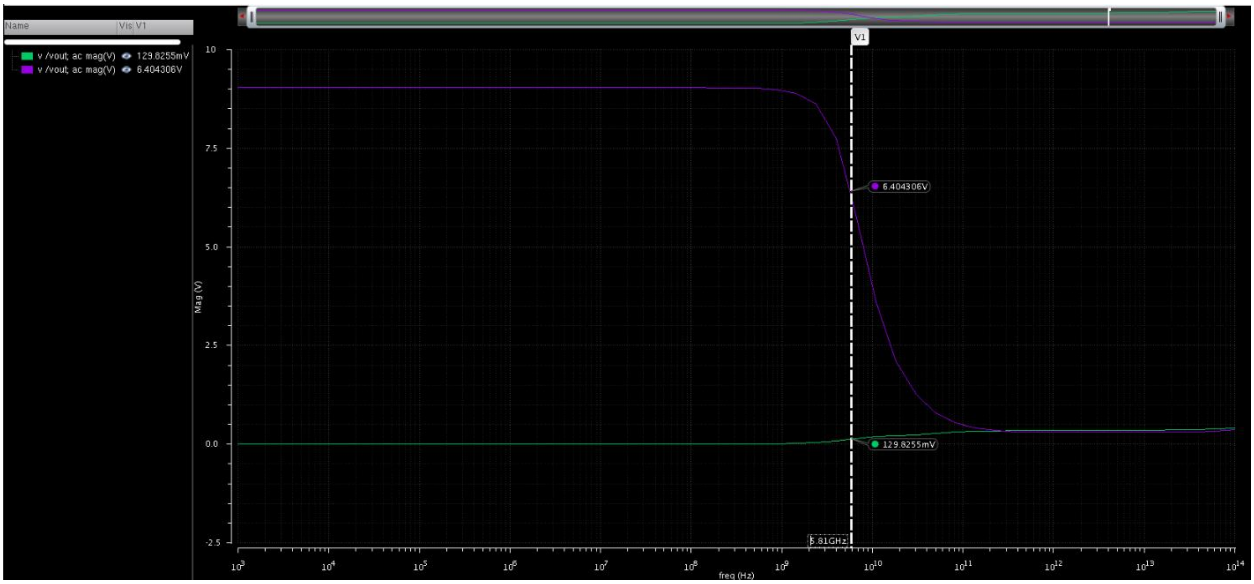


Figure 19. CMRR Calculation



We can see here that common mode gain is 0 for the bandwidth of our amplifier operation. This is due to the use of an ideal current source. The CMRR is then in turn infinite according to equation (2.9).

References

[1] The aspect ratios are not correct; figure is just to illustrate the MOS active-load configurations

[2] http://cc.ee.ntu.edu.tw/~lhlu/eecourses/Electronics2/Electronics_Ch7.pdf