Table of Contents

Figures:

Constraints and Theory:

The bootstrapped current source consists of three major components, a current source (M1 and M2), a current mirror (M3 and M4) and a starter circuit (M7 and M8). The current source has a logarithmic curve, where the current saturates. The current mirror copies the Input current to produce an Output current. The combination of these two circuit topologies results in two possible operating points (OP), Point A and Point B. Point A is our desired OP since the current is non-zero. The circuit has a natural tendency to leave OP B and move to OP A (since the gain at B is a lot higher than at A) but in practice and with small currents to leave OP B we need a starter circuit, which works only for a short time instance and then turns off.

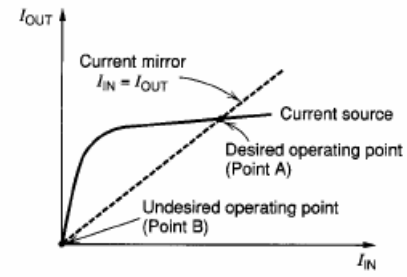


Figure 1. Circuit's current behaviour [1]

Time 0:

The system is in OP B. There is 0 current through $I_{1,2}$ and M2 is OFF. Since there is no current over the resistor at the source of M2, R_L the voltage at the source of M2 is ground (0 V). In order to turn ON M2 we need a voltage of **at least** V_{TH2} over it. Making the voltage $V_{G2} = V_{S7} = V_{TH2}$. In order to have M7 ON we need it's gate-source voltage greater than V_{TH7} . Therefore the total voltage V_{G7}, which we design, should be: $V_{G7} > V_{TH2} + V_{TH7}$.

Time 1:

Since M7 is now ON, and there is no current flowing through it $V_{D7} = V_{S7} = V_{G2} = V_{DD} > V_{TH2}$ and therefore M2 is ON.

Time 2:

Now since M2 is ON we have the current in this branch still being 0 and therefore the voltage on M4 source and gate (diode-connected PMOS transistor) is 0 as well. This will defiantly turn off the transistor since $V_{DD} > |V_{THP}|$.

Time 3:

M3 is now also being turned on, since its gate is connected with M4s and its source is at V_{DD} therefore the transistors must be on if M4 is ON. M1 is also turned on by the current flowing through R_L which will raise V_{gs1} high enough to be ON.

Time 4:

All are transistors are now running in saturation. Also we are at the desired OP since there are no other options (no more OPs), if current is flowing we are not at OP B. The problem now is that the starter circuit still injects unwanted current therefore we must turn M7 off. If we minimize the voltage $V_{GS7} < V_{TH7}$ we can achieve this:

$V_{GS7} = V_{G7} - V_{S7} \Rightarrow V_{S7}|_{T4} > V_{DD} - I_R R_R - V_{TH7}$ [Condition One]

From T1: $V_{DD} - I_R R_R > V_{TH2} + V_{TH7}$ [Condition Two]

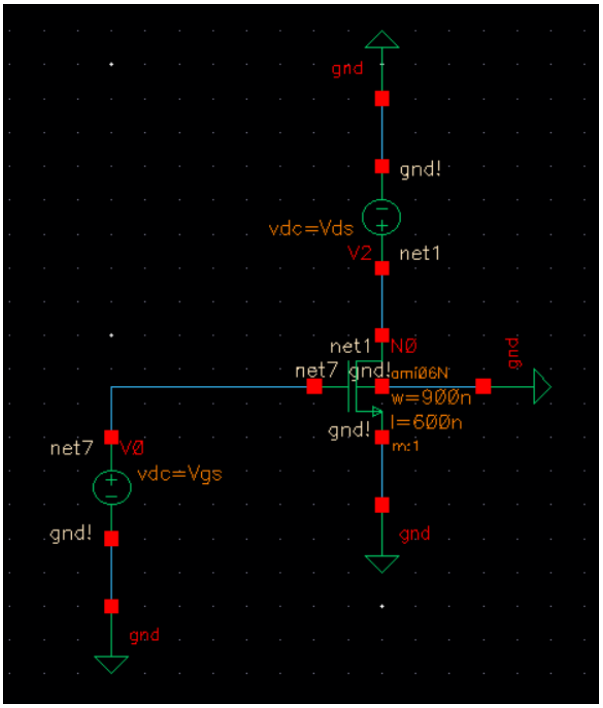
Let: $V_R = I_R R_R$

Overall: $V_{TH2} < V_R < V_{S7}|_{T4}$ [Bounds]

The Design:

We begin by finding the correct values of V_{TH2} and V_{TH7}. We can do this by building a simple circuit in Cadence consisting only of a NMOS transistor, V_{TH7}, and use a resistor in the source of the NMOS to find V_{TH2}, as well as R_L.

Figure 2. Finding V_{TH} in NMOS with V_{DS} and V_{GS} control, base is Grounded, no R_L Resistor.



The V_{TH} analysis consists of sweeping V_{GS}, at a constant V_{DS}, in order to generate the proper plots, they are showing when the transistor starts conducting *significant* current. We take the derivative of the plot (g_m) and then we draw a tangent to find the intersection with y=0 line of the curve. See the figures 3 and 4. For finding V_{TH2} we add another resistor, R_L

Figure 3. Analyzing V_{th7}. V_{GS} sweep, no R_L. Finding derivative (g_m) and tangent at max.

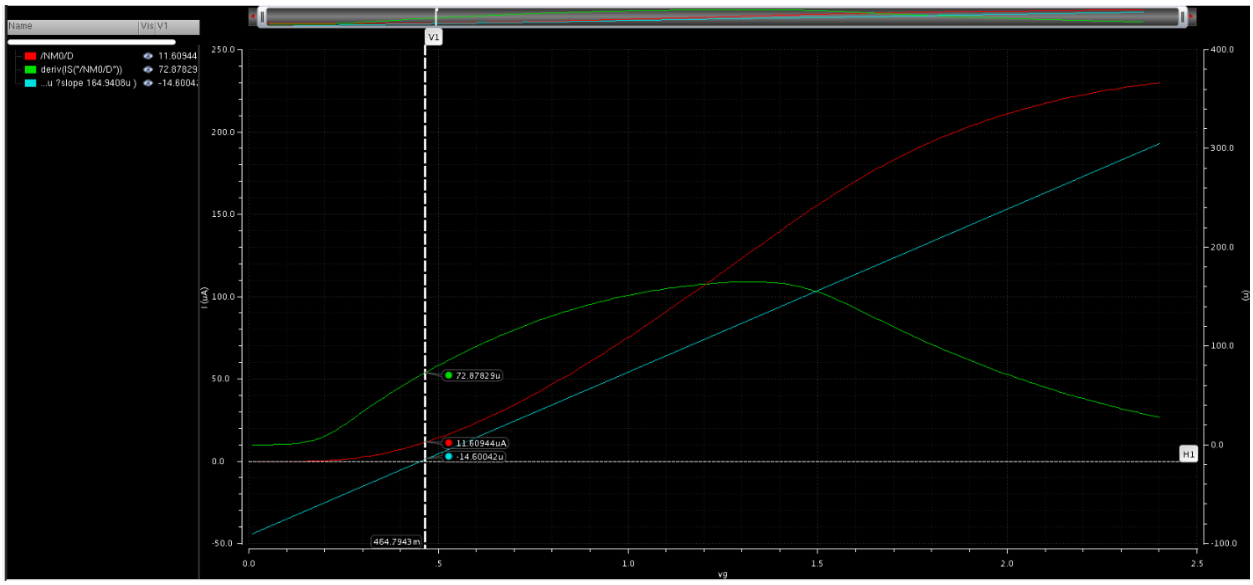


Figure 4. Analyzing V_{th2}. V_{GS} sweep, with R_L=250k[Ohm]. Finding derivative (g_m) and tangent at max.

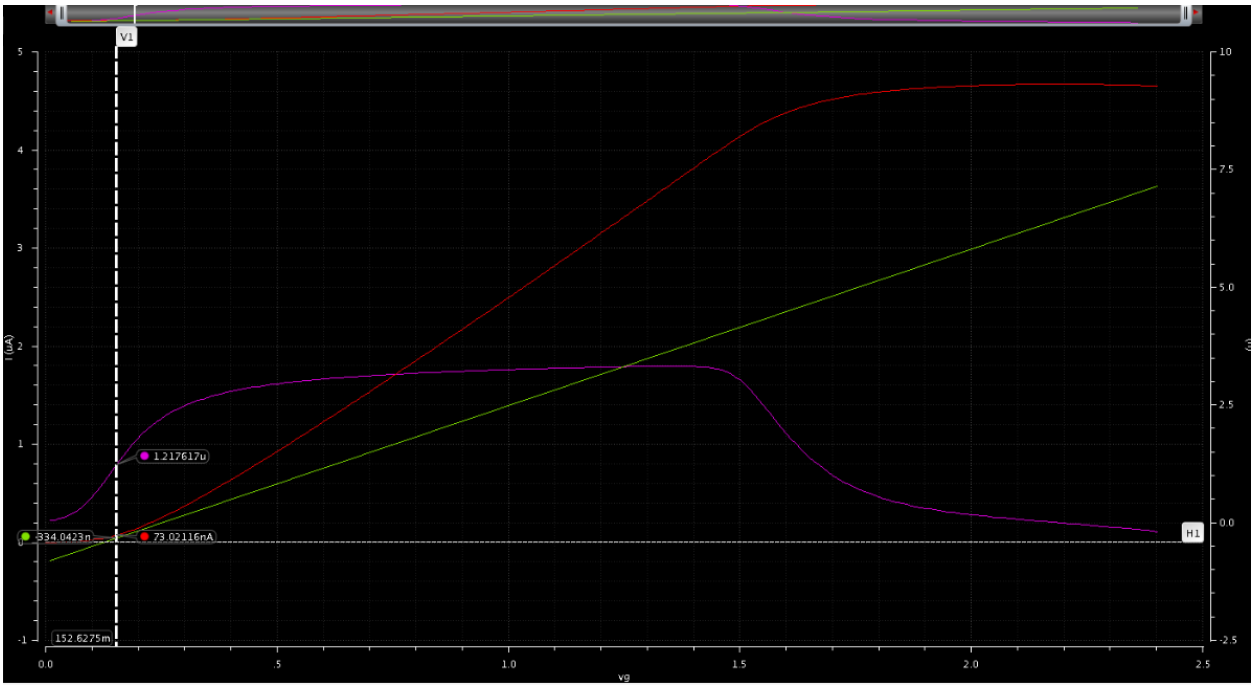
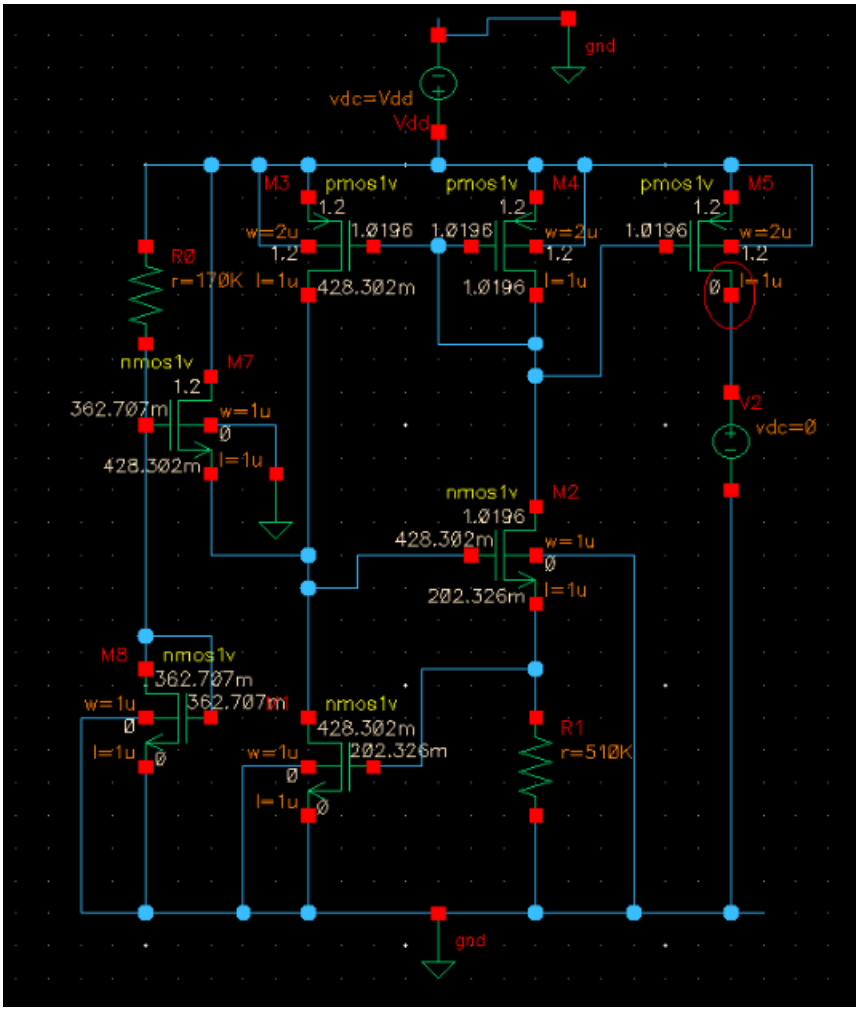


Figure 5. Cadence MOSFET Layout for Testing



To find the optimal solution we will do iteration over the equations we have derived, as well we can input the design into Cadence and then test the result.

<u>The Design Conditions:</u>

$V_{GS7} = V_{G7} - V_{S7} \Rightarrow V_{S7}|_{T4} > V_{DD} - I_R R_R - V_{TH7}$ [Condition One]

From T1: $V_{DD} - I_R R_R > V_{TH2} + V_{TH7}$ [Condition Two]

Overall: $V_{TH2} < V_R < V_{S7}|_{T4}$ [Bounds]

Iteration 1:

After we find the V_{TH} values we can start calculating according to our constraints. At first I used a resistor (R_R = 100K [Ohms]) with R_L = 200K [Ohms] this results in V_{th2} ~= 300m [V], V_{th7} ~= 460m [V] for the analysis with no resistor. For my design I wanted a current of 1u [A], we will need to adjust R_L to control this value.

From [Condition Two], $V_{G7} > V_{TH2} + V_{TH7}$. $V_{G7} > 760m$ [V]. $V_{G7} = V_{DD} – I_R R_R$, with our chosen values from [Condition One], V_{G7} = 1.1 [V]. From [Condition Two]: $V_{s7}|_{T4} > V_{DD} – I_R R_R – V_{th7}$ -> 0.64 [V].

$V_{th2} < V_R < V_{s7}|_{T4}$: 300m < 100m < 640m. This choice fails.

Iteration 2:

User R_R = 250k [Ohms]. V_R = 0.250 [V]. Picking an R_L = 550k [Ohms] V_{TH2} now equals 0.150 [V] while V_{TH7} = 0.460 [V] still. From Condition Two again: $V_{S7}|_{T4} > V_{DD} – I_R R_R – V_{TH7}$ -> 0.190 [V].

$V_{th2} < V_R < V_{s7}|_{T4}$: 150m < 250m < 490m. This choice is suitable.

Note: at this choice of R_R leads to a good current at 1.25 V_{DC} 1.03 uA, but experimentally with a value of 255k [Omhs] at 1.25 V_{DC} 1.01 uA. We can continue iterating until we find an optimal solution but this value might serve our purpose. See figure 5.

Note: Current is controlled by the R_L resistor which controls the V_{S2} and V_{G1} voltages of M1 and M2 transistors in our current source. The relationship is inversely proportional: an increase in R_L leads to a smaller current and a decrease in R_L leads to an increase in the current. Of course adjusting R_L also leads to changing of the threshold voltage, V_{TH2}, which raises our lower bound (see [Bounds]).

From observations R_R is controlling our upper bound and R_L is controlling current and lower bound.

Figure 6. Current output; the circuit from assignment 2.

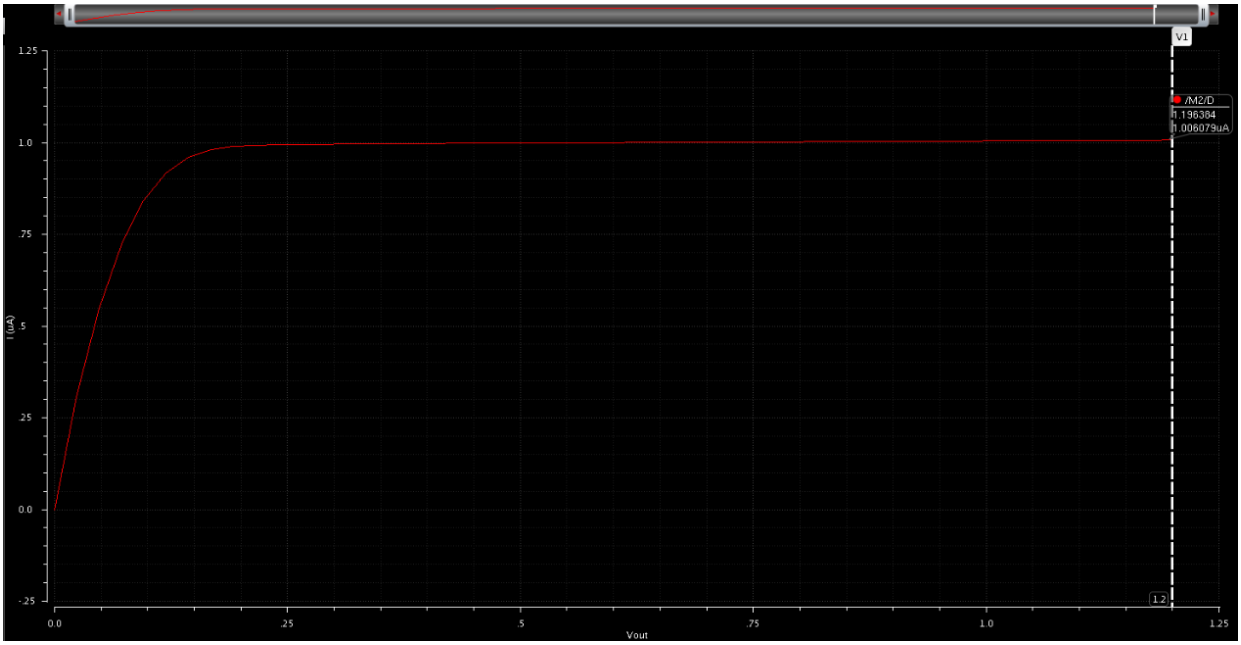
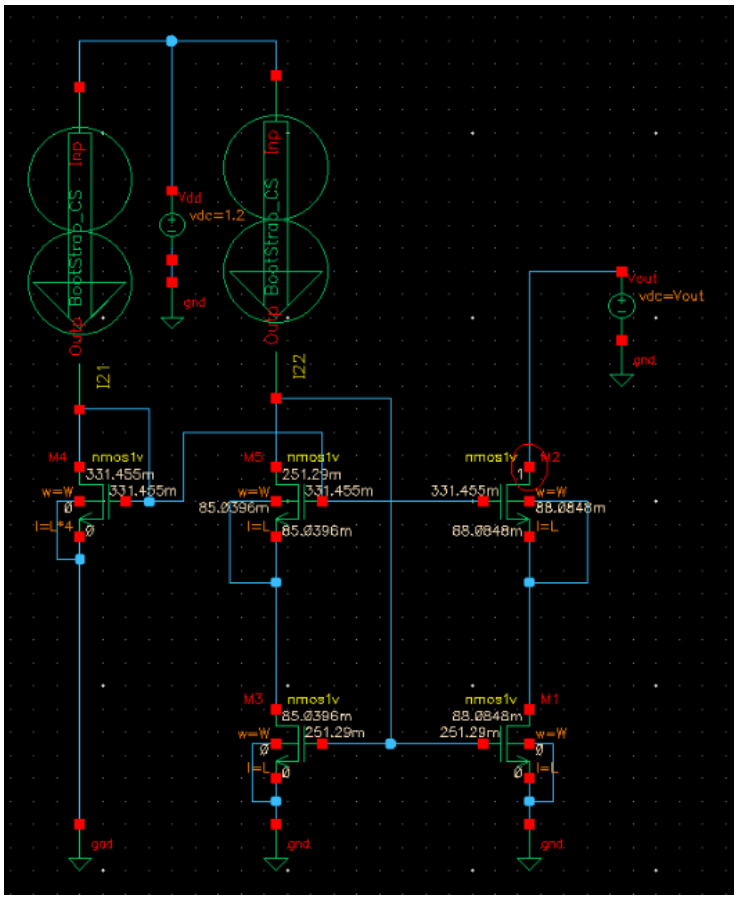


Figure 7. Bootstrapped current sources inserted in Assignment 2 circuit.



References:

1) Figure 4.37b) Analysis And Design of Analog Integrated Circuits, 4th ed., Gray Hurst Lewis Meyer