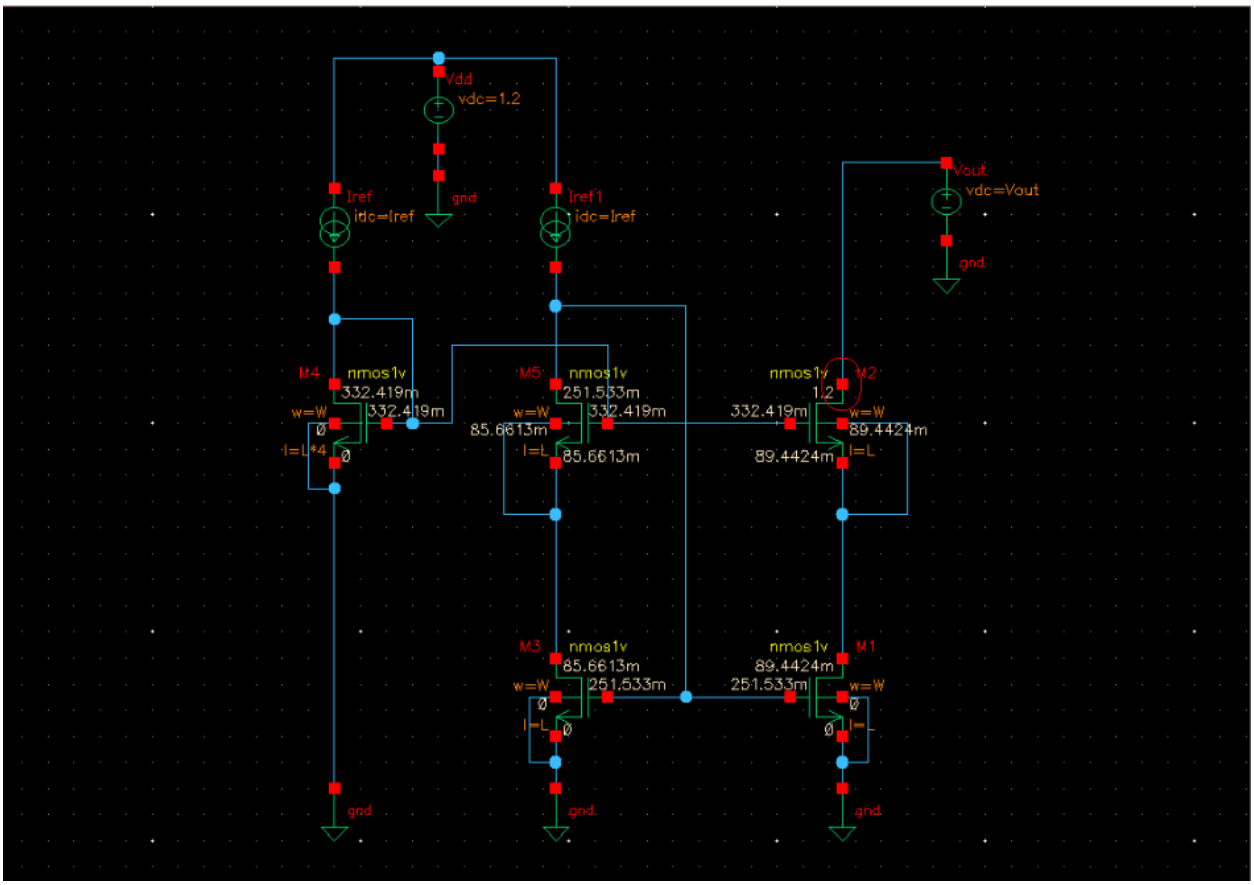
Figure 1. Circuit Picture [Improved High-Swing Cascode Current Sink]



Circuit Analysis:

Evolution:

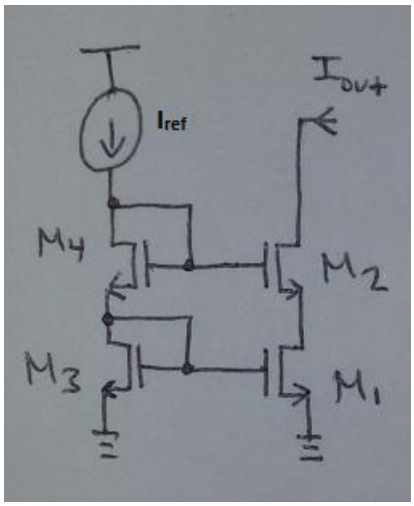
In class in an attempt to create a current sink we began by using a single NMOS with a biasing Vg, provided by a diode-connected transistor (Gate and Drain are tied). As shown in our first lab this has certain problems mainly the CLM effect, as the channel Length got smaller.

In order to combat the increase in CLM effect, we tried adding a Passive Resistor in series with a single transistor, at the source terminal. Rout was now increased to Ro = gm * Rds * R. This increase had an undesired voltage drop across the Resistor which consumed power and increased transistor source voltage. We then realized that we need to increase Rac not Rdc.

Next we replace the Passive Resistor with an Active Resistor (a diode-connected NMOS transistor). This is supposed to add AC Resistance, but after the analysis we know that diode-connected transistors have Rout ~= 1 / gm, so in all we actually made Ro ~= Rds, which is just the resistance of a single transistor – we again failed.

The next step was to bias the current sink transistor(M2) and the transistor that increases Rout(M1). Here we bias it using two diode-connected NMOS transistors. Now the problem becomes that the voltage on the gate of the sink (M2) is 2 Von + 2 Vth, and Vmin becomes 2Von + Vth. We must offset this Vth by splitting up the biasing transistors (M4 and M3) into two branches, each containing Iref (reference current).

Figure 2.Diode-Connected Biasing Circuit, V_{th} Offset to be removed

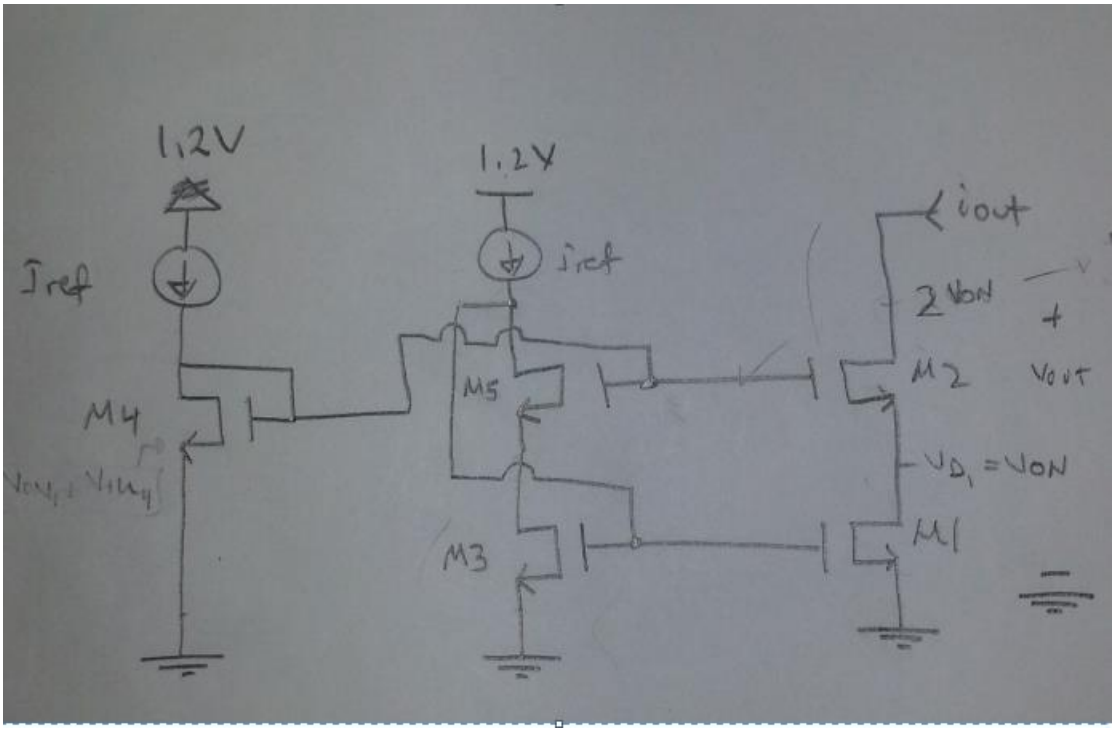


Finally to reduce CML at M3 we add a final transistor M5. We now go into detailed circuit analysis of our schematic; we focus on different transistors (M1 – M5):

Analysis:

The two main driving forces in our overall design are increase of Rout (decrease CML effect) and minimize Vmin (there shouldn't be a high required minimum voltage across a current supply for it to conduct). So we begin our analysis at M1 since we are looking to minimize Vmin (across M1 and M2).

Figure 3. Hand-drawn schematic of the High-Swing Cascode Sink to be Analyzed



M1:

Solve for Von. We require Von across Vds_1 since by definition this is the smallest possible voltage across a transistors in order for it to operate in Saturation, and that is exactly what we require, since changes in Vout should not change the current in a current source (saturation). From here we also derive the Gate voltage, Vg_1 and Vg_3, required at those points.

$Von_1 = Vgs_1 – Vth_1$ $\quad\quad$ $Vs_1 = 0$ (gnd)

$Vg_1 = Vg_3 = Von_1 + Vth_1$

Here we get a value for the gate voltage to be provided by the Bias transistor M3 in order to have Von across Vds of M1.

M2:

In order to have the minimum value across our current sink, of 2Von, we require that the voltage across M2 is also Von. This will set a constraint on our Gate voltage, Vg_2.

$Von_2 = Vgs_2 – Vth_2$

$Von_2 = Vg_2 - Vs_2 – Vth_2$

$Vg_2 = Vg_5 = Vg_4 = 2\ Von_{1,2} + Vth_2$ Note: $Von_1 = Von_2$ since W/L and manufacture build

M4:

For this transistor we can modify it's aspect ratio. The saturation Vds for this transistor, since it is Drain and Gate tied, is equal to Von + Vth. With that logic Vd = Vg, but as a requirement by our current sink transistor M2 we need $Vg_2 = Vg_5 = Vg_4 = Von_{1,2} + Vth_2$.

$Von_4 + Vth = 2\ Von_2 + Vth$

$(2*I_{ref} / (C'ox * (W/L)_4))^{1/2} = 2 * (2*I_{ref} / (C'ox * (W/L)_2))^{1/2}$

$1 / (W/L)_4 = 4 / (W/L)_2$ Setting $W_2 = W_4$

$L_4 = 4*L_2$ Length of M4 must be 4 times length of the rest

M3:

The only unknown voltage is on the drain, Vd_3. By symmetry with M1 (same current and NMOS build) the voltage must be Von.

M5:

After inserting this transistor we must check whether it is On and if it's in saturation.

On Check:

$Vgs_5 => Vth$

$Vg_5 – Vs_5 => Vth$

$(2*Von + Vth) – (Von) => Vth$

$Von => 0$ Von must be greater than 0, therefore M5 is definitely ON.

Saturation Check:

$Vds_5 => Vgs_5 – Vth$

$Vd_5 – Vs_5 => Vg_5 – Vs_5 – Vth$

(Von + Vth) => (2*Von + Vth)

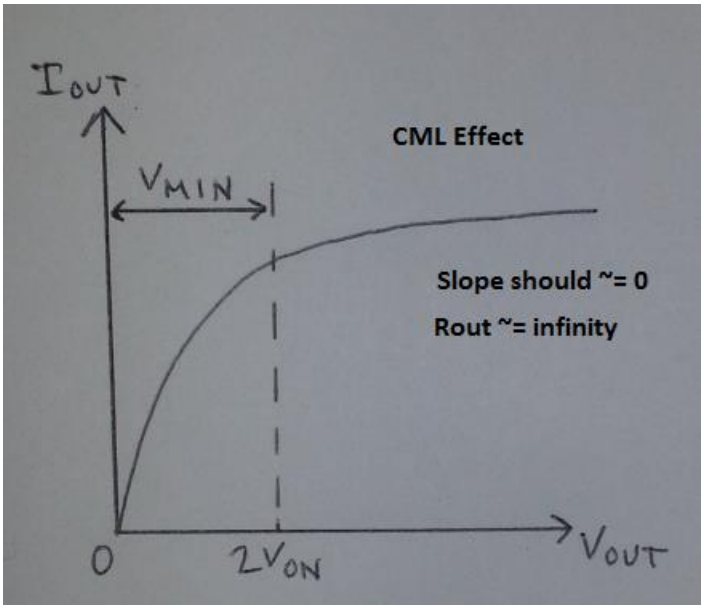
Vth => Von

Vth => $2*I_{ref} / (C'ox * (W/L)))^{1/2}$ This sets a constraint on W/L ratio and I_{ref}.

Overall:
All transistors must be ON and work in saturation. We are trying to reduce Vmin while we still have a constant current in saturation (i.e. minimize CML effect).

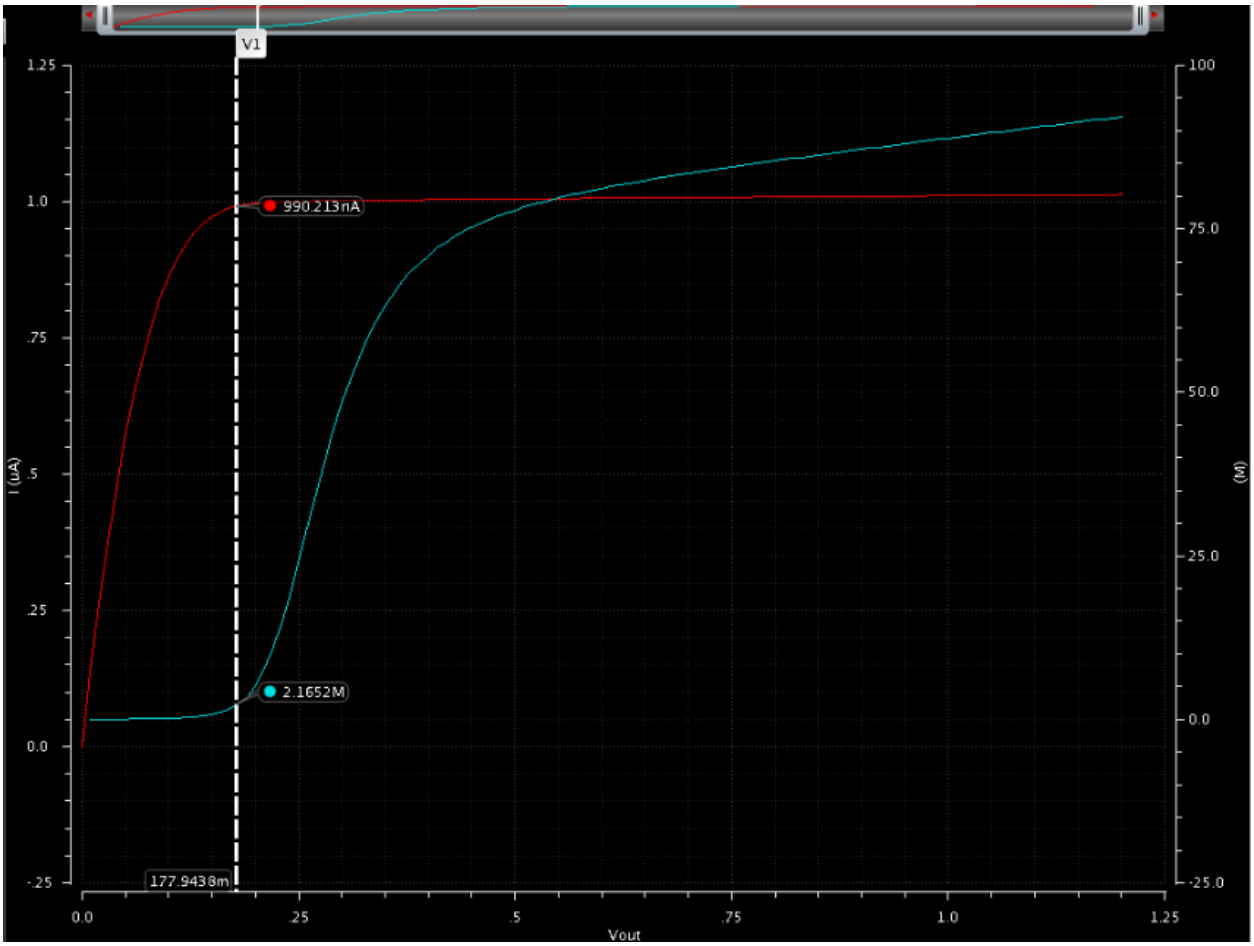
Some Assumptions:
Vth is approximately constant overall transistors, since we cancel it out many times, this assumptions must be made. Vth is temperature and technology related. M1, M2, M3, M5 should be manufactured from the same parameters and M4 should have 4x the Length of the rest. It is assumed the current sources provide constant current I_{ref}.

Figure 4. The parameters to be minimized. Vout vs Iout, with labels.



Cadence Analysis:

Figure 5. Graphing Vout vs Iout. Rout = 1 / (dI/dV) vs Vout. I_{ref} = 1um, W = 1um, L = 1um,



Data Table:

	W=1um	L=1um		betaeff	
Current	Vmin	Vth	gds	K* (W/L)	Rout
0.25uA	137.000uV	187.148mV	21.288n	314.256um	7.150M
1.0uA	175.000uV	191.388mV	78.589n	314.231um	2.165M
4.0uA	285.000mV	202.214mV	272.513n	312.058um	4.034n
	W = 1	L = 5		betaeff	
Current	Vmin	Vth	gds	K* (W/L)	Rout
0.25uA	194.074mV	166.823mV	4.4997n	61.2393um	9.855M
1.0uA	314.050mV	166.823mV	17.430n	60.859um	3.104M
	W = 5	L = 1		betaeff	
Current	Vmin	Vth	gds	K* (W/L)	Rout
0.25uA	100.000mV	183.962mV	22.100n	4.512um	5.100M
1.0uA	124.550mV	183.964mV	85.392n	1.584um	2.040M
	W = 1	L = 0.2		betaeff	
Current	Vmin	Vth	gds	K* (W/L)	Rout
0.25uA	Linear - CLM				
1.0uA	Irrelevant Data				

Here we have data for Vmin, from the graph Vout vs Iout (1% of Iout), Vth, gds and betaeff from the Cadence DC operating point window, and Rout from the inverse of the derivative of Iout vs Vout graph at Vmin. The Rout values are in Mohms (MΩ). Choices for these L and W are made after trying out some combinations. There is a tradeoff between Vmin and Rout, generally larger Rout leads to larger Vmin and vise-versa.

Figure 6. I_{ref} = 0.25 uA W = 1um L = 1um, Gm and Iout vs Vout.

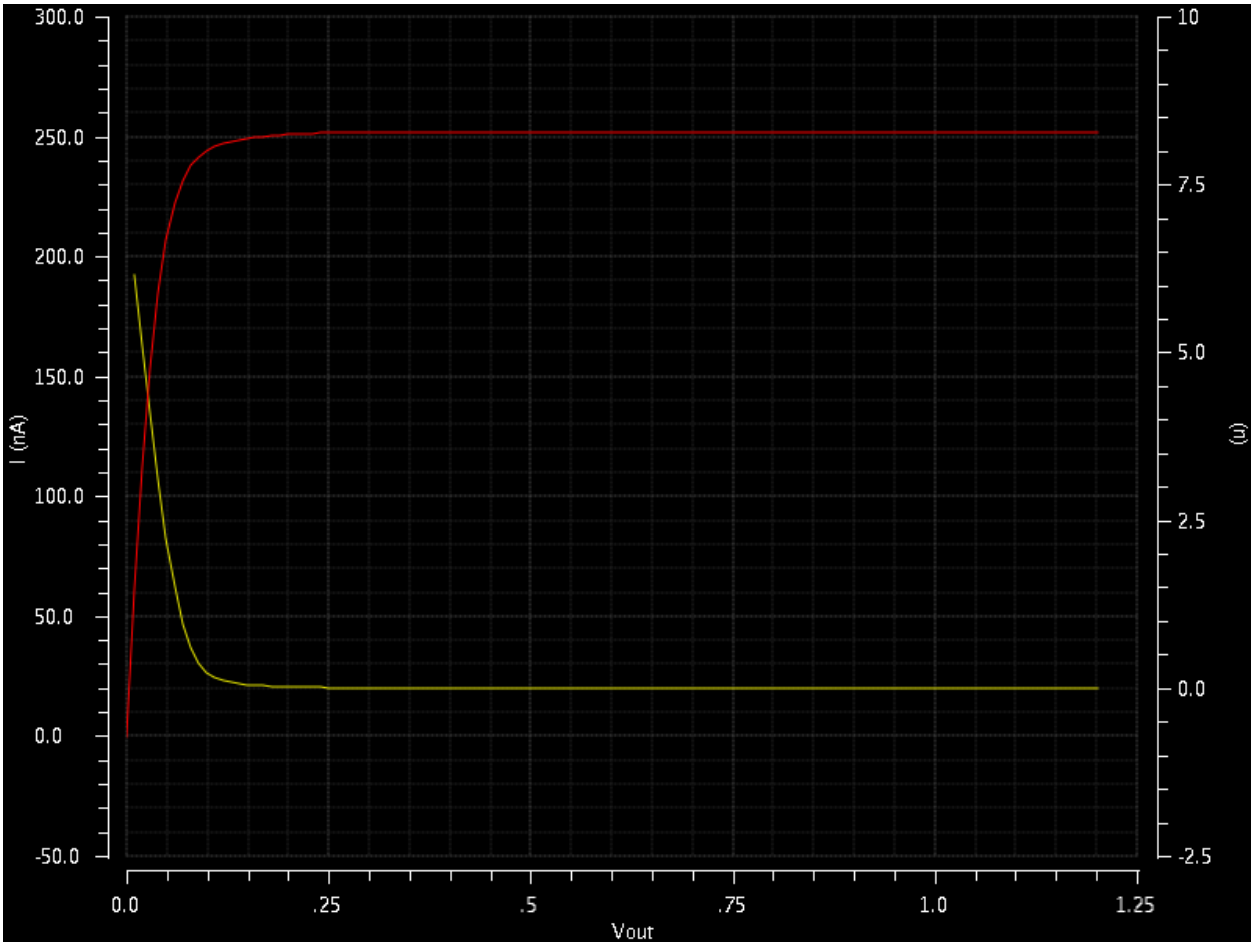


Figure 7. Another image of finding Rout. I_{ref} = 1uA W = 1um L = 1um