PAVAN BHARADWAJ MADHUVARSU

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SUMMARY

Hardware Design Engineer with 5+ years of experience in analog/mixed-signal IC design and PCB development. Proven track record delivering production-ready designs from concept through manufacturing. Deep expertise in signal/power integrity, multi-layer board layout, and full-stack power management from IC-level to system integration.

EDUCATION

M.S.E. in Computer Engineering (Electrical & Electronics) Aug 2023 – May 2025
Arizona State University, Tempe, AZ 3.52 GPA

B.Tech. in Electrical and Electronics Engineering 2013 – 2017
Vellore Institute of Technology (VIT University), Vellore, Tamil Nadu, India 8.48/10 CGPA

EXPERIENCE

Electrical Engineer, Heat kept LLC, Pheonix , Arizona **September 2025 – Present**

Consumer electronics hardware development (concurrent with graduate studies completion)

- Power Delivery Architecture: Designed complete heater-coil power path with MCU-driven PWM control (980Hz, 1.8-2A @ 18-28V) using back-to-back AOD4184A MOSFET H-bridge switching; integrated USB-C PD controller (IP2721) for dynamic voltage negotiation up to 28V.
- Power Tree Design: Architected downstream 3-rail power distribution (21-28V → 5V → 3.3V) using TI TPS54331 synchronous buck (5V/3A), TLV1117 LDO (3.3V/800mA), and BQ24072 Li-ion charger with load-step validation under 2A transients
- High-Speed Digital Design: Implemented MCU-to-LED display interface and UART/I^2C communication to PD controller with signal integrity optimization: 50Ω impedance-controlled traces, differential pair routing, ground return management.
- Design Ownership: Led schematic capture, PCB design reviews, and hardware bring-up; integrated debug infrastructure with strategic test points and LED indicators for power sequencing validation.

Hardware Design Engineer, Green Tiger Mobility Pvt. Ltd., Bangalore, Karnataka, India **March 2022- August 2023**

Vehicle Control Unit (VCU) product development from concept to production:

- High-Voltage Power Electronics: Designed EV/ICE mode-switching circuitry handling 12-60V rails using PMOS/NMOS power switches (IRFZ44N, IRF9540) with optocoupler isolation (PC817); integrated buck/boost converters for auxiliary power management.
- IoT Telemetry System: Architected connected vehicle platform with ESP32 (WiFi/BLE), u-blox NEO-6M GPS, SIM800L GSM, and Quectel EC200U 4G module; enabled real-time diagnostics streaming to AWS IoT Core with MQTT protocol and OTA firmware capabilities.
- PCB Design & DFM: Executed 4-layer board layout in Altium Designer for production volumes; collaborated cross functionally on component placement, thermal analysis, designed TP4056-based 3.7V Li-ion charging with CV/CC regulation.

Hardware Design Engineer, Jaidka power systems **December 2019 – June 2021**

- Engineered multi-layer PCB layouts for 3-wheeler EV control systems, optimizing routing for buck/boost power converters and ensuring signal integrity in automotive environments.
- Signal Integrity & Reliability: Implemented gate drive circuits with proper layout techniques (Kelvin connections, low-inductance loops); ensured signal integrity for CAN bus, analog sensing, and PWM signals in electrically noisy automotive environment.

Hardware Design Engineer, HCL Technologies Pvt. Ltd., Chennai, Tamil Nadu, India **August 2017 – November 2019**

- Schematic Design: Created circuit schematics in OrCAD Capture with custom component libraries symbols/footprints performed design rule checks, BOM validation, and design review coordination with electrical teams.
- Manufacturing Support: Generated Gerber/ODB++ files, assembly drawings, and fab notes; coordinated with CM partners on DFM feedback, achieving 95%+ first pass yield on production builds.

Technical projects

- Capless LDO Regulator: Designed fully on-chip PMOS pass device achieving 200mV dropout @ 50mA load, 2.8V±10mV line/load regulation (2.5-3.3V input), 69° phase margin with 100pF load cap, 80µA quiescent current, and <250mv overshoot/undershoot; implemented error amplifier, bandgap reference, and current-limit protection.
- Voltage-Mode Buck Converter: 3.3V→1.5V @ 1A with integrated PWM controller, Type-3 compensation network (optimized for 60° phase margin), custom gate driver with 20ns dead-time control, and soft-start sequencing; achieved 85% efficiency at full load.

- Bandgap Voltage Reference: 1.2V±10mV precision reference using sub-1V ΔVBE biasing and PTAT/CTAT current summing; validated across -40°C to 160°C and FF/SS/TT corner stability under ±10% supply variation (2.5V nominal).
- Folded Cascode Op-Amp: Two-stage design with 63.2dB DC gain, 33.2MHz GBW, 0.55mW power (2.5V supply), and 1921µm² layout; optimized input pair sizing, bias current distribution, and compensation capacitor for 65° phase margin.

Technical Skills

- Design Tools: Cadence Virtuoso (Schematic/Layout/ADE-L), Altium Designer, OrCAD Capture/Layout, KiCad.