```
module tb_digital_clock;

  logic clk = 0;
  logic rst=0;
  logic [5:0] sec;
  logic [5:0] min;

  // DUT
  digital_clock dut (
    .clk(clk),
    .rst(rst),
    .sec(sec),
    .min(min)
  );

  // Clock generation
  always #5 clk = ~clk;

  // Coverage: verify 59 => 0 transition
  covergroup sec_cg @(posedge clk);
    coverpoint sec {
      bins rollover = (59 => 0);
    }
  endgroup

  sec_cg cg = new();

  // Test sequence
  initial begin
$dumpfile("dump.vcd");
$dumpvars;
    rst = 1;
    #10 rst = 0;

    // Run long enough to see rollover
    repeat (130) begin
      @(posedge clk);
      cg.sample();
    end

    $display("DIGITAL CLOCK TEST COMPLETED");
    $finish;
  end

endmodule
```