# Lab #6: DRAM Row Buffer Management

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**Objective:** To understand the internals of DRAM row-buffer management

**Open-page row-buffer policy:**
Read latency can be either t-CAS on a row-buffer hit or (t-RP + t-RCD + t-CAS) on a row-buffer miss. This is better when memory request sequences show high access locality.

**Closed-page row-buffer policy:**
Read latency is (t-RCD + t-CAS). This is better when memory request sequences show low access locality, low request rates.

**Hybrid row-buffer policy:**
A timer is used to control the sense amplifiers. The timer is set to an initial value when a row is activated or re-accessed. If there's no buffer hit before the timer goes off, we switch to closed-page row-buffer policy. Else, we reset the timer.

**Adaptive-page management policy:**
A 4-bit saturation counter is used with a low-threshold value of 7 and high-threshold value of 12. Initially, the counter is set to a value of 10. When open-page row-buffer policy is followed, the counter is incremented on page-miss and unchanged on page-hit. When closed-page row-buffer policy is followed, the counter is decremented on page-hit and unchanged on page-miss.

**Observations:**

Open-page row-buffer policy:

Sum of execution times for all programs: 2961704405
Num reads merged: 2222
Num writes merged: 0
Number of aggressive precharges: 0

Closed-page row-buffer policy:

Sum of execution times for all programs: 2797864901
Num reads merged: 2098
Num writes merged: 0
Number of aggressive precharges: 23011541

Adaptive-page management policy:

Sum of execution times for all programs: 2892983406
Num reads merged: 2172
Num writes merged: 1
Number of aggressive precharges: 11274191

**Conclusion:**
According to the obtained stats for the policies by running the simulator the best policy is the closed-page row-buffer policy as the simulation cycles are low in closed-page row-buffer policy. This is for first address mapping.